

# Compal Confidential

## NCWGO/H0 Schematics Document

AMD S1g1 / RS780MN/ SB710

2009 / 06 / 24

LA-5481

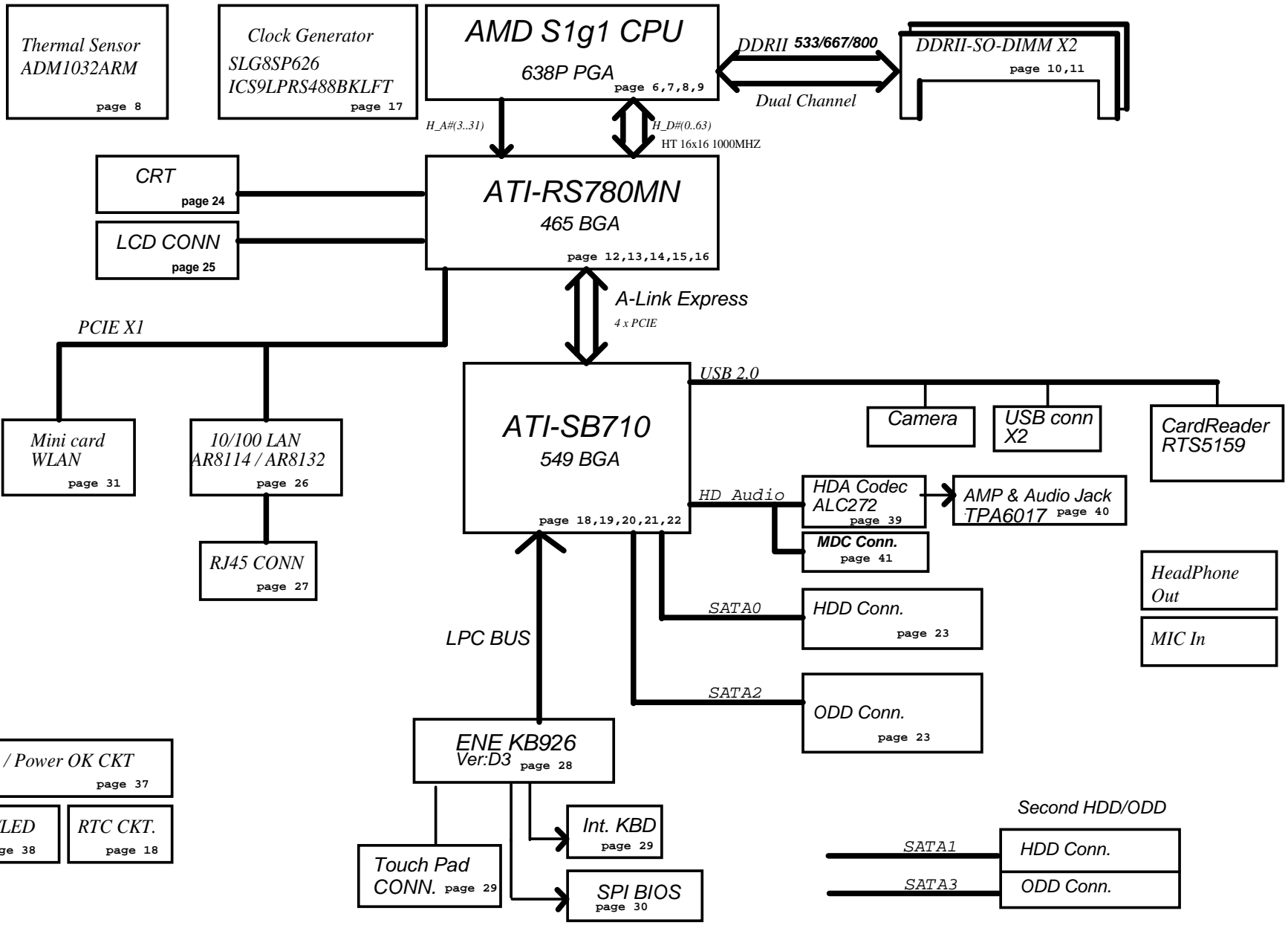
Rev:1.0

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Project Code: NCWG0/H0

File Name : LA-5481P



Power On/Off CKT / LID switch / Power OK CKT page 37

DC/DC Interface CKT. page 41

CIR/LED page 38

RTC CKT. page 18

Power Circuit DC/DC page 42-48

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### Voltage Rails

VIN	Adapter power supply (19V)			
B+	AC or battery power rail for power circuit.			
+CPU_CORE	Core voltage for CPU			
+0.9V	0.9V switched power rail for DDR terminator			
+1.2V_HT	1.2V switched power rail	ON	OFF	
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON		ON*
+1.8VS	1.8V switched power rail		OFF	
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

### External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

### EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b

### EC SM Bus2 address

### SB600 SM Bus 1 address

Device	Address	Device	Address
Clock Generator	1101 001Xb	New Card	
DDR DIMM0	1001 000Xb		
DDR DIMM2	1001 010Xb		
Wireless Lan			

### SB600 SM Bus 2 address

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

### Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

### BOARD ID Table

Board ID	PCB Revision
0	No Support VaryBright
1	
2	
3	Support VaryBright
4	
5	
6	
7	

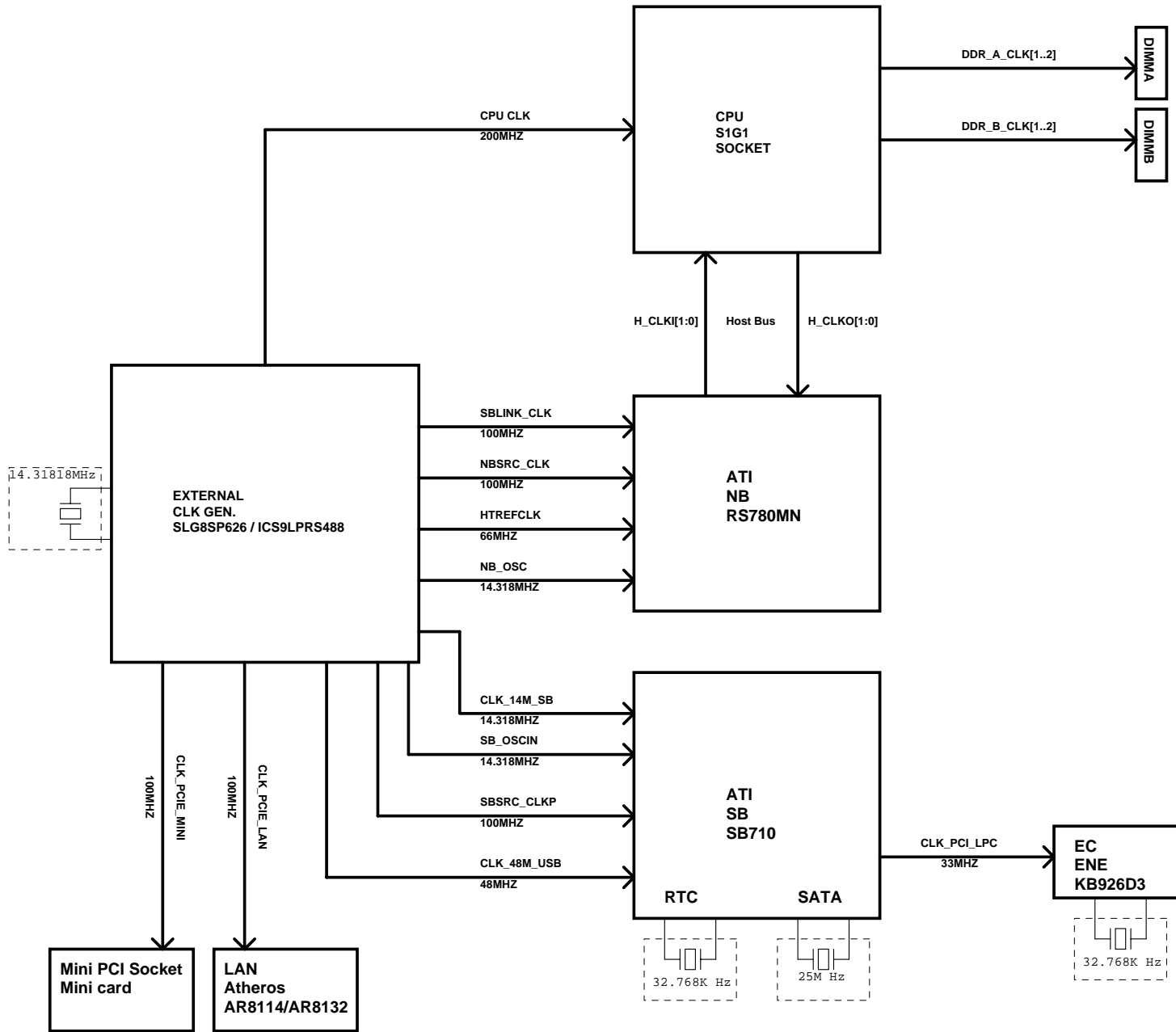
### BTO Option Table

BTO Item	BOM Structure
10/100 Lan	8114@
GIGA Lan	8132@
17" ID	17@
15" ID	15@
Support VaryBright	VARY@

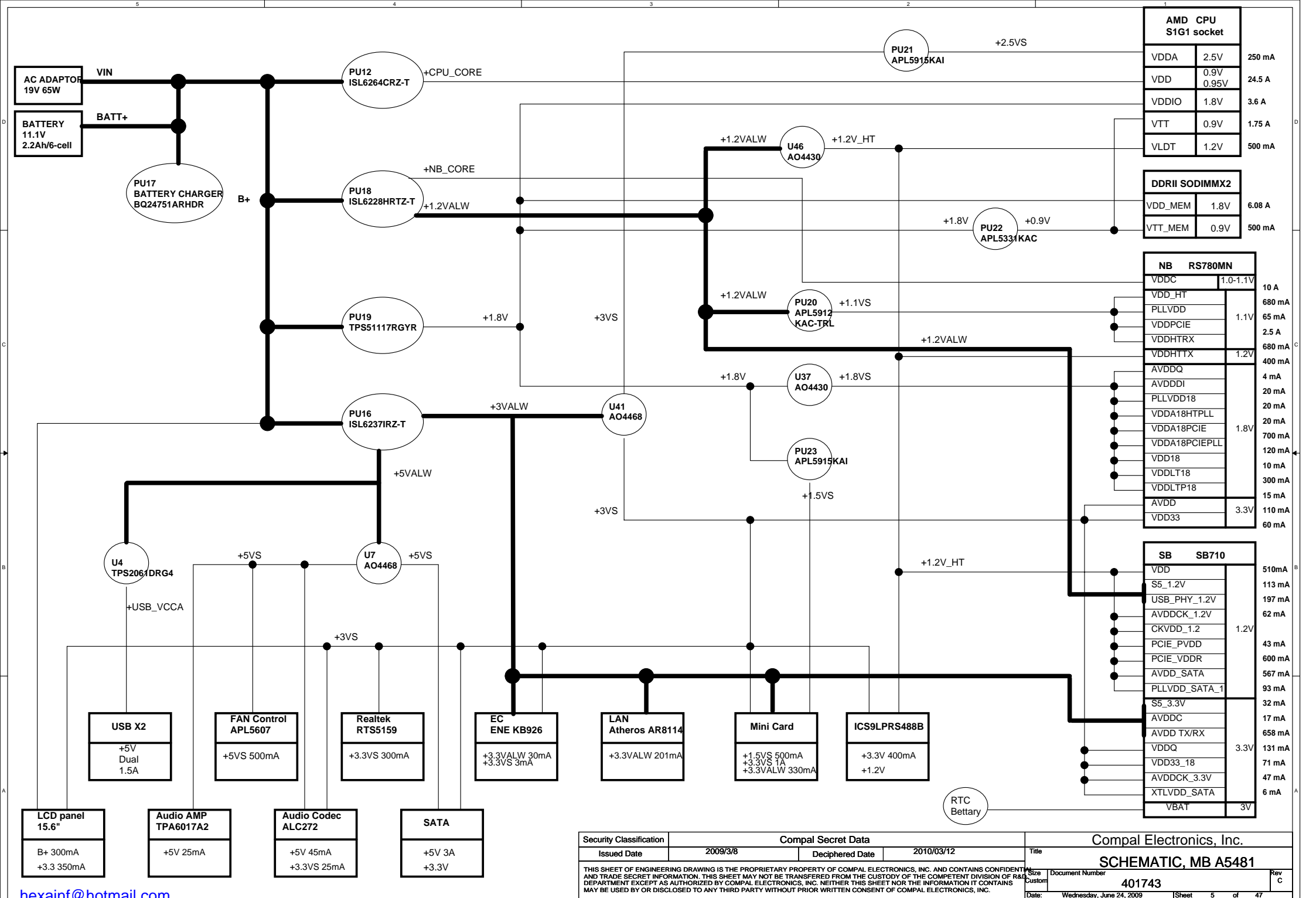
### PROJECT ID Table

SKU ID	SKU
0	NCWGO
1	
2	
3	NAL00
4	
5	
6	
7	NCWH0

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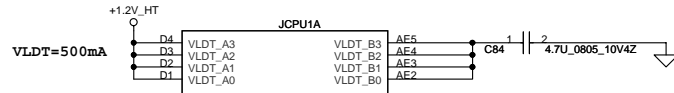


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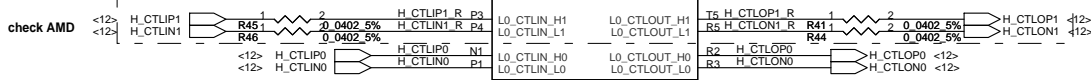
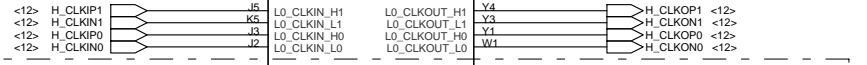
hexainf@hotmail.com  
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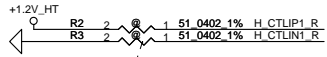


H_CADIP15 N5	L0_CADIN_H15	L0_CADOUT_H15	T4 H_CADOP15
H_CADIP15 P6	L0_CADIN_L15	L0_CADOUT_L15	T3 H_CADON15
H_CADIP14 M3	L0_CADIN_H14	L0_CADOUT_H14	V6 H_CADOP14
H_CADIP14 M4	L0_CADIN_L14	L0_CADOUT_L14	V5 H_CADON14
H_CADIP13 L5	L0_CADIN_H13	L0_CADOUT_H13	V4 H_CADOP13
H_CADIP13 M5	L0_CADIN_L13	L0_CADOUT_L13	V3 H_CADON13
H_CADIP12 K3	L0_CADIN_H12	L0_CADOUT_H12	V6 H_CADOP12
H_CADIP12 K4	L0_CADIN_L12	L0_CADOUT_L12	V5 H_CADON12
H_CADIP11 H3	L0_CADIN_H11	L0_CADOUT_H11	AE5 H_CADOP11
H_CADIP11 H4	L0_CADIN_L11	L0_CADOUT_L11	AE4 H_CADON11
H_CADIP10 G5	L0_CADIN_H10	L0_CADOUT_H10	AE4 H_CADOP10
H_CADIP10 G6	L0_CADIN_L10	L0_CADOUT_L10	AE3 H_CADON10
H_CADIP9 E3	L0_CADIN_H9	L0_CADOUT_H9	AE5 H_CADOP9
H_CADIP9 E4	L0_CADIN_L9	L0_CADOUT_L9	AE4 H_CADON9
H_CADIP8 E5	L0_CADIN_H8	L0_CADOUT_H8	AD4 H_CADOP8
H_CADIP8 E6	L0_CADIN_L8	L0_CADOUT_L8	AD3 H_CADON8
H_CADIP7 N3	L0_CADIN_H7	L0_CADOUT_H7	T1 H_CADOP7
H_CADIP7 N2	L0_CADIN_L7	L0_CADOUT_L7	R1 H_CADON7
H_CADIP6 L1	L0_CADIN_H6	L0_CADOUT_H6	U2 H_CADOP6
H_CADIP6 M1	L0_CADIN_L6	L0_CADOUT_L6	U3 H_CADON6
H_CADIP5 L3	L0_CADIN_H5	L0_CADOUT_H5	V1 H_CADOP5
H_CADIP5 L2	L0_CADIN_L5	L0_CADOUT_L5	V2 H_CADON5
H_CADIP4 J1	L0_CADIN_H4	L0_CADOUT_H4	W2 H_CADOP4
H_CADIP4 K1	L0_CADIN_L4	L0_CADOUT_L4	W3 H_CADON4
H_CADIP3 G1	L0_CADIN_H3	L0_CADOUT_H3	AA2 H_CADOP3
H_CADIP3 H1	L0_CADIN_L3	L0_CADOUT_L3	AA3 H_CADON3
H_CADIP2 G3	L0_CADIN_H2	L0_CADOUT_H2	AB1 H_CADOP2
H_CADIP2 G2	L0_CADIN_L2	L0_CADOUT_L2	AA1 H_CADON2
H_CADIP1 E1	L0_CADIN_H1	L0_CADOUT_H1	AC2 H_CADOP1
H_CADIP0 E3	L0_CADIN_H0	L0_CADOUT_H0	AC3 H_CADON1
H_CADIN0 E2	L0_CADIN_L0	L0_CADOUT_L0	AD1 H_CADOP0
			AC1 H_CADON0

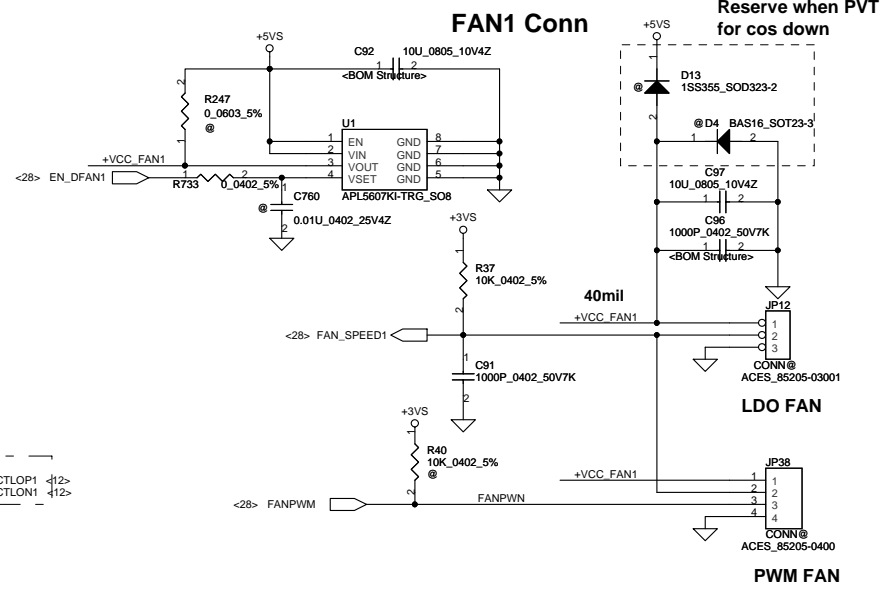
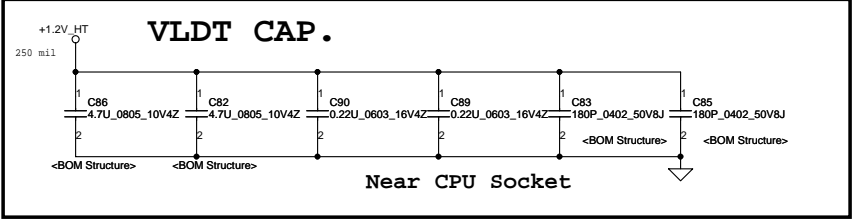
HIT Interface



FOX\_P263823-284S-41F  
 CONN@  
 Athlon 64 S1  
 Processor Socket

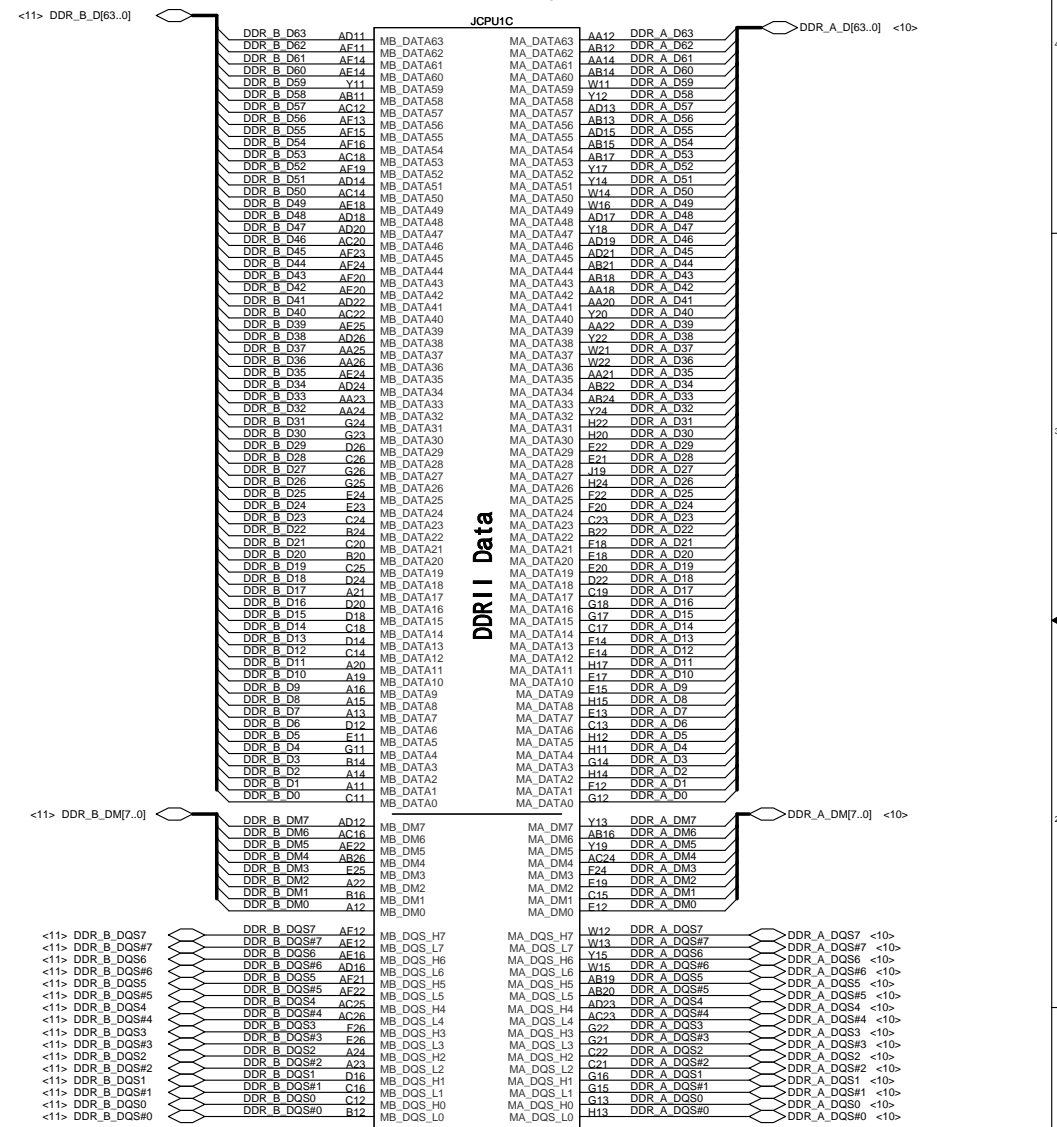
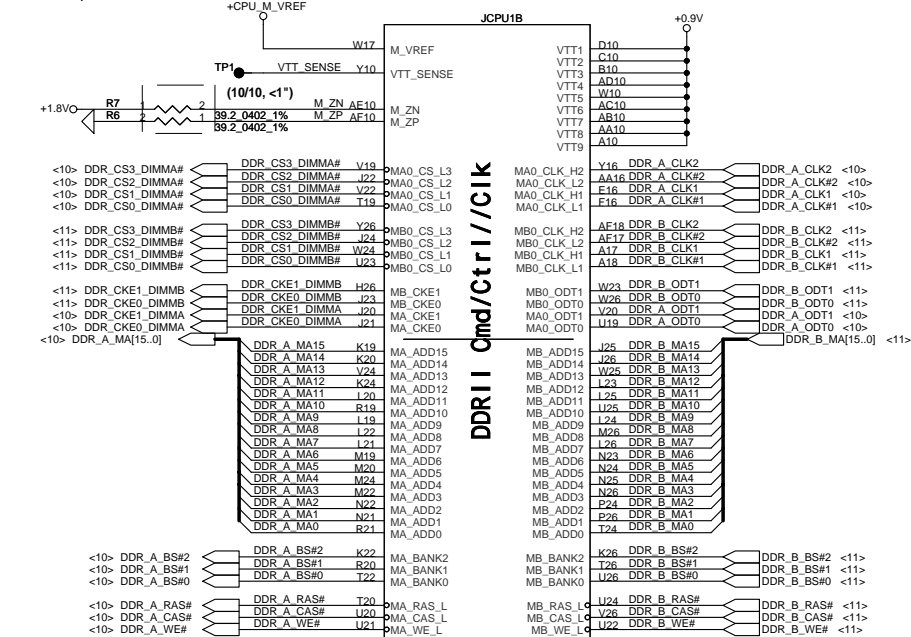
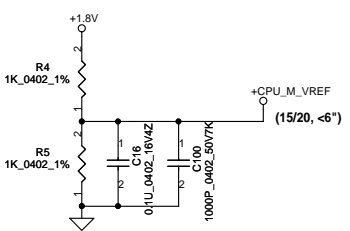


AMD : 49.9 1%  
 ATI : 51 1%

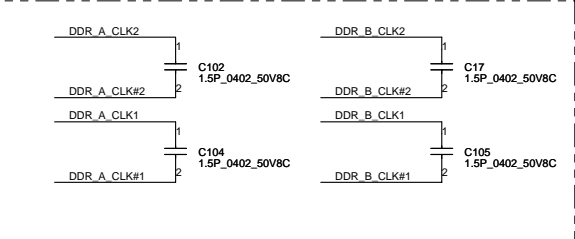


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# Processor DDR2 Memory Interface

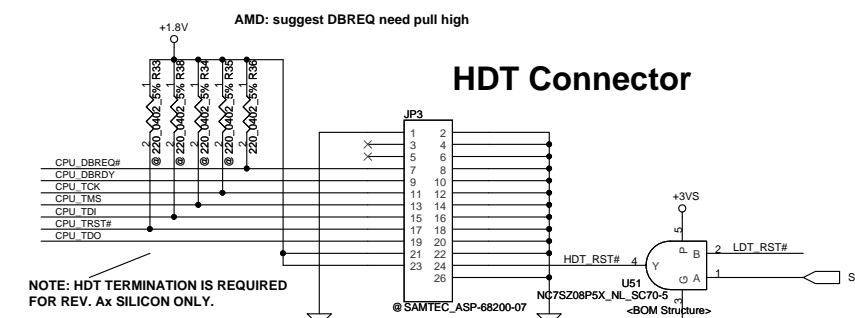
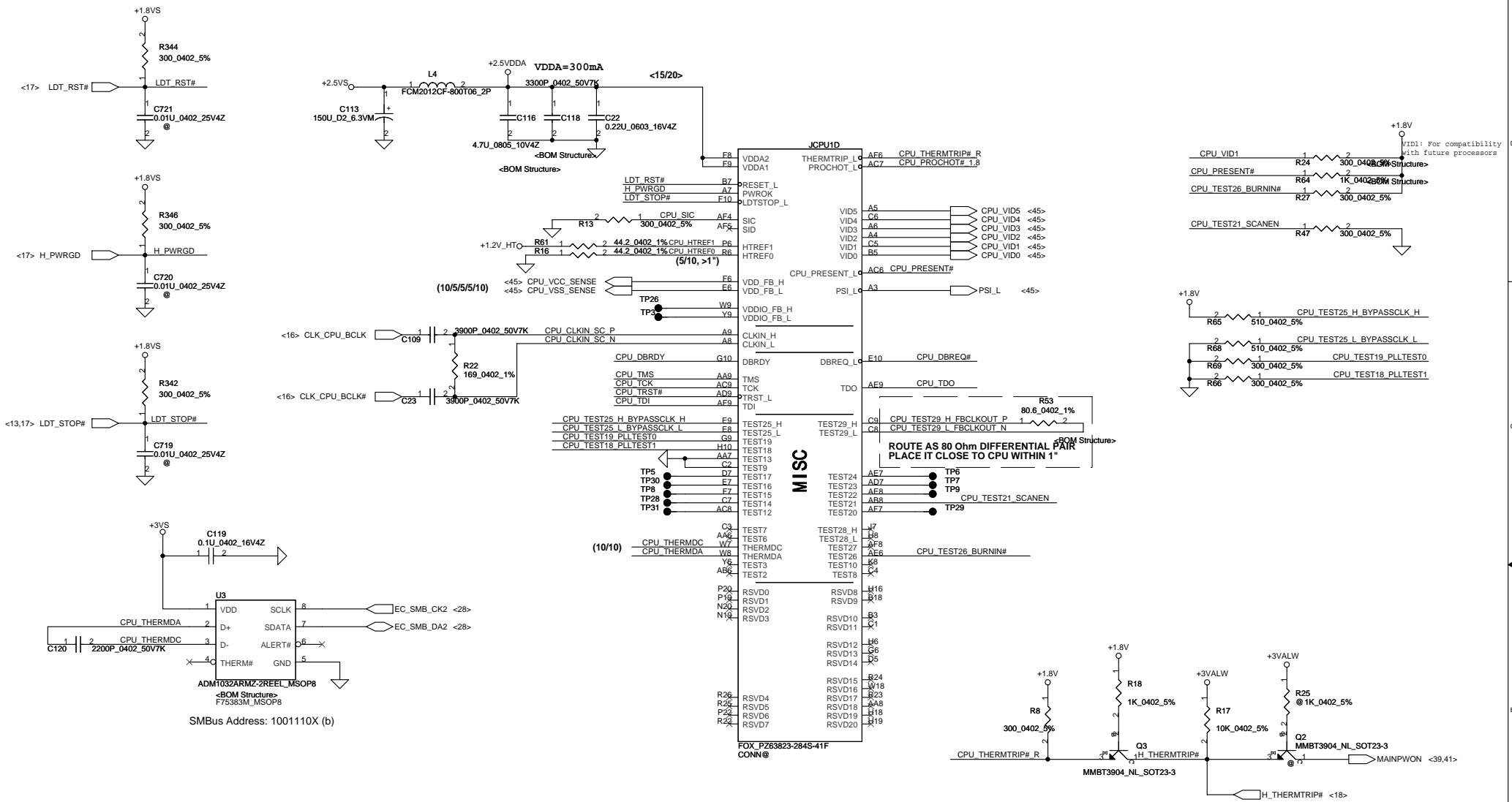


PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH



CONN@ FOX\_P263823-2845-41F  
Athlon 64 S1  
Processor Socket

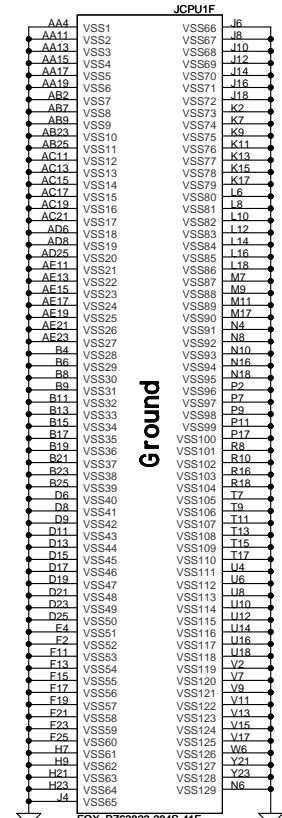
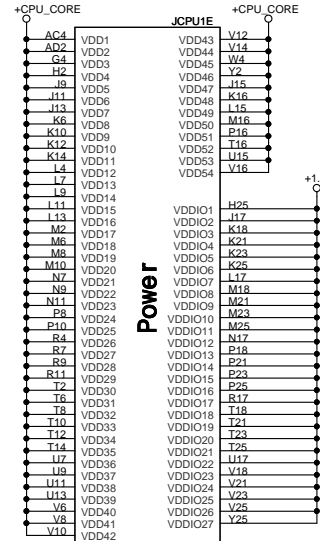
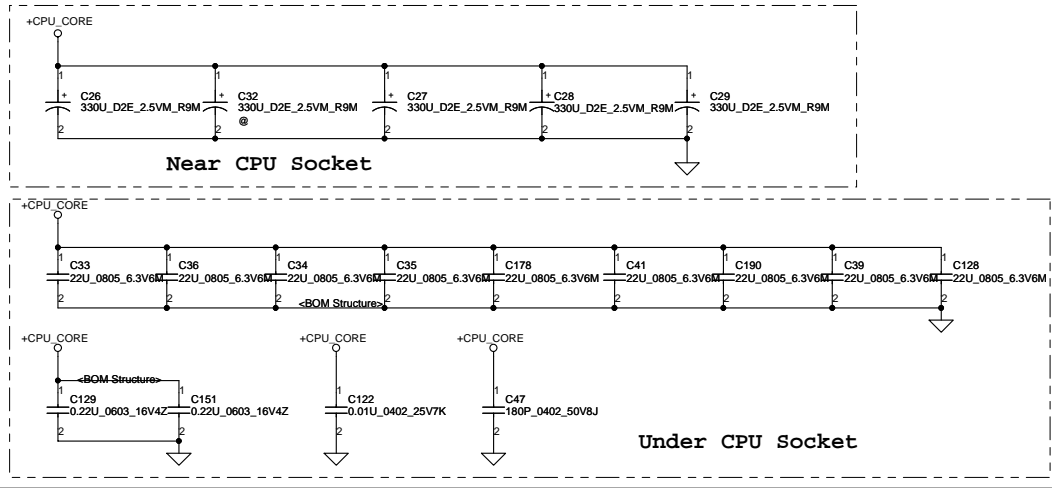
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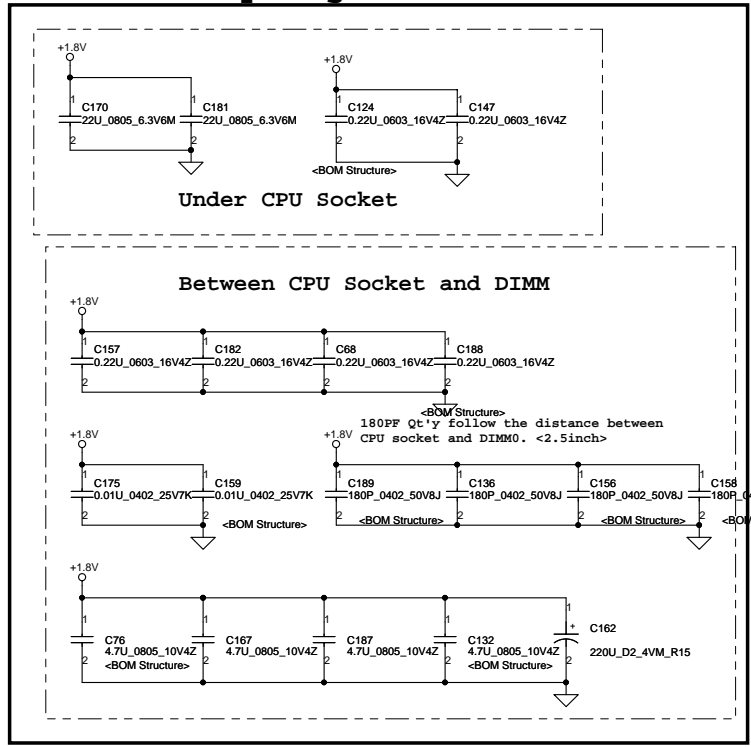
## VDD(+CPU\_CORE) decoupling.



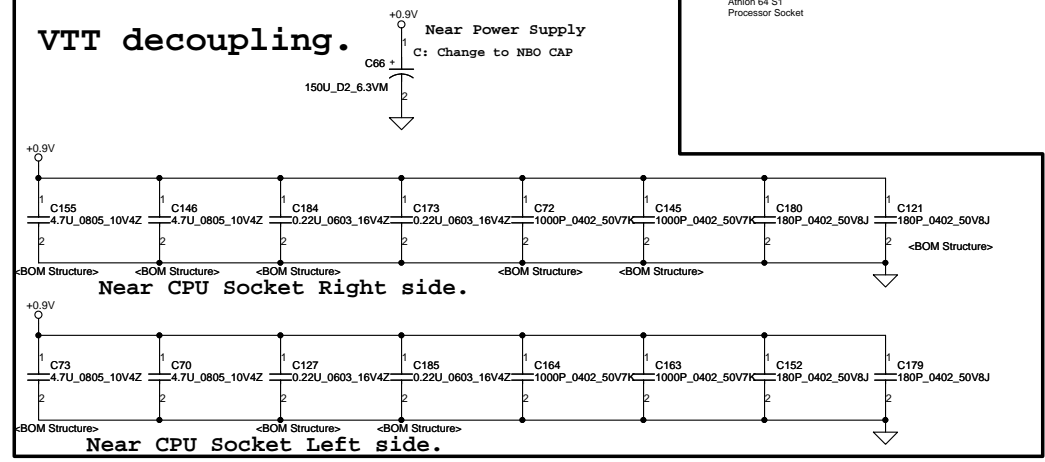
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 Athlon 64 S1  
 Processor Socket

FOX\_PZ63823-284S-41F  
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 Athlon 64 S1  
 Processor Socket

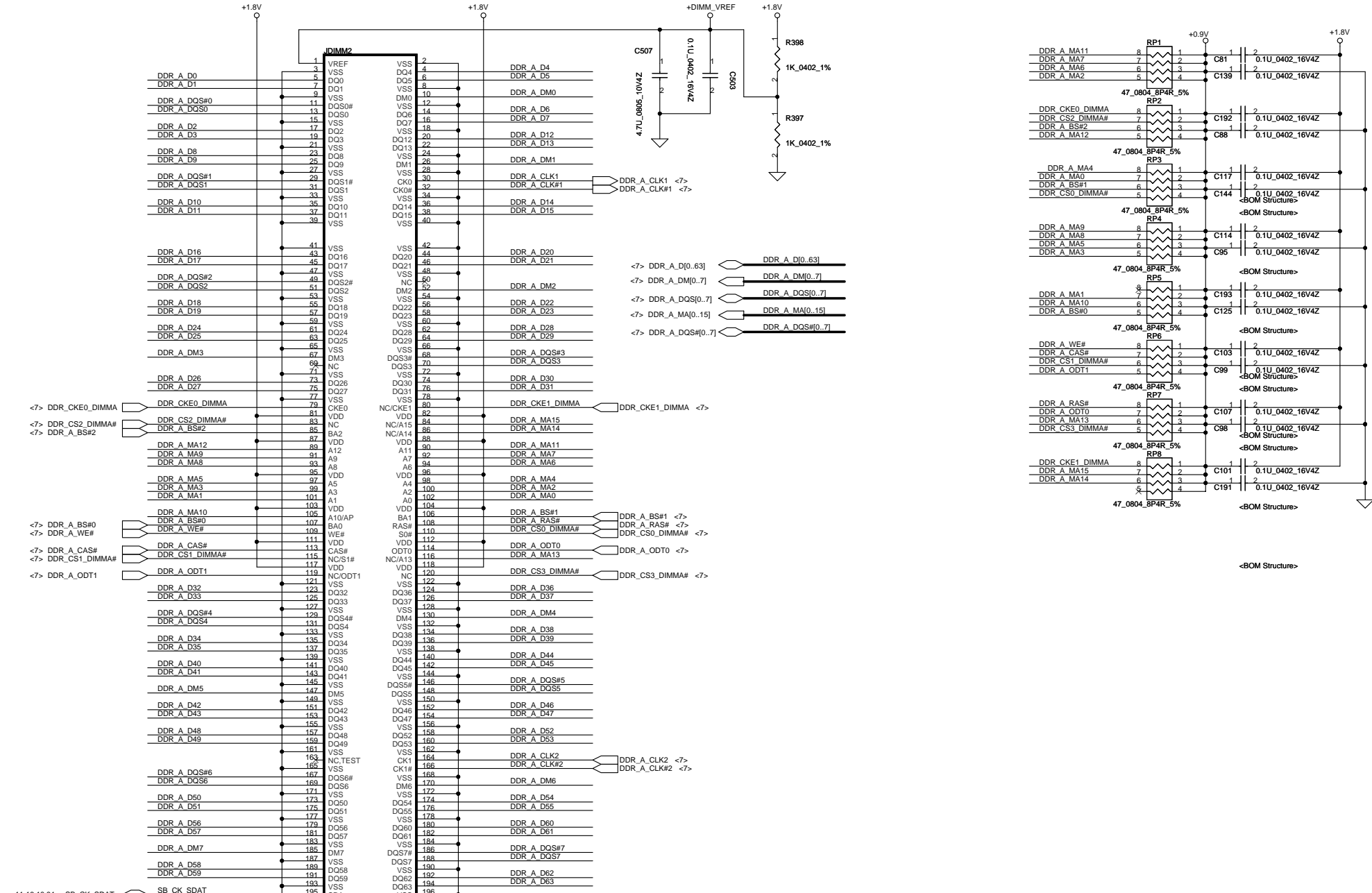
## VDDIO decoupling.



## VTT decoupling.

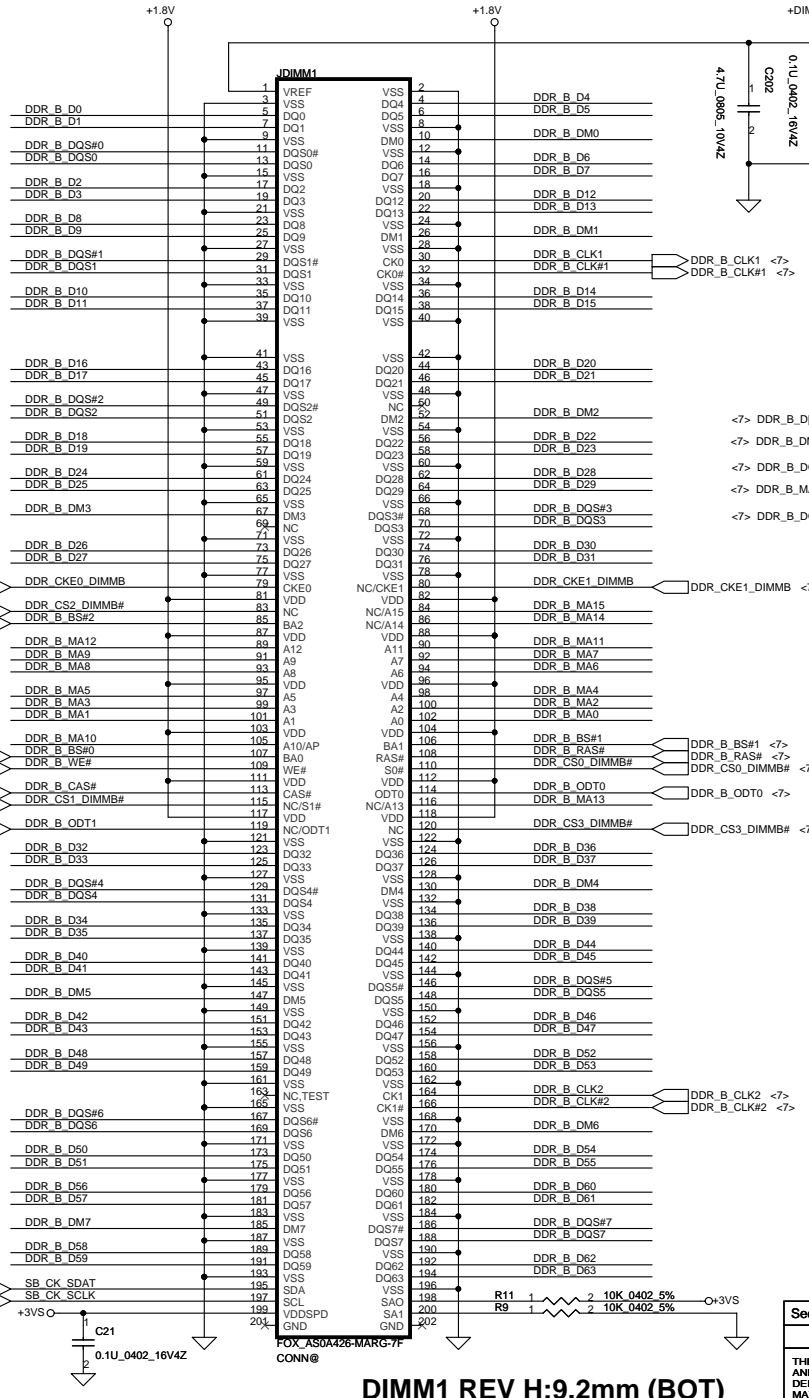


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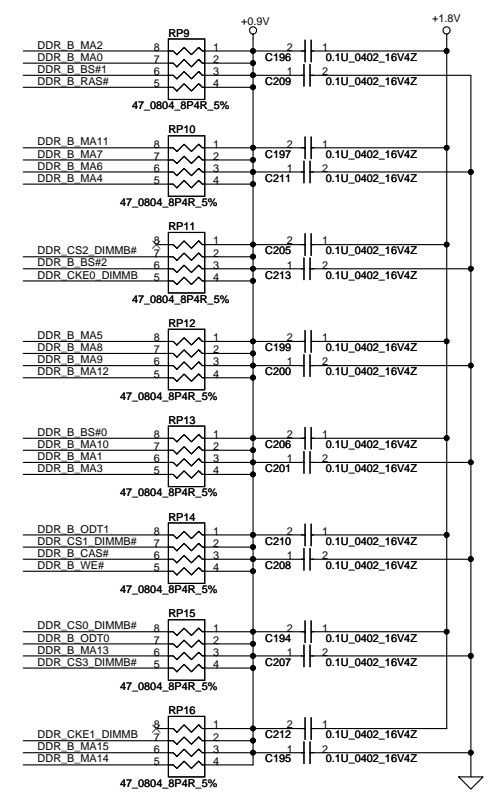


**DIMM2 REV H:5.2mm (BOT)**

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				<b>Date:</b> Wednesday, June 24, 2009	<b>Sheet 10 of 46</b>

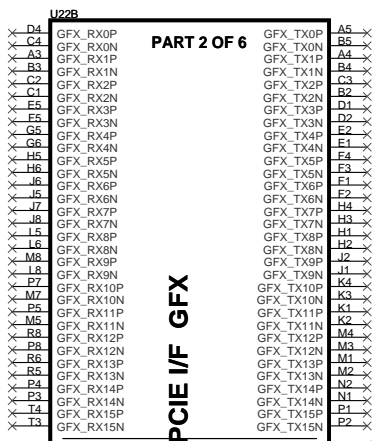


- <?> DDR\_B\_D[0..63]      DDR\_B D[0..63]
- <?> DDR\_B\_DM[0..7]     DDR\_B DM[0..7]
- <?> DDR\_B\_DQS[0..7]    DDR\_B DQS[0..7]
- <?> DDR\_B\_MA[0..15]    DDR\_B MA[0..15]
- <?> DDR\_B\_DQS#[0..7]   DDR\_B DQS#[0..7]

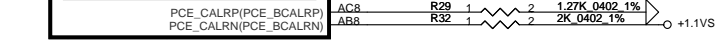
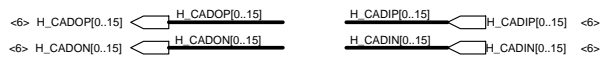
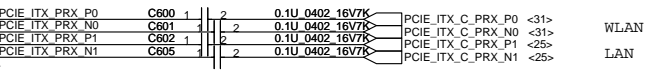
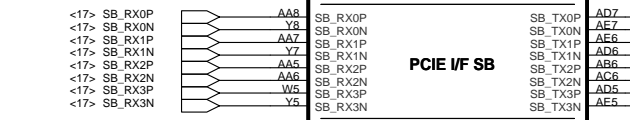
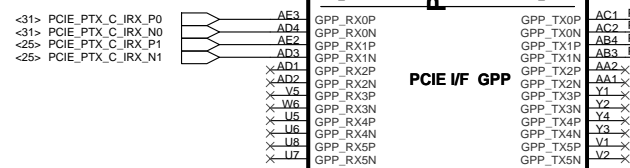


**DIMM1 REV H:9.2mm (BOT)**

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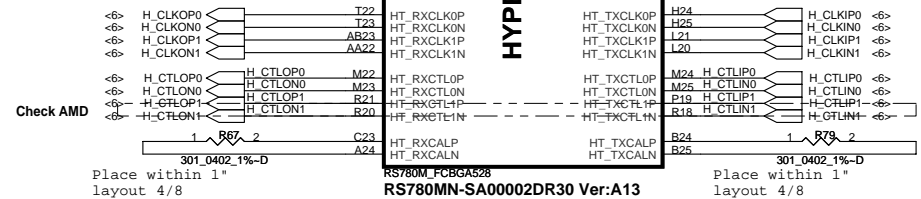
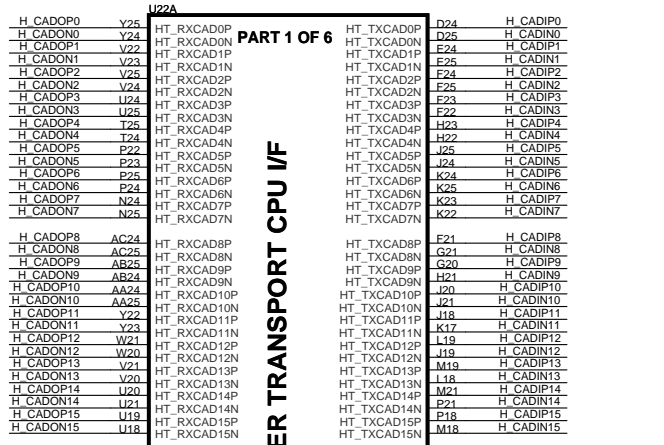
**Check SW Routing**  
 AN\_RS780MN1. Only suggest pair0-3 can use for power save.



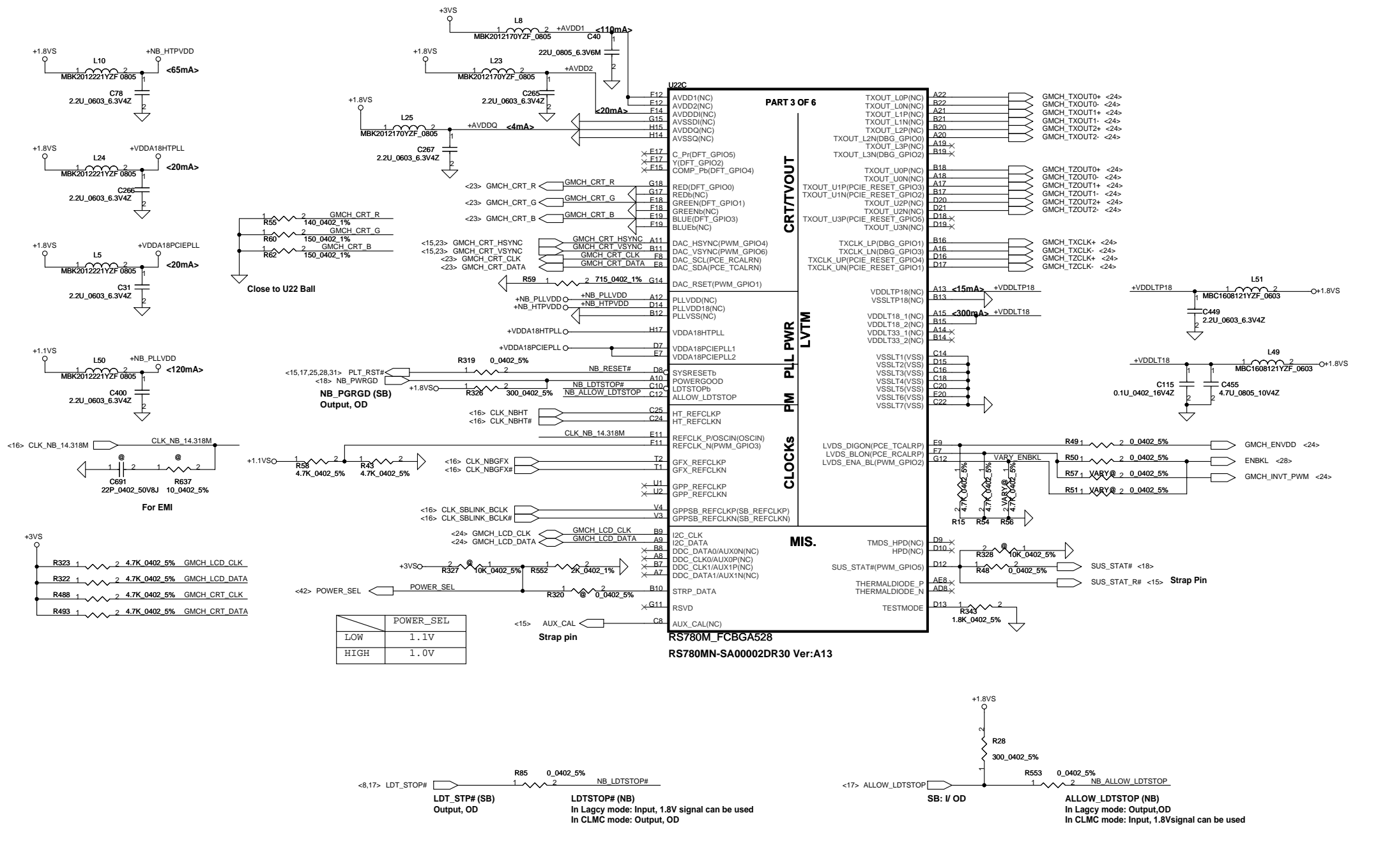
**RS780M Display Port Support (muxed on GFX)**

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

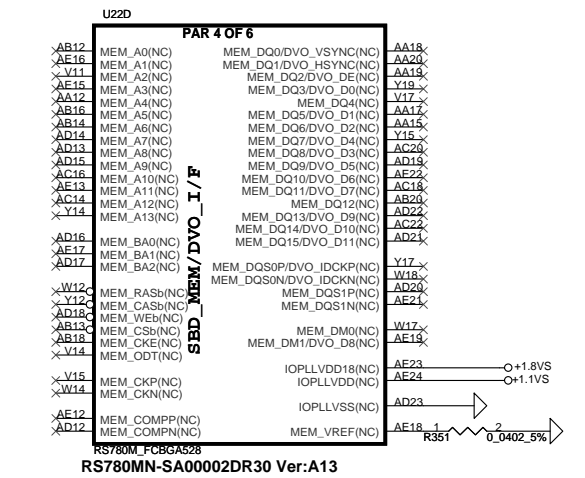
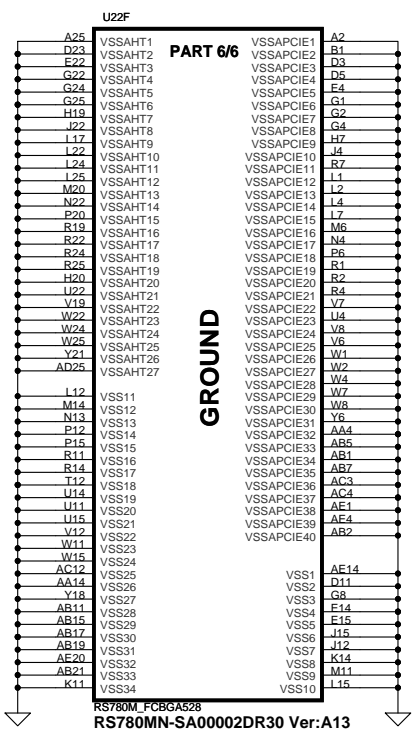
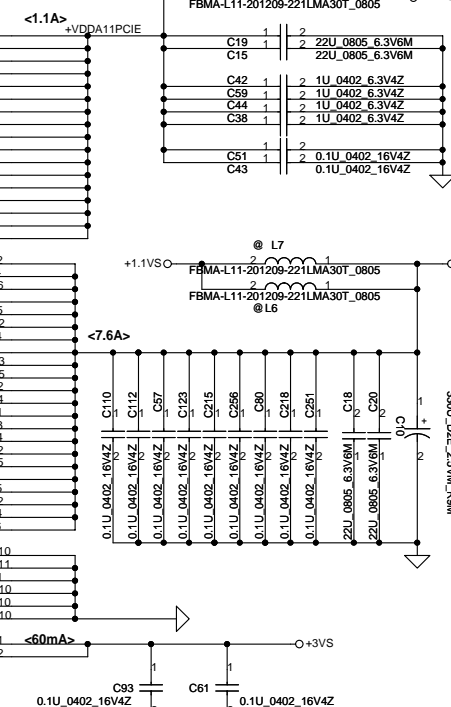
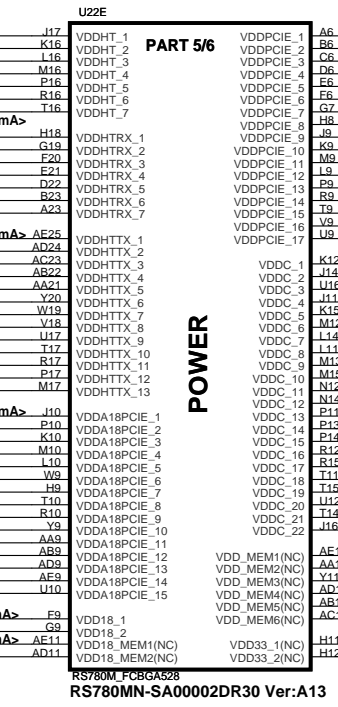
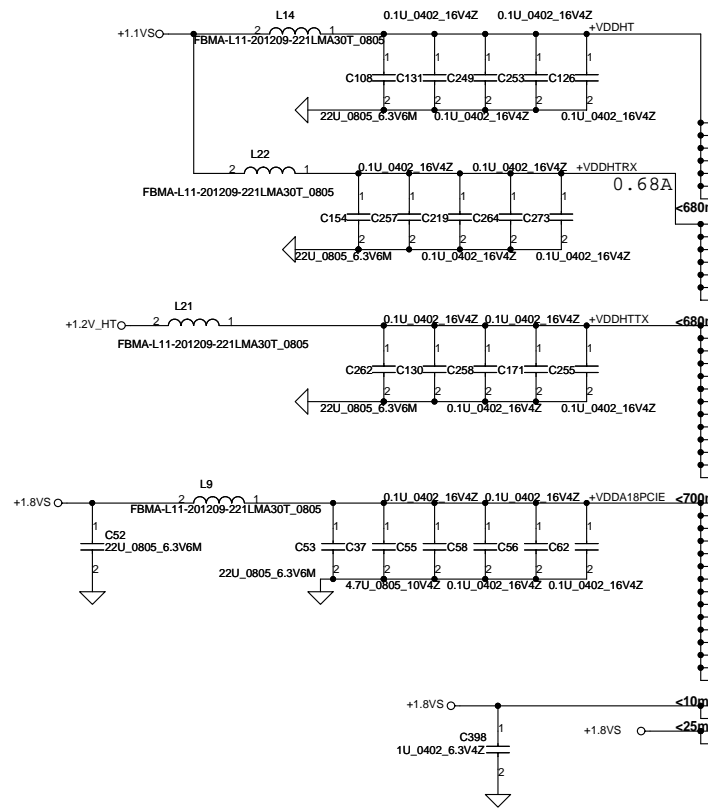
**HT Link**  
 When tune trace length, must keep 1:4 on self-trace



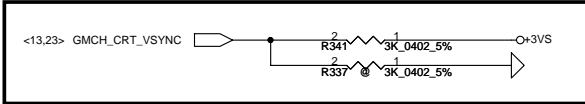
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RS780MN-SA0002DR30 Ver:A13				Document Number 401743
Date: Wednesday, June 24, 2009				Rev C
Sheet 13 of 47				

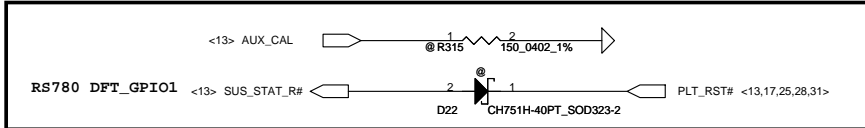


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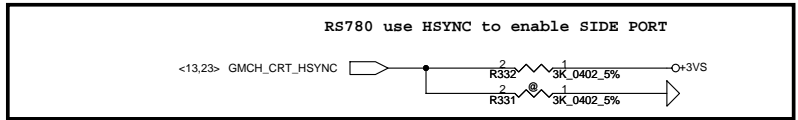
**DFT\_GPIO5:STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb**

Enables the Test Debug Bus using GPIO. (VSYNC)  
 1 : Disable (RS780)  
 0 : Enable (Rs780)



**DFT\_GPIO1: LOAD\_EEPROM\_STRAPS**

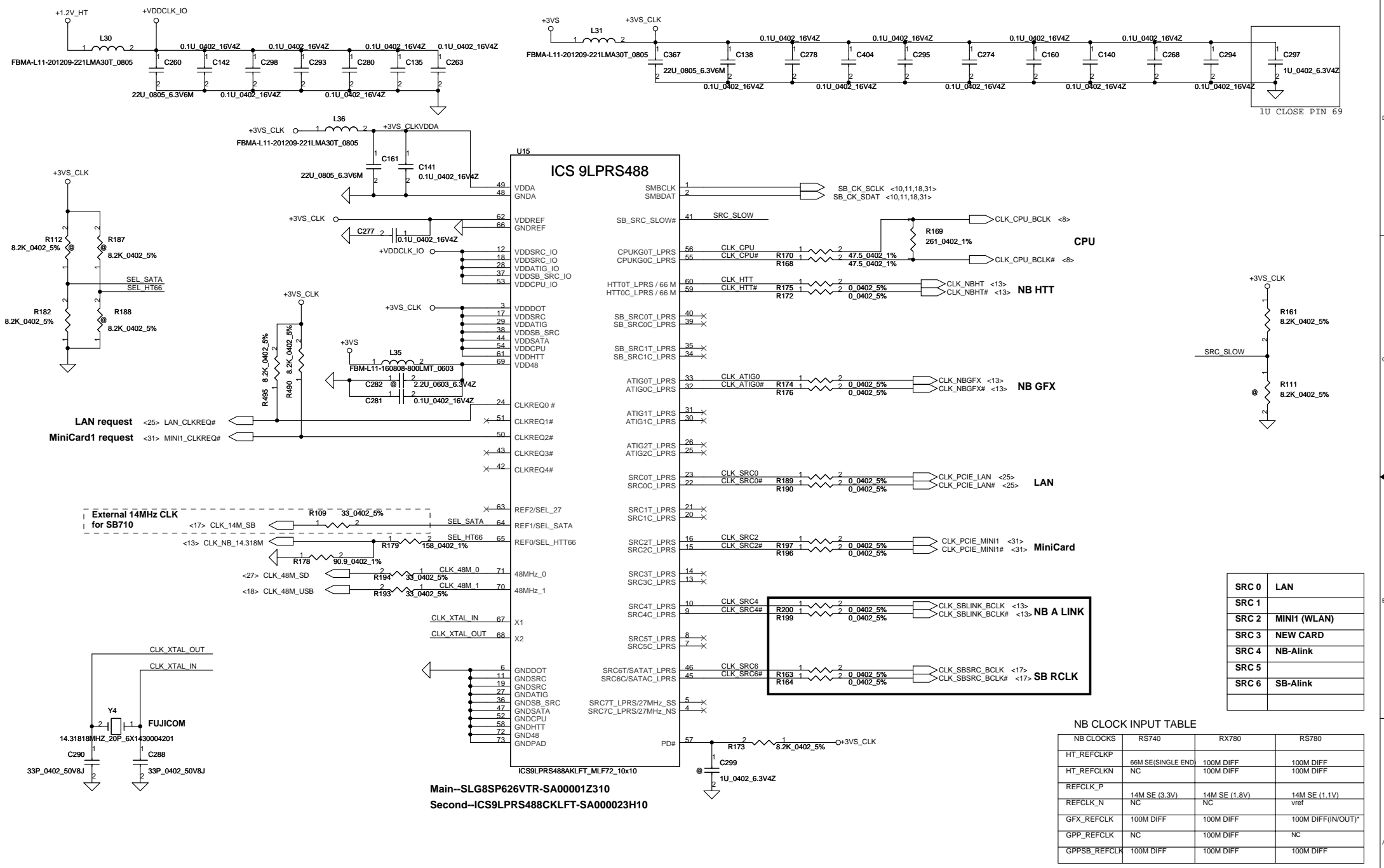
Selects Loading of STRAPS from EPROM  
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected  
 RS740/RX780: DFT\_GPIO1 RS780:SUS\_STAT



**RS780 use HSYNC to enable SIDE PORT**

RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)  
 0. Enable (RS780)  
 1 : Disable(RS780)

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Main-SLG8SP626VTR-SA00001Z310  
 Second-ICS9LPRS488CLKLFT-SA000023H10

SRC 0	LAN
SRC 1	
SRC 2	MINI1 (WLAN)
SRC 3	NEW CARD
SRC 4	NB-Alink
SRC 5	
SRC 6	SB-Alink

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	NC	NC	vref
REFCLK_N	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

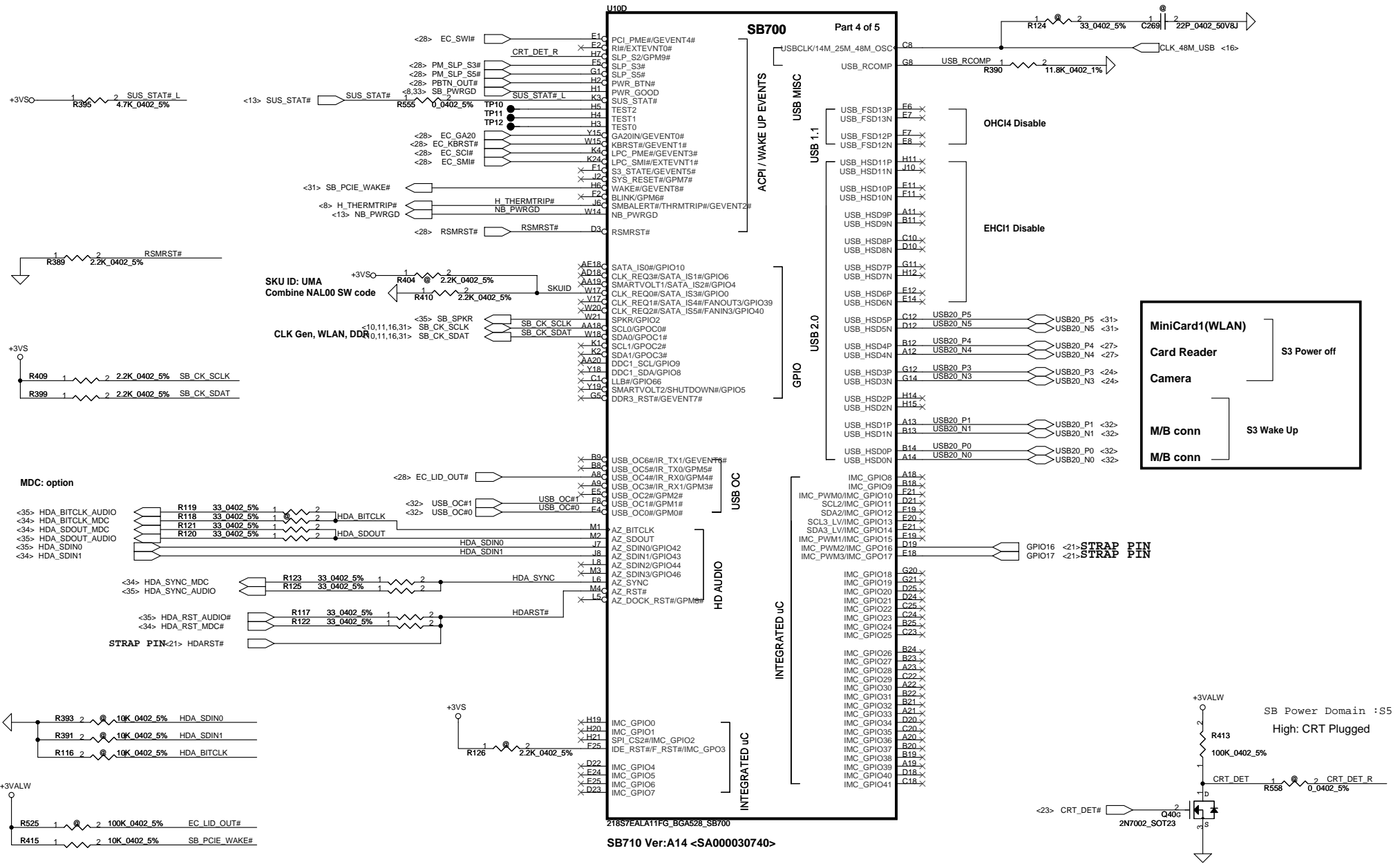
SEL_HTT66	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output
SEL_SATA	1*	SS 100M SATA SRC6 output
	0	SS 100M SATA SRC6 output

SEL_27M	1	configure as 27M and 27M_SS output
No used	0	configure as SRC_7 output

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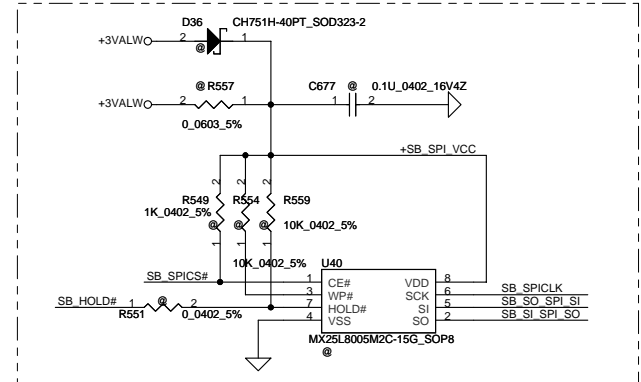
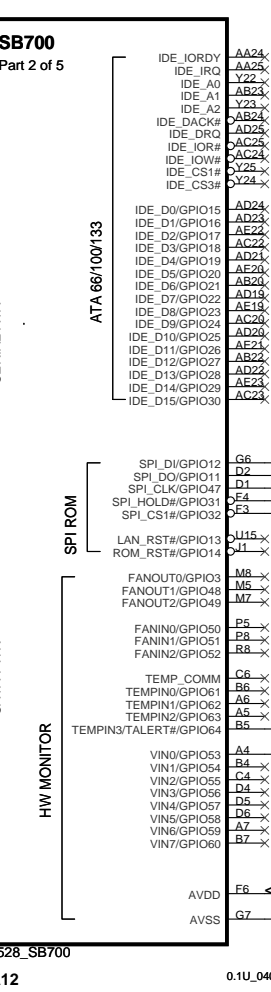
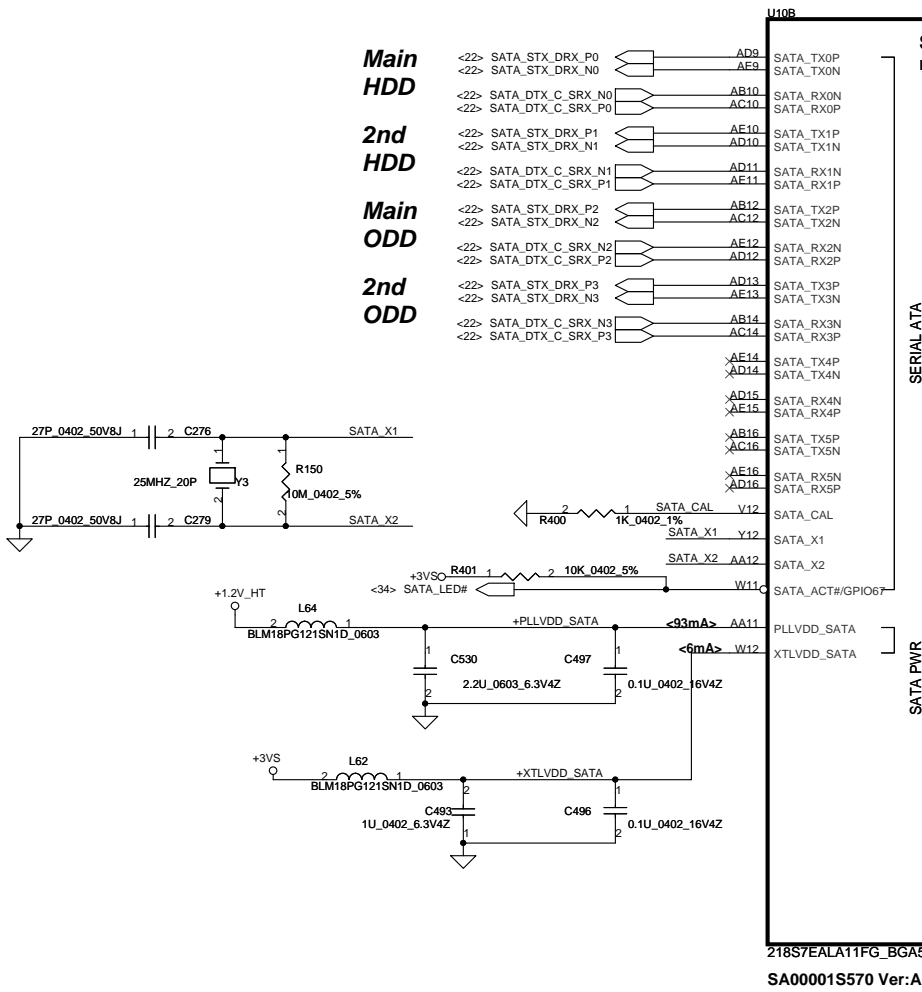




SB710 Ver:A14 <SA000030740>

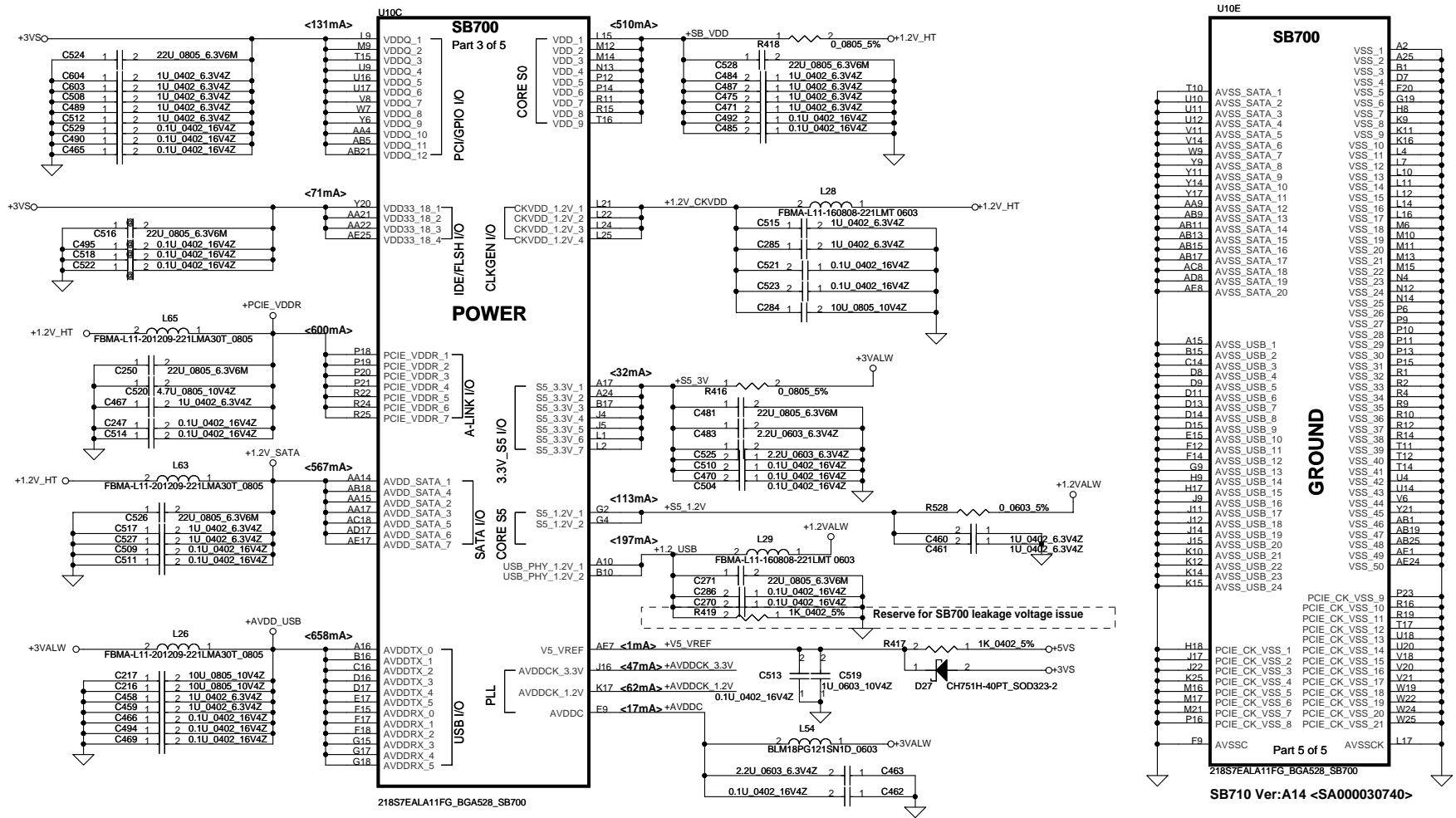
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Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 1	Secondary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller
Port 4	Primary (Secondary) master	PATA controller
Port 5	Primary (Secondary) slave	PATA controller

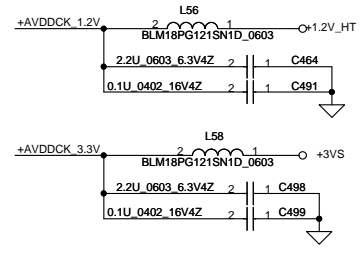


218S7EALA11FG\_BGA528\_SB700  
SA00001S570 Ver:A12

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218S7EAL11FG\_BGA528\_SB700  
 SB710 Ver:A14 <SA000030740>



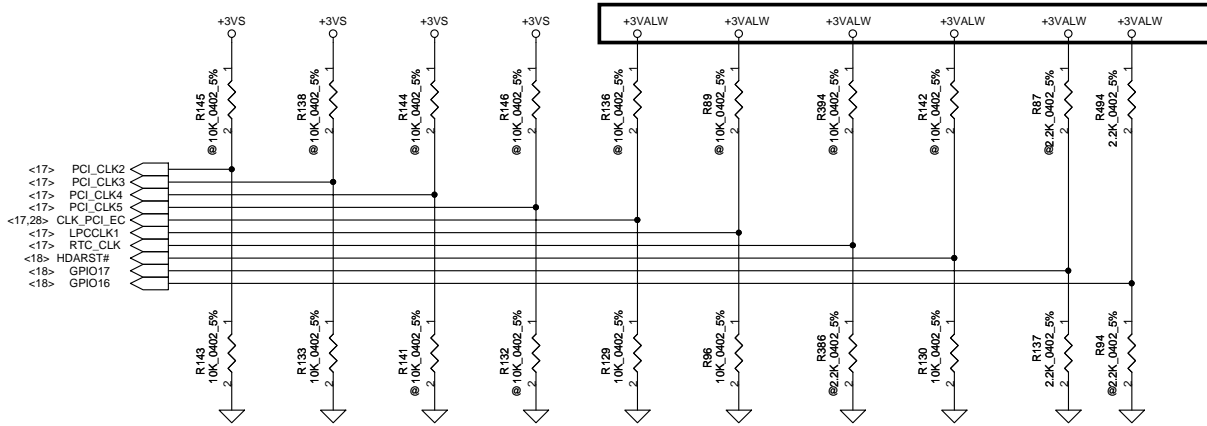
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SB710 Ver:A14 <SA000030740>

# REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
<b>PULL HIGH</b>	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	<b>INTERNAL RTC</b>  DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
<b>PULL LOW</b>	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default L,NC) L,L = FWH ROM	

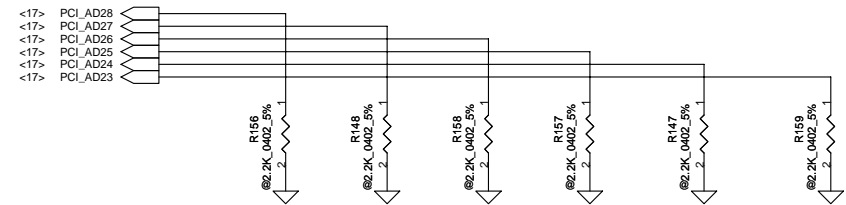


# DEBUG STRAPS

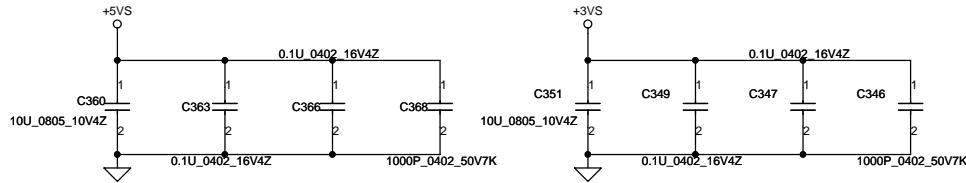
# DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]

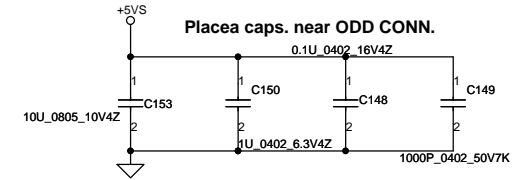
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
<b>PULL LOW</b>	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



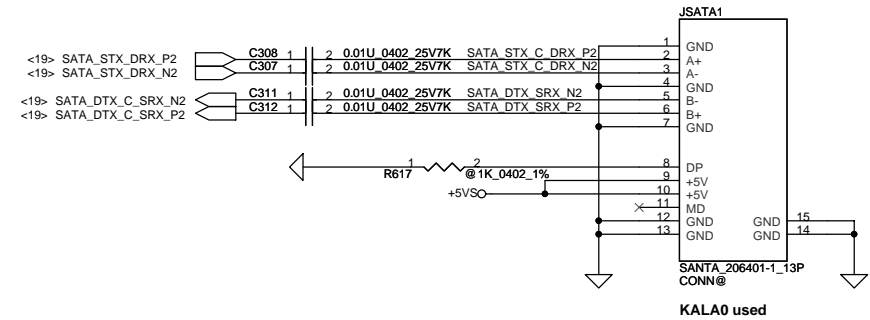
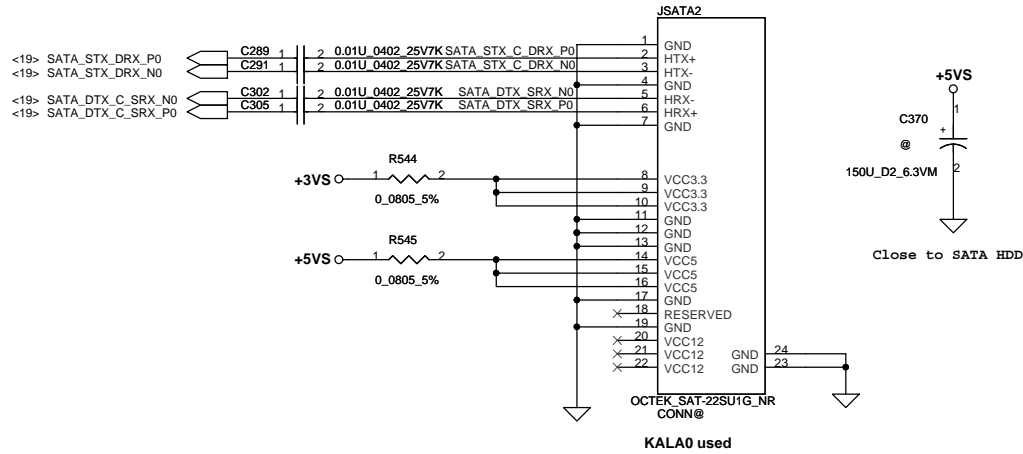
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**SATA HDD CONN**

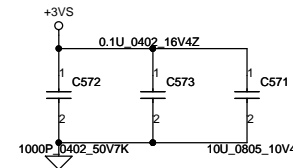
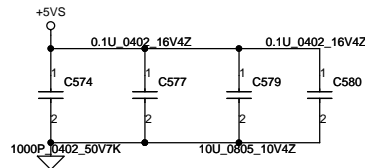
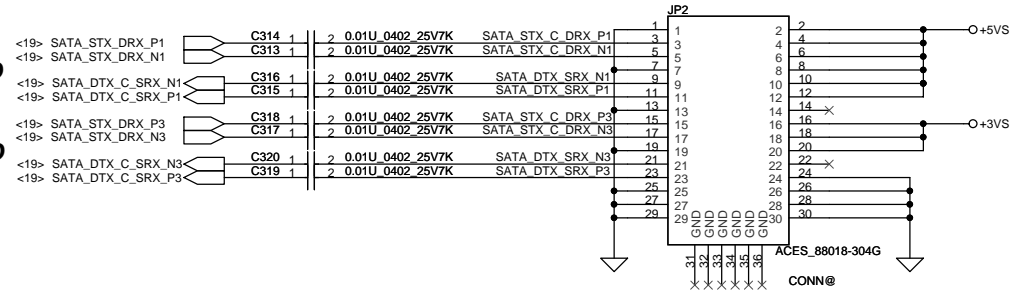


**SATA ODD CONN**



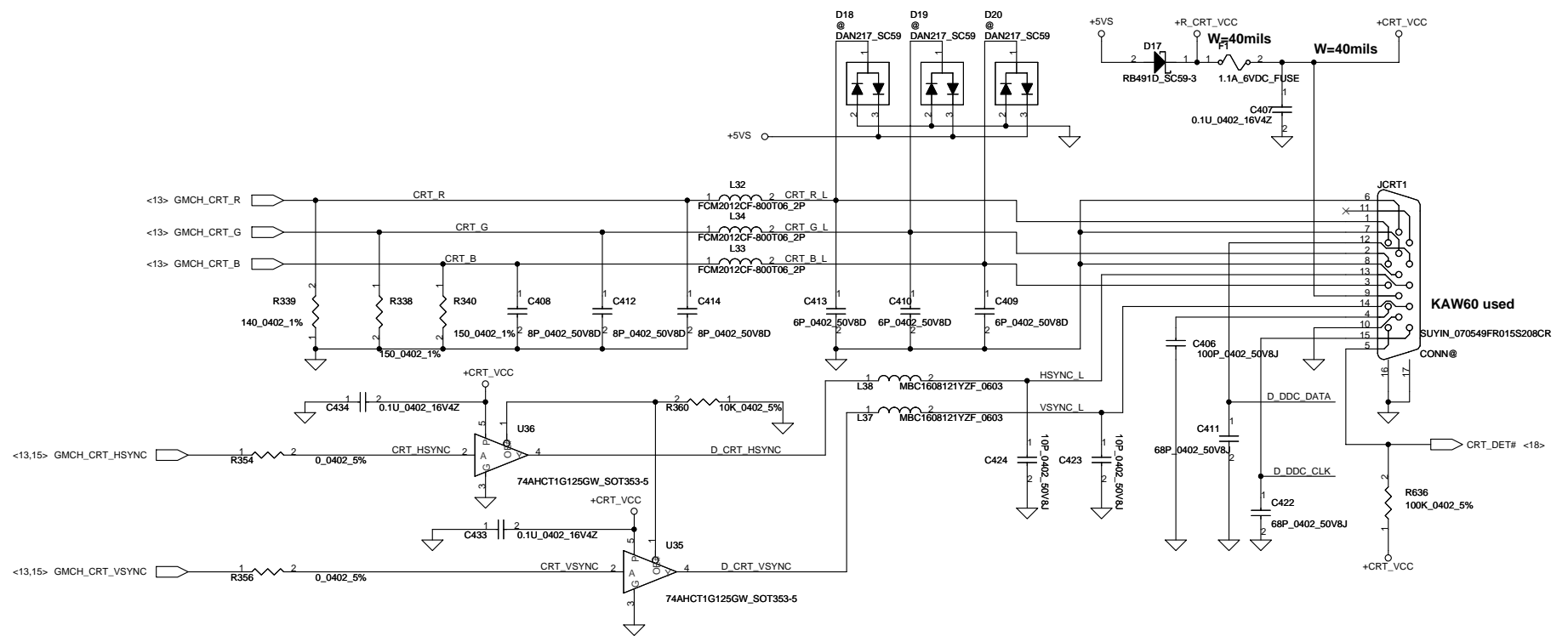
**Second HDD**

**Second ODD**

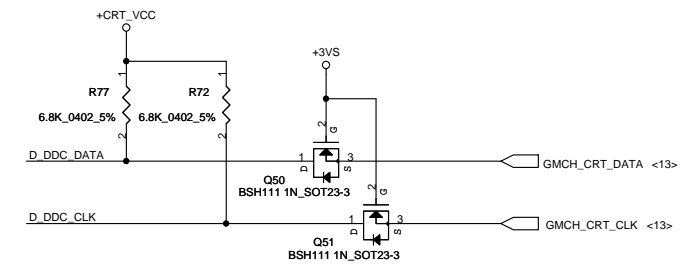


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# CRT Connector



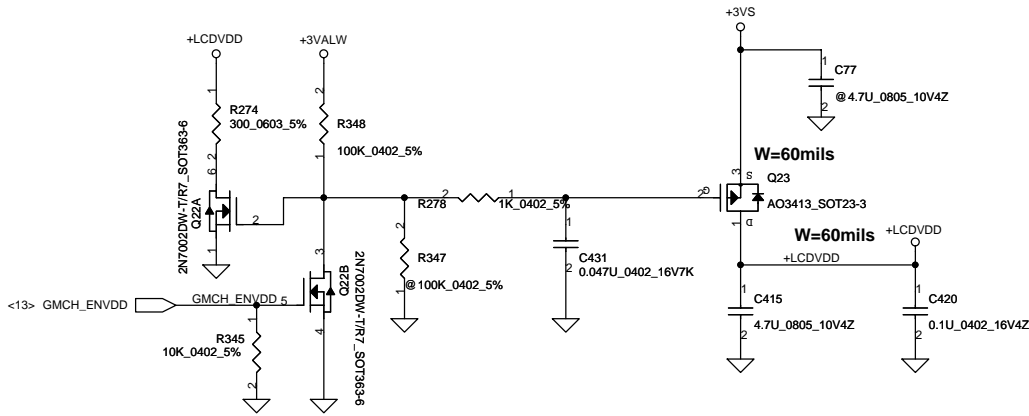
## Close to Conn side



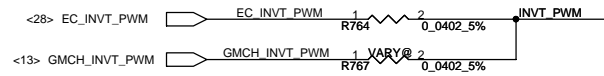
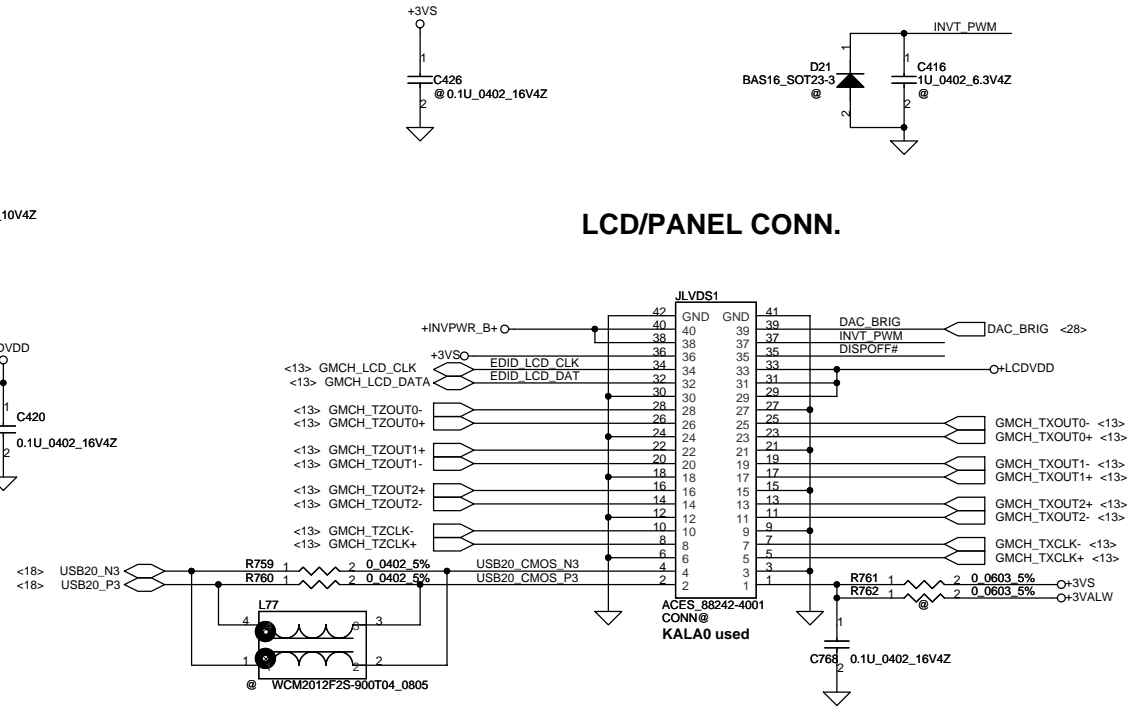
hexainf@hotmail.com  
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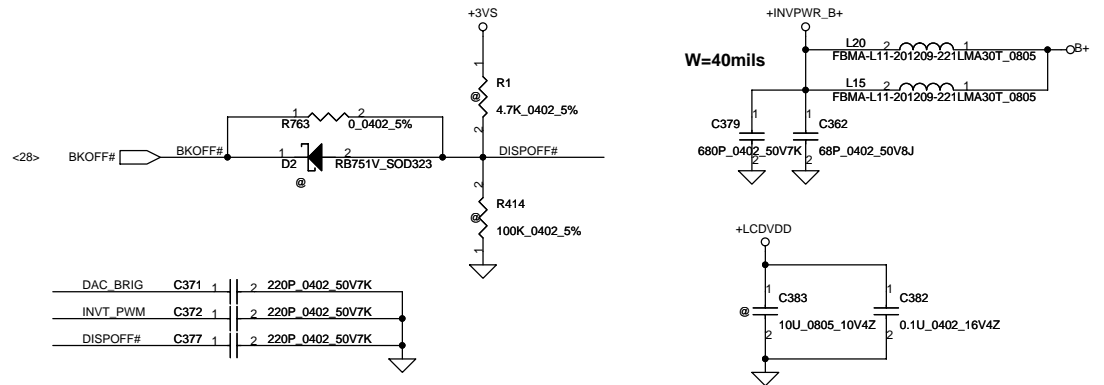
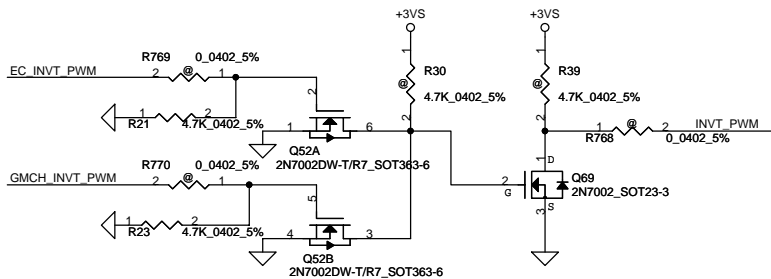
# LCD POWER CIRCUIT



# LCD/PANEL CONN.

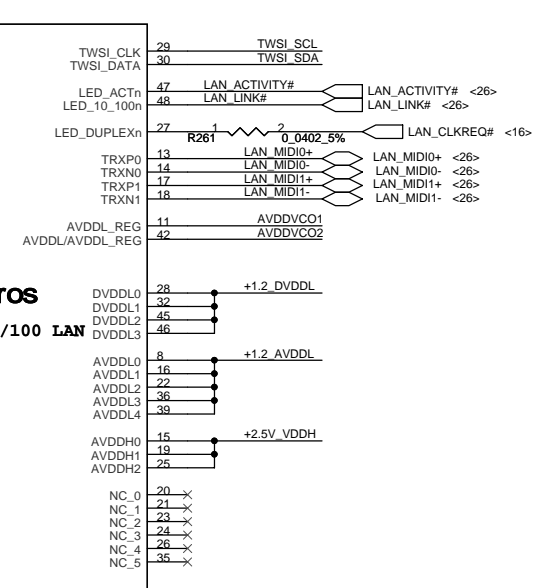
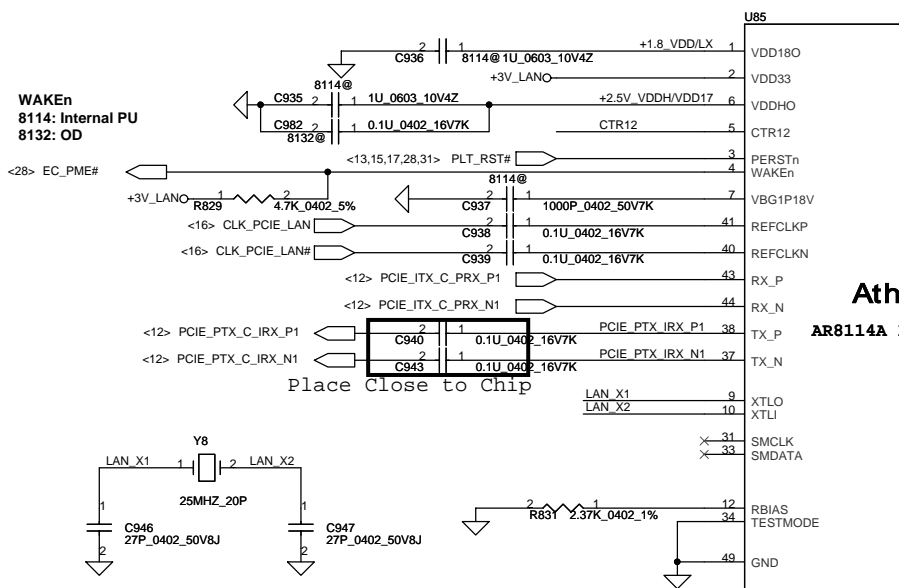
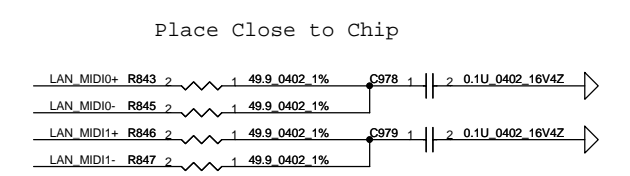
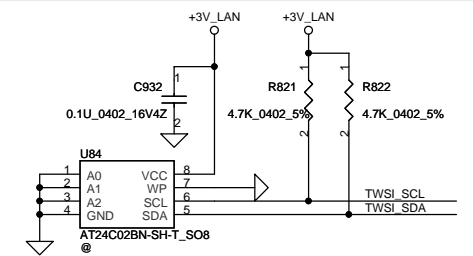
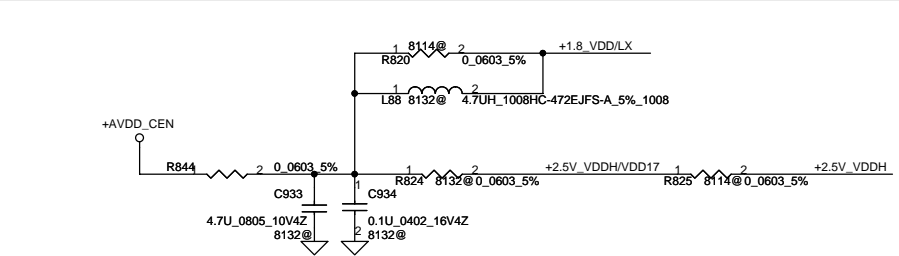


# VARYBRIGHT FUNCTION

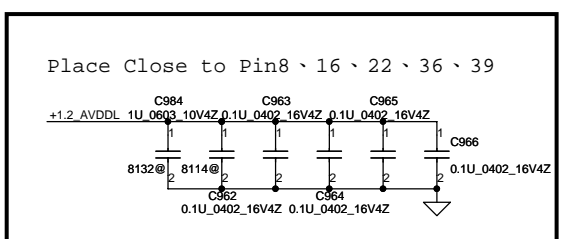
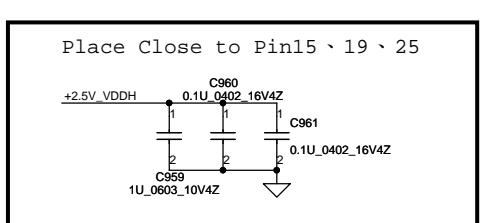
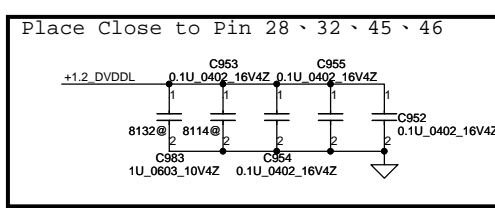
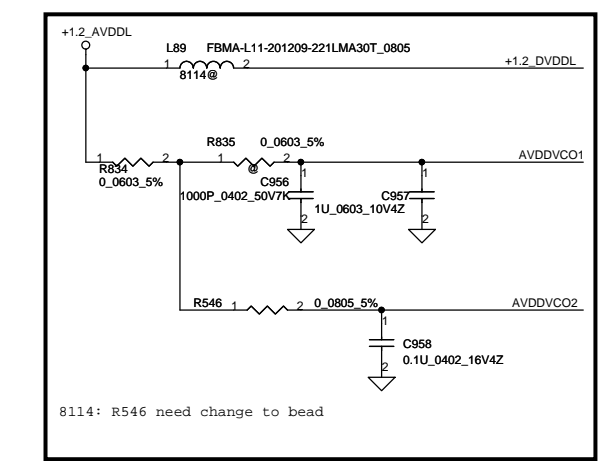
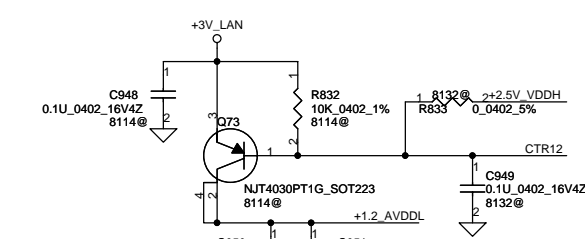
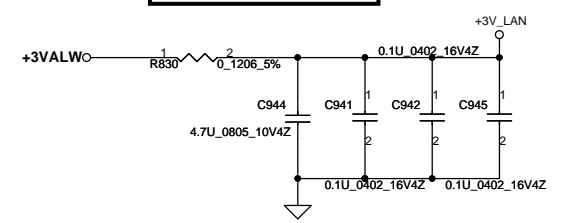


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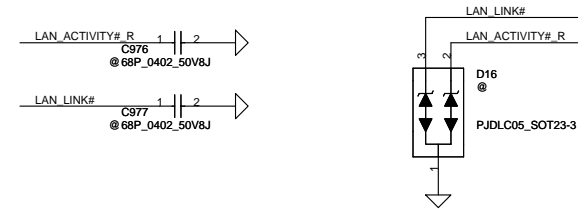
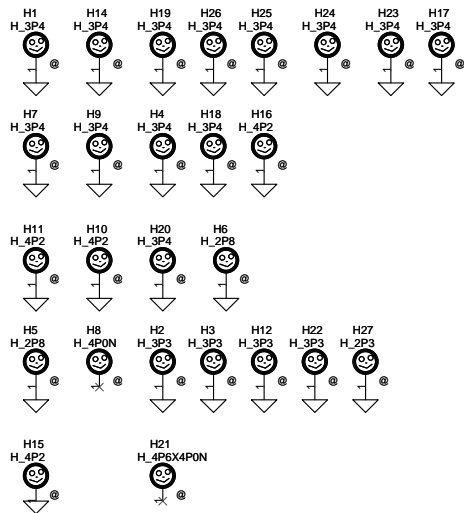
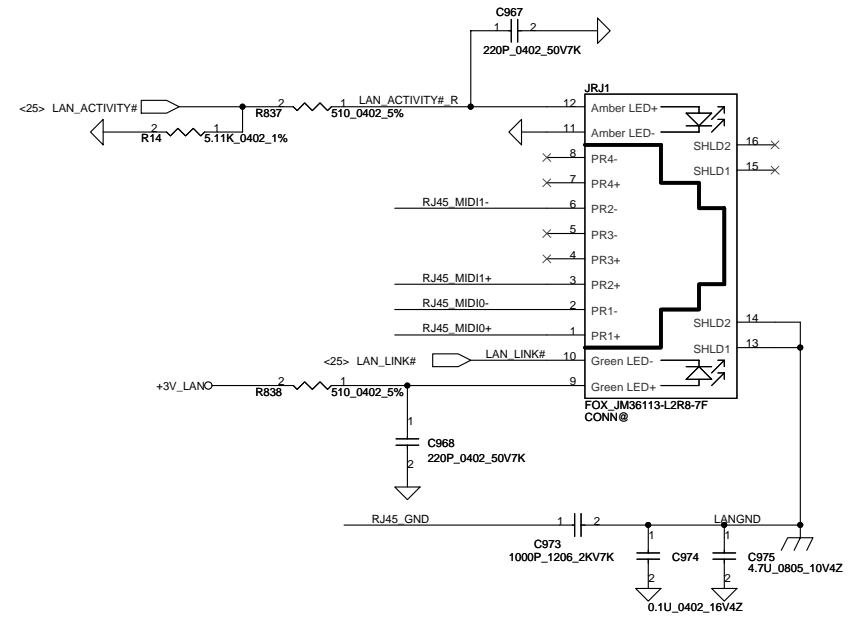
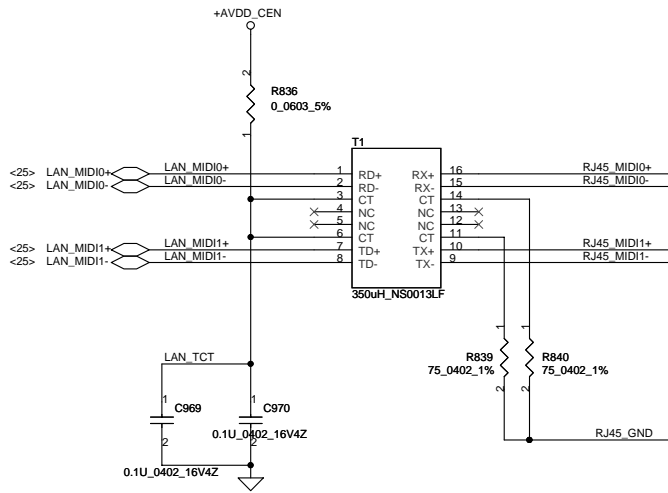


Layout Notice : Close to chip

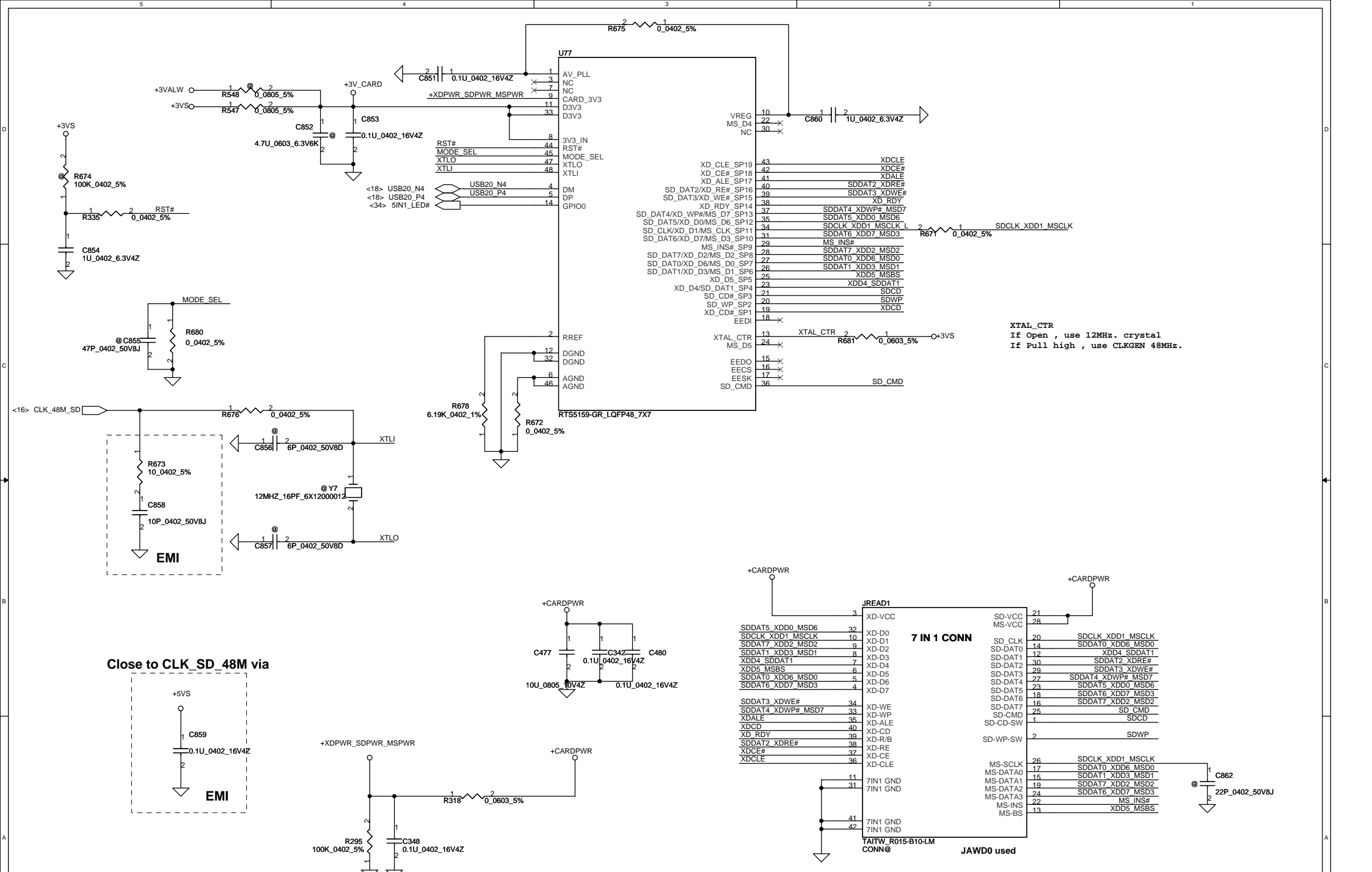


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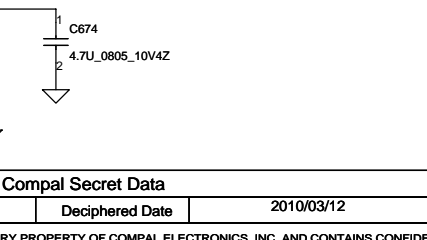
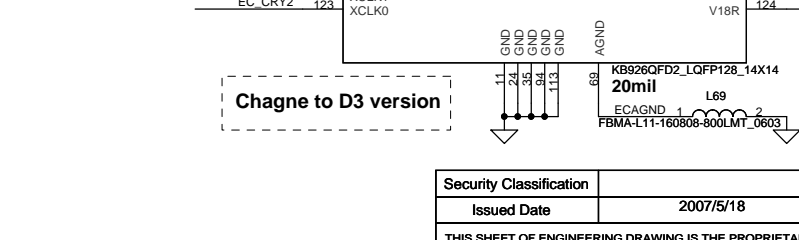
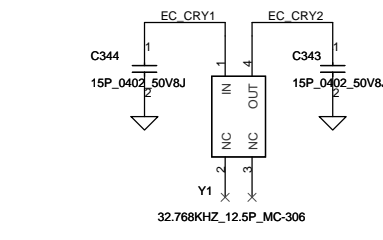
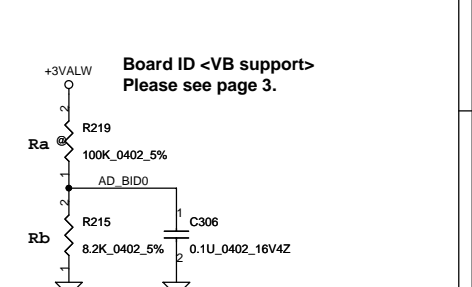
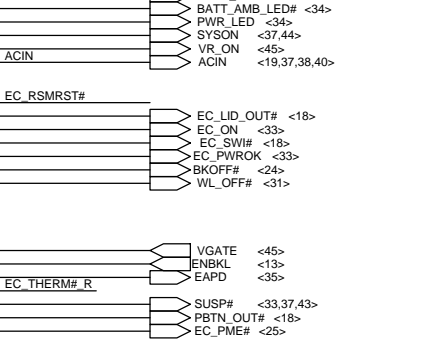
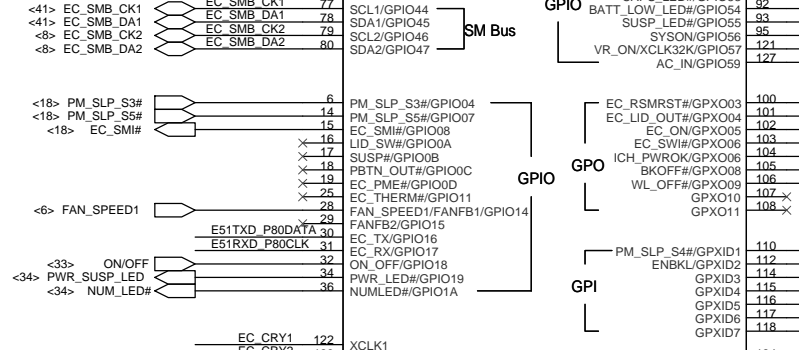
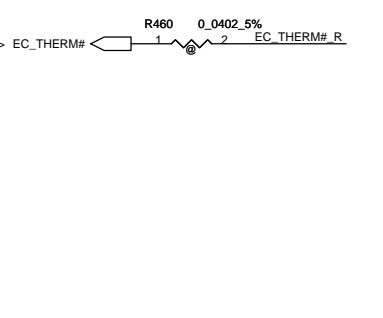
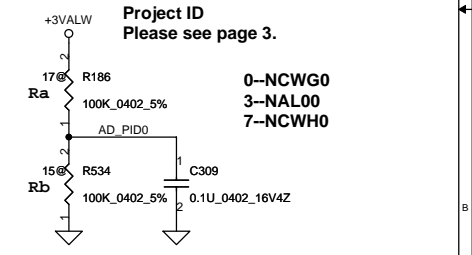
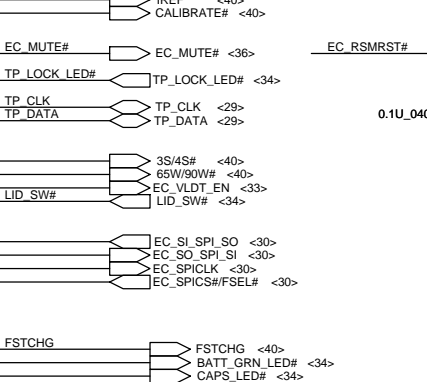
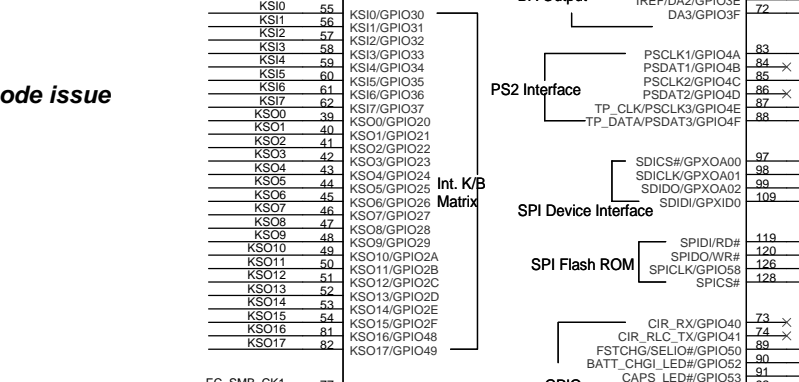
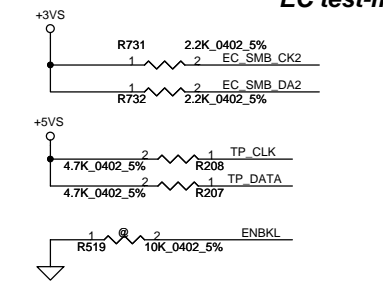
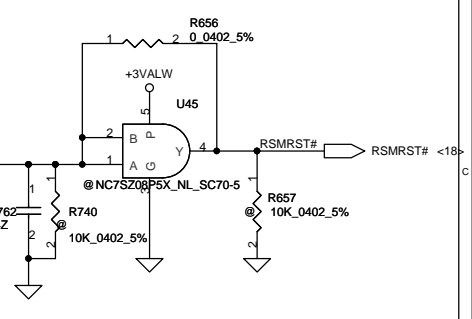
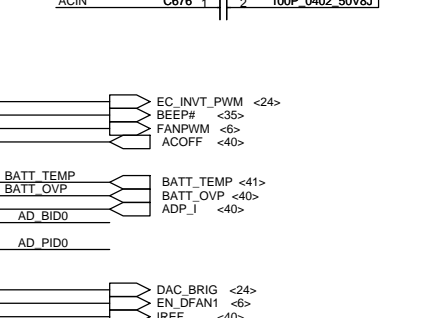
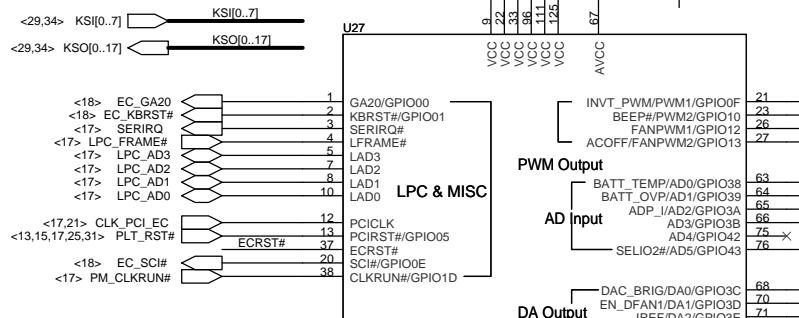
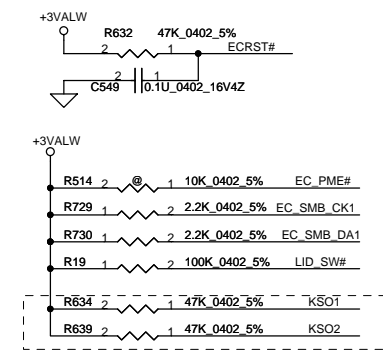
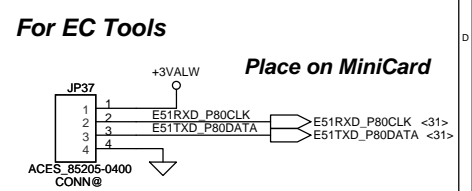
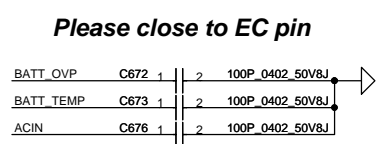
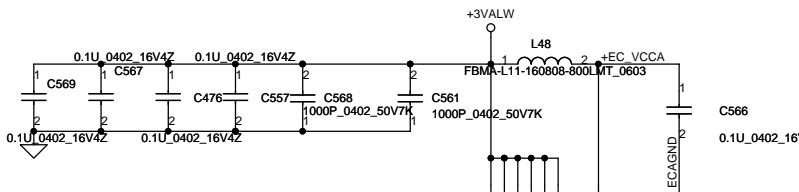
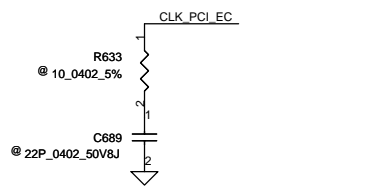


**XTAL\_CTR**  
 If Open , use 12MHz. crystal  
 If Pull high , use CLKNG 48MHz.

Close to CLK\_SD 48M via

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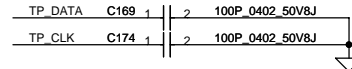
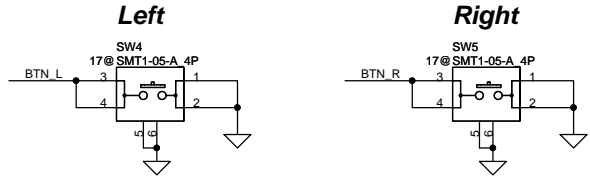
hexainf@hotmail.com  
 GRATIS - FOR FREE



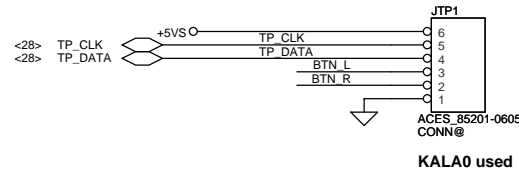
Chagne to D3 version

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For 17"

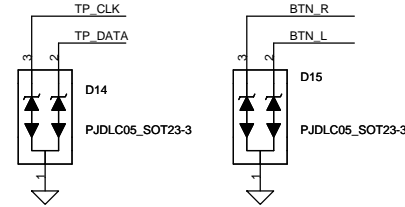
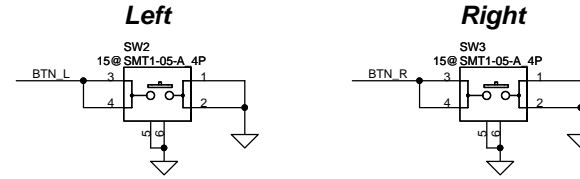


To TP/B Conn.

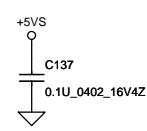


KALA0 used

For 15"



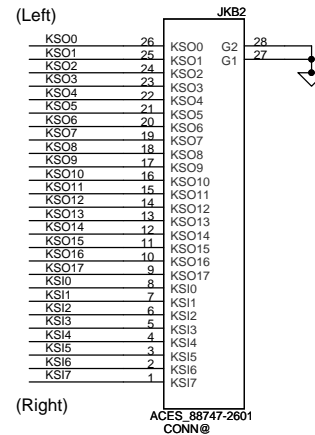
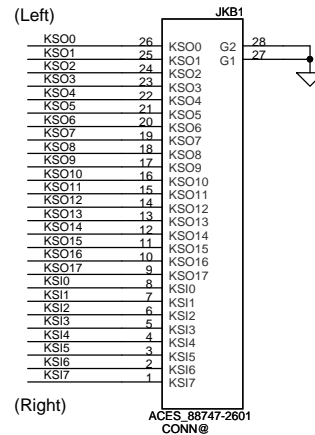
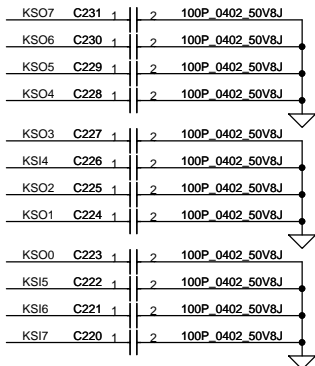
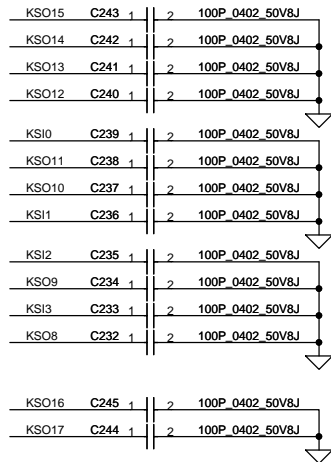
Change to SCA00000200



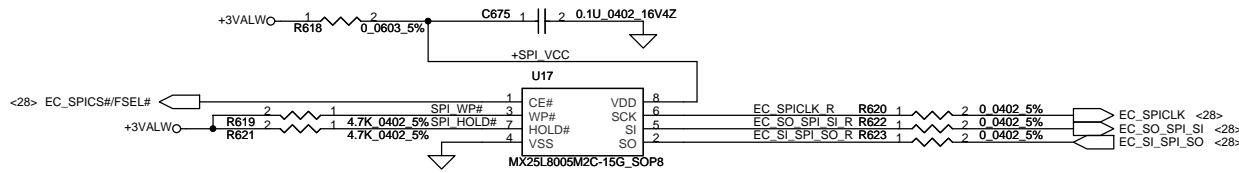
INT\_KBD Conn.



KB1 for 15"  
KB2 for 17"

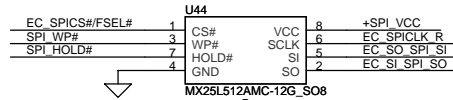
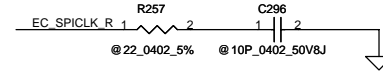


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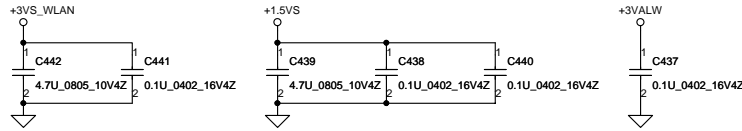
SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P  
 ENE suggestion SPI Frequency over 66MHz  
 SST: 50MHz  
 MXIC: 70MHz  
 ST: 40MHz

**ONLY MXIC used in this project (66MHz)**

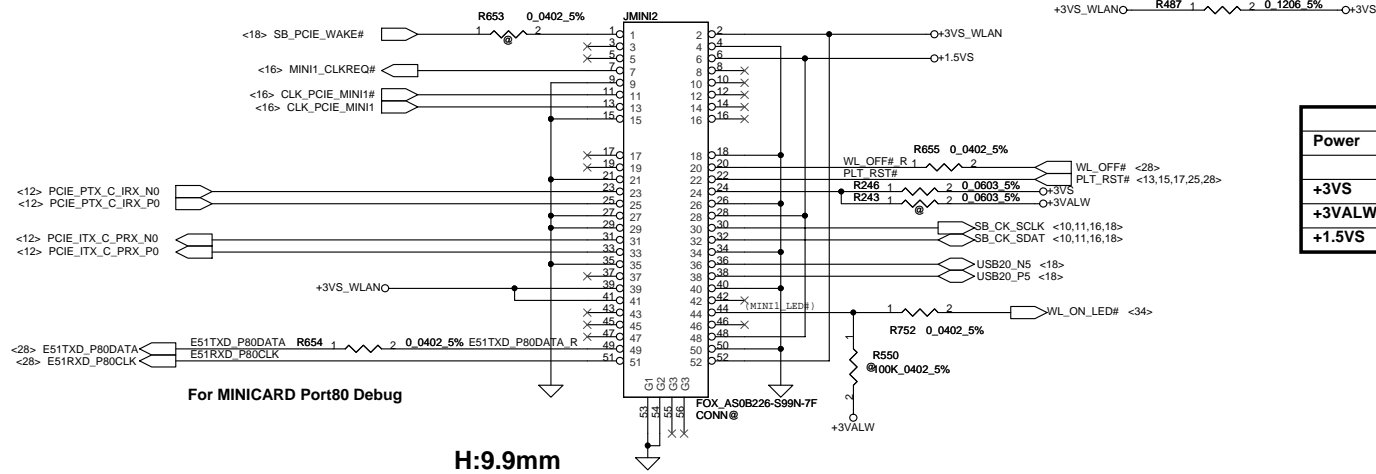


Reserved for BIOS simulator.  
 Footprint S08  
**SPI ROM Footprint 150mil**

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### For Wireless LAN

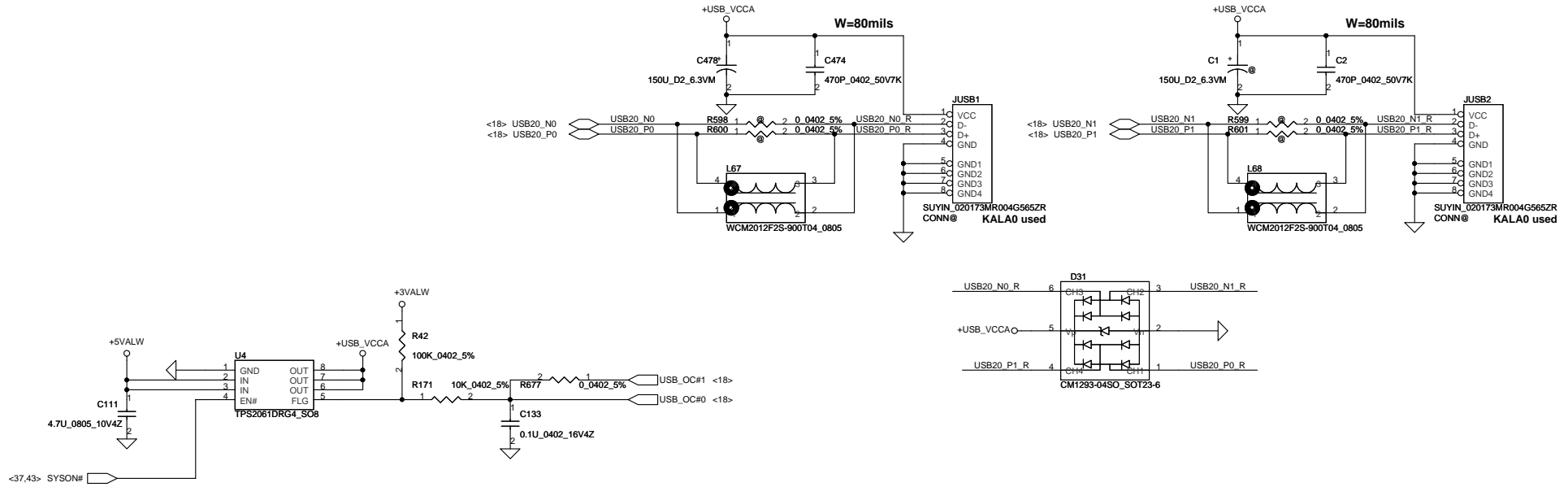


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

H:9.9mm

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### USB CONN. 1 & 2

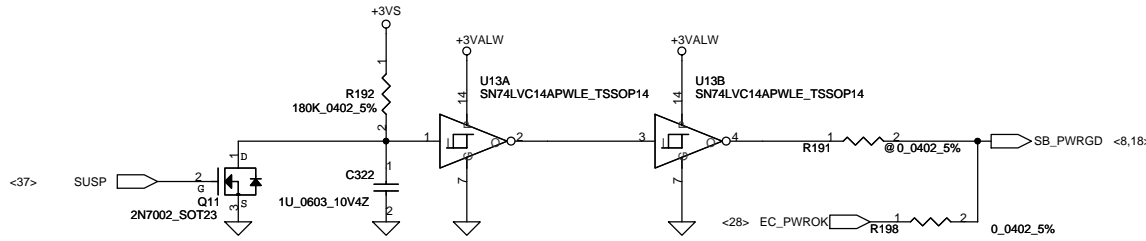


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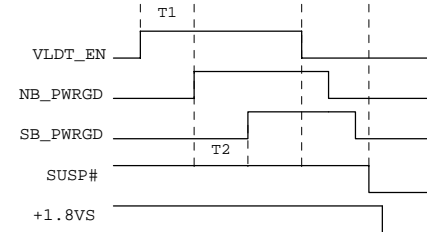


### Power ON Circuit

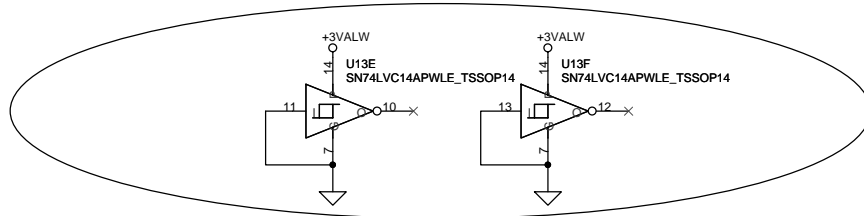
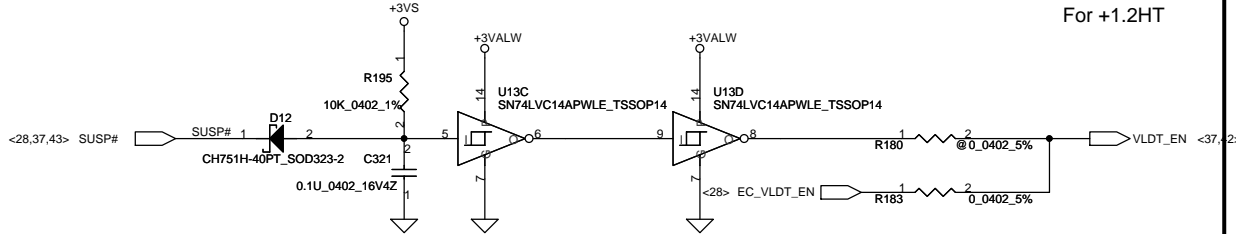
For South Bridge



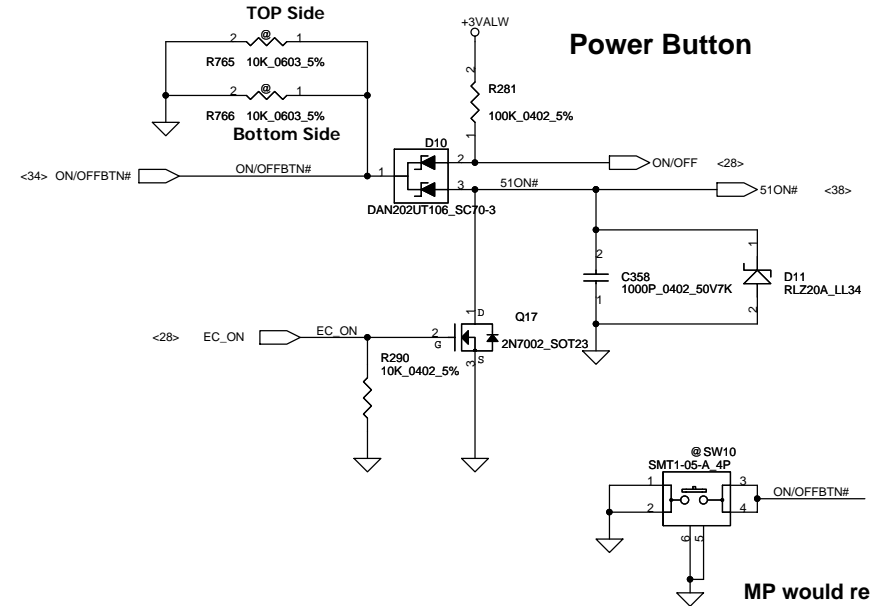
note: T1 minimum 15ms, T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB\_PWRGD goes to low for power down.



For +1.2HT

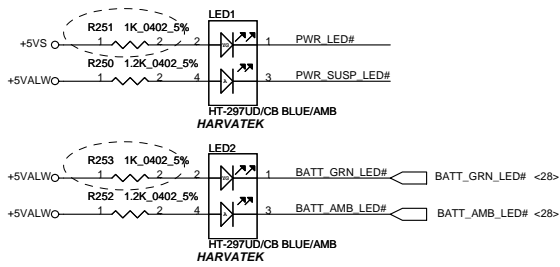
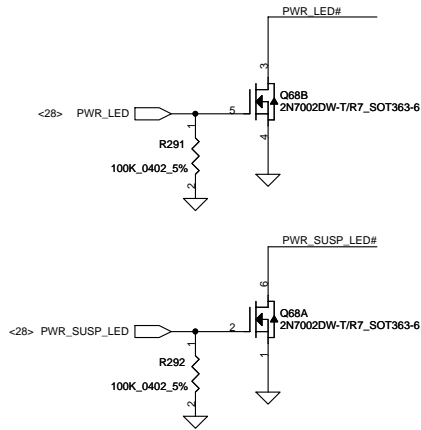


### Power Button

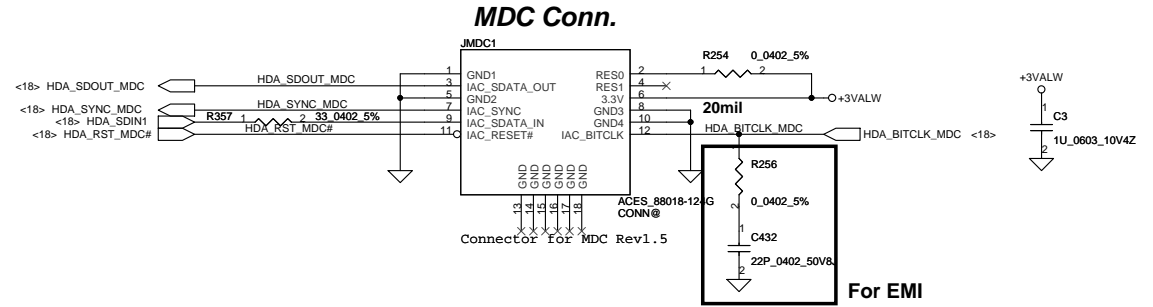


MP would remove

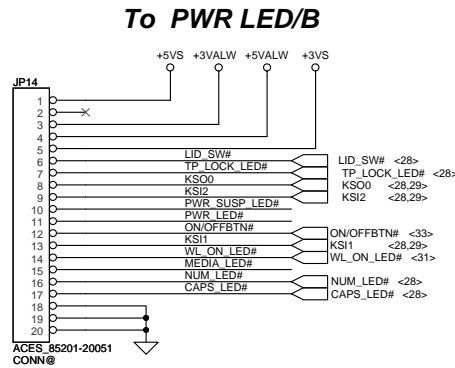
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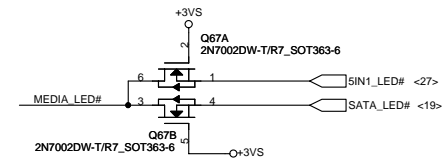
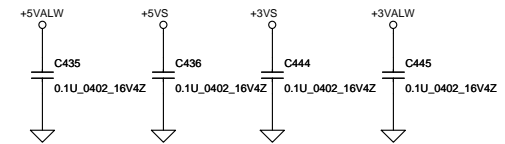
**BLUE/AMB LED**



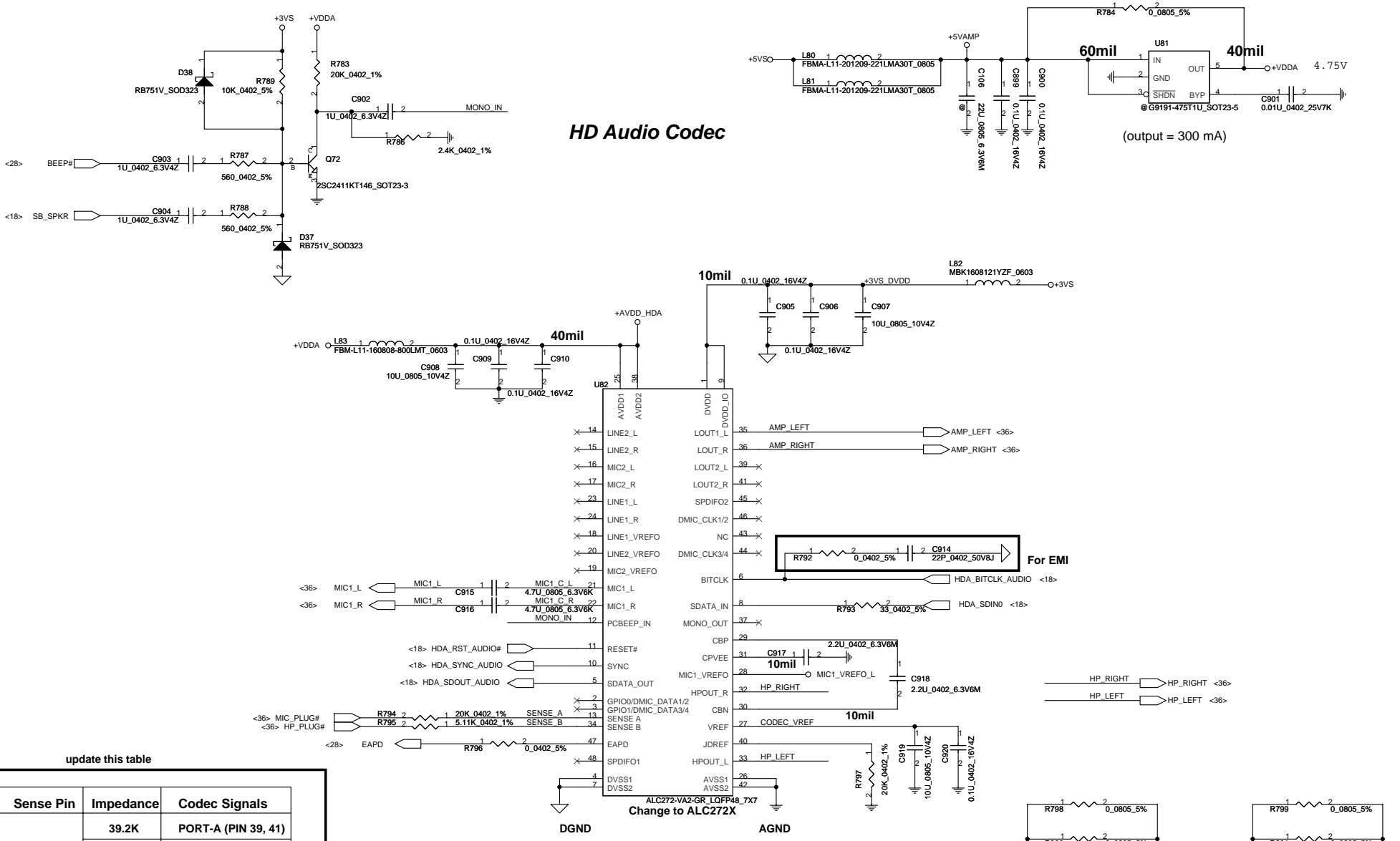
**For EMI**



	<b>KSO0</b>
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	

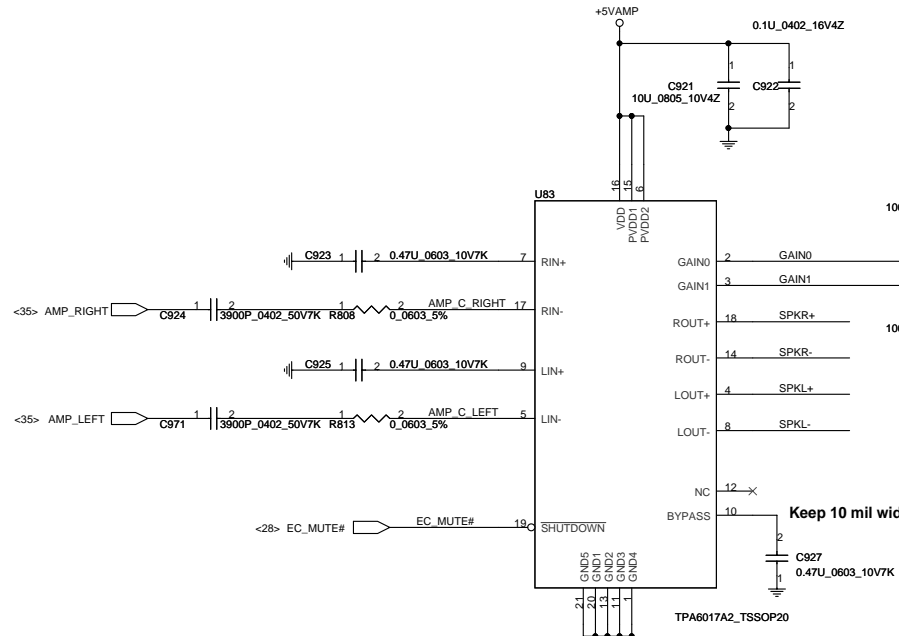


# HD Audio Codec

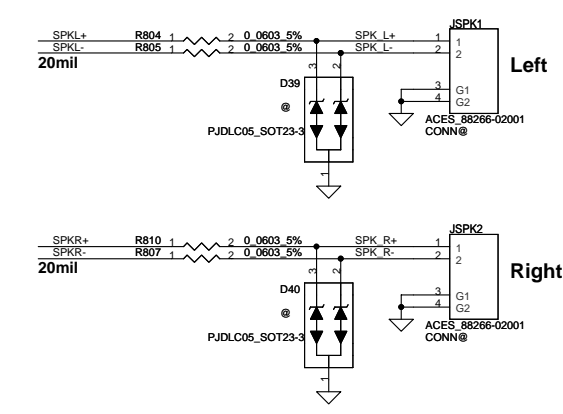


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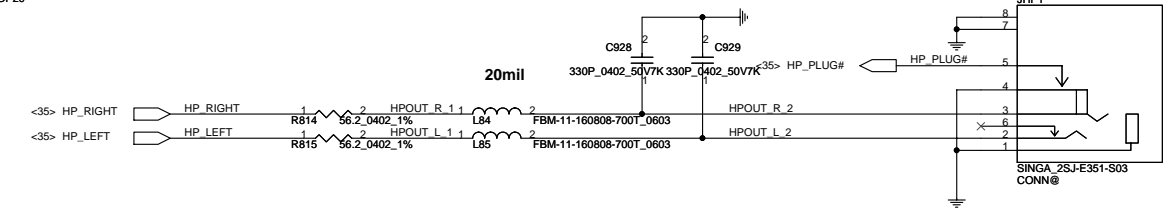
hexainf@hotmail.com  
GRATIS FOR FREE



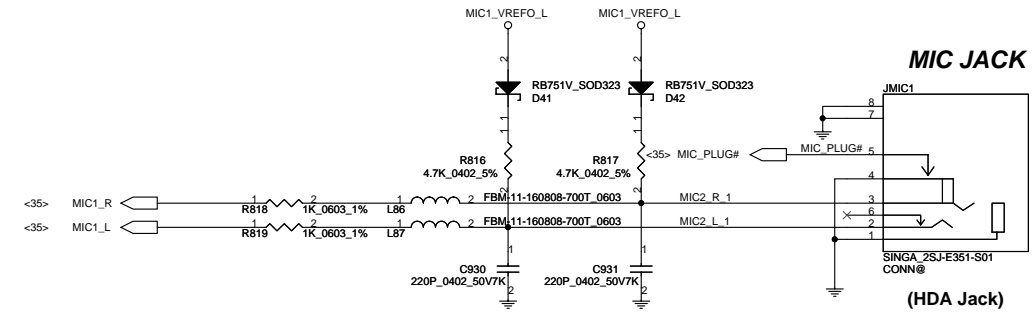
**Int. Speaker Conn.**



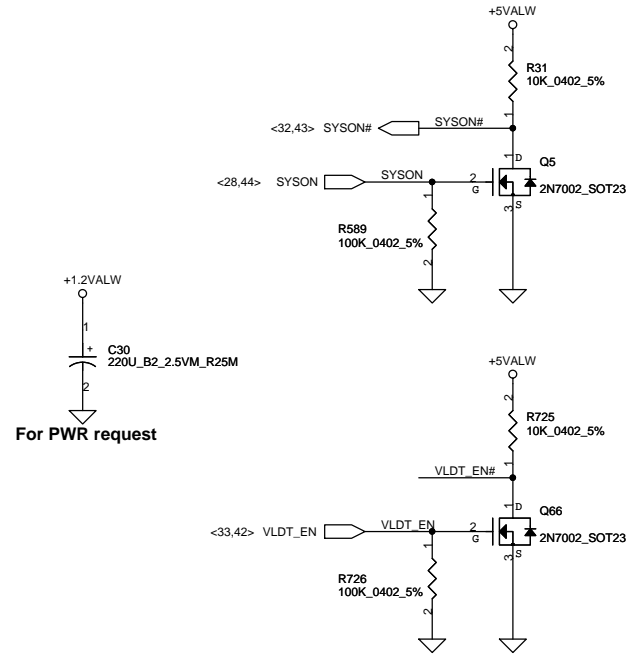
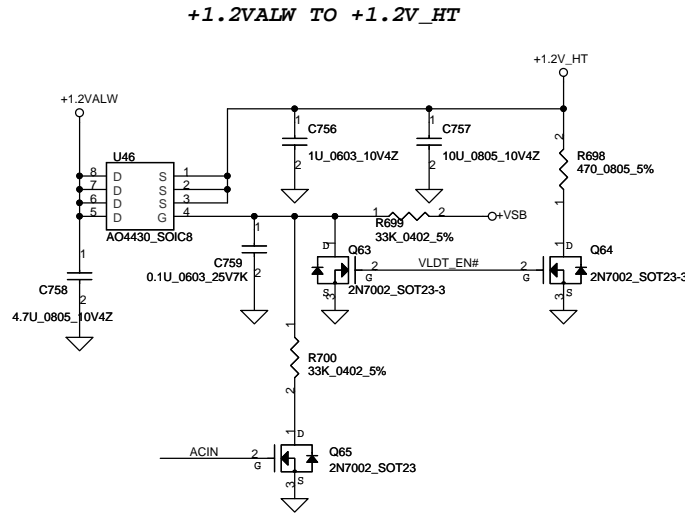
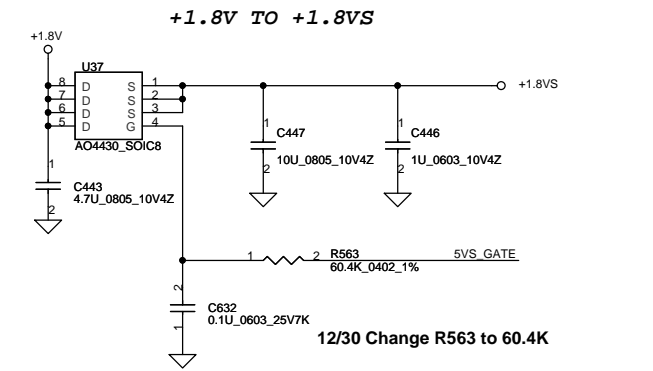
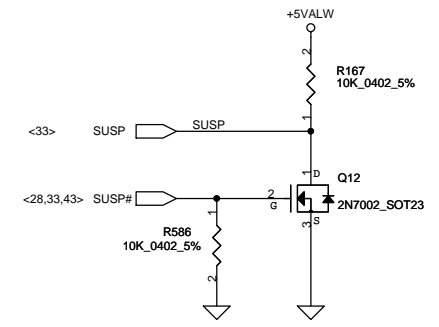
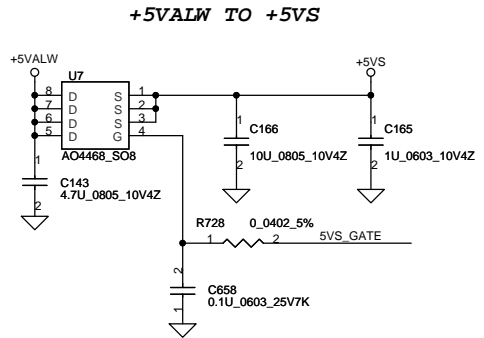
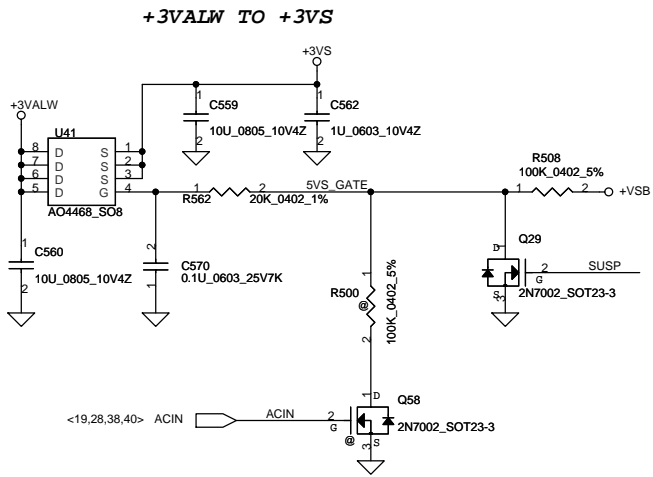
**LINE Out/Headphone Out**



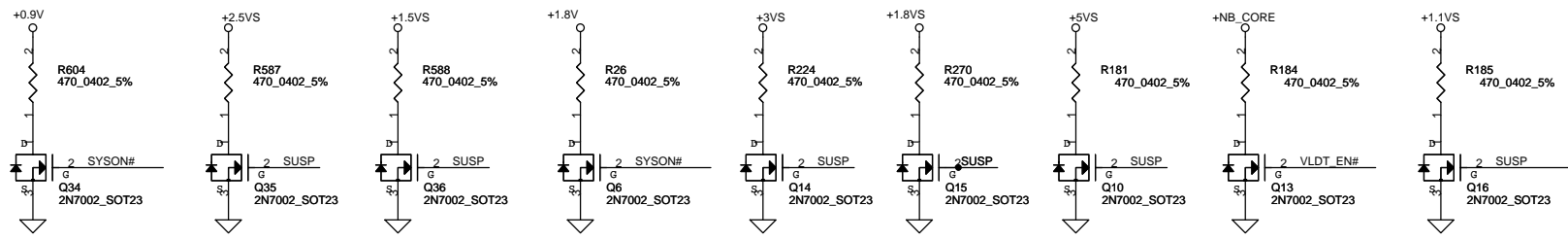
**MIC JACK**



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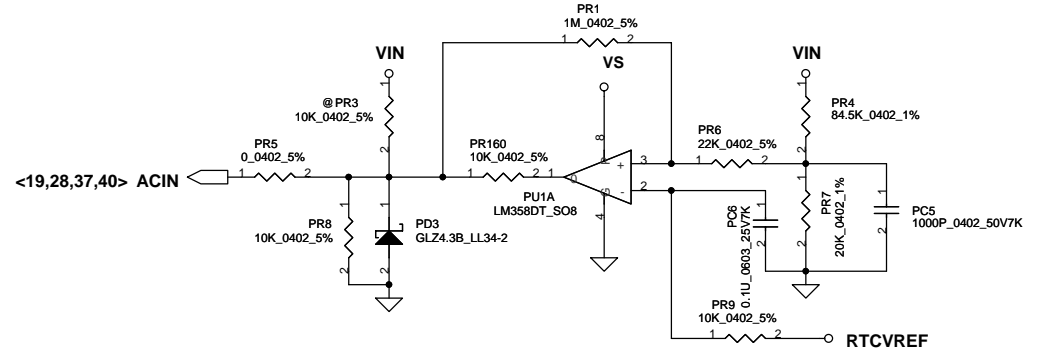
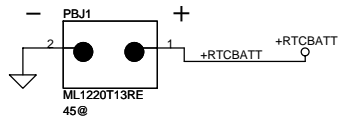
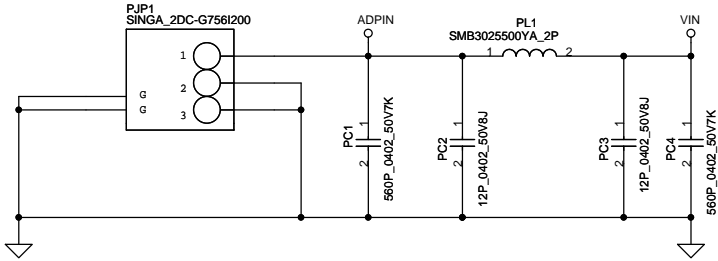
For PWR request



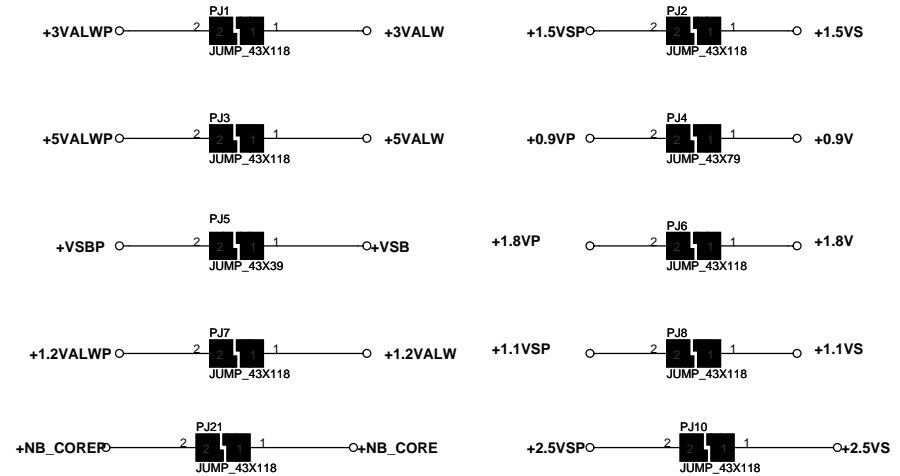
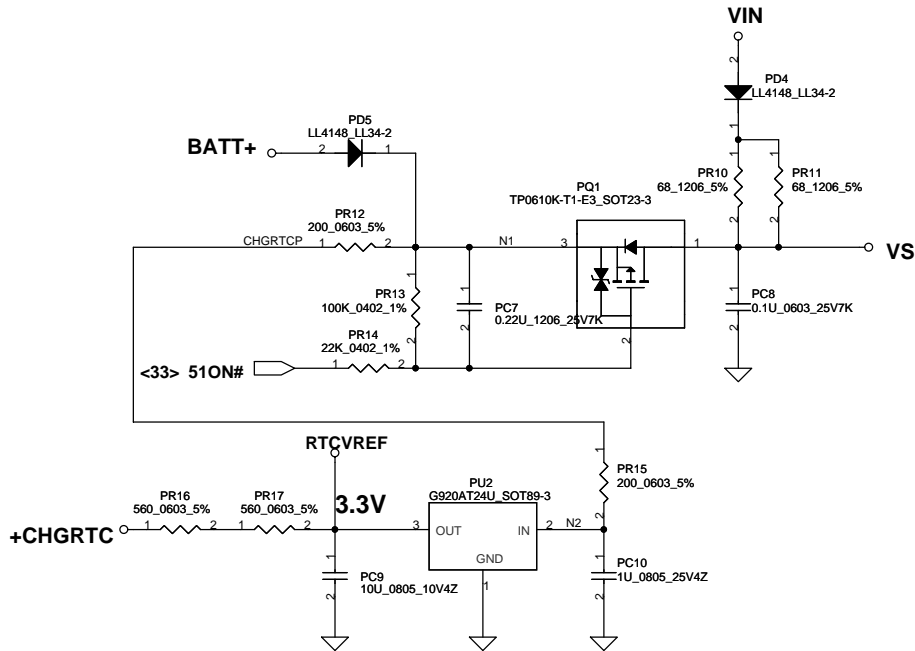
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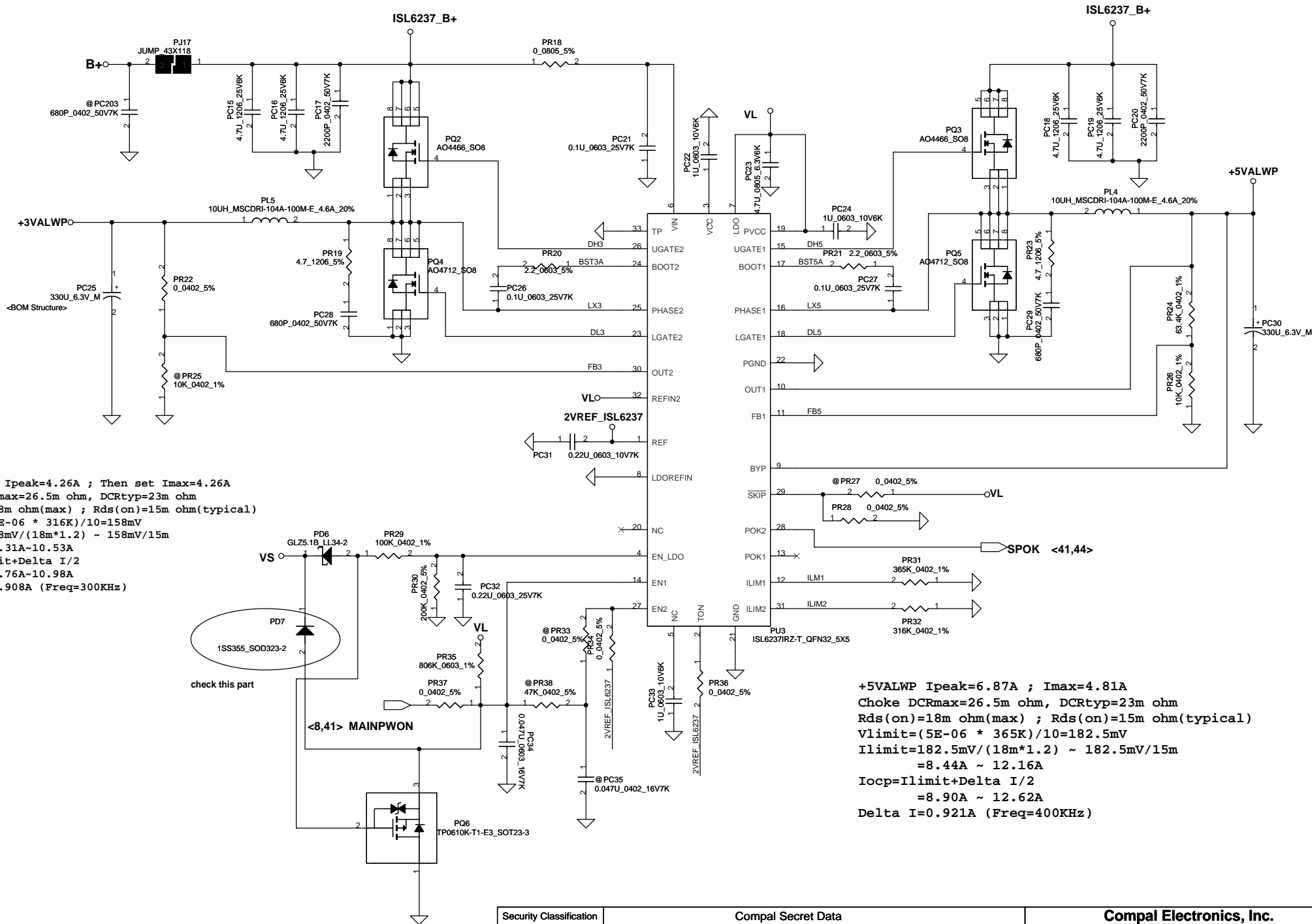
**DC231000500**



Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

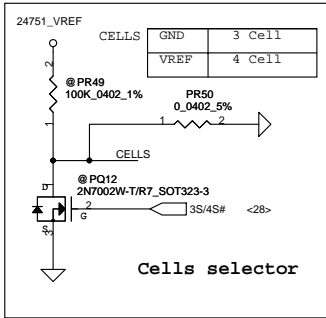
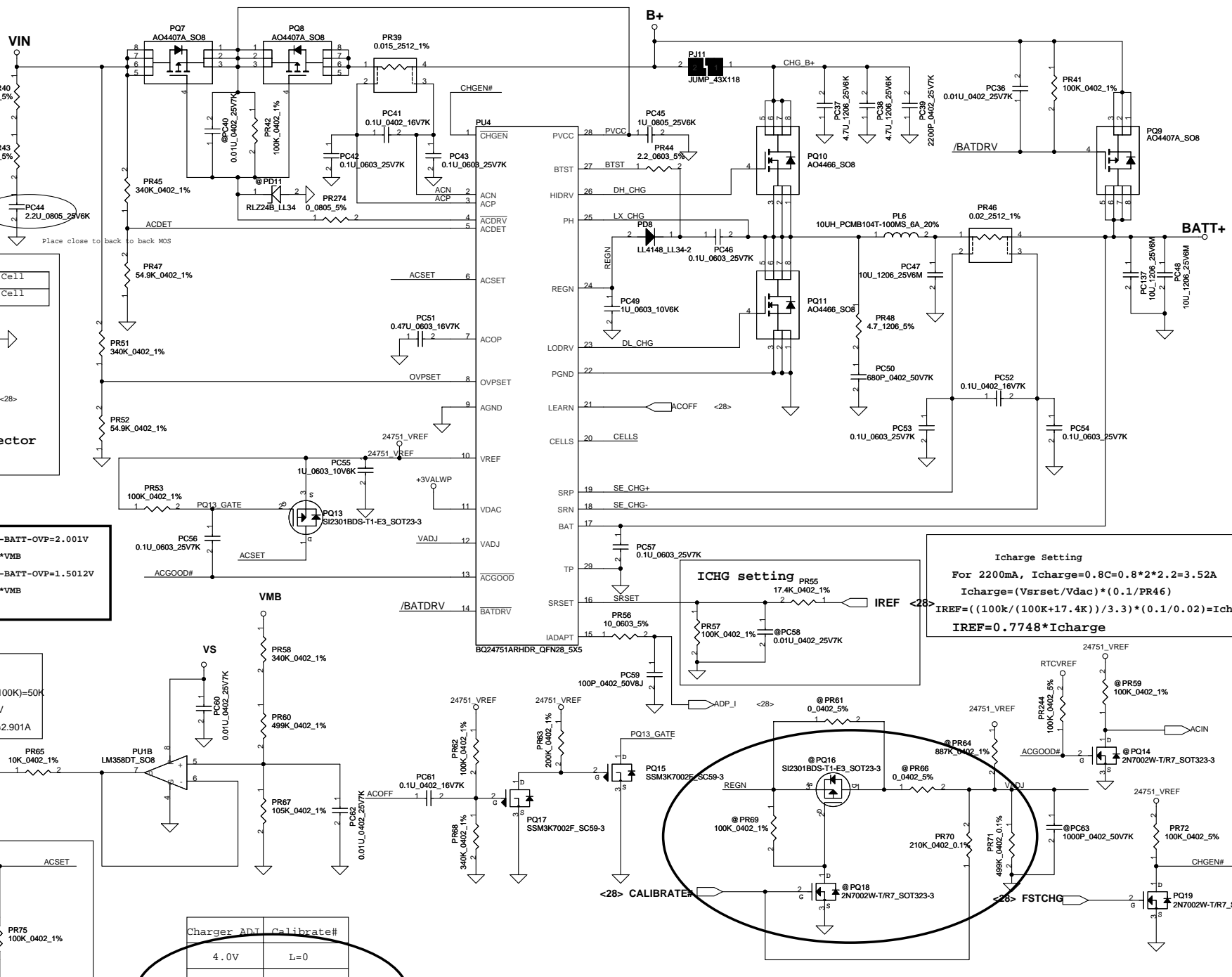


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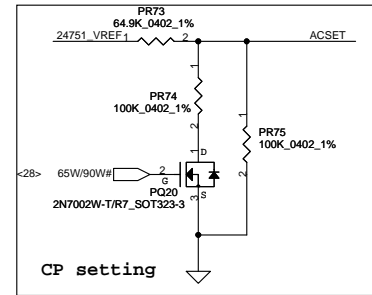
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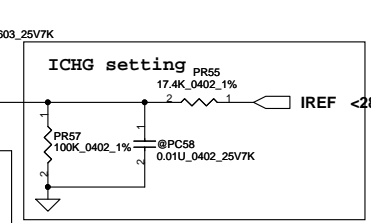
Input OVP : 22.3V  
 Input UVP : 17.26V  
 Fsw : 300KHz

LI-4S : 18.0V----BATT-OVP=2.001V  
 BATT-OVP=0.1112\*VMB  
 LI-3S : 13.5V----BATT-OVP=1.5012V  
 BATT-OVP=0.1112\*VMB  
 per cell=3.5V

CP Point Setting  
 CP point=ladapter\*85%  
 65W adapter R=(100K\*100K)/(100K+100K)=50K  
 Vacset=3.3\*(50K/(50K+64.9K))=1.436V  
 CP POINT=(1.436V/3.3V)\*(0.1/0.015)=2.901A



Charger ADI	Calibrate#
4.0V	L=0
4.2V	1.8755V
4.3V	2.8132V
4.35V	H=3.3V

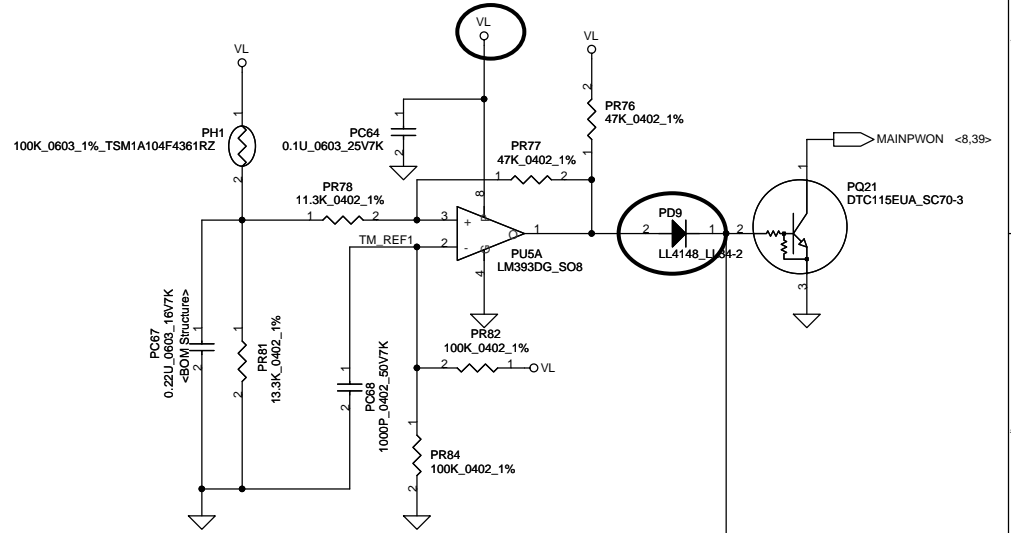


Icharge Setting  
 For 2200mA, Icharge=0.8C=0.8\*2\*2.2=3.52A  
 Icharge=(Vsrset/Vdac)\*(0.1/PR46)  
 $IREF = ((100k / (100k + 17.4k)) / 3.3) * (0.1 / 0.02) = Icharge$   
 IREF=0.7748\*Icharge

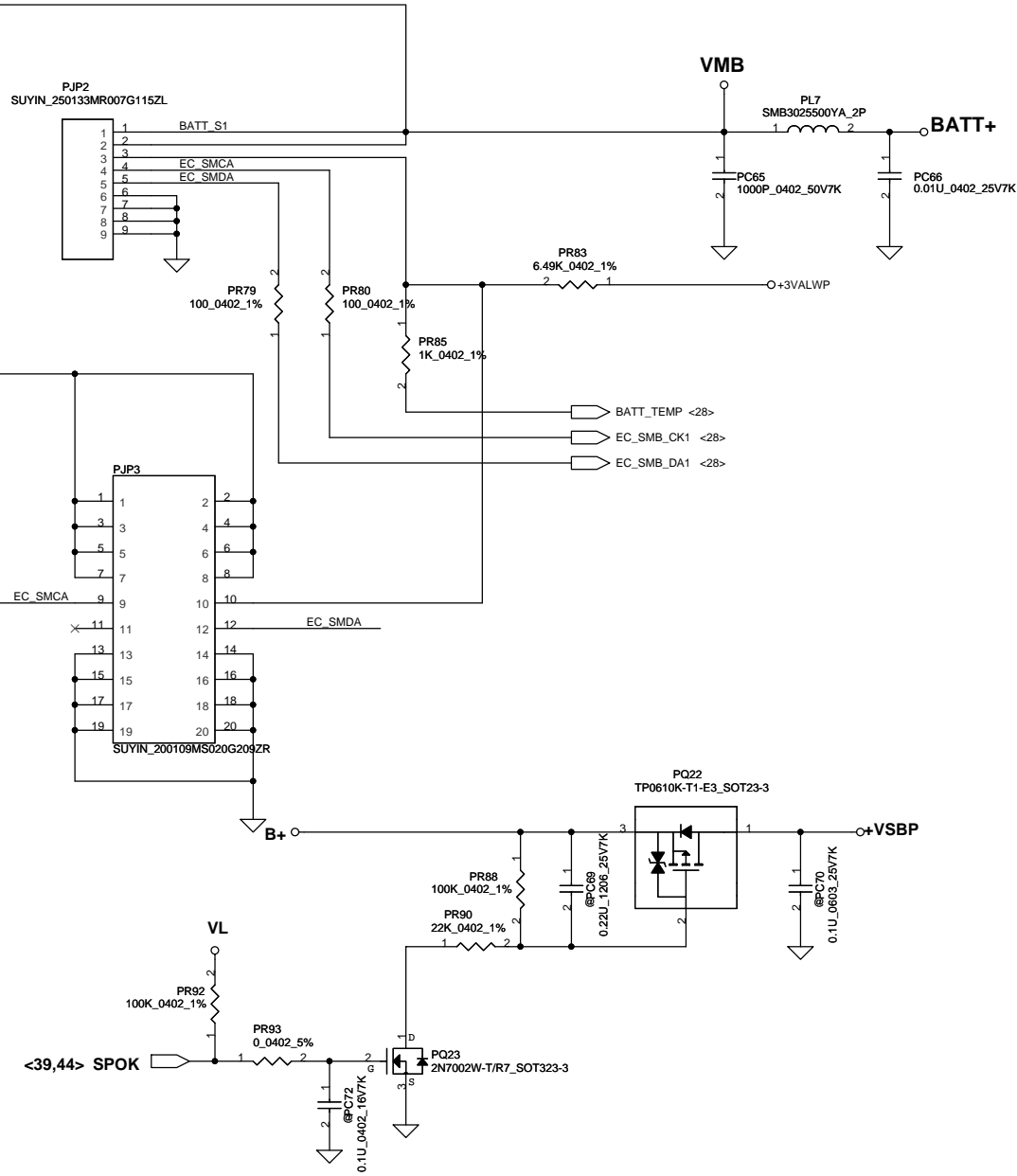
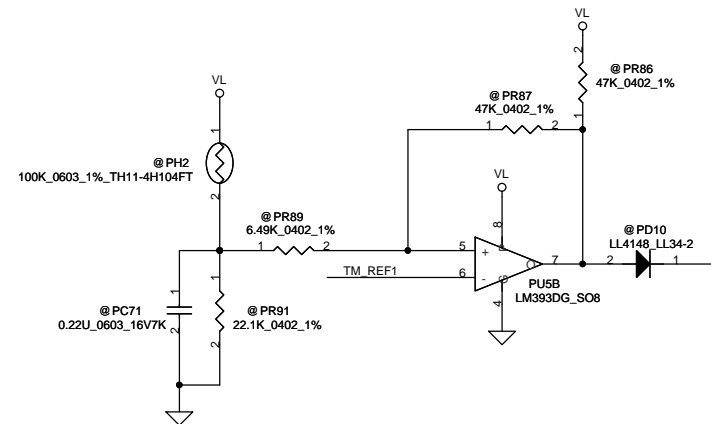
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PH1 under CPU bottom side :  
CPU thermal protection at 92 degree C

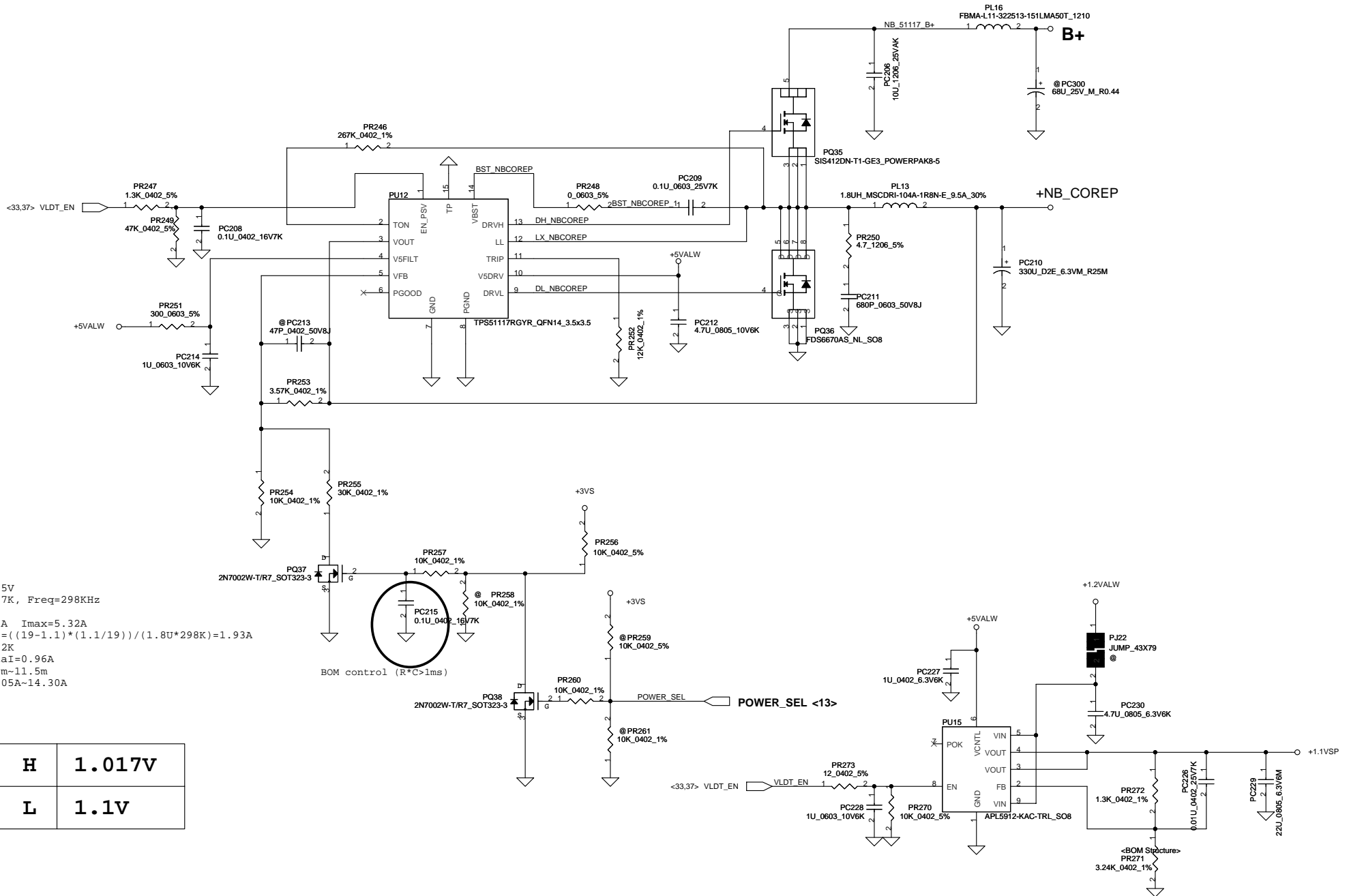


PH2 near main Battery CONN :  
BAT. thermal protection at 75 degree C



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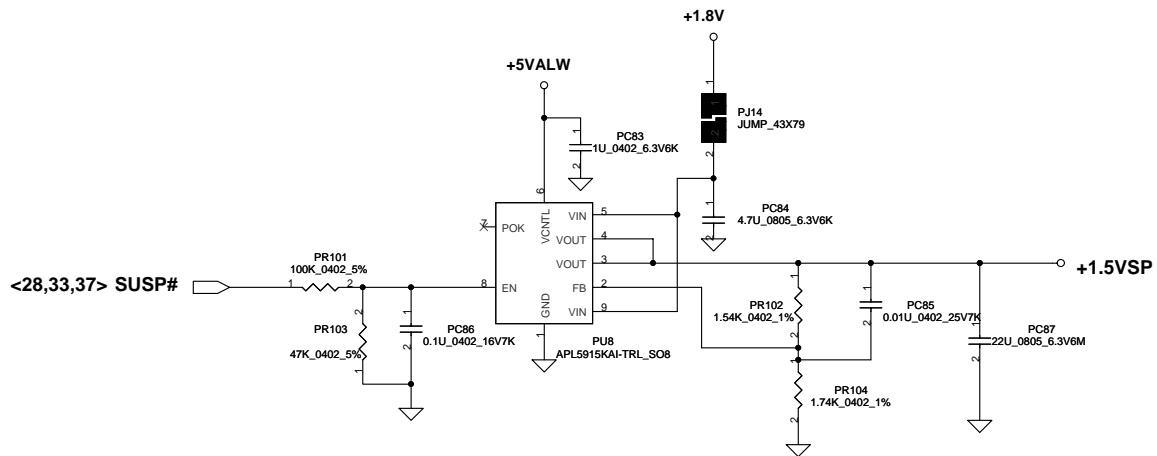
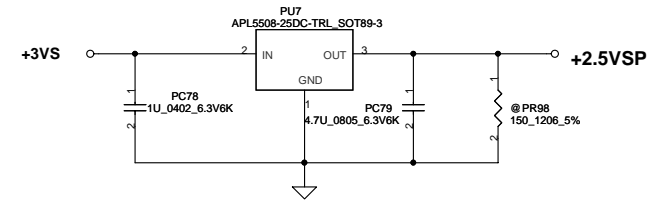
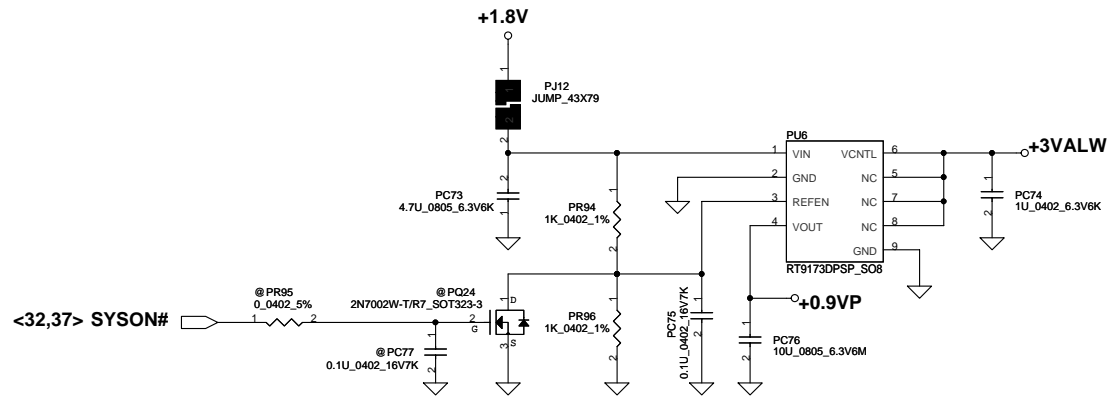


VFB=0.75V  
 Rton=267K, Freq=298KHz  
 Ipeak=7A Imax=5.32A  
 $\Delta I = ((19-1.1) * (1.1/19)) / (1.8U * 298K) = 1.93A$   
 Rtrip=12K  
 $1/2 \Delta I = 0.96A$   
 Rdson=9m~11.5m  
 Iocp=9.05A~14.30A

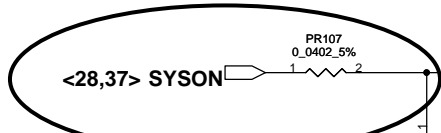
BOM control (R\*C>1ms)

H	1.017V
L	1.1V

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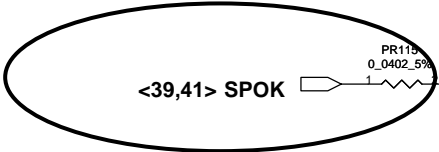
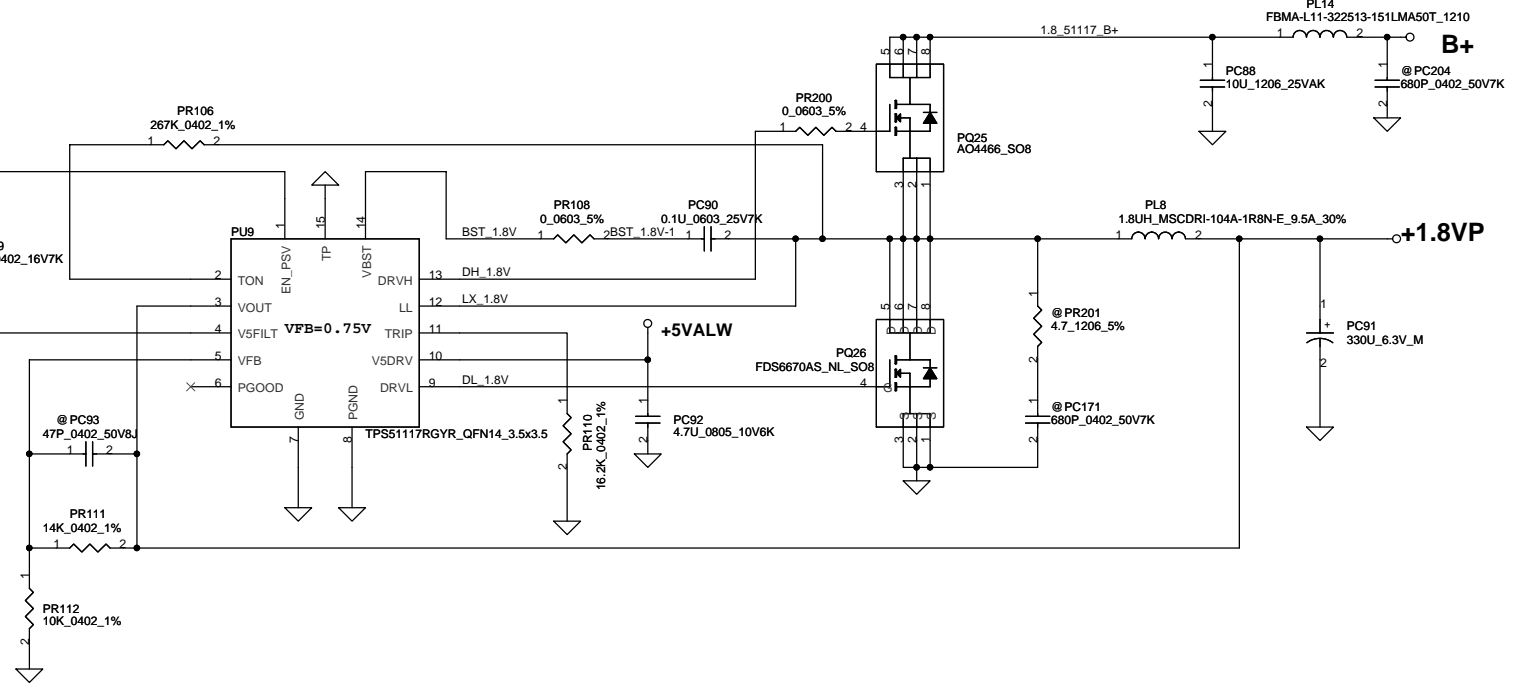
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VFB=0.75V  
 $V_o = VFB * (1 + PR111 / PR112) = 0.75 * (1 + 14K / 10K) = 1.8V$   
 $R_{ton} = 267K \Rightarrow F_{sw} = 297KHz$

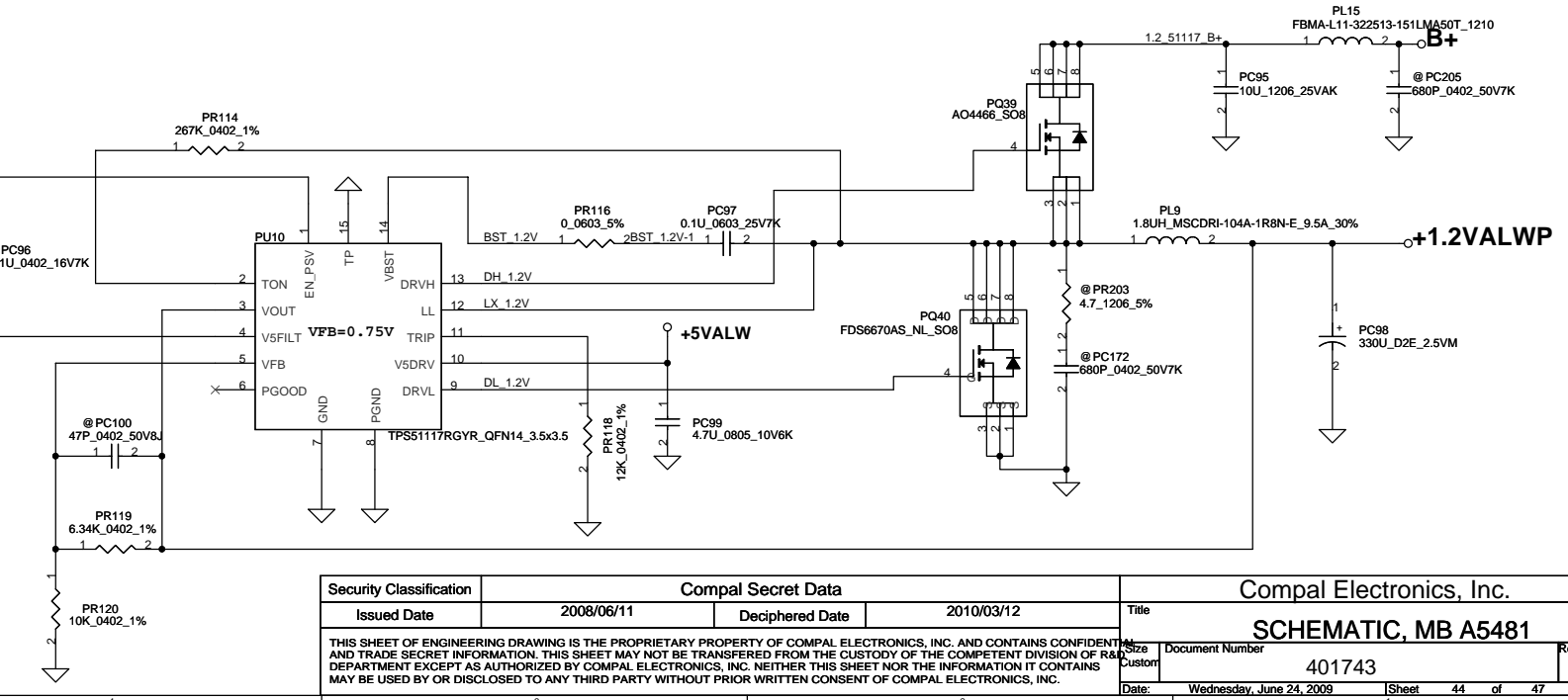
Cout ESR=15m ohm  
 $I_{peak} = 11.96A, I_{max} = 8.372A$   
 $\Delta I = ((19-1.8) * (1.8/19)) / (L * F_{sw})$   
 $((19-1.8) * (1.8/19)) / (1.8u * 297000) = 3.048A$   
 $\Rightarrow 1/2 \Delta I = 1.524A$

Rtrip=16.2K  
 $I_{ocp} = 12.39A \sim 20.69A$

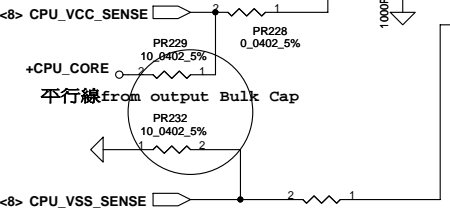
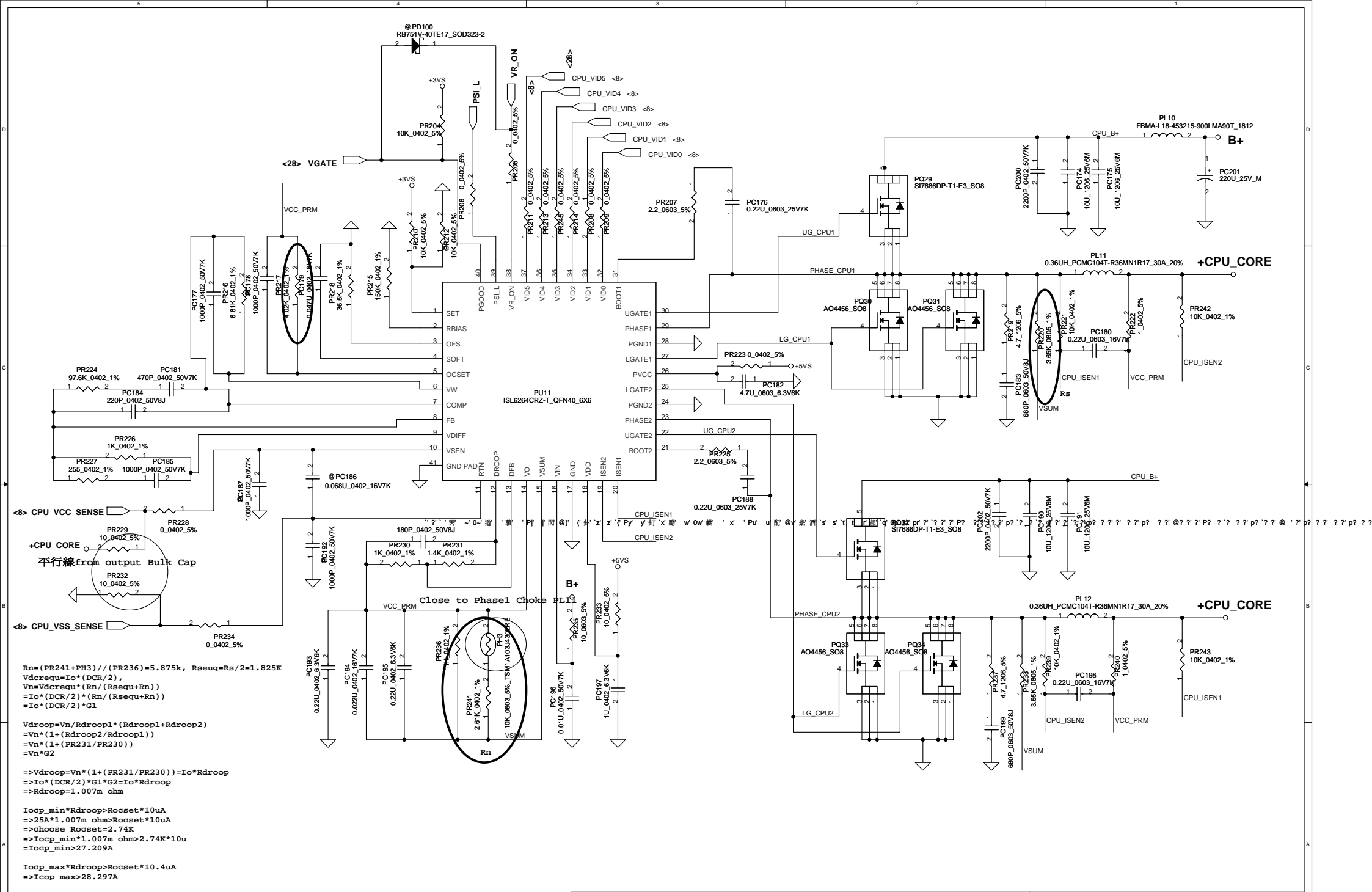


VFB=0.75V  
 $V_o = VFB * (1 + PR119 / PR120) = 0.75 * (1 + 6.04K / 10K) = 1.203V$   
 $R_{ton} = 267K \Rightarrow F_{sw} = 298KHz$

1.2VP Ipeak=7.4A ; Imax=5.180A  
 $\Delta I = ((19-1.2) * (1.2/19)) / (L * F_{sw})$   
 $((19-1.2) * (1.2/19)) / (1.8u * 298000) = 2.10A$   
 $\Rightarrow 1/2 \Delta I = 1.05A$   
 $R_{dson} = 11.5m / 9m \text{ ohm}$   
 set Rtrip=12K  
 $I_{ocp\_min} = 9.11A$   
 $I_{ocp\_max} = 14.38A$



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$R_n = (PR241 + PH3) / (PR236) = 5.875k$ ,  $R_{seque} = R_s / 2 = 1.825k$   
 $V_{dcreq} = I_o * (DCR / 2)$   
 $V_n = V_{dcreq} * (R_n / (R_{seque} + R_n))$   
 $I_o = I_c * (DCR / 2) * (R_n / (R_{seque} + R_n))$   
 $I_o = I_c * (DCR / 2) * G1$   
 $V_{droop} = V_n / R_{droop1} * (R_{droop1} + R_{droop2})$   
 $= V_n * (1 + (R_{droop2} / R_{droop1}))$   
 $= V_n * (1 + (PR231 / PR230))$   
 $= V_n * G2$   
 $=> V_{droop} = V_n * (1 + (PR231 / PR230)) = I_o * R_{droop}$   
 $=> I_o = (DCR / 2) * G1 * G2 = I_o * R_{droop}$   
 $=> R_{droop} = 1.007m\ ohm$   
 $I_{ocp\_min} * R_{droop} > R_{ocset} * 10\ \mu A$   
 $=> 25A * 1.007m\ ohm > R_{ocset} * 10\ \mu A$   
 $=> choose\ R_{ocset} = 2.74k$   
 $=> I_{ocp\_min} * 1.007m\ ohm > 2.74k * 10\ \mu A$   
 $=> I_{ocp\_min} > 27.209A$   
 $I_{ocp\_max} * R_{droop} > R_{ocset} * 10.4\ \mu A$   
 $=> I_{ocp\_max} > 28.297A$   
 $I_{ocp} = -27.209A - 28.297A$

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	HW required to adjust from 1.14V to 1.12V	HW required to adjust from 1.14V to 1.12V	0.1	42	Change PR271 from SD034300180 (S RES 1/16W 3K +-1% 0402) to SD034324180 (S RES 1/16W 3.24K 0402 1%)	09, 05/07	to PVT
2	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Add PC208 SE076104K80 (S CER CAP .1U 16V K X7R 0402)	09, 05/07	to PVT
3	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Change PR247 from SD028000080 (S RES 1/16W 0 +-5% 0402) to SD028130180 (S RES 1/16W 1.3K 0402 5%)	09, 05/07	to PVT
4	NB_COREP working frequency has issue.	Because NB_COREP working frequency will be gitter while system at heavy loading. Change to larger ESR Cap will be solve.	0.1	42	Change PC210 from SGA19331D00 (S POLY C 330U 2.5V M D2 TPE LESR15M H1.8) to SGA00002B00 (S POLY C 330U 6.3V M D2E ESR25M TPE H1.8)	09, 05/07	to PVT
5	BOM error	BOM error	0.1	42	Add PR270 SD28100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
6	BOM error	BOM error	0.1	42	Change PR103 from SD028470280(S RES 1/16W 47K 0402 5%) to SD028100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
7							
8							
9							
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Version change list (P.I.R. List) for HW

Item	Reason for change	Modify List	PG#	Date	Item	Reason for change	Modify List	Rev.	PG#
1	PWR update circuit			4/9	26				
2	BOM change	R118 reserve	P.18	4/9	27				
3	BOM change	Change R178, R179 to 90.9/158 ohm	P.16	4/9	28				
4	BOM change	R30, R39 reserve	P.24	4/9	29				
5	BOM change	Add C30	P.38	4/9	30				
6	BOM change	Add R634, R639	P.28	4/9	31				
7	BOM change	C383 Reserve	P.24	4/9	32				
8		Pop R419	P.20	4/10	33				
9	PWR update circuit			5/15					
10	For Panel flash issue	R1.D2 Reserve, pop R763	P.24	5/18					
11	For Panel flash issue	Add R414 and non-pop	P.24	5/18					
12	Lid_SW intial issue	Add R19	P.28	5/18					
13	HPET timer issue	Change C288,C290 to 33P	P.16	5/18					
14	BOM change	change C276,C279 10P to 27P	P.19	5/19					
15									
16									
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18									
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22									
23									
24									
25									

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