

Compal confidential

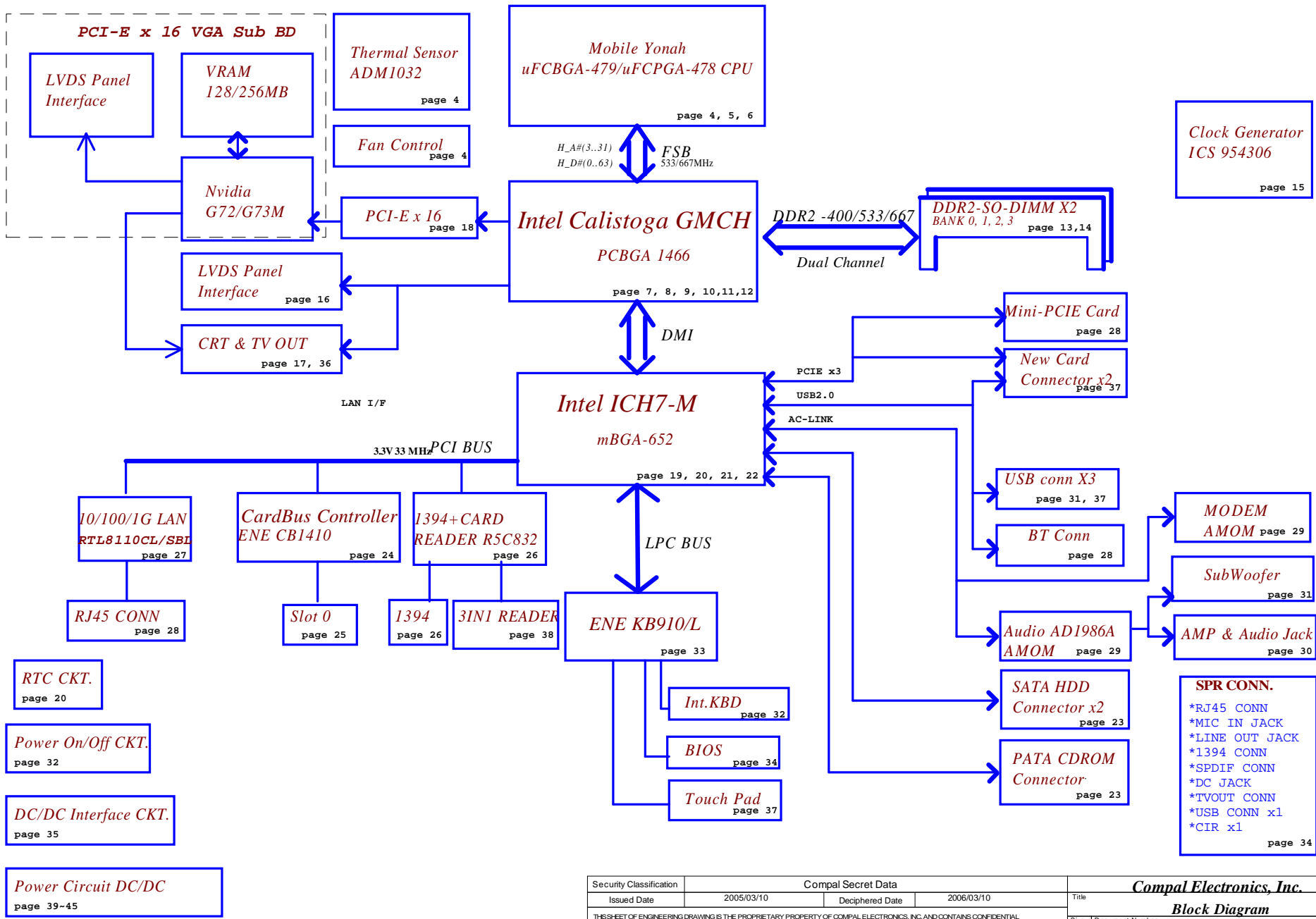
IGL50/51 Schematics Document

Mobile Yonah uFCPGA with Intel
Calistoga_GM/PM+ICH7-M core logic

2006-05-15

REV:0.1

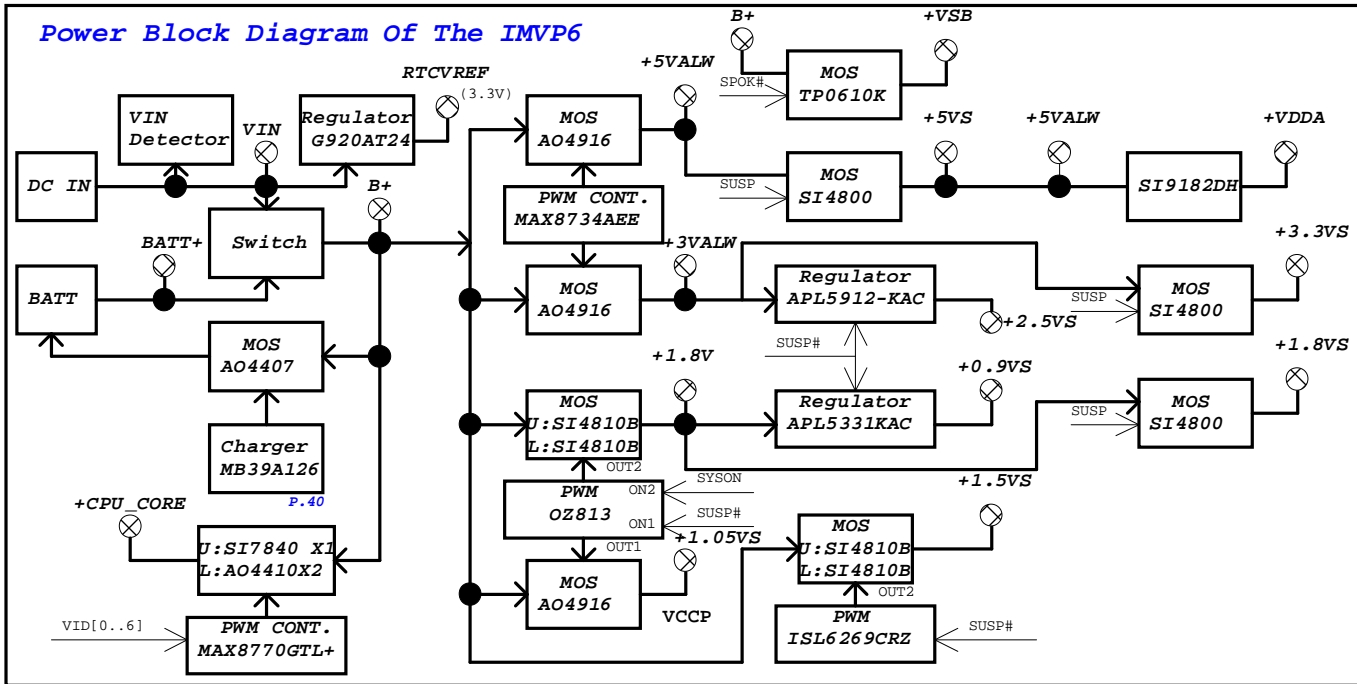
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				Custom	IGL50/51 LA-3771	0.1
Date:	星期四, 六月 08, 2006	Sheet	1	of	48	



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Block Diagram	
Size	Document Number
Customer	IGL50/51 LA-3771
Date: 星期日, 六月 08, 2006	Sheet 2 of 48
Rev	0.1

Power Block Diagram Of The IMVP6



+3VALW	KB910L SB RTL8110SBL/CL	mA 160mA
+CPU_CORE	CPU	36A
+VCCP	CPU NB	2.5A 9.8A (14.7A)
+5VS	EXPRESS CARD HDD ODD MDC APA2066 TPA0211 AD1986 USB PORT * 6	1A 1.5A 1.8A 300mA 1A mA 70mA 3A
+3VS	NB EXPRESS CARD CLK_GEN LCDVCC VGA CARD (G7XM) SB R5C832 BIOS ROM KB910L CB1410	480mA 1A 200mA 1A 655mA 680mA mA 15mA 200mA mA
+2.5VS	VGA CARD (G7XM) NB	130mA (143mA)
+1.8V	DDR2_DIMM NB (667Mhz)	8A 3.1A
+1.8VS	GDDR2 VGA CARD (G7XM)	6A 4.06A
+0.9VREF	DDR2_DIMM	10mA
+0.9VS	GDDR2 DDR2_DIMM	1A 2A
+1.5V	SB	40mA
+1.5VS	NB SB MiniCard EXPRESS CARD VGA CARD (G7XM)	8.9A (13.8A) 3.8A 1A 0.65A 2A

PCI DEVICES

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS CB1410	AD20	2	PCI_PIRQA#
CARD READER & 1394 R5C832	AD22	0	PCI_PIRQG# PCI_PIRQH#
LAN CONTROLLER RTL8110SBL/CL	AD17	3	PCI_PIRQF#

Voltage Rails

power plane	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +VGA_CORE +1.2VS +0.9VS +CPU_CORE +VCCP
State S4 : STD S5 : SOFT OFF				
S0	O	O	O	O
S1	O	O	O	O
S3 : STR	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

O MEANS ON
X MEANS OFF

PCIE LANE

LANE	DEVICE
1	Express Card
2	Mini Card

USB

PORT	DEVICE
0	LEFT SIDE
1	BLUE TOOTH
2	RIGHT SIDE
3	JP810
4	RIGHT SIDE
5	CMOS
6	RIGHT SIDE

I2C / SMB Address

KB910/L (SM1-Pulled-Up 5V)	
DEVICE	ADDRESS R/W
AT24C16AN	A3/A2 H
SMART BATTERY	17/16 H
KB910/L (SM2-Pulled-Up 3.3V)	
ADM1032AR	99/98 H
G7xM (I2CC-Pulled-Up 3.3V)	
G781-1 (RESERVED)	9B/9A
ICH7M SM Bus	
ICS9LPR325AKLFT	D3/D2 H (3.3V)
DDR II DIMMO	A1/AO H (3.3V)
DDR II DIMM1	A3/A2 H (3.3V)
Express Card	NC (2.5V)
Mini-Express	NC (2.5V)

BOM Structure

MARK	FUNCTION
@	NC FOR ALL
EXP@	PCIE-NEW CARD
BT@	BLUE TOOTH
UMA@	Internal 945GM
VGA@	External G7xM
SUBWOOFER@	SUBWOOFER
HGT30@	HGT30
CB@	PCMCIA/CARD BUS
GIGA@	8110SBL(SCL)Giga LAN
10/100@	8110CL 10/100Mb LAN

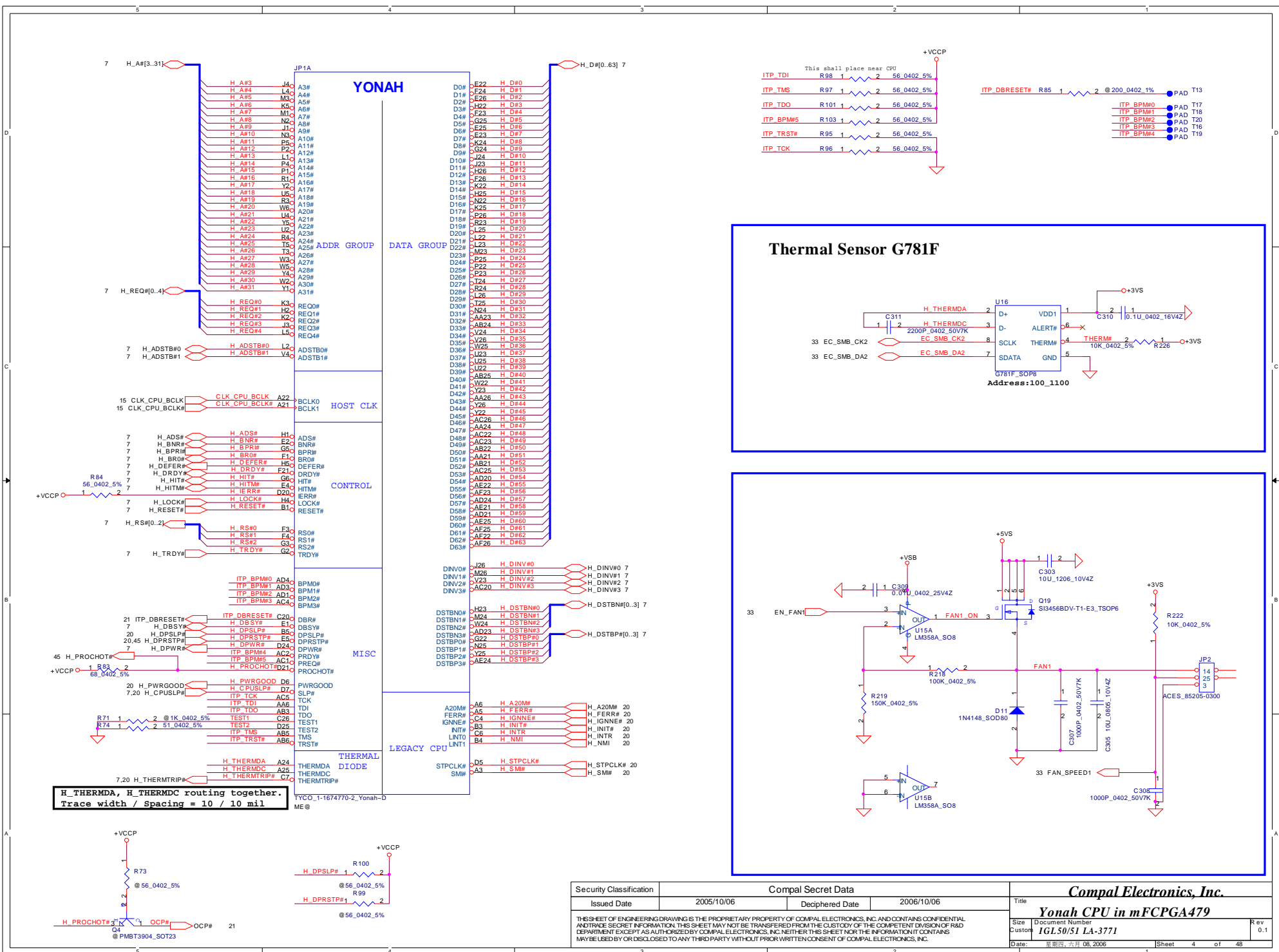
MB_ID

MB ID	P NAME
0	IGL-50
1	IGL-51

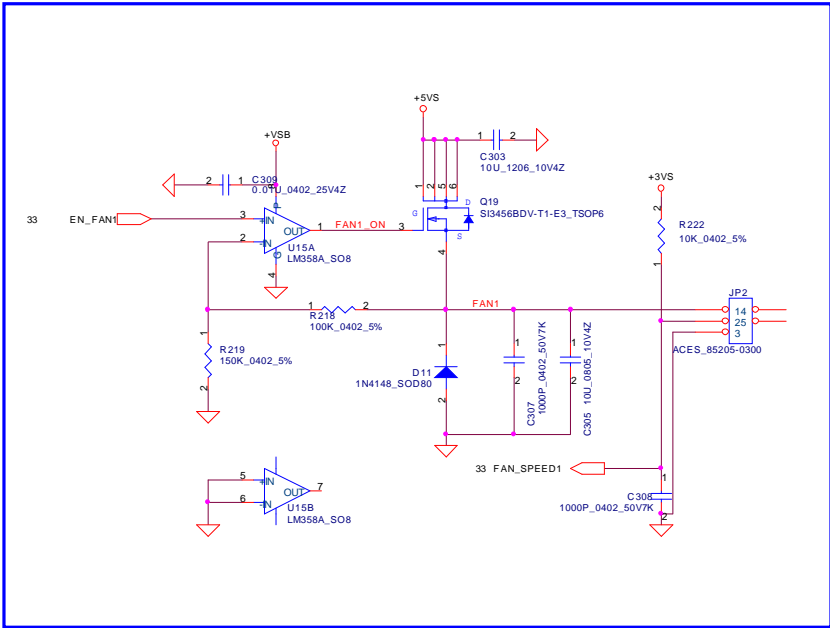
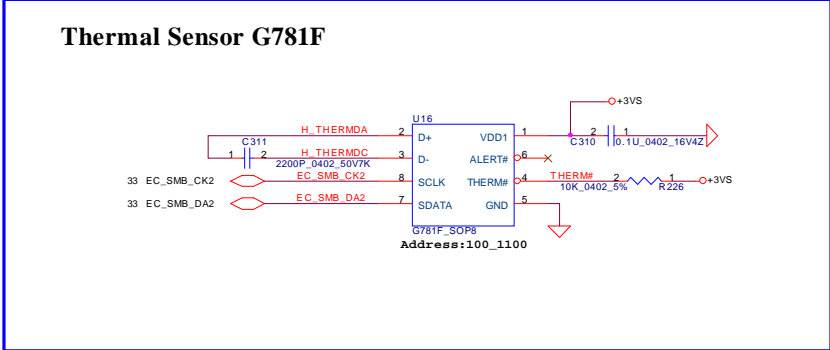
BRD_ID R119(Ra)=100K Ohm

ID	MB REV#	R115(Rb)	Vab
0	R0.1 (EVT)	0	0V
1	R0.2 (DVT)	8.2K	0.25V
2	R0.3 (PVT)	18K	0.50V
3	R1.0 (MP)	33K	0.82V
4		56K	1.19V
5		100K	1.65V
6		200K	2.20V
7		NC	3.30V

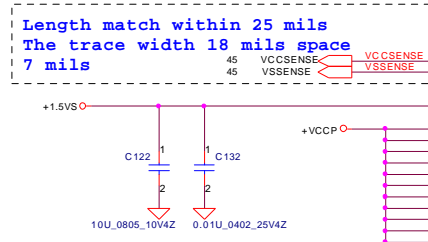
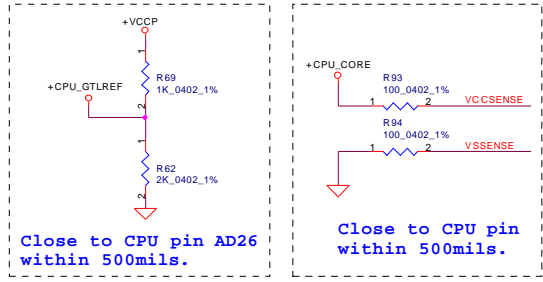
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				Document Number	0.1
				IGL50/SI LA-3771	
				Date:	Rev
				星期五, 六月 08, 2006	Sheet 3 of 48



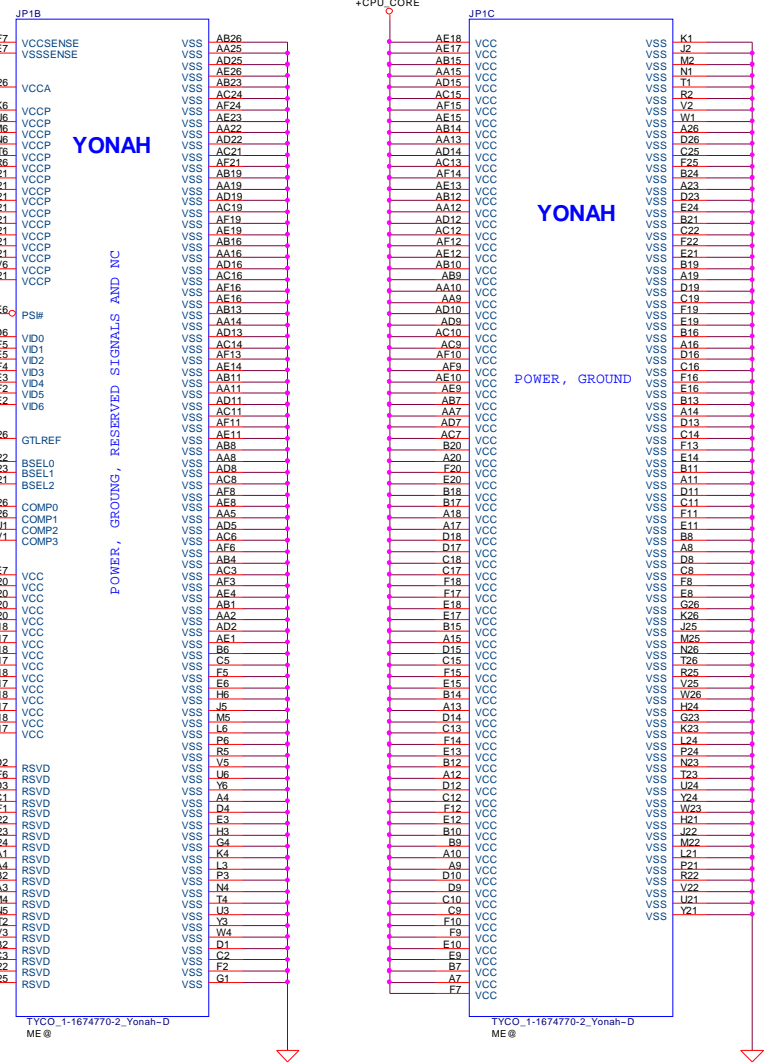
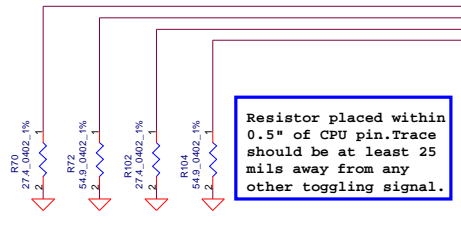
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Trace width / Spacing = 10 / 10 mil



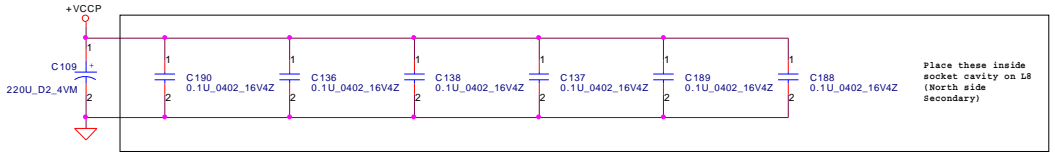
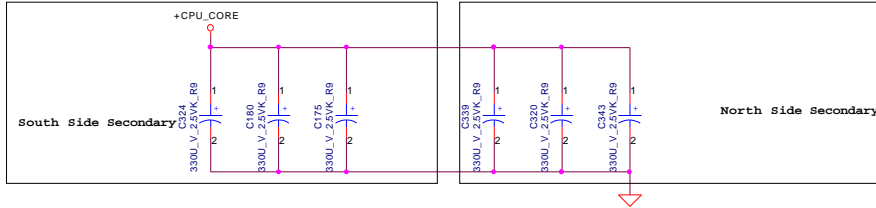
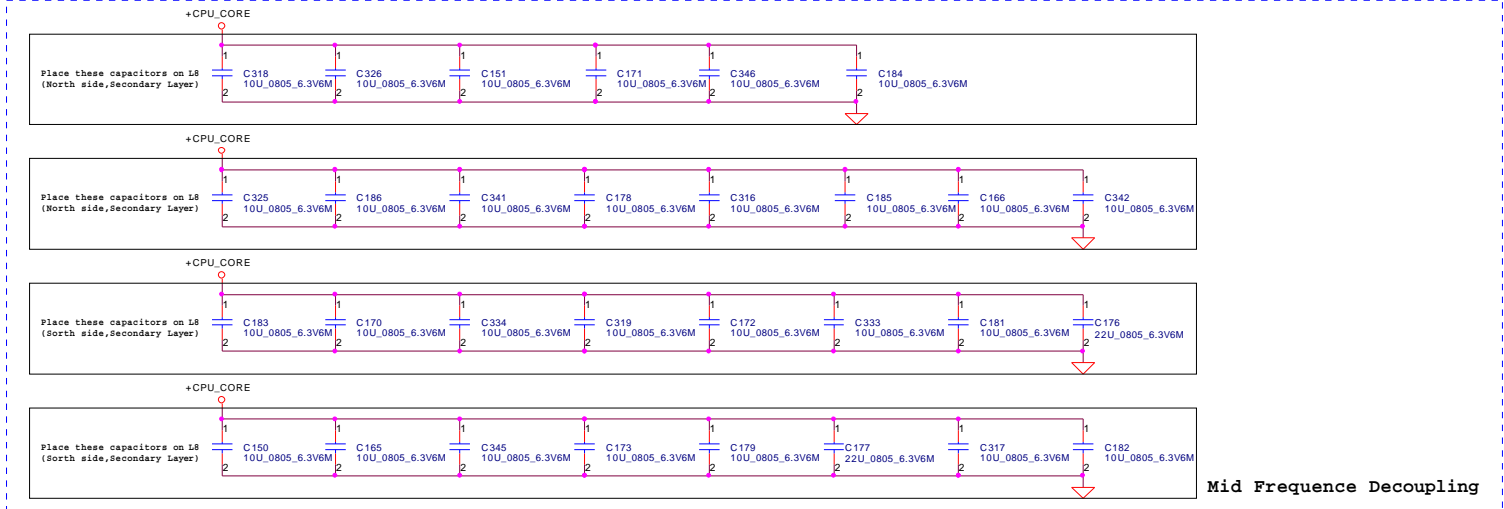
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Size	Document Number	Customer		Rev	
	IGL50/51 LA-3771			0.1	
Date:	星期四, 六月 08, 2006	Sheet	4	of 48	



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

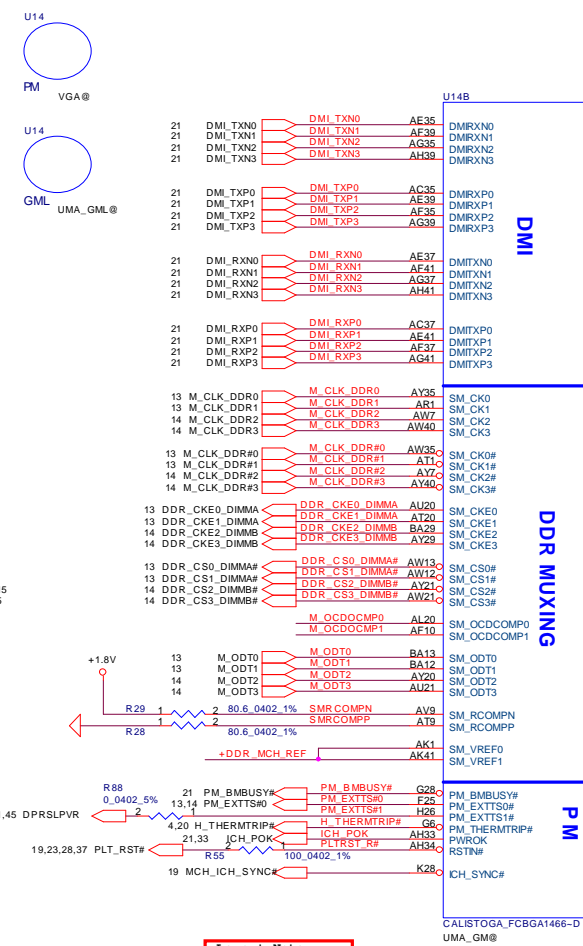
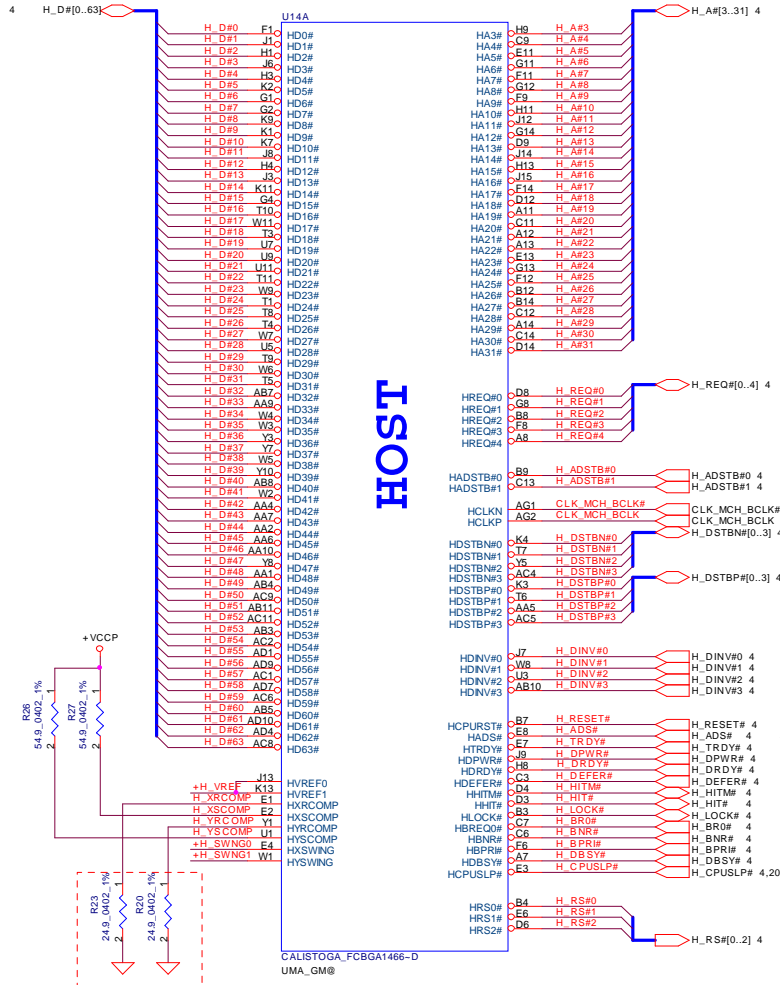


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Date	星期四, 六月 08, 2006	Sheet	5	of 48



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CPU Bypass capacitors		
Title	Document Number	
Size	IGL50/51 LA-3771	
Custom	R ev	
	0.1	
Date:	星期日, 六月 08, 2006	Sheet 6 of 48



Description at page15.

HOST

DMI

CFG

CLK

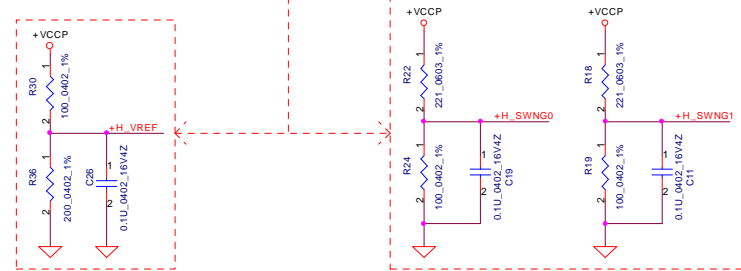
DDR MUXING

NC

RESERVED

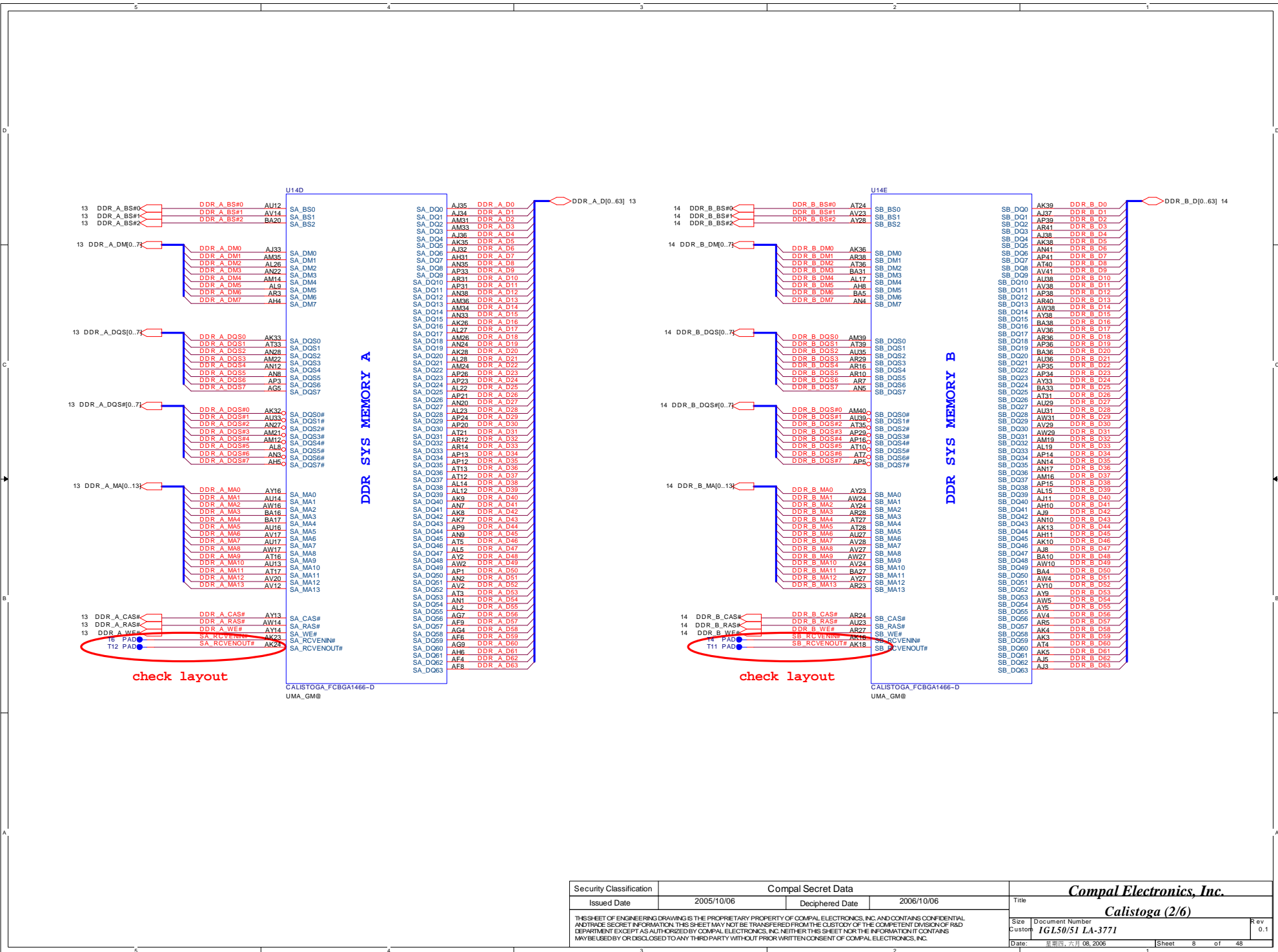
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trace width and
spacing is 20/20.

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H_SWNG1 trace width and spacing is 10/20.

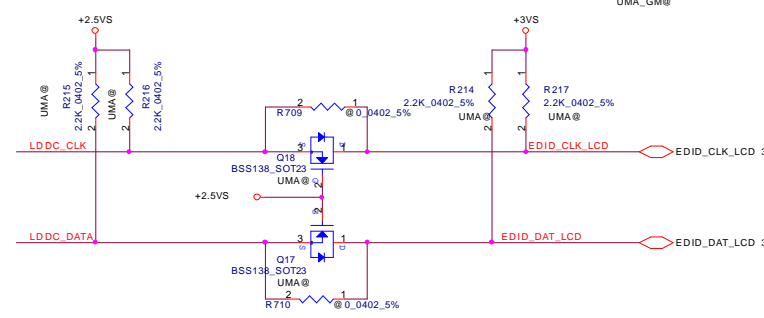
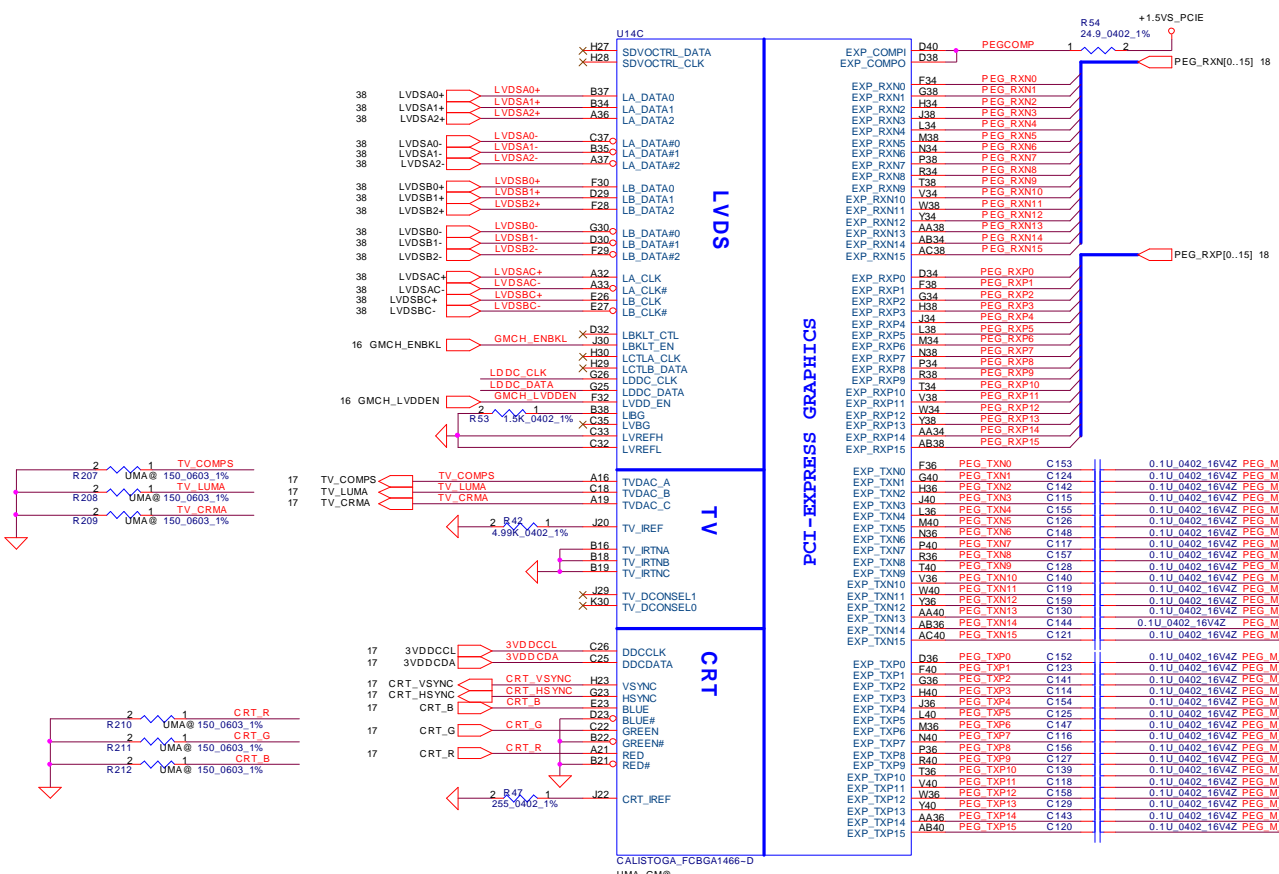


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Calistoga (1/6)	
Title	
Size	Document Number
Customer	IGL50151 LA-3771
Date	Rev
2006年06月08日	0.1
Sheet	7 of 48



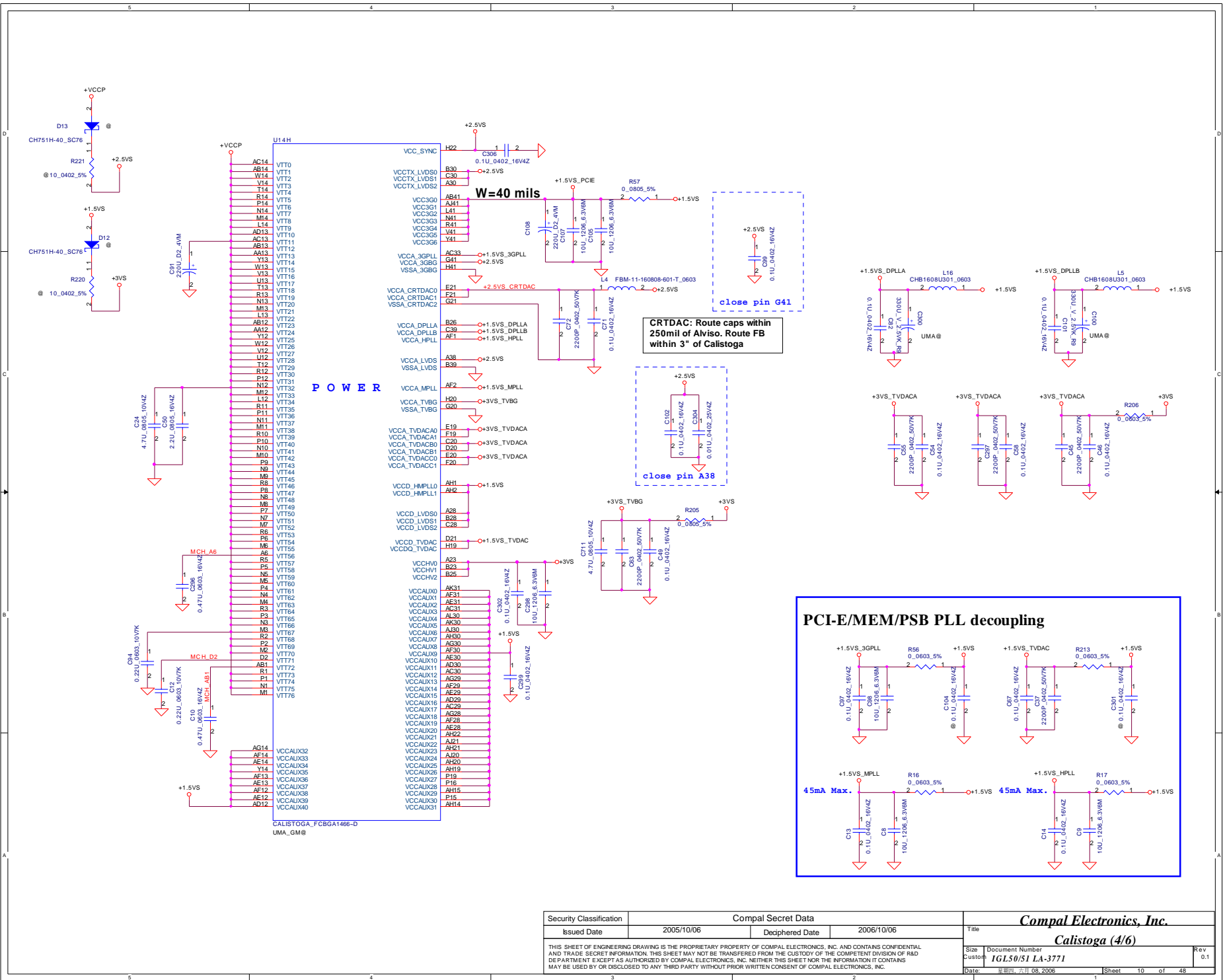
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Size	Document Number			Rev	
Custom	IGL50/51 LA-3771			0.1	
Date:	星期四, 六月 08, 2006	Sheet	8	of 48	



Chip Pin	Signal Name	Chip Pin	Signal Name	Component	Value	Notes
D40	PEGCOMP	D38	PEGCOMP			
F24	PEG_RXN0	G38	PEG_RXN1			
H34	PEG_RXN2	J38	PEG_RXN3			
L34	PEG_RXN4	M38	PEG_RXN5			
N34	PEG_RXN6	P38	PEG_RXN7			
R34	PEG_RXN8	T38	PEG_RXN9			
V38	PEG_RXN10	W38	PEG_RXN11			
Y34	PEG_RXN12	AA38	PEG_RXN13			
AB34	PEG_RXN14	AC38	PEG_RXN15			
D34	PEG_RXP0	F38	PEG_RXP1			
G34	PEG_RXP2	H38	PEG_RXP3			
J34	PEG_RXP4	L38	PEG_RXP5			
M34	PEG_RXP6	N38	PEG_RXP7			
P34	PEG_RXP8	R38	PEG_RXP9			
T34	PEG_RXP10	V38	PEG_RXP11			
W34	PEG_RXP12	Y38	PEG_RXP13			
AA34	PEG_RXP14	AC34	PEG_RXP15			
F36	PEG_TXN0	C153	PEG_TXN0		0.1U 0402 16V4Z	PEG_M_TXN0
H36	PEG_TXN2	C142	PEG_TXN2		0.1U 0402 16V4Z	PEG_M_TXN2
J40	PEG_TXN3	C115	PEG_TXN3		0.1U 0402 16V4Z	PEG_M_TXN3
L36	PEG_TXN4	C155	PEG_TXN4		0.1U 0402 16V4Z	PEG_M_TXN4
M40	PEG_TXN5	C126	PEG_TXN5		0.1U 0402 16V4Z	PEG_M_TXN5
N36	PEG_TXN6	C148	PEG_TXN6		0.1U 0402 16V4Z	PEG_M_TXN6
P40	PEG_TXN7	C117	PEG_TXN7		0.1U 0402 16V4Z	PEG_M_TXN7
R36	PEG_TXN8	C157	PEG_TXN8		0.1U 0402 16V4Z	PEG_M_TXN8
T40	PEG_TXN9	C128	PEG_TXN9		0.1U 0402 16V4Z	PEG_M_TXN9
V36	PEG_TXN10	C140	PEG_TXN10		0.1U 0402 16V4Z	PEG_M_TXN10
W40	PEG_TXN11	C119	PEG_TXN11		0.1U 0402 16V4Z	PEG_M_TXN11
Y36	PEG_TXN12	C159	PEG_TXN12		0.1U 0402 16V4Z	PEG_M_TXN12
AA40	PEG_TXN13	C130	PEG_TXN13		0.1U 0402 16V4Z	PEG_M_TXN13
AB36	PEG_TXN14	C144	PEG_TXN14		0.1U 0402 16V4Z	PEG_M_TXN14
AC40	PEG_TXN15	C121	PEG_TXN15		0.1U 0402 16V4Z	PEG_M_TXN15
D36	PEG_TXP0	C152	PEG_TXP0		0.1U 0402 16V4Z	PEG_M_TXP0
F40	PEG_TXP1	C123	PEG_TXP1		0.1U 0402 16V4Z	PEG_M_TXP1
G36	PEG_TXP2	C141	PEG_TXP2		0.1U 0402 16V4Z	PEG_M_TXP2
H40	PEG_TXP3	C114	PEG_TXP3		0.1U 0402 16V4Z	PEG_M_TXP3
J36	PEG_TXP4	C154	PEG_TXP4		0.1U 0402 16V4Z	PEG_M_TXP4
L40	PEG_TXP5	C125	PEG_TXP5		0.1U 0402 16V4Z	PEG_M_TXP5
M36	PEG_TXP6	C147	PEG_TXP6		0.1U 0402 16V4Z	PEG_M_TXP6
N40	PEG_TXP7	C116	PEG_TXP7		0.1U 0402 16V4Z	PEG_M_TXP7
P36	PEG_TXP8	C156	PEG_TXP8		0.1U 0402 16V4Z	PEG_M_TXP8
R40	PEG_TXP9	C127	PEG_TXP9		0.1U 0402 16V4Z	PEG_M_TXP9
T36	PEG_TXP10	C139	PEG_TXP10		0.1U 0402 16V4Z	PEG_M_TXP10
V40	PEG_TXP11	C118	PEG_TXP11		0.1U 0402 16V4Z	PEG_M_TXP11
W36	PEG_TXP12	C158	PEG_TXP12		0.1U 0402 16V4Z	PEG_M_TXP12
Y40	PEG_TXP13	C129	PEG_TXP13		0.1U 0402 16V4Z	PEG_M_TXP13
AA36	PEG_TXP14	C143	PEG_TXP14		0.1U 0402 16V4Z	PEG_M_TXP14
AB40	PEG_TXP15	C120	PEG_TXP15		0.1U 0402 16V4Z	PEG_M_TXP15

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Size	Document Number	Rev
Custom	IGL50/51 LA-3771	0.1
Date:	星期日, 六月 08, 2006	Sheet 9 of 48



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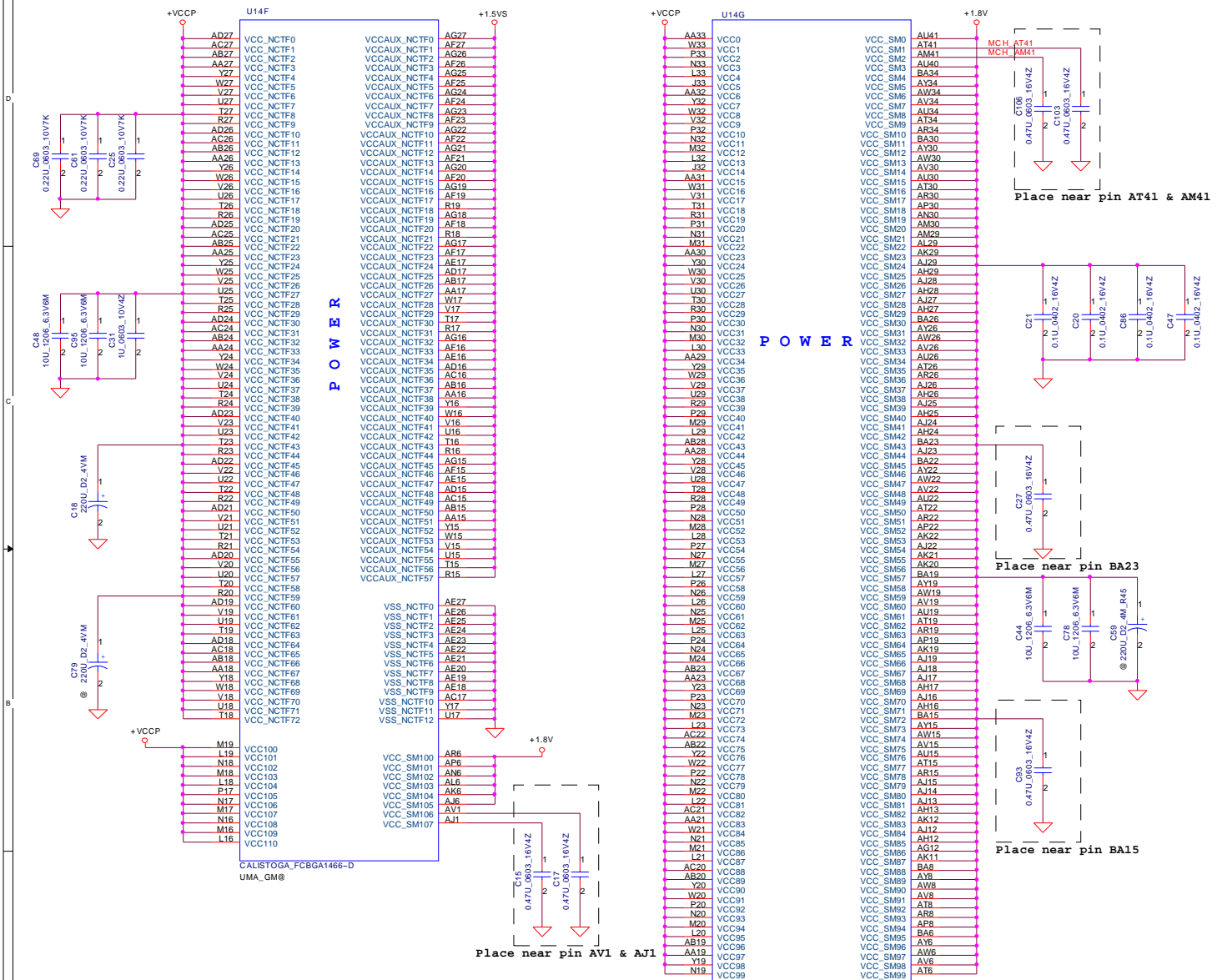
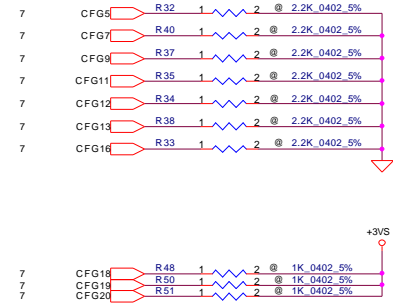
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Calistoga (4/6)		
Size	Document Number	Rev
	IGL50/51 LA-3771	0.1
Date:	日期: 六月 08, 2006	Sheet 10 of 48

Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V *(Default) 01 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



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				IGL50/51 LA-3771
				Rev 0.1
Date: 星期四, 六月 08, 2006				Sheet 11 of 48

U14I		AE34	
AC41	VSS0	VSS100	AC34
AA41	VSS1	VSS101	C34
W41	VSS2	VSS102	AW33
T41	VSS3	VSS103	AW33
P41	VSS4	VSS104	AV33
M41	VSS5	VSS105	AR33
J41	VSS6	VSS106	AE33
F41	VSS7	VSS107	AB33
AV40	VSS8	VSS108	V33
AP40	VSS9	VSS109	T33
AN40	VSS10	VSS110	R33
AK40	VSS11	VSS111	M33
AJ40	VSS12	VSS112	H33
AH40	VSS13	VSS113	G33
AG40	VSS14	VSS114	F33
AF40	VSS15	VSS115	D33
AE40	VSS16	VSS116	B33
B40	VSS17	VSS117	AH32
AV39	VSS18	VSS118	AG32
AW39	VSS19	VSS119	AF32
AV39	VSS20	VSS120	AE32
AR39	VSS21	VSS121	AC32
AN39	VSS22	VSS122	AB32
AJ39	VSS23	VSS123	G32
AC39	VSS24	VSS124	G32
AB39	VSS25	VSS125	B32
AA39	VSS26	VSS126	AY31
Y39	VSS27	VSS127	AV31
W39	VSS28	VSS128	AN31
V39	VSS29	VSS129	AM31
T39	VSS30	VSS130	AL31
R39	VSS31	VSS131	AK31
P39	VSS32	VSS132	Y31
N39	VSS33	VSS133	AB30
M39	VSS34	VSS134	E30
L39	VSS35	VSS135	AT29
J39	VSS36	VSS136	AM29
H39	VSS37	VSS137	AB29
G39	VSS38	VSS138	T29
F39	VSS39	VSS139	N29
D39	VSS40	VSS140	G29
AT38	VSS41	VSS141	E29
AM38	VSS42	VSS142	C29
AH38	VSS43	VSS143	B29
AG38	VSS44	VSS144	A29
AF38	VSS45	VSS145	BA28
AE38	VSS46	VSS146	AW28
C38	VSS47	VSS147	AU28
AK37	VSS48	VSS148	AP28
AH37	VSS49	VSS149	AM28
AB37	VSS50	VSS150	AD28
AA37	VSS51	VSS151	U14
Y37	VSS52	VSS152	AC28
W37	VSS53	VSS153	W28
V37	VSS54	VSS154	E14
T37	VSS55	VSS155	E28
R37	VSS56	VSS156	AP27
P37	VSS57	VSS157	AM27
N37	VSS58	VSS158	AK27
M37	VSS59	VSS159	J27
L37	VSS60	VSS160	G27
J37	VSS61	VSS161	F27
H37	VSS62	VSS162	C27
G37	VSS63	VSS163	B27
F37	VSS64	VSS164	AN26
D37	VSS65	VSS165	M26
AV36	VSS66	VSS166	K26
AW36	VSS67	VSS167	F26
AN36	VSS68	VSS168	D26
AH36	VSS69	VSS169	AK25
AG36	VSS70	VSS170	P25
AF36	VSS71	VSS171	H25
AE36	VSS72	VSS172	K25
AC36	VSS73	VSS173	E25
C36	VSS74	VSS174	D25
B36	VSS75	VSS175	A25
BA35	VSS76	VSS176	BA24
AV35	VSS77	VSS177	AU24
AR35	VSS78	VSS178	AL24
AH35	VSS79	VSS179	AW23
AG35	VSS80	VSS180	AT23
AF35	VSS81	VSS181	AN23
AE35	VSS82	VSS182	AM23
AC35	VSS83	VSS183	AH23
C35	VSS84	VSS184	AC23
B35	VSS85	VSS185	W23
AW35	VSS86	VSS186	K23
AN35	VSS87	VSS187	J23
AH35	VSS88	VSS188	F23
AG35	VSS89	VSS189	C23
AF35	VSS90	VSS190	AA22
AE35	VSS91	VSS191	K22
AC35	VSS92	VSS192	G22
C35	VSS93	VSS193	E22
B35	VSS94	VSS194	D22
BA34	VSS95	VSS195	A22
AV34	VSS96	VSS196	BA21
AR34	VSS97	VSS197	AV21
AH34	VSS98	VSS198	AR21
AG34	VSS99	VSS199	AR21

POWER

U14J		AG10	
AN21	VSS200	VSS280	AC10
AL21	VSS201	VSS281	W10
AB21	VSS202	VSS282	U10
Y21	VSS203	VSS283	BA9
P21	VSS204	VSS284	BA9
K21	VSS205	VSS285	AW9
J21	VSS206	VSS286	AR9
H21	VSS207	VSS287	AH9
G21	VSS208	VSS288	AG9
AW20	VSS209	VSS289	Y9
AR20	VSS210	VSS290	R9
AM20	VSS211	VSS291	G9
AZ20	VSS212	VSS292	E9
K20	VSS213	VSS293	A9
B20	VSS214	VSS294	AG8
AZ20	VSS215	VSS295	AD8
AN19	VSS216	VSS296	AA8
AC19	VSS217	VSS297	UB
W19	VSS218	VSS298	K8
K19	VSS219	VSS299	CB
G19	VSS220	VSS300	BA7
C19	VSS221	VSS301	AV7
AH18	VSS222	VSS302	AP7
P18	VSS223	VSS303	AL7
H18	VSS224	VSS304	AJ7
D18	VSS225	VSS305	AH7
A18	VSS226	VSS306	AZ7
AY17	VSS227	VSS307	AC7
AR17	VSS228	VSS308	R7
AJ17	VSS229	VSS309	C7
AM17	VSS230	VSS310	D7
AK17	VSS231	VSS311	AG6
AV16	VSS232	VSS312	AD6
AM16	VSS233	VSS313	AB6
AL16	VSS234	VSS314	Y6
J16	VSS235	VSS315	U6
AM16	VSS236	VSS316	UB
C16	VSS237	VSS317	K6
AN15	VSS238	VSS318	H6
AM15	VSS239	VSS319	B6
K29	VSS240	VSS320	AV5
N15	VSS241	VSS321	AF5
M15	VSS242	VSS322	AD5
L15	VSS243	VSS323	AJ4
B15	VSS244	VSS324	AR4
A15	VSS245	VSS325	AP4
BA14	VSS246	VSS326	AL4
AT14	VSS247	VSS327	Y4
AK14	VSS248	VSS328	U4
AD14	VSS249	VSS329	R4
AA14	VSS250	VSS330	J4
U14	VSS251	VSS331	F4
K14	VSS252	VSS332	C4
H14	VSS253	VSS333	AJ3
E14	VSS254	VSS334	AW3
AV13	VSS255	VSS335	AV3
AR13	VSS256	VSS336	AL3
AM13	VSS257	VSS337	AH3
AL13	VSS258	VSS338	AG3
AG13	VSS259	VSS339	AF3
F13	VSS260	VSS340	AD3
D13	VSS261	VSS341	AC3
B13	VSS262	VSS342	AA3
AY12	VSS263	VSS343	C3
AC12	VSS264	VSS344	AT2
K12	VSS265	VSS345	AR2
H12	VSS266	VSS346	AP2
E12	VSS267	VSS347	AY2
A12	VSS268	VSS348	AJ2
AD11	VSS269	VSS349	AD2
K25	VSS270	VSS350	AB2
Y11	VSS271	VSS351	Y2
J11	VSS272	VSS352	U2
D11	VSS273	VSS353	T2
B11	VSS274	VSS354	J2
AV10	VSS275	VSS355	H2
AP10	VSS276	VSS356	F2
AL10	VSS277	VSS357	C2
AJ10	VSS278	VSS358	CB
AV29	VSS279	VSS359	AL1
		VSS360	

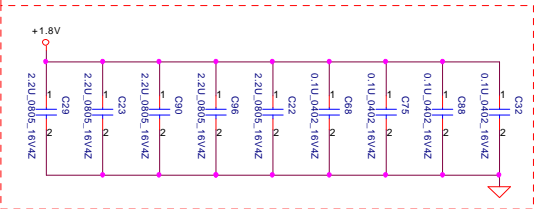
POWER

CALISTOGA_FCBGA1466-D
UMA_GM@

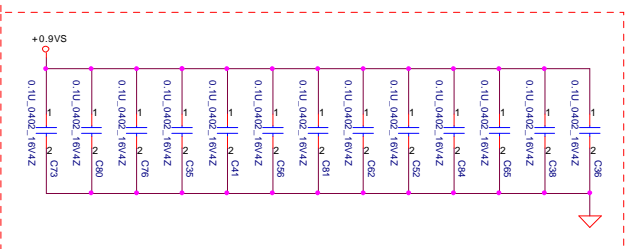
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				Customer	IGL50/51 LA-3771
				Date:	星期四, 六月 08, 2006
				Sheet	12 of 48
				Rev	0.1

- 8 DDR_B_DQS#[0..7]
- 8 DDR_B_D[0..63]
- 8 DDR_B_DM[0..7]
- 8 DDR_B_DQS[0..7]
- 8 DDR_B_MA[0..13]

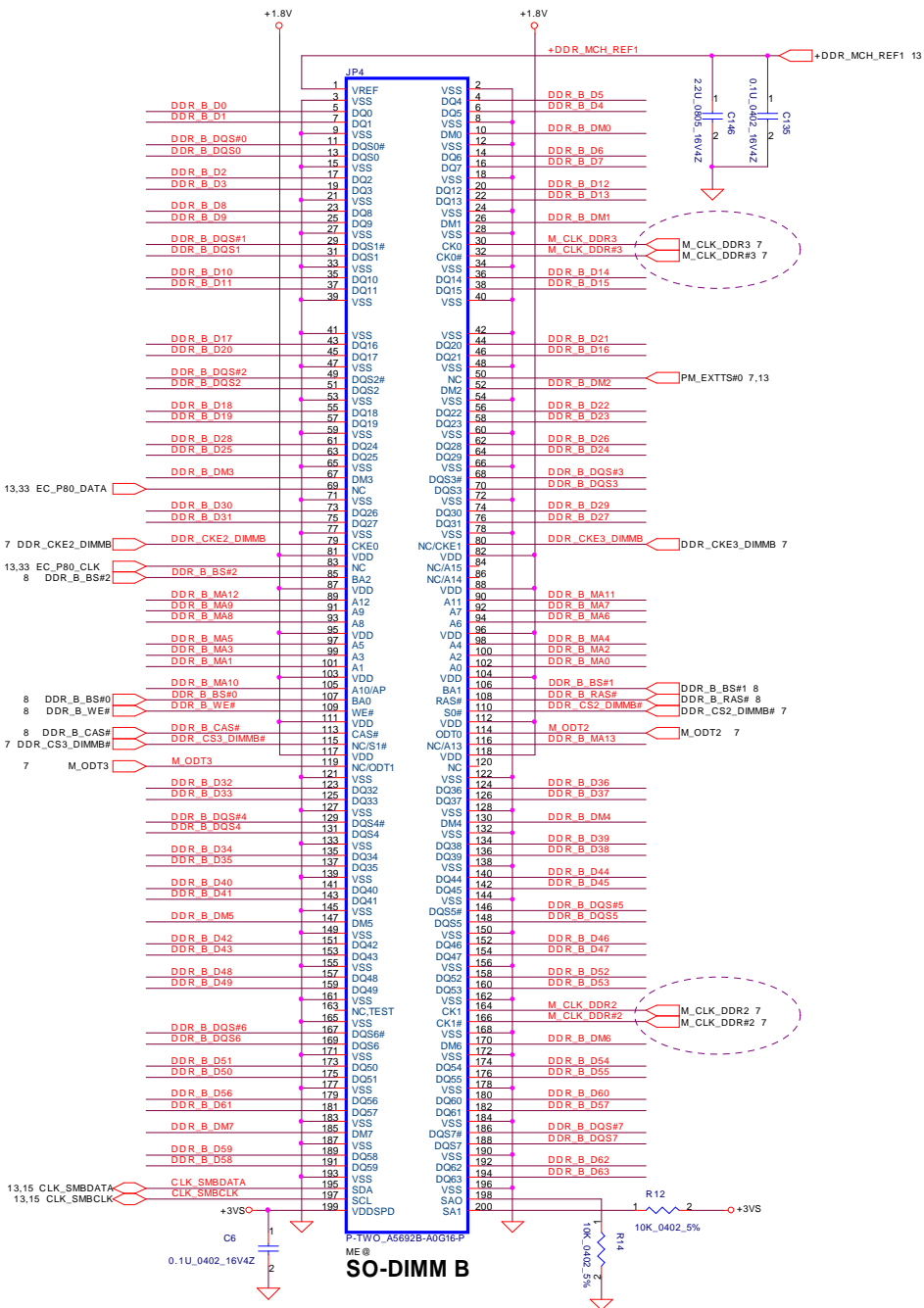
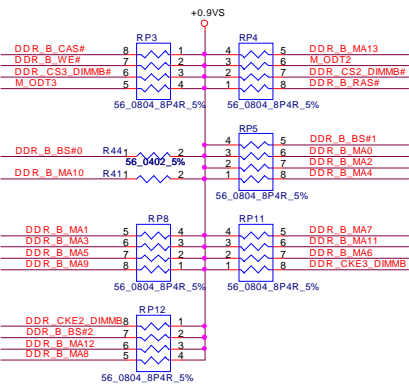
Layout Note:
Place near JP42



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP42, all trace length Max=1.5"



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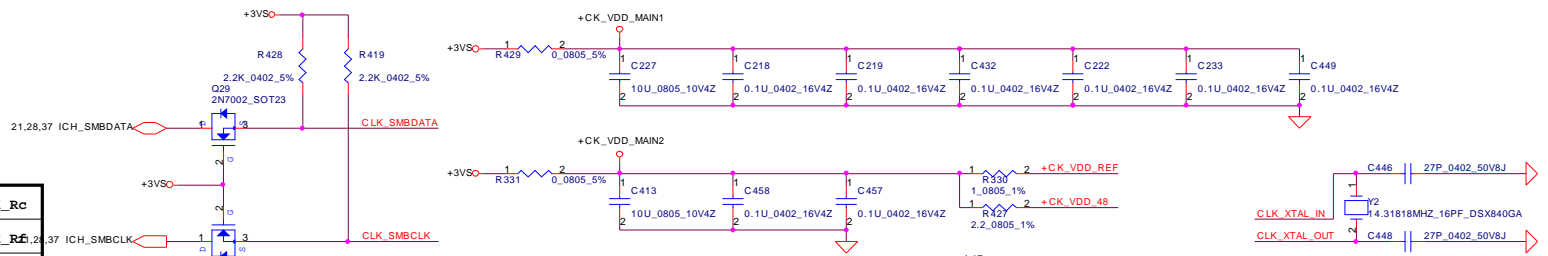
Compal Electronics, Inc.	
DDR II - SODIMM SLOT 2	
Size	Document Number
	IGL50/51 LA-3771
Date:	Rev. 0.1
星期四, 六月 08, 2006	Sheet 14 of 48

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS954306

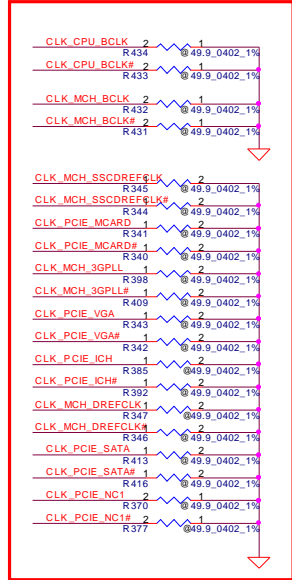
FSB Frequency Set:

CPU Driven	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
	* (Default)	No Stuff	CLK_Rd	CLK_Re
533MHz	Stuff	CLK_Rd	CLK_Re	CLK_Rf
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc
667MHz	Stuff	CLK_Rd	CLK_Re	CLK_Rf
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc



Place crystal within 500 mils of CK410

Place near U4
Place these components near each pin within 40 mils.



PCI_MINI = FCTSEL1

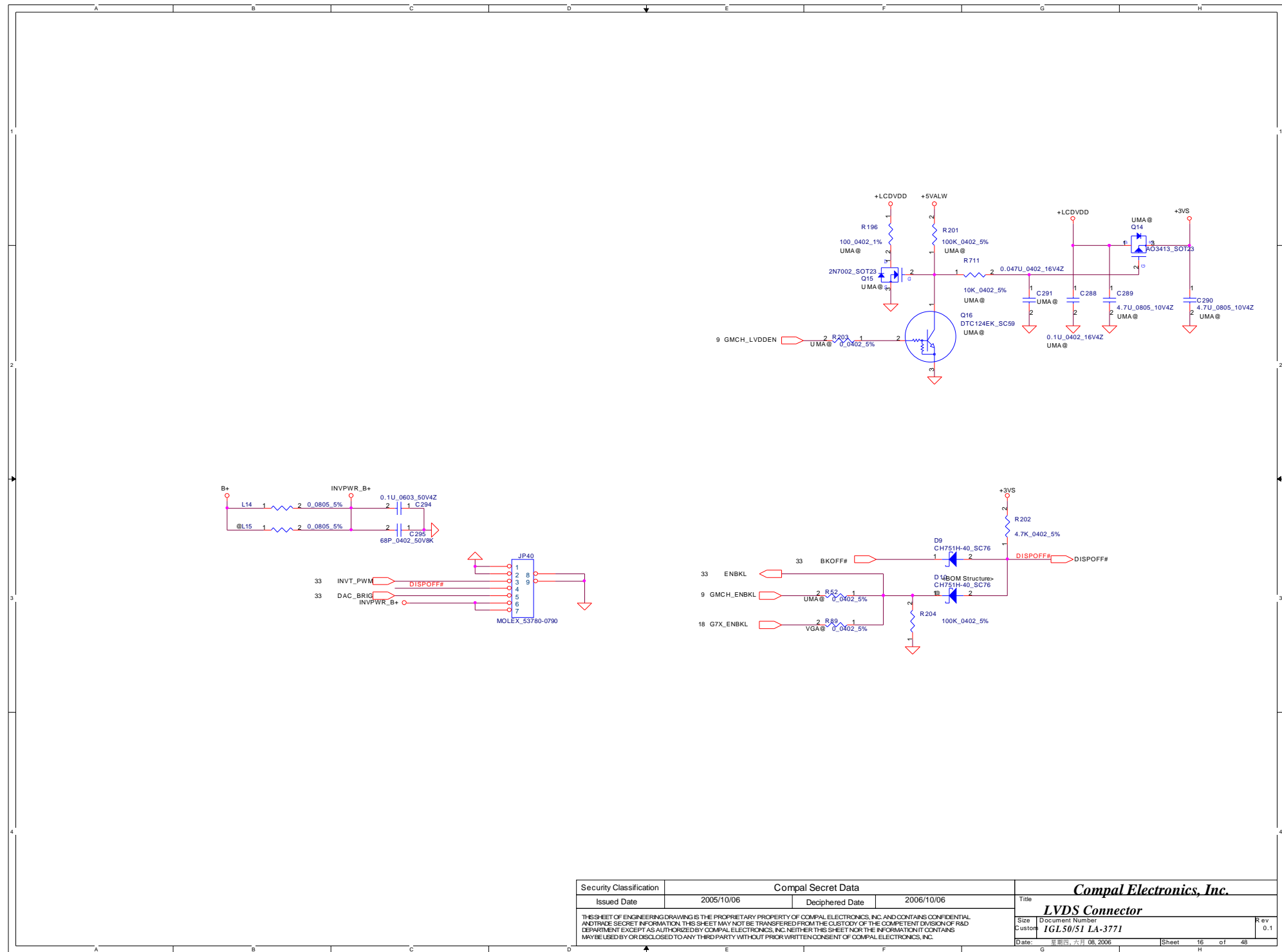
FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0	DOT96T	DOT96C	96/100M_T	96/100M_C
1	27Mout	27MSout	SRCT0	SRCC0

PCI_PME=SEL_PCI6

PCI_LAN	PIN27
0	CLKREQ5
1	PCICLK6

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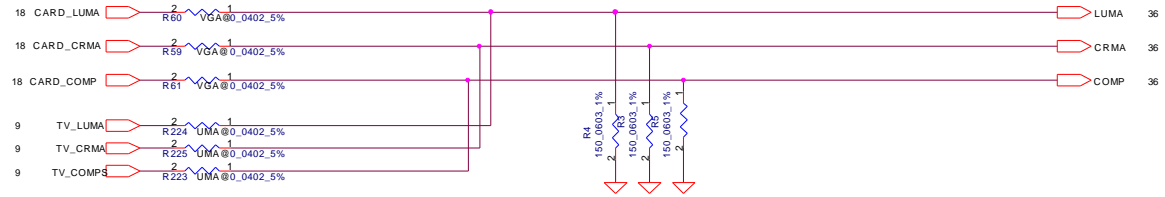
Compal Electronics, Inc.			
Clock generator			
Size	Document Number	IGL50/51 LA-3771	
Date	星期 四, 六月 08, 2006	Sheet	15 of 48



Security Classification	Compal Secret Data	
Issued Date	2005/10/06	Deciphered Date
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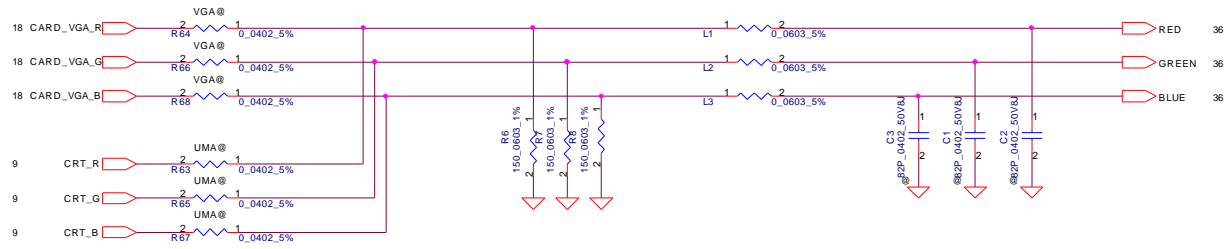
Compal Electronics, Inc.		
LVDS Connector		
Size	Document Number	R ev
Custom	IGL50/51 LA-3771	0.1
Date:	星期日, 六月 08, 2006	Sheet 16 of 48

TV-OUT Conn.

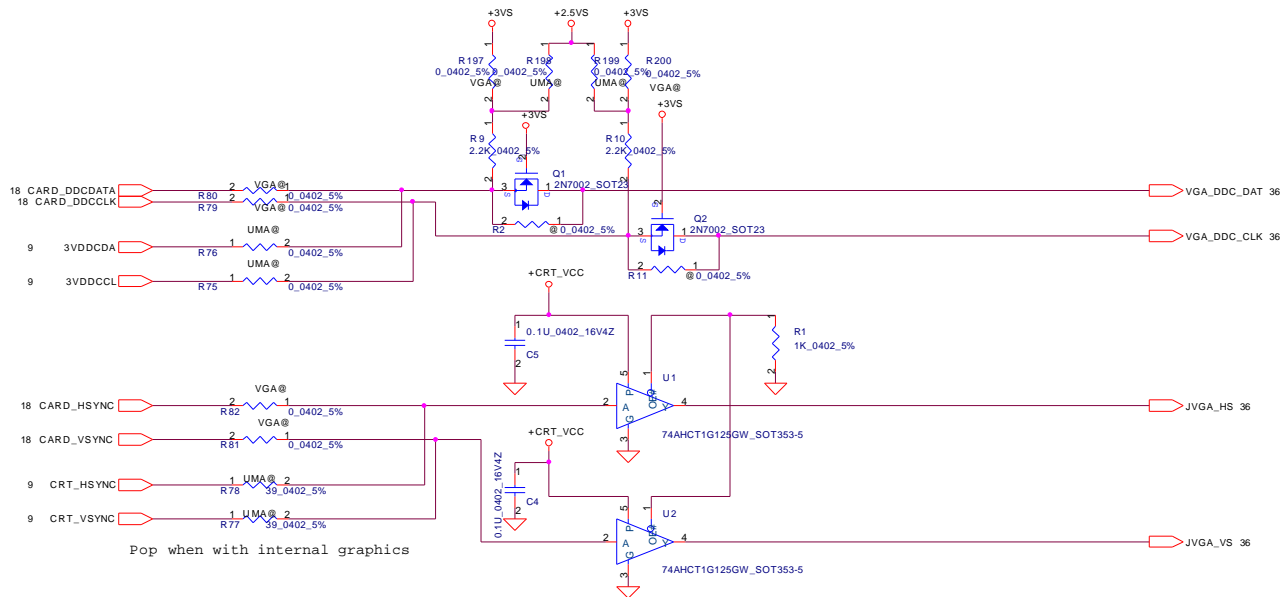


Pop when with internal graphics

CRT Conn.



Pop when with internal graphics



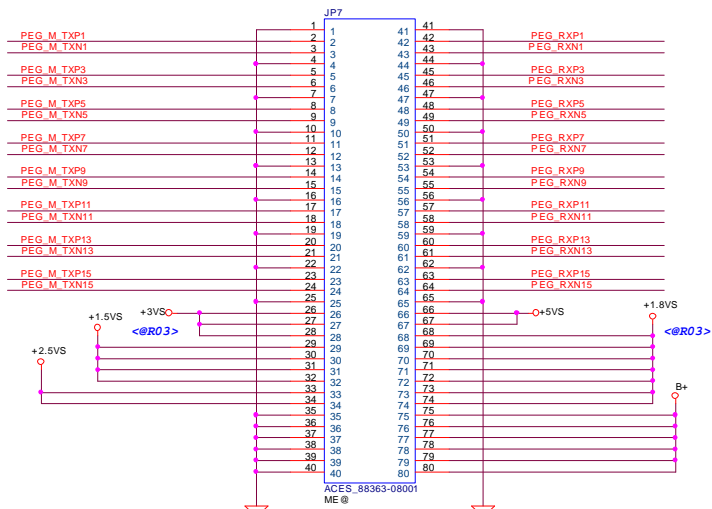
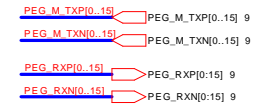
Pop when with internal graphics

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				Customer	IGL50/51 LA-3771
Date:	星期四, 六月 08, 2006	Sheet	17	of	48

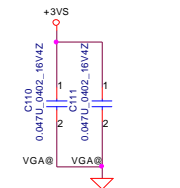
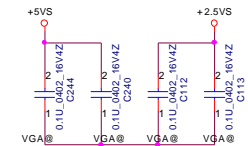
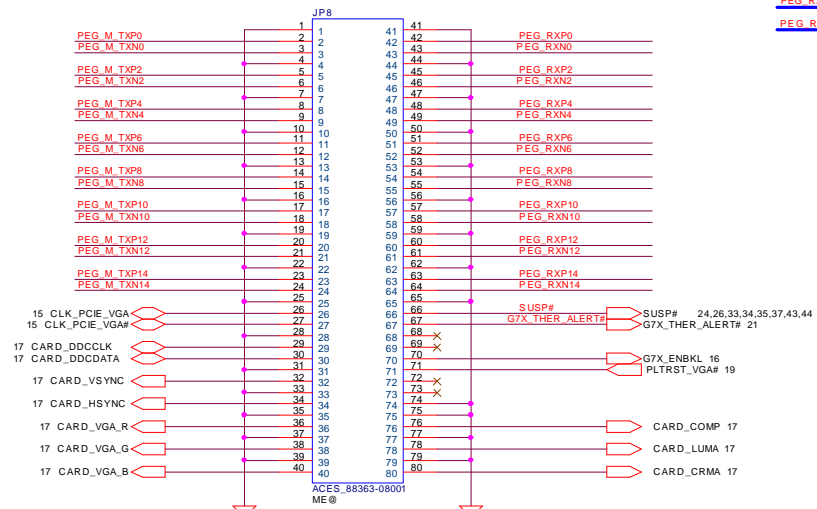
MAX. 4.06A @ 1.8V

MAX. 130mA @ 2.5V

MAX. 655mA @ 3.3V



< New Add Pin.28 for +3V, Pin.68 for +1.8V @R03 >

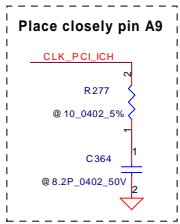
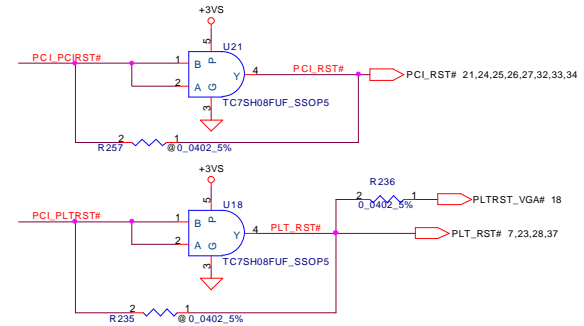
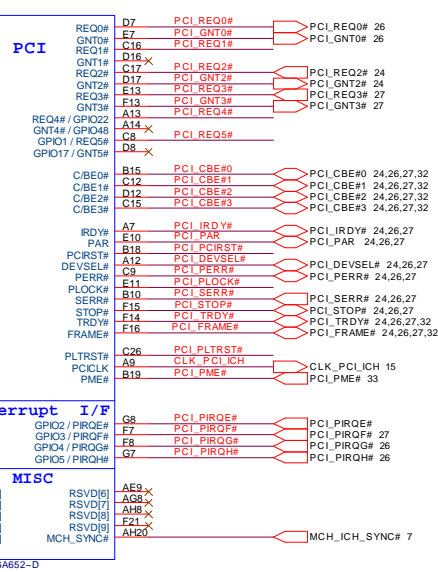
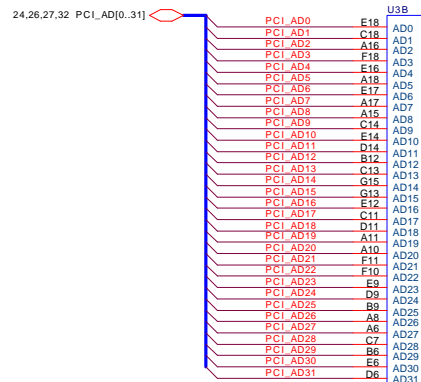
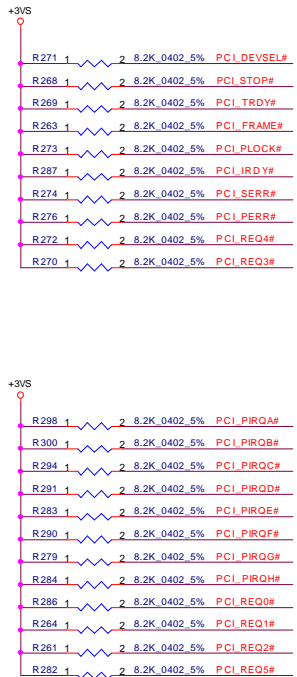


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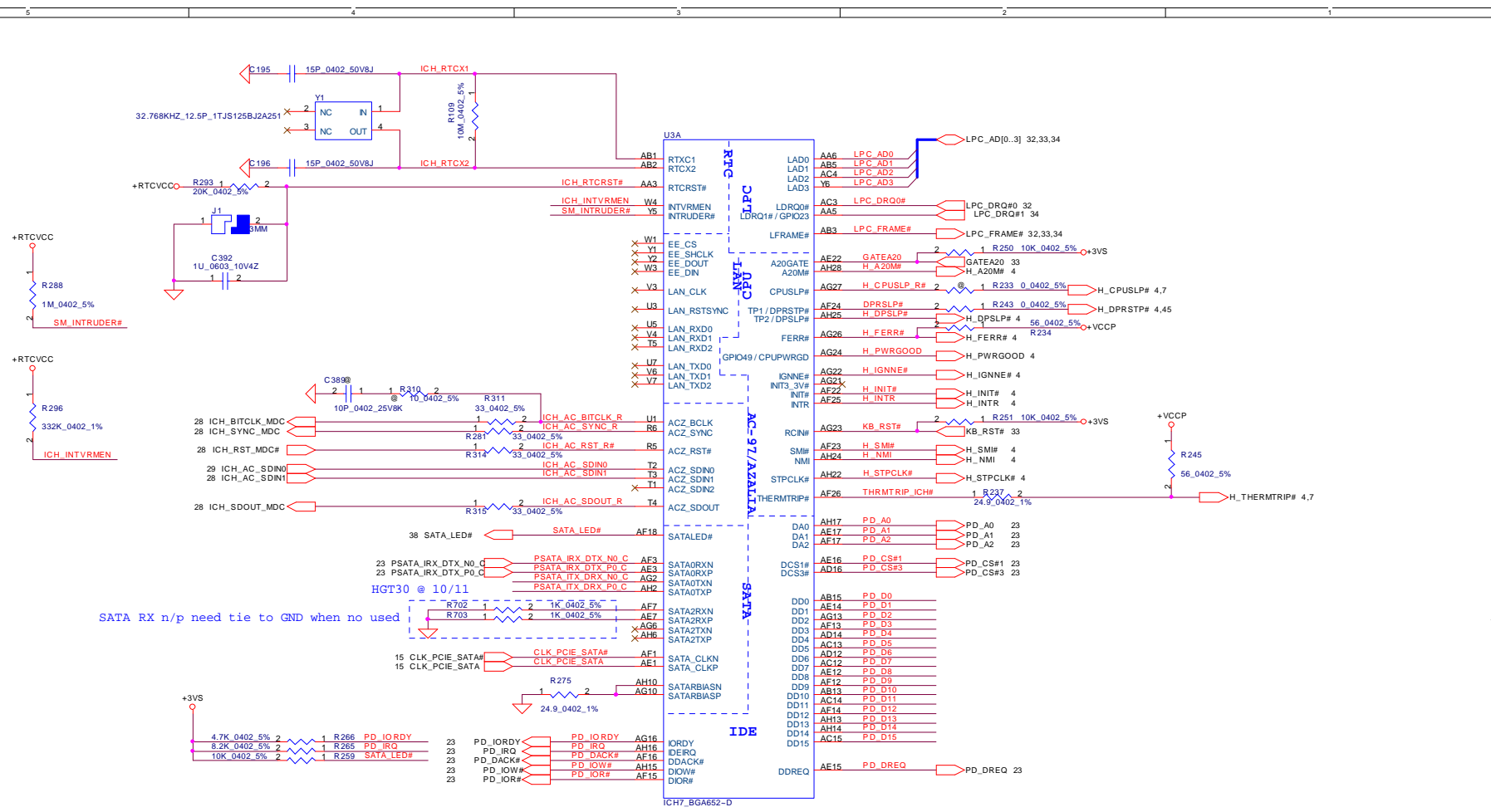
VGA/B connector

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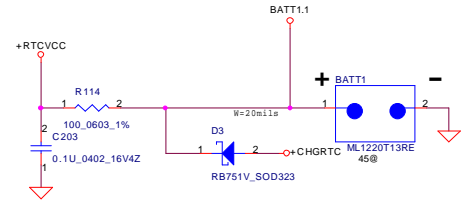
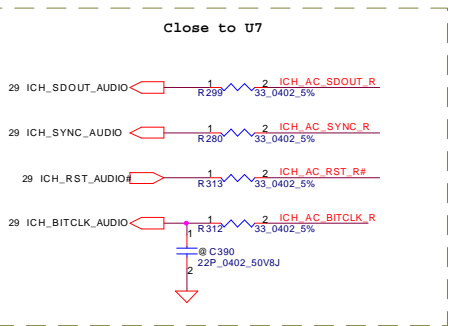
Title	VGA/B connector		Rev	0.1
Size	Document Number			
Custom	IGL50/51 LA-3771			
Date:	星期四, 六月 08, 2006	Sheet	18 of 48	



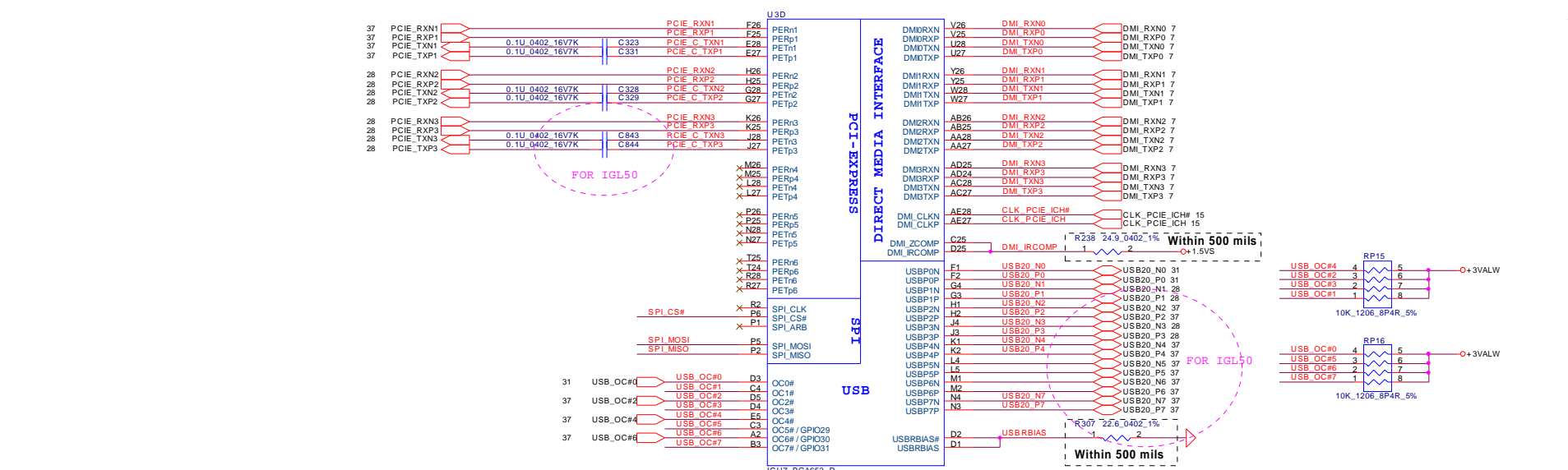
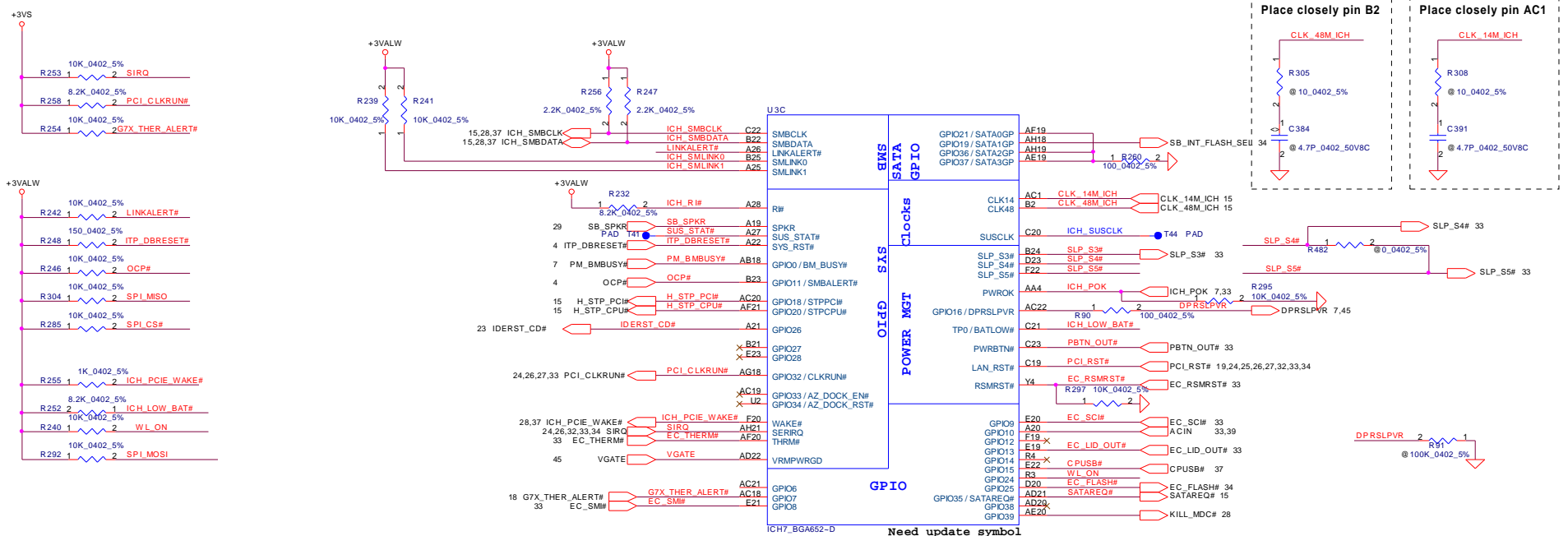
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Size	Document Number			R rev	
	IGL50/51 LA-3771			0.1	
Date:	星期日, 六月 08, 2006	Sheet	19	of	48



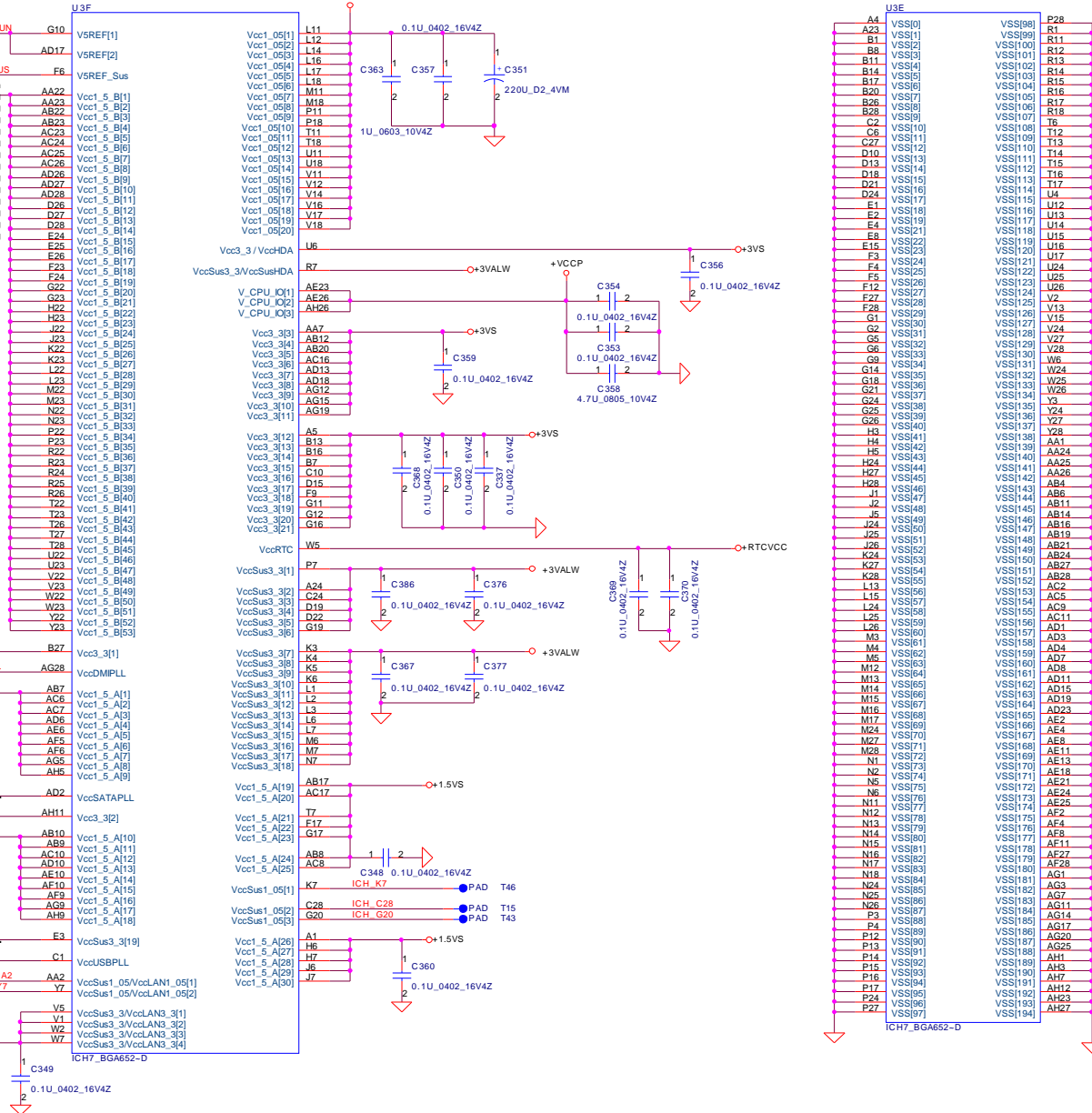
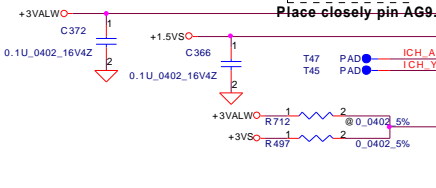
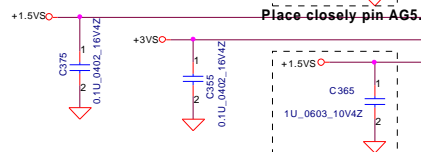
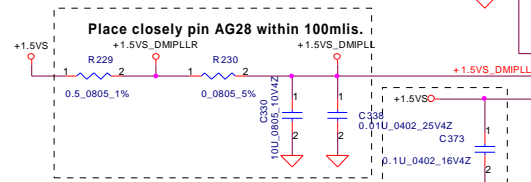
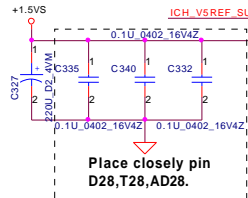
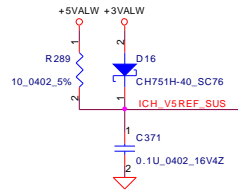
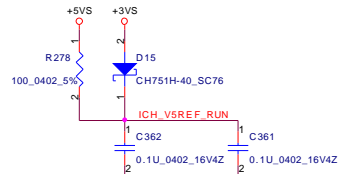
SATA RX n/p need tie to GND when no used



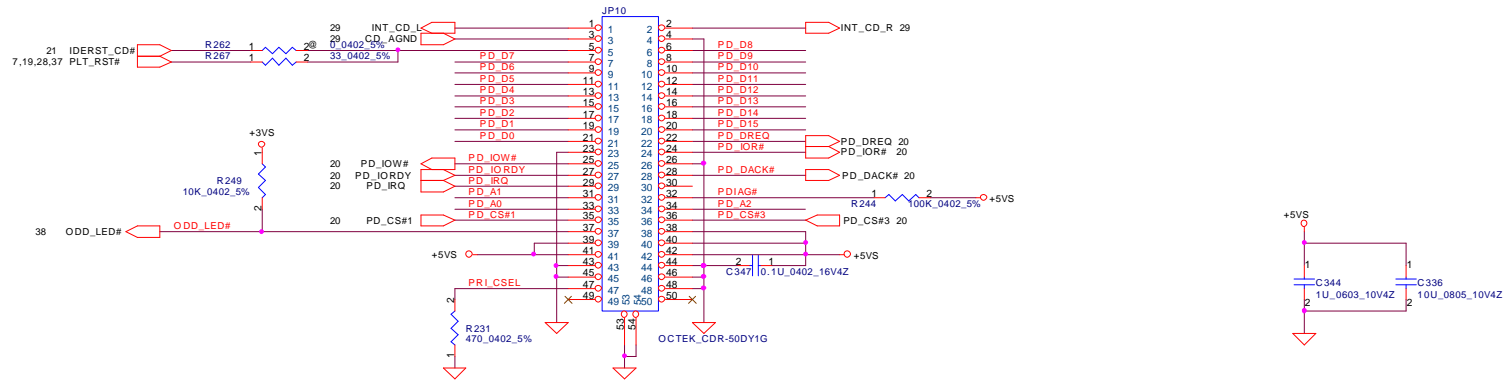
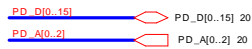
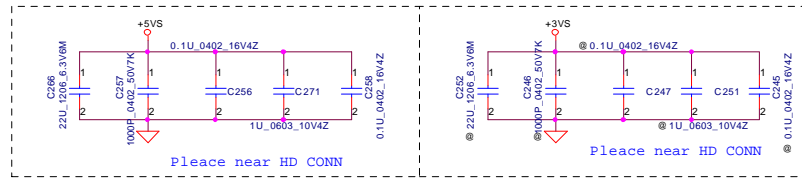
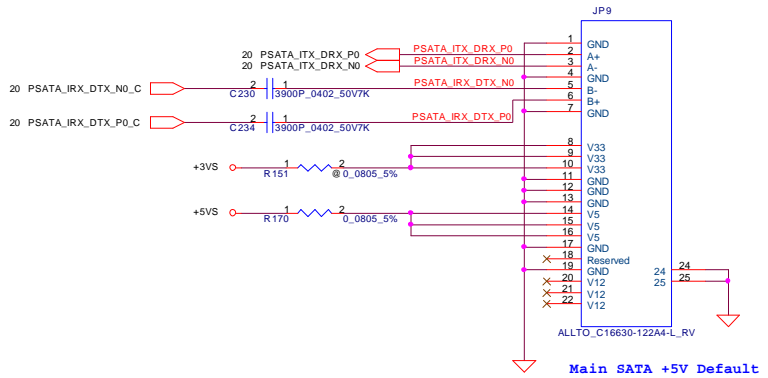
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				Date	Rev
				星期日, 六月 08, 2006	0.1
				Sheet	20 of 48



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		Customer		IGL50/LA 3771	
		Date		Rev	
		星期日, 六月 08, 2006		0.1	
		Sheet		21 of 48	

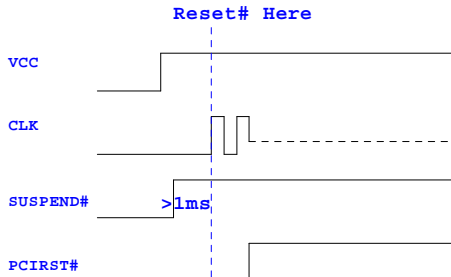


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Size	Document Number			R rev	
Custom	IGL50/51 LA-3771			0.1	
Date:	星期四, 六月 08, 2006	Sheet	22	of	48

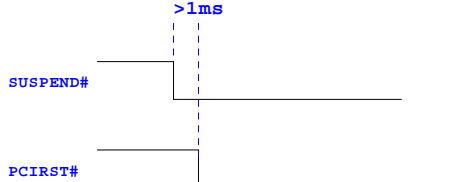


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Issued Date	2005/10/06	Deciphered Date	2006/10/06	Title HDD & CDROM
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Date:	星期日, 六月 08, 2006	Sheet	23	of 48
				Rev 0.1

Power on RESET#

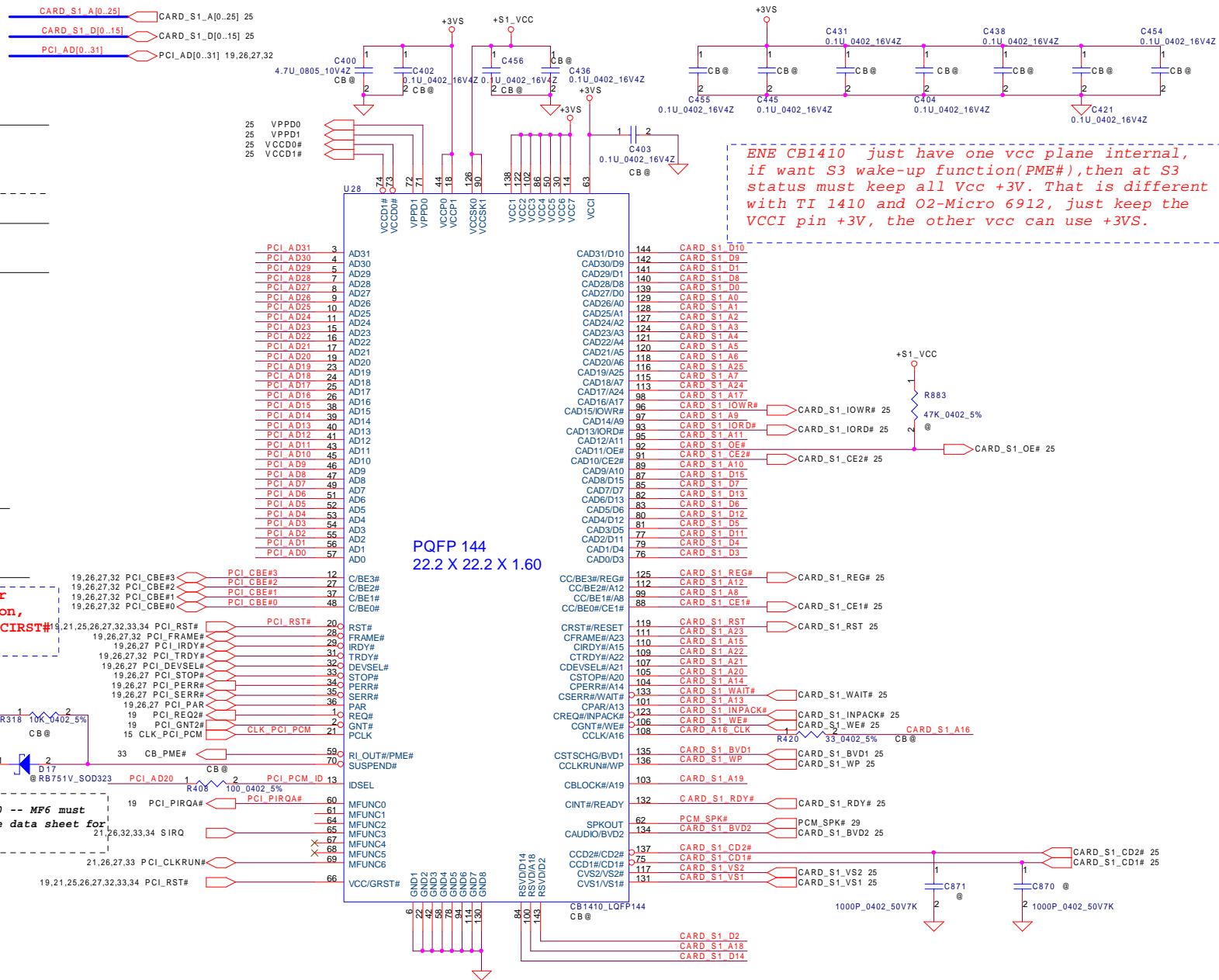


Entry S3



SUSPEND# will gate the PCIRST# or GRST#, so need S3 wake-up function, SUSPEND# must be LOW ahead the PCIRST# about 1ms.

Note: MF0 -- MF6 must refer the data sheet for design.



ENE CBI410 just have one vcc plane internal, if want S3 wake-up function(PME#), then at S3 status must keep all Vcc +3V. That is different with TI 1410 and O2-Micro 6912, just keep the VCCI pin +3V, the other vcc can use +3VS.

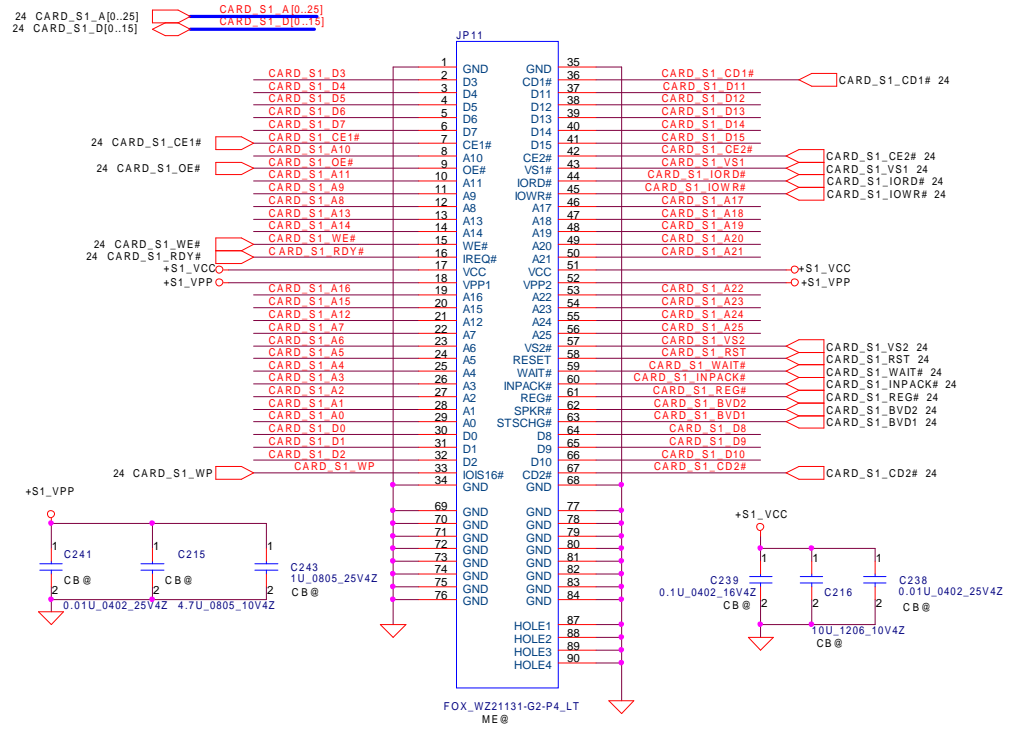
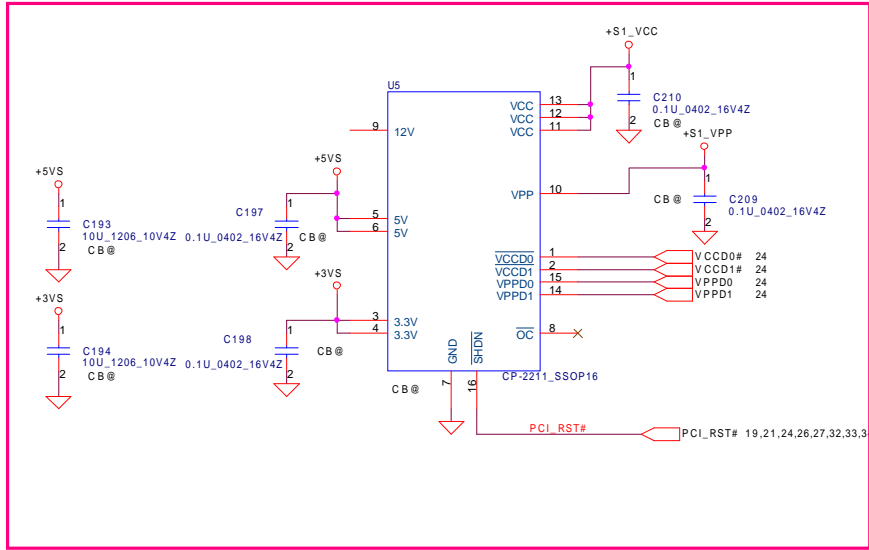
PQFP 144
22.2 X 22.2 X 1.60

Security Classification	Compal Secret Data	
Issued Date	2005/10/06	Deciphered Date
		2006/10/06

Compal Electronics, Inc.		
Title CB ENE1410(One Solt)		
Size	Document Number	Rev
Custom	IGL50/51 LA-3771	0.1
Date:	日期: 2006.10.06	Sheet 24 of 48

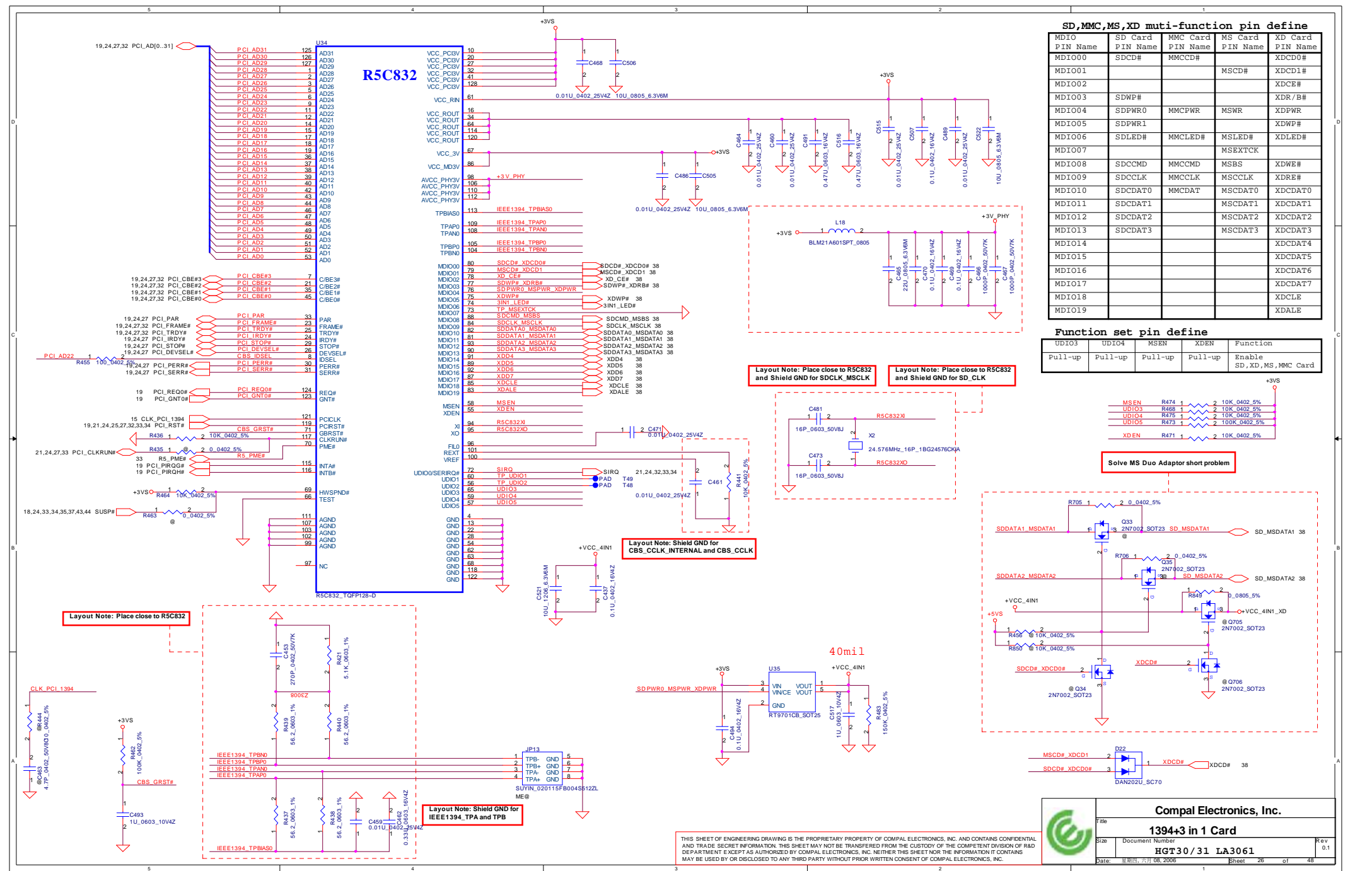
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PCMCIA Power Controller



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Compal Electronics, Inc.		
Title CardBus Socket		
Size	Document Number	Rev
Customer	IGL50/51 LA-3771	0.1
Date:	日期: 2006.10.06	Sheet 25 of 48



R5C832

SD,MMC,MS,XD multi-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO0	SDCD#	MMCCD#		XDCD0#
MDIO1	SDCD#		MSCD#	XDCD1#
MDIO2				XDCD#
MDIO3	SDWP#			XDR/B#
MDIO4	SDPWR0	MMCPWR	MSWR	XDPWR
MDIO5	SDPWR1			XDWP#
MDIO6	SDLED#	MMLED#	MSLED#	XDLED#
MDIO7				MSEXTC#
MDIO8	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO9	SDCLK	MMCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1		MSCDAT1	XDCDAT1
MDIO12	SDCDAT2		MSCDAT2	XDCDAT2
MDIO13	SDCDAT3		MSCDAT3	XDCDAT3
MDIO14				XDCDAT4
MDIO15				XDCDAT5
MDIO16				XDCDAT6
MDIO17				XDCDAT7
MDIO18				XDCLE
MDIO19				XDALE

Function set pin define

UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-up	Pull-up	Enable SD, XD, MS, MMC Card

Layout Note: Place close to R5C832 and Shield GND for SDCLK, MSCLK

Layout Note: Place close to R5C832 and Shield GND for SD_CLK

Solve MS Duo Adaptor short problem

Layout Note: Shield GND for CBS_CCLK_INTERNAL and CBS_CCLK

40mil

Layout Note: Shield GND for IEEET1394_TPA and TPB

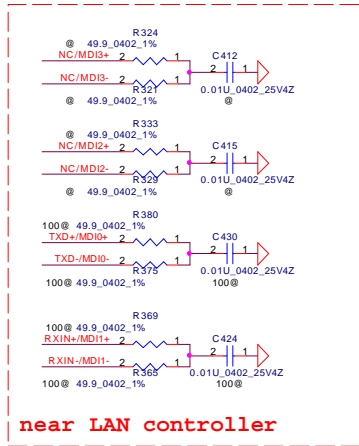
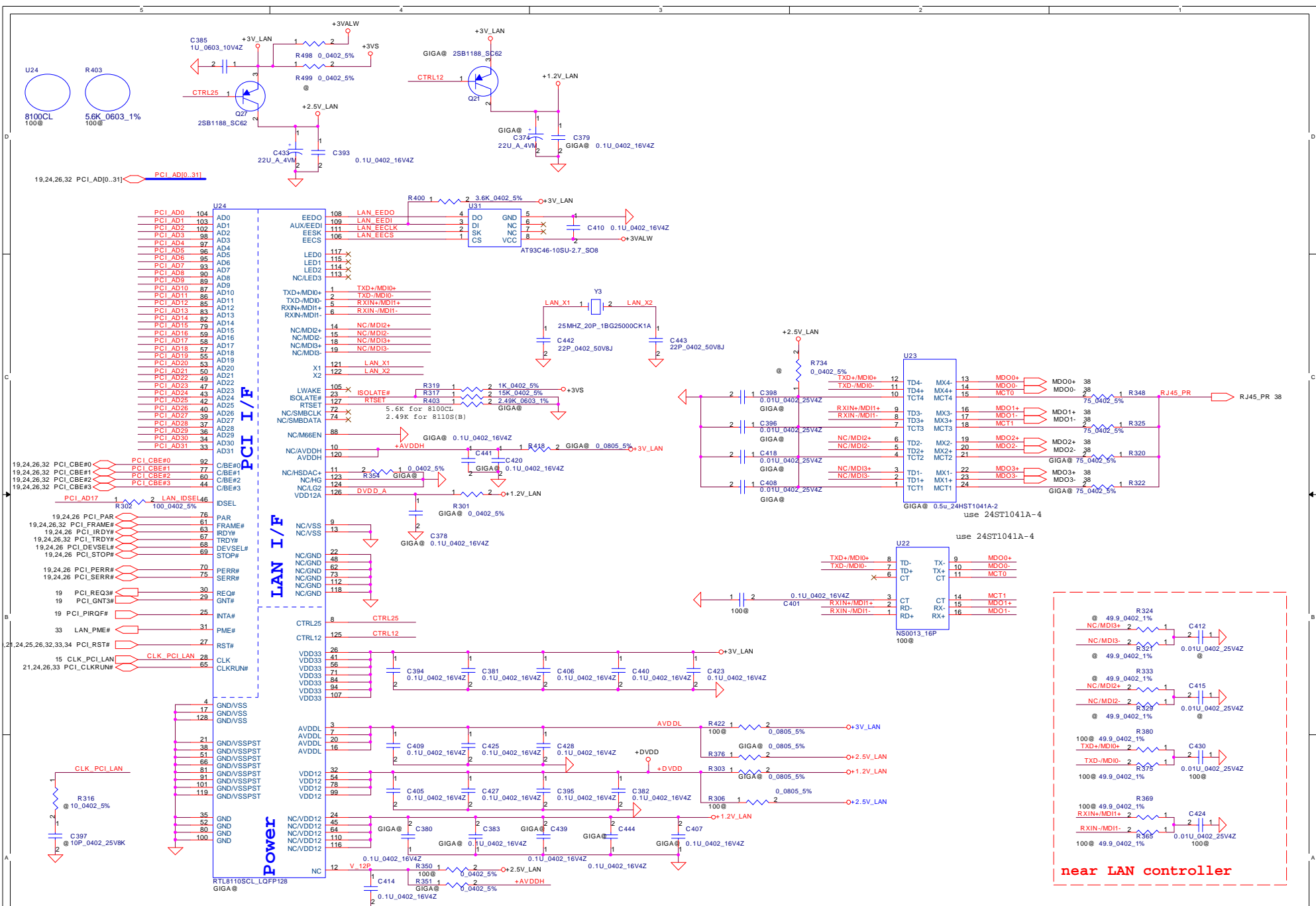
Layout Note: Place close to R5C832

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1394+3 in 1 Card

File	1394+3 in 1 Card		Rev	0.1
Size	Document Number			
	HGT30/31 LA3061			
Date	2008.08.26	Sheet	26	of 48



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Size	Document Number	Date		Sheet	Rev
Customer	IGL50/51 LA-3771	日期: 星期四, 六月 08, 2006		27	0.1
				of	48

Compal Electronics, Inc.

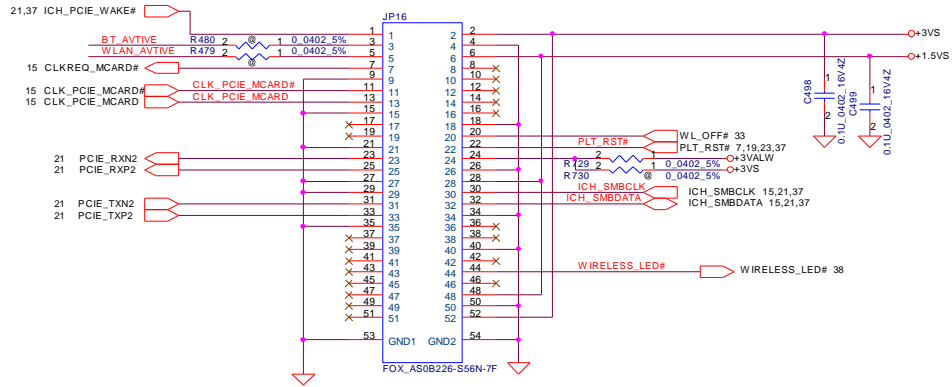
LAN CONTROLLER

IGL50/51 LA-3771

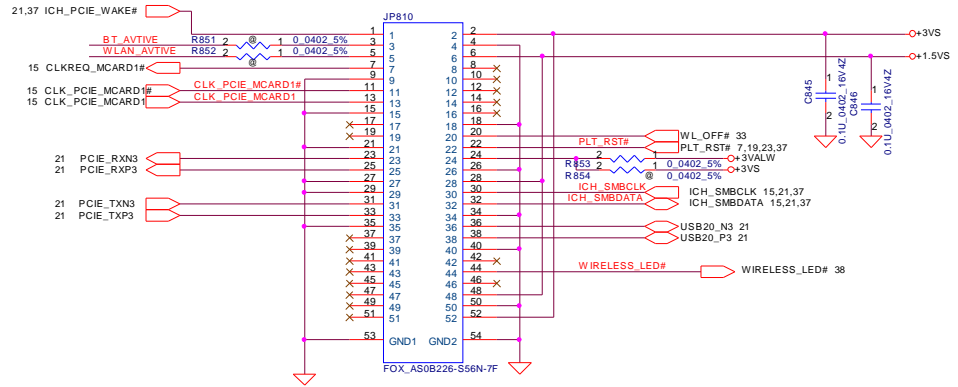
日期: 星期四, 六月 08, 2006

Sheet 27 of 48

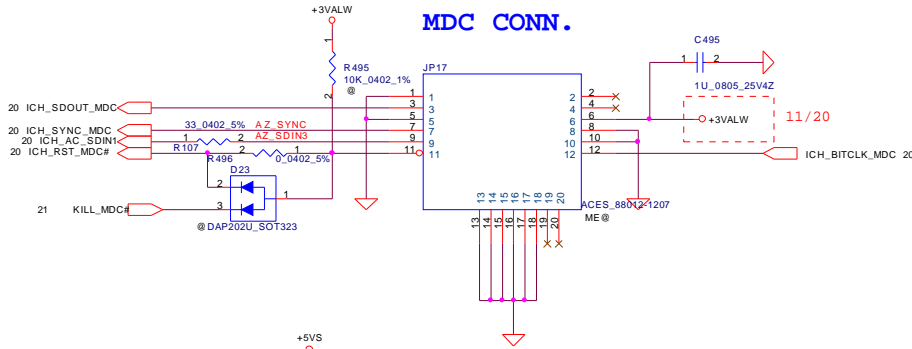
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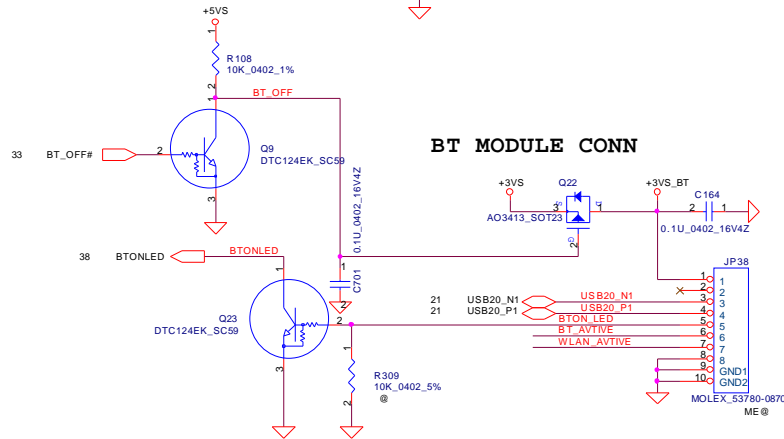
Mini-Express Card(Slot 2-WLAN)



MDC CONN.



BT MODULE CONN



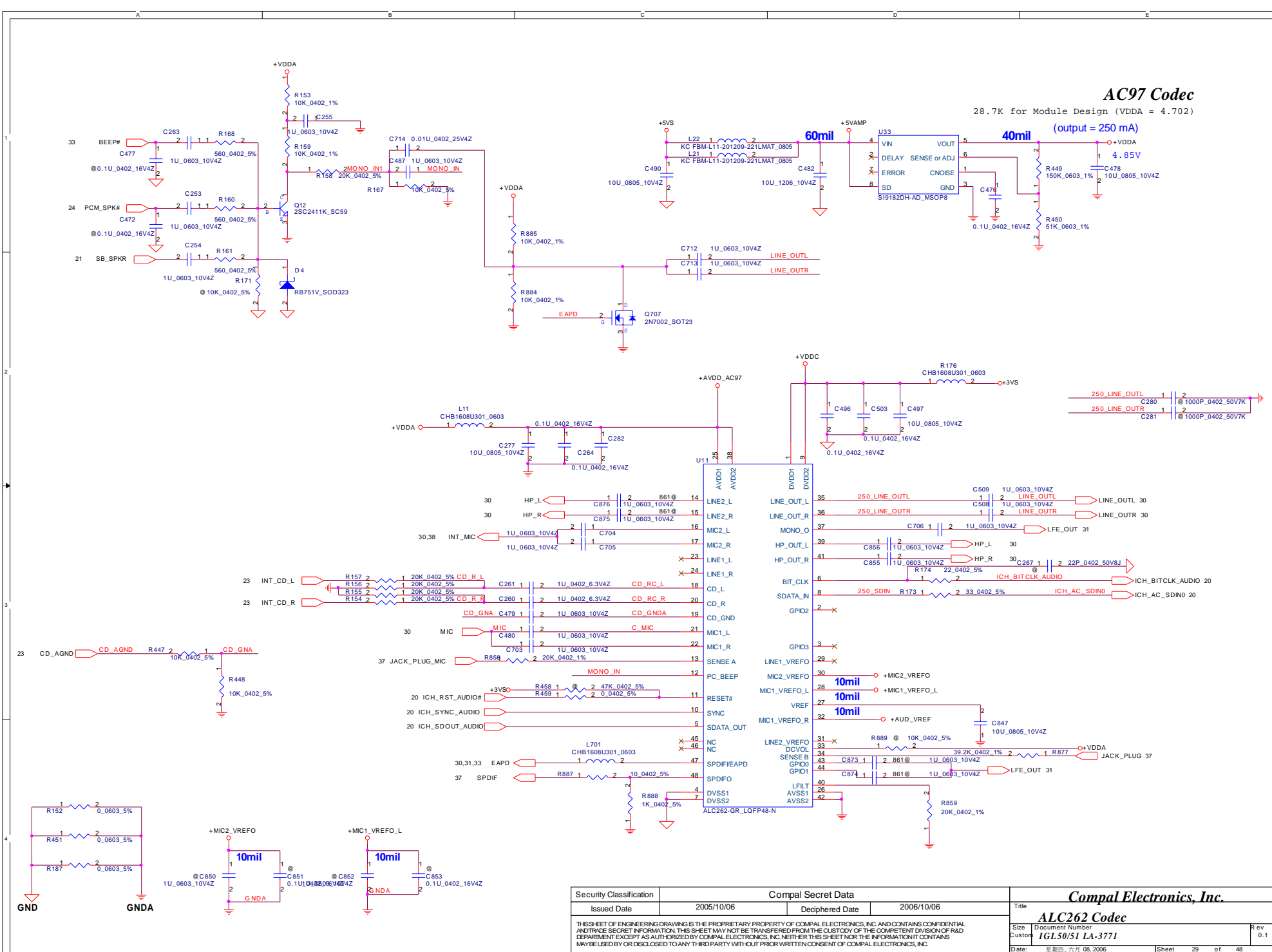
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Mini Card / MDC CONN		
Size	Document Number	R ev
Custom	IGL50/51 LA-3771	0.1
Date:	星期四, 六月 08, 2006	Sheet 28 of 48

AC97 Codec

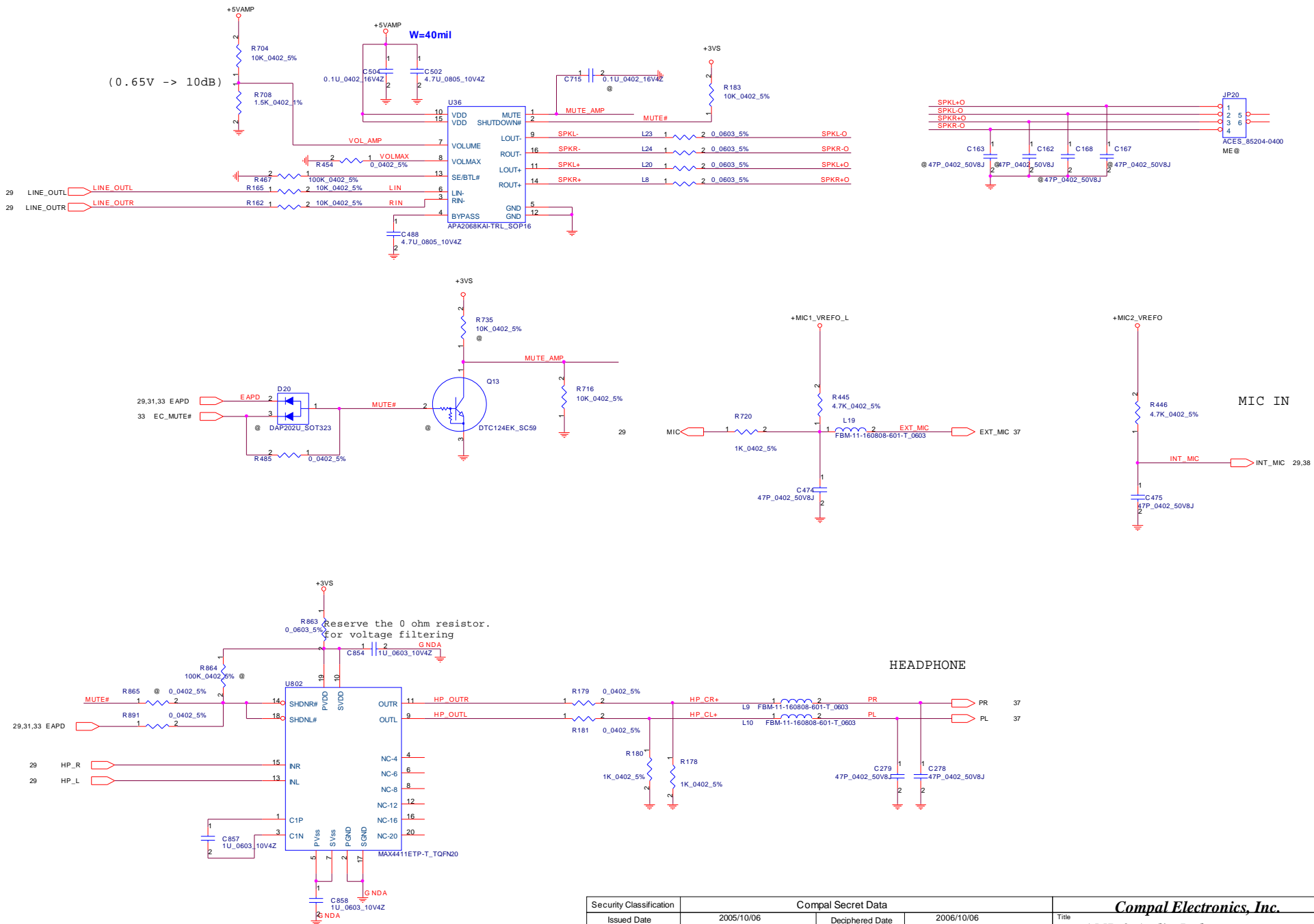
28.7K for Module Design (VDDA = 4.702)

(output = 250 mA)



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Title: ALC262 Codec		
Size	Document Number	R ev
Custom	1GL50/51 LA-3771	0.1
Date:	星期四, 六月 08, 2006	Sheet 29 of 48



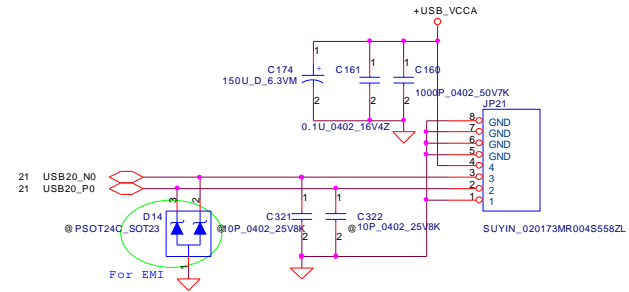
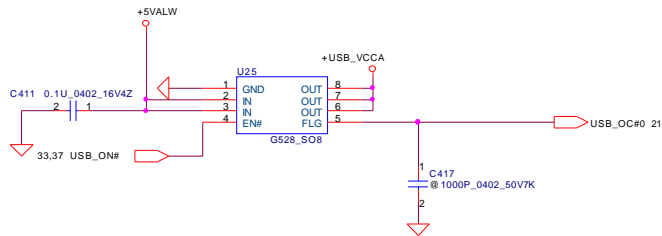
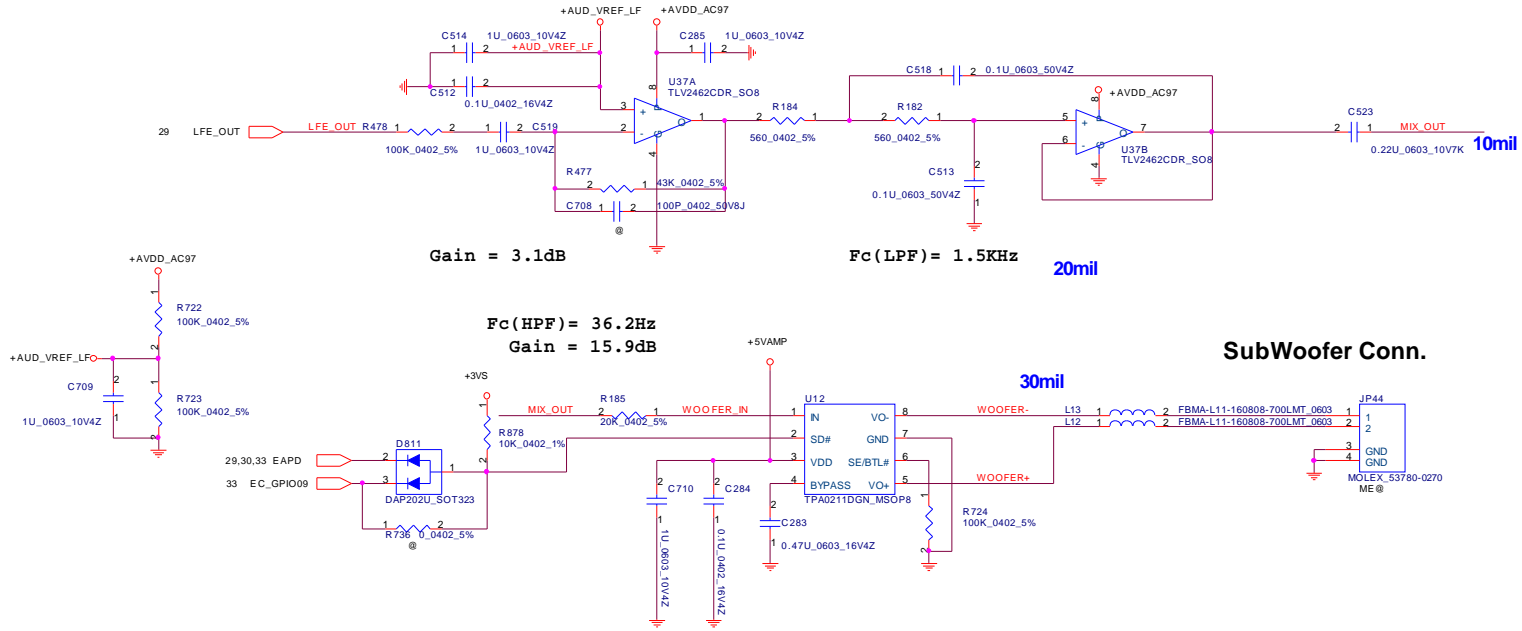
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		2006/10/06

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AMP & Audio Jack	
Size	Document Number
Custom	IGL50/51 LA-3771
Date:	Rev
星期四, 六月 08, 2006	0.1

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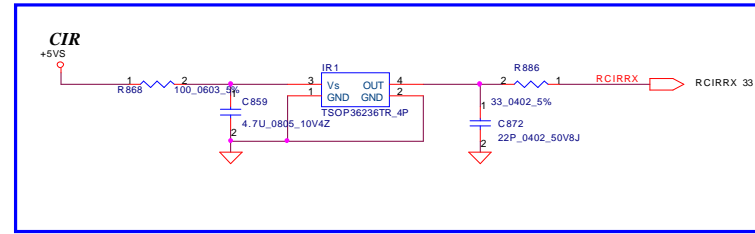
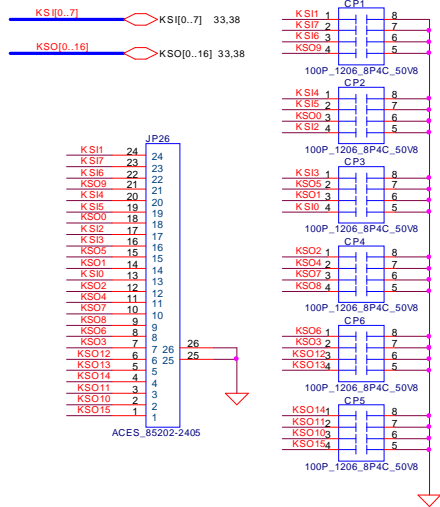
SUBWOOFER (Reserved for C38)

WOOFER@

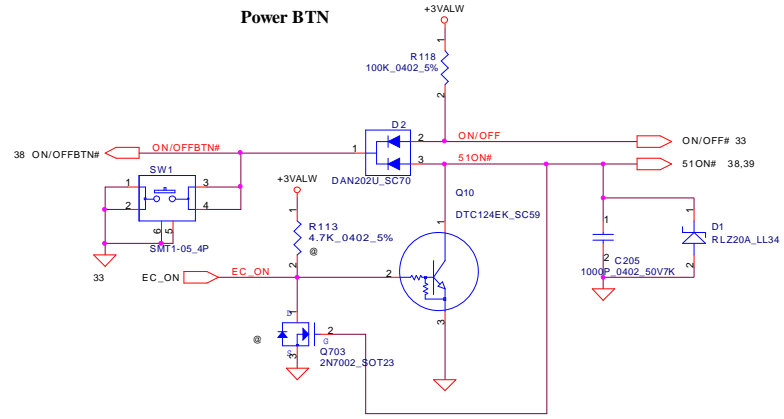


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				1GL50/51 LA-3771
Date:	星期四, 六月 08, 2006	Sheet	31 of 48	

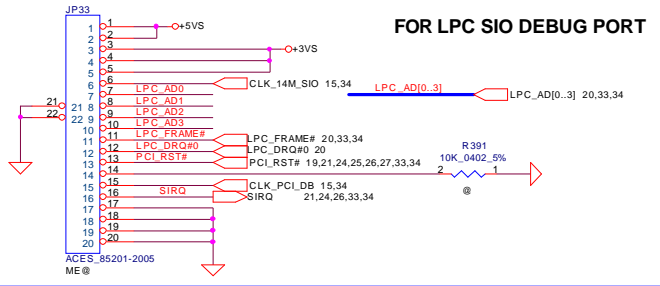
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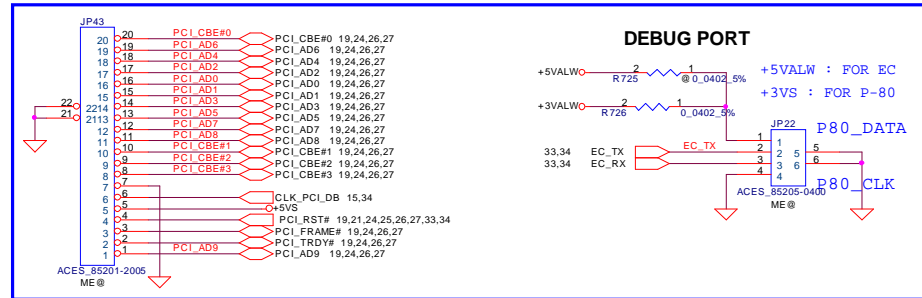
Power BTN



FOR LPC SIO DEBUG PORT

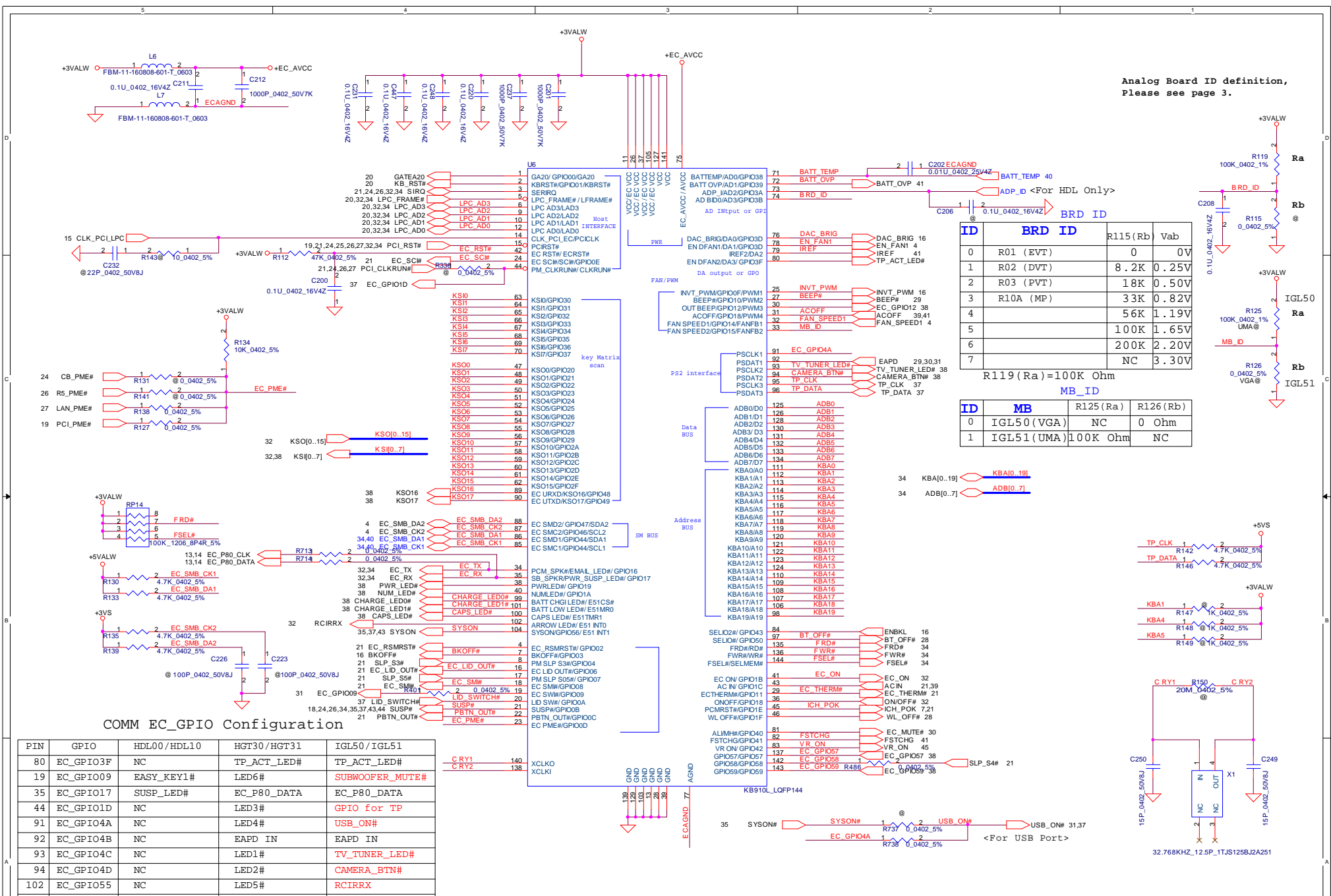


DEBUG PORT



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				Date:	Rev 0.1
				Date:	星期四, 六月 08, 2006
				Sheet	32 of 48

Analog Board ID definition,
Please see page 3.



ID	BRD ID	R115 (Rb)	Vab
0	R01 (EVT)	0	0V
1	R02 (DVT)	8.2K	0.25V
2	R03 (PVT)	1.8K	0.50V
3	R10A (MP)	33K	0.82V
4		56K	1.19V
5		100K	1.65V
6		200K	2.20V
7		NC	3.30V

R119 (Ra)=100K Ohm

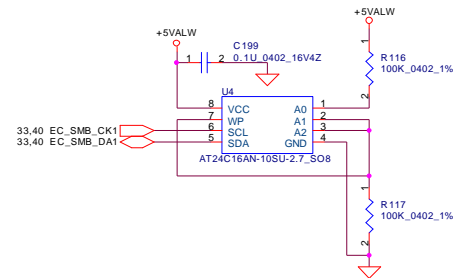
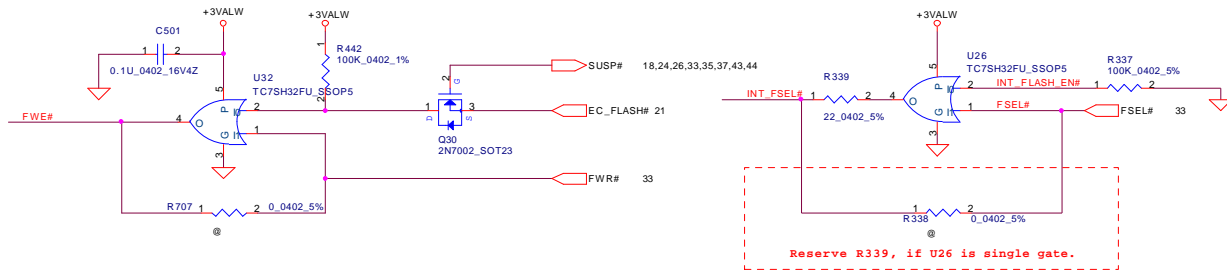
ID	MB	R125 (Ra)	R126 (Rb)
0	IGL50 (VGA)	NC	0 Ohm
1	IGL51 (UMA)	100K Ohm	NC

COMM EC_GPIO Configuration

PIN	GPIO	HDL00/HDL10	HGT30/HGT31	IGL50/IGL51
80	EC_GPIO3F	NC	TP_ACT_LED#	TP_ACT_LED#
19	EC_GPIO09	EASY_KEY1#	LED6#	SUBWOOFER_MUTE#
35	EC_GPIO17	SUSP_LED#	EC_P80_DATA	EC_P80_DATA
44	EC_GPIO1D	NC	LED3#	GPIO for TP
91	EC_GPIO4A	NC	LED4#	USB_ON#
92	EC_GPIO4B	NC	EAPD IN	EAPD IN
93	EC_GPIO4C	NC	LED1#	TV_TUNER_LED#
94	EC_GPIO4D	NC	LED2#	CAMERA_BTN#
102	EC_GPIO55	NC	LED5#	RCIRRX
97	EC_GPIO50	MEDIA#	BT_OFF#	BT_OFF#
137	EC_GPIO57	VOL_UP#	NOVO_BTN#	NOVO_BTN#
142	EC_GPIO58	VOL_DOWN#	SLP_S4#	SLP_S4#
143	EC_GPIO59	KILL_SW#	WIRE_LAN_BTN#	RF_BTN#
30	EC_GPIO12	AMP_MUTE	TP_LOCK_LED#	SUBWOOFER_BTN#

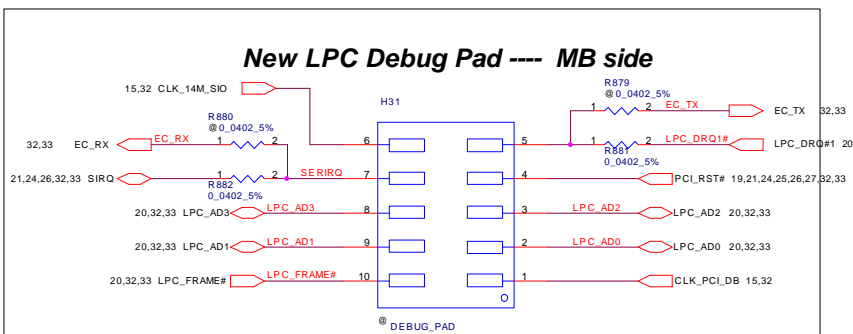
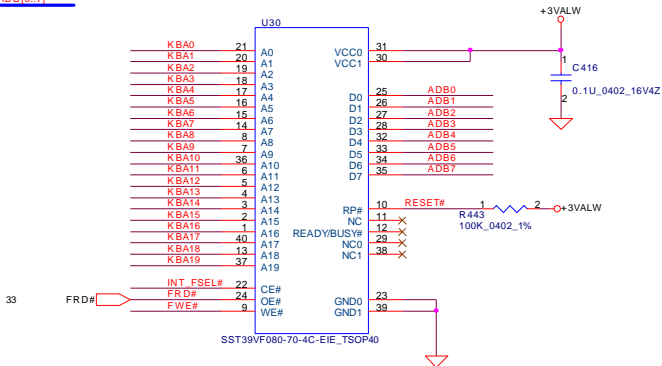
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ENE-KB910L	Document Number
IGL50/51 LA-3771	Rev 0.1
Date: 星期六月 08, 2006	Sheet 33 of 48

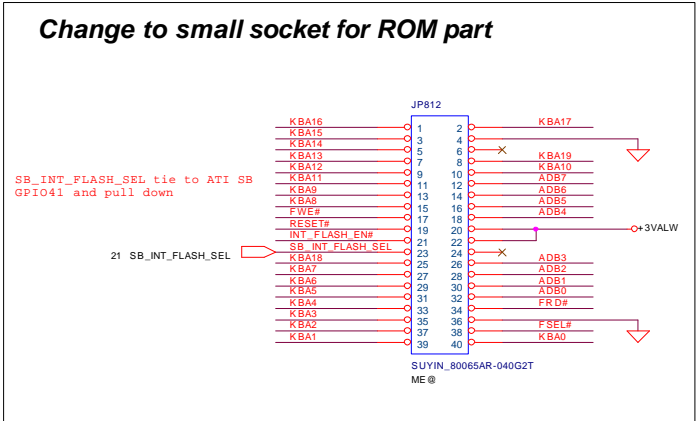


- 33 KBA[0..19] **KBA[0..19]**
- 33 ADB[0..7] **ADB[0..7]**

1MB Flash ROM

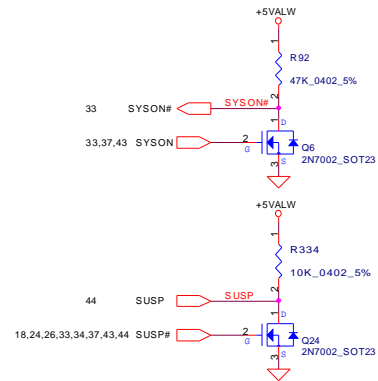
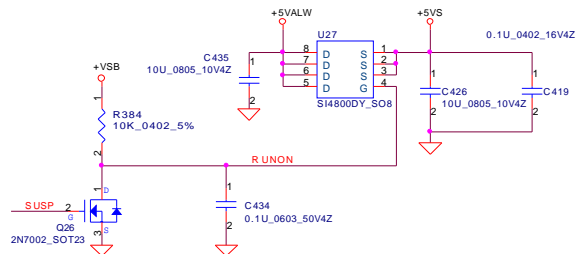


Under DDR ME Assignment Area
Keep Resistor near Debug Pad and in the same side
Standard side DIMM ---- Pin 1 near DIMM
Reverse side DIMM ---- Pin 1 keep away DIMM

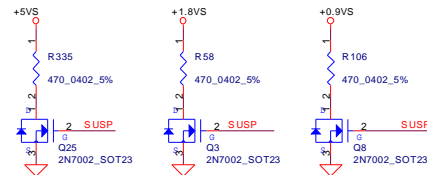
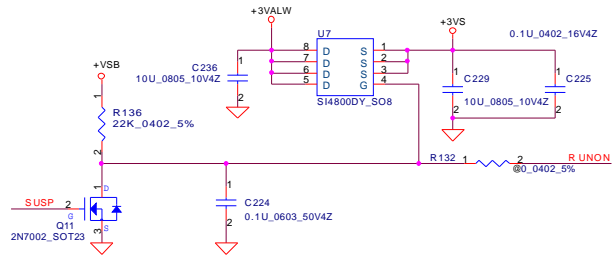


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Issued Date	2005/10/06	Deciphered Date	2006/10/06	BIOS & EC I/O Port	
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			Date:	星期四, 六月 08, 2006	Sheet 34 of 48

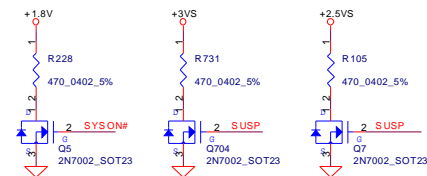
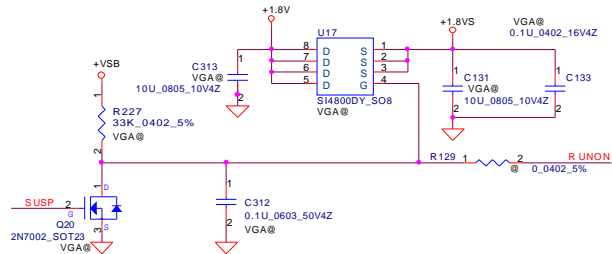
+5VALW to +5VS Transfer



+3VALW to +3VS Transfer

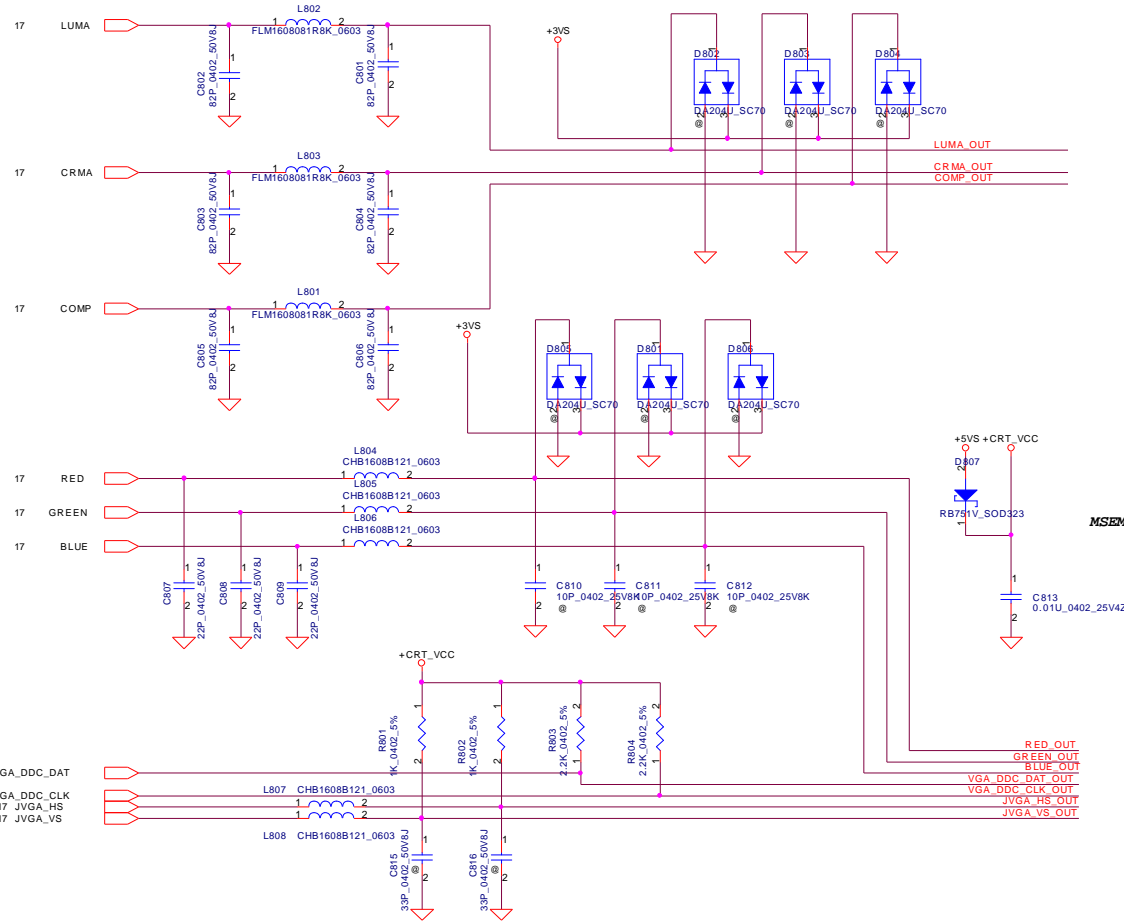


+1.8V to +1.8VS Transfer



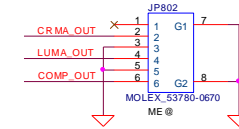
Security Classification	Compal Secret Data		Title	
Issued Date	2005/10/06	Deciphered Date	2006/10/06	DC/DC Circuit
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				Document Number IGL50/51 LA-3771
				Rev 0.1
				Date: 星期四, 六月 08, 2006
				Sheet 35 of 48

CLOSE TO JTVOUT1

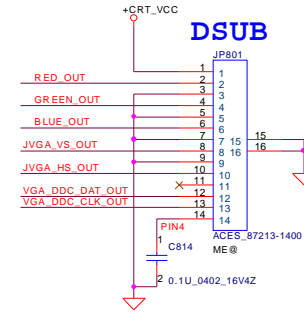


VGA I/O PORT Connector

S-VIDEO

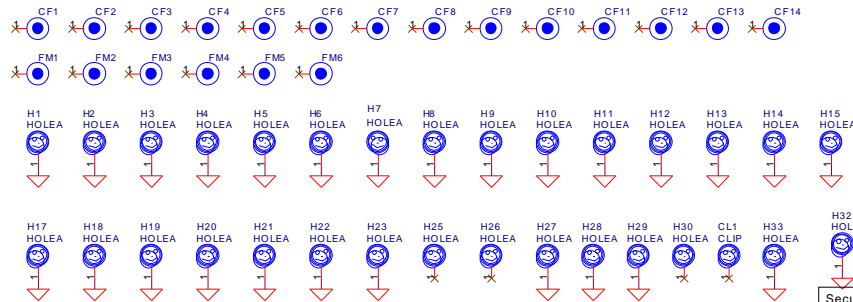


DSUB



PIN ASSIGNMENT

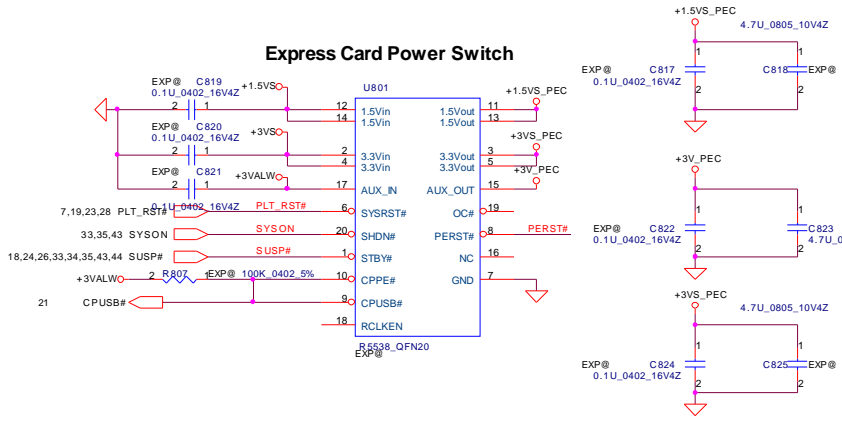
PIN	D-SUB	FUNCTION	PIN	SVIDEO	FUNCTION
1	9	+CRT_VCC	1	1	NC
2	1	RED	2	4	CRMA
3	6	GND	3	2	GND
4	2	GREEN	4	3	LUMA
5	7	GND	5	5	GND
6	3	BLUE	6	6	CVBS
7	8	GND			
8	14	VSYNC			
9	10	GND			
10	13	HSYNC			
11	11	SENSE			
12	12	SM_DAT			
13	15	SM_CLK			
14	4	PIN4			



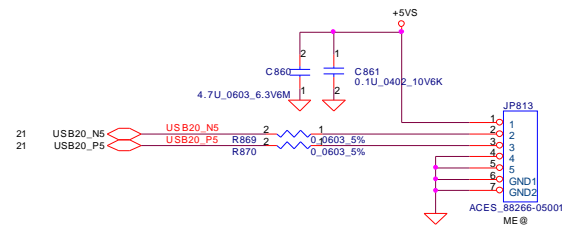
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	CRT & TVout Connector	
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				Customer	IGL50/51 LA-3771
				Date	Rev
				星期日, 六月 08, 2006	0.1
				Sheet	36 of 48

NEW CARD FOR C38

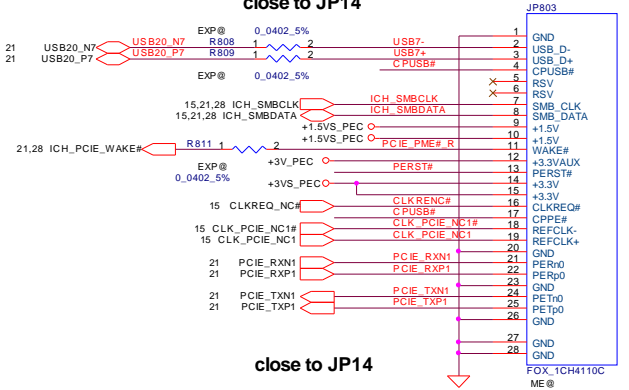
Express Card Power Switch



CMOS Camera Conn

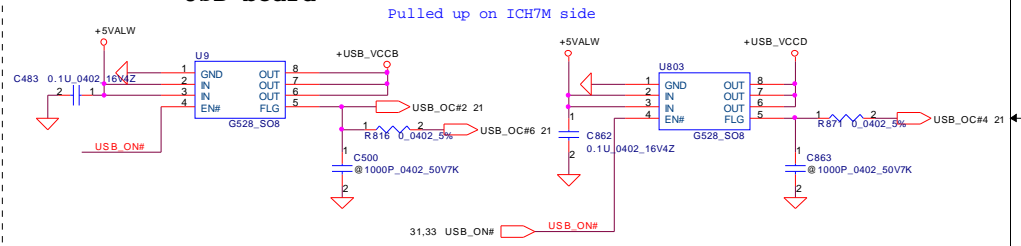


close to JP14



close to JP14

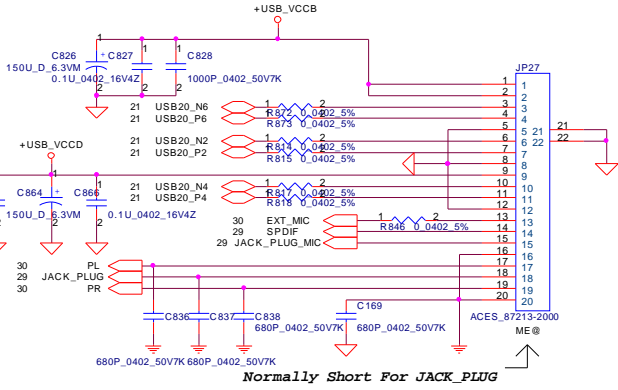
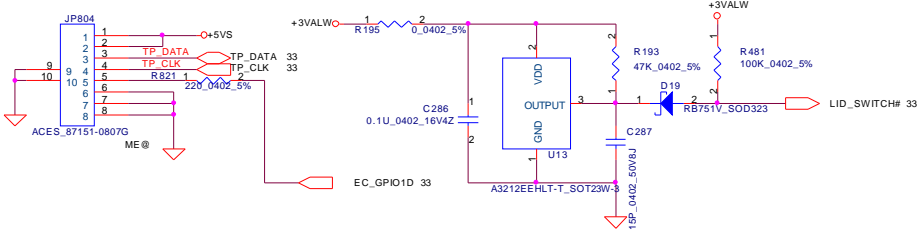
USB board



Pulled up on ICH7M side

T/P Board

LID Switch

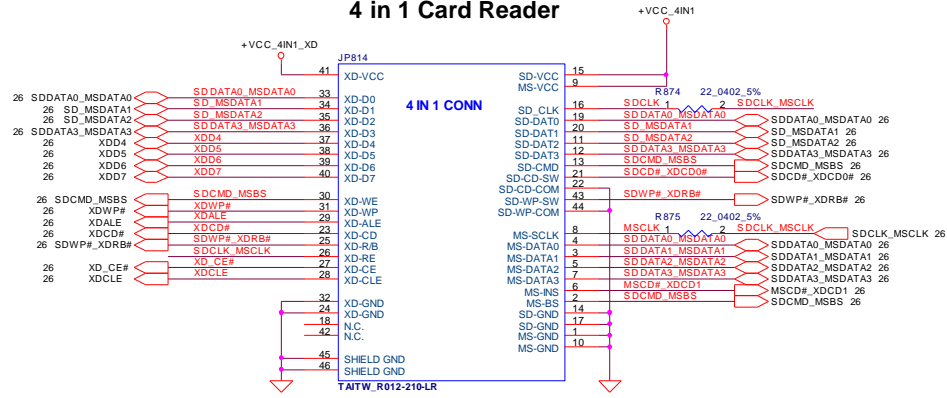


C835 ~ C838 For EMI Solution

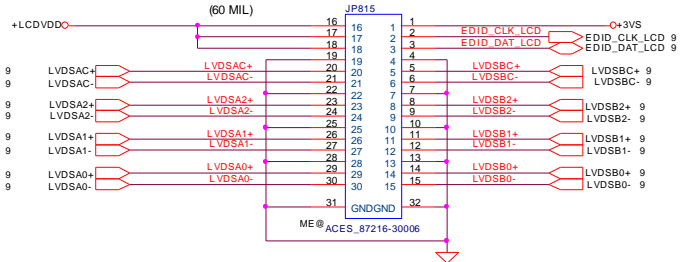
Normally Short For JACK_PLUG

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title	INDICATE LED
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Size	Document Number			Rev	0.1
Custom	IGL50/51 LA-3771			Date:	星期四, 六月 08, 2006
				Sheet	37 of 48

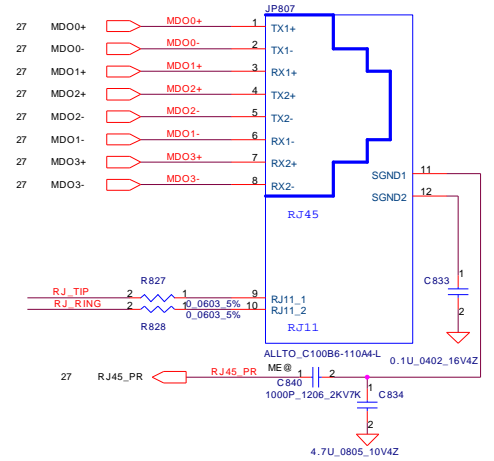
4 in 1 Card Reader



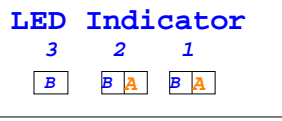
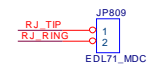
UMA LCD/PANEL Conn.



RJ11+RJ45 CONN



MDC CONN

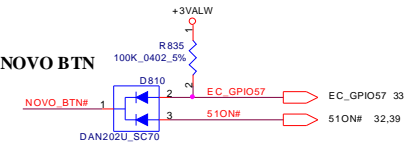
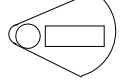


Wireless / Bluetooth LED **Blue**
 BATT_CHG_LED# **Blue**
 BATT_LOW_LED# **Amber**

STATUS	LED
AC	BLUE
Chargin	Blinking Blue
Low BATT	Amber

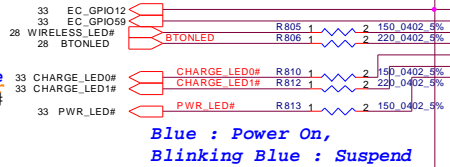
Function		
KEY Matrix	K016	K017
KSI0	DW-UP	DW-DOWN
KSI1	DW-ENTER	MUTE

Dial Wheel



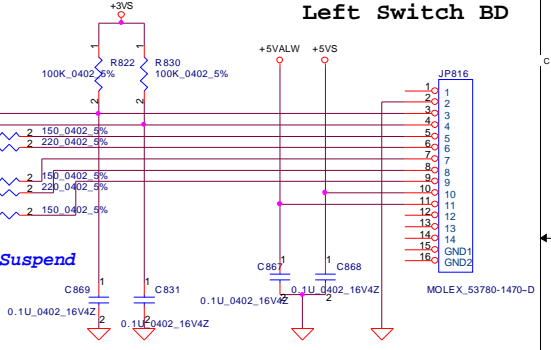
SUBWOOFER_ON/OFF_BTN#

RF_ON/OFF_BTN#

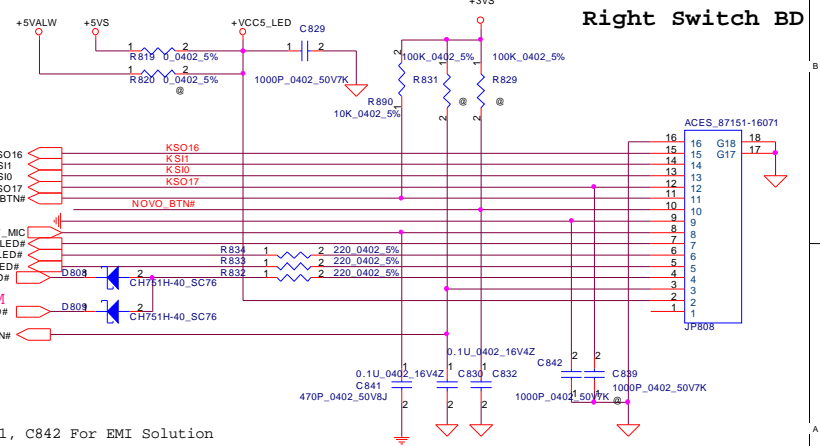


Blue : Power On,
Blinking Blue : Suspend

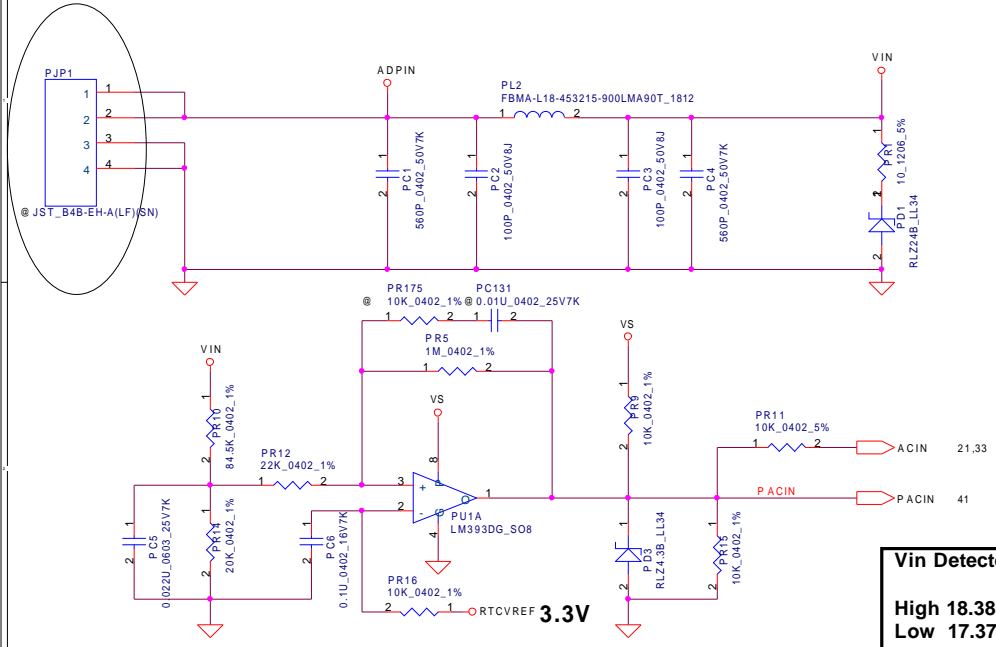
Left Switch BD



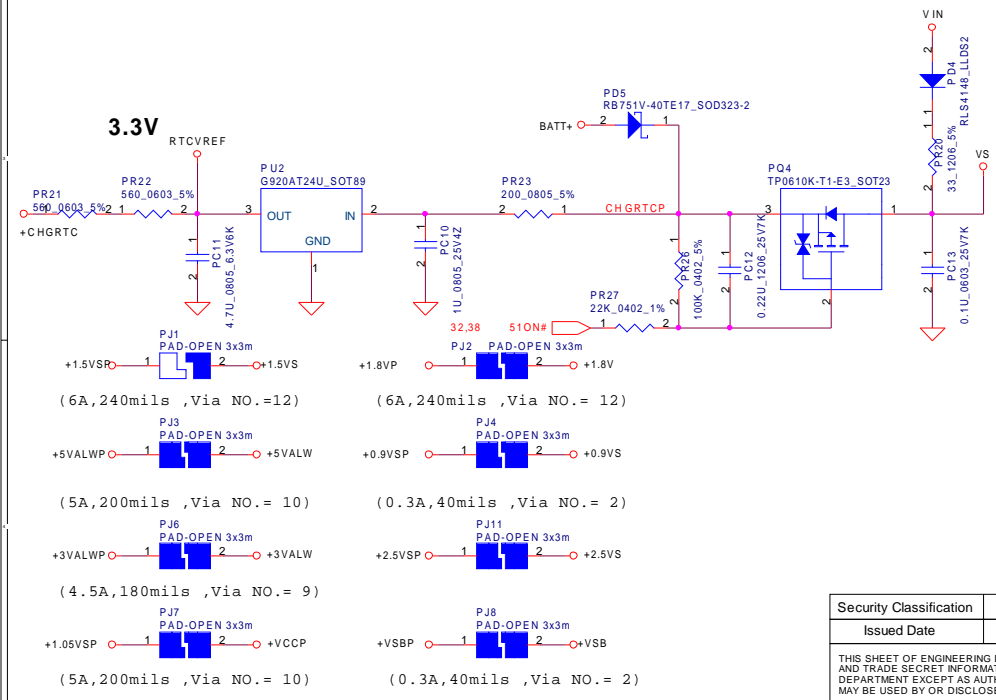
Right Switch BD



C839, C841, C842 For EMI Solution

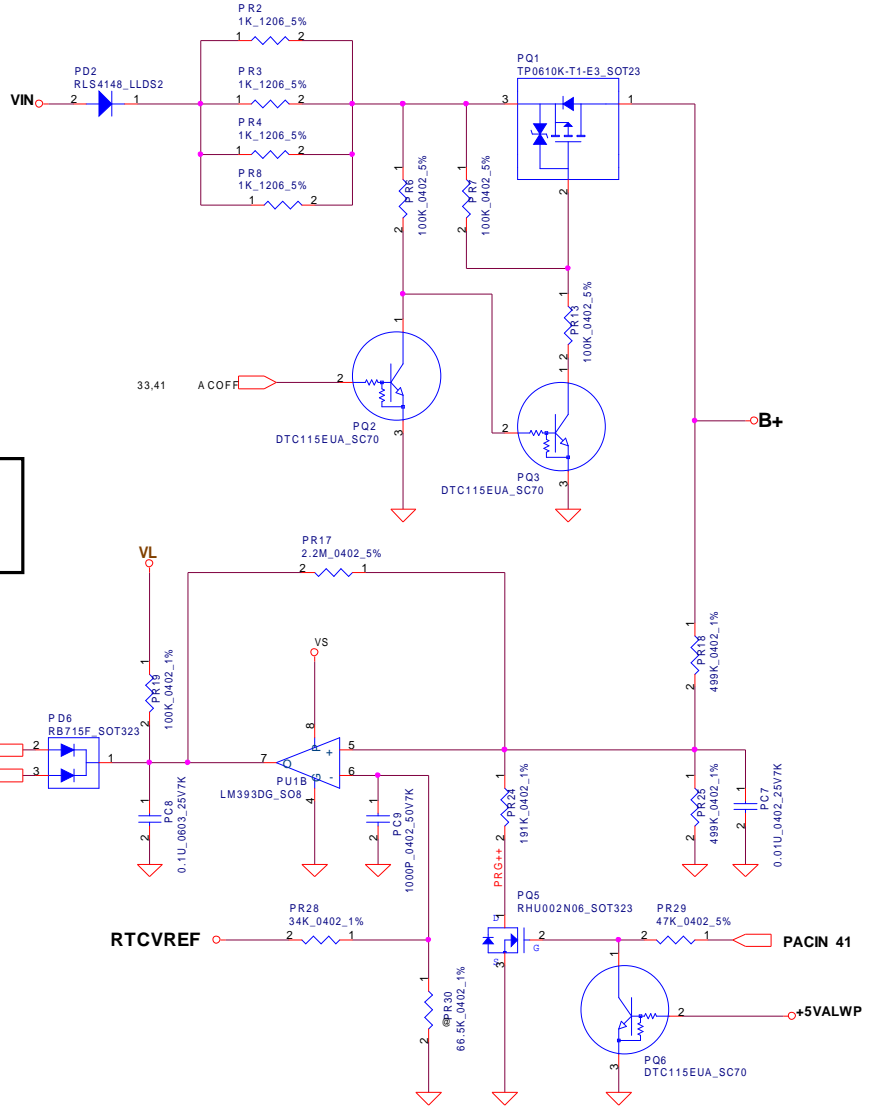


Vin Detector			
High	18.384	17.901	17.430
Low	17.370	16.907	16.630



ACIN			
Precharge detector			
	Min.	typ.	Max.
H-->L	14.620V	14.853V	15.245V
L-->H	15.534V	15.970V	16.421V

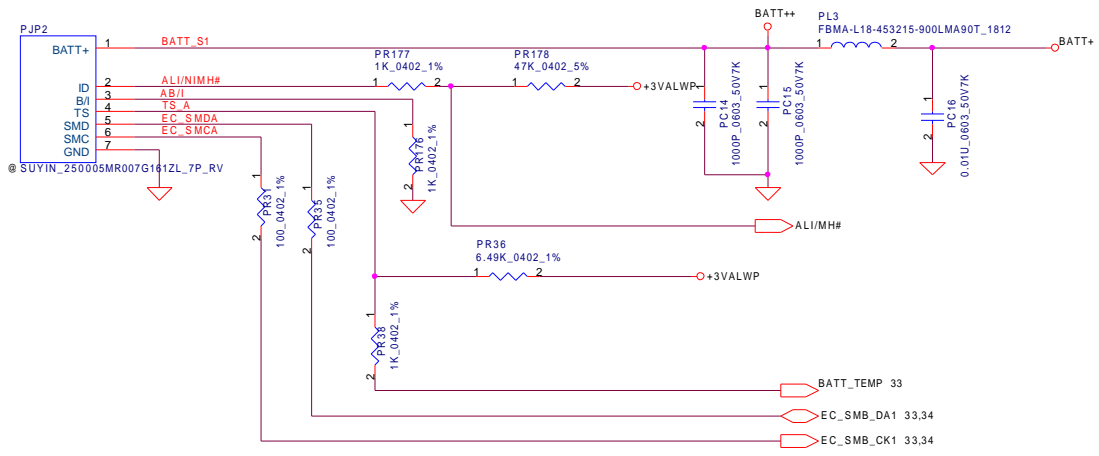
BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H-->L	6.169V	6.231V	6.361V
L-->H	7.168V	7.349V	7.537V



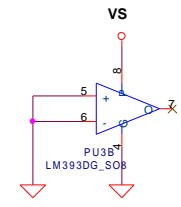
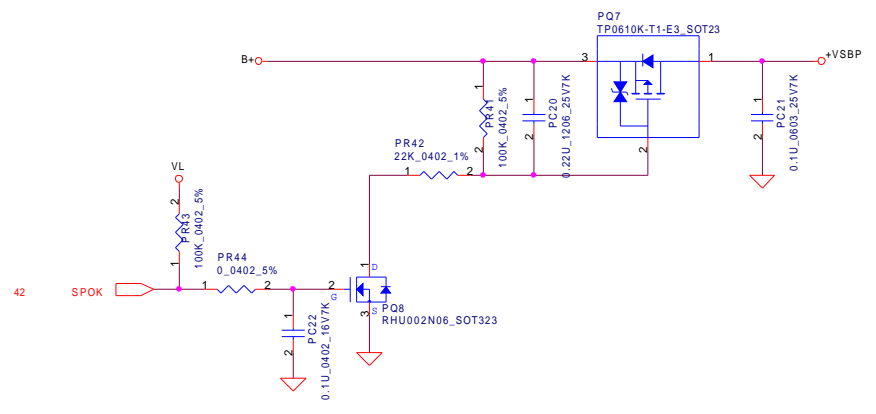
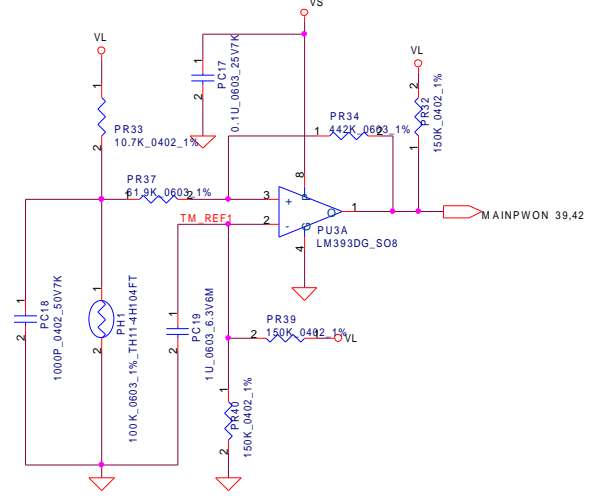
Security Classification	Compal Secret Data	
Issued Date	2005/08/01	Deciphered Date
		2006/08/01

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Title		
DCIN/DECTOR		
Size	Document Number	Rev
B		0.1
Date:	星期四, 六月 08, 2006	Sheet 39 of 48

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PH1 under CPU bottom side :
 CPU thermal protection at 85 degree C
 Recovery at 70 degree C

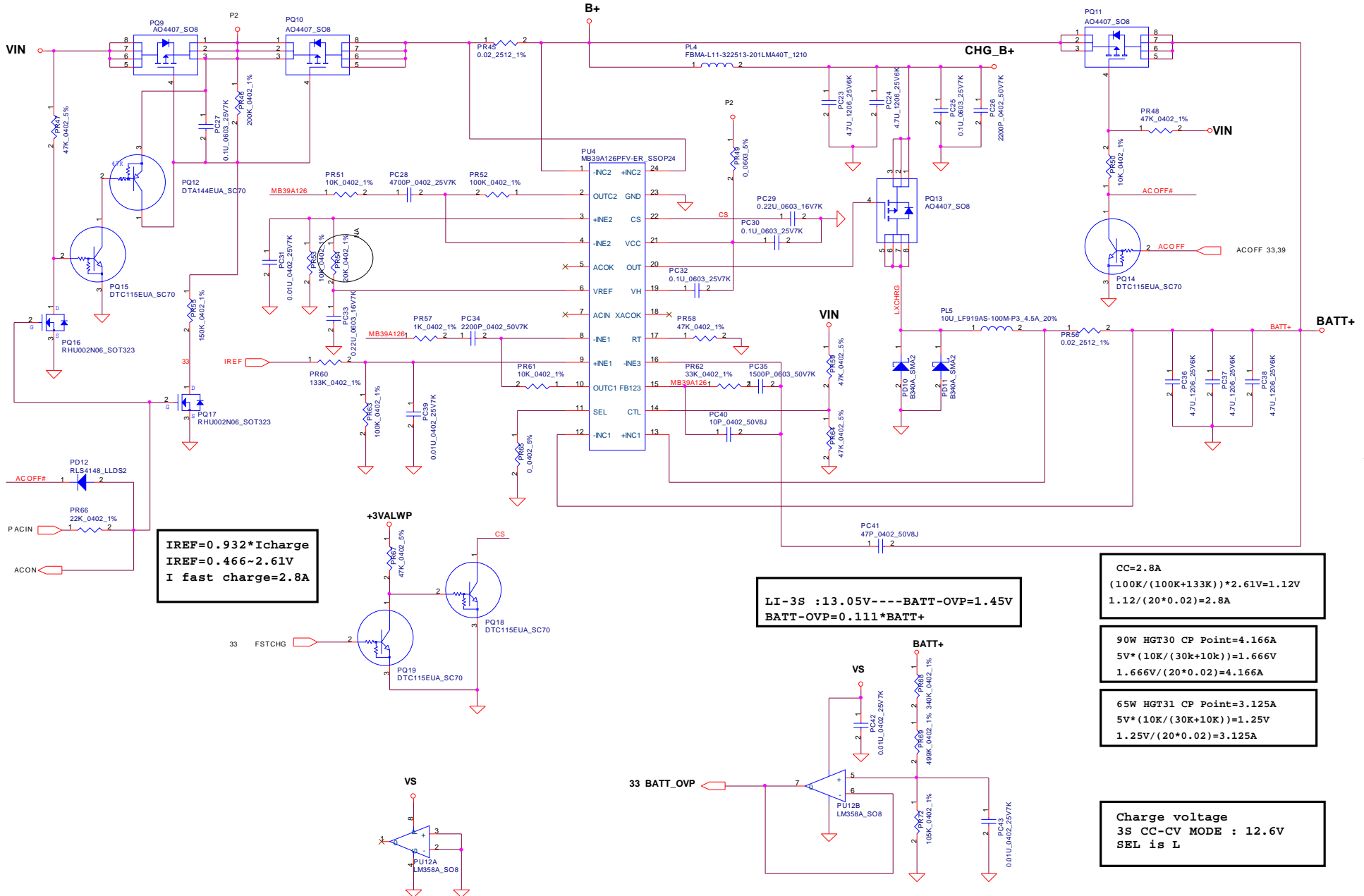


Security Classification		Compal Secret Data		Title		
Issued Date	2005/08/01	Deciphered Date	2006/08/01	BATTERY CONN. / OTP		
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Date: 星期四, 六月 08, 2006				Sheet 40	of 48	

65W PR45=0.02_2512_1% PR54=30K_0402_1% Iadp=0~3.125A
 90W PR45=0.02_2512_1% PR54=20K_0402_1% Iadp=0~4.166A

Fosc=14100/Rt=14100/47=300KHz

Charger



IREF=0.932*Icharge
 IREF=0.466~2.61V
 I fast charge=2.8A

LI-3S :13.05V----BATT-OVP=1.45V
 BATT-OVP=0.111*BATT+

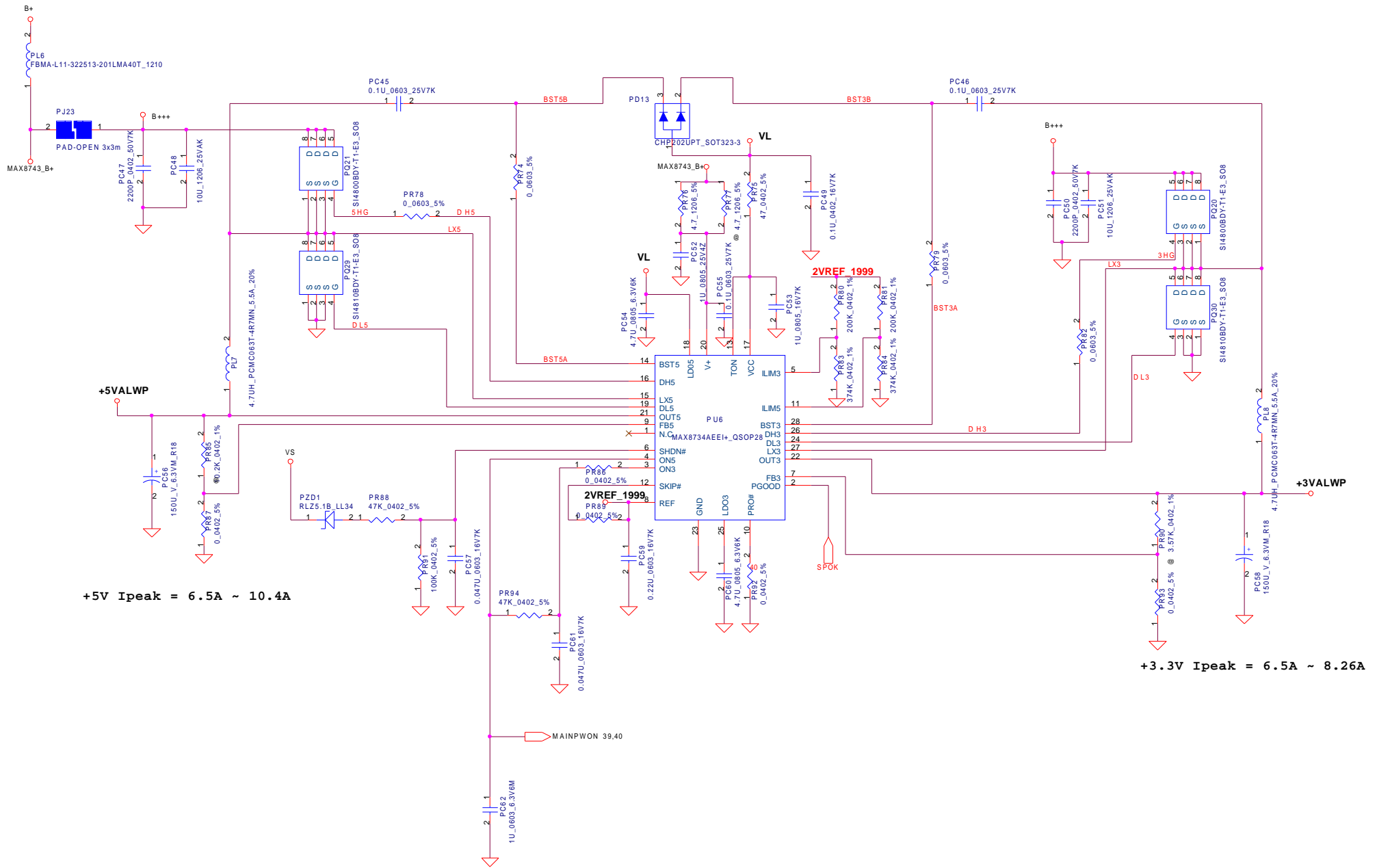
CC=2.8A
 $(100K/(100K+133K))*2.61V=1.12V$
 $1.12/(20*0.02)=2.8A$

90W HGT30 CP Point=4.166A
 $5V*(10K/(30K+10K))=1.666V$
 $1.666V/(20*0.02)=4.166A$

65W HGT31 CP Point=3.125A
 $5V*(10K/(30K+10K))=1.25V$
 $1.25V/(20*0.02)=3.125A$

Charge voltage
 3S CC-CV MODE : 12.6V
 SEL is L

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Size	Document Number	Date		Sheet	Rev
B		Date: 星期日, 六月 08, 2006		41	0.1
				of	48

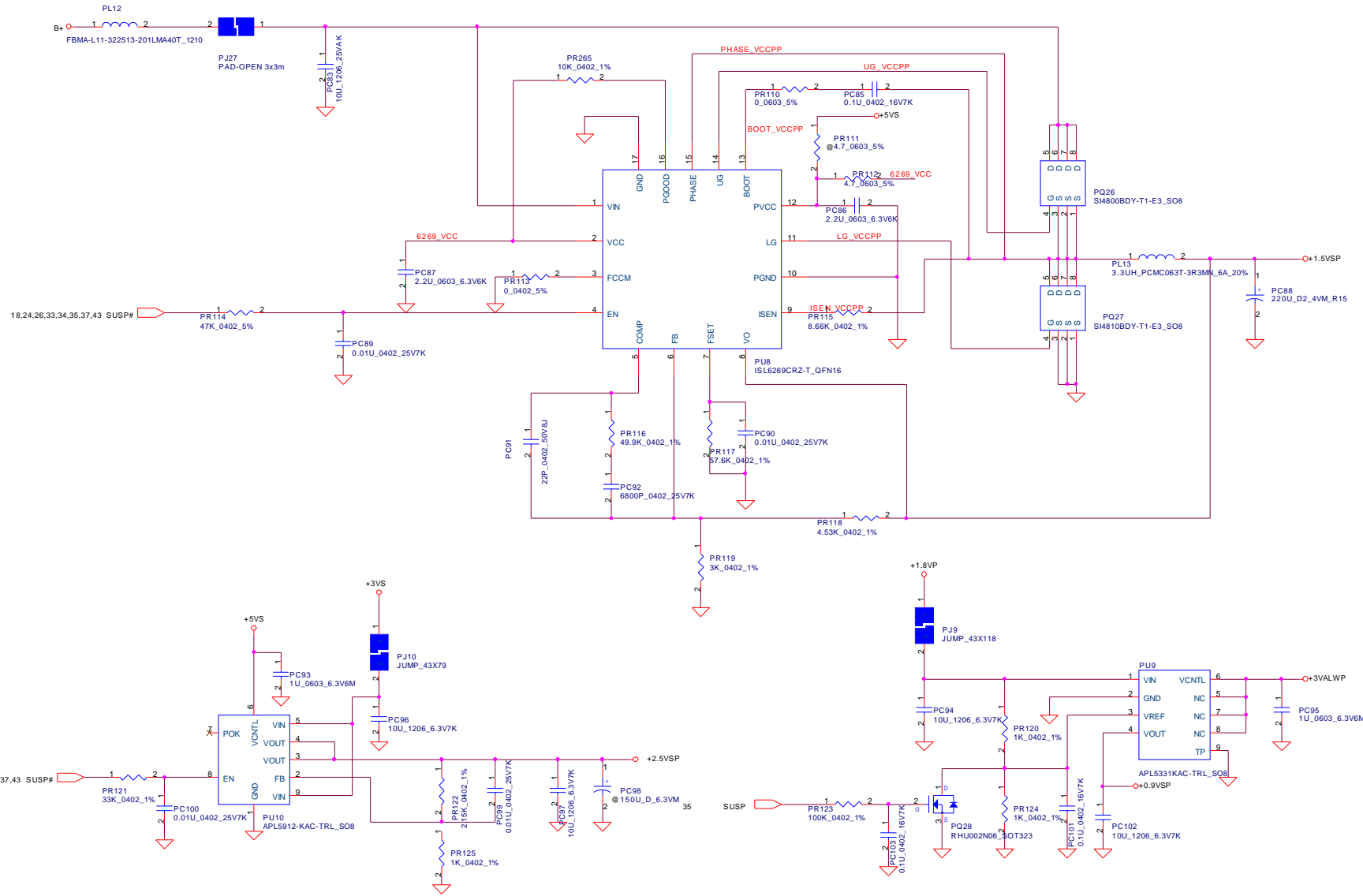


+5V Ipeak = 6.5A ~ 10.4A

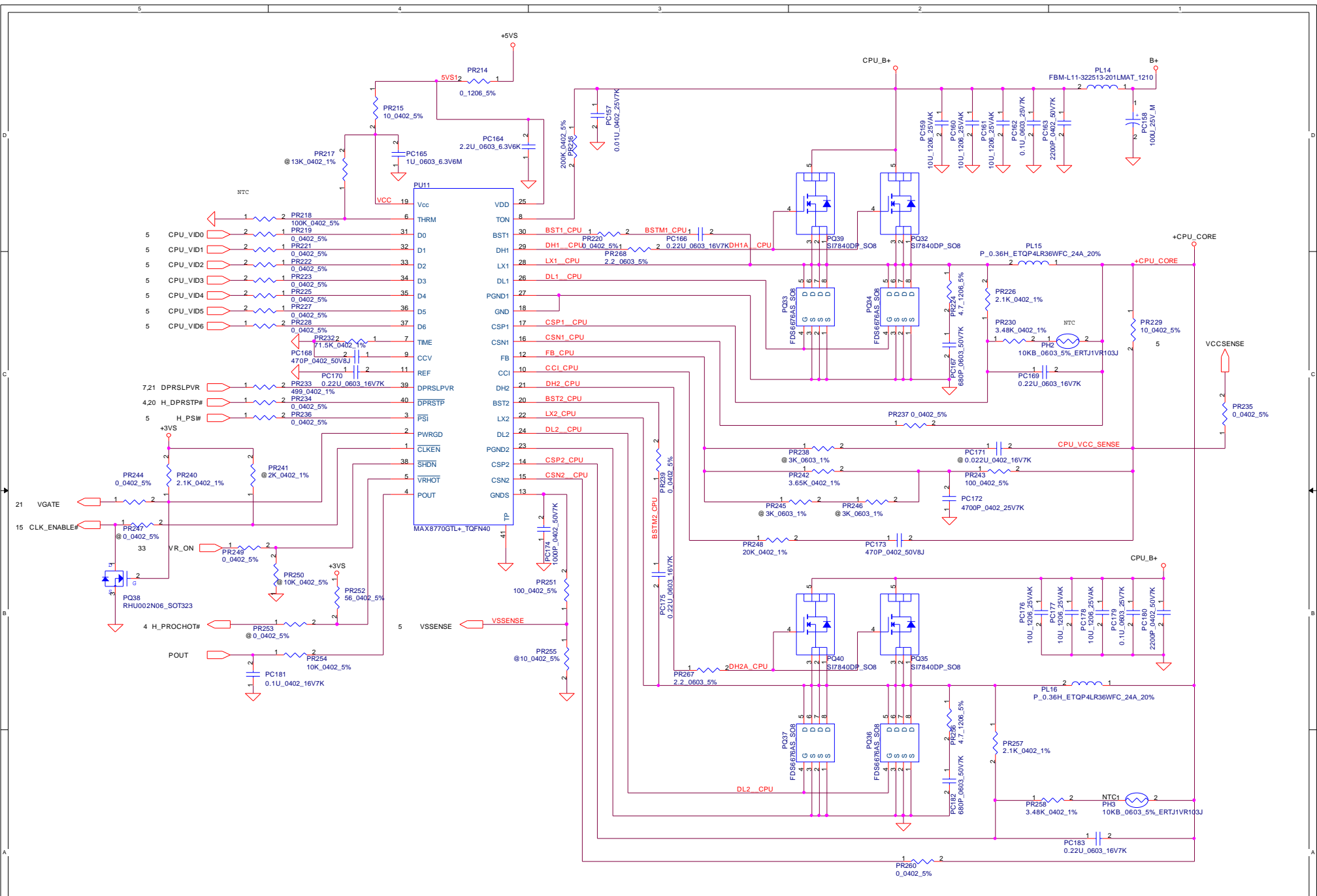
+3.3V Ipeak = 6.5A ~ 8.26A

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/08/01	Deciphered Date	2006/08/01	Title	
				+5VALWP/+3VALWP	
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				Custom	Rev 0.1
Date: 星期四, 六月 08, 2006				Sheet	42 of 48

+1.5VSP Ilimit = 9.38A-12.5A



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Issued Date	2005/08/01	Deciphered Date	2006/08/01	Title +VCCPP/+2.5VSP/0.9VSP	
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Security Classification		Compal Secret Data		Title	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	+CPU_CORE	
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Date:	星期四, 六月 08, 2006	Sheet	45 of 48	Size	Document Number
				Custom	Rev 0.1

Version change list (P.I.R. List)

Page 1 of 1
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
8							
9							

Compal Electronics, Inc.			
Title PIR (PWR)			
Size	Document Number		Rev 0.2
Date: 星期四, 六月 08, 2006	Sheet	46 of 48	

Version change list (P.I.R. List)

Item	Fixed Issue	Rev.	PG#	Modify List	B.Ver#	Phase
1					0.2	DVT
2					0.2	DVT
3					0.2	DVT
4					0.2	DVT
5					0.2	DVT
6					0.2	DVT
7					0.2	DVT
8					0.2	DVT
9					0.2	DVT
10					0.2	DVT
11					0.2	DVT

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Compal Electronics, Inc.		
Title PIR		
Size	Document Number HGT30/31 LA-3061	Rev 0.0
Date: 星期一, 六月 08, 2006	Sheet 47	of 48

Version change list (P.I.R. List)

Item	Fixed Issue	Rev.	PG#	Modify List	B.Ver#	Phase
12					0.3	PVT
13					0.3	PVT
14					0.3	PVT
15					0.3	PVT
16					0.3	PVT

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Compal Electronics, Inc.		
Title PIR		
Size	Document Number HGT30/31 LA-3061	Rev 0.0
Date: 星期一, 六月 08, 2006	Sheet 48	of 48