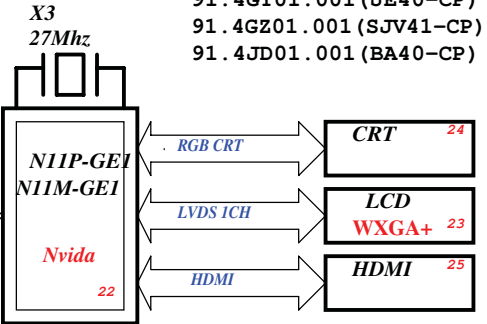
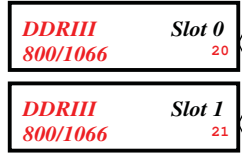
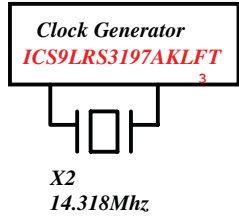


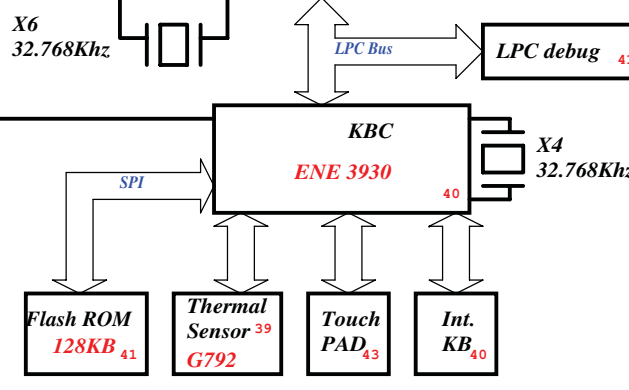
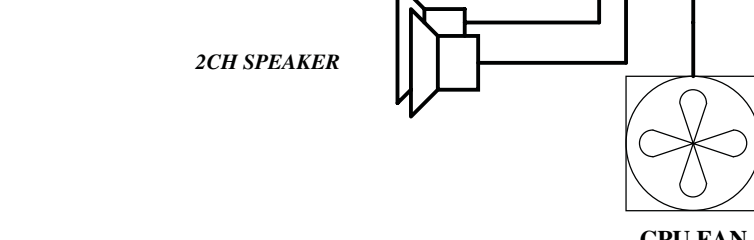
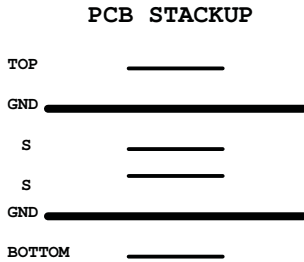
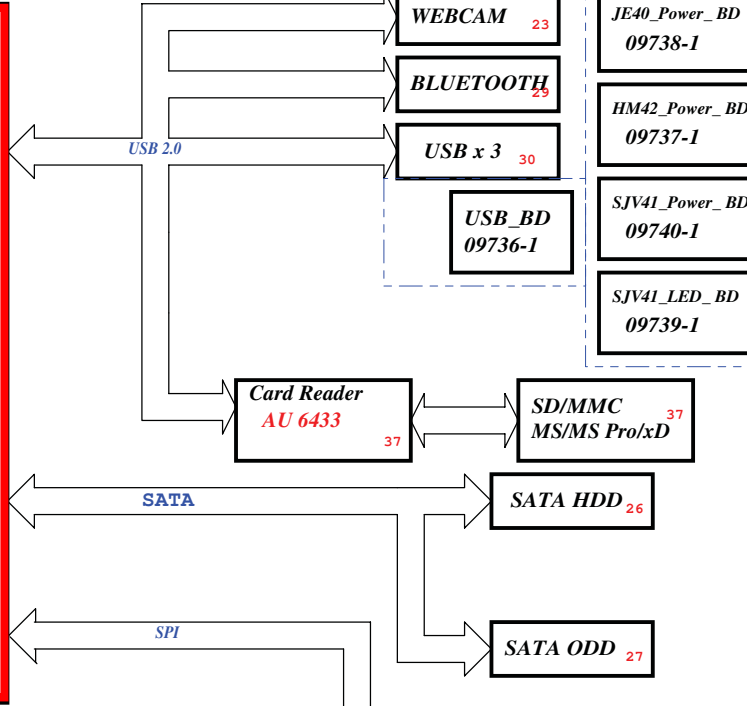
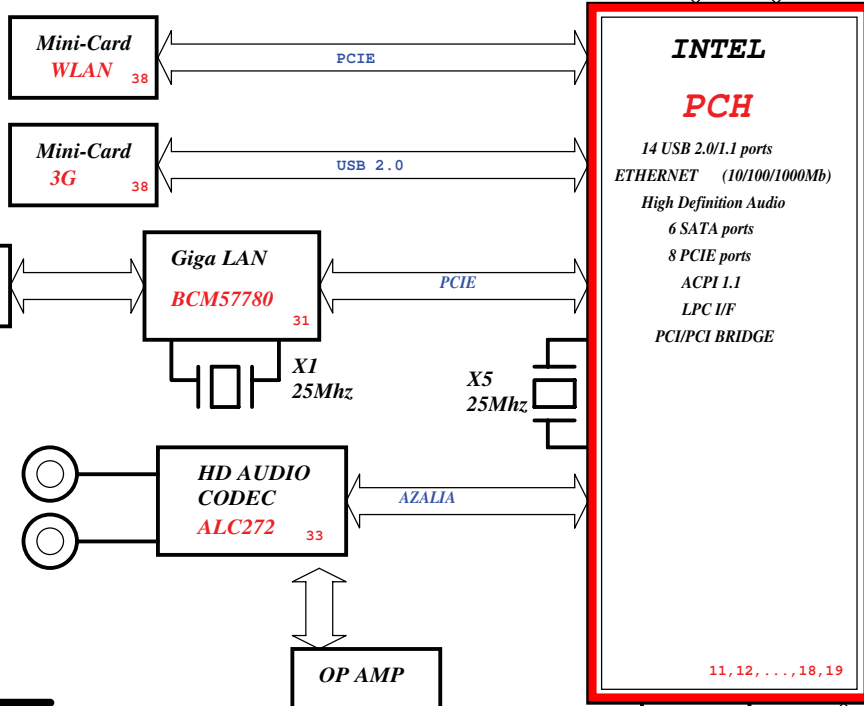
HM42-CP Block Diagram

PCB P/N : 48.4GW01.011
 REVISION : -1 09920

Project code: 91.4GW01.001 (HM42-CP)
 91.4GY01.001 (JE40-CP)
 91.4GZ01.001 (SJV41-CP)
 91.4JD01.001 (BA40-CP)



SYSTEM DC/DC RT8223	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 49
SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 50
SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 1D05V_S0 51
SYSTEM DC/DC RT9025	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S0 52
SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 55
SYSTEM DC/DC TPS5161	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 47, 48
CPU DC/DC ISL62882C	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 47, 48
CHARGER ISL88731C	
INPUTS	OUTPUTS
DCBATOUT	BT+ 53



Discrete N11M

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Title: **Block Diagram**

Size A3 Document Number **HM42-CP** Rev **SC**

Date: Friday, January 22, 2010 Sheet 1 of 72

PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

USB Table

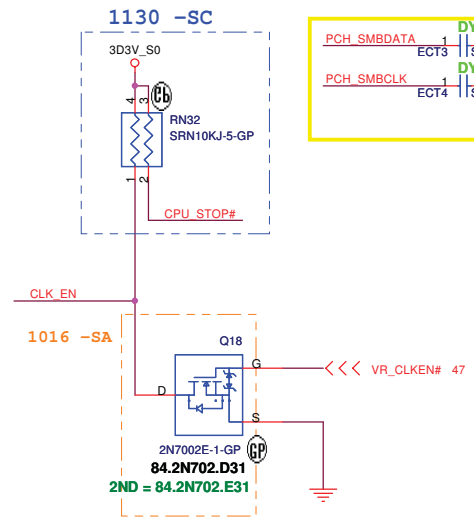
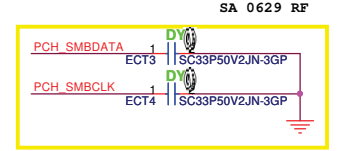
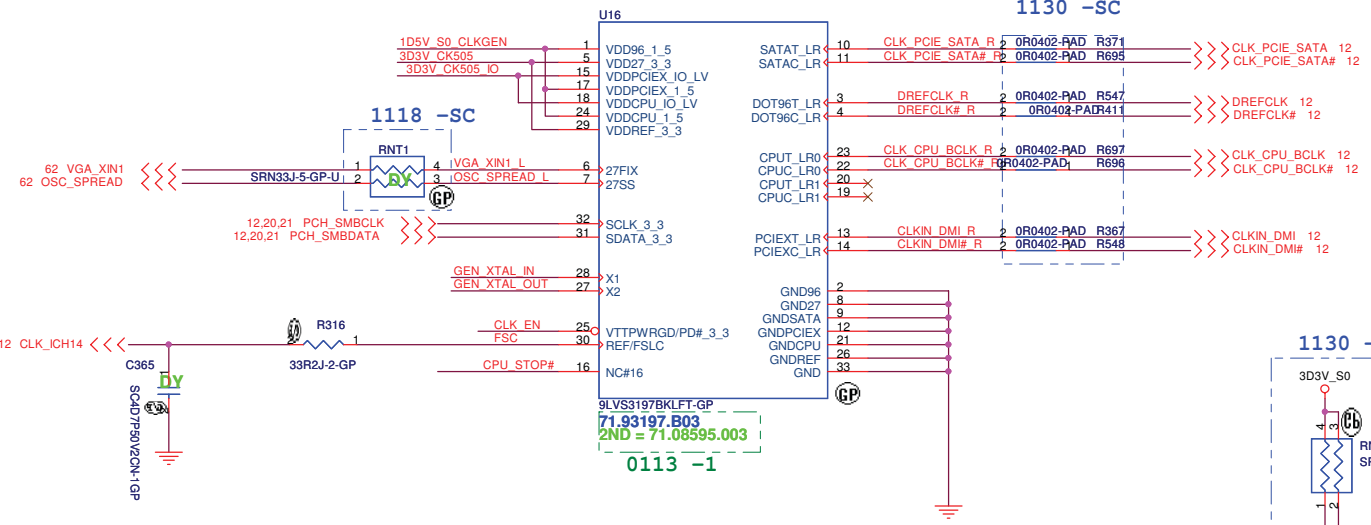
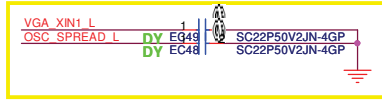
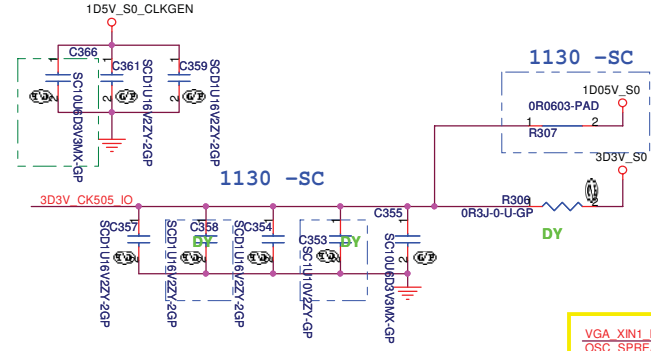
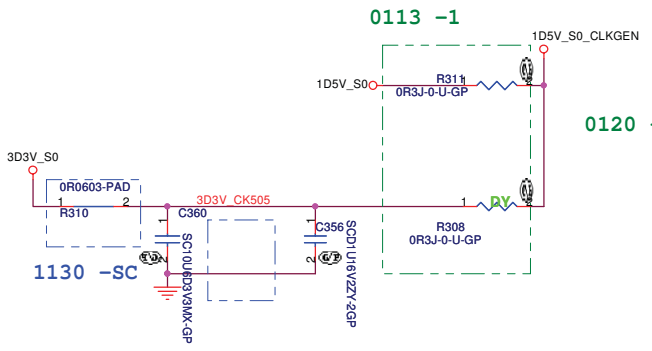
Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1 (HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

PCIE Routing

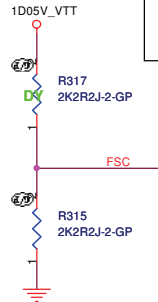
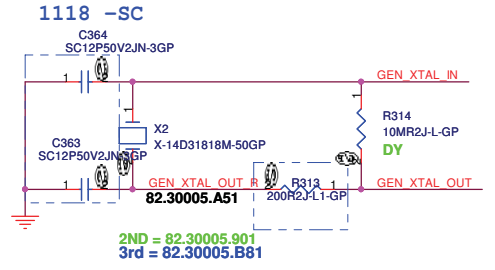
LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

<Variant Name>

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Title			
Table of Content			
Size A3	Document Number HM42-CP	Rev SC	
Date: Friday, January 22, 2010		Sheet 2	of 72



FSC	0	1
SPEED	133MHz (Default)	100MHz



SB 0813 CL = 10pF
Freq tolerance : +/- 30 ppm

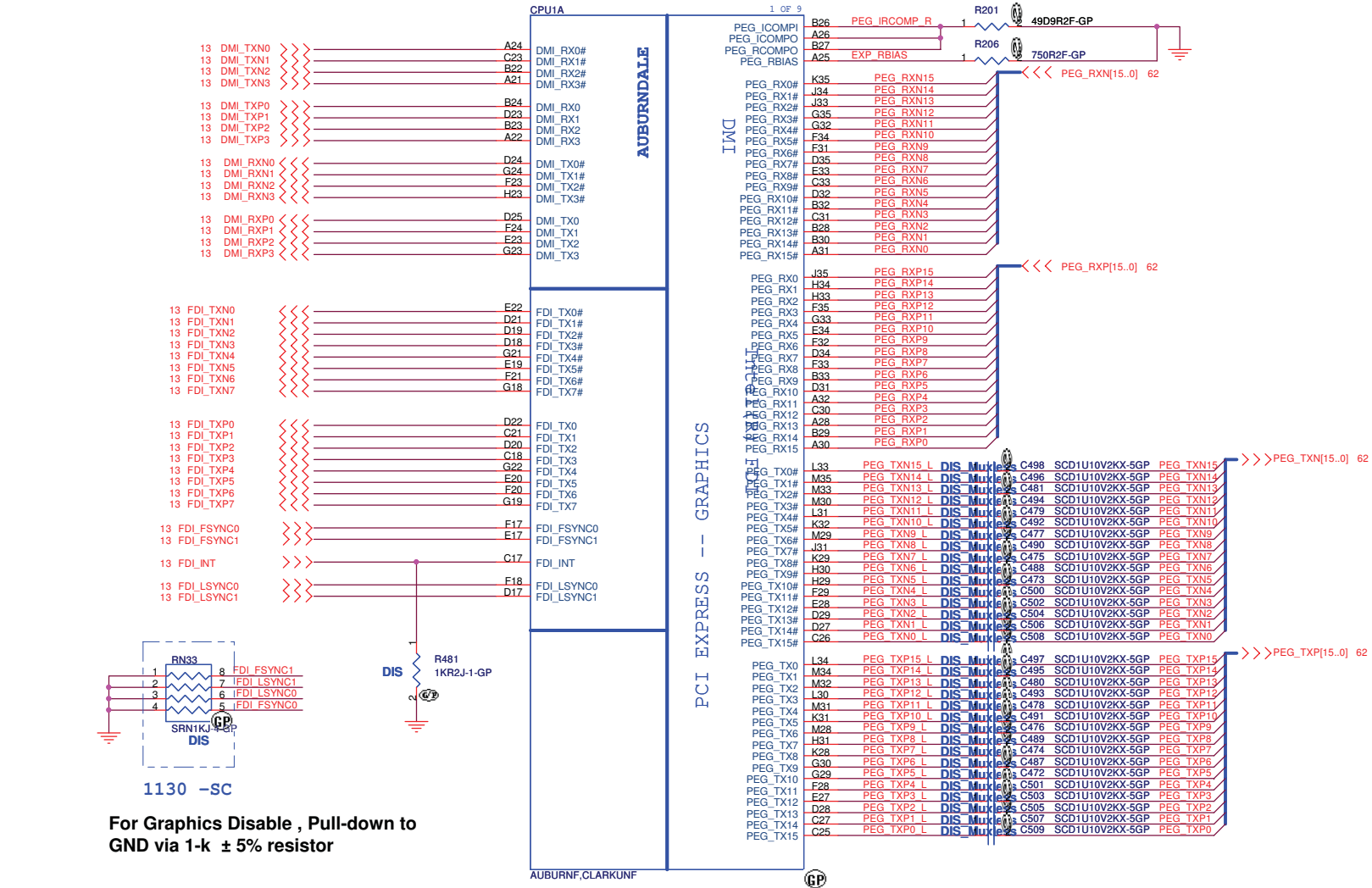
UMA

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Title: **Clock Generator**

Size A3 Document Number: **HM42-CP** Rev: **SC**

Date: Friday, January 22, 2010 Sheet 3 of 72

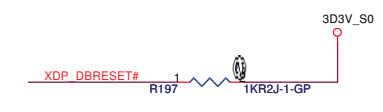
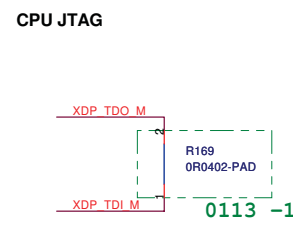
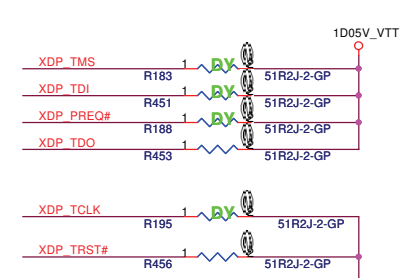
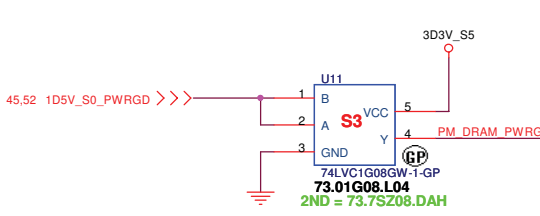
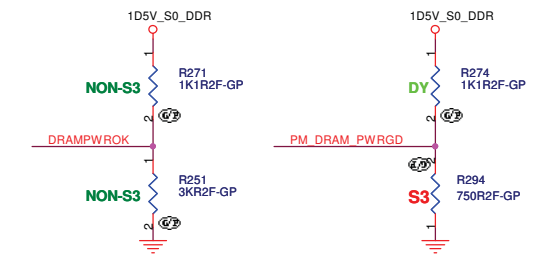
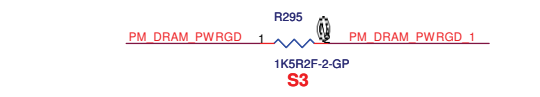
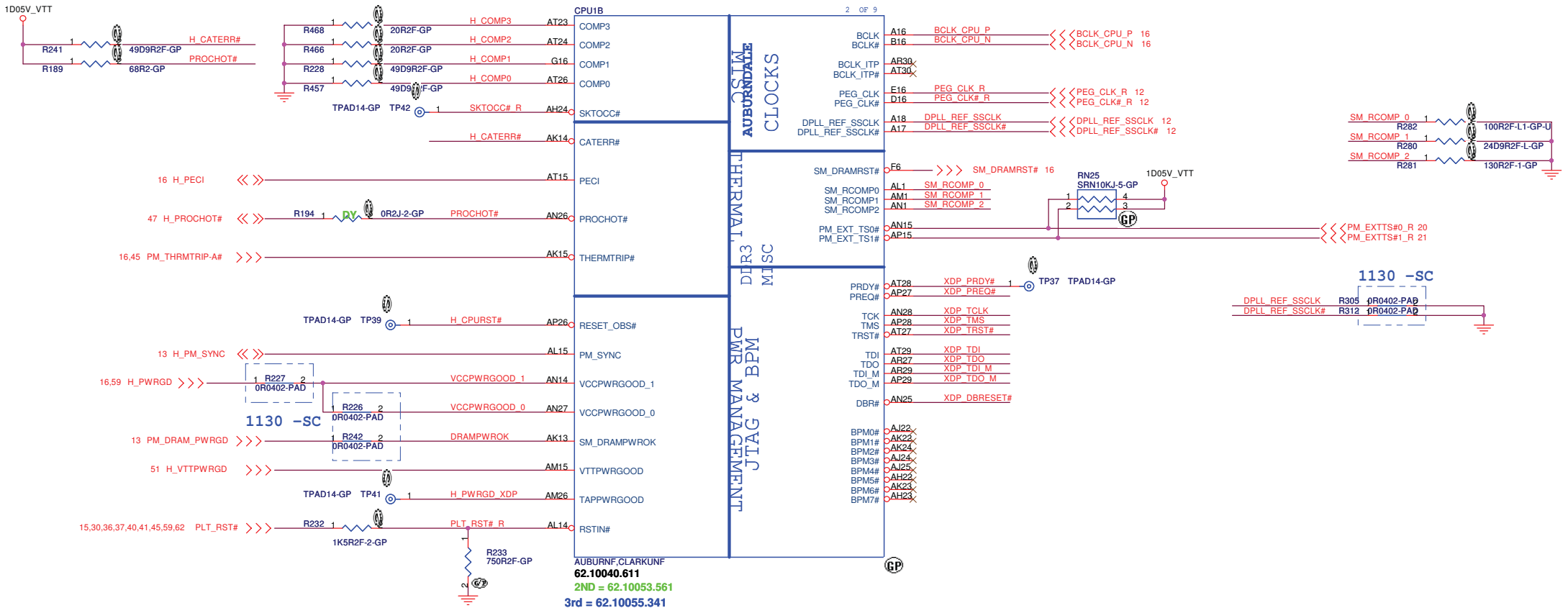


62.10040.611
 2ND = 62.10055.561
 3RD = 62.10055.341
 4th = 62.10055.321

lab stuff 2nd,3rd and 4 th in BOM
 Eng add 1st source (62.10040.611)
 Eng do not stuff 4 th in BOM
 because 4 th have been purge , so stuff 1st in BOM
 but CE said, 4th need stuff in PD if not any concern

0113 -1

del 3rd 62.10055.341 and 4th 62.10055.321
 3rd and 4th have been purged
 CE will confirm SQM if it can add BOM
 CE will release EC to add to BOM



hexainf@hotmail.com
 GRATIS - FOR FREE

UMA

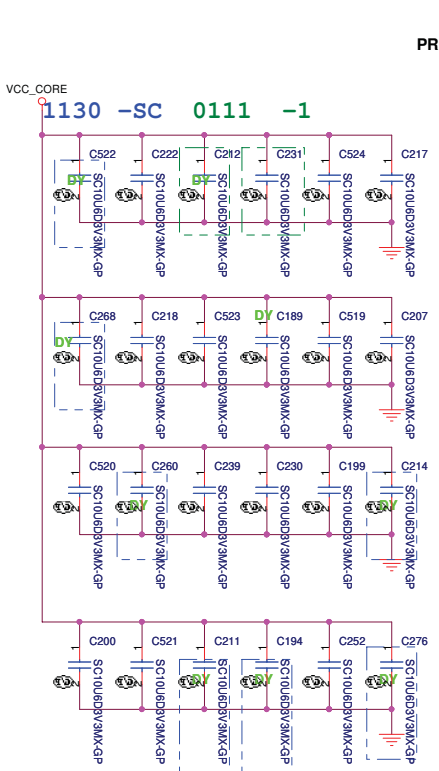
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File

CPU (2/7)

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PROCESSOR CORE POWER

VCC_CORE
48A

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AF26 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- V35 VCC
- V34 VCC
- V33 VCC
- V32 VCC
- V31 VCC
- V30 VCC
- V29 VCC
- V28 VCC
- V27 VCC
- V26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
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- R30 VCC
- P29 VCC
- P28 VCC
- P27 VCC
- P26 VCC

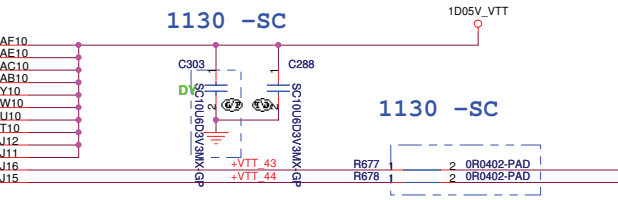
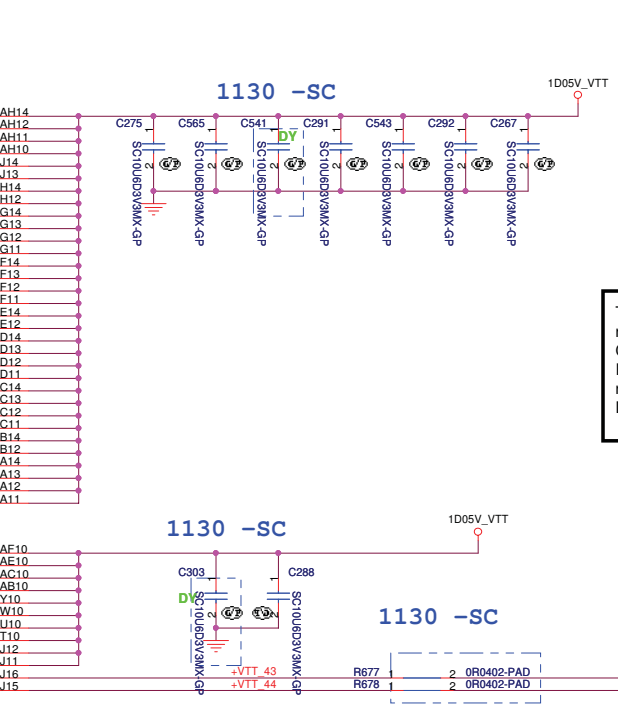
AUBURNDALE

1.1V RAIL POWER

CPU CORE SUPPLY

- VTT0 VCC
- AH14 VCC
- AH12 VCC
- AH11 VCC
- AH10 VCC
- J14 VCC
- J13 VCC
- H14 VCC
- H12 VCC
- G14 VCC
- G13 VCC
- G12 VCC
- F14 VCC
- F13 VCC
- F12 VCC
- F11 VCC
- E14 VCC
- E12 VCC
- D14 VCC
- D13 VCC
- D12 VCC
- D11 VCC
- C14 VCC
- C13 VCC
- C12 VCC
- C11 VCC
- B14 VCC
- B12 VCC
- A14 VCC
- A13 VCC
- A12 VCC
- A11 VCC

- PSI# AN33 >>> PSI# 47
- VID0 AK35 H_VID0 >>> H_VID[6..0] 47
- VID1 AK33 H_VID1 >>> H_VID[6..0] 47
- VID2 AK34 H_VID2 >>> H_VID[6..0] 47
- VID3 AL35 H_VID3 >>> H_VID[6..0] 47
- VID4 AL33 H_VID4 >>> H_VID[6..0] 47
- VID5 AM33 H_VID5 >>> H_VID[6..0] 47
- VID6 AM35 H_VID6 >>> H_VID[6..0] 47
- PROC_DPRSLPVR AM34 >>> PM_DPRSLPVR 47
- VTT_SELECT G15 H_VTTVID1 >>> TP53 TPAD14-GP
- ISENSE AN35 <<< IMVP_MON 47
- VCC_SENSE AJ34 >>> VCC_SENSE 47
- VSS_SENSE AJ35 >>> VSS_SENSE 47
- VTT_SENSE VSS_SENSE_VTT B15 TP_VSS_SENSE_VTT >>> VTT_SENSE 51
- VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT >>> VSS_SENSE 51



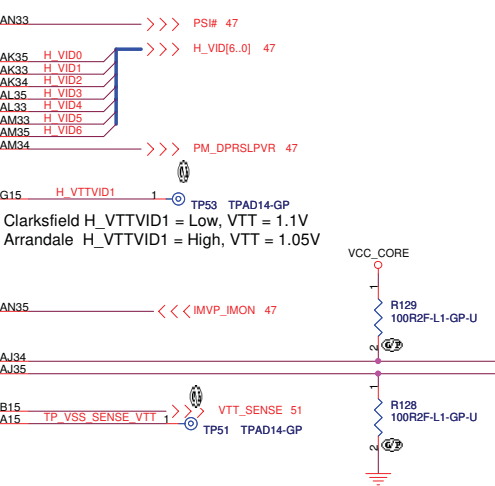
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

POWER

CPU VIDS

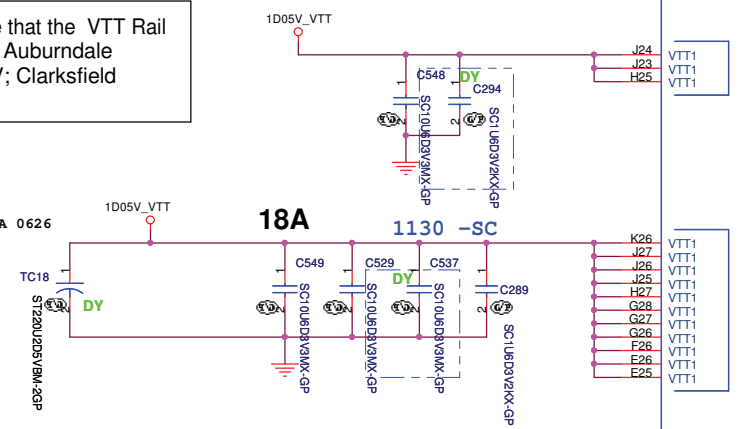
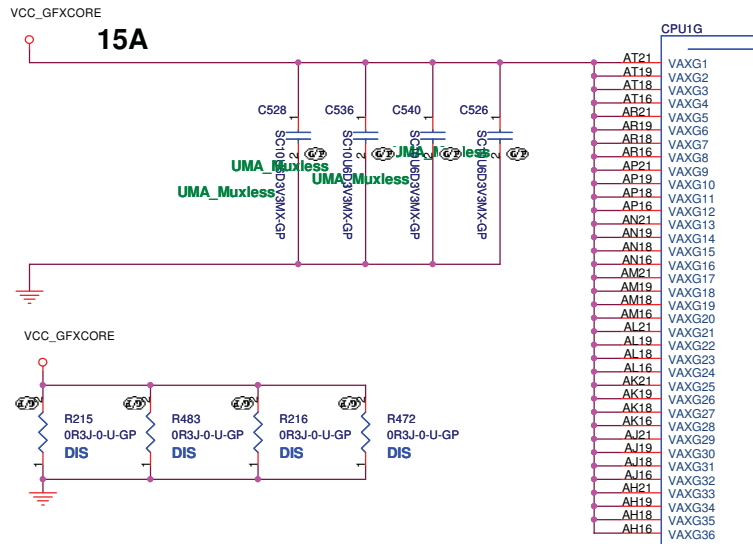
SENSE LINES



Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V

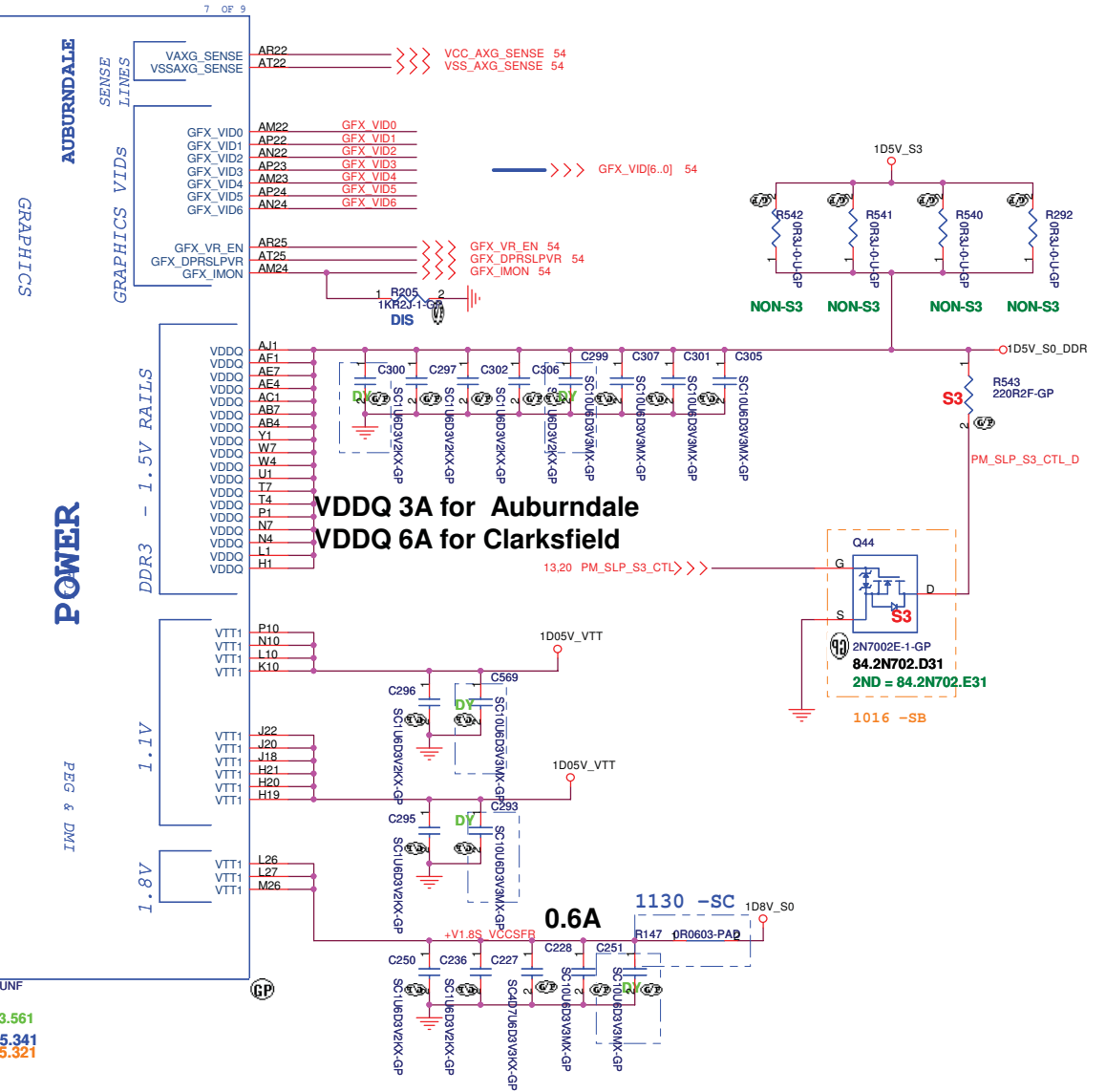
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CPU (4/7)			
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Custom	HM42-CP		
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Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

AUBURN, CLARKUNF
62.10040.611
 2ND = 62.10053.561
 3rd = 62.10055.341
 4th = 62.10055.321



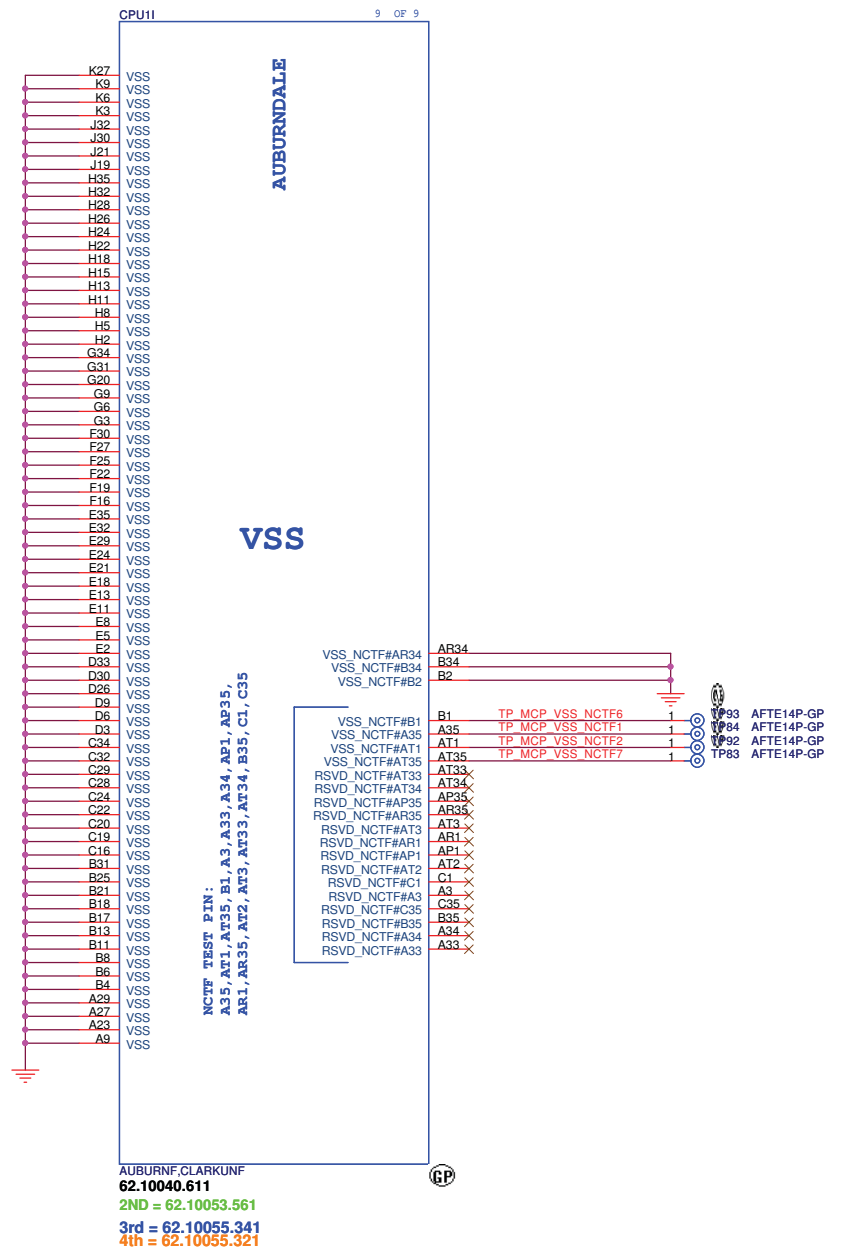
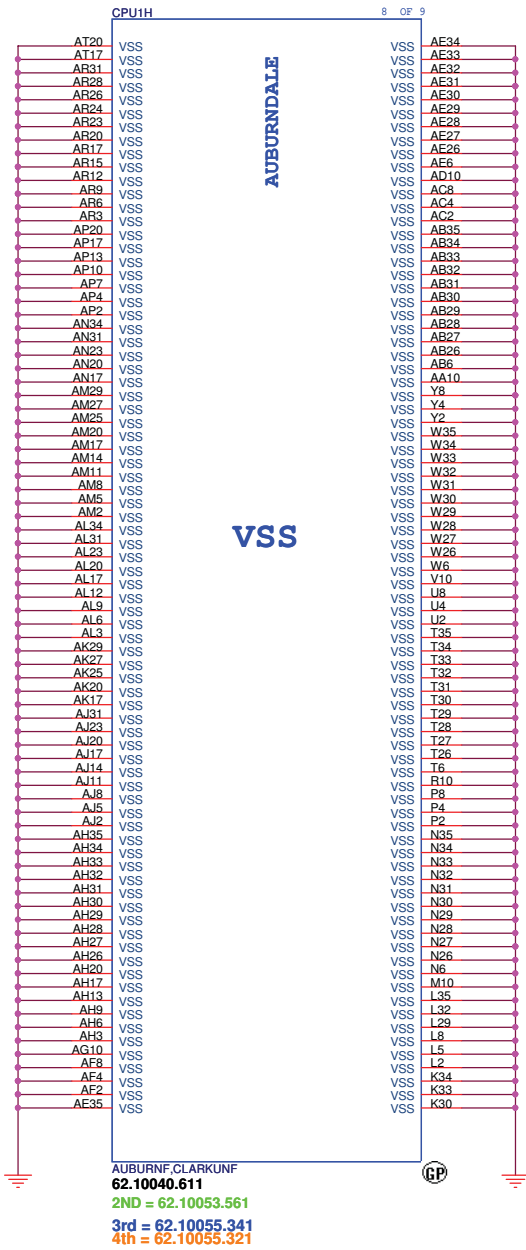
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Title: **CPU (5/7)**

Size A3 Document Number: **HM42-CP** Rev: **SC**

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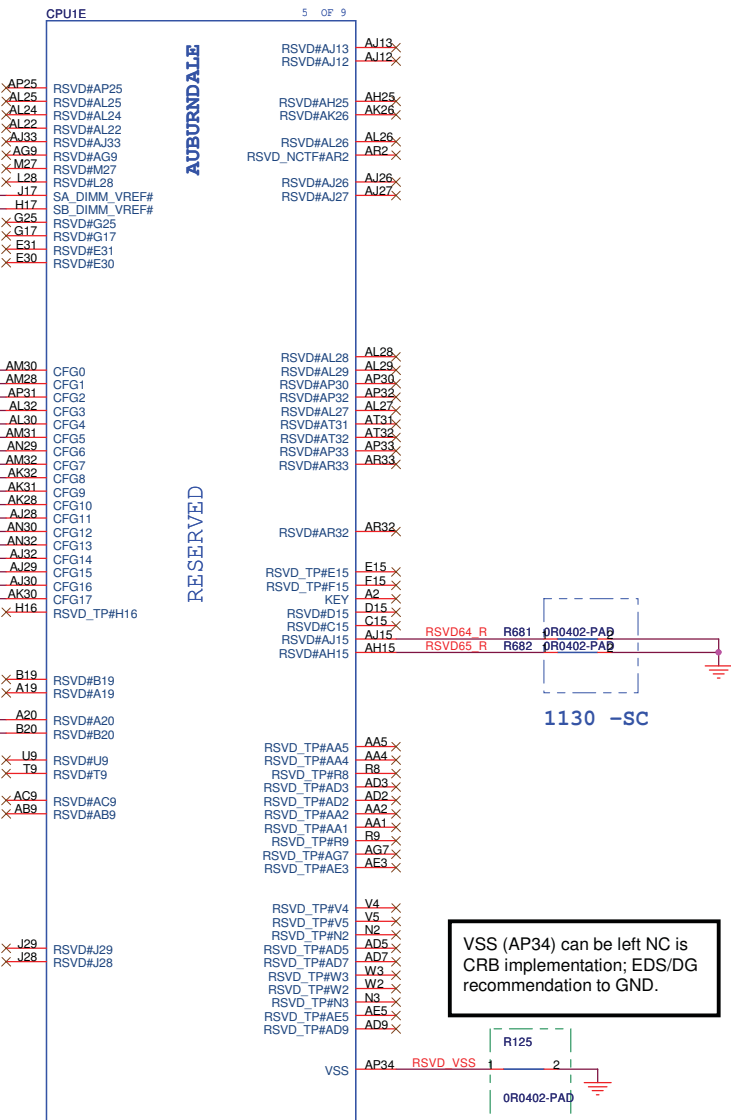
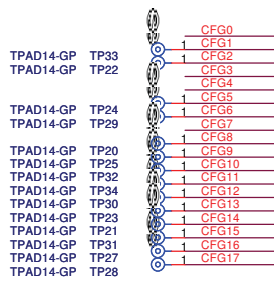
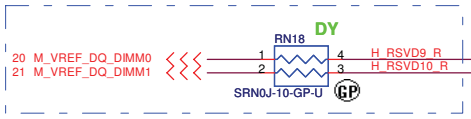
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (6/7)**

Size A3	Document Number HM42-CP	Rev SC
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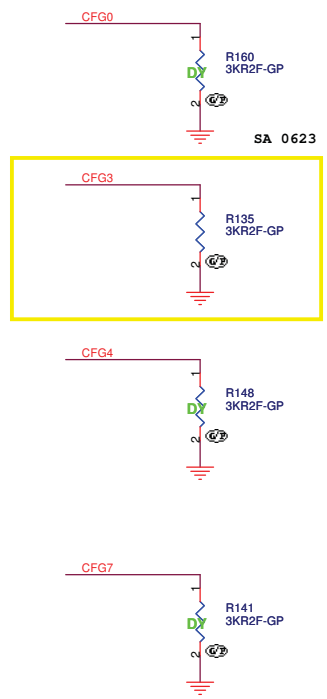
SO-DIMM VREFDQ (M3) Circuit for Clarkfield Processor



AUBURNF.CLARKUNF
62.10040.611
 2ND = 62.10053.561
 3rd = 62.10055.341
 4th = 62.10055.321

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

Processor Strapping

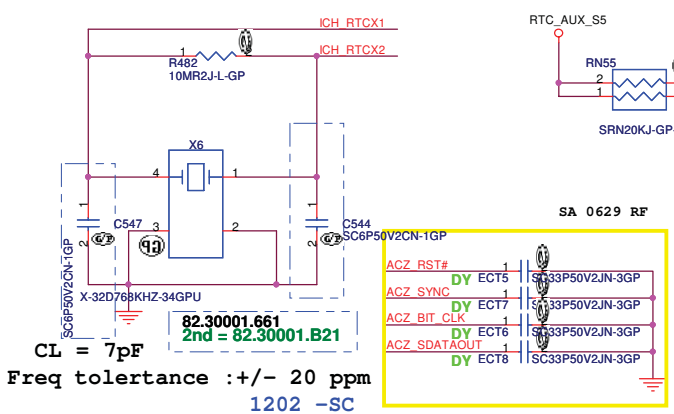


PCI-Express Configuration Select	
CFG0	1:Single PEG(Default) 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation(Default) 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

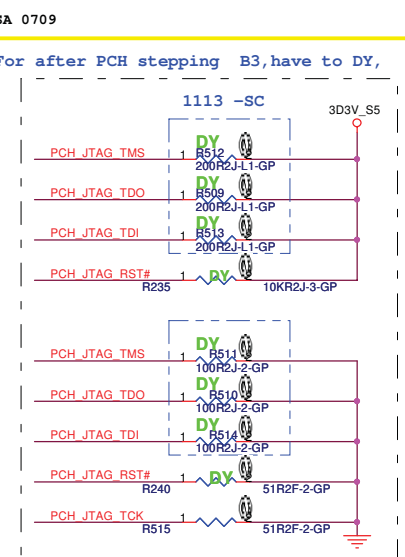
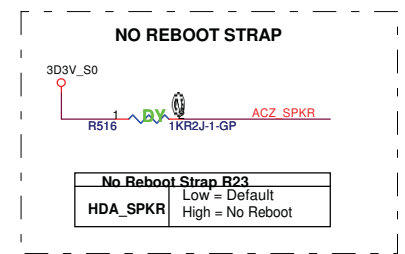
CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (Default) 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarkfield samples.	
CFG7	Clarkfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

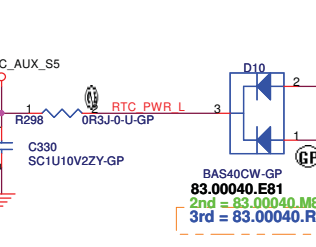
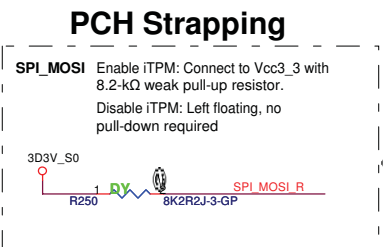
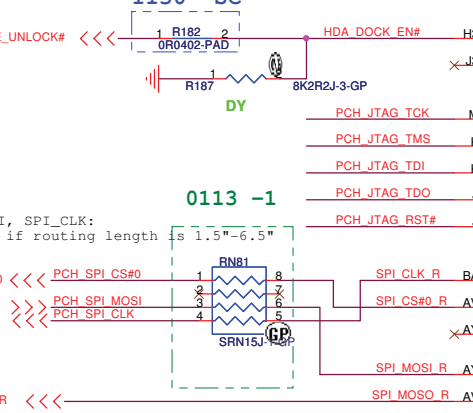
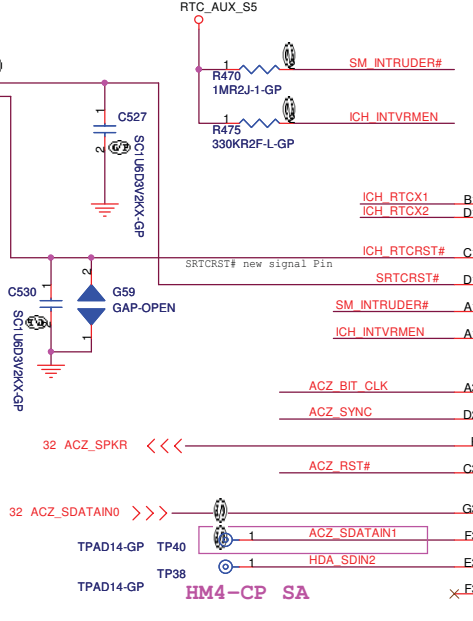


32 ACZ_RST#_AUDIO
 32 ACZ_SYNC_AUDIO
 32 ACZ_BITCLK_AUDIO
 32 ACZ_SDATAOUT_AUDIO

SIV fail when stuff 10-ohm,
 fine tune 33-ohm for solving
 33-ohm is required for intel recommend,
 real value base on fine tune result

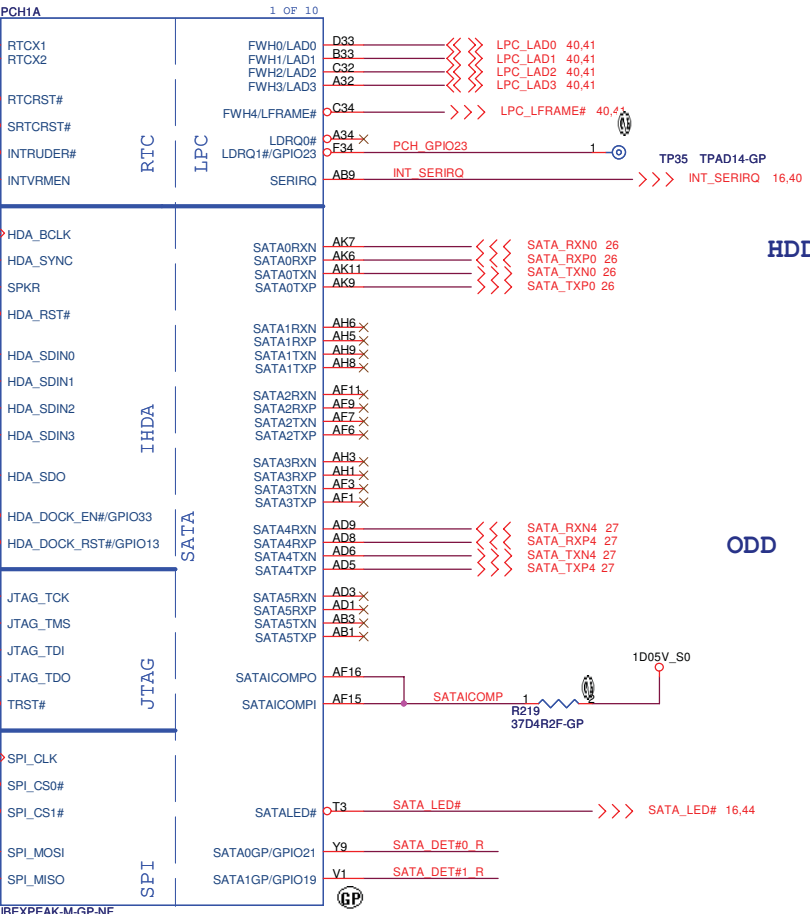


hexwin@hotmail.com
 GRATIS - FOR FREE



INTVRMEN- Integrated SUS
 1.1V VRM Enable
 High - Enable internal VRs

Integrated VccSus1_05, VccSus1_5, VccCl1_5
INTVRMEN High=Enable Low=Disable
Integrated VccLan1_05VccCl1_05
LAN100_SLP High=Enable Low=Disable



PCH 1 stuff 71.0IBEX.G0U

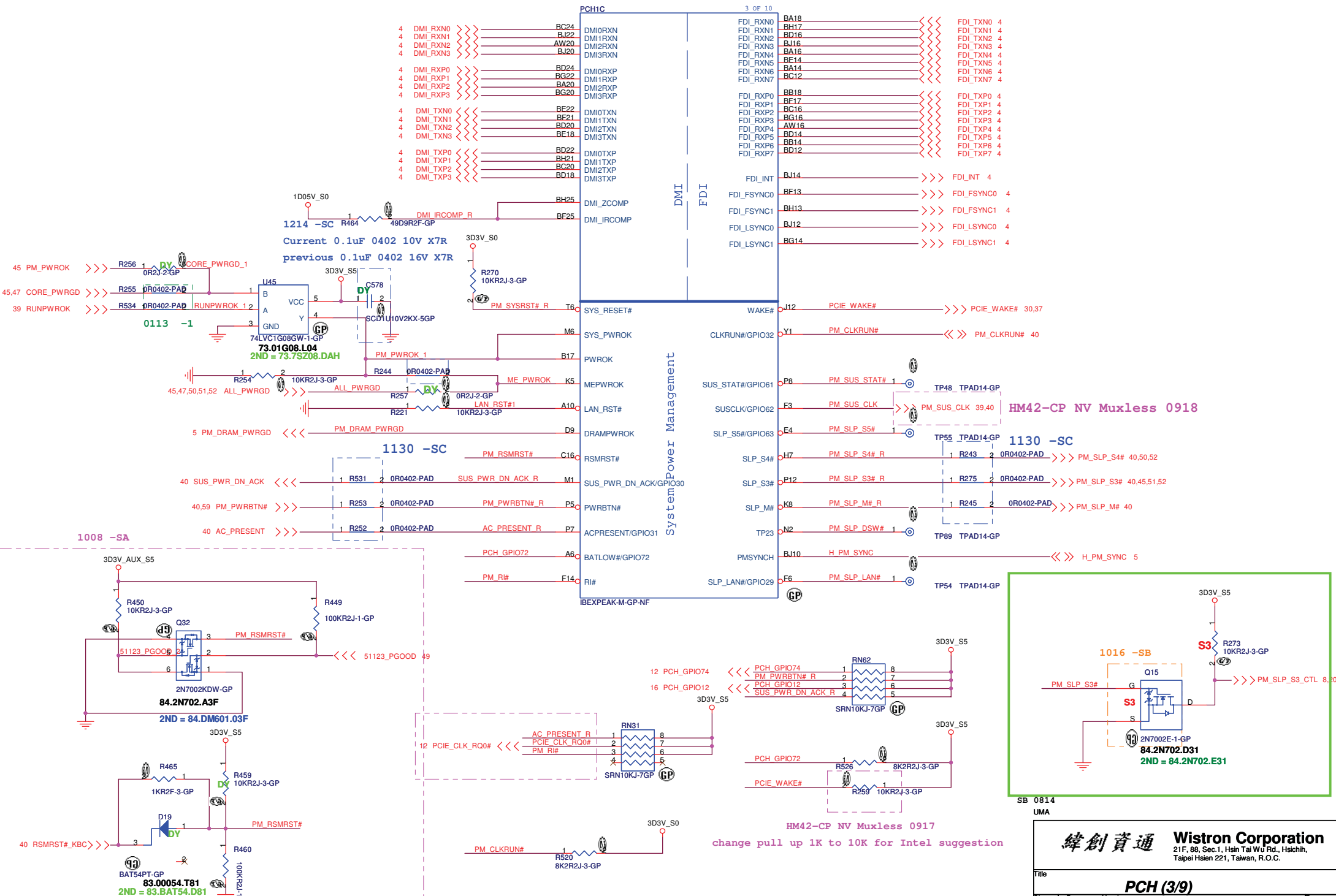
83.00040.Q81 is ROHS parts
 83.00040.R81 is Halogens free Part
 arrange qual in Eng SKU

1130 -SC
 0113 -1

20.F1035.002
 2nd = 20.F0772.002
 3rd = 21.D0300.102
 4th = 20.F1729.002

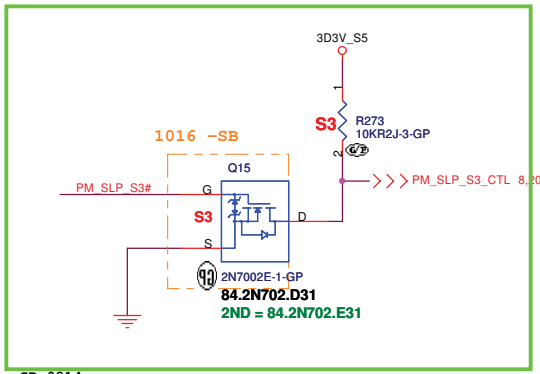
UMA

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HM42-CP NV Muxless 0917
change pull up 1K to 10K for Intel suggestion



SB 0814
UMA

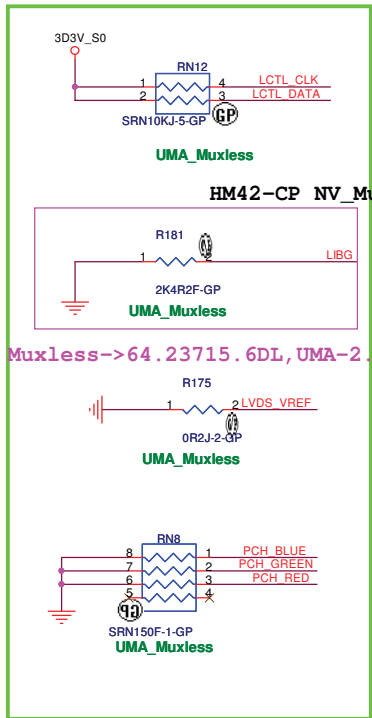
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (3/9)**

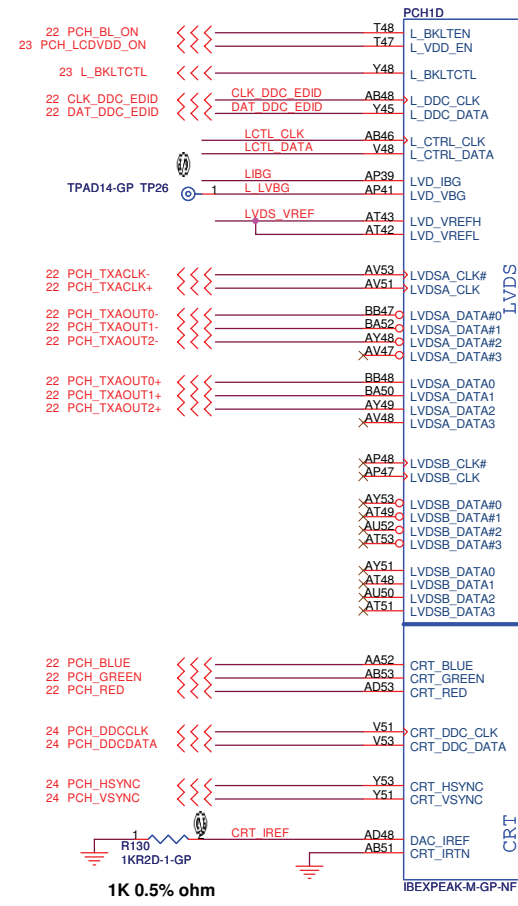
Size A3 Document Number: **HM42-CP**

Date: Friday, January 22, 2010 Sheet 13 of 72

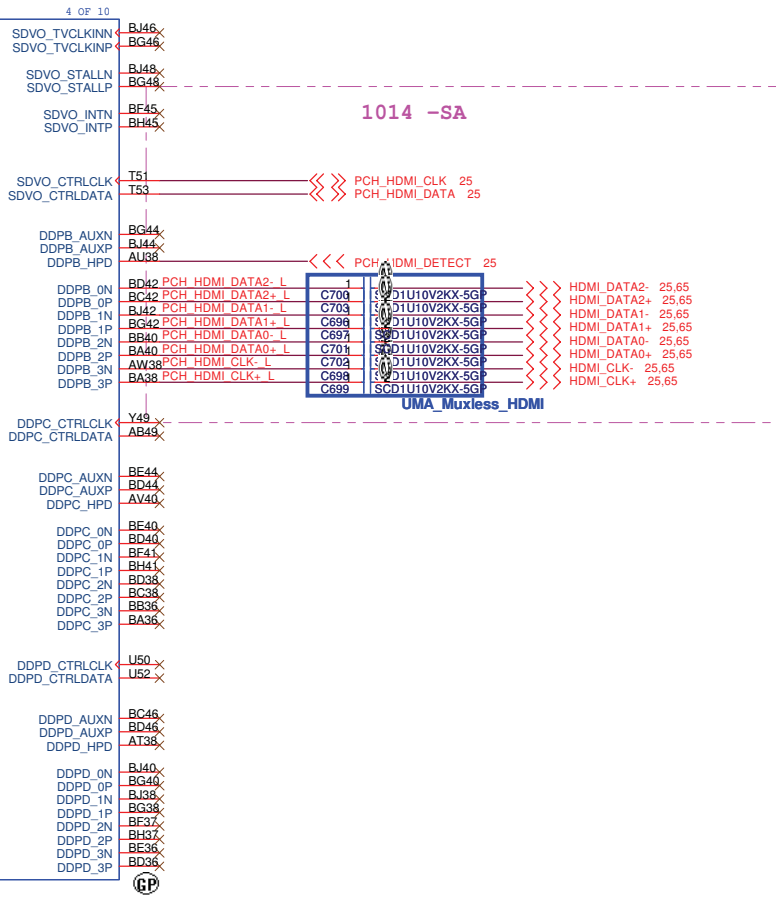
Rev: **SC**



SB 0811



Digital Display Interface



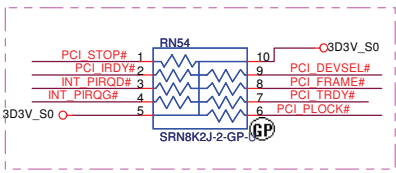
<Core Design>

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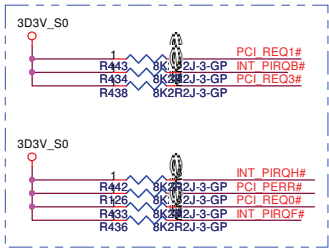
Title: **PCH (4/9)**

Size A3 Document Number **HM42-CP** Rev **SC**

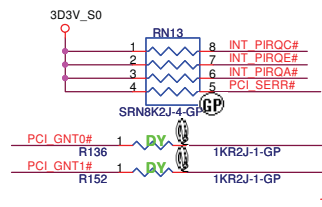
Date: Friday, January 22, 2010 Sheet 14 of 72



HM42 NV Muxless SA 0925
1209 -SC



HM42 NV Muxless SA 0924

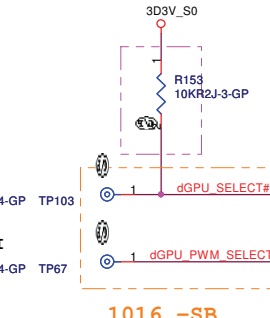


PCH strapping

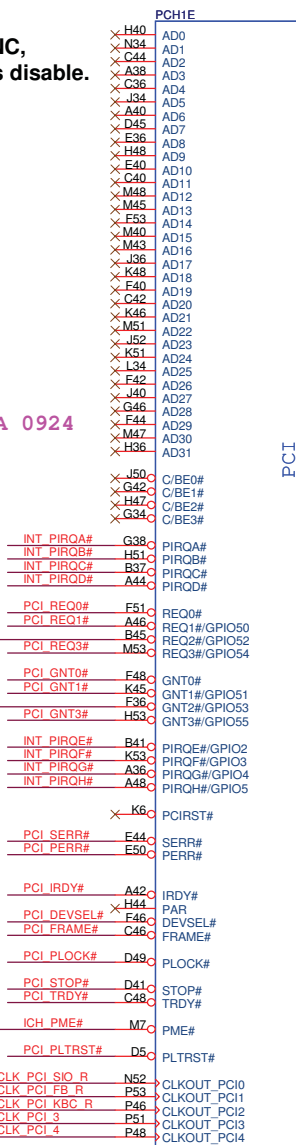
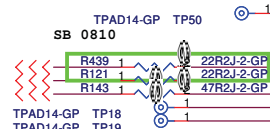
BOOT BIOS Strap		
GNT#0	GNT#1	BOOT BIOS Location
0	0	LPC
1	0	Reserved
floating	0	PCI
floating	floating	SPI (Default)

PCI_GNT#1	Default
1	Default (internal pull up)
0	Configures DMI for ESI compatible operation (Not for Mobile platform)

- 41 PCLK_FWH
- 12 CLK_PCI_FB
- 40 CLK_PCI_KBC



1016 -SB



These pins are left as NC,
because the function is disable.

These pins are left as NC,
because the function is disable.

PCH strapping

NV_CLE	DMI termination voltage
floating	internal pull-up

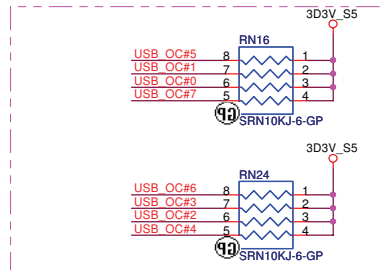
NV_ALE	Enable Anti-Theft Tech
1	Disable (internal pull down)

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

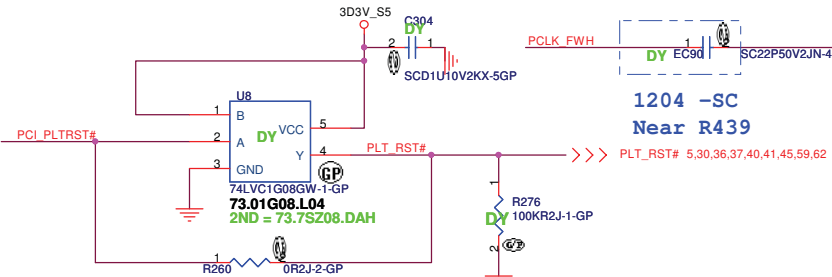
USB

Pair	Device
0	USB3
1	USB2
2	NC
3	MINICARD1 (WLAN)
4	WECAM
5	NC
6	NC
7	NC
8	3G SIM Card
9	USB1 (HS)
10	NC
11	Blue Tooth
12	MINIC2 (3G)
13	Cardreader

-SA 1001
HM42-CP SA



1006 -SA swap net



1204 -SC
Near R439

PCH strapping

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

<Variant Name>

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Title: PCH (5/9)

Size A3 Document Number: HM42-CP Rev: SC

Date: Friday, January 22, 2010 Sheet 15 of 72

GPIO8 has a weak[20K] internal pull down.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.

HM42-CP_NV_Muxless SA

62 DGPU_HOLD_RST# >>> DGPU_HOLD_RST#
55,61,62 DGPU_PWROK >>> DGPU_PWROK

TPAD14-GP TP36 <<<< EC_HDMI#
TPAD14-GP TP36 <<<< EC_SCI#
TPAD14-GP TP36 <<<< EC_SWI#
TPAD14-GP TP46 <<<< PCH_GPIO24
TPAD14-GP TP45 <<<< PCH_GPIO27
TPAD14-GP TP56 <<<< PCH_GPIO28

61 DGPU_PWR_EN# <<<< DGPU_PWR_EN#
1016 -SB <<<< PCH_GPIO39

SB 0814 <<<< RST_GATE
11 PCH_GPIO48 <<<< PCH_GPIO48

TPAD14-GP TP105 <<<< dGPU_EDID

SB 0819 <<<< PCH_GPIO45

SB 0814 <<<< PCH_GPIO15

PSW_CLR# <<<< PSW_CLR#

11,44 SATA_LED# <<<< SATA_LED#
11,40 INT_SERIRQ <<<< INT_SERIRQ

STP_PCI# <<<< STP_PCI#
PCH_GPIO22 <<<< PCH_GPIO22
PCH_GPIO28 <<<< PCH_GPIO28
dGPU_EDID <<<< dGPU_EDID

PCH_GPIO35 <<<< PCH_GPIO35

SB 0722 <<<< PCH_TP95
SB 0722 <<<< PCH_TP96
SB 0722 <<<< PCH_TP97
SB 0722 <<<< PCH_TP98

11,44 SATA_LED# <<<< SATA_LED#
11,40 INT_SERIRQ <<<< INT_SERIRQ

STP_PCI# <<<< STP_PCI#
PCH_GPIO22 <<<< PCH_GPIO22
PCH_GPIO28 <<<< PCH_GPIO28
dGPU_EDID <<<< dGPU_EDID

PCH_GPIO35 <<<< PCH_GPIO35

SB 0812 <<<< DIS_UMA

SB 0812 <<<< DGPU_HOLD_RST#

SB 0812 <<<< DGPU_PWR_EN#

SB 0812 <<<< DIS_UMA

SB 0812 <<<< DGPU_HOLD_RST#

SB 0812 <<<< DGPU_PWR_EN#

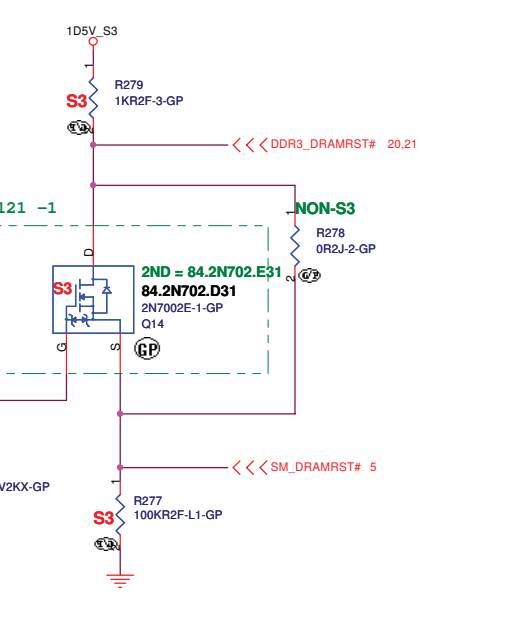
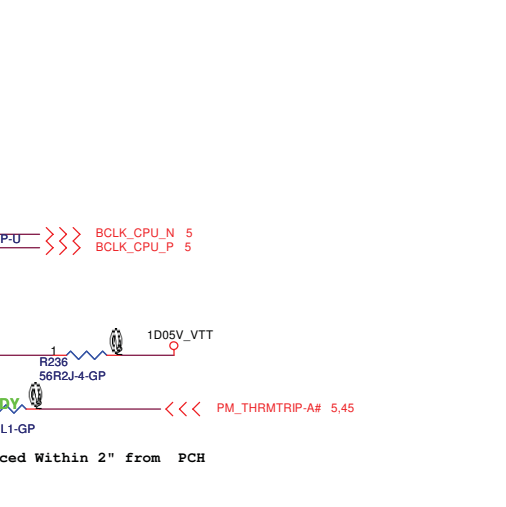
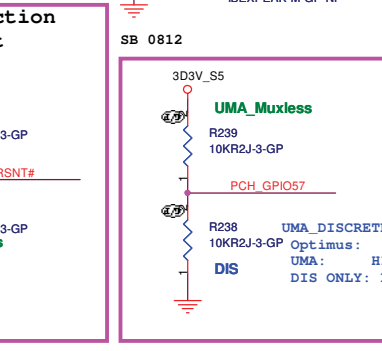
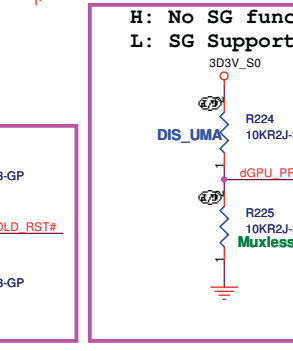
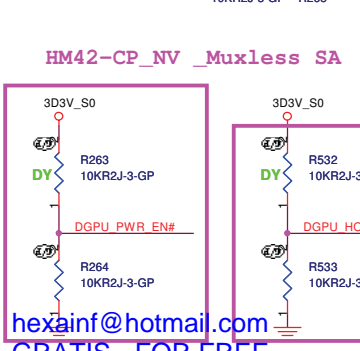
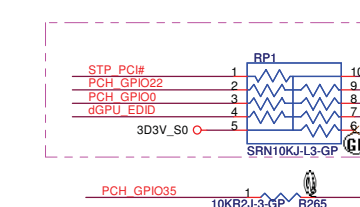
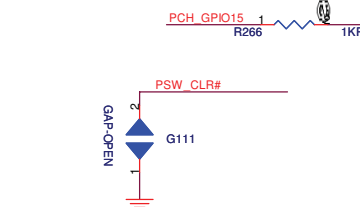
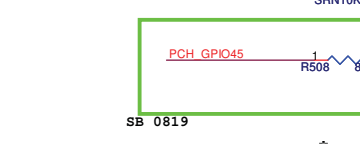
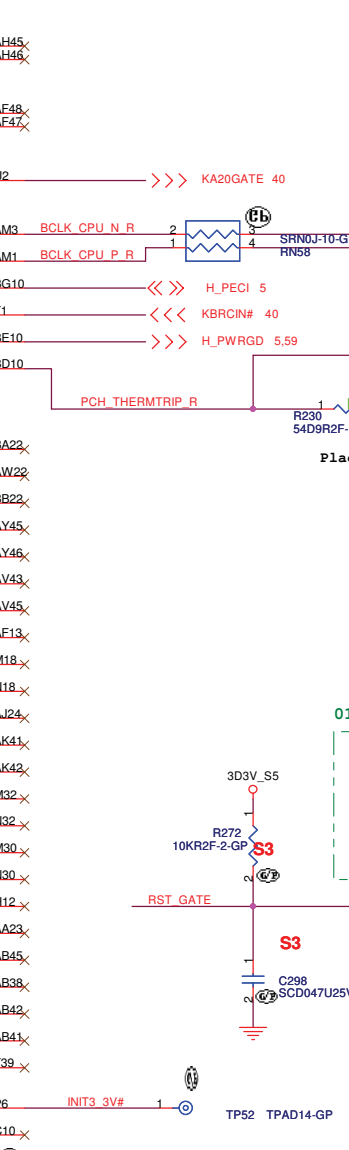
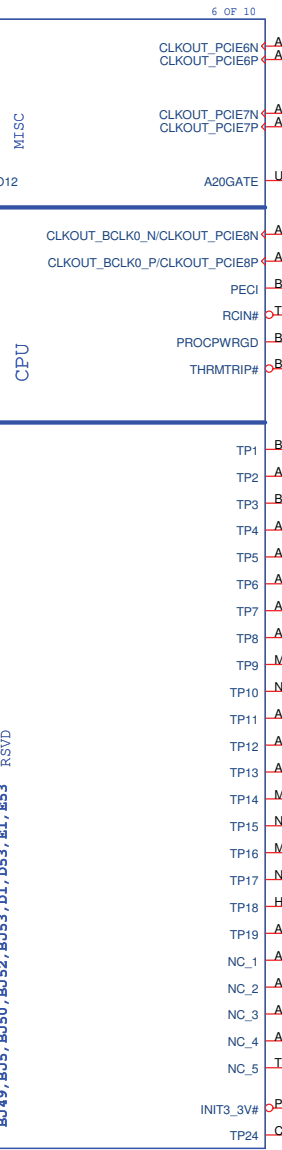
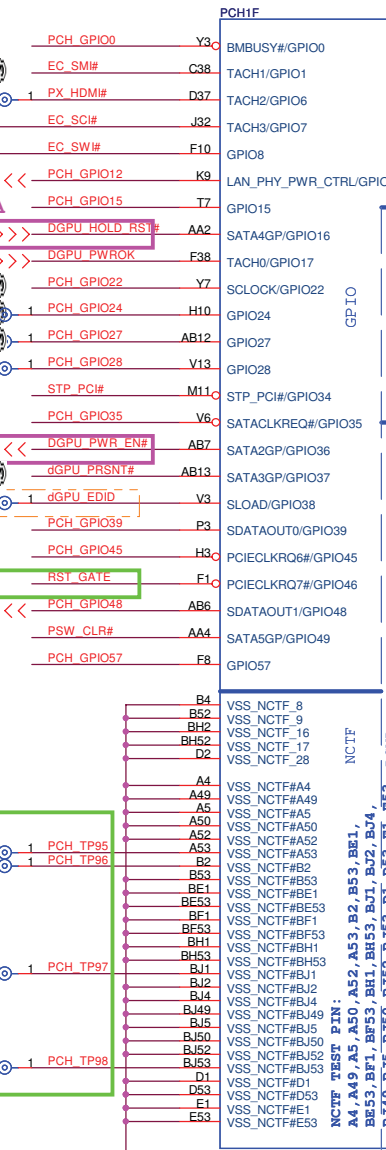
SB 0812 <<<< DIS_UMA

SB 0812 <<<< DGPU_HOLD_RST#

SB 0812 <<<< DGPU_PWR_EN#

SB 0812 <<<< DIS_UMA

SB 0812 <<<< DGPU_HOLD_RST#

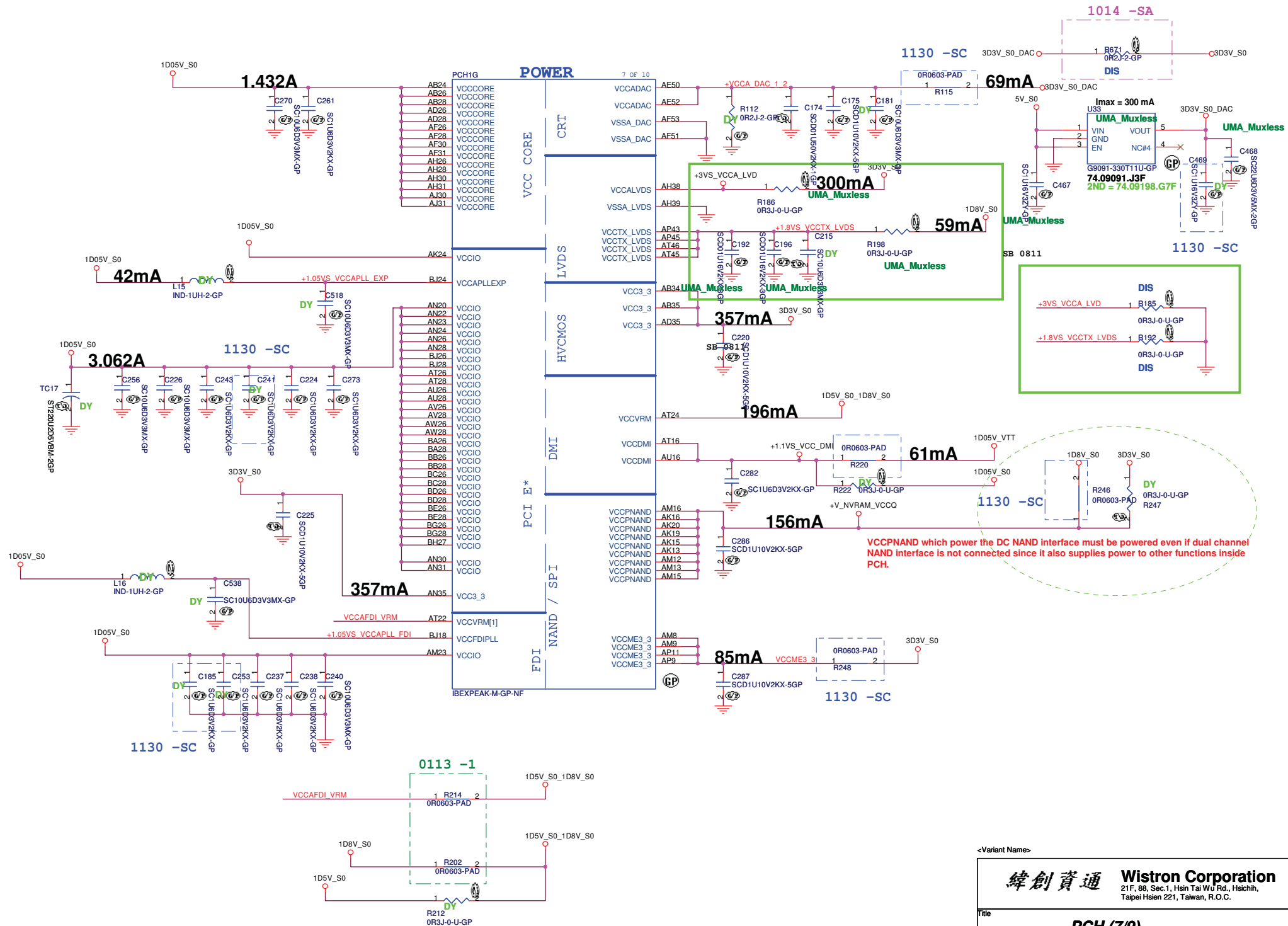


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Title: **PCH (6/9)**
 Size: A3
 Document Number: **HM42-CP**
 Date: Friday, January 22, 2010
 Sheet: 16 of 72

Rev: **SC**



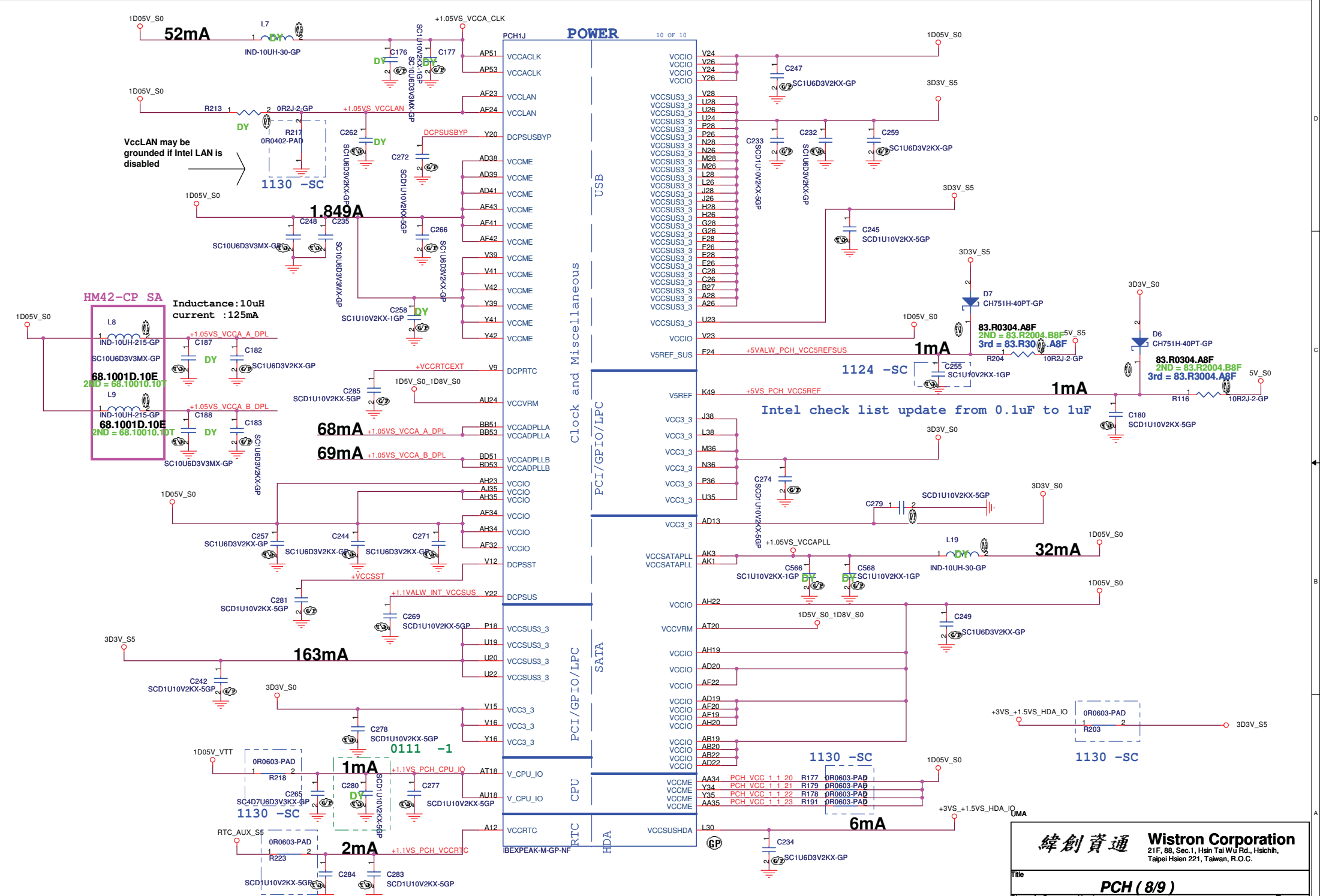
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Title: **PCH (7/9)**

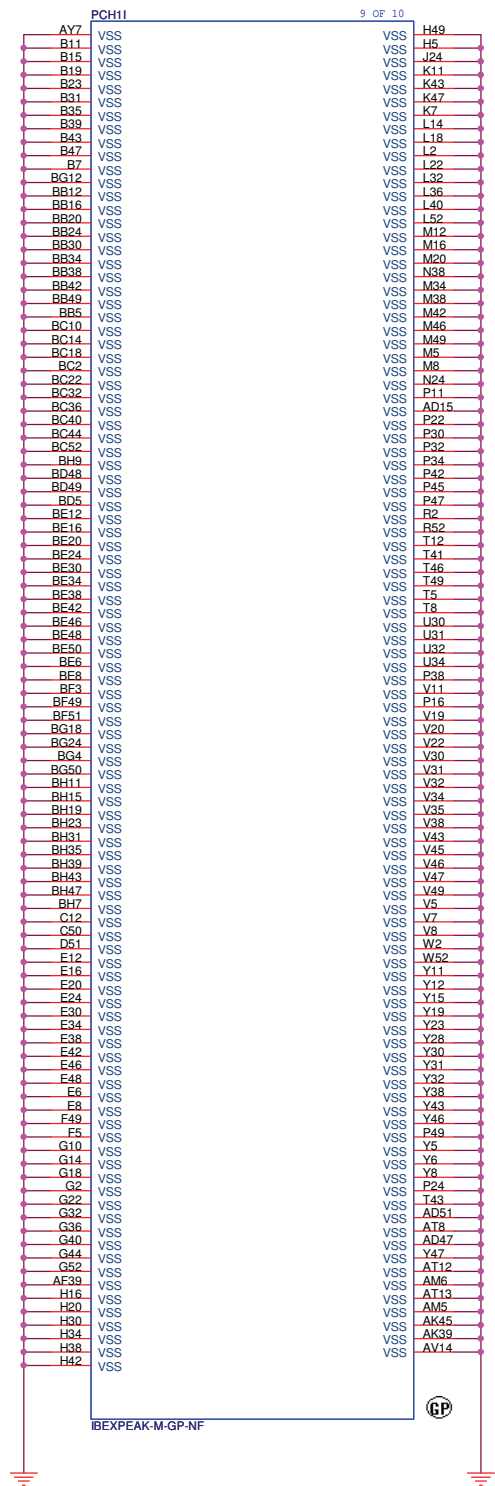
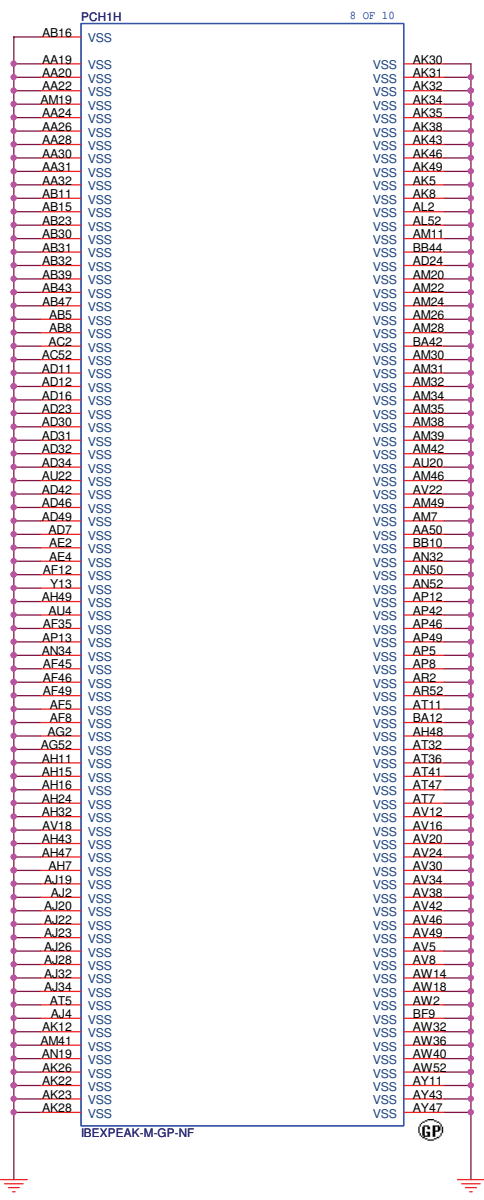
Size A3 Document Number: **HM42-CP** Rev: **SC**

Date: Friday, January 22, 2010 Sheet 17 of 72



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Title	
PCH (8/9)	
Size	Document Number
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18	72

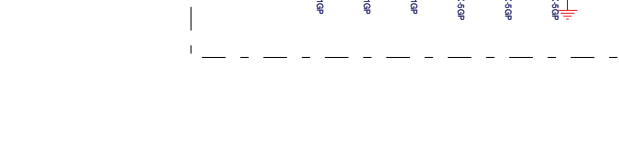
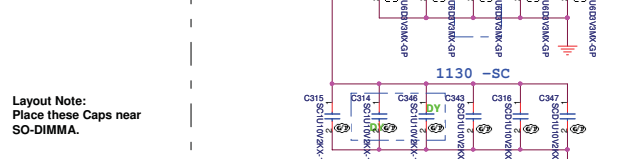
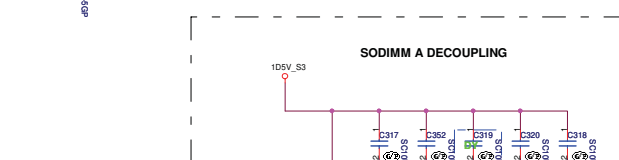
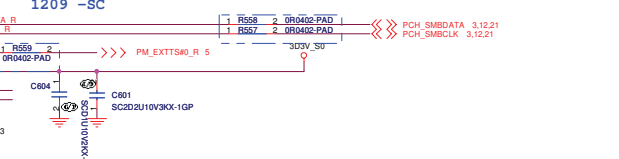
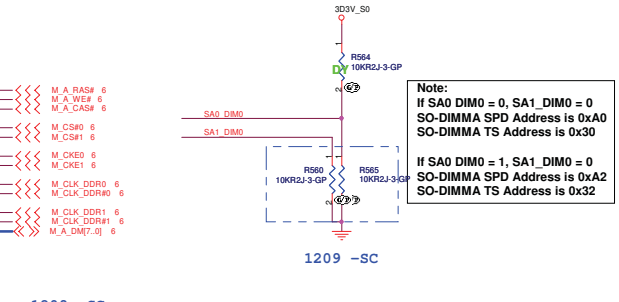
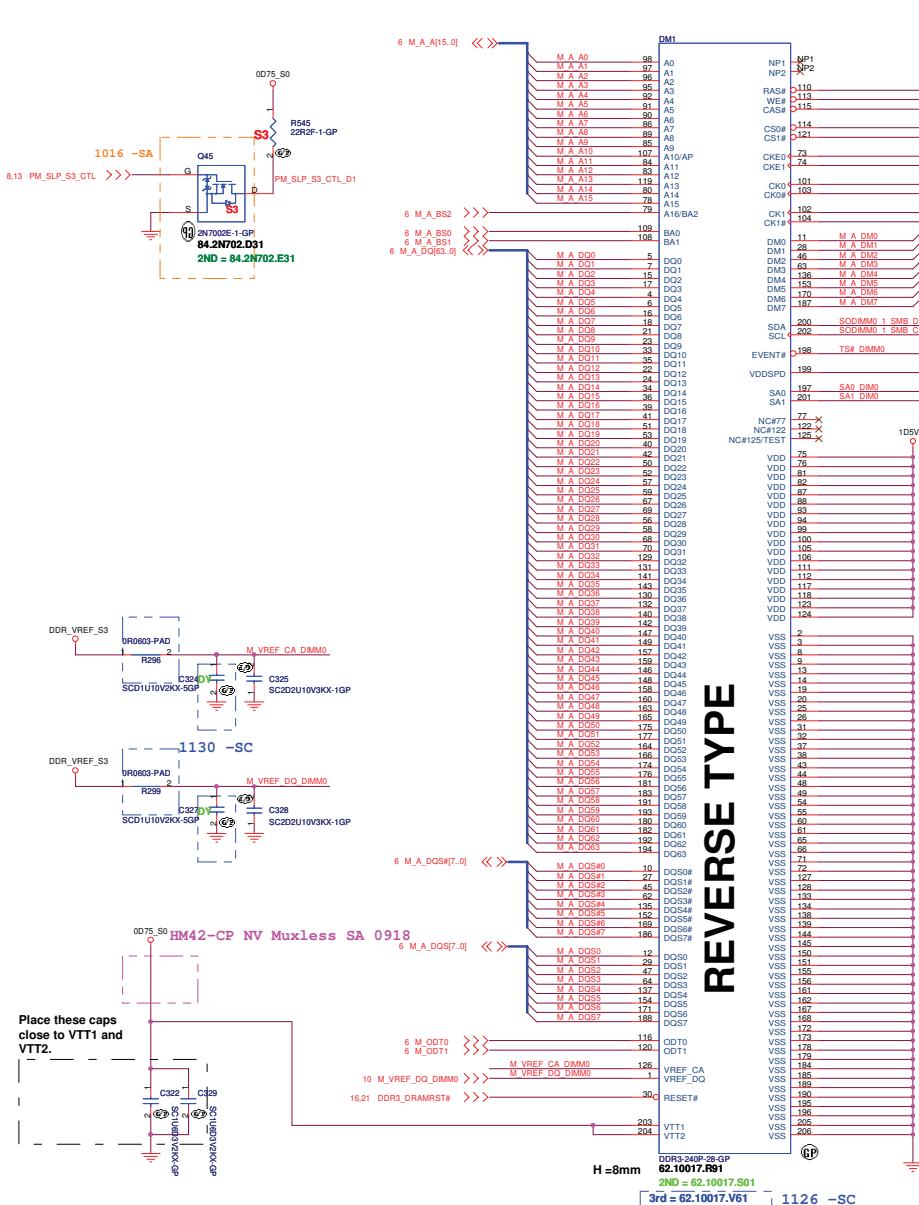


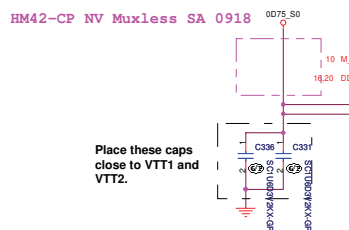
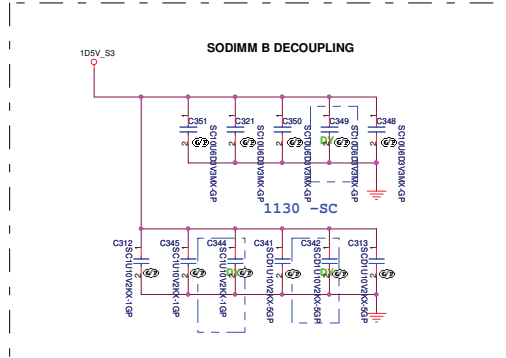
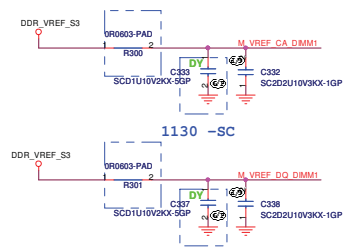
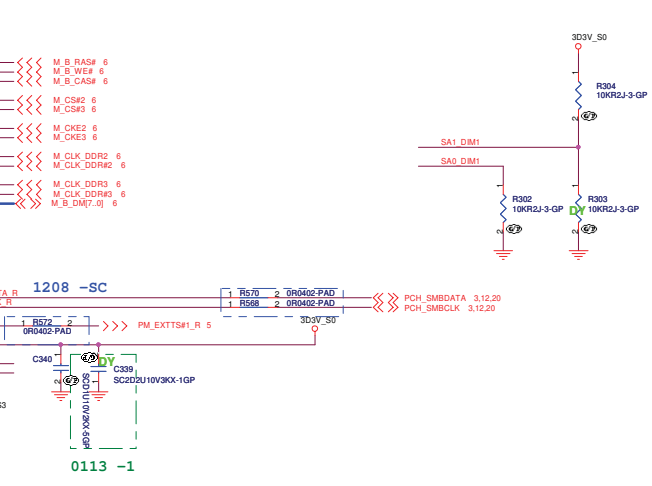
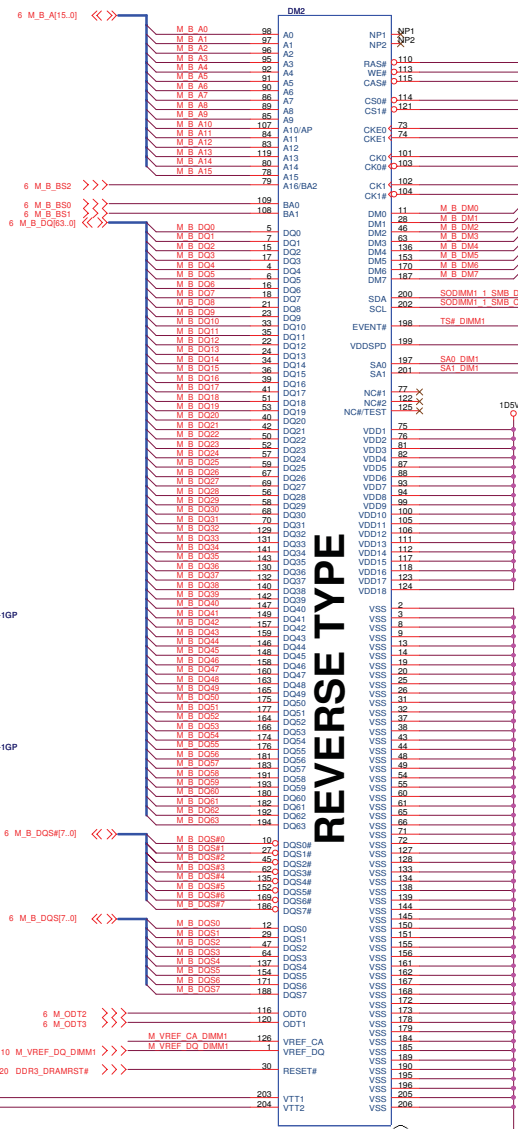
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Title: **PCH (9/9)**

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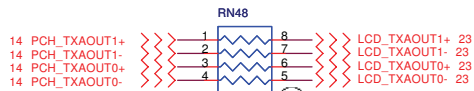




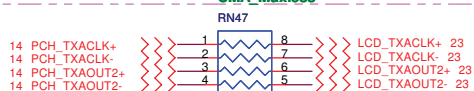
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

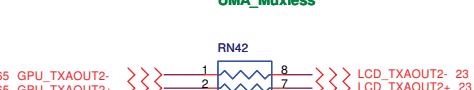
1st and 2nd change
1st: 20.F115.204 and 2nd: 20.F1207.204
(use in lab stage)



SRNOJ-7-GP
UMA_Muxless



SRNOJ-7-GP
UMA_Muxless

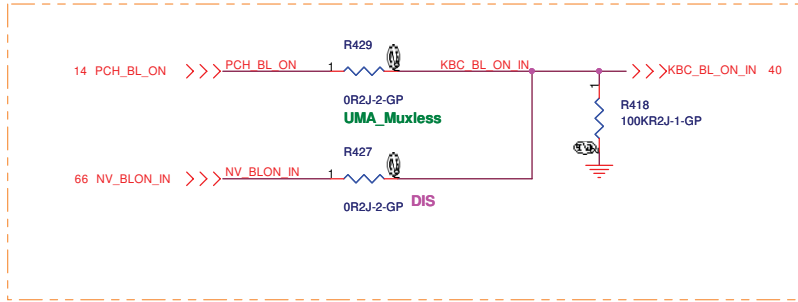


SRNOJ-7-GP
DIS



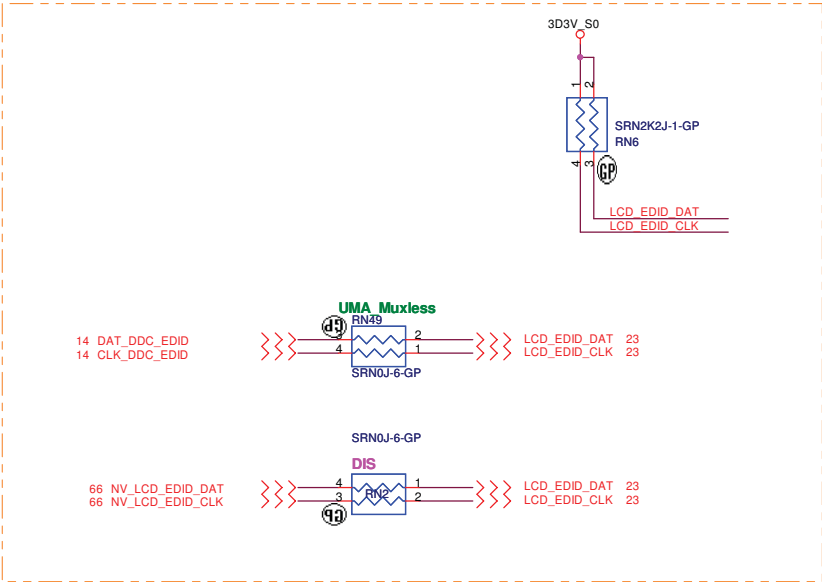
SRNOJ-7-GP
DIS

1016 -SB

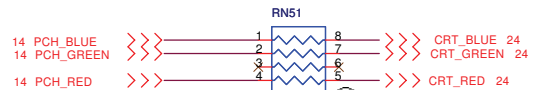


0R2J-2-GP
UMA_Muxless

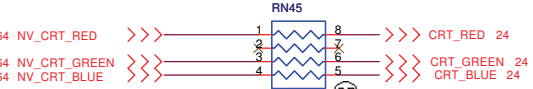
0R2J-2-GP
DIS



1016 -SB

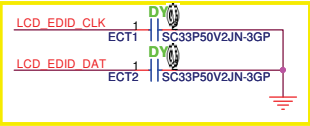
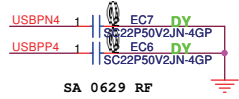


SRNOJ-7-GP
UMA_Muxless

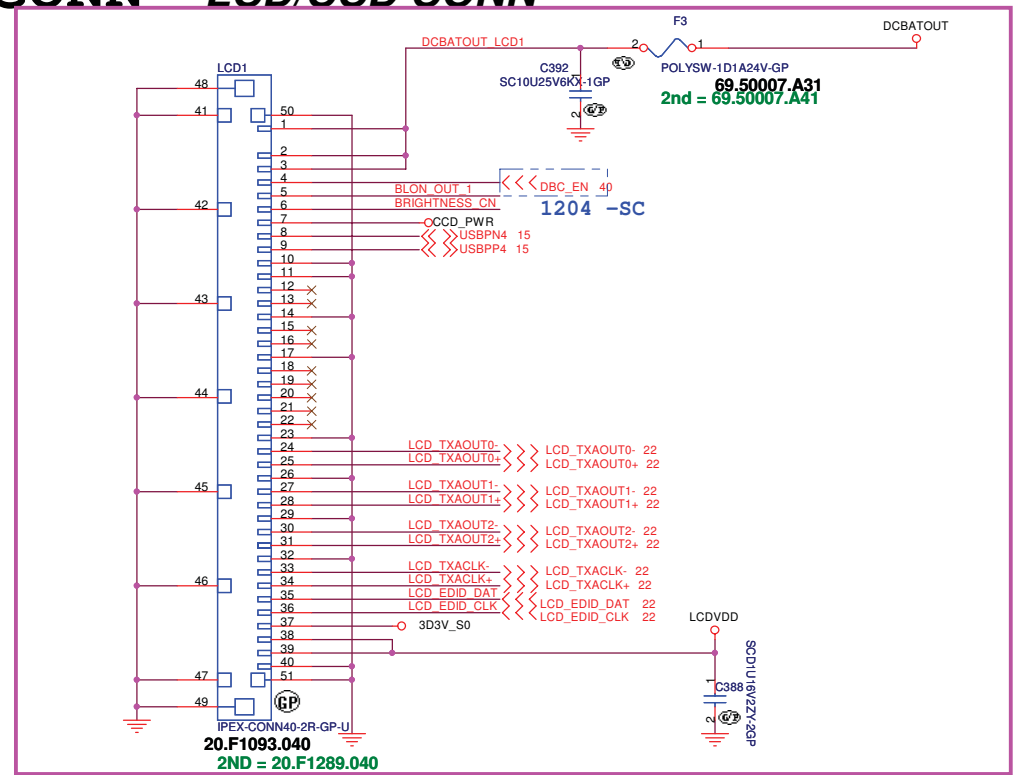
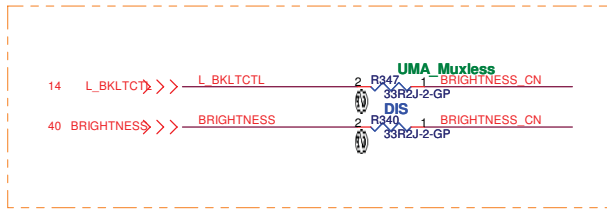


SRNOJ-7-GP
DIS

LCD/INVERTER/CCD CONN LCD/CCD CONN

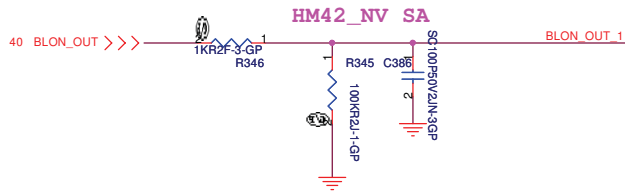


1016 -SB

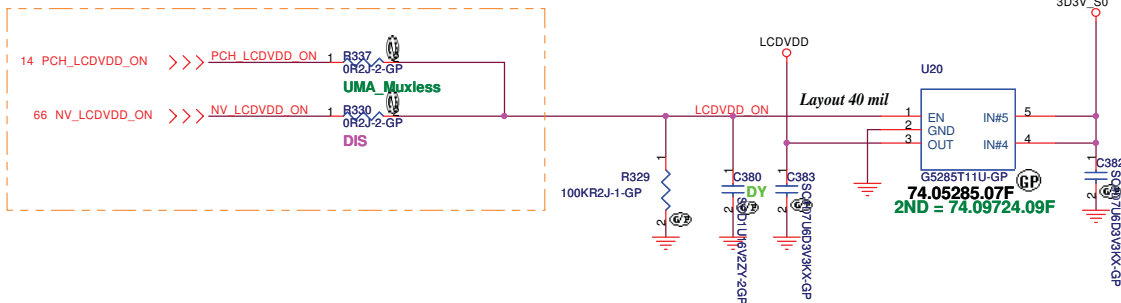


1005 -SA

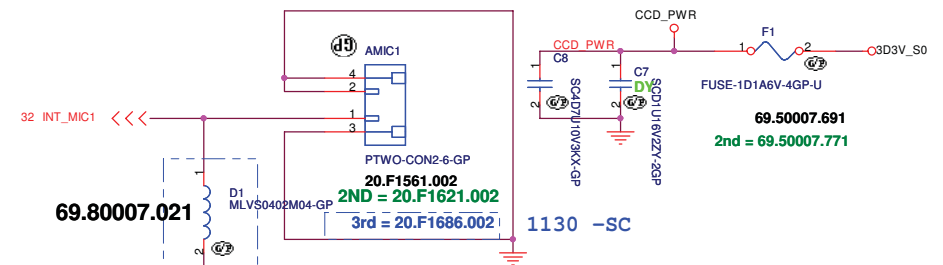
define same as SJM50-PU, can use SJM50 Cable



1016 -SB



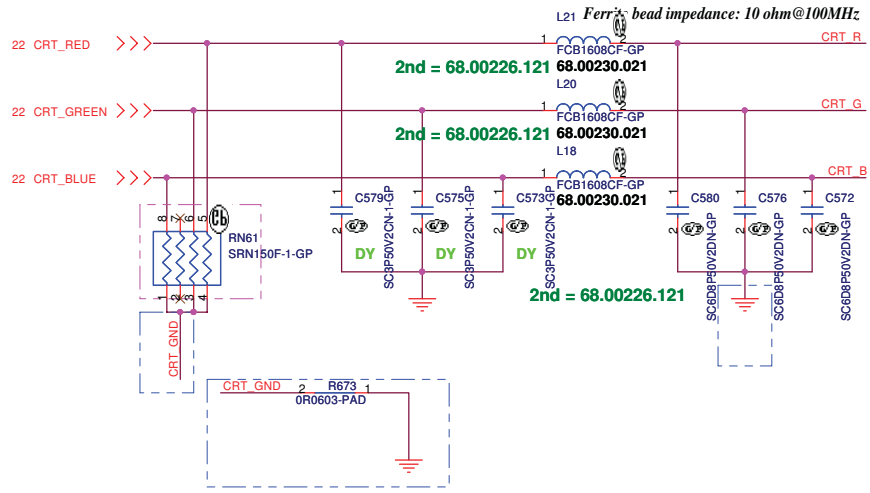
Internal Mic



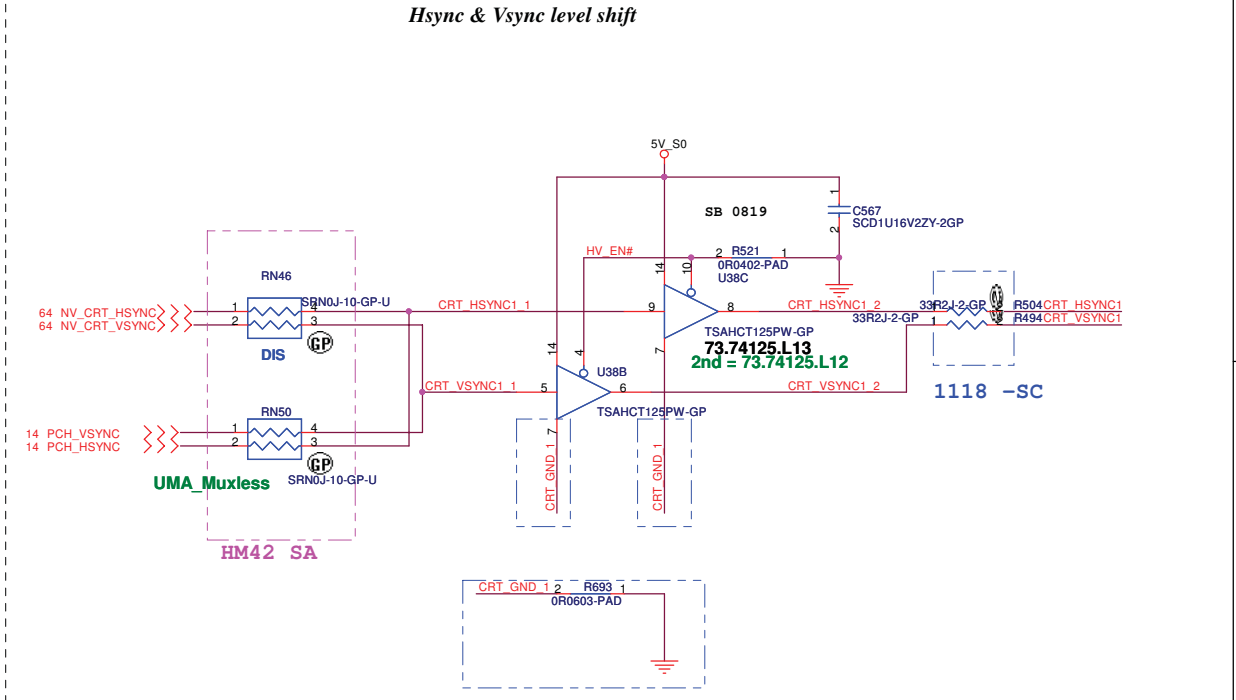
Pin 1 -> right side
 1209 -SC 20.F1240.002 Pin1->left side
 request by EMI Aaron same as JV70-CP

Discrete N11M		
緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
LCD CONN		
Title	HM42-CP	
Size	Document Number	Rev
Date: Friday, January 22, 2010	Sheet 23 of 72	SC

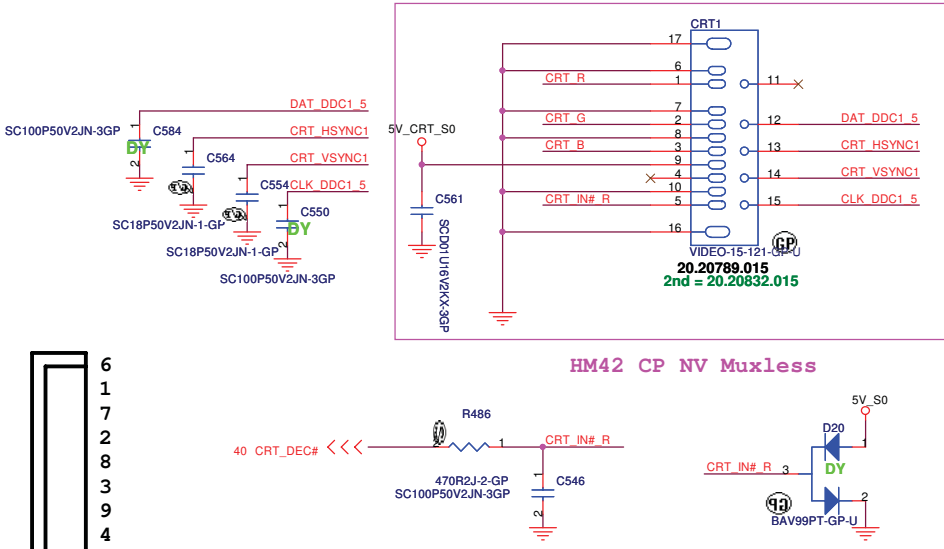
Layout Note:
Place these resistors close to the CRT-out connector



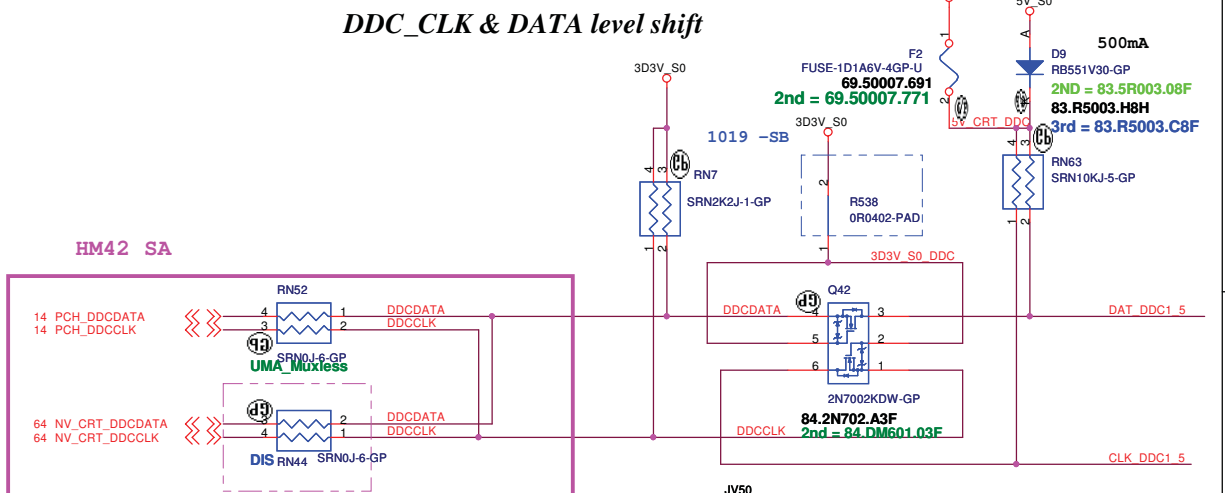
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



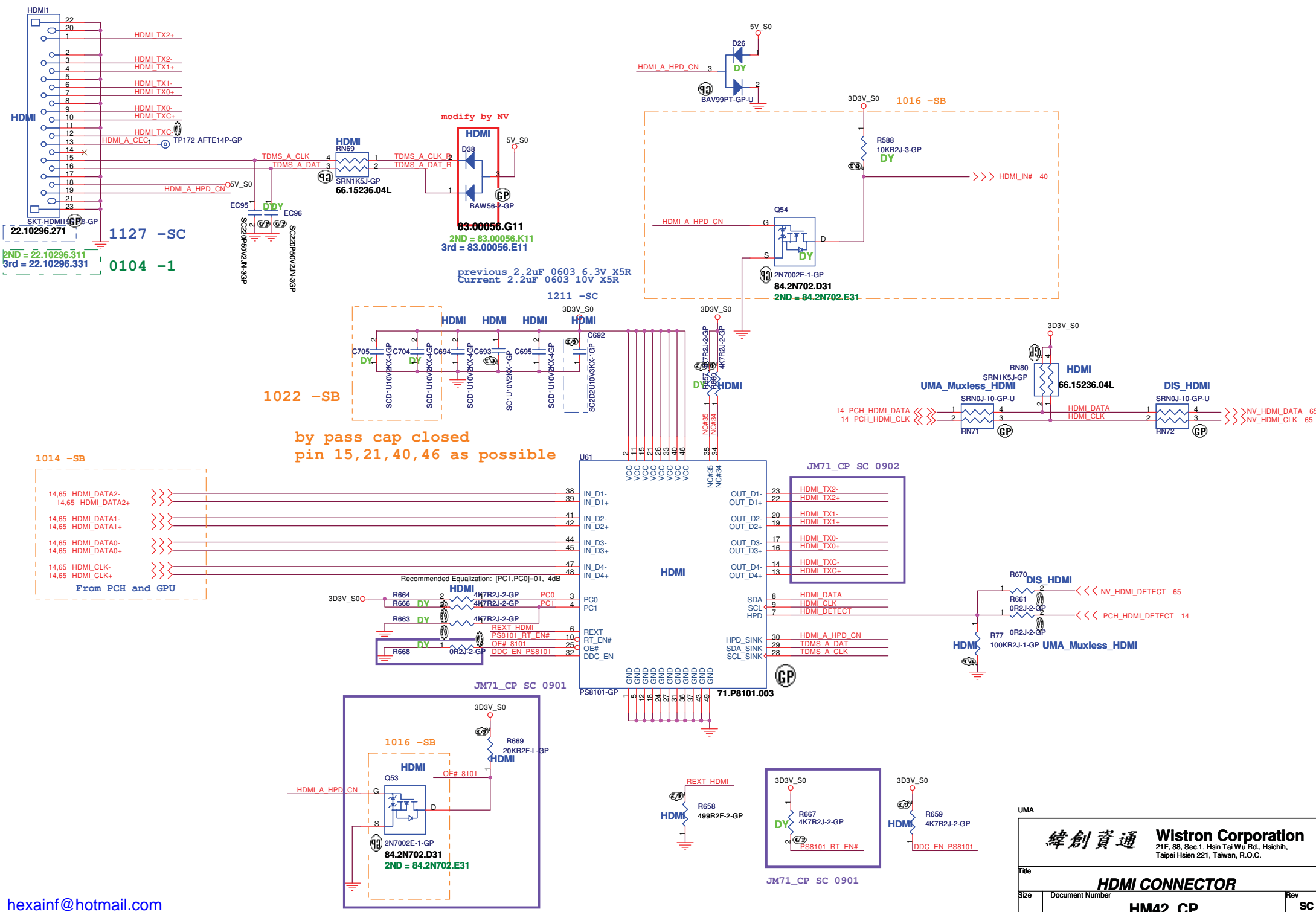
CRT I/F & CONNECTOR



hexanf@hotmail.com
GRATIS - FOR FREE



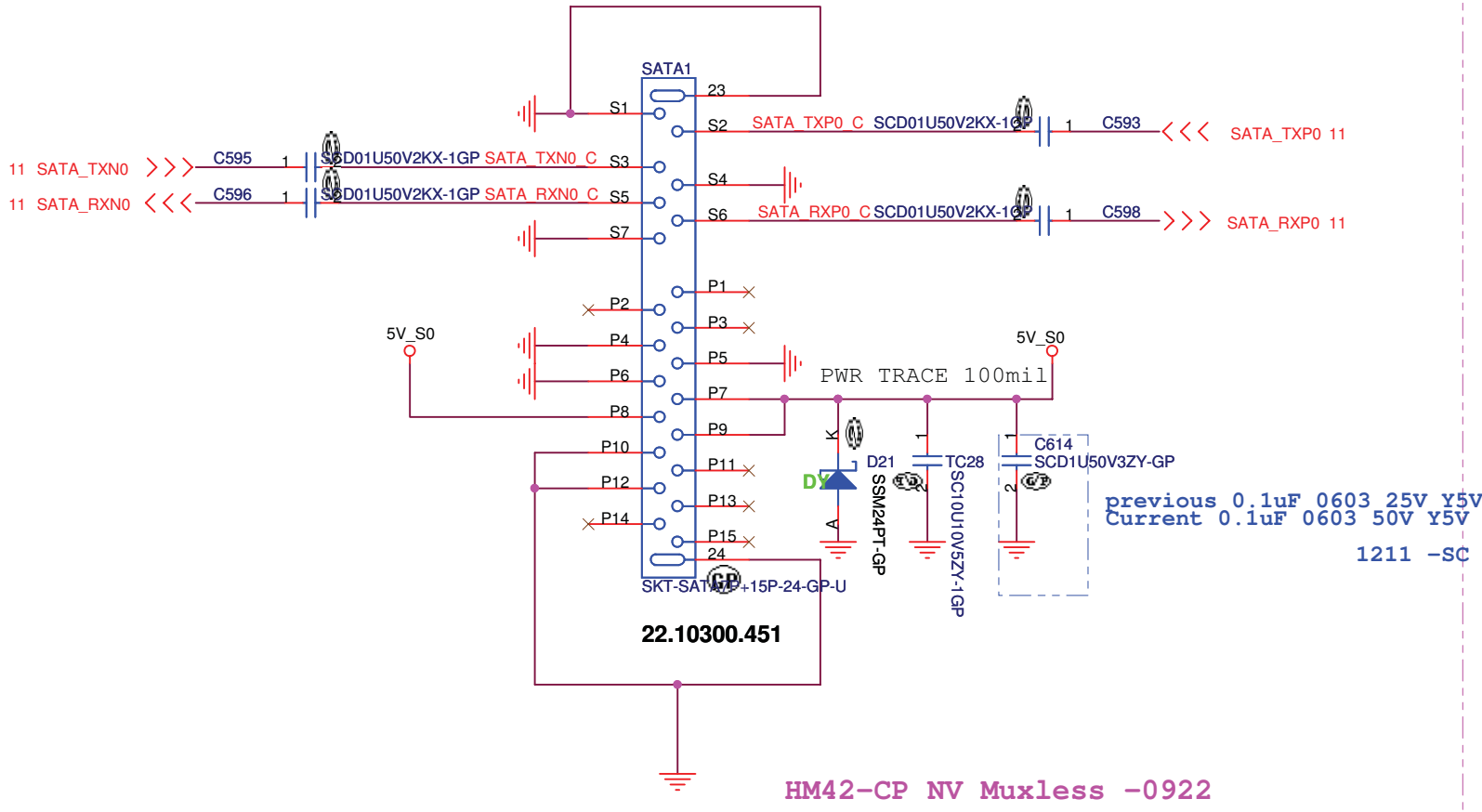
<p>緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title: CRT CONN</p>	
Size: Document Number	Rev: SC
<p>HM42-CP</p>	
Date: Friday, January 22, 2010	Sheet 24 of 72



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HDMI CONNECTOR	
HM42_CP	
Title:	SC
Size:	Rev:
Document Number:	Sheet 25 of 72
Date: Friday, January 22, 2010	

SATA Connector

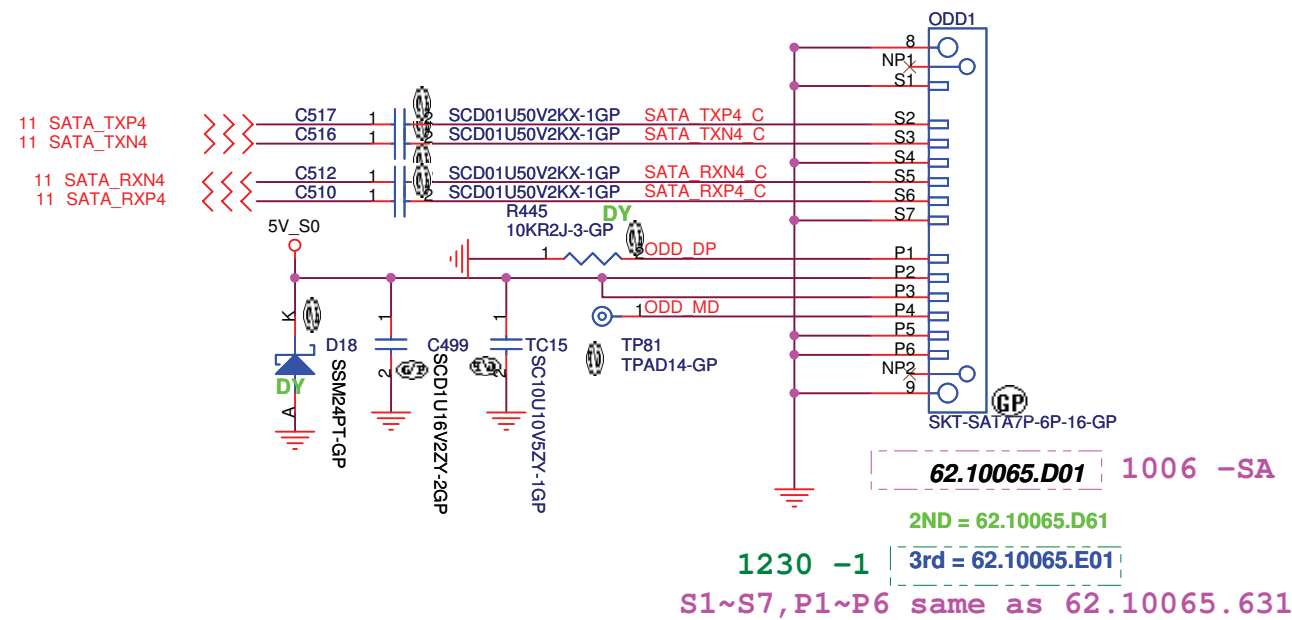


UMA

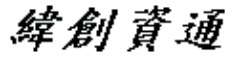
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDD CONN		
Size	Document Number	Rev
	HM42-CP	SC
Date:	Friday, January 22, 2010	Sheet 26 of 72

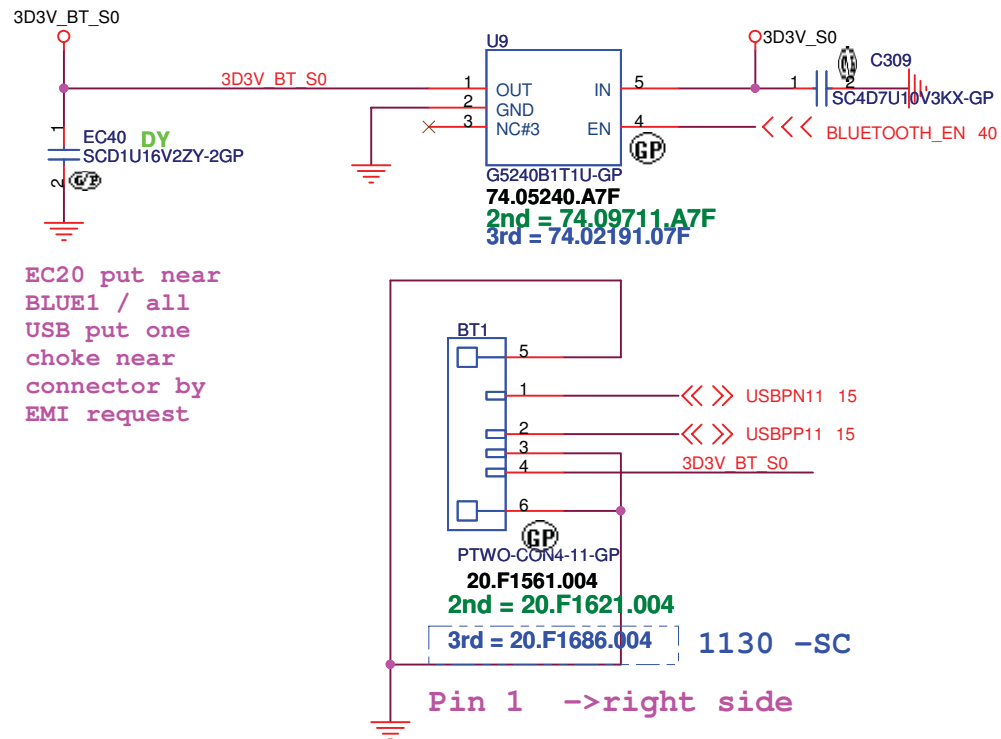
ODD Connector



UMA

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
ODD	
Size	Document Number
HM42-CP	
Date:	Rev
Friday, January 22, 2010	SC
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BLUETOOTH MODULE



EC20 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request

JV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title

BLUETOOTH

Size

Document Number

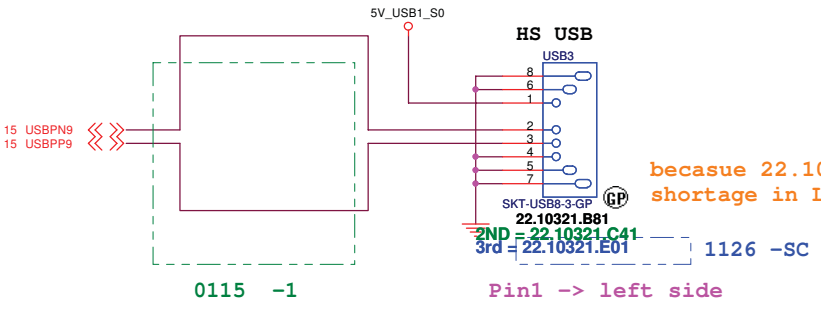
HM42-CP

Rev

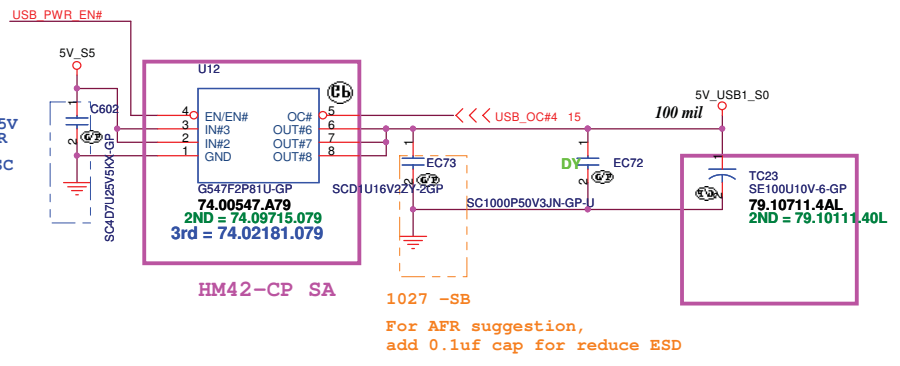
SC

Date: Friday, January 22, 2010

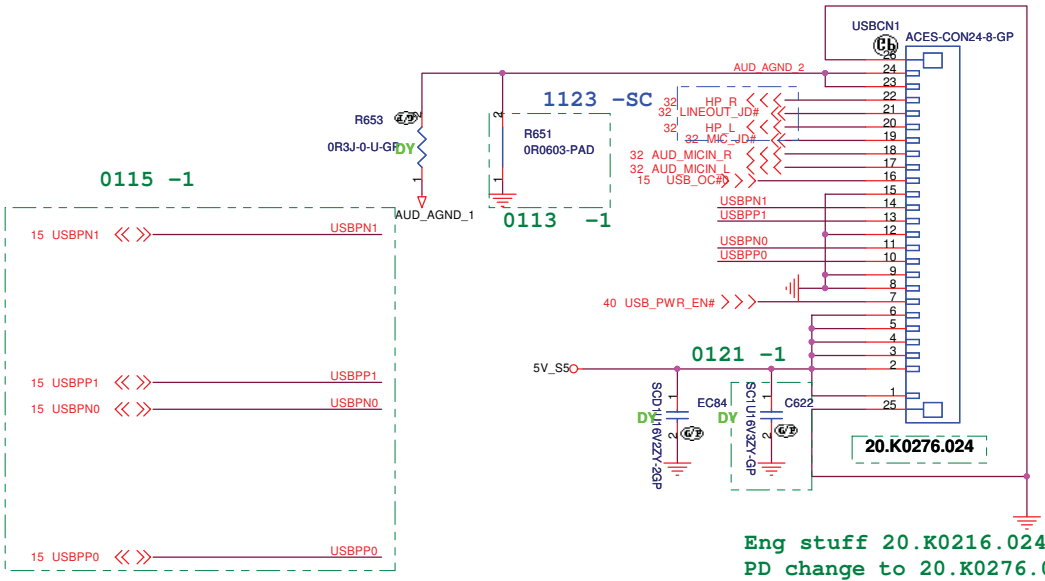
Sheet 28 of 72



previous 4.7uF 0805 16V Y5V
Current 4.7uF 0805 25V X5R
1211 -SC




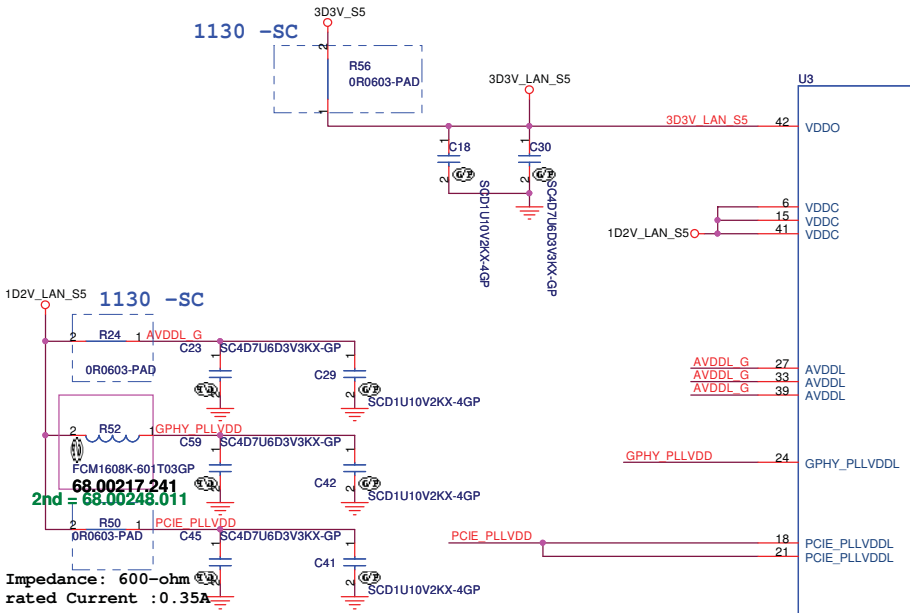
because 22.10321.B81 and 22.10321.C41
shortage in Lab stage, stuff 22.10321.361.



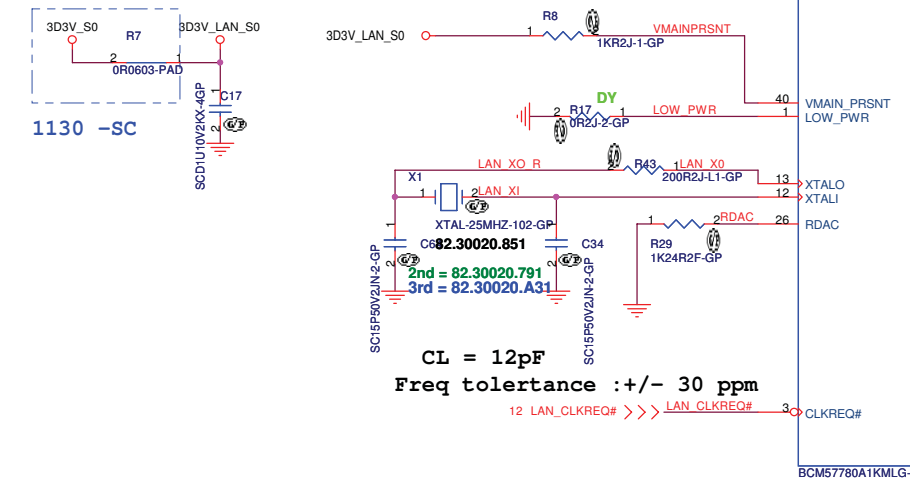
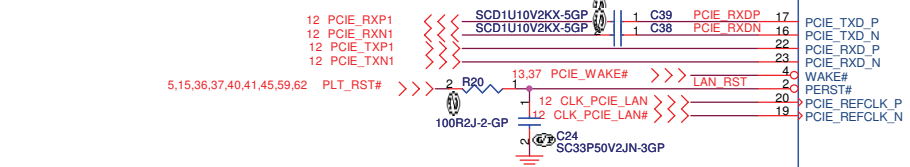
Eng stuff 20.K0216.024 Pin1 -> left side
PD change to 20.K0276.024 Pin1 -> left side
so do not swap net

hexainf@hotmail.com
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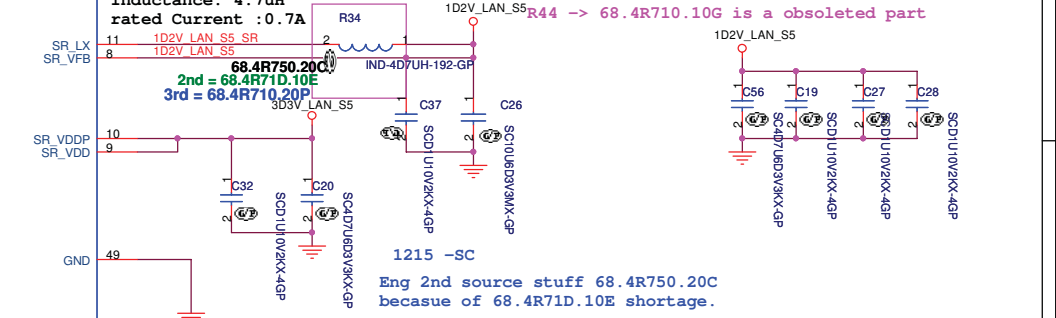
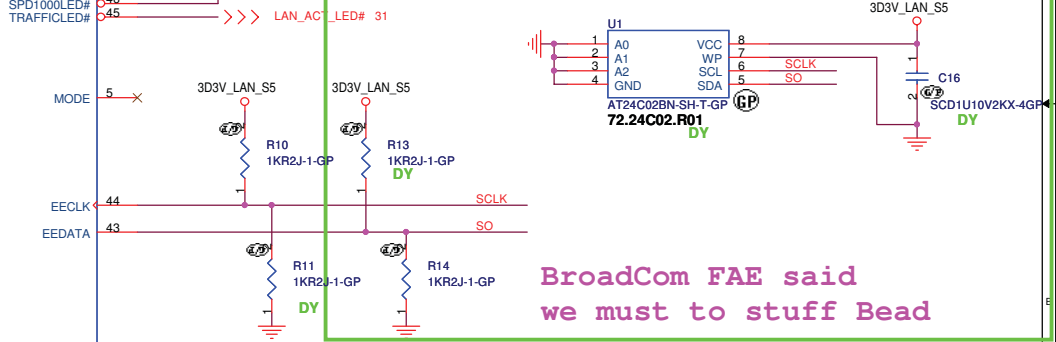
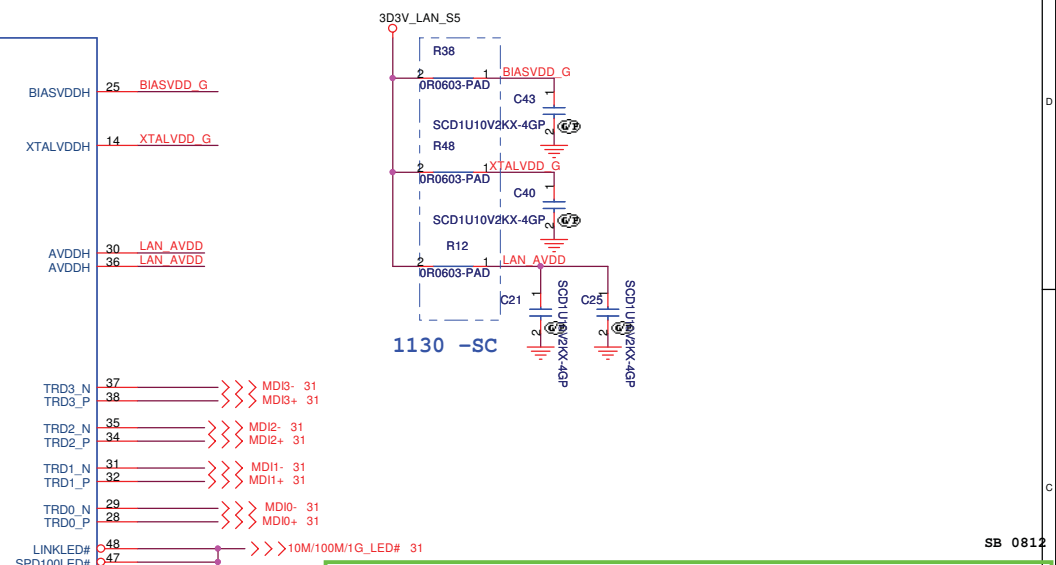
 Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
USB and Audio CONN		
Size	Document Number	Rev
	HM42-CP	SC
Date: Friday, January 22, 2010		Sheet 29 of 72



BroadCom FAE said we must to stuff Bead



CL = 12pF
Freq tolerance : +/- 30 ppm

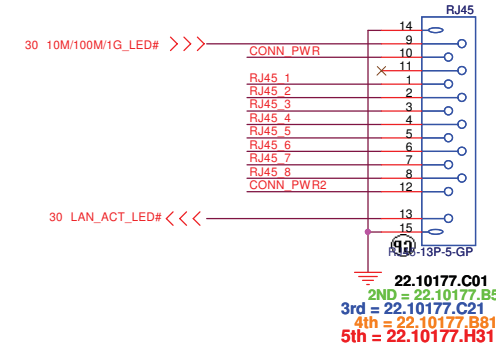
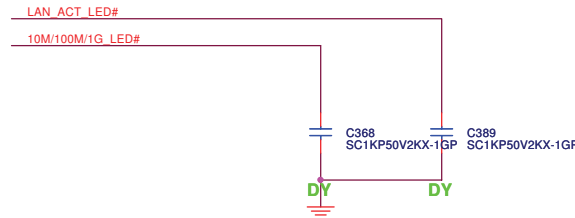
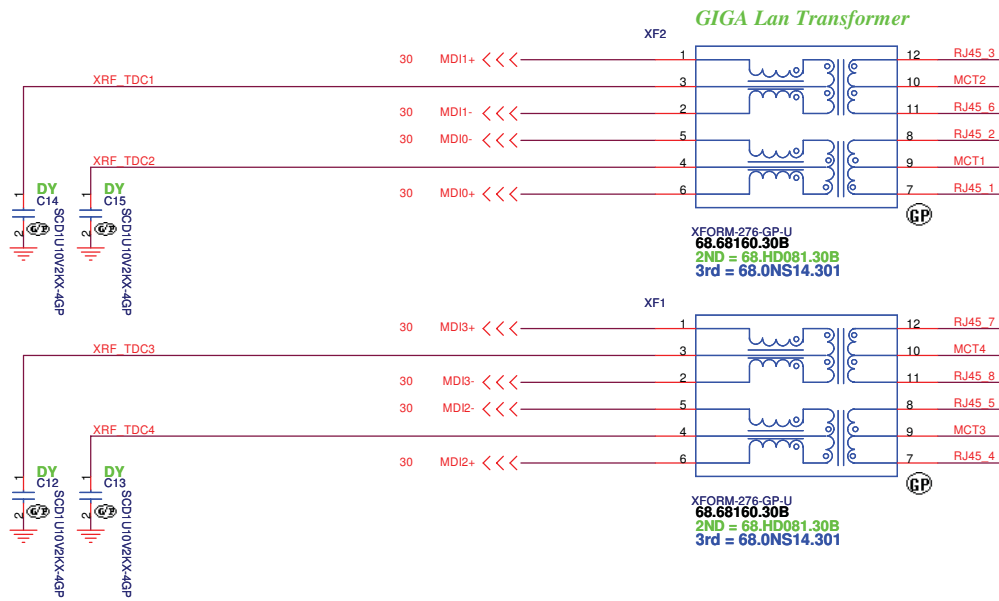


Inductance: 4.7uH
rated Current : 0.7A
r44 -> 68.4R710.10G is a obsoleted part
Eng 2nd source stuff 68.4R750.20C because of 68.4R71D.10E shortage.

LAN Connector

LAN Connector

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

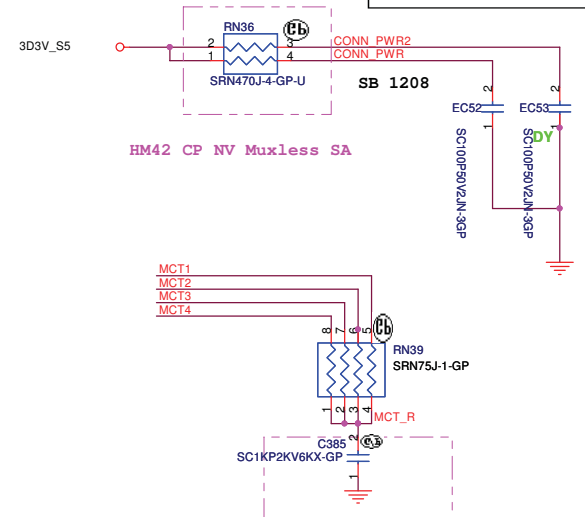


2 LED LAYOUT

NODE	COLOR
12(+)	YELLOW
13(-)	YELLOW

3 LED LAYOUT

NODE	COLOR
9(-)	GREEN
10(+)	GREEN
11(-)	ORANGE
10(+)	ORANGE

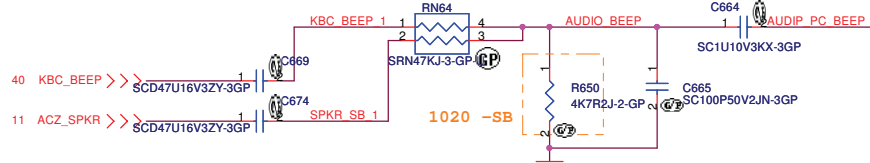


UMA

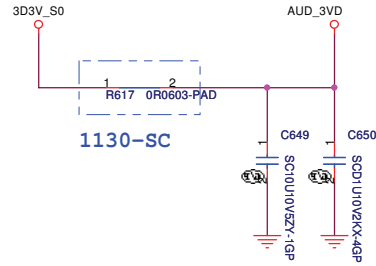
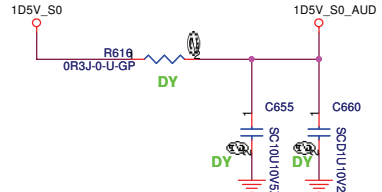
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**

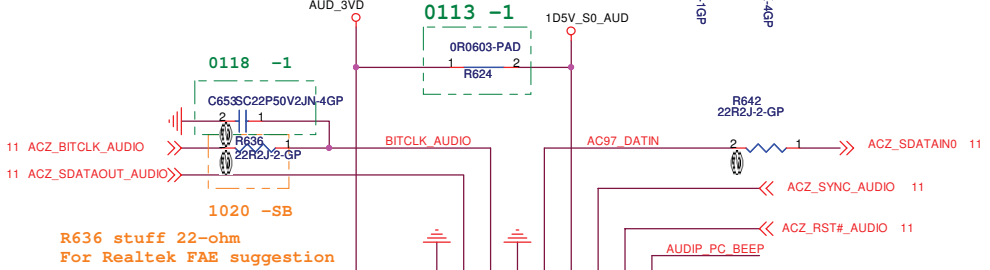
Size A3	Document Number HM42-CP	Rev SC
Date: Friday, January 22, 2010	Sheet 31 of 72	



change R650 from 10K-ohm to 4.7K-ohm
For preventing the beep sound is too loudly
from Realtek FAE suggestion

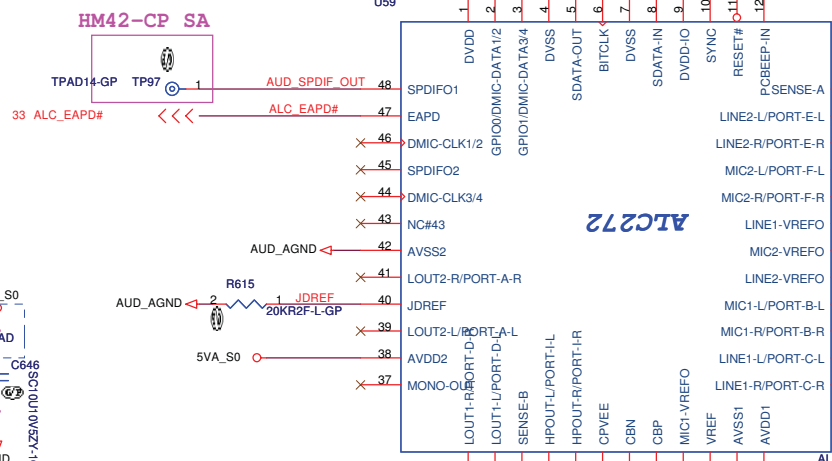


1130-SC

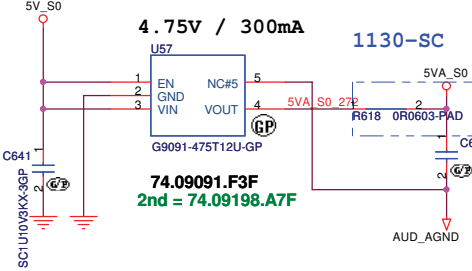


R636 stuff 22-ohm
For Realtek FAE suggestion

HM42-CP SA



ALC272



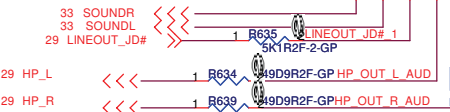
4.75V / 300mA

1130-SC

74.09091.F3F
2nd = 74.09198.A7F

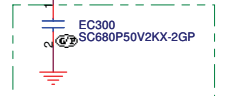
HM4-CP SA

71.ALC272.A0G

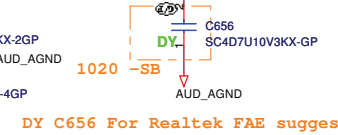


29 HP_L
29 HP_R

0118 -1 EMI

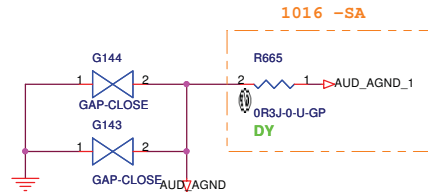


83.00355.A1F
2nd = 83.00355.D1F
3rd = 83.00355.E1F



DY C656 For Realtek FAE suggestion

previous 2.2uF 0603 10V Y5V
Current 2.2uF 0603 10V X5R
1211 -SC



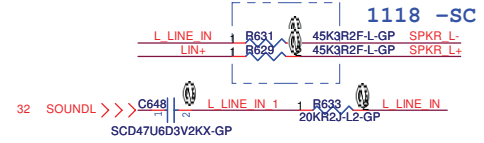
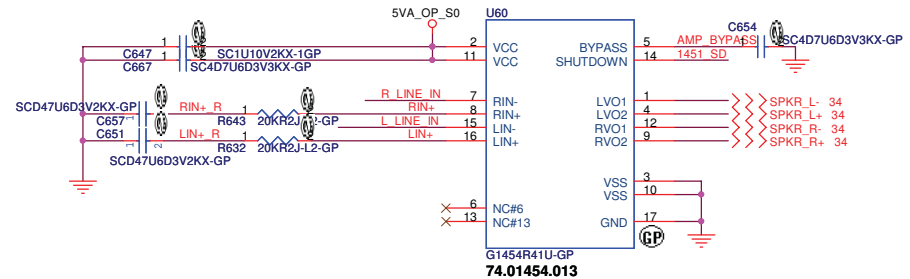
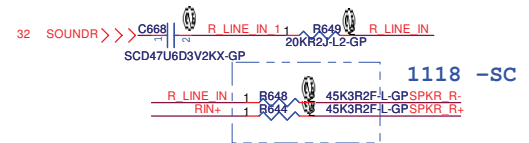
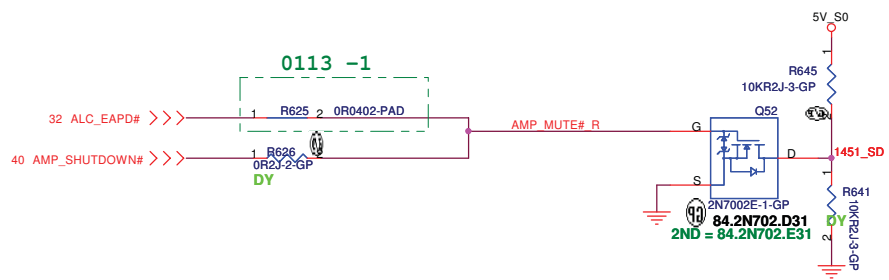
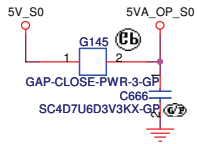
1016 -SA

<Core Design>

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Title: **Azalia codec ALC272**

Size A3	Document Number	Rev
	HM42-CP	SC
Date: Friday, January 22, 2010	Sheet 32 of 72	

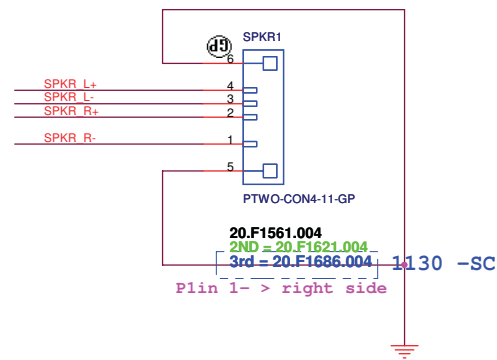
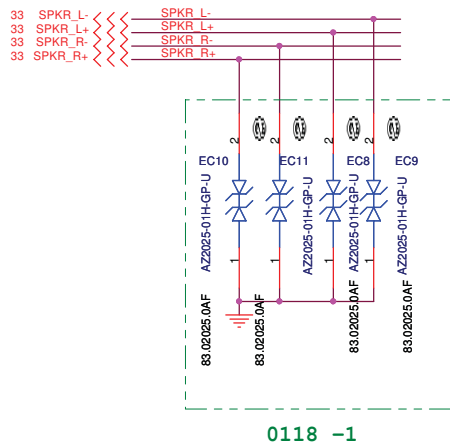


Gain = $R_f/R_i = 52K/20K = 2.6V/V$
 $f(HP) = 1/(2 \cdot \pi \cdot 20K \cdot 0.47\mu f) = 16.9Hz$
 If $V_{IN} = 1.54V$ Gain = $2.6V/V$ $R_L = 4\Omega$ $V_O(peak) = 4V$ $V(rms) = 2.828V$
 Power = $2.446^2/4 = 1.5W$

UMA

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
AUDIO AMP		
Size	Document Number	Rev
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Internal Speaker



Discrete N11M

緯創資通

Wistron Corporation

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Title

AUDIO SPEARK

Size

Document Number

HM42-CP

Rev

SC

Date: Friday, January 22, 2010

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JV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Resrve MDC

Size

Document Number

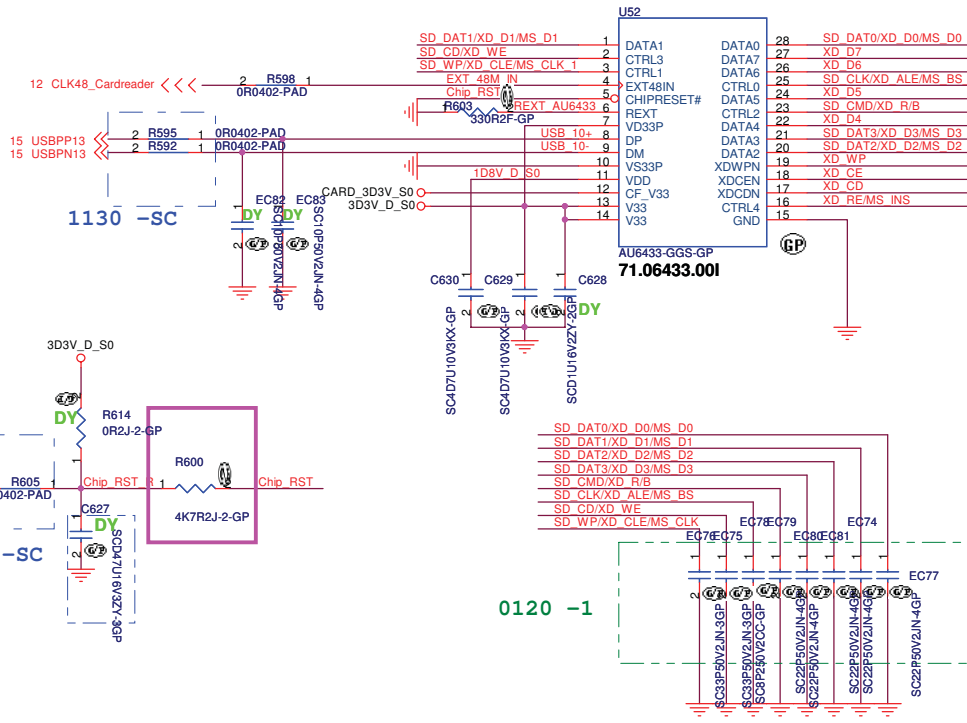
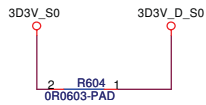
HM42-CP

Rev

SC

Date: Friday, January 22, 2010

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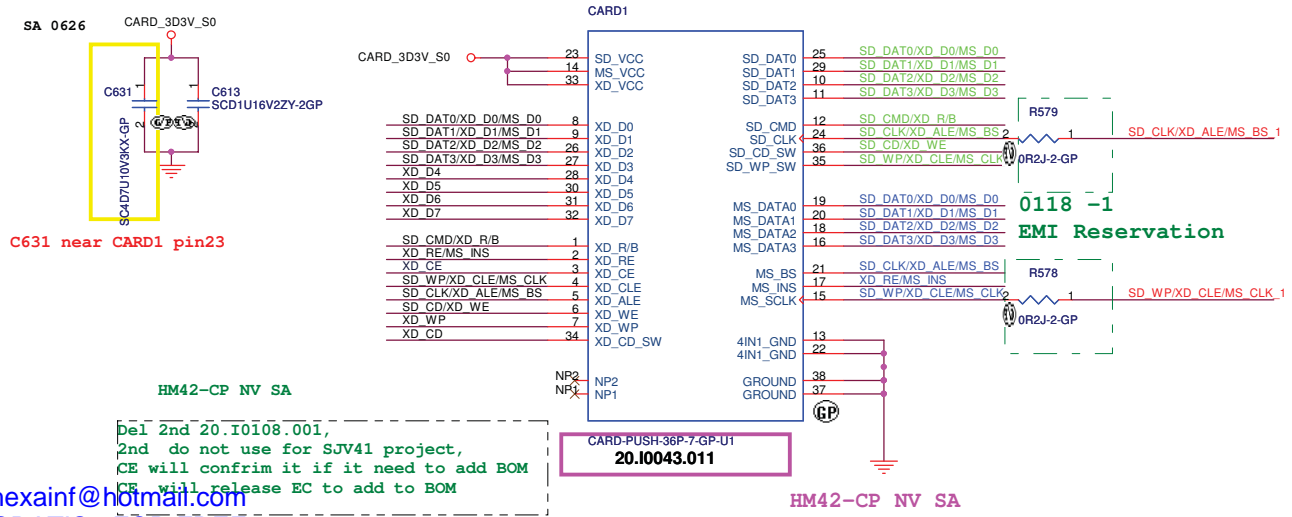


Pin	Name	SD Mode Description
1	CD/DAT3	Card detect/Data line[Bit 3]
2	CMD	Command/Response
3	VSS1	Supply voltage ground
4	VDD	Supply voltage
5	CLK	Clock
6	VSS2	Supply voltage ground
7	DAT0	Data line[Bit 0]
8	DAT1	Data line[Bit 1]
9	DAT2	Data line[Bit 2]

Pin No.	SD/MMC	MS/MS PRO	xD
P1	xD-R/B		2P
P2	xD-RE		3P
P3	xD-CE		4P
P4	xD-CLE		5P
P5	xD-ALE		6P
P6	xD-WE		7P
P7	xD-WP		8P
P8	xD-DO		10P
P9	xD-D1		11P
P10	SD-DAT2	9P	
P11	SD-DAT3	1P	
P12	SD-CMD	2P	
P13	4in1-GND	3P/6P	1P/10P 1P/9P
P14	MS-VCC		8P
P15	MS-SCLK		8P
P16	MS-DATA3		7P
P17	MS-INS		6P
P18	MS-DATA2		5P
P19	MS-DATA0		4P

Pin No.	SD/MMC	MS/MS PRO	xD
P20	MS-DATA1		3P
P21	MS-BS		2P
P22	4in1-GND	3P/6P	1P/10P 1P/9P
P23	SD-VCC	4P	
P24	SD-CLK	5P	
P25	SD-DAT0	7P	
P26	xD-D2		12P
P27	xD-D3		13P
P28	xD-D4		14P
P29	SD-DAT1	8P	
P30	xD-D5		15P
P31	xD-D6		16P
P32	xD-D7		17P
P33	xD-VCC		18P
P34	xD-CD-SW		19P
P35	SD-WP-SW	SD-WP-SW	
P36	SD-CD-SW	SD-CD-SW	
P37	4 in 1-GND	SD-WP/CD-SW-GND	
P38			

5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



Pin	Name	Dir	description
1	XD_CD#	-	presence detect
2	R/B#	OUT	Ready / Busy (open-drain)
3	RE#	IN	Read Enable
4	CE#	IN	Card Enable
5	CLE	IN	Command Latch Enable
6	ALE#	IN	Address Latch Enable
7	WE#	IN	Write Enable
8	WP#	IN	Write Protect
9	GND	-	Ground
10	SD0	IN/OUT	data bit 0
11	SD1	IN/OUT	data bit 1
12	SD2	IN/OUT	data bit 2
13	SD3	IN/OUT	data bit 3
14	SD4	IN/OUT	data bit 4
15	SD5	IN/OUT	data bit 5
16	SD6	IN/OUT	data bit 6
17	SD7	IN/OUT	data bit 7
18	VCC	-	3.3V power

Pin	Pin Name	Description
1	VSS	Vss
2	BS	Bus state signal
3	DATA1	Data1 Parallel / NC Serial
4	SDIO/DATA0	Data0 Parallel / Data Serial
5	DATA2	Data2 Parallel / NC Serial
6	INS	Stick detect (connected to VSS)
7	DATA3	Data3 Parallel / NC Serial
8	SCLK	Clock signal
9	VCC	Vcc (2.7V - 3.6V)
10	VSS	Vss

UMA

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Title: **Cardreader**

Size: Document Number **HM42-CP** Rev **SC**

Date: Friday, January 22, 2010 Sheet 36 of 72

hexainf@hotmail.com
GRATIS - FOR FREE

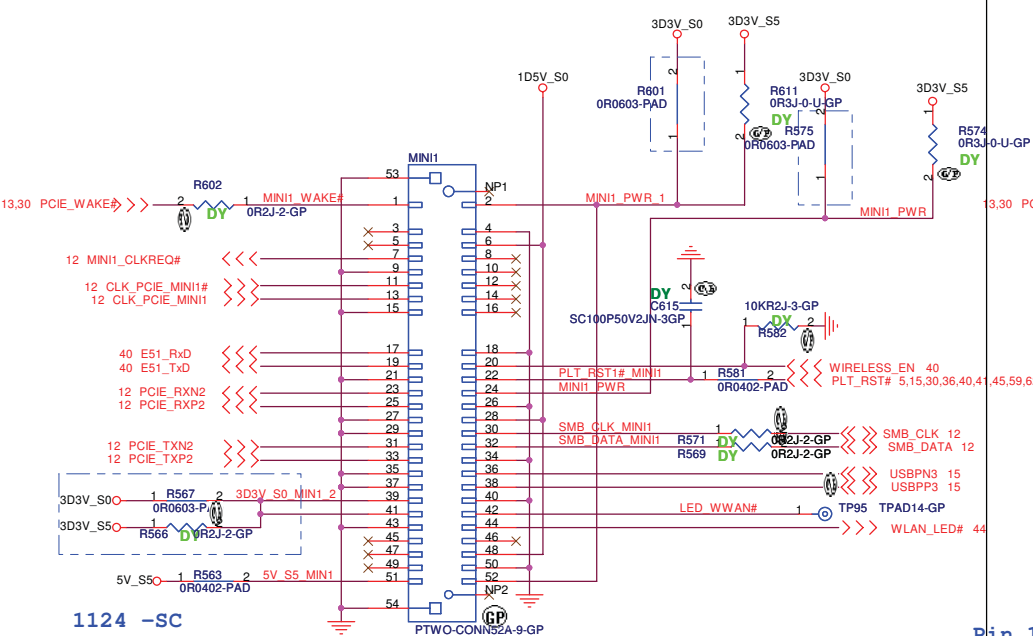
Del 2nd 20.10108.001,
2nd do not use for SJV41 project,
CE will confirm it if it need to add BOM
CE will release EC to add to BOM

CARD-PUSH-36P-7-GP-U1
20.10043.011

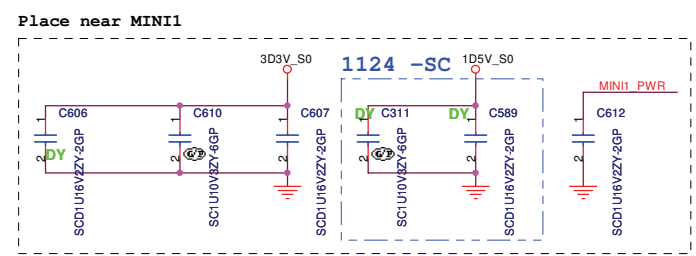
HM42-CP NV SA

Mini Card Connector(WLAN)

Support debug-card

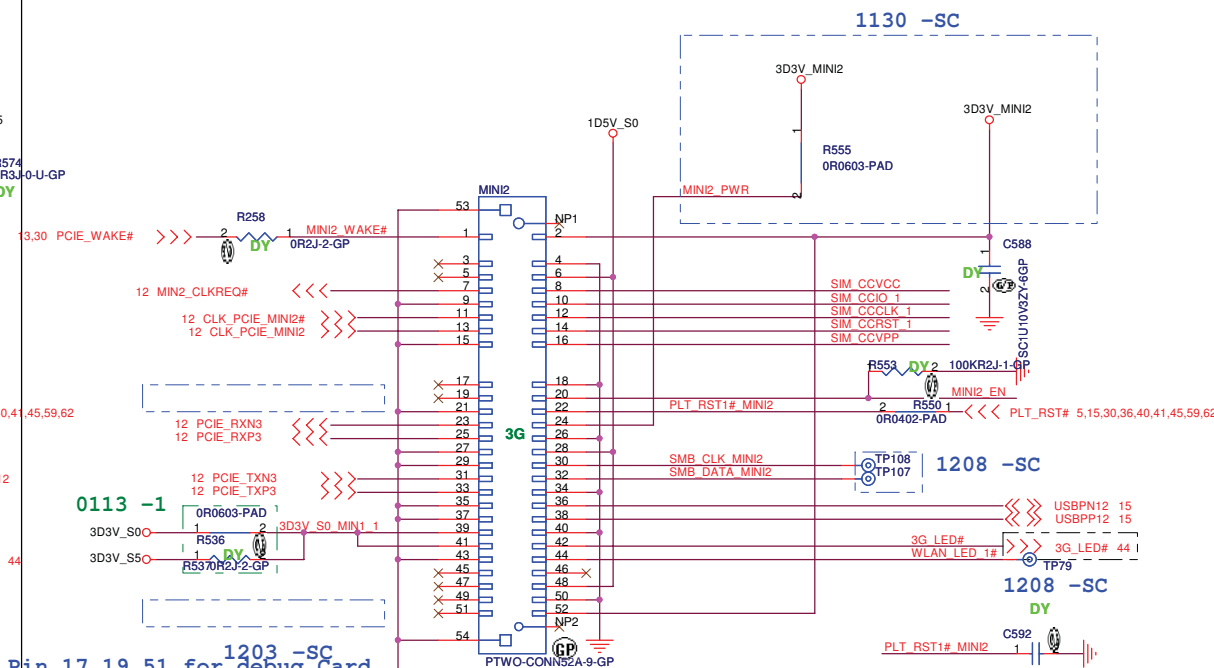


20.F1519.052
 2ND = 62.10043.601
 3rd = 62.10043.841
 4th = 20.F1693.052



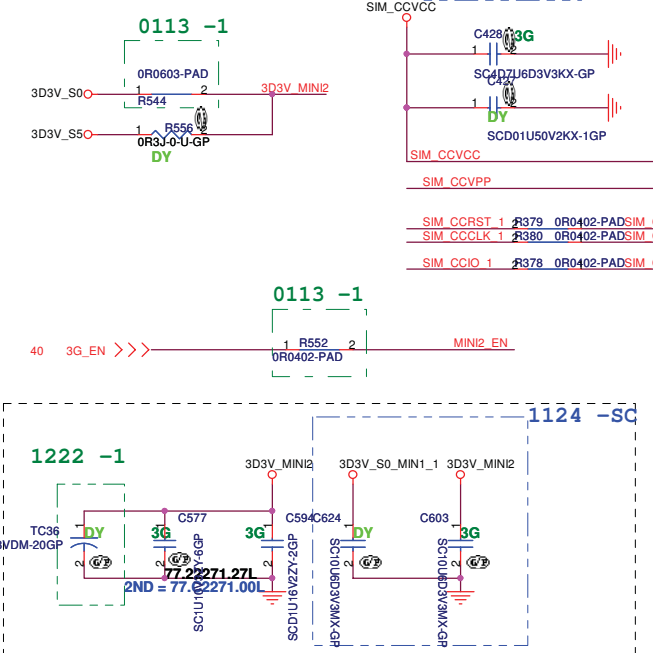
hexainf@hotmail.com
 GRATIS - FOR FREE

Mini Card Connector(Robson2 and 3G)



Pin 17,19,51 for debug Card

20.F1519.052
 2ND = 62.10043.601
 3rd = 62.10043.841
 4th = 20.F1693.052



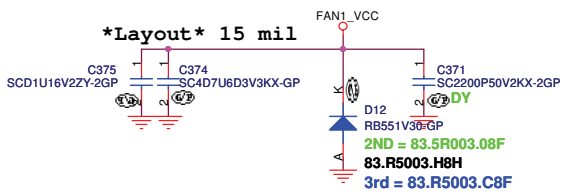
Discrete N11M

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD**

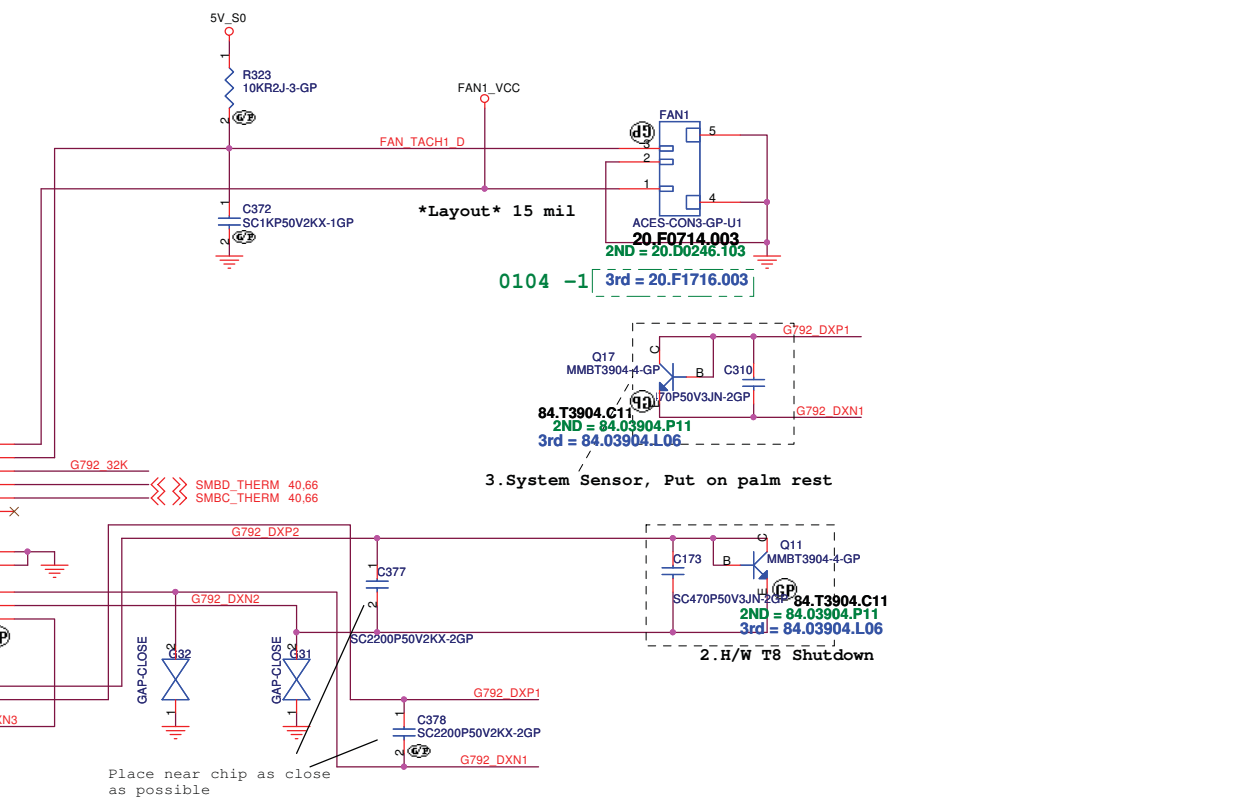
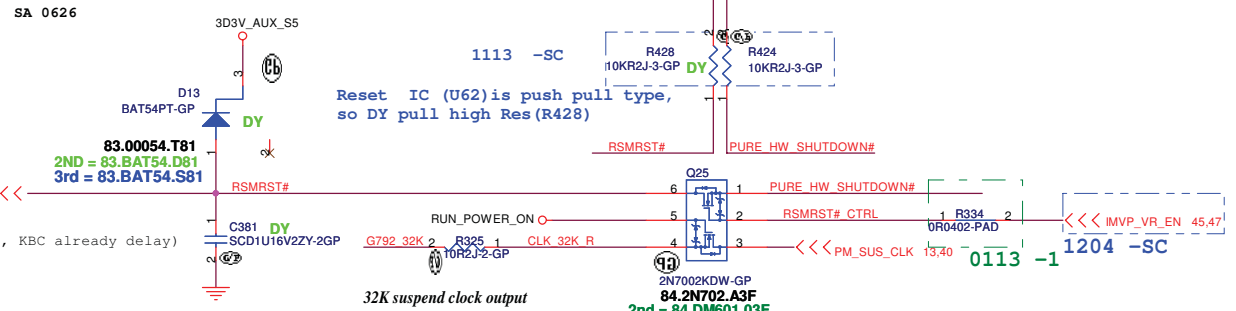
Size A3 Document Number: **HM42-CP** Rev: **SC**

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Thermal Get define

- Sensor0 => CPU
- Sensor1=> system temp (thermal DPX1)
- Sensor2=> HW T8 shut down(thermal DPX2)
- Sensor3=> unused(thermal DPX3)
- Sensor4=> MCH
- Sensor5=> PCH
- Sensor6=> Adpater Current
- Sensor7=>dGPU
- Sensor8=>Battery Thermal
- Sensor9=>Battery Current



Therm_set voltage = $[49.9K / (21K + 49.9K)] \times 5 = 3.519 \text{ V}$

$T_{\text{set}} = 90 \text{ degree}$

therm_set is 3.5V => $[(90 - 72) \times 0.02 + 0.34] \times 5 = 3.5 \text{ V}$

DXP1: System Sensor
 DXP2: H/W Setting (T8)
 DXP3: do not use

UMA

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal/Fan Connector**

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	HM42-CP	SC

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EC BIOS Flash ROM

for ENE FAE suggest, SPICS# is push-pull pin, don't need to pull high

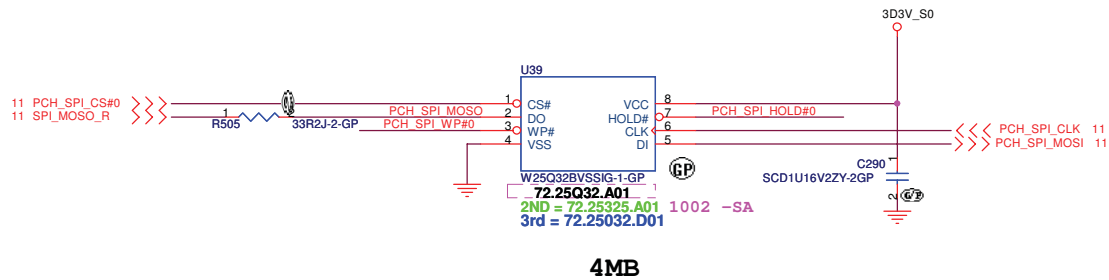
-SA 0930

1021 -SB
base on FAE Kevin discuss with KBC

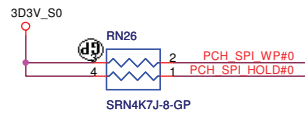
128KB 0121 -1
delete 1st source (72.25105.A01) in PD SMT because it is obsolete parts

close to SPI ROM

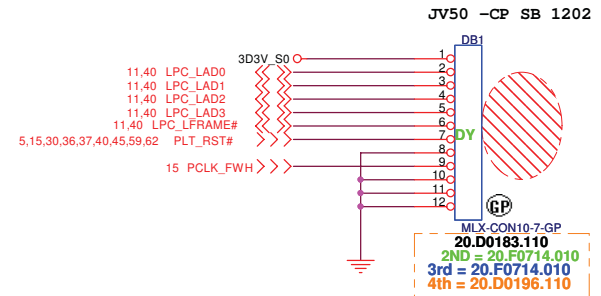
System BIOS Flash ROM



4MB



GOLDEN FINGER FOR DEBUG BOARD

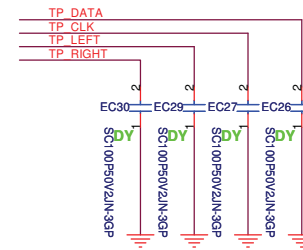
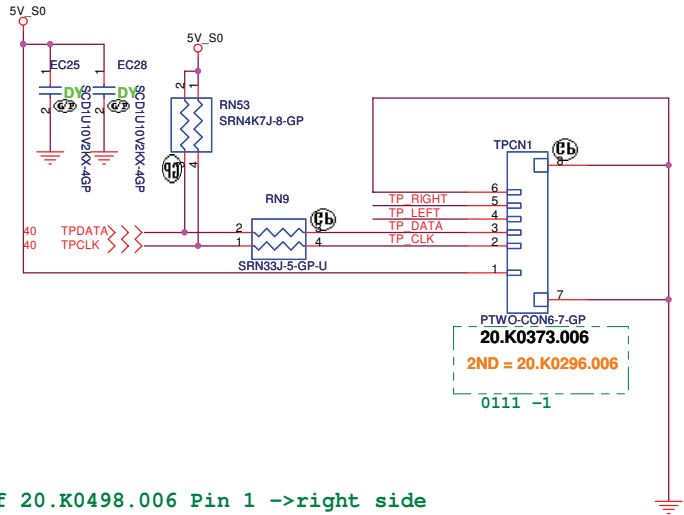


1022 -SB

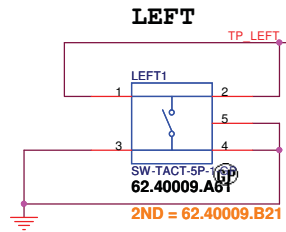
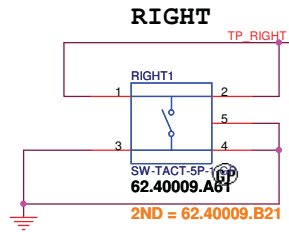
Lab only stuff 4th source (20.D0196.110)
Eng and PD DY DB1

Discrete N11M

Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: BIOS	
Size: Document Number	Rev: SC
HM42-CP	
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Eng stuff 20.K0498.006 Pin 1 ->right side
 PD change to 20.K0373.006 pin 1 ->left side
 so net mirror Vertically

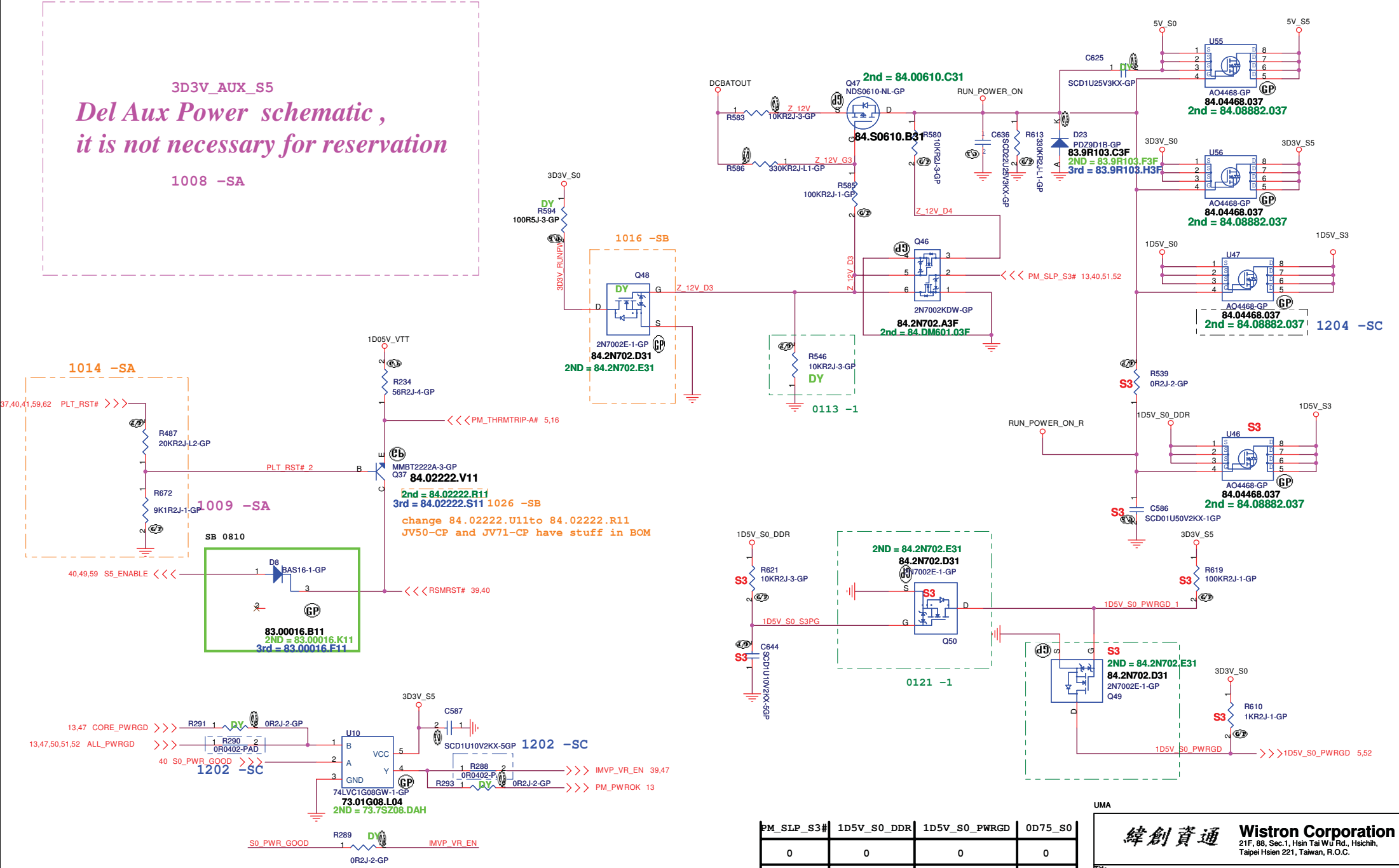


Discrete N11M

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Touch PAD		
Size	Document Number	Rev
	HM42-CP	SC
Date: Friday, January 22, 2010	Sheet 43 of 72	

Run Power

3D3V_AUX_S5
*Del Aux Power schematic,
 it is not necessary for reservation*
 1008 -SA



PM_SLP_S3#	1D5V_S0_DDR	1D5V_S0_PWRGD	0D75_S0
0	0	0	0
1	1	1	1

UMA

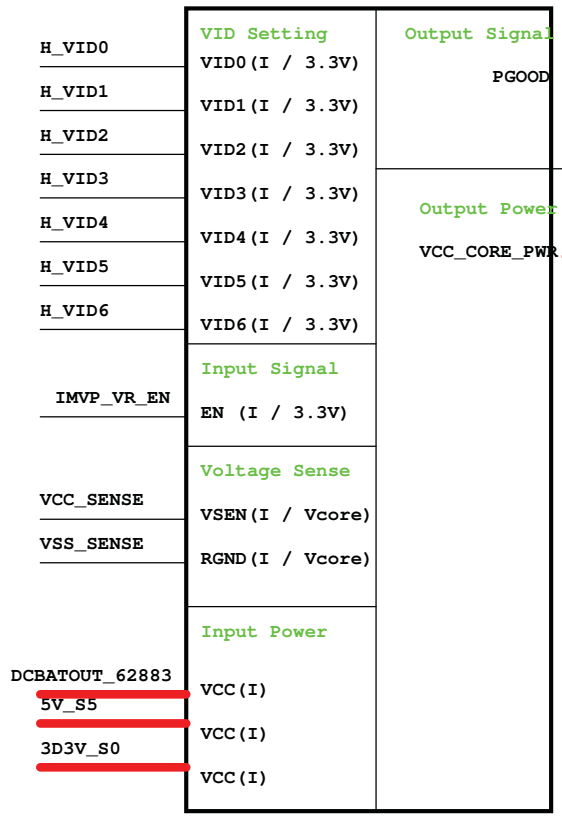
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN POWER and 3D3V AUX S5**

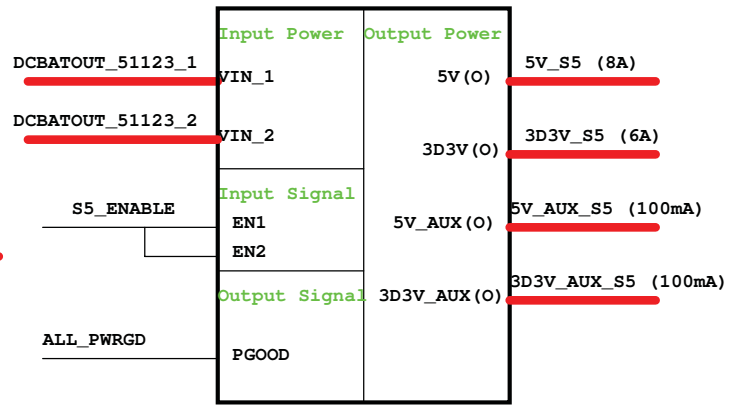
Size: Document Number **HM42-CP** Rev **SC**

Date: Friday, January 22, 2010 Sheet 45 of 72

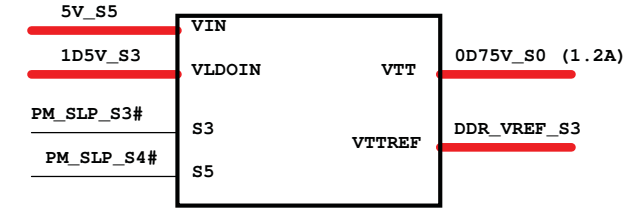
ISL62883 VCC_CORE



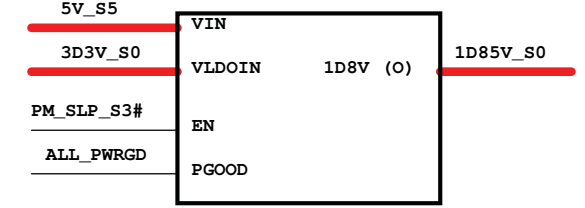
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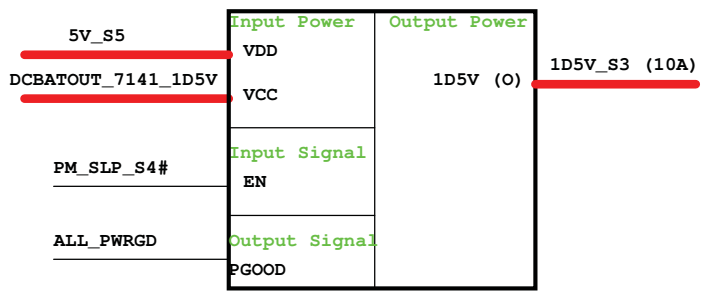
RT9026 0D75V_S0



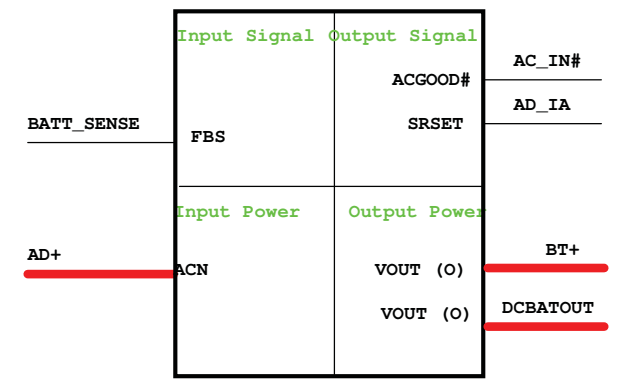
RT9025 1D8V



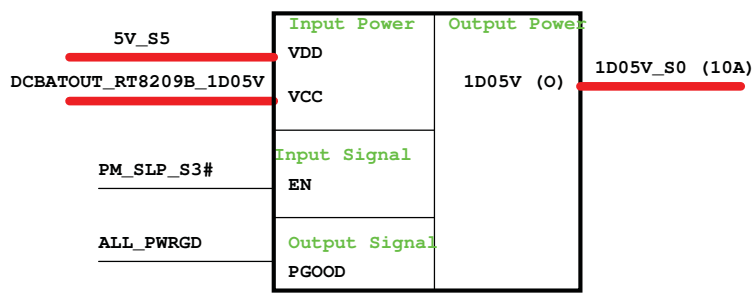
RT9025 1D5V



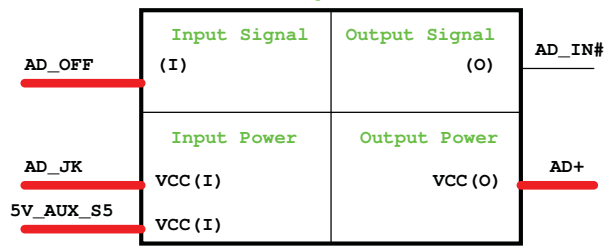
Charger BQ24745



RT8209B 1D05V

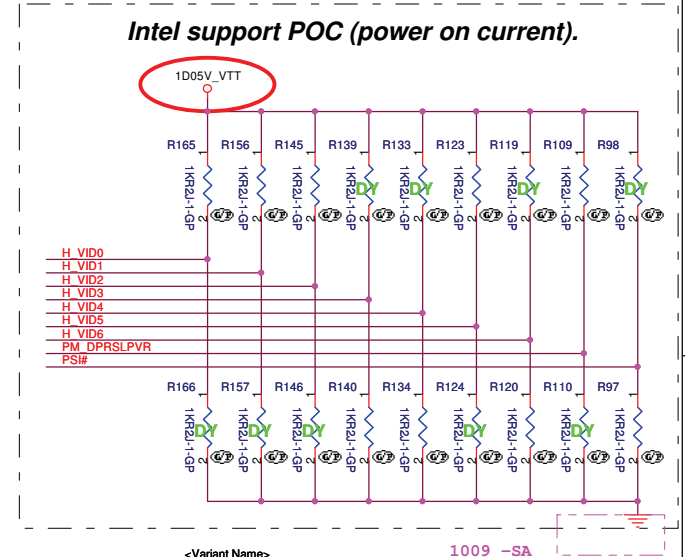
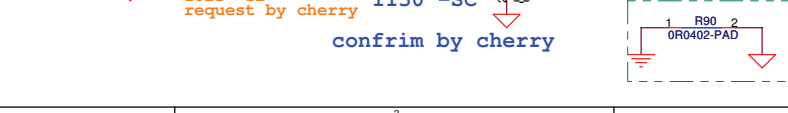
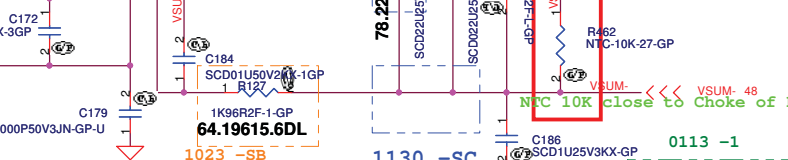
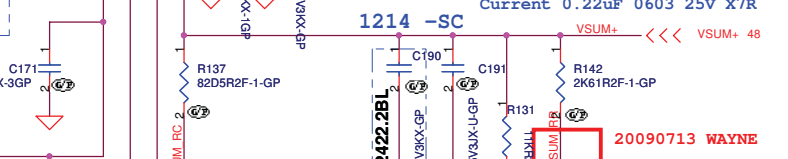
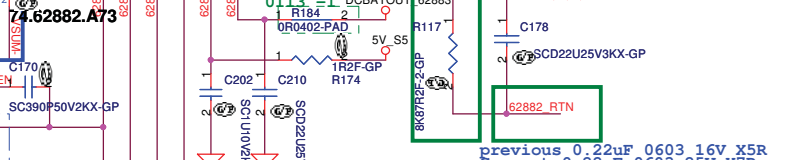
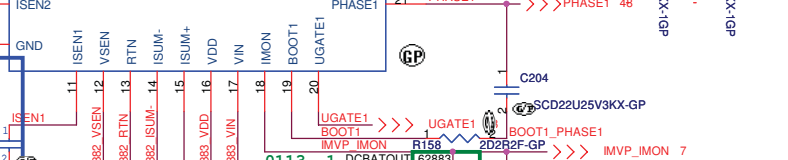
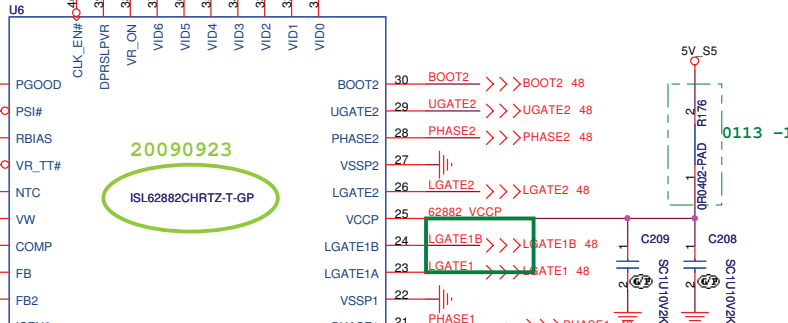
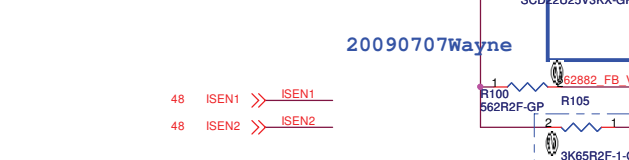
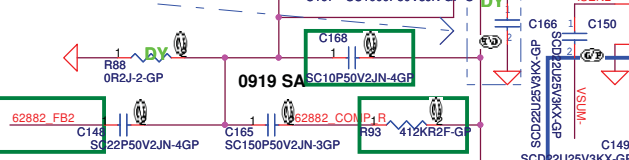
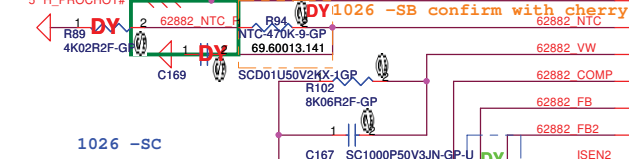
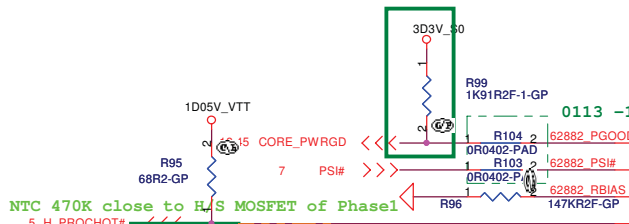
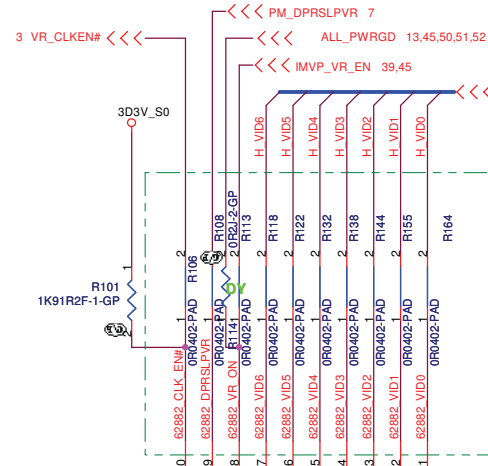
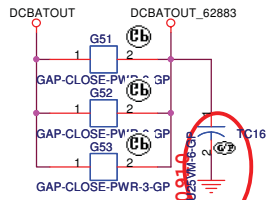
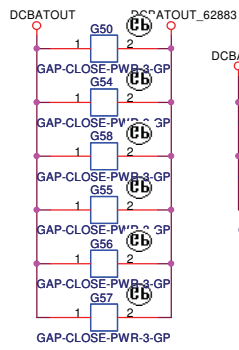


Adapter



Discrete N11M

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Power Block Diagram			
Title	Document Number	Rev	SC
	HM42-CP		
Date: Friday, January 22, 2010	Sheet 46	of	72



Variant Name: 1009 -SA

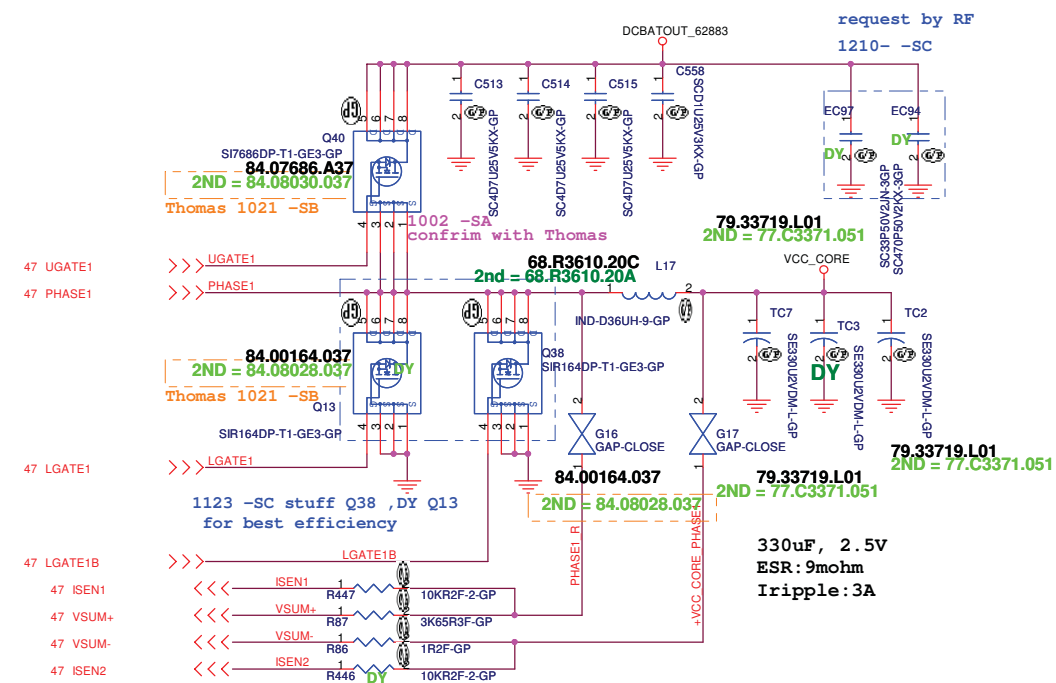
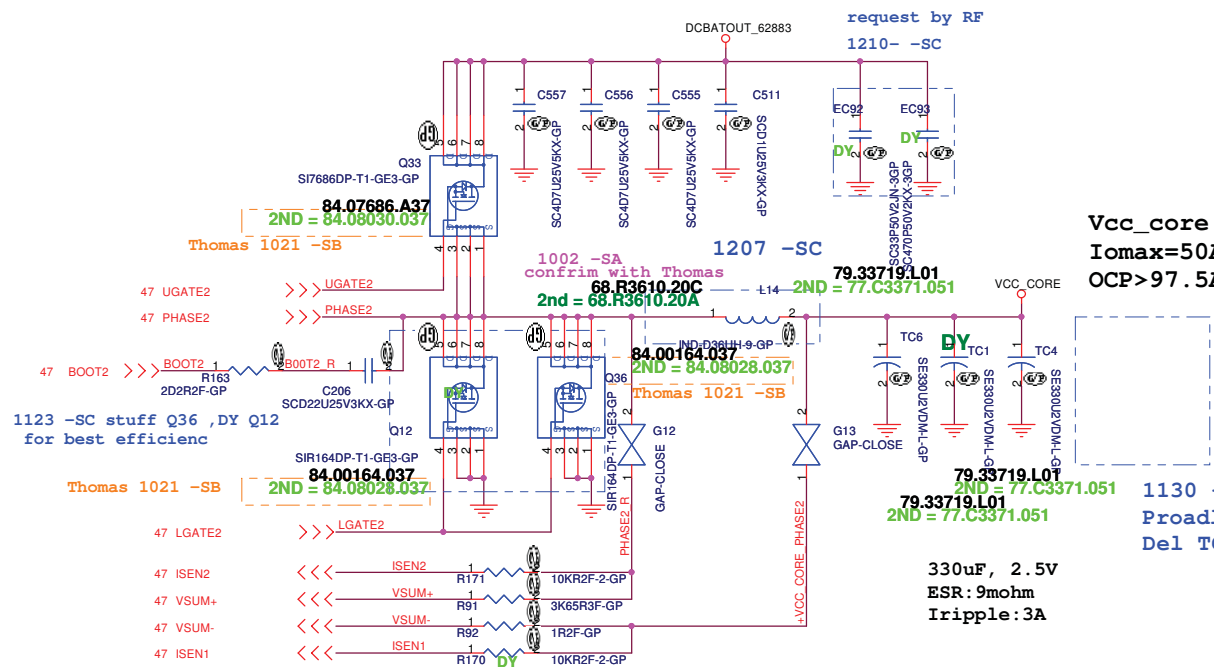
緯創資通 Wistron Corporation
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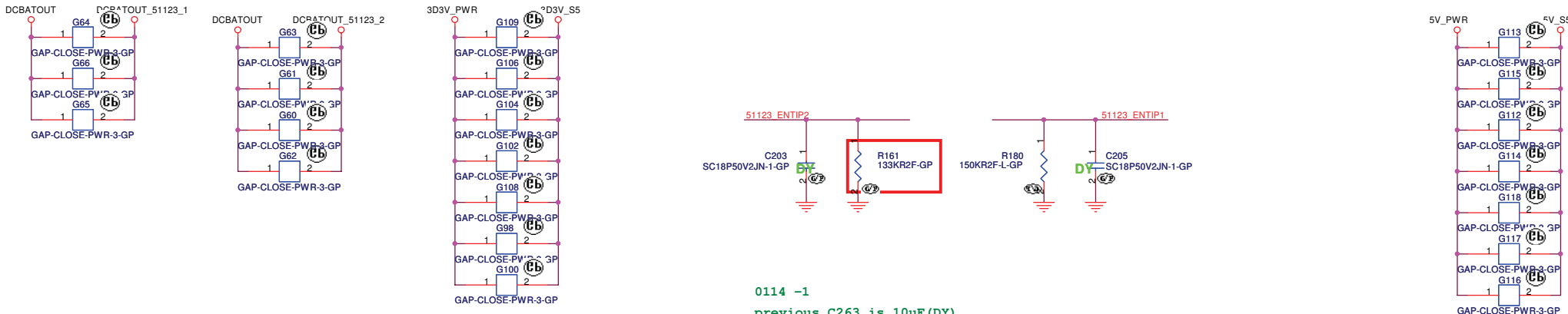
Title: **ISL62882 CPU CORE (1/2)**

Size: Document Number

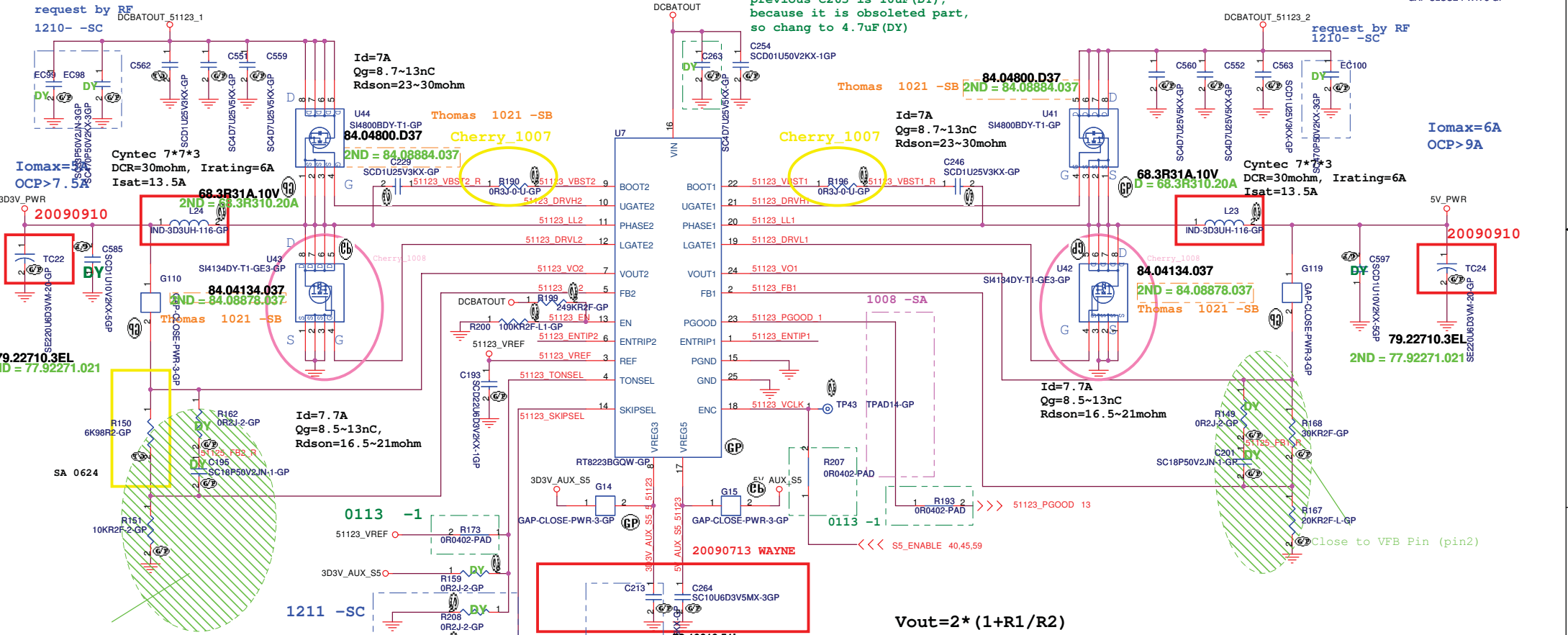
Rev: **SC**

Date: Friday, January 22, 2010 Sheet 47 of 72





0114 -1
 previous C263 is 10uF (DY),
 because it is obsoleted part,
 so change to 4.7uF (DY)



$$V_{out} = 2 * (1 + R1/R2)$$

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

<Variant Name>

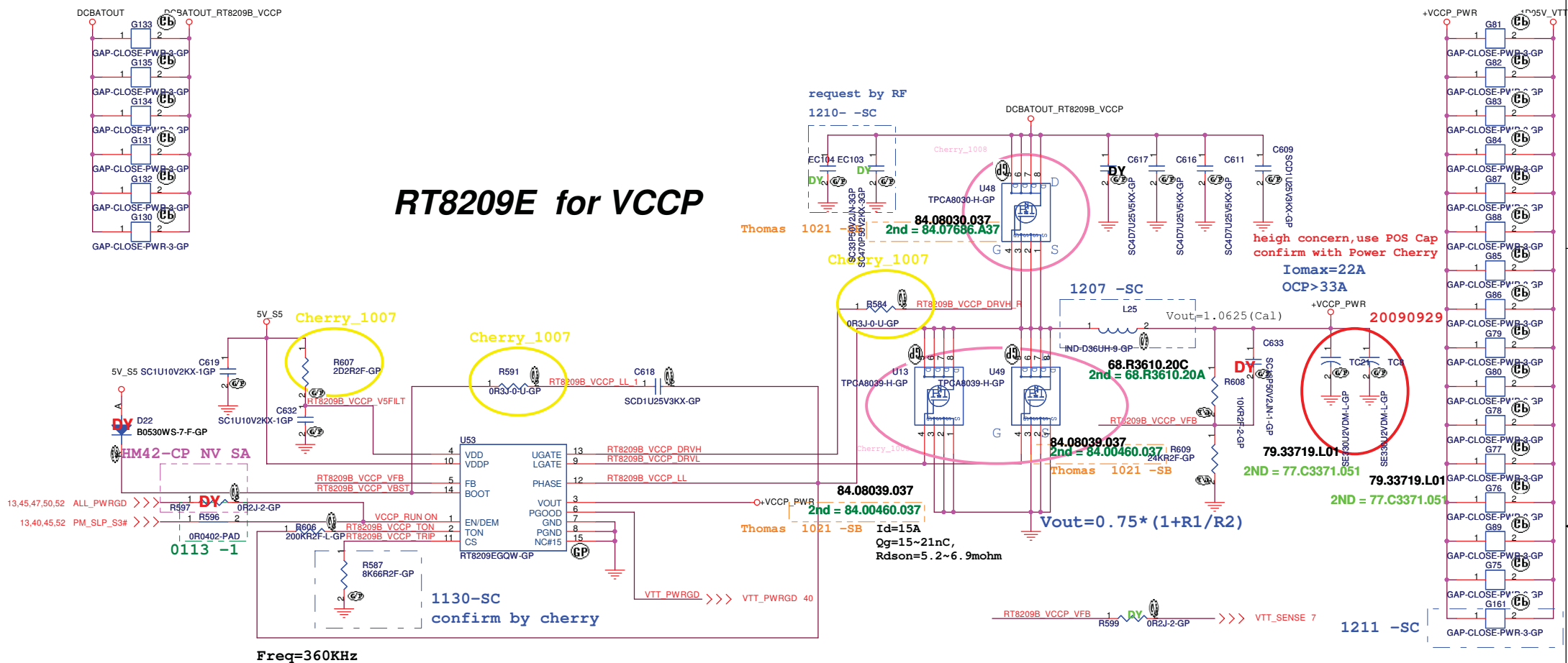
緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8223 5V/3D3V**

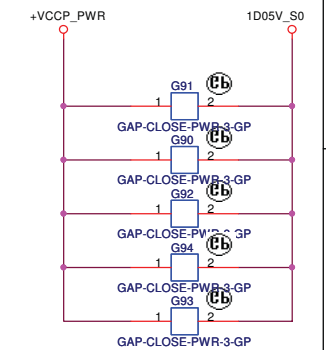
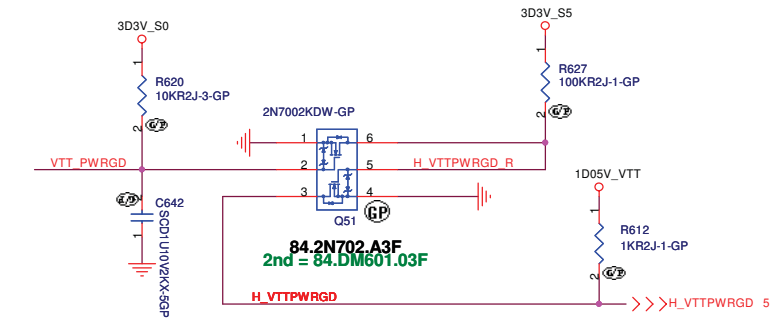
Size: Document Number **HM42-CP** Rev: **SC**

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RT8209E for VCCP

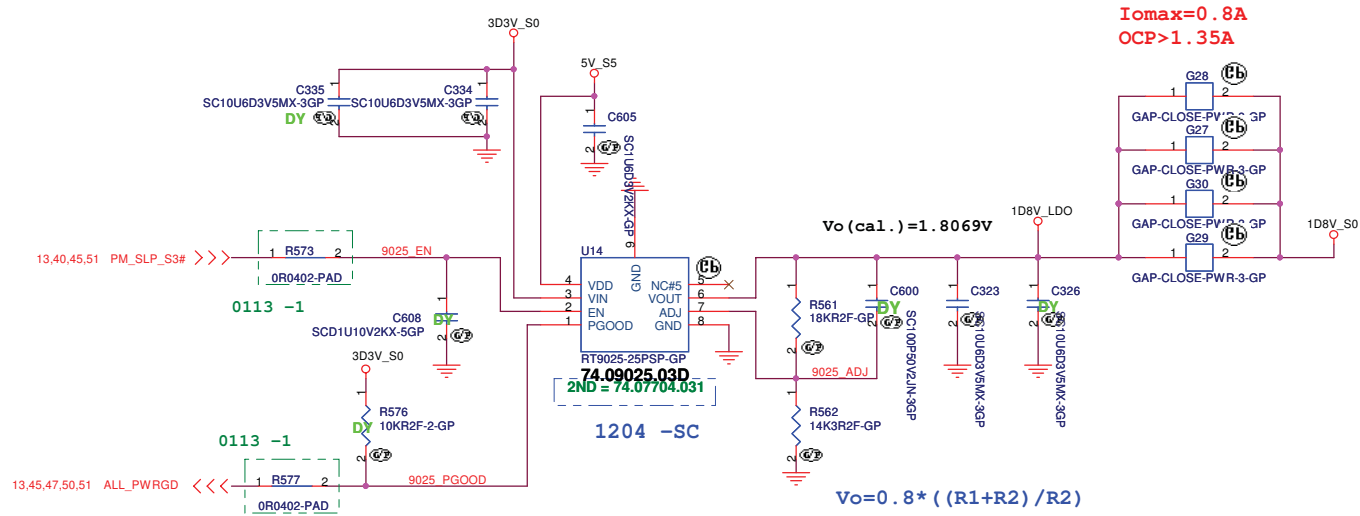


because of 1.05V_S0 and 1.05V_VTT combin together
use PM_SLP_S3# Enable 1.05V power

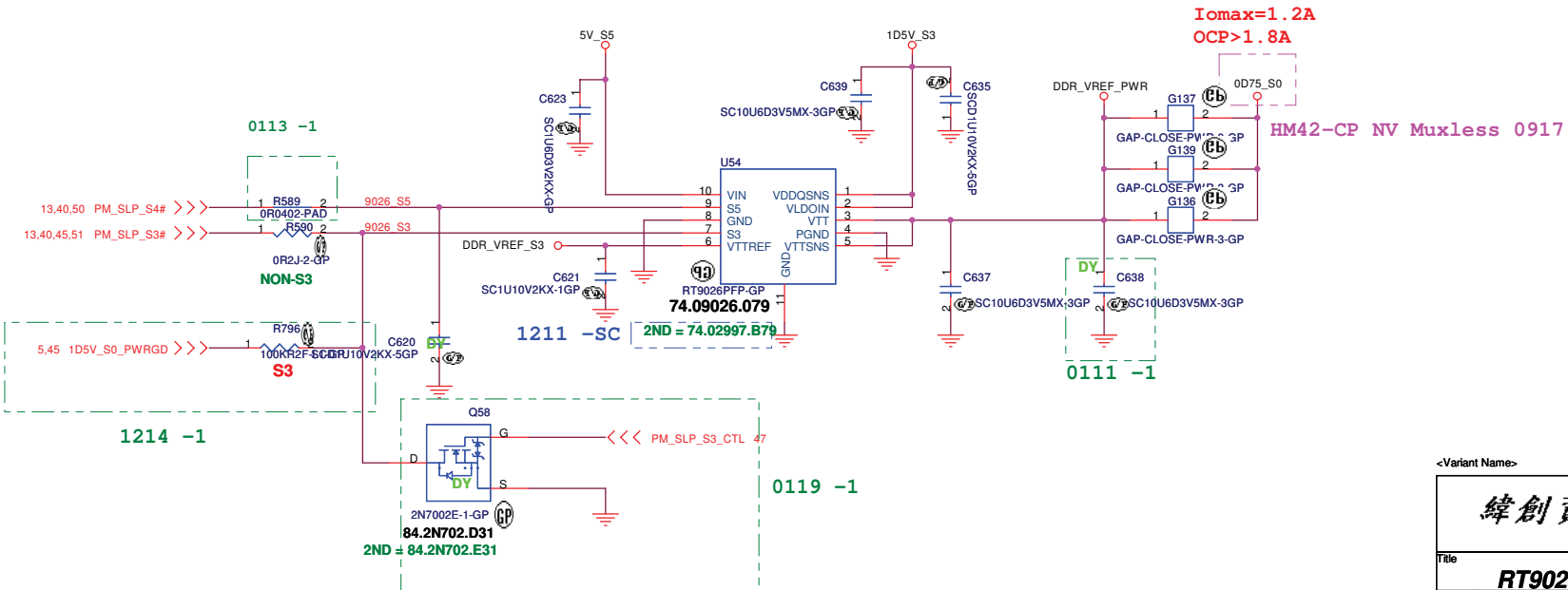


RT9025 for 1D8V_S0

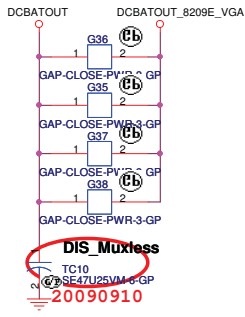
20090915



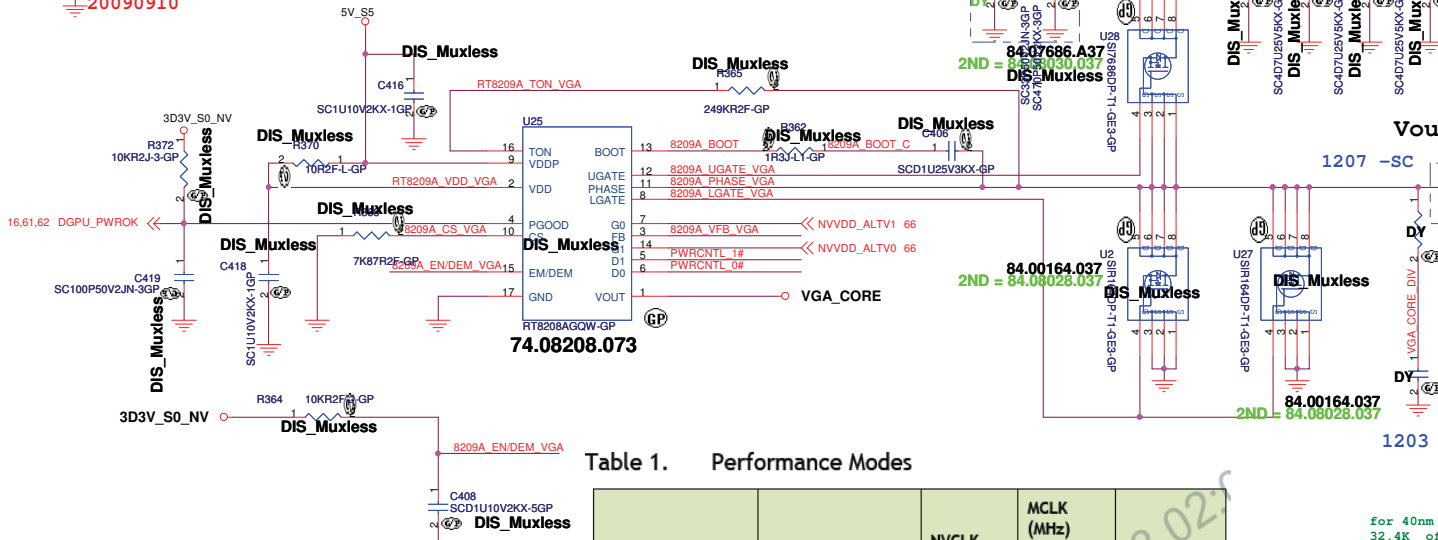
RT9026 for 0D75V_S0



<Variant Name>		
緯創資通 Wistron Corporation		
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File		
RT9025 1D8V/RT9026 0D75		
Size	Document Number	Rev
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RT8208A for VGA



RT8208A		RT8208B		Output Voltage Equation
G0	G1	G0	G1	
0	0	1	1	$V_{OUT} = \frac{R1+R2}{R2} \times 0.75$
1	0	0	1	$V_{OUT} = \frac{R1+(R2/R3)}{(R2/R3)} \times 0.75$
0	1	1	0	$V_{OUT} = \frac{R1+(R2/R4)}{(R2/R4)} \times 0.75$
1	1	0	0	$V_{OUT} = \frac{R1+(R2/R3/R4)}{(R2/R3/R4)} \times 0.75$

$V_{out} = 0.75V * (R1+R2) / R2$
 2nd = 68.83610.20C
 2nd = 68.83610.20A

I_{omax}=27A
 OCP>40A
 VGA_CORE

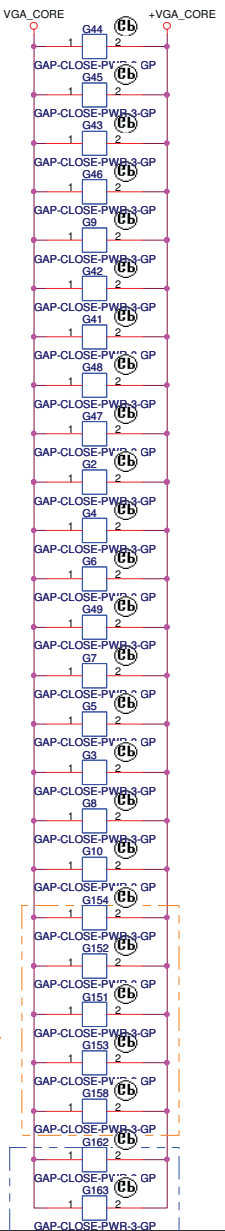


Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVDD
Performance (P0)	N11P-GE1	575	790	0.95 V
Performance (P0)	N11P-LP1	475	700	0.85 V
Balanced (P8)	N11P-GE1, N11P-LP1	405	324	0.85 V
Battery (P12)	N11P-GE1, N11P-LP1	135	135	0.80 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVDD
Performance (P0)	N11M-OP1	625	790	1.03 V
Performance (P0)	N11M-OP2	525	700	0.86 V
Balanced (P8)	N11M-OP1, N11M-OP2	405	405	0.85 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVDD
Performance (P0)	N11M-GE1	625	790	1.03 V
Performance (P0)	N11M-LP1	525	700	0.86 V
Balanced (P8)	N11M-GE1, N11M-LP1	405	405	0.85 V
Battery (P12)	N11M-GE1, N11M-LP1	135	135	0.85 V

N11P-GE1
 For 40nm GPU the NVDD and GPIO5 (NVVDD_ALT0) /GPIO6 (NVVDD_ALT1) relationship

GPIO6/NVVDD_ALT1	GPIO5/NVVDD_ALT0	NVDD
0	0	0.8
0	1	0.85
1	0	0.95

N11M-GE1/N11M-OP1
 For 40nm GPU the NVDD and GPIO5 (NVVDD_ALT0) /GPIO6 (NVVDD_ALT1) relationship

GPIO6/NVVDD_ALT1	GPIO5/NVVDD_ALT0	NVDD
0	1	0.85
1	0	1.03

cherry request 9 pcs Gap, because of space concern, only add 5pcs Cap.

UMA

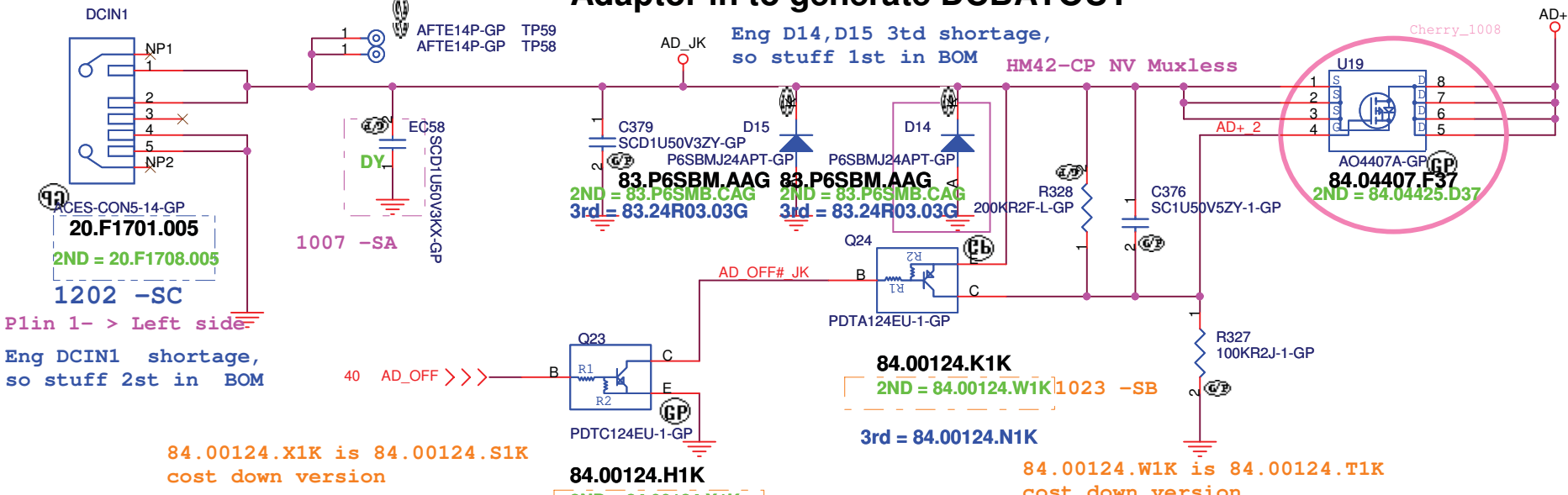
緯創資通 **Wistron Corporation**
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Title: **RT8209A VGA CORE**

Size Custom Document Number **HM42-CP** Rev

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Adaptor in to generate DCBATOUT

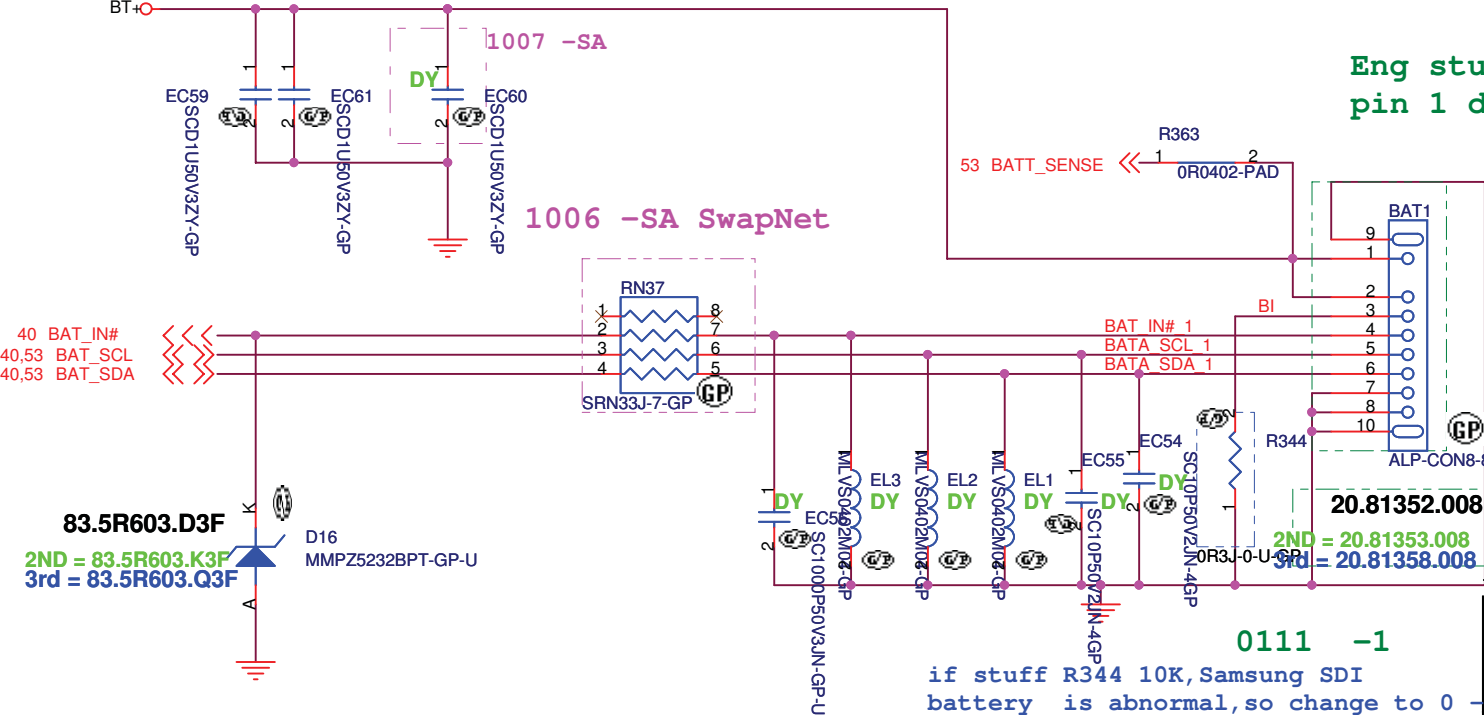


Plin 1- > Left side
Eng DCIN1 shortage, so stuff 2st in BOM

84.00124.X1K is 84.00124.S1K cost down version

84.00124.W1K is 84.00124.T1K cost down version

BATTERY CONNECTOR



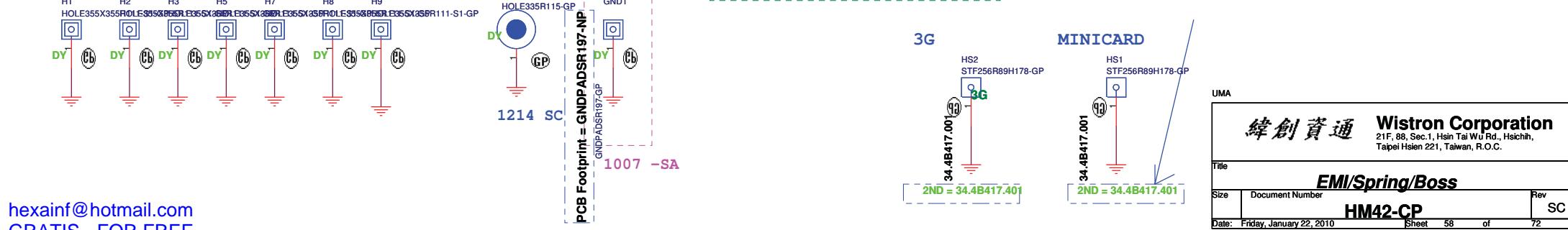
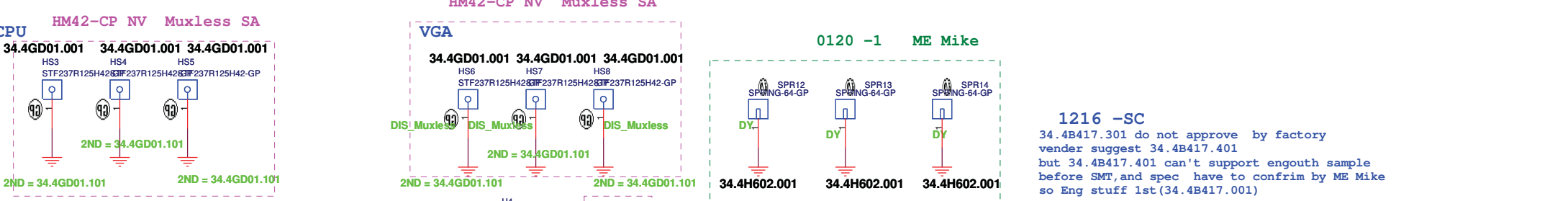
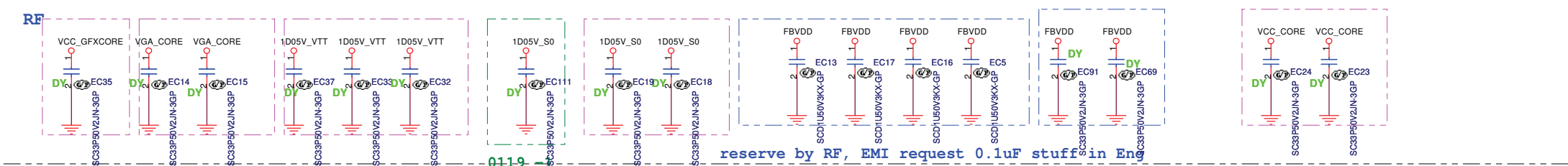
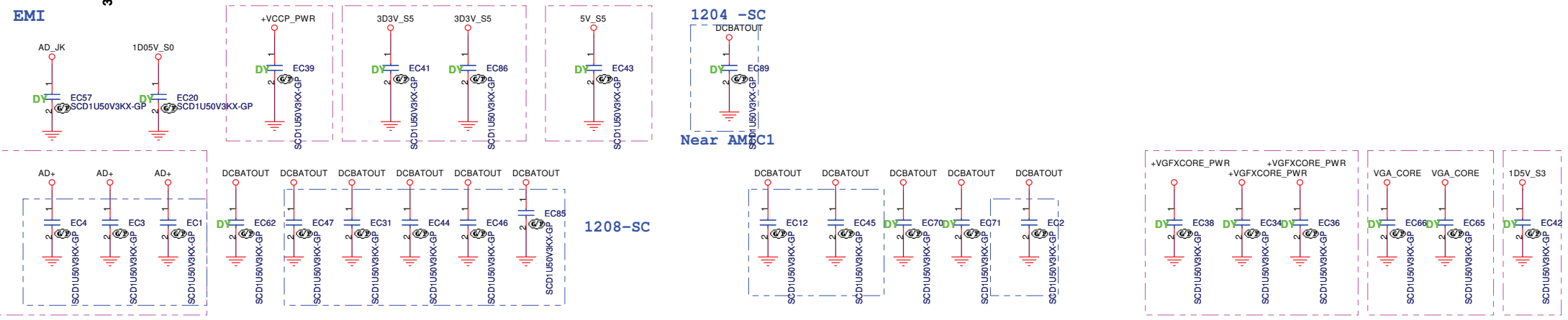
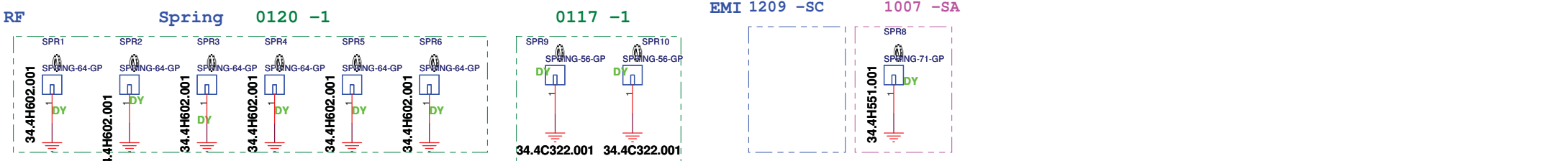
Pin Definition:

1	GND	Batt-, Battery Negative Terminal
2	GND	Batt-, Battery Negative Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	TH	Connect to Resistor to GND (10kΩ to GND)
6	BI	System present pin, low active
7	BATT+	Batt+, Battery Positive Terminal
8	BATT+	Batt+, Battery Positive Terminal

<Core Design>

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Title		
AD/BATT CONN		
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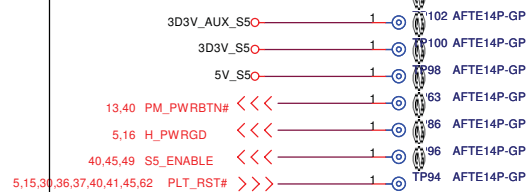
34.4B417.301 do not approve by factory
 vender suggest 34.4B417.401
 but 34.4B417.401 can't support engouth sample
 before SMT, and spec have to confirm by ME Mike
 so Eng stuff 1st(34.4B417.001)

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		EM1/Spring/Boss	
Title	Document Number		Rev
Size	Date: Friday, January 22, 2010		Sheet 58 of 72
HM42-CP		34.4B417.001 2ND = 34.4B417.401	
		34.4B417.001 2ND = 34.4B417.401	

Check test point

~~delete 3D3V_S0 test point~~



Test Point 放在 Dimm Door 打開可量測處

<Variant Name>

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Title

AFTE TP

Size

Document Number

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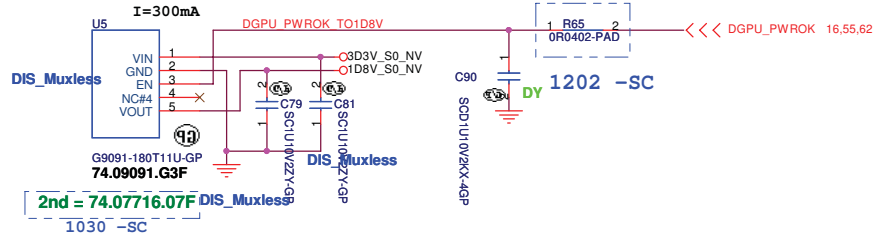
Rev

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Date: Friday, January 22, 2010

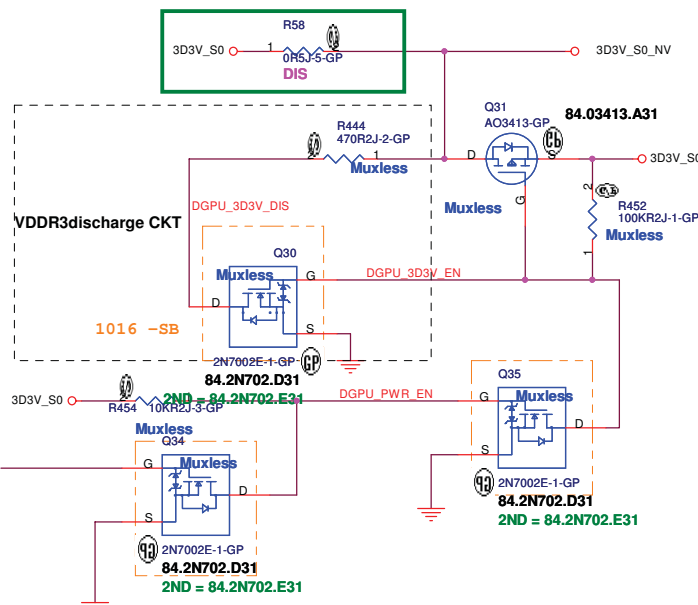
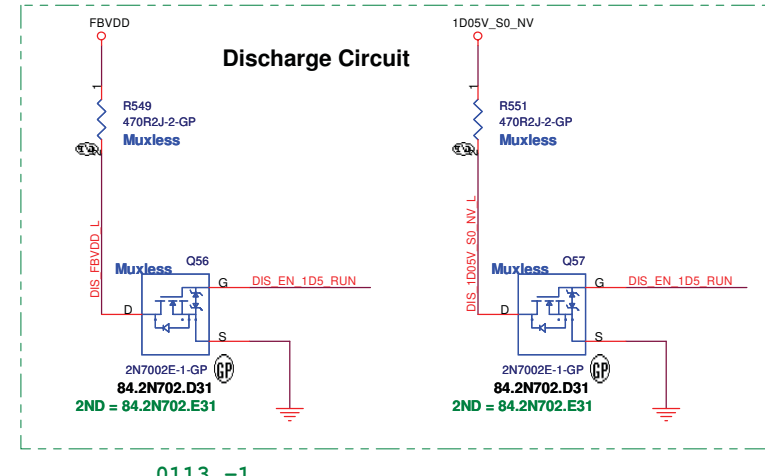
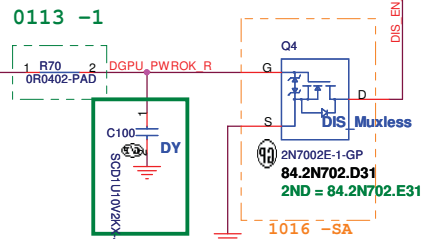
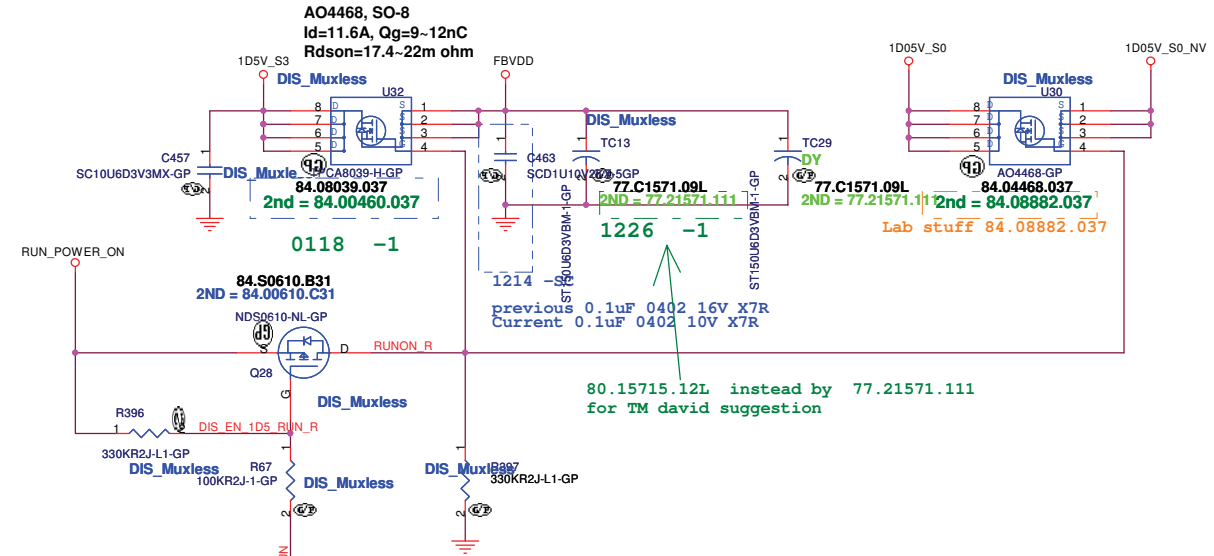
Sheet 59 of 72

+3VS to 1.8V Transfer



+1.5V to FBVDD Transfer

+1.05V to +1.05V_NV Transfer



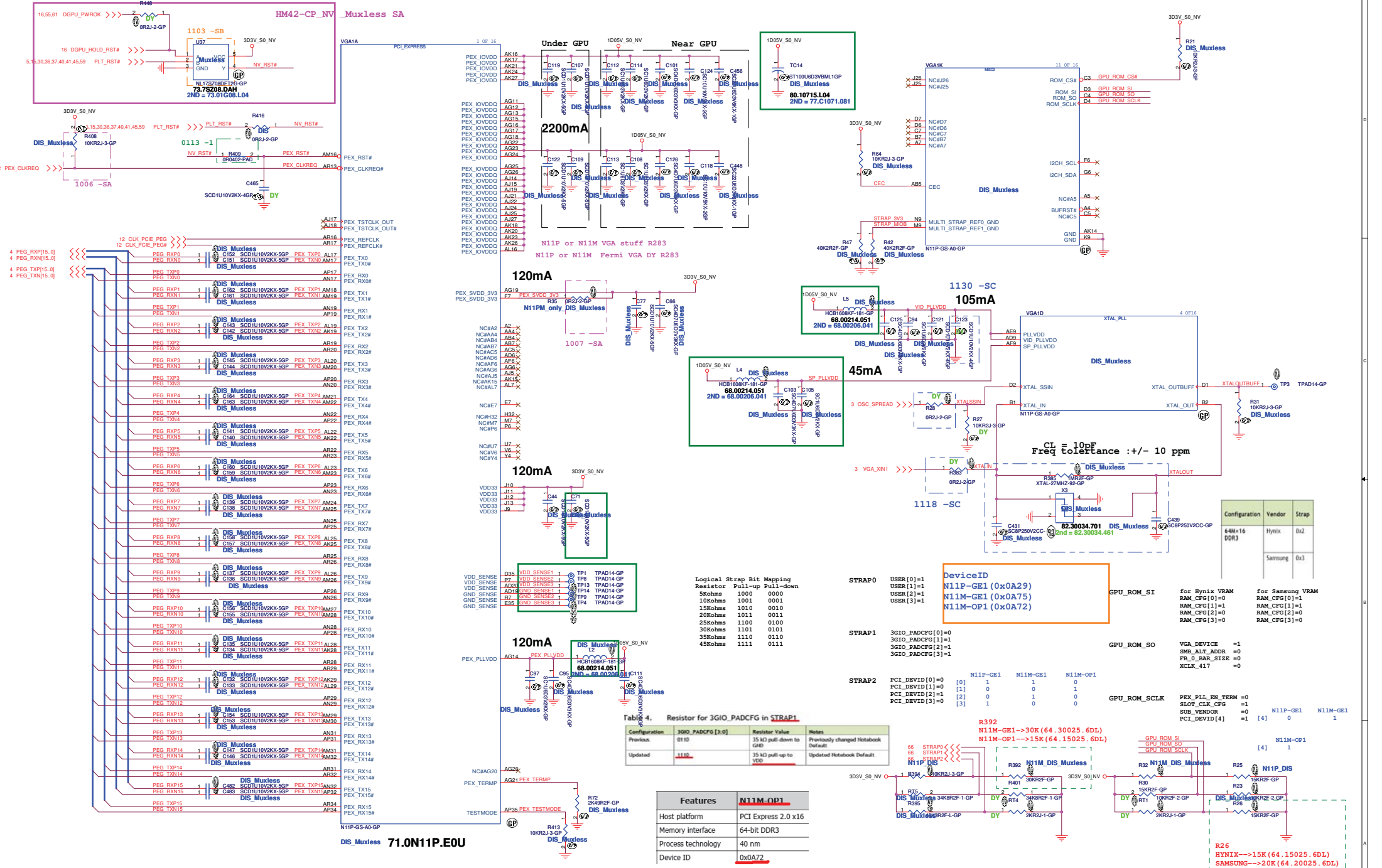
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Title: **NV power**

Size A3	Document Number	Rev
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VGA 1 N11P-GE1 A3-->71.0N11P.GOU,
N11M-GE1-B -A3 -> 71.0N11M.EOU

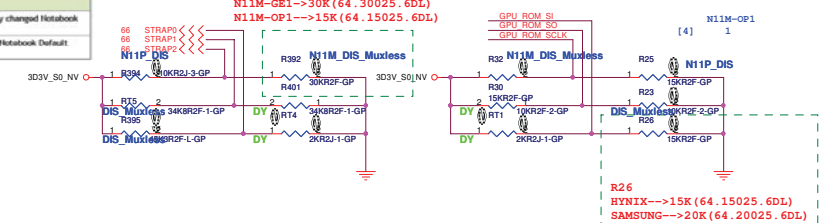
Table 4. Resistor for 3GIO_PADCFG in STRAP1

Configuration	3GIO_PADCFG [3-0]	Resistor Value	Notes
Previous	0110	35 kΩ pull down to GND	Previously changed Notebook Default
Updated	1110	35 kΩ pull up to VDD	Updated Notebook Default

Features	N11M-OP1
Host platform	PCI Express 2.0 x16
Memory interface	64-bit DDR3
Process technology	40 nm
Device ID	0x0A72

DeviceID

DeviceID	GPU_ROM_S1	GPU_ROM_S0	GPU_ROM_SCLK
N11P-GE1 (0x0A29)	for Rynix VRAM	VGA_DEVICE = 1	PEX_PLI_EN_TERM = 0
N11M-GE1 (0x0A75)	RAM_CFG[0]=0	SMB_ALZ_ADDR = 0	SLOT_CLK_CFG = 1
N11M-OP1 (0x0A72)	RAM_CFG[0]=1	FB_0_SAR_SIZE = 0	SUB_VENDOR = 0
	RAM_CFG[1]=1	XCLX 417	PCI_DEVID[4] = 1
	RAM_CFG[2]=0		
	RAM_CFG[3]=0		



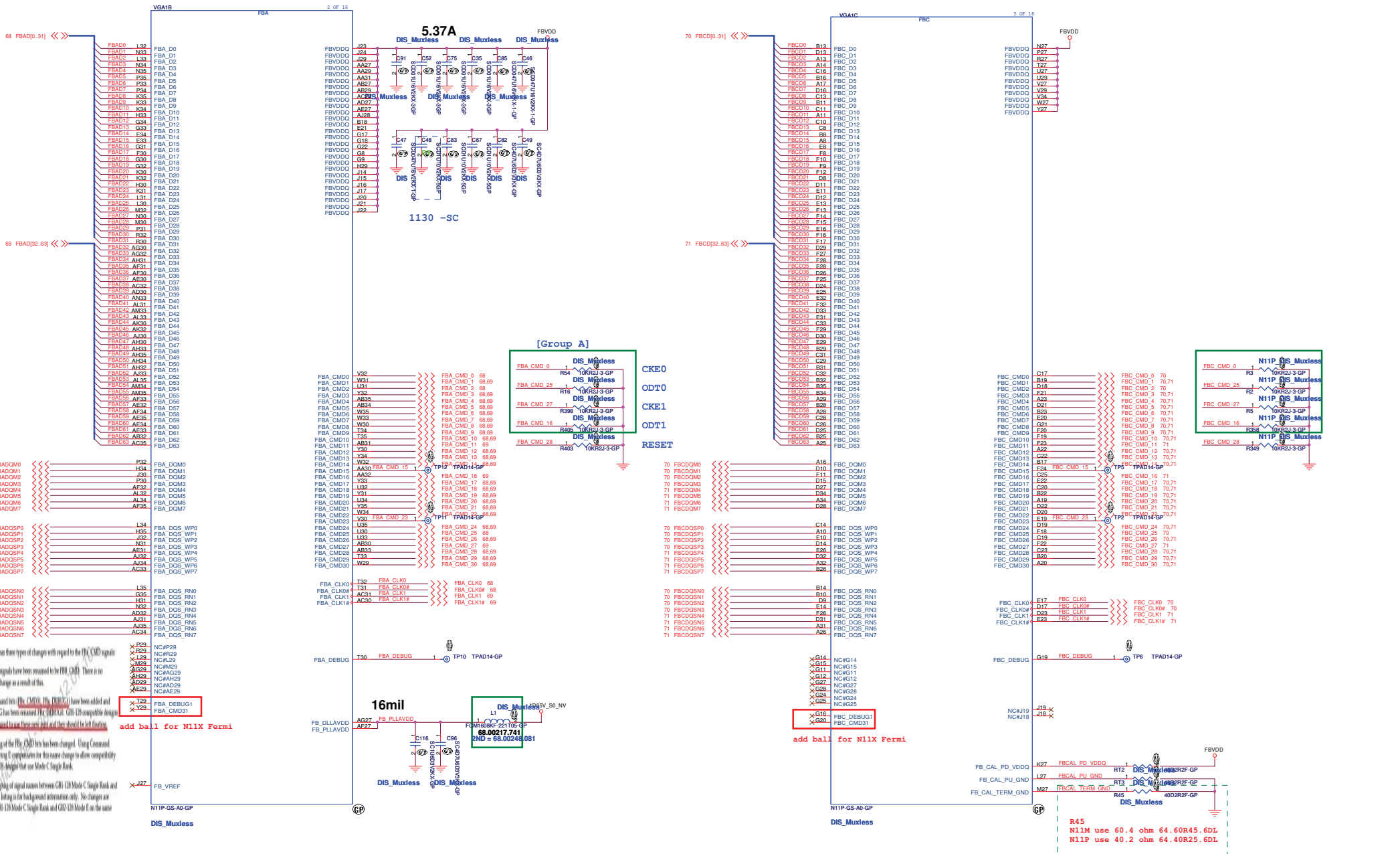
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Chip	N11P-GS1-A2	N11P-GE1-A2	N11P-LP1-A2
Device ID	0x0A35	0x0A75	0x0A28

Chip	N11M-GS1-B-A2	N11M-GE1-B-A2
Device ID	0x0A35	0x0A75

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File: N11P(1/6) PEG
Size: Document Number
Date: Friday, January 22, 2010



- The GR1-128 package has three types of changes with regard to the FB_CMD signals
1. FB_CMD signals have been re-assigned to be FB_CMD. There is no functional change as a result of this.
 2. Extra command bits (FB_CMD10, FB_CMD11, FB_CMD12) have been added and the FB_CMD0 has been re-assigned to be FB_CMD1. GR1-128 compatible design should maintain these signals and they should be left floating.
 3. The ordering of the FB_CMD bits has been changed. Using Command Mode Mapping 1, compatibility for this name change to allow compatibility with GR1-128 design that use Mode C Single Rank.
- Table 1 shows the mapping of signal names between GR1-128 Mode C Single Rank and GR1-128 Mode E. This listing is for background information only. No changes are required to support GR1-128 Mode C Single Rank and GR1-128 Mode E on the same design.

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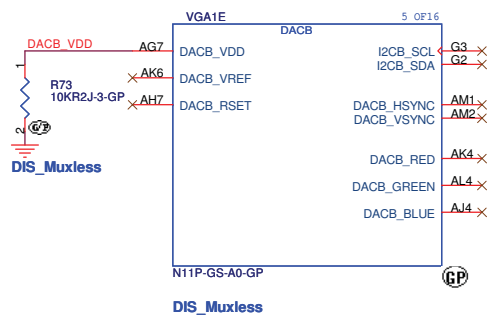
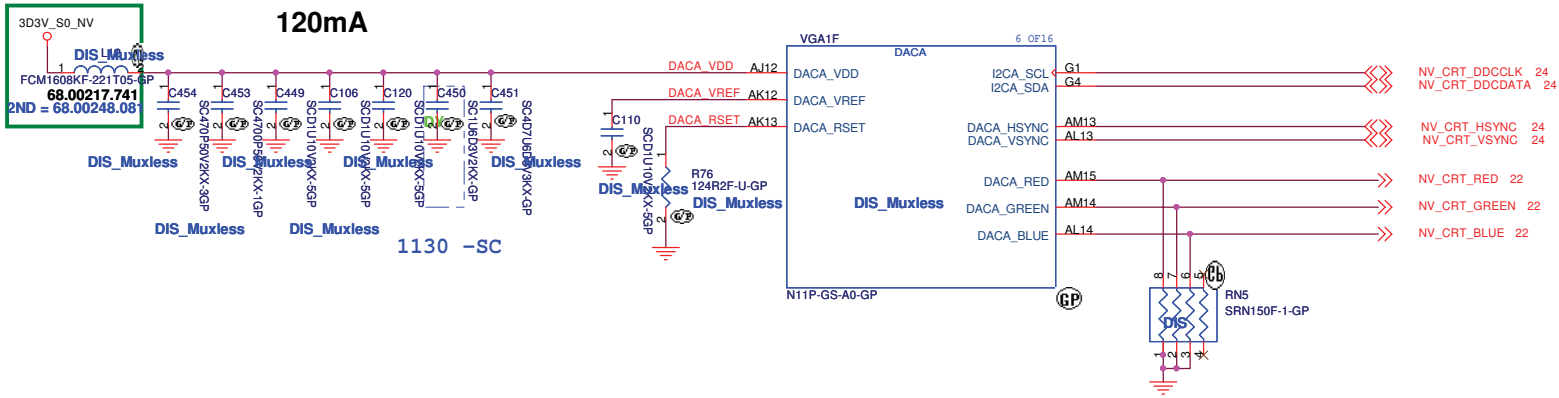
UMA

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File: **N11P(2/6) MEMO**

Size: A2 Document Number: **HM42-COPY** Rev: SC

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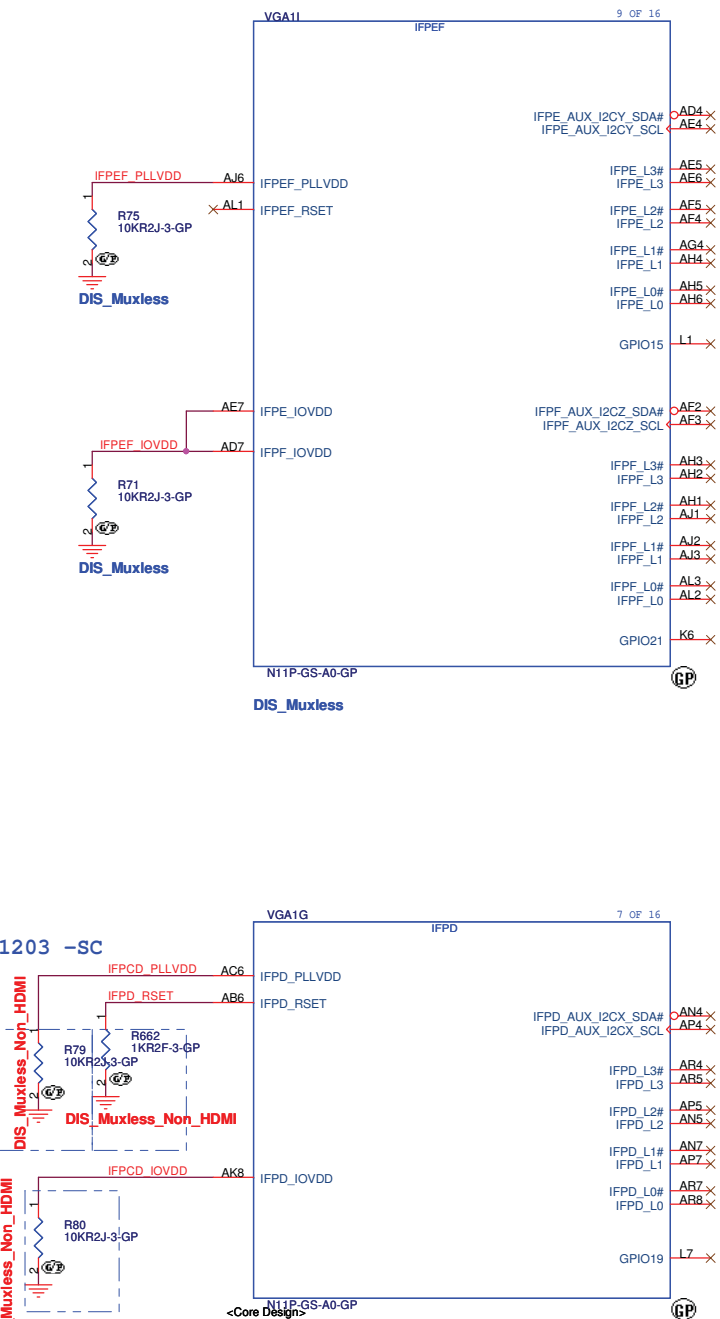
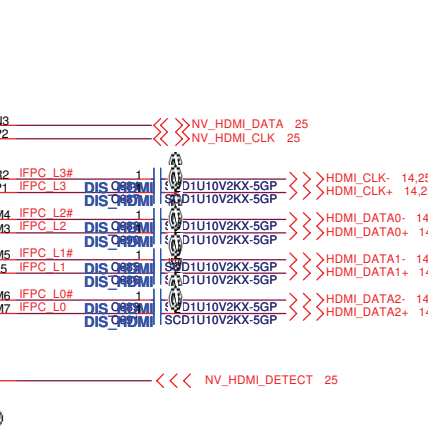
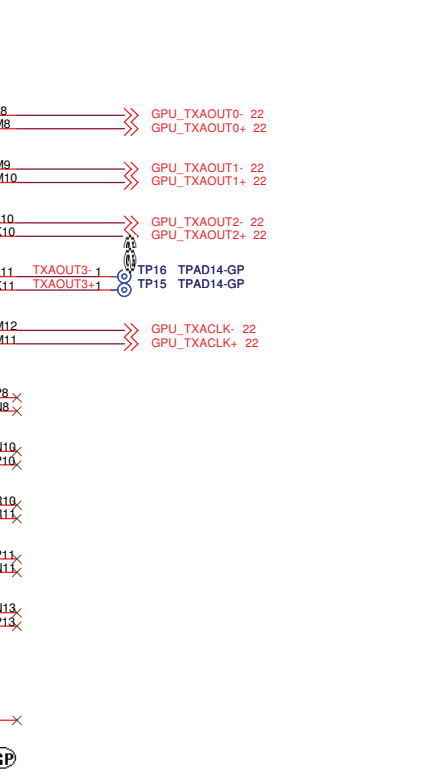
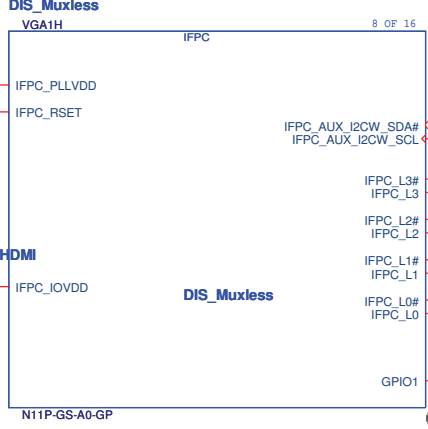
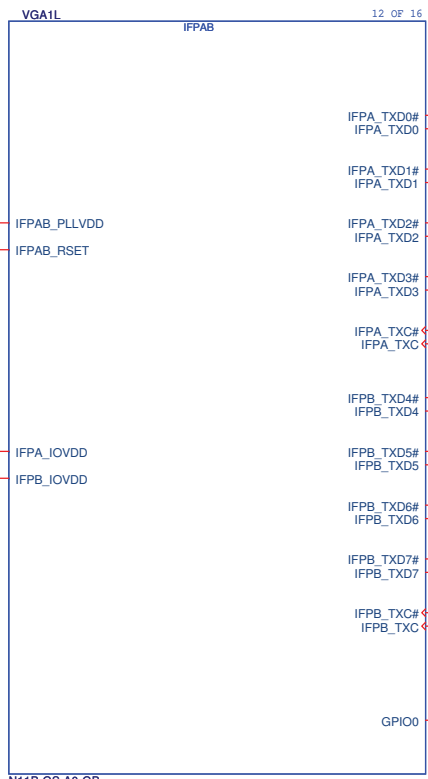
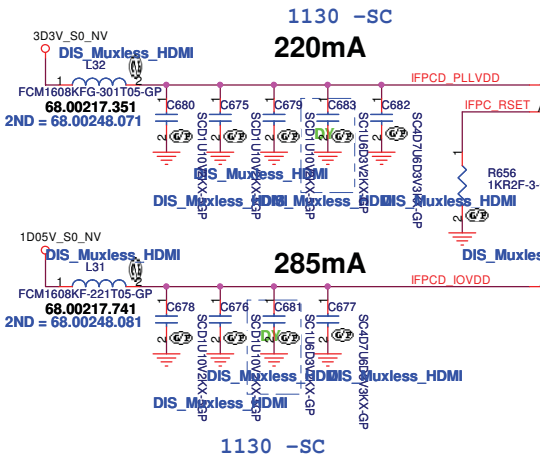
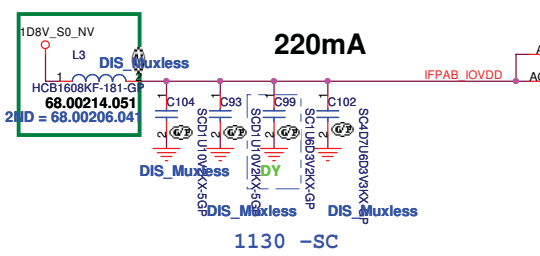
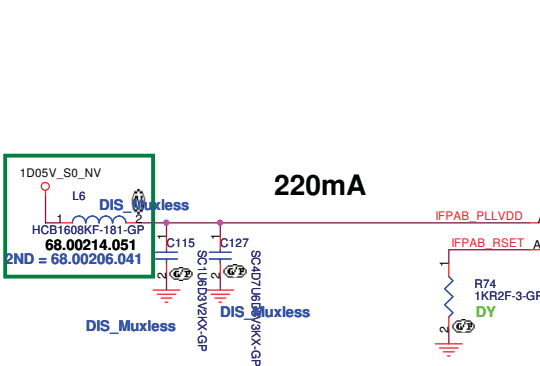


Discrete N11M

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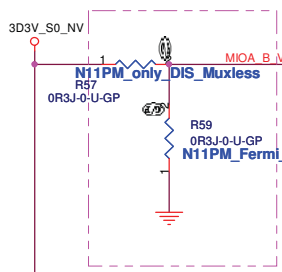
Title: **N11P(3/6) DAC**

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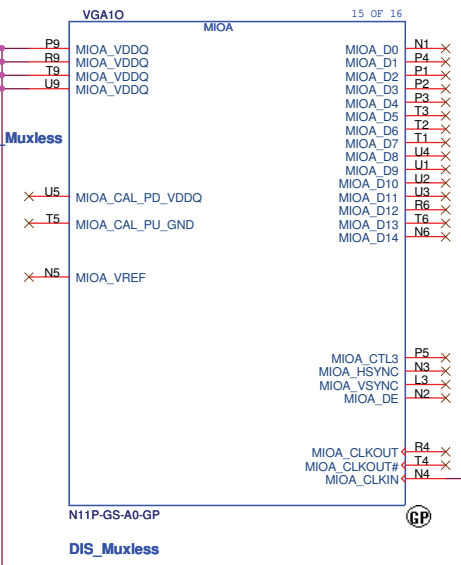
<Core Design>
DIS Muxless
緯創資通 Wistron Corporation
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Title: N11P(4/6)
Size A3 Document Number: HM42-CP Rev SC
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120mA

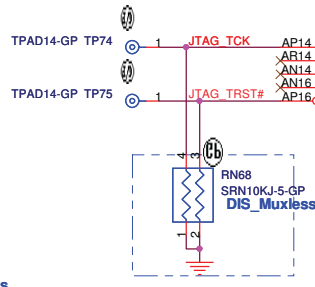
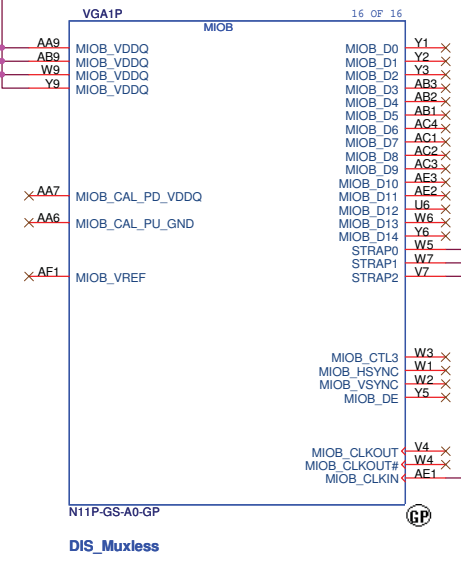
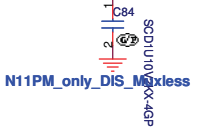


1006 -SA

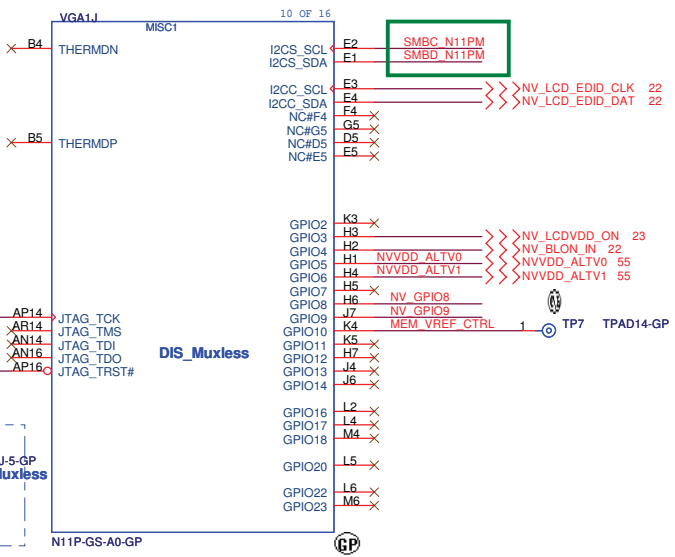
N11P or N11M VGA stuff R277
N11P or N11M Fermi VGA stuff R282



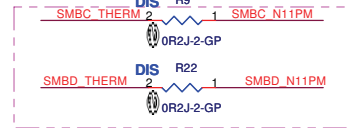
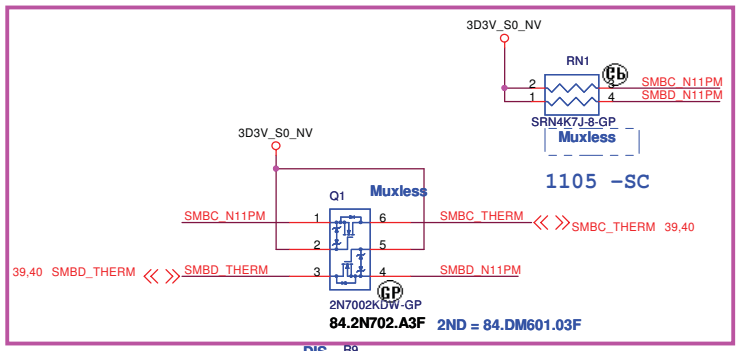
120mA



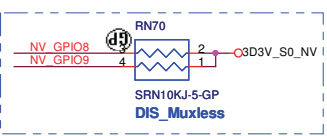
1202 -SC



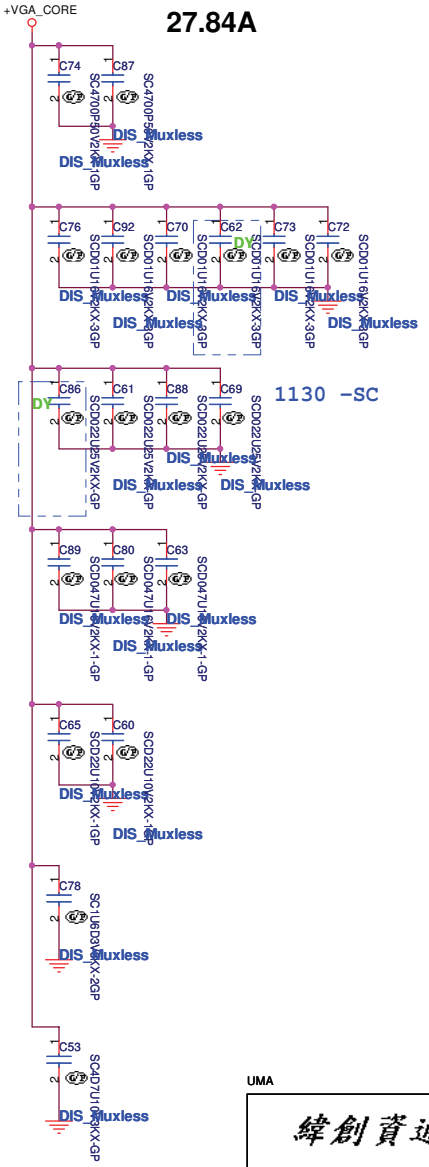
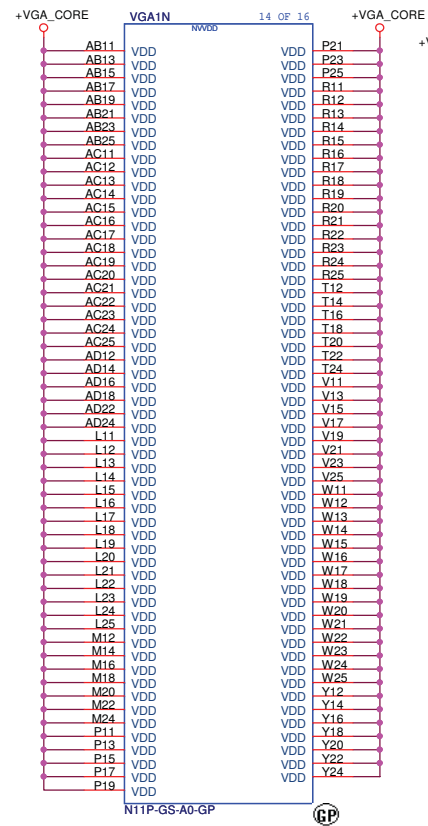
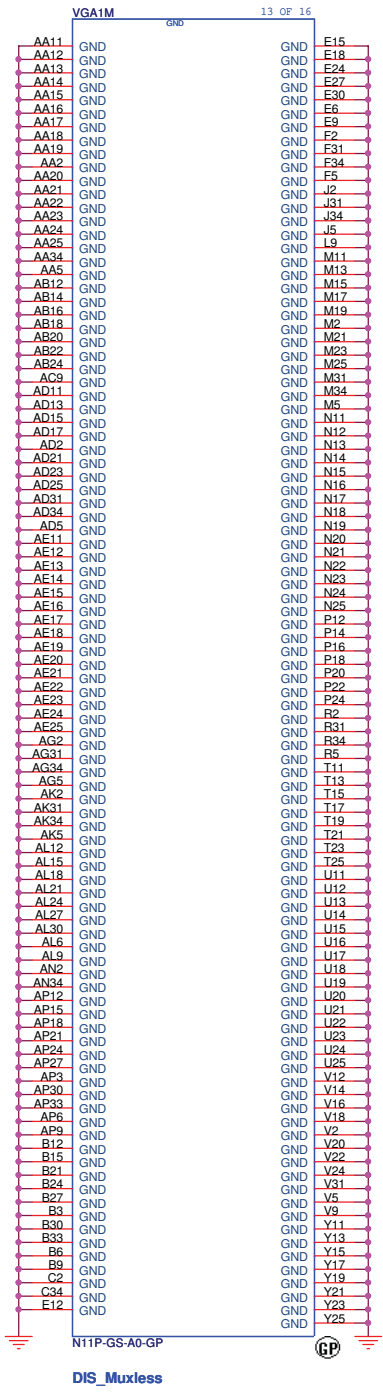
HM42-CP NV Muxless SA 0916



HM42-CP NV Muxless SA 0923



1202 -SC



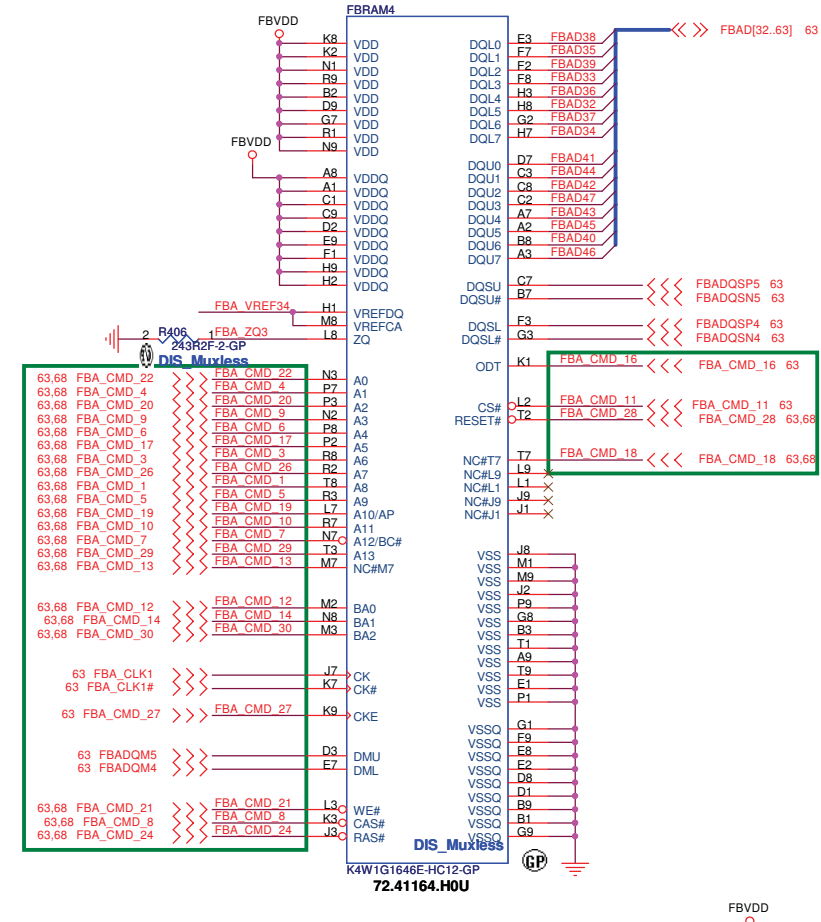
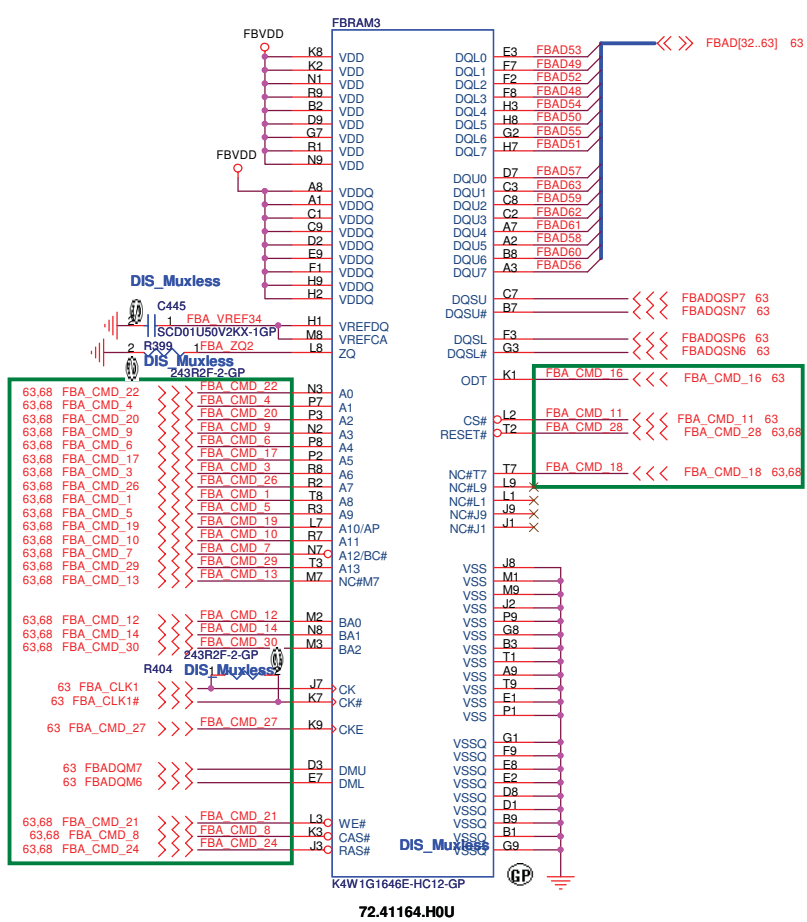
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 Taipei Hsien 221, Taiwan, R.O.C.

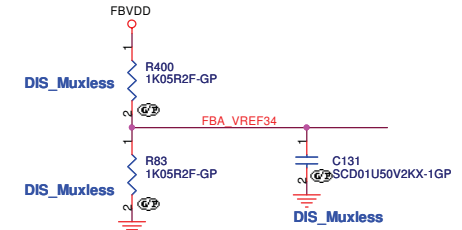
Title **N11P(6/6) POWER**

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DDR3



SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



HM42-CP

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Title: **VRAM(2/4)**

Size: A3 Document Number: **HM42-CP** Rev: **SC**

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3) Samsung VRAM FBRAM1~8 PN:VR.1GB0B.006

Hynix VRAM FBRAM1~8 PN:VR.1GB0G.004

4) VGA 1 N11P-GE1 A3->71.0N11P.G0U,
N11M-GE1-B -A3 -> 71.0N11M.E0U
N11M-OP1 ->

6) VGA 1 N11P-GE1-> R53 49.9K(64.49925.6DL)
N11M-GE1 -> R53 32.4K(64.32425.6DL)

7) R26 stuff Hynix VRAM : 15K(64.15025.6DL)
Samsung VRAM : 20K(64.20025.6DL)

8) R45 stuff N11M use 60.4 ohm (64.32425.6DL)
N11P use 40.2 ohm (64.40R25.6DL)

9) Muxless SKU stuff R181 2.37K (64.23715.6DL)
UMA SKU Stuff R181 2.4K (64.24015.6DL)

10) N11M OP1 ->R392 15K(64.15025.6DL)
N11M GE1 ->R392 30K(64.30025.6DL)

Mini Card 2nd and 3rd source PN confirm

Card Reader 2nd source confirm

[ECR]

Date	released by	ECR Number
11/22	Anita	R1001240

[Old]
PCH1 PN : 71.0IBEX.A0U

[New]
PCH1 PN : 71.0HM55.00U(KI.G5501.002)

hexainf@hotmail.com
GRATIS - FOR FREE

[lab -SB]

2nd -> UMA (S01G)

1st -> Diserete N11P Hynix(S02G)
1st +3rd -> Diserete N11M Hynix(S03G)
2nd +4th -> Diserete N11M Samsung(S04G)
1st -> Diserete N11P Samsung (S05G)
2nd -> N11M Hynix_support Optimus (S06G)

[Eng -SC]

2nd -> UMA Non 3G (55.4GY01.S07G)

1st -> Diserete N11P Hynix_3G(55.4GZ01.S03G)
1st +3rd -> Diserete N11M Hynix_3G(55.4GY01.S09G)
2nd +4th -> Diserete N11M Samsung_Non 3G(55.4GZ01.S02G)
1st + 5th -> Diserete N11P Samsung_3G(55.4GY01.S10G)
1st +3 rd -> UMA Non 3G Non HDMI (55.4GW01.S01G)

[PD -1]

UMA 3G (55.4GY01.M01G)

Diserete N11P Hynix_3G(55.4GY01.M02G) => 1st

Diserete N11P Hynix_Non 3G(55.4GY01.M03G) => 2nd

UMA Non 3G (55.4GY01.M04G)

Diserete N11M Hynix_3G(55.4GY01.M05G)

Diserete N11P Samsung_3G(55.4GY01.M06G) =>1 st

Diserete N11M Samsung_Non 3G(55.4GY01.M07G)

[PD action]

qual TPCN1 2nd source(20.K0296.006)

qual KB1 2nd source(20.K0382.026)

qual HDMI 2nd and 3rd

qual ODD1 3rd source(62.10065.E01)

qual PWRCN1 2nd and 3rd

qual RTC1 4th source

qual BT1 2nd and 3 source

qual U51 and U15 2nd source
qual TC13 2nd source(77.21571.111)
qual U32 2nd source
Qual HS1,HS2 2nd: 34.4B417.401

UMA

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Modify History			
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