

Compal Confidential

KBLG0/NBLG0 Schematics Document

AMD Puma (JV40-PU) : Griffin Processor with RS780MN/SB700/M92-M2 XT
Tigris (JV40-TR) : Caspian Processor with RS880M/SB710/M92-M2 XT

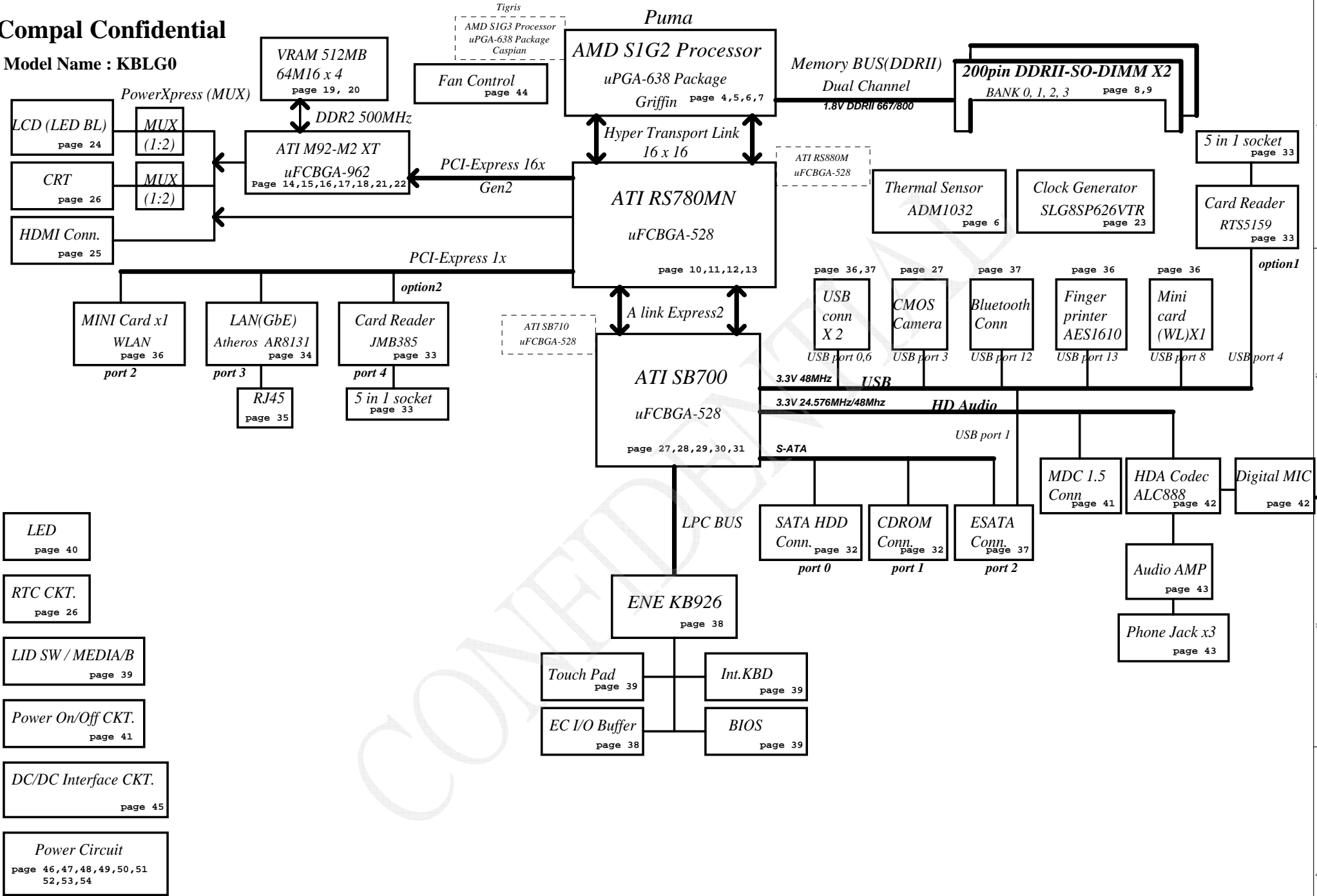
2009-03-11

REV:1.0

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Model Name : KBLG0



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)DN	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (CPU)	1001 100X b	98H
			GMT G781-1 (GPU)	1001 101X b	9AH
			SB-Temp Sensor		9CH

SB700 SM Bus 0 address

Device	Address	HEX	Device	Address
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2	New card	
DDR DIMM1	1001 000Xb	90		
DDR DIMM2	1001 010Xb	94		
Mini card				

EC SM Bus2 address

SB700 SM Bus 1 address

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

BTO Option Table

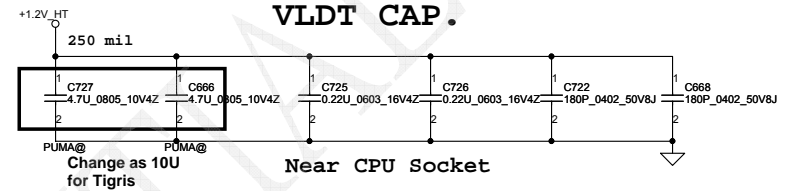
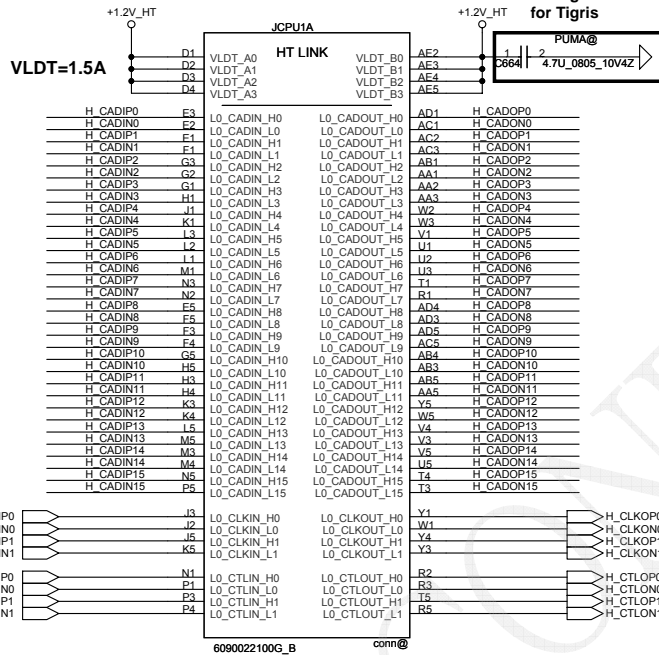
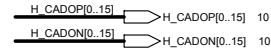
BTO Item	BOM Structure
Discrete	VGA@
UMA	UMA@
M92-M2 XT	M92@
VRAM STRAP	VRAM@
LAN 8121	8121@
LAN 8131	8131@
HDT debug	HDT@
JMB385 CR	JMB385@
RTS5159 CR	RTS5159@
FOR PUMA	PUMA@
FOR TIGRIS	TIGRIS@
FOR TEST	UB@

	SB700	SB700	RS780MN	DISPLAY OUTPUT
	PX_GPIO0	PX_GPIO1	PX_GPIO2	
Function Description	dGPU_Reset	dGPU_PWR_Enable	PX Mode Switch	
IGP only mode	X	X	X	
PowerXpress mode	H : Enable	H : Enable	L : IGPU(DC) / H : dGPU(AC)	LVDS / CRT

KB926						
	PX_GPIO1	PX_GPIO2	PX_+3VS	PX_+1.8VS	PX_+VGA_CORE	PX_GPIO2_NB
Function Description	Enable +1.1VS_PX	PX MODE SWITCH	Enable +3VS_DELAY	Enable +1.8VS_PX	Enable +VGA_CORE	Trigger from SB
IGP only mode	X	X	X	X	X	X
PowerXpress mode	H : Enable	Reserved	H : Enable	H : Enable	H : Enable	Reserved

KB926	
	PX_GPIO1_SB
Function Description	Trigger from SB to Enable (PX_GPIO1/PX_+3VS/PX_+1.8VS/PX_+VGA_CORE)
IGP only mode	X
PowerXpress mode	H : Enable

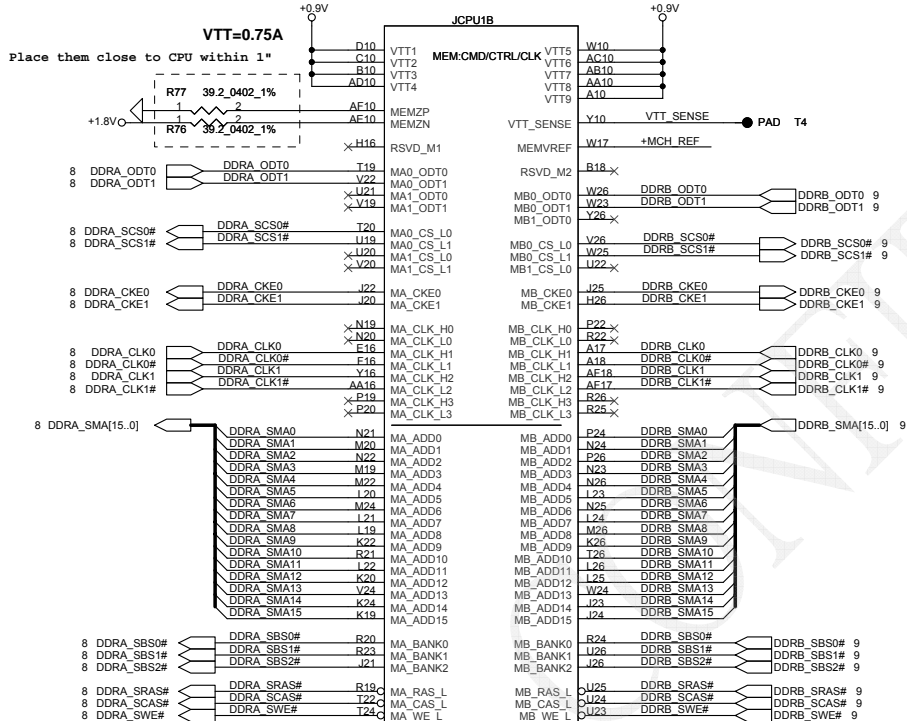
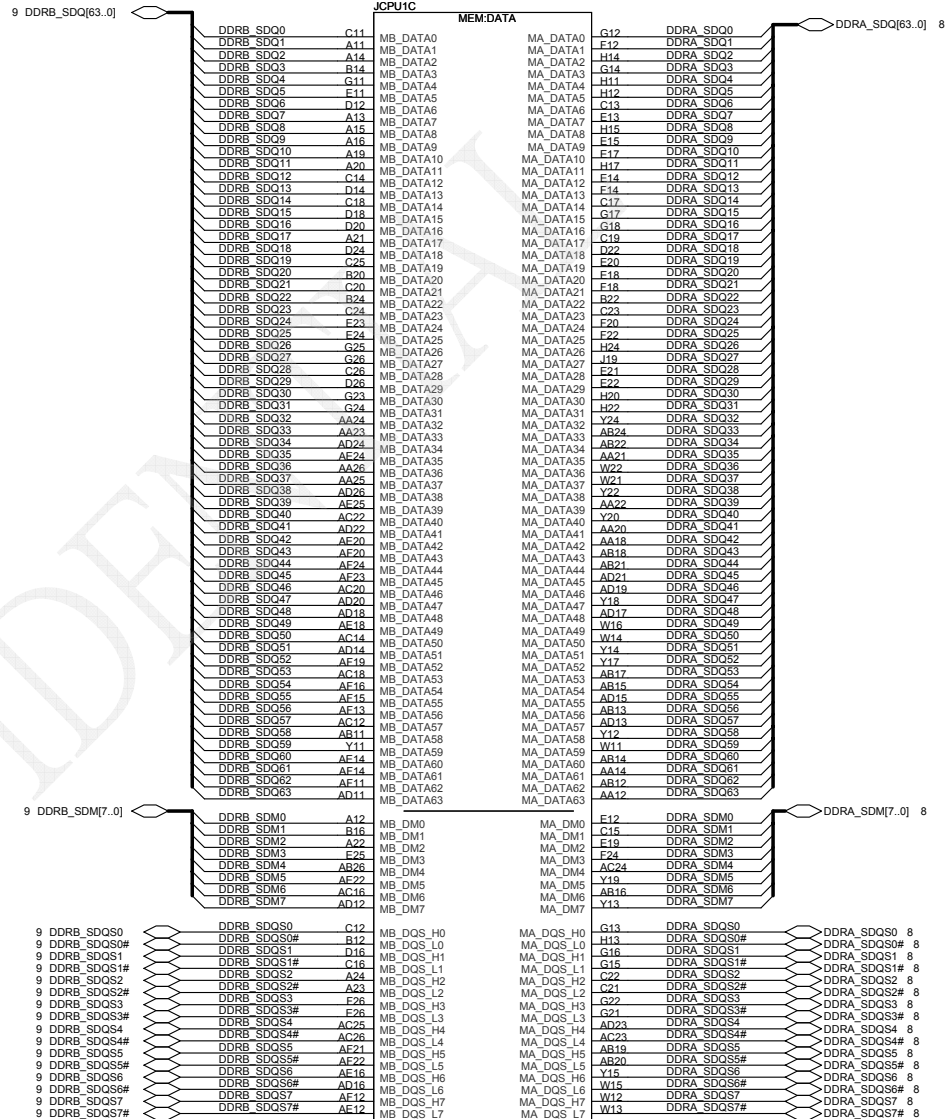
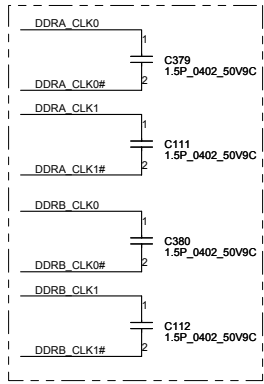
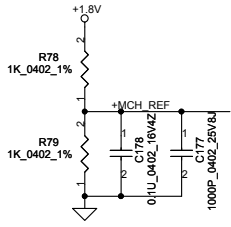
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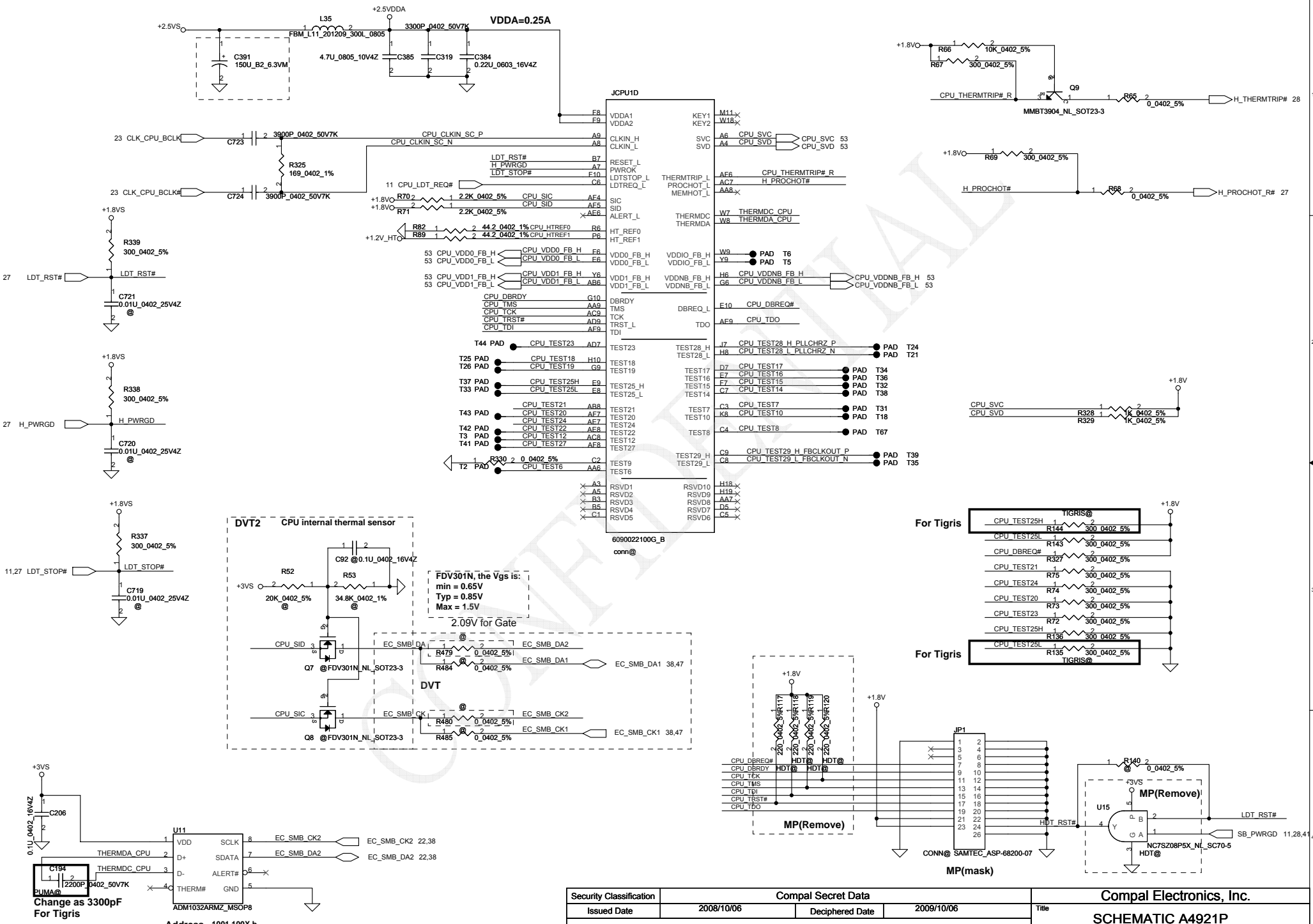
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Processor DDR2 Memory Interface

PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



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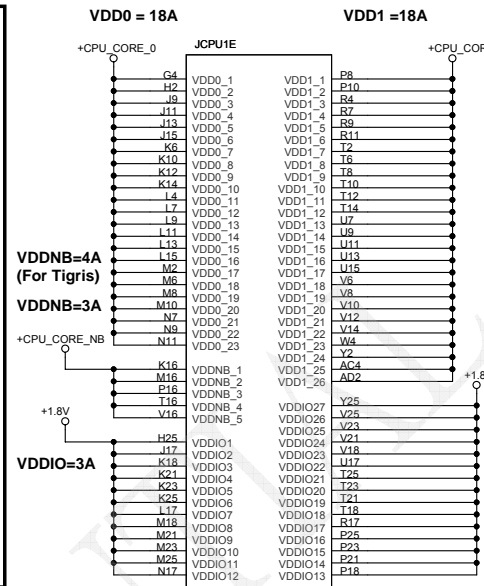
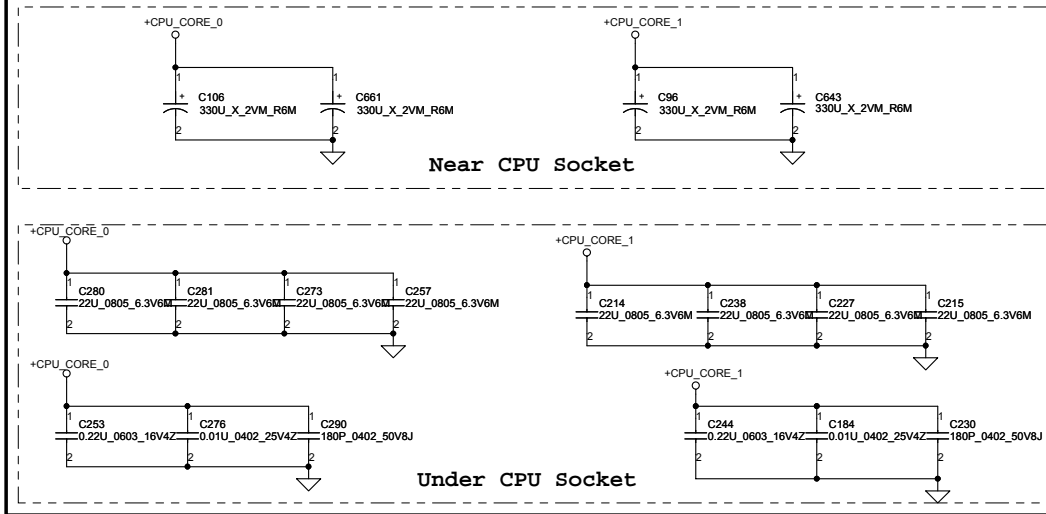


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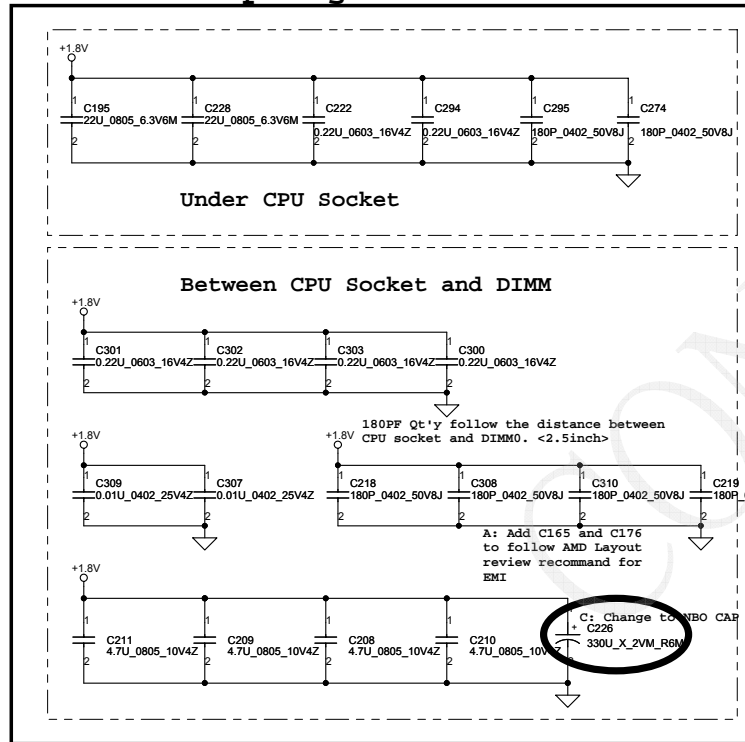
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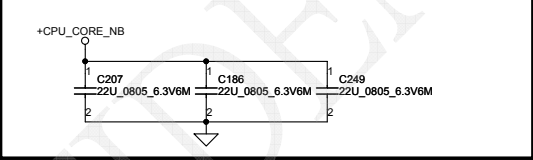
VDD(+CPU_CORE) decoupling.



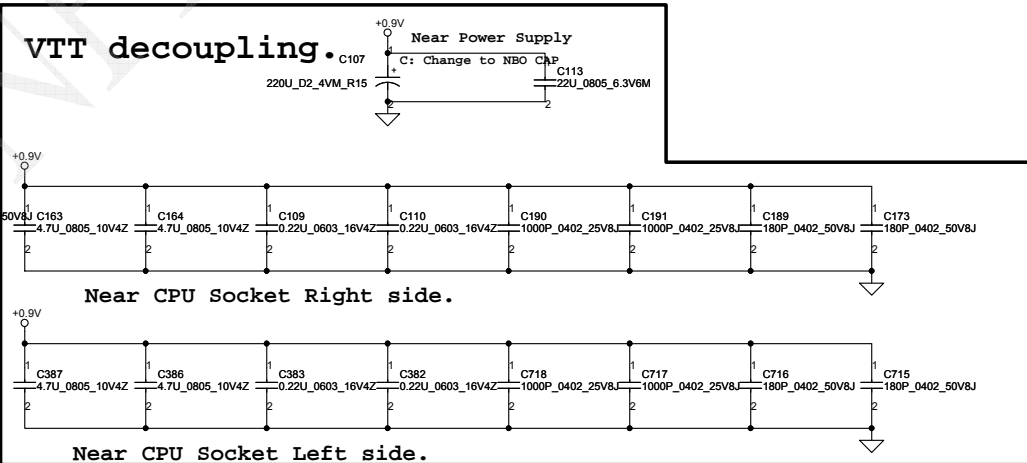
VDDIO decoupling.



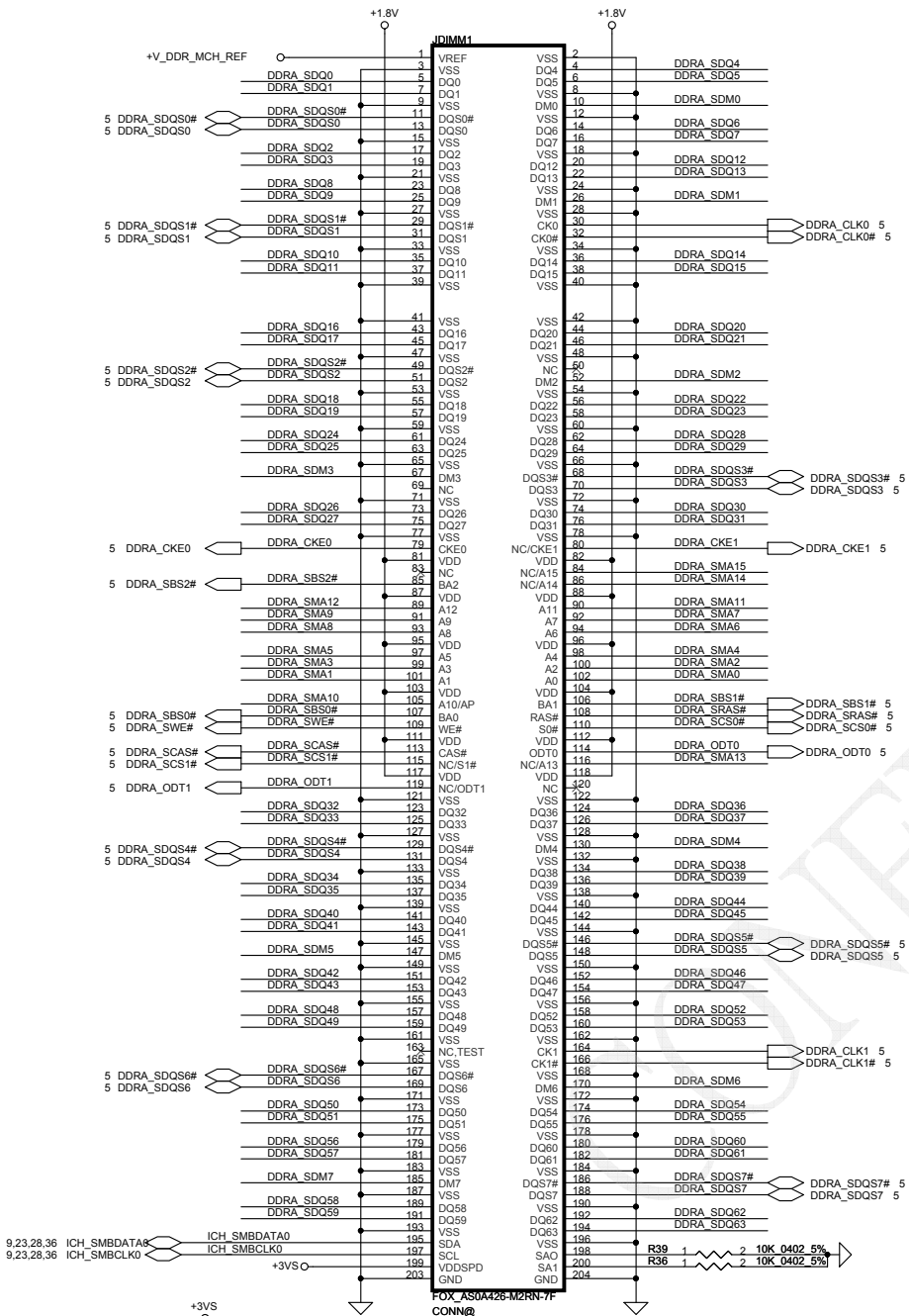
+CPU_CORE_NB decoupling.



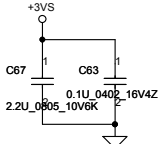
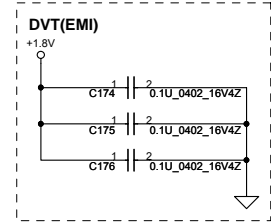
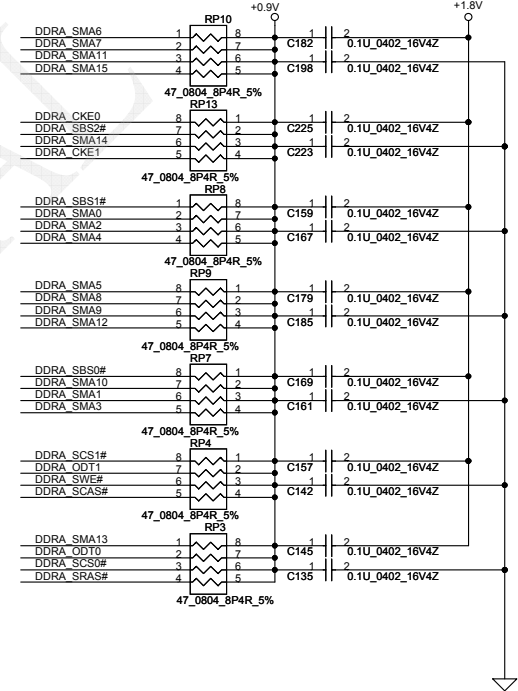
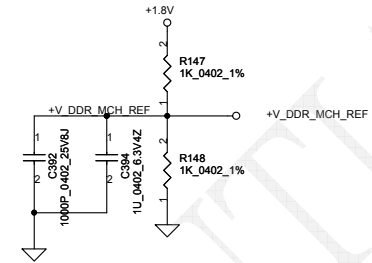
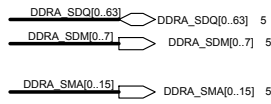
VTT decoupling.



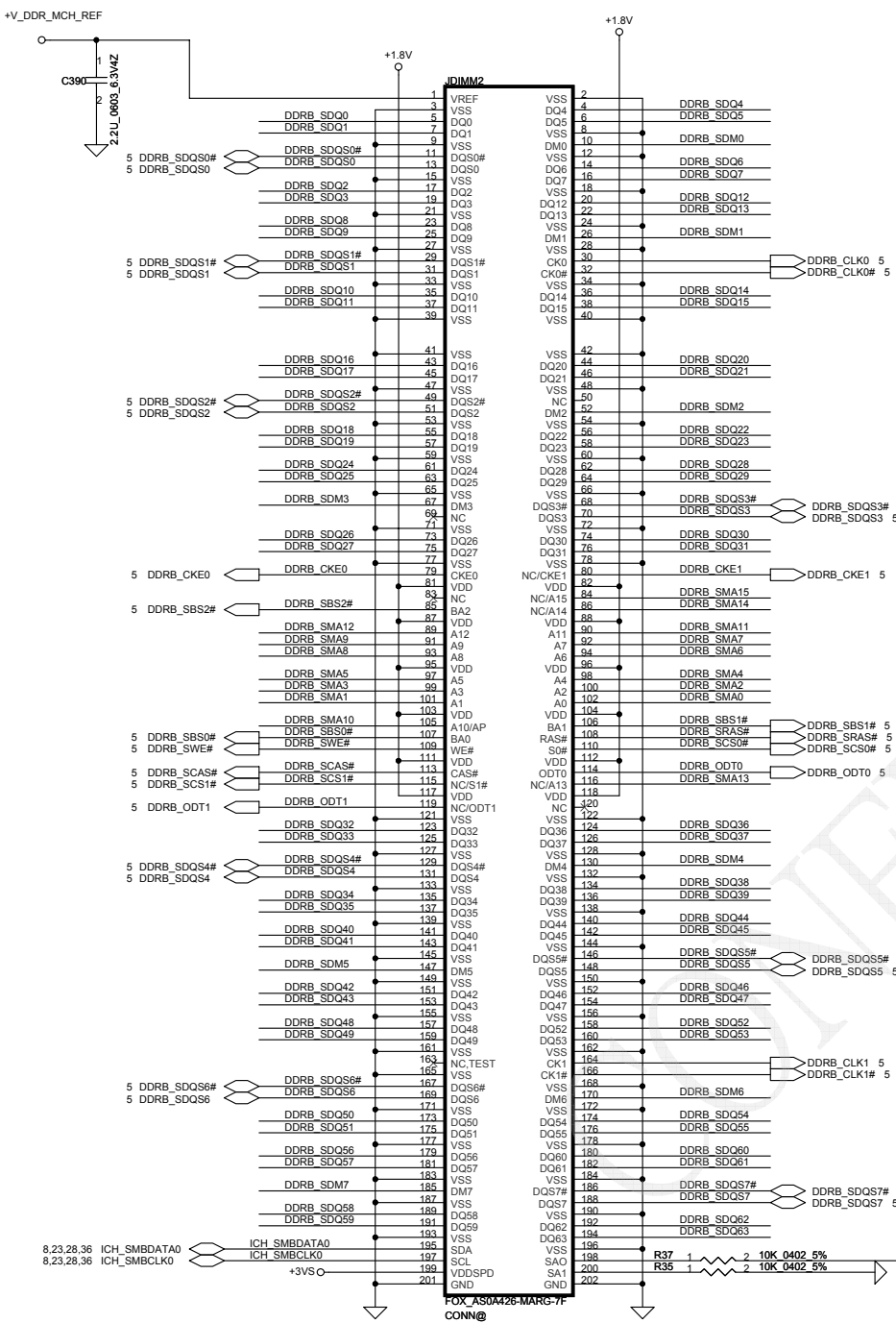
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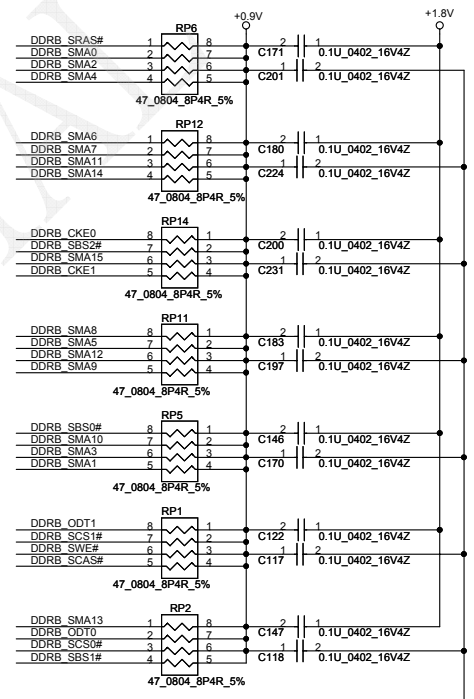
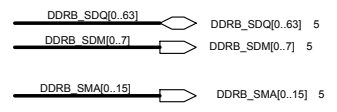
DIMM1 REV H:5.2mm (BOT)



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DIMM2 REV H:9.2mm (BOT)

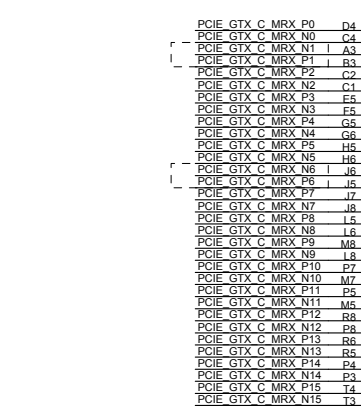


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14 PCIE_GTX_C_MRX_P0..15] PCIE GTX C MRX P0..15]
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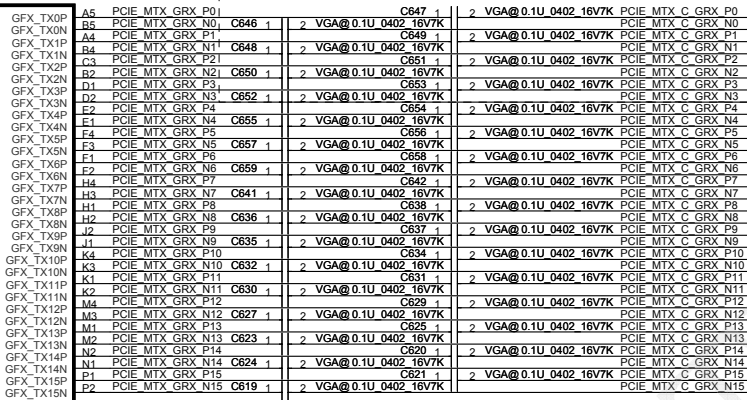
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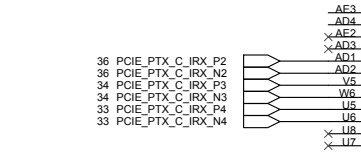


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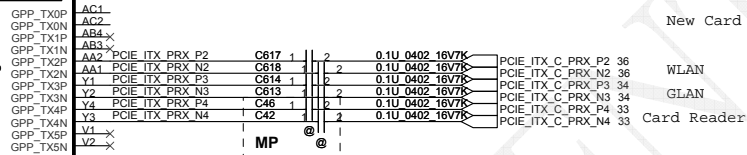
PCIE I/F GFX



DVT



PCIE I/F GPP



New Card

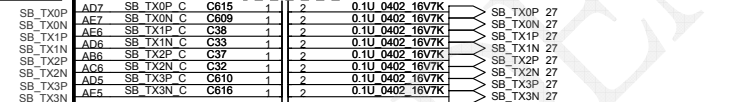
WLAN

GLAN

Card Reader



PCIE I/F SB



PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)

RS780M_FCBGA528

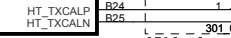
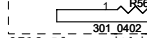
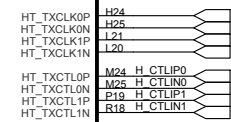
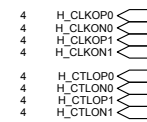
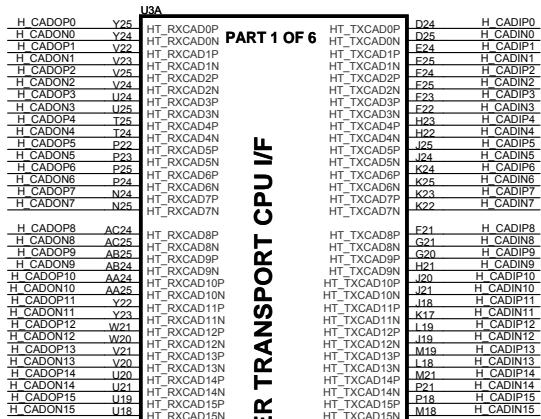
RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

USA

PART 1 OF 6

HYPER TRANSPORT CPU I/F



0718 Place within 1" layout 1:2

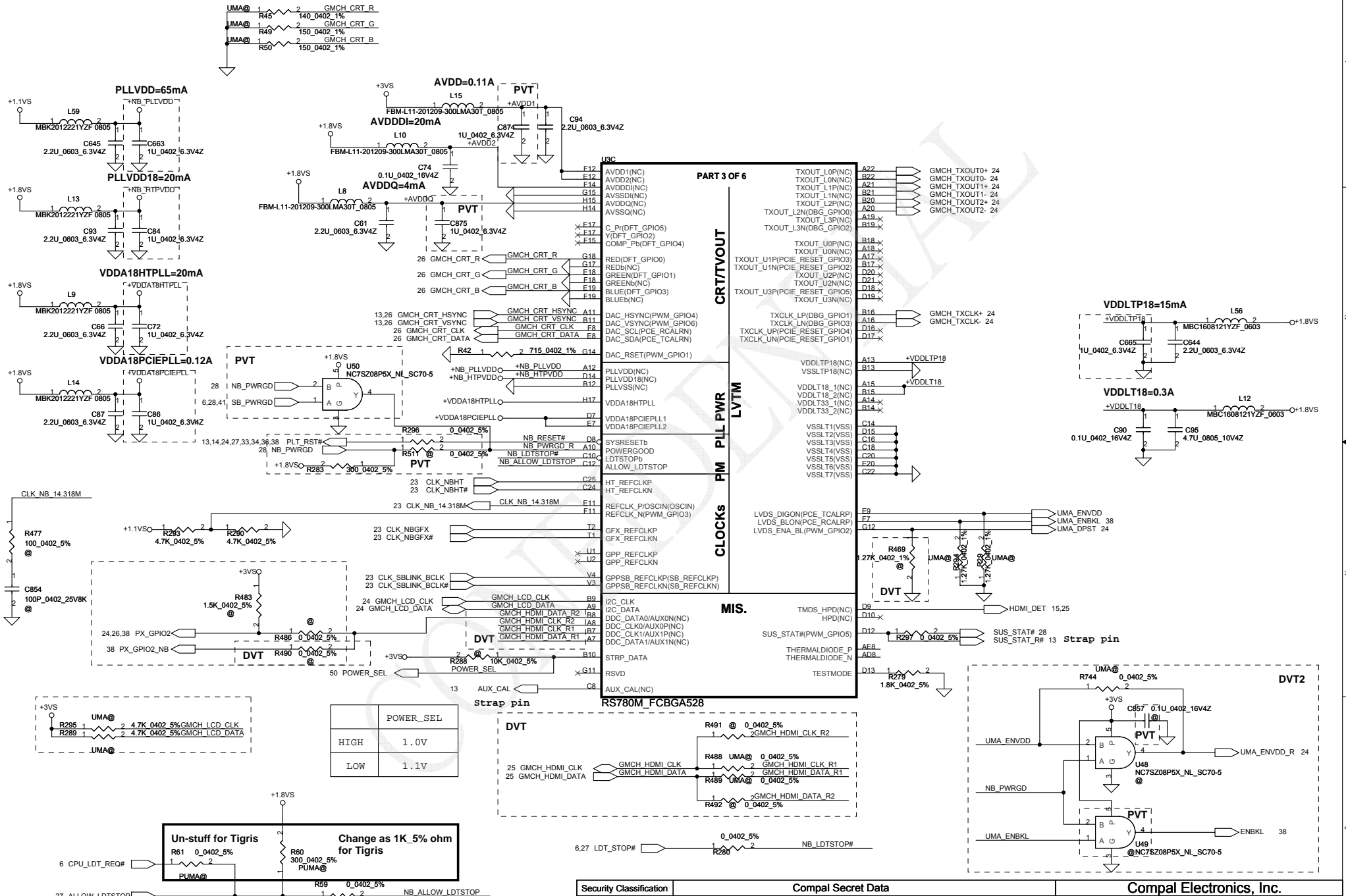
RS780M_FCBGA528

0718 Place within 1" layout 1:2

SA00002DR30 S IC 216-0674026 A13 RS780MN FCBGA 0FA

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For RS780M A13
 RED: Connected to GND through two separate 140ohm 1% resistor

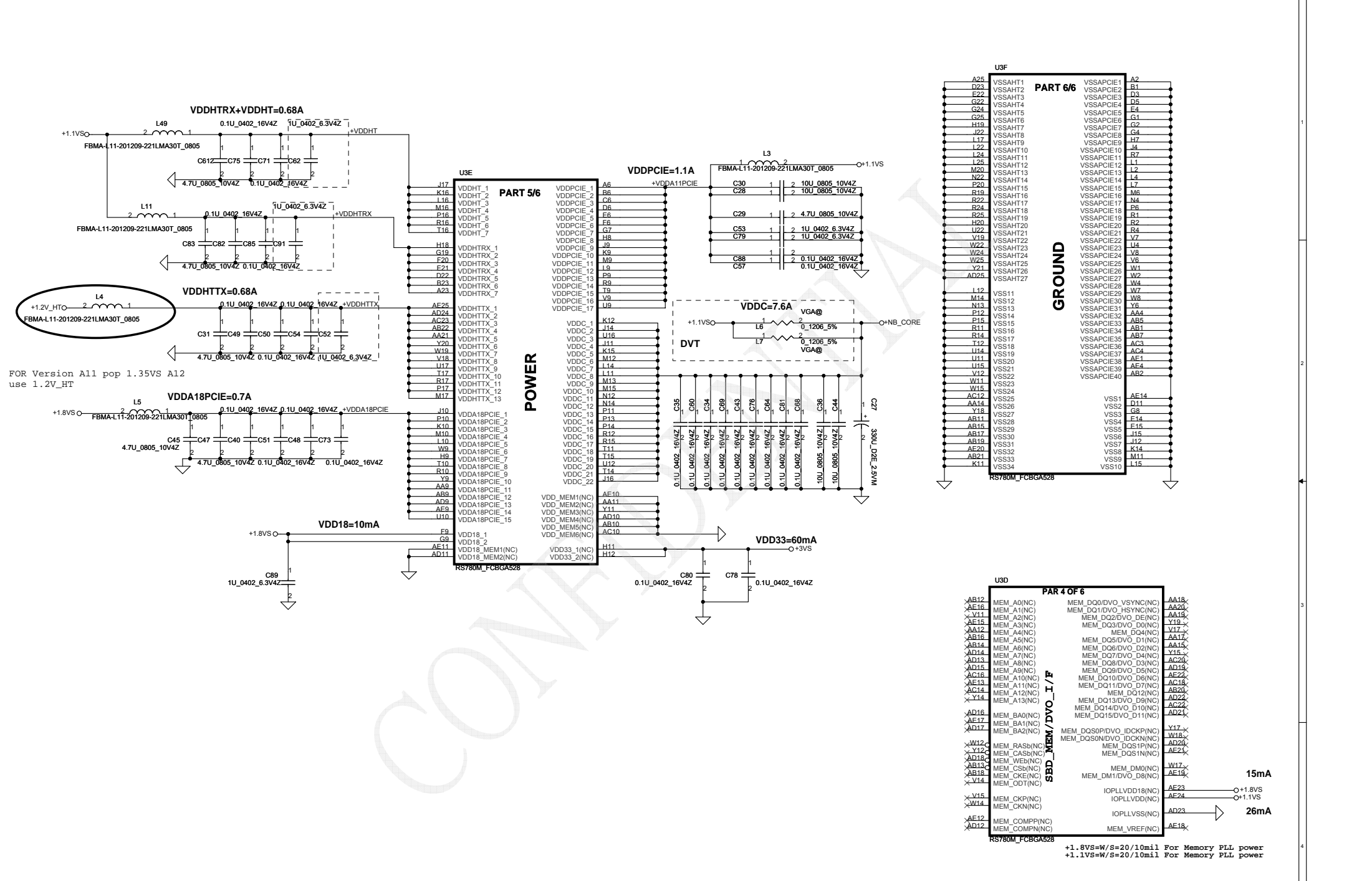


Un-stuff for Tigris
 R61 0.0402 5% PUMA@
 R60 300.0402 5% PUMA@
 R59 0.0402 5% PUMA@

Change as 1K.5% ohm for Tigris

	POWER_SEL
HIGH	1.0V
LOW	1.1V

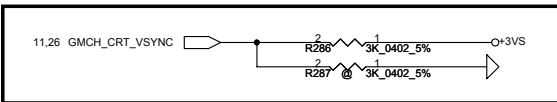
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FOR Version A11 pop 1.35VS A12
use 1.2V_HT

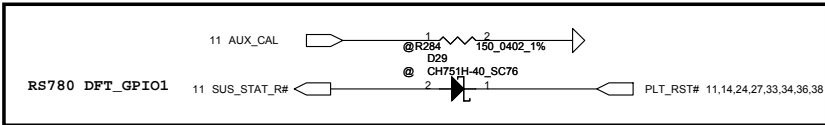
+1.8VS=W/S=20/10mil For Memory PLL power
+1.1VS=W/S=20/10mil For Memory PLL power

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Date:	Thursday, March 26, 2009	Sheet	12	of	57		



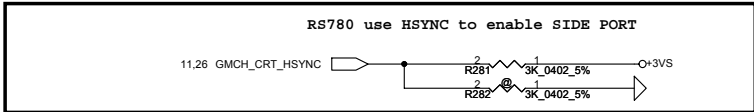
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO. (VSYNC)
 1 : Disable (RS780)
 0 : Enable (Rs780)



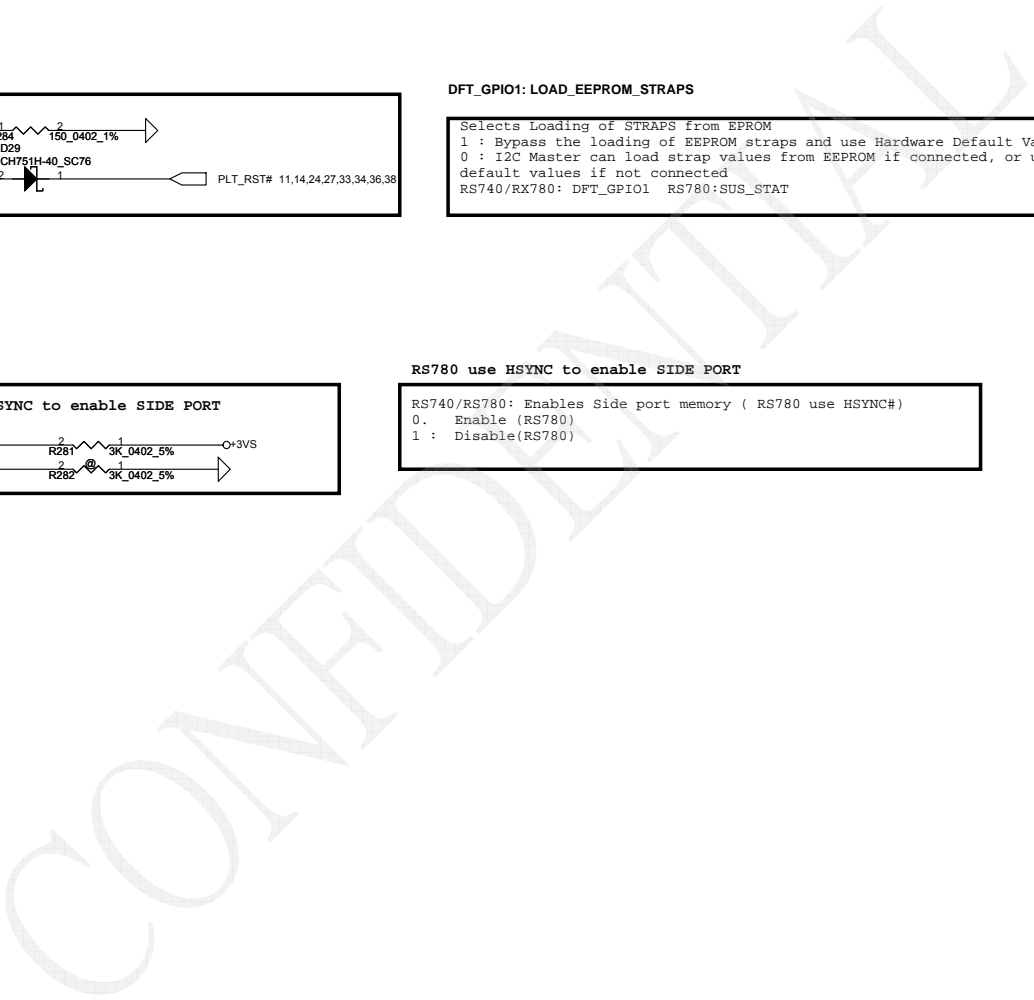
DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RS740/RX780: DFT_GPIO1 RS780:SUS_STAT



RS780 use HSYNC to enable SIDE PORT

RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
 0 : Enable (RS780)
 1 : Disable(RS780)

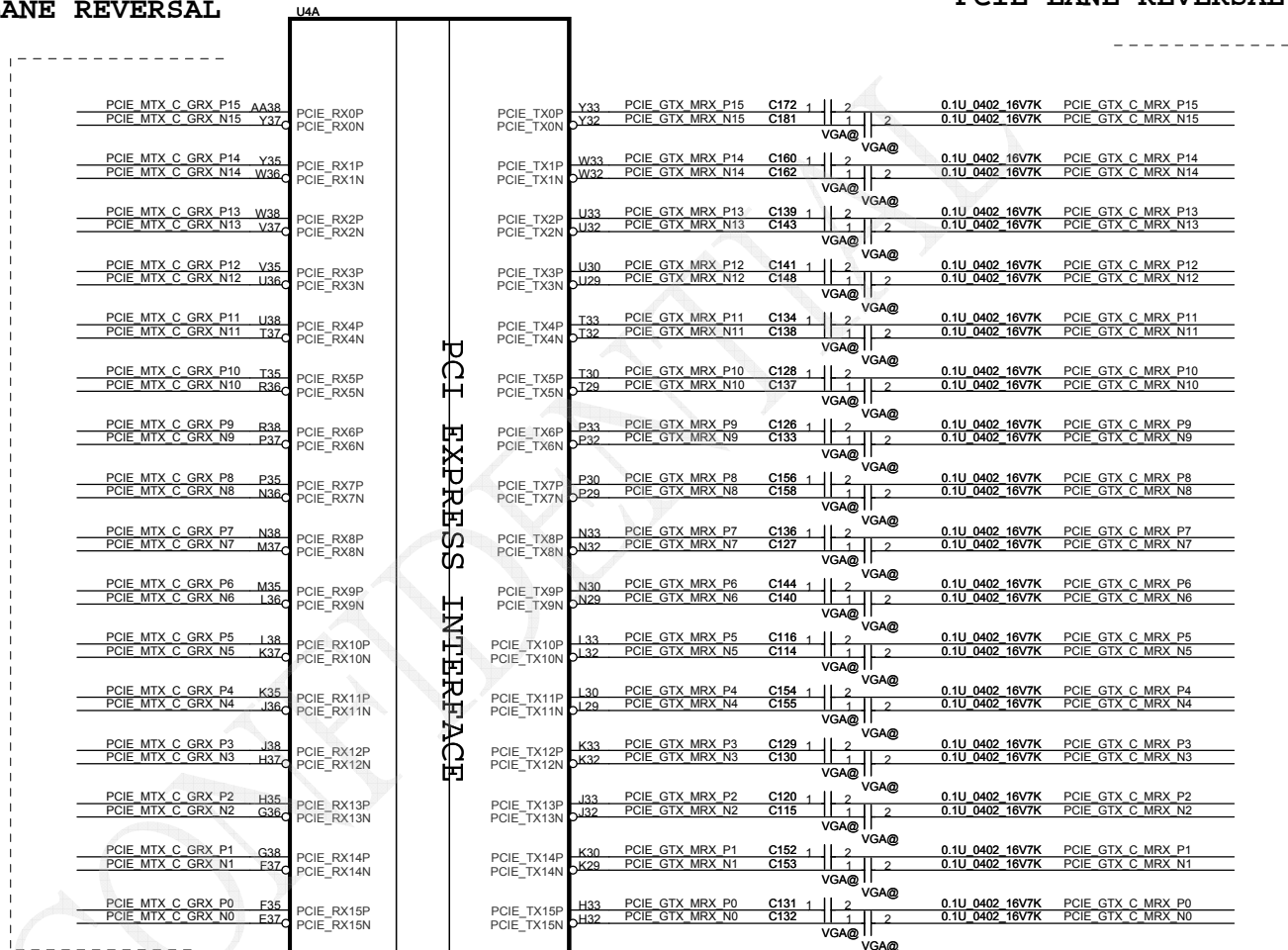


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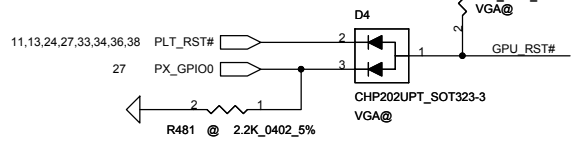
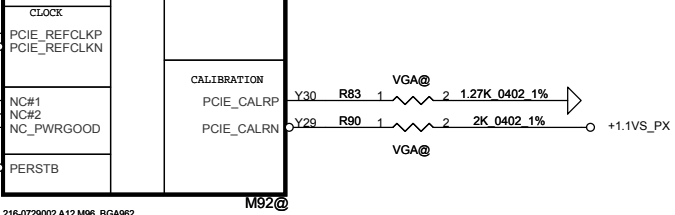
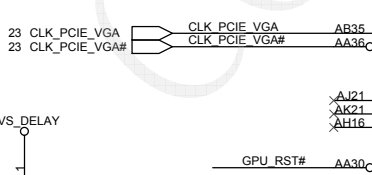
- 10 PCIE_GTX_C_MRX_P[0..15] \leftarrow PCIE GTX C MRX P[0..15]
- 10 PCIE_GTX_C_MRX_N[0..15] \leftarrow PCIE GTX C MRX N[0..15]
- 10 PCIE_MTX_C_GRX_P[0..15] \leftarrow PCIE MTX C GRX P[0..15]
- 10 PCIE_MTX_C_GRX_N[0..15] \leftarrow PCIE MTX C GRX N[0..15]

PCIE LANE REVERSAL

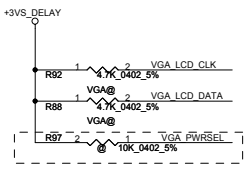
PCIE LANE REVERSAL



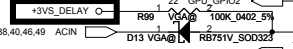
PCI EXPRESS INTERFACE



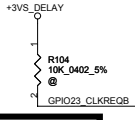
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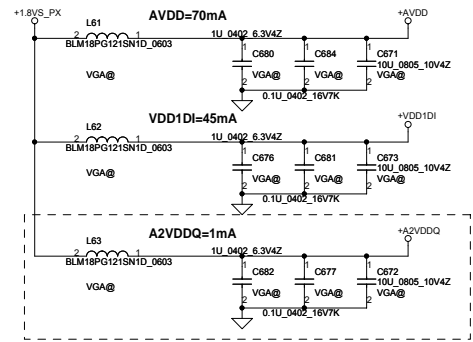
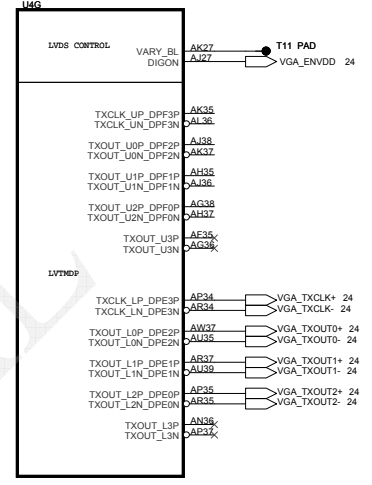
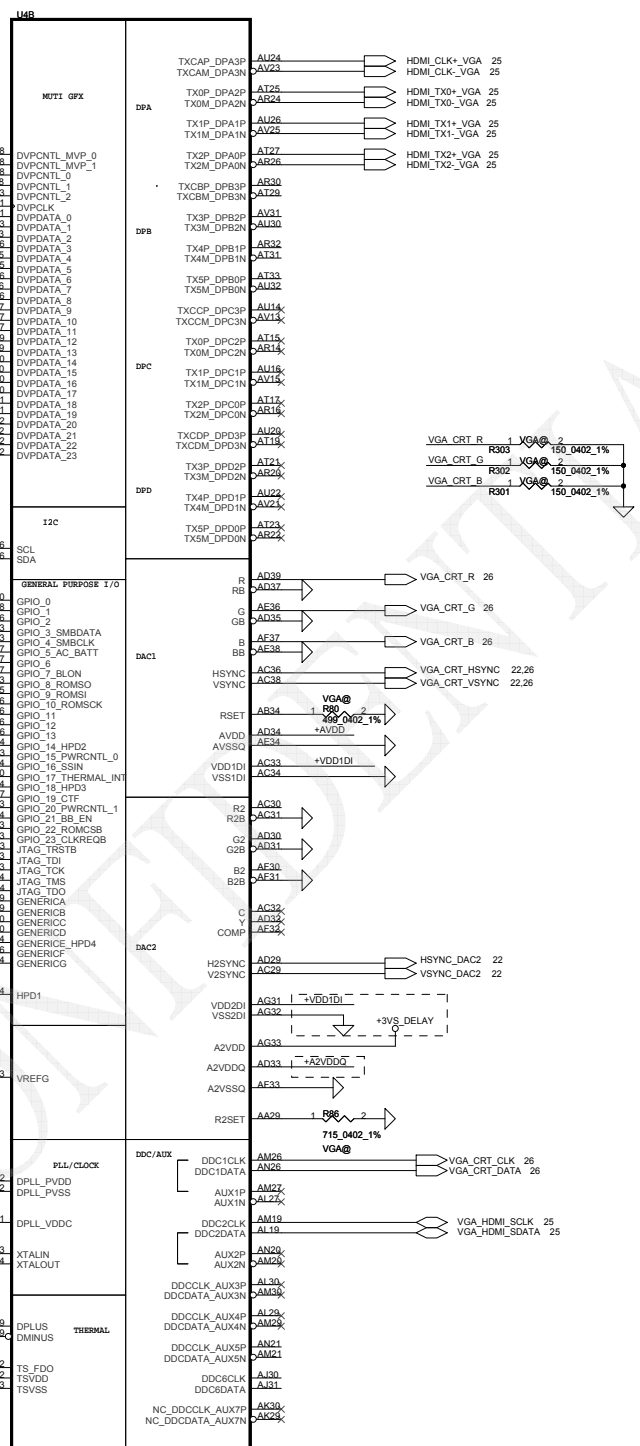
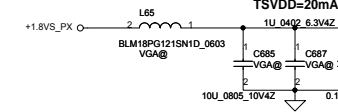
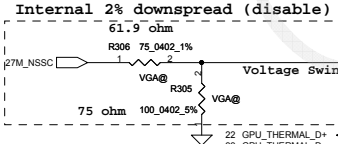
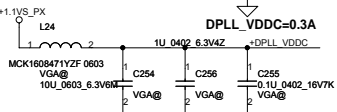
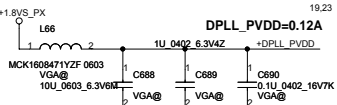
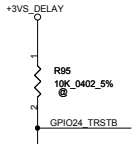
GPIO_5_AC_BATT
AC (Performance mode) = 3.3 V
Battery saving mode = 0.0 V



VGA_PWRSEL
High:VGA_CORE 0.95V
Low :VGA_CORE 1.2V

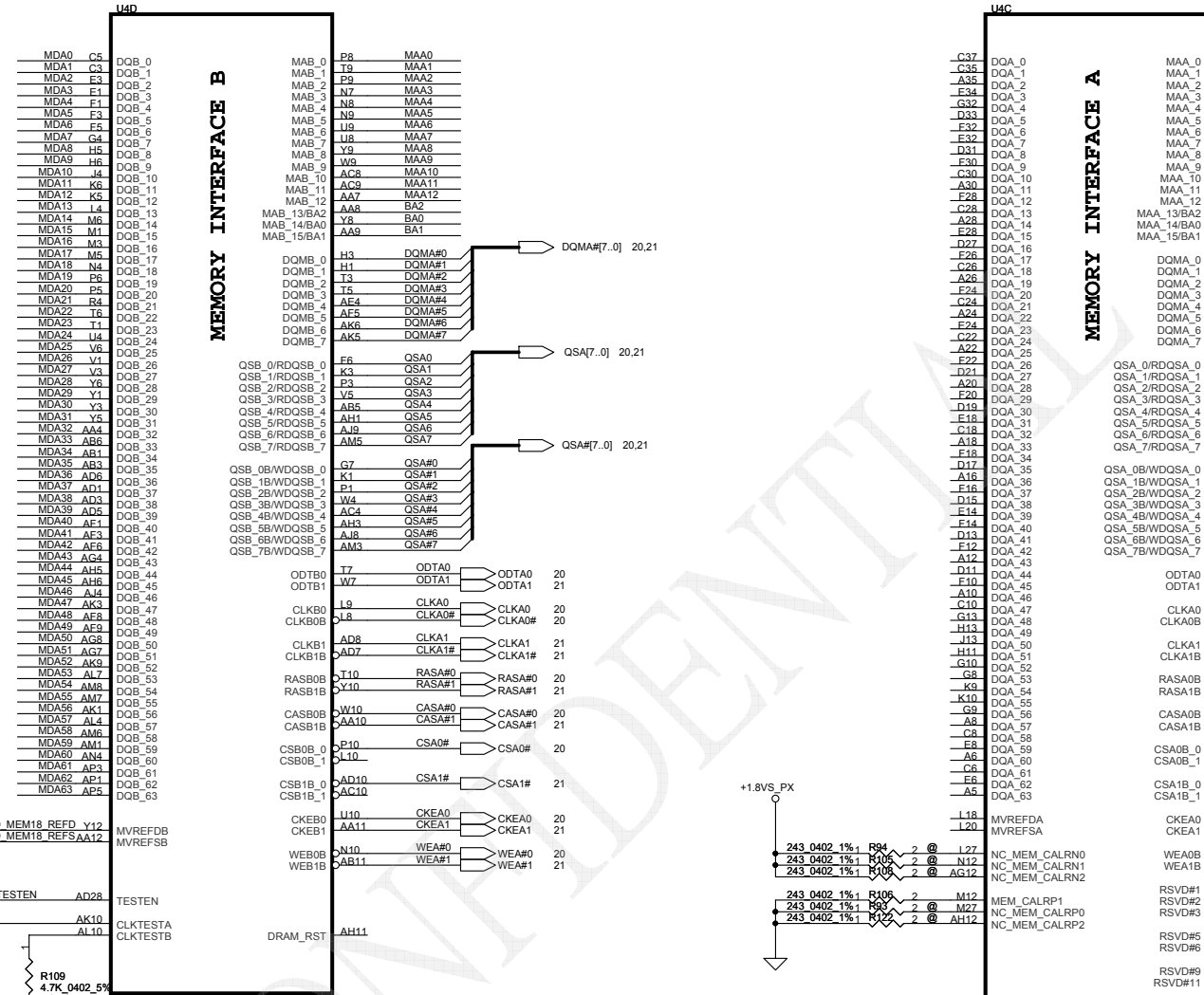


Back bias (BB) control
Back Bias Disabled :
GPIO_21_BB_EN = 0V
BBF connect directly to VDDC



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hexainf@hotmail.com
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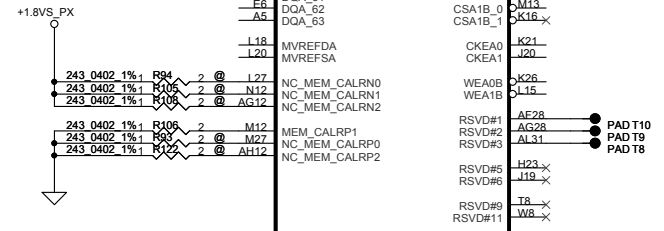
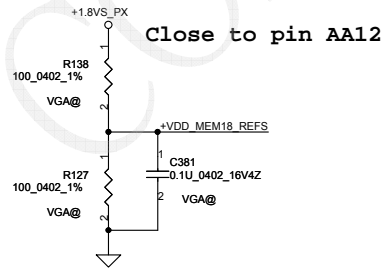
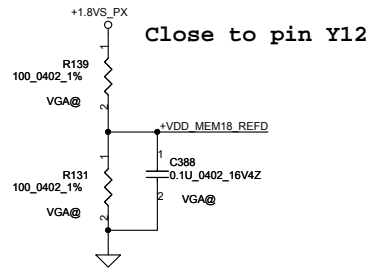
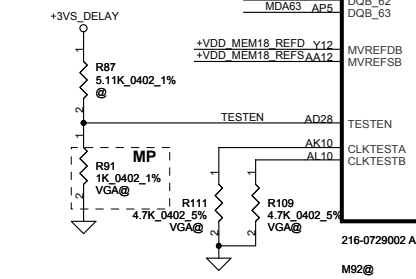
MEMORY INTERFACE B

MEMORY INTERFACE A

- MDA0 C5 DOB_0
- MDA1 C3 DOB_1
- MDA2 E3 DOB_2
- MDA3 F1 DOB_3
- MDA4 F1 DOB_4
- MDA5 F3 DOB_5
- MDA6 E5 DOB_6
- MDA7 G4 DOB_7
- MDA8 H5 DOB_8
- MDA9 H4 DOB_9
- MDA10 H4 DOB_10
- MDA11 K6 DOB_11
- MDA12 K5 DOB_12
- MDA13 L4 DOB_13
- MDA14 M6 DOB_14
- MDA15 M1 DOB_15
- MDA16 M3 DOB_16
- MDA17 M5 DOB_17
- MDA18 N4 DOB_18
- MDA19 P8 DOB_19
- MDA20 P5 DOB_20
- MDA21 R4 DOB_21
- MDA22 T1 DOB_22
- MDA23 T1 DOB_23
- MDA24 U4 DOB_24
- MDA25 V6 DOB_25
- MDA26 V1 DOB_26
- MDA27 V3 DOB_27
- MDA28 Y6 DOB_28
- MDA29 Y1 DOB_29
- MDA30 Y3 DOB_30
- MDA31 Y5 DOB_31
- MDA32 A44 DOB_32
- MDA33 AB6 DOB_33
- MDA34 AB1 DOB_34
- MDA35 AB3 DOB_35
- MDA36 AD6 DOB_36
- MDA37 AD1 DOB_37
- MDA38 AD3 DOB_38
- MDA39 AD5 DOB_39
- MDA40 AF1 DOB_40
- MDA41 AF3 DOB_41
- MDA42 AF6 DOB_42
- MDA43 AG4 DOB_43
- MDA44 AH5 DOB_44
- MDA45 AH6 DOB_45
- MDA46 AH4 DOB_46
- MDA47 AK3 DOB_47
- MDA48 AF8 DOB_48
- MDA49 AF9 DOB_49
- MDA50 AG8 DOB_50
- MDA51 AG7 DOB_51
- MDA52 AK9 DOB_52
- MDA53 AL7 DOB_53
- MDA54 AM8 DOB_54
- MDA55 AM7 DOB_55
- MDA56 AK1 DOB_56
- MDA57 AL4 DOB_57
- MDA58 AM6 DOB_58
- MDA59 AM1 DOB_59
- MDA60 AN4 DOB_60
- MDA61 AP3 DOB_61
- MDA62 AP1 DOB_62
- MDA63 AP5 DOB_63

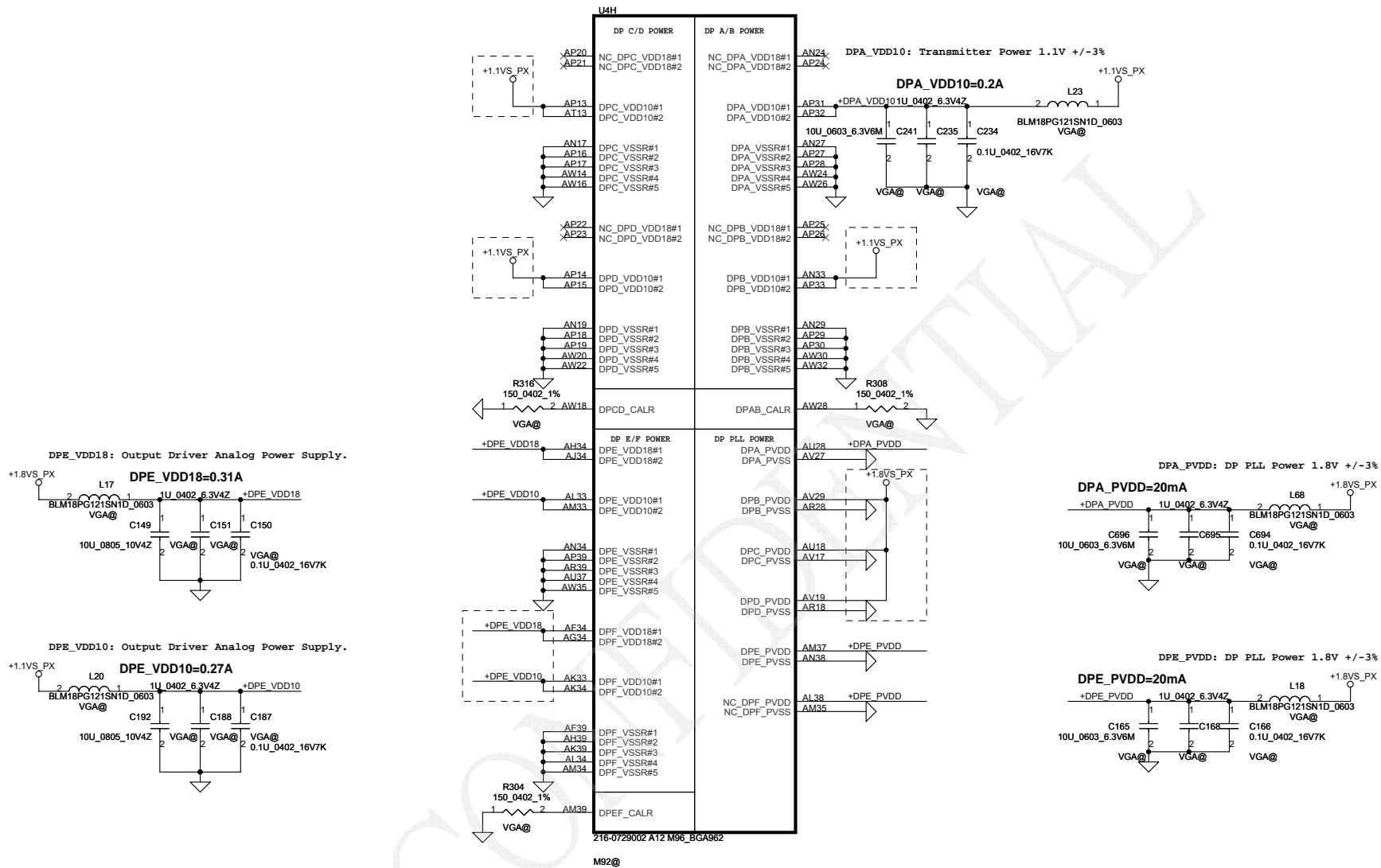
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- MAB_1 T9 MAA1
- MAB_2 P9 MAA2
- MAB_3 N7 MAA3
- MAB_4 N8 MAA4
- MAB_5 N9 MAA5
- MAB_6 U9 MAA6
- MAB_7 UR MAA7
- MAB_8 Y9 MAA8
- MAB_9 W9 MAA9
- MAB_10 AC9 MAA10
- MAB_11 AC9 MAA11
- MAB_12 AA7 MAA12
- MAB_13 AA8 MAA13
- MAB_14 BA0 MAA14
- MAB_15 BA1 MAA15
- DQMB_0 H3 DQMA#0
- DQMB_1 H1 DQMA#1
- DQMB_2 T3 DQMA#2
- DQMB_3 T5 DQMA#3
- DQMB_4 AF4 DQMA#4
- DQMB_5 AF5 DQMA#5
- DQMB_6 AK6 DQMA#6
- DQMB_7 AK5 DQMA#7
- QSB_0/RDQSB_0 E6 QSA0
- QSB_1/RDQSB_1 K3 QSA1
- QSB_2/RDQSB_2 P3 QSA2
- QSB_3/RDQSB_3 V5 QSA3
- QSB_4/RDQSB_4 AB5 QSA4
- QSB_5/RDQSB_5 AH1 QSA5
- QSB_6/RDQSB_6 AJ2 QSA6
- QSB_7/RDQSB_7 AM5 QSA7
- QSB_0B/WDQSB_0 G7 QSA#0
- QSB_1B/WDQSB_1 K1 QSA#1
- QSB_2B/WDQSB_2 P1 QSA#2
- QSB_3B/WDQSB_3 W4 QSA#3
- QSB_4B/WDQSB_4 AC4 QSA#4
- QSB_5B/WDQSB_5 AH3 QSA#5
- QSB_6B/WDQSB_6 AJ8 QSA#6
- QSB_7B/WDQSB_7 AM3 QSA#7
- ODTB0 T7 ODTA0
- ODTB1 W7 ODTA1
- CLKB0 L9 CLKA0
- CLKB0B L8 CLKA#0
- CLKB1 AD8 CLKA1
- CLKB1B AD7 CLKA1#
- RASB0B T10 RASA#0
- RASB1B Y40 RASA#1
- CASB0B W10 CASA#0
- CASB1B AA10 CASA#1
- CSB0B_0 P10 CSA#0
- CSB0B_1 L10 CSA#0
- CSB1B_0 AD10 CSA1#
- CSB1B_1 AC10 CSA1#
- CKEB0 U10 CKEA0
- CKEB1 AA11 CKEA1
- WEB0B N10 WEA#0
- WEB1B AB11 WEA#1

- C37 DQA_0
- C38 DQA_1
- A35 DQA_2
- E34 DQA_3
- G32 DQA_4
- D33 DQA_5
- F32 DQA_6
- E32 DQA_7
- D31 DQA_8
- E30 DQA_9
- DQA_10 A30
- DQA_11 DQA_11
- F28 DQA_12
- C28 DQA_13
- E28 DQA_14
- DQA_15 DQA_15
- DQA_16 DQA_16
- F26 DQA_17
- C25 DQA_18
- A25 DQA_19
- E24 DQA_20
- C24 DQA_21
- A24 DQA_22
- F22 DQA_23
- C22 DQA_24
- A22 DQA_25
- E22 DQA_26
- K3 DQA_27
- A20 DQA_28
- F20 DQA_29
- D19 DQA_30
- E18 DQA_31
- C18 DQA_32
- A18 DQA_33
- F18 DQA_34
- D17 DQA_35
- K1 DQA_36
- E16 DQA_37
- D15 DQA_38
- E14 DQA_39
- E14 DQA_40
- D13 DQA_41
- F12 DQA_42
- A12 DQA_43
- D11 DQA_44
- E10 DQA_45
- A10 DQA_46
- C10 DQA_47
- DQA_48 DQA_48
- H13 DQA_49
- H13 DQA_50
- H11 DQA_51
- G10 DQA_52
- G8 DQA_53
- K3 DQA_54
- K10 DQA_55
- G9 DQA_56
- A8 DQA_57
- C8 DQA_58
- E8 DQA_59
- A6 DQA_60
- C6 DQA_61
- E6 DQA_62
- A5 DQA_63
- L18 MVREFDA
- L20 MVREFSA
- NC_MEM_CALRN0
- NC_MEM_CALRN1
- NC_MEM_CALRN2
- MEM_CALRP1
- NC_MEM_CALRP0
- NC_MEM_CALRP2
- WEA0B
- WEA1B
- RSVD#1
- RSVD#2
- RSVD#3
- RSVD#5
- RSVD#6
- RSVD#9
- RSVD#11
- MAA_0 G24
- MAA_1 H24
- MAA_2 H24
- MAA_3 J24
- MAA_4 H26
- MAA_5 H26
- MAA_6 G21
- MAA_7 H21
- MAA_8 H19
- MAA_9 H20
- MAA_10 G16
- MAA_11 G16
- MAA_12 H16
- MAA_13/BA2 H17
- MAA_14/BA0 H17
- MAA_15/BA1 H17
- DOMA_0 A32
- DOMA_1 C32
- DOMA_2 E22
- DOMA_3 C14
- DOMA_4 A14
- DOMA_5 E10
- DOMA_6 D9
- DOMA_7 D9
- QSA_0/RDQSA_0 C34
- QSA_1/RDQSA_1 E28
- QSA_2/RDQSA_2 E25
- QSA_3/RDQSA_3 E20
- QSA_4/RDQSA_4 F16
- QSA_5/RDQSA_5 F12
- QSA_6/RDQSA_6 D7
- QSA_7/RDQSA_7 D7
- QSA_0B/WDQSA_0 A34
- QSA_1B/WDQSA_1 E30
- QSA_2B/WDQSA_2 E28
- QSA_3B/WDQSA_3 C20
- QSA_4B/WDQSA_4 C16
- QSA_5B/WDQSA_5 C12
- QSA_6B/WDQSA_6 H11
- QSA_7B/WDQSA_7 F8
- ODTA0 J21
- ODTA1 G19
- CLKA0 H27
- CLKA0B G27
- CLKA1 H14
- CLKA1B H14
- RASA0B K23
- RASA1B K19
- CASA0B K20
- CASA1B K17
- CSA0B_0 K24
- CSA0B_1 K27
- CSA1B_0 M13
- CSA1B_1 K16
- CKEA0 K21
- CKEA1 J20
- WEA0B K26
- WEA1B L15
- RSVD#1 AE28
- RSVD#2 AC28
- RSVD#3 AL31
- RSVD#5 H23
- RSVD#6 J19
- RSVD#9 TR
- RSVD#11 WR

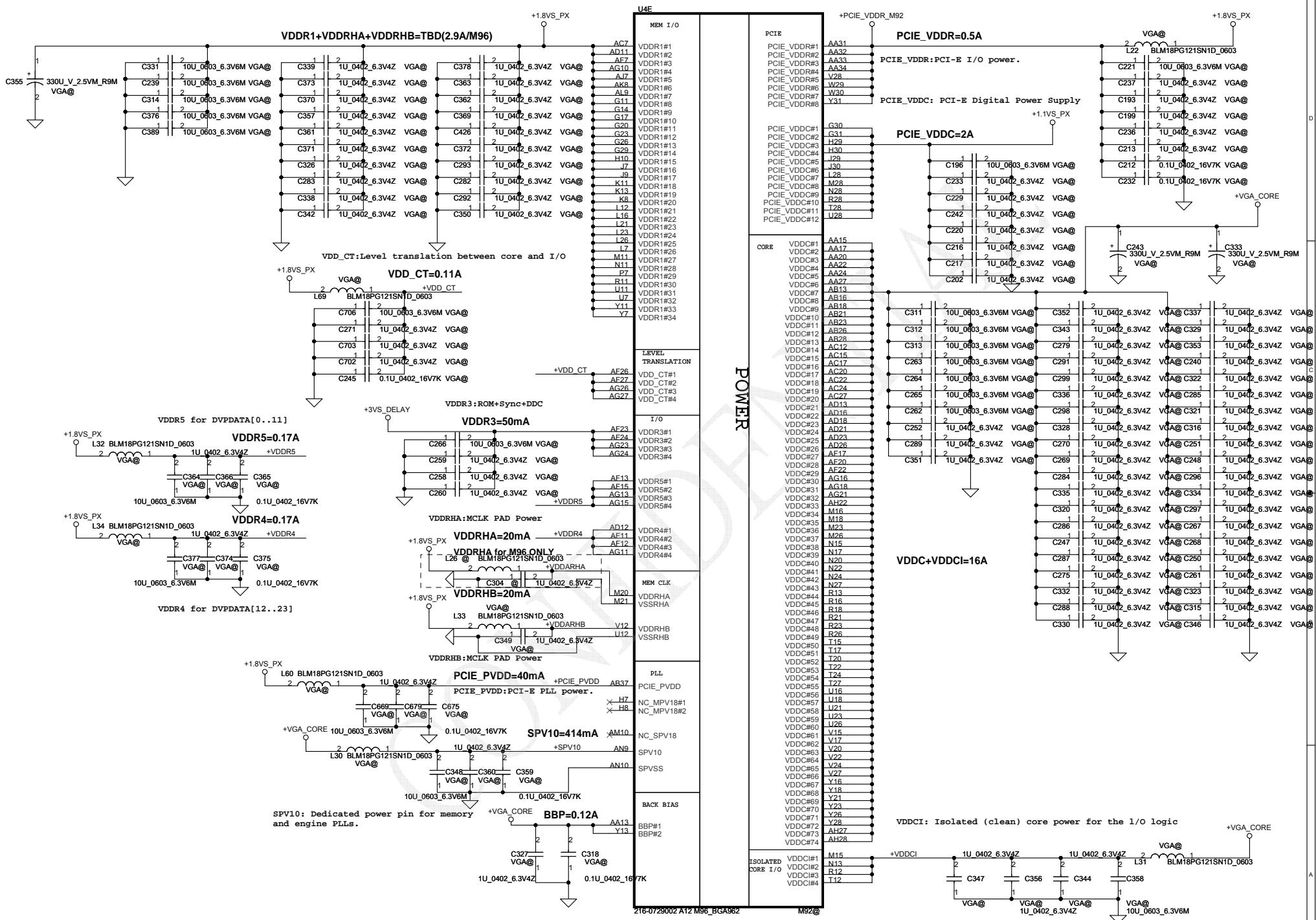


M92-S2 and M92-M use memory group A only while M92-M2 uses memory group B only.

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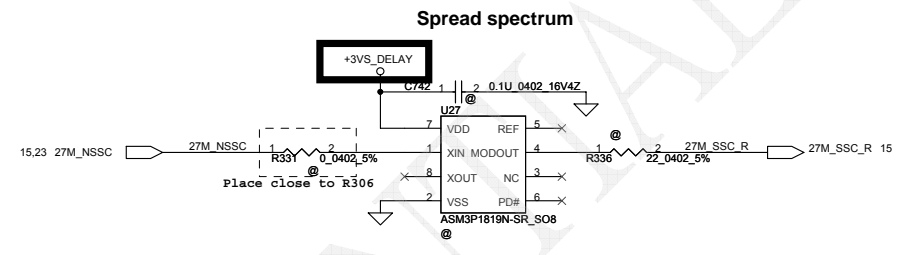


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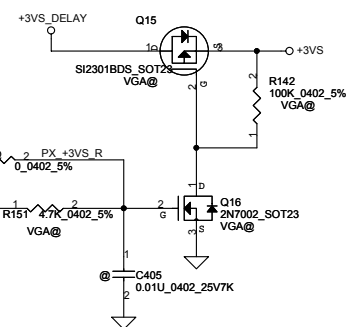
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AB39	PCIE_VSS#1	A3
E39	PCIE_VSS#2	A37
F34	PCIE_VSS#3	GND#2
E38	PCIE_VSS#4	GND#3
G33	PCIE_VSS#5	GND#4
G34	PCIE_VSS#6	GND#5
H31	PCIE_VSS#7	GND#6
H34	PCIE_VSS#8	GND#7
H39	PCIE_VSS#9	GND#8
I31	PCIE_VSS#10	GND#9
I34	PCIE_VSS#11	GND#10
K31	PCIE_VSS#12	GND#11
K34	PCIE_VSS#13	GND#12
K39	PCIE_VSS#14	GND#13
L31	PCIE_VSS#15	GND#14
L34	PCIE_VSS#16	GND#15
M34	PCIE_VSS#17	GND#16
M39	PCIE_VSS#18	GND#17
N31	PCIE_VSS#19	GND#18
N34	PCIE_VSS#20	GND#19
P31	PCIE_VSS#21	GND#20
P34	PCIE_VSS#22	GND#21
P39	PCIE_VSS#23	GND#22
R34	PCIE_VSS#24	GND#23
T31	PCIE_VSS#25	GND#24
T34	PCIE_VSS#26	GND#25
T39	PCIE_VSS#27	GND#26
U31	PCIE_VSS#28	GND#27
U34	PCIE_VSS#29	GND#28
V34	PCIE_VSS#30	GND#29
V39	PCIE_VSS#31	GND#30
W31	PCIE_VSS#32	GND#31
W34	PCIE_VSS#33	GND#32
Y34	PCIE_VSS#34	GND#33
Y39	PCIE_VSS#35	GND#34
GND		
E15	GND#101	A39
E17	GND#102	AW1
F19	GND#103	AW39
F21	GND#104	
F23	GND#105	
F25	GND#106	
F27	GND#107	
F29	GND#108	
F31	GND#109	
F33	GND#110	
F7	GND#111	
F9	GND#112	
G2	GND#113	
G6	GND#114	
H9	GND#115	
J2	GND#116	
J27	GND#117	
J6	GND#118	
J6	GND#119	
K14	GND#120	
K7	GND#121	
L11	GND#122	
L2	GND#123	
L22	GND#125	
L24	GND#126	
L6	GND#127	
M17	GND#128	
M22	GND#129	
M24	GND#130	
N16	GND#131	
N18	GND#132	
N2	GND#133	
N21	GND#134	
N23	GND#135	
N26	GND#136	
N6	GND#137	
R13	GND#138	
R17	GND#139	
R2	GND#140	
R20	GND#141	
R22	GND#142	
R24	GND#143	
R27	GND#144	
R6	GND#145	
T11	GND#146	
T13	GND#147	
T16	GND#148	
T18	GND#149	
T21	GND#150	
T23	GND#151	
T26	GND#152	
U15	GND#153	
U17	GND#154	
U2	GND#155	
U23	GND#156	
U24	GND#157	
U27	GND#158	
U27	GND#159	
V11	GND#160	
V16	GND#161	
V18	GND#162	
V21	GND#163	
V23	GND#164	
V26	GND#165	
W2	GND#166	
W2	GND#167	
Y15	GND#168	
Y17	GND#169	
Y20	GND#170	
Y22	GND#171	
Y22	GND#172	
Y27	GND#173	
Y27	GND#174	
U13	GND#175	
V13	GND#176	

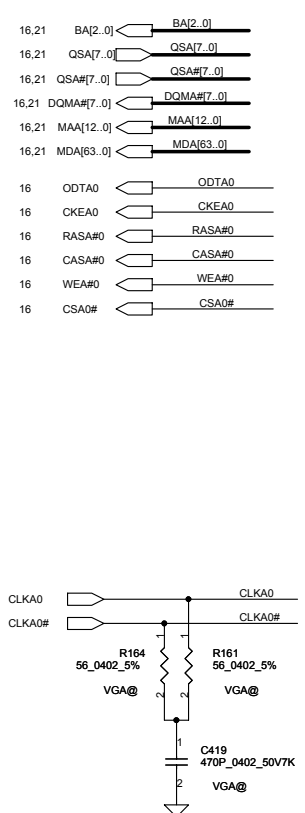
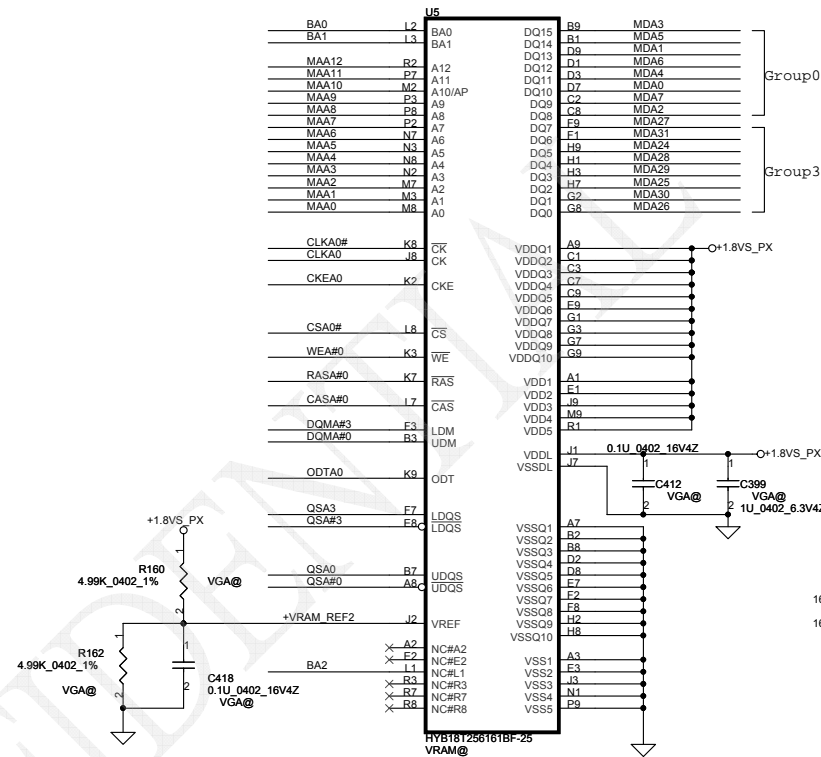
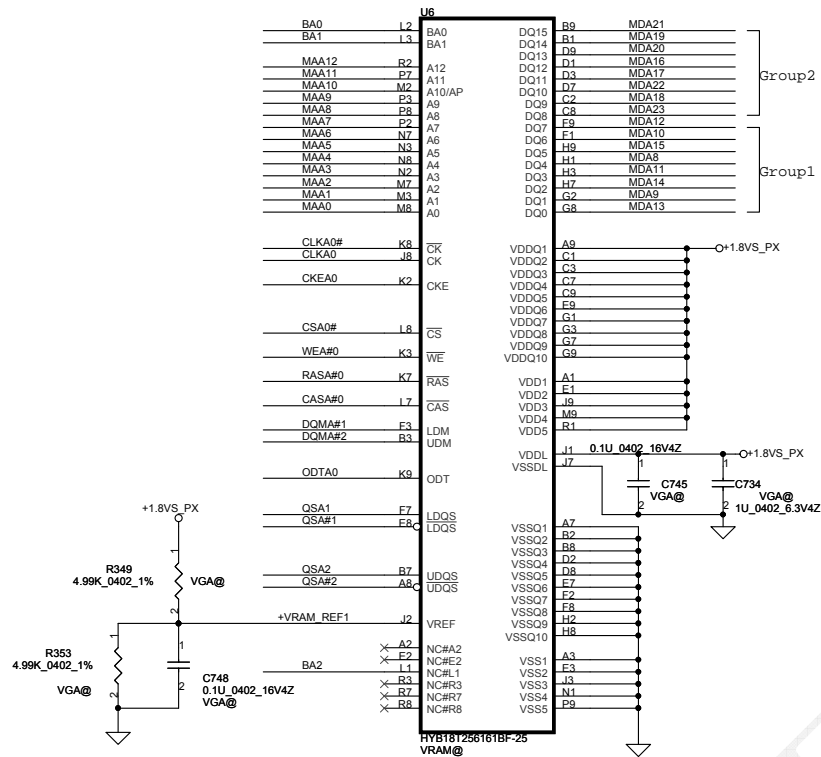


Spread spectrum



Use Delay 3.3V BUS (VDDR3) for GPIO/DDC Pull up to reduce Leakage to VDDR3 Bus.

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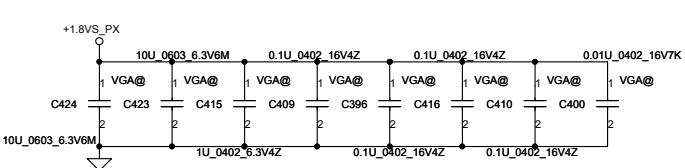
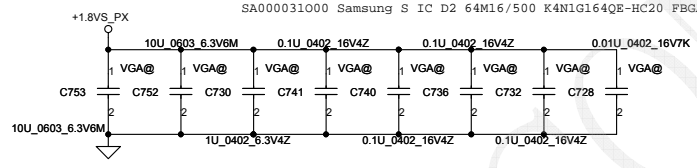


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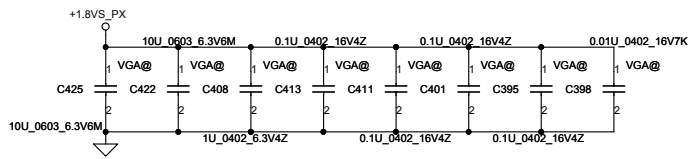
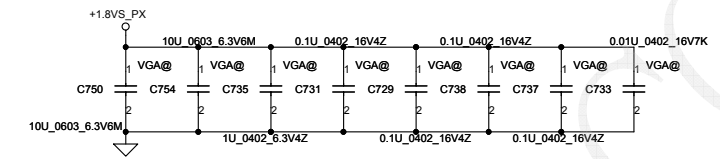
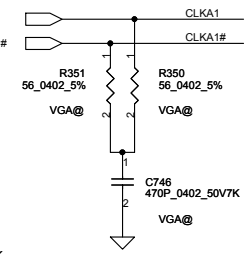
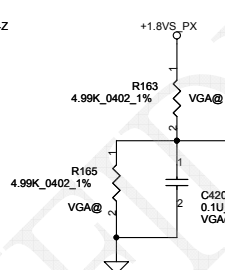
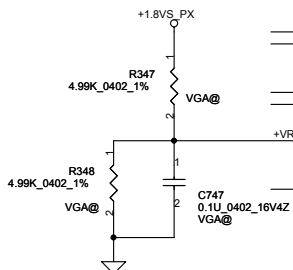
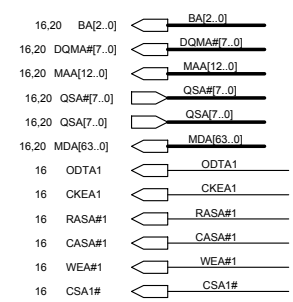
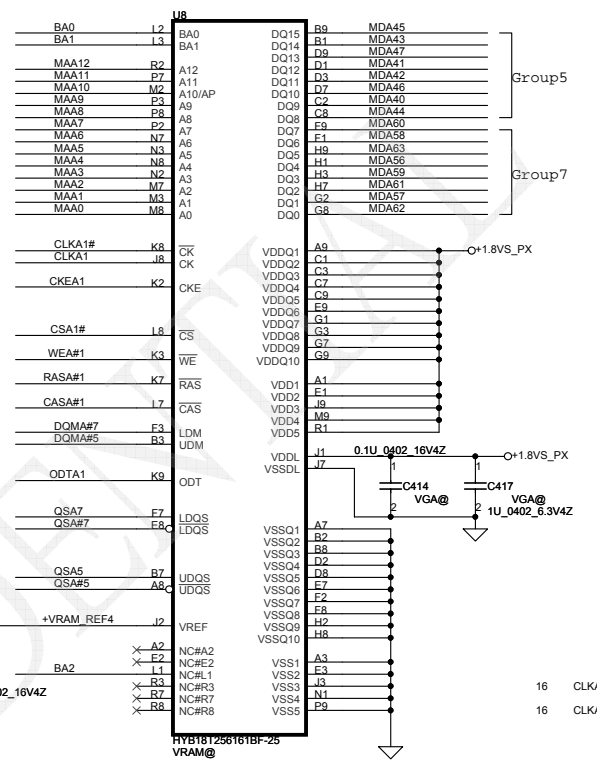
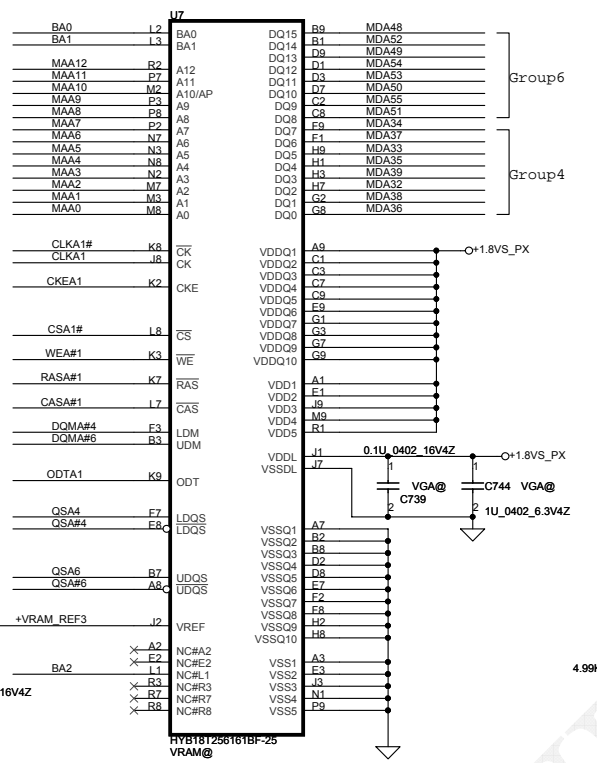
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SA00002MD00 Samsung S IC D2 64M16/500 K4N1G1640Q-HC20 FBGA84

SA000031000 Samsung S IC D2 64M16/500 K4N1G1640E-HC20 FBGA 84P

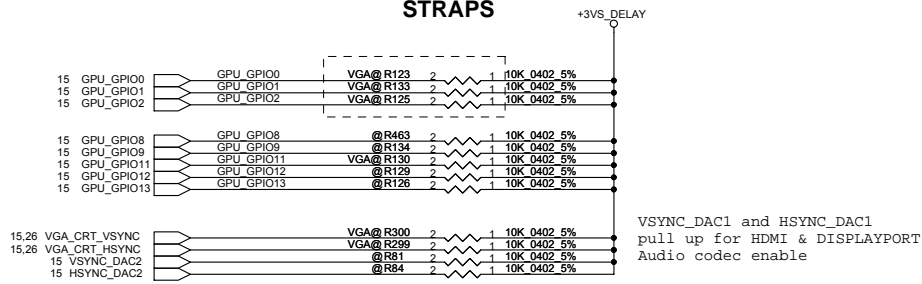


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STRAPS

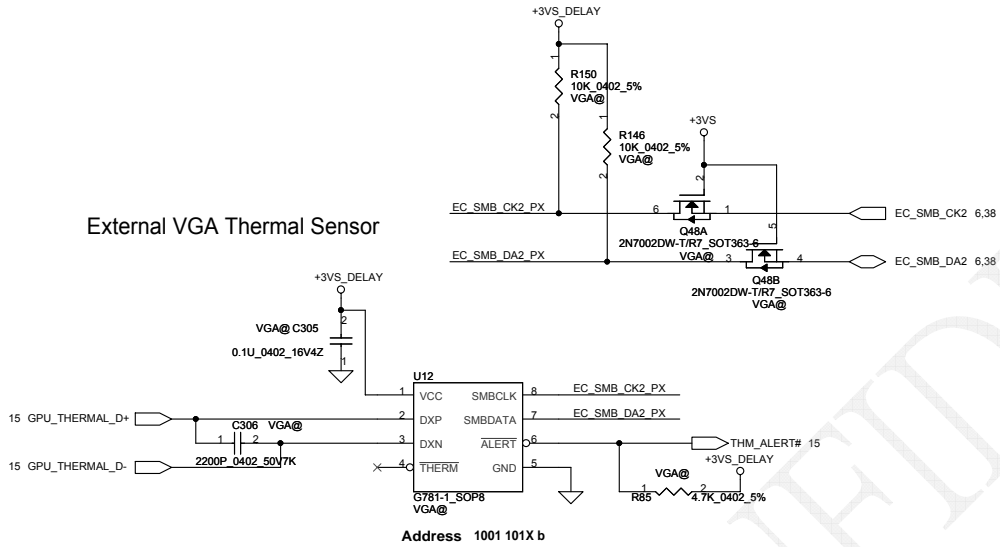


CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable	1: PCIe bus Full Tx output swing 0: PCIe bus 50% Tx output swing
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable	1: Tx de-emphasis enabled 0: Tx de-emphasis disabled
BIF_GEN2_EN_A	GPIO2	PCIe GNE2 ENABLED 0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0 (5.0 GT/s capability will be controlled by software)
VGA_DIS	GPIO9	VGA Disable determines whether or not the card will be recognized as the system's VGA controller	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller
CONFIG(2:0)	GPIO[13:11]	Size of the primary memory apertures	0 0 1
VIP_DEVICE_STRAP_EN	V2SYNC		0
RESERVED	H2SYNC		0
AUD[1]	HSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected	11
AUD[0]	VSYSN	1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	
RESERVED	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB		0: Disable external BIOS ROM device 1: Enable external BIOS ROM device
CCBYPASS	GENERICC	IGNORE VIP DEVICE STRAPS	0
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0

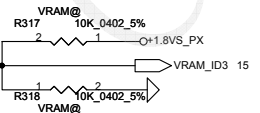
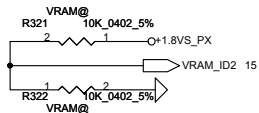
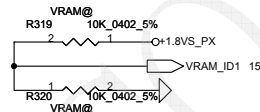
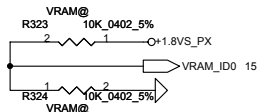
External VGA Thermal Sensor



AMD RESERVED CONFIGURATION STRAPS

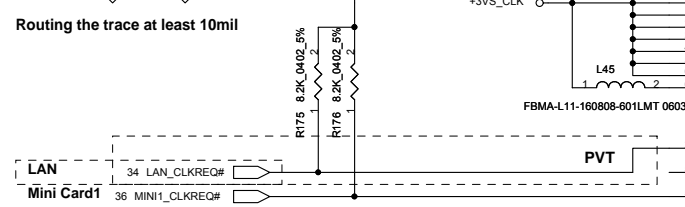
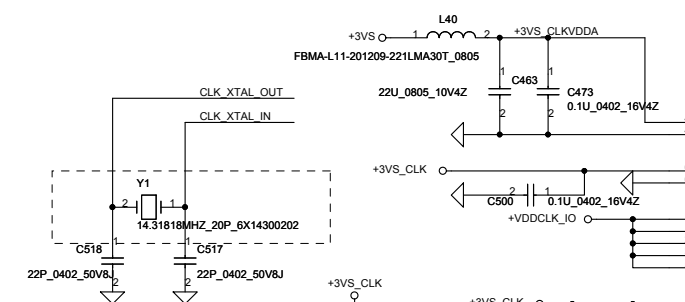
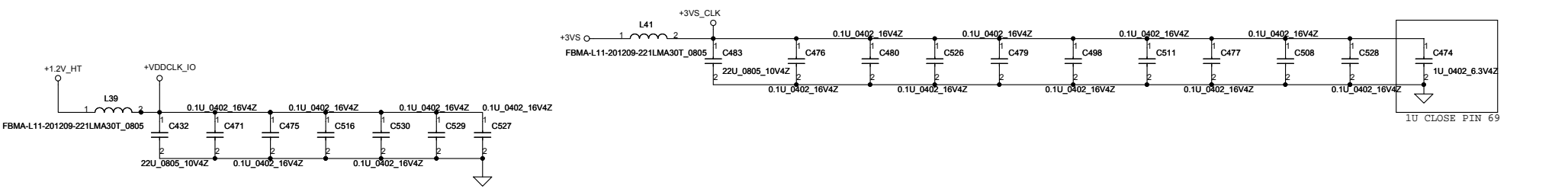
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO28_TDO	GPIO21_BB_EN

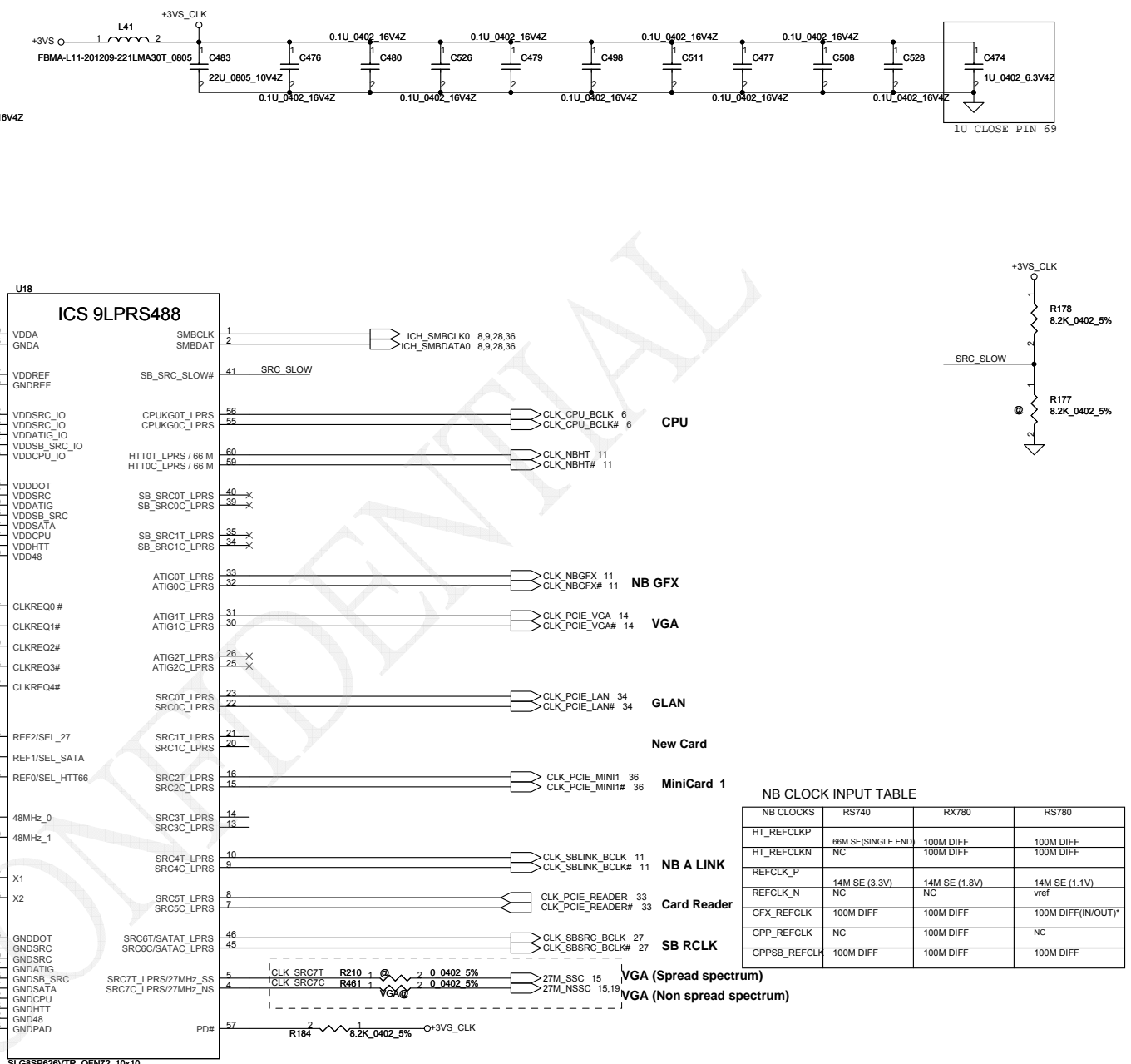
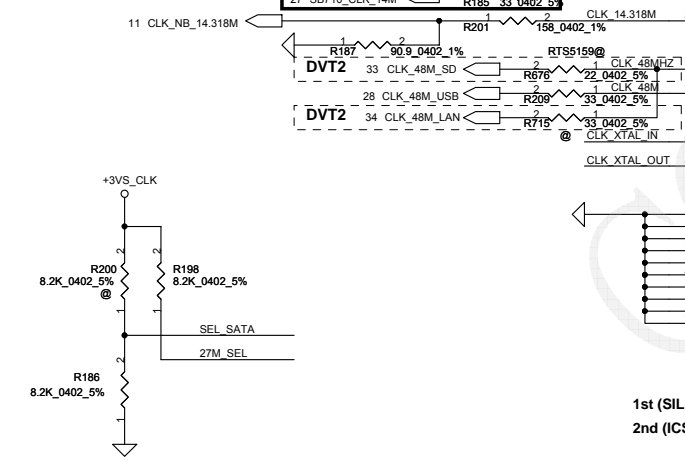


STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 3.2,1,0
VRAM_ID[3:0]	DVPDATA (23,22,21,20)	M92-M2 XT	JV40-PU_KBLG0	512M(x4)	Samsung 64Mx16 1.8V (Q-die)	SA00002MD00	0 0 0 0
			JV40-PU_KBLG0	512M(x4)	Hynix 64Mx16 1.8V	SA00002UH20	0 0 0 1
			JV40-PU_KBLG0	512M(x4)	Qimonda 64Mx16 1.8V	SA00002MF0PVT	0 0 1 0
			JV40-PU_KBLG0	512M(x4)	Samsung 64Mx16 1.8V (E-die)	SA000031010	0 1 0 0

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CLK_NB_14.318M	
RS780	1.1V 158R/90.0R



1st (SILEGO) : SA00001Z310 S IC SLG8SP626VTR QFN 72P CLK GEN
 2nd (ICS) : SA000023H10 S IC ICS9LPRS488CKLFT MLF 72P CLK GEN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	68M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)
GPP_REFCLK	NC	100M DIFF	NC
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF

SEL_HTT66	1	single-ended 66MHz HTT output
	0*	differential 100MHz HTT output
SEL_SATA	1*	NON SPREAD 100M SATA SRC6 output
	0	SPREAD 100M SATA SRC6 output

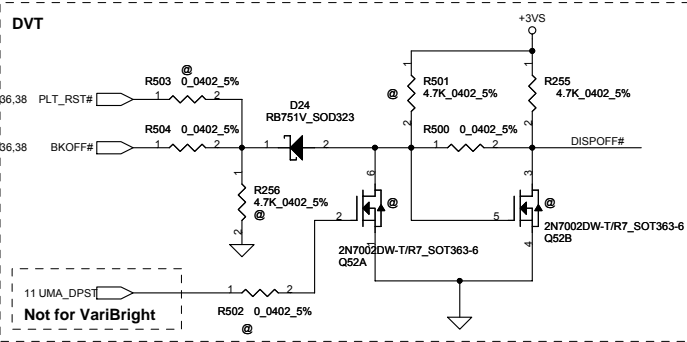
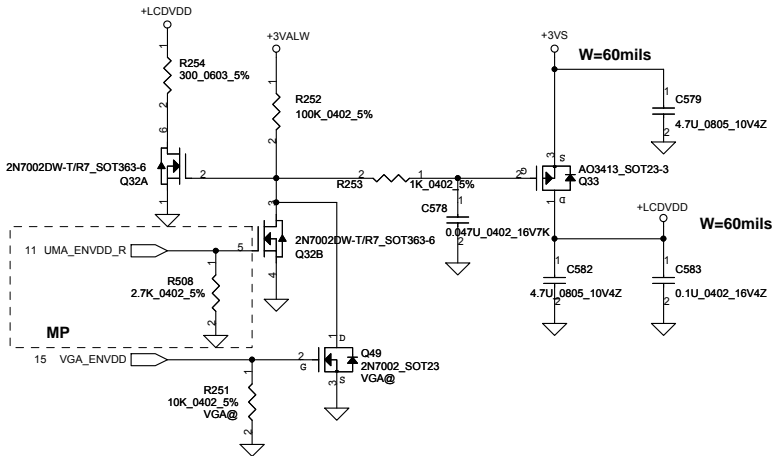
27M_SEL	1*	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC 7 output

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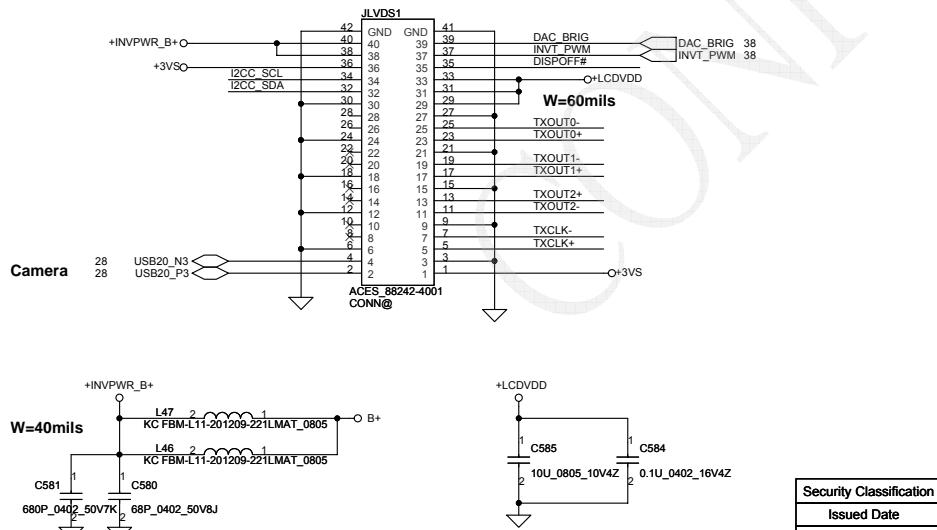
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hexainf@hotmail.com
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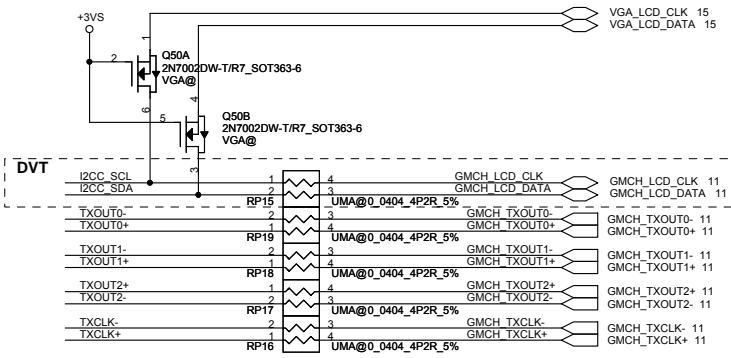
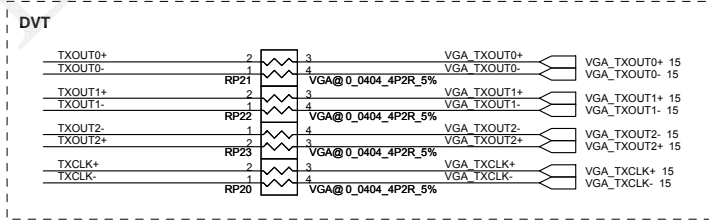
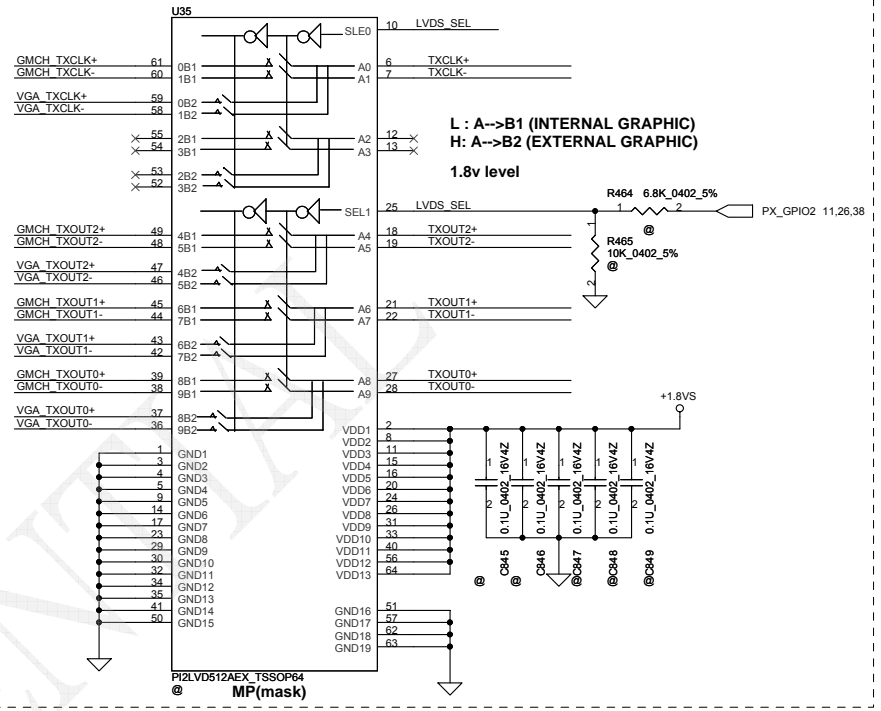
LCD POWER CIRCUIT



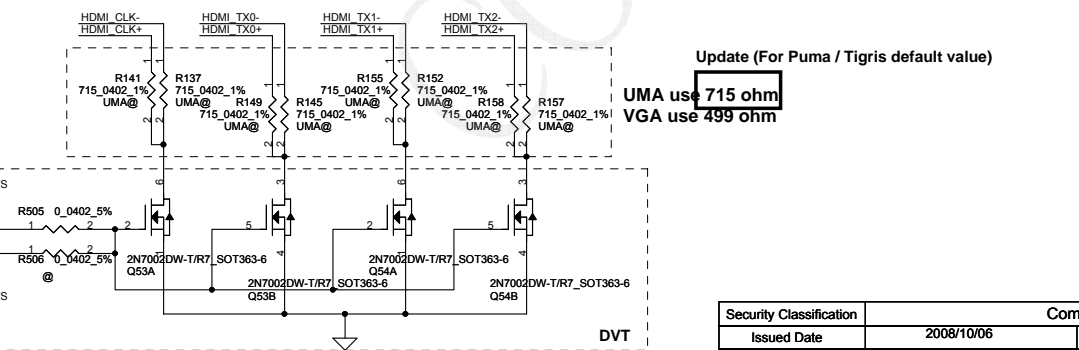
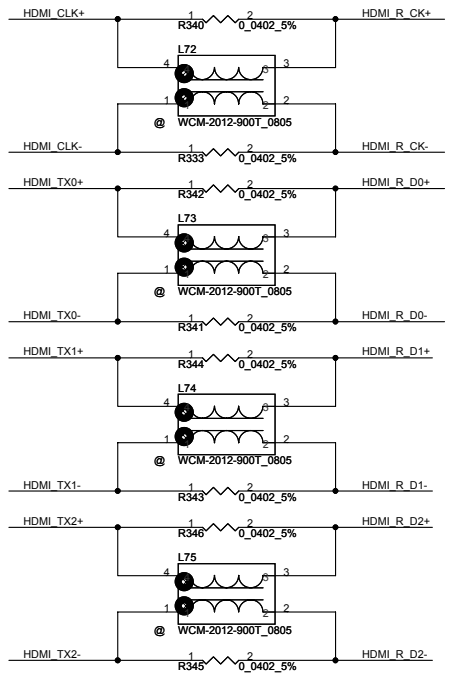
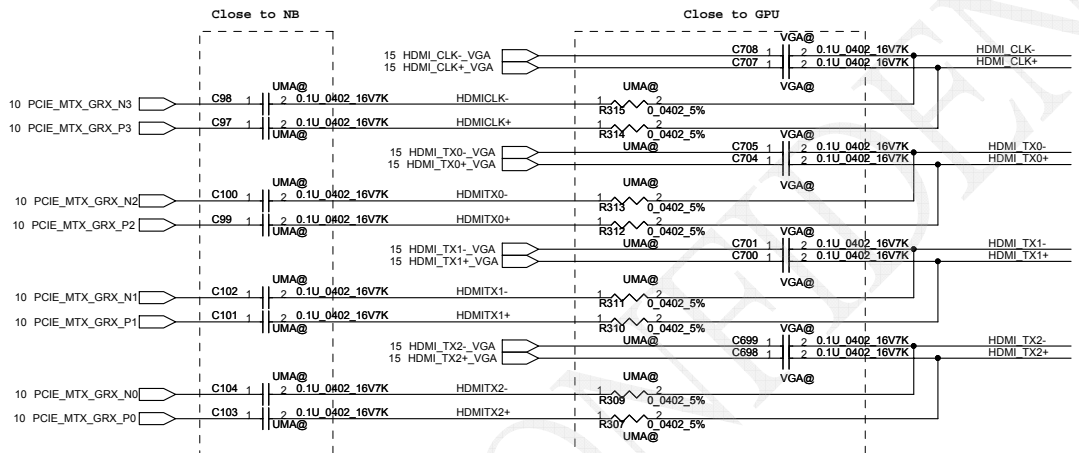
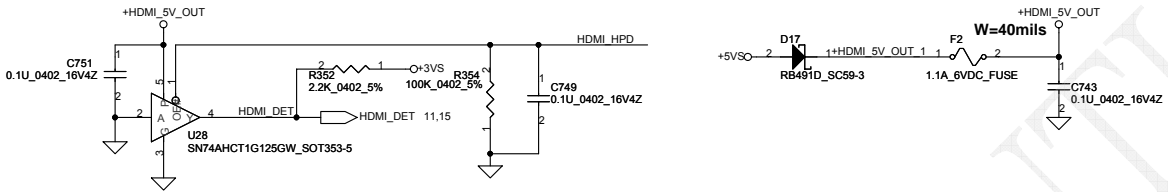
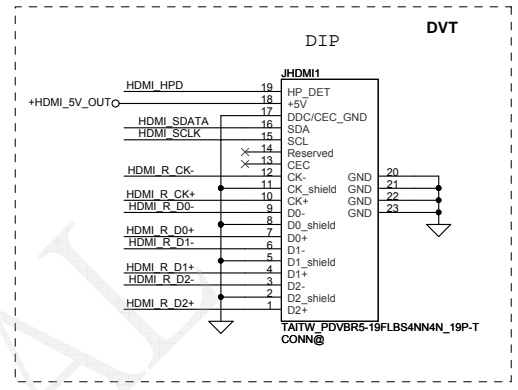
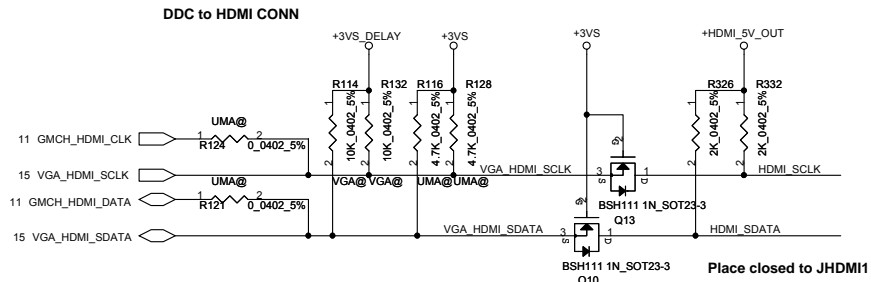
LCD/PANEL BD. Conn.



DVT

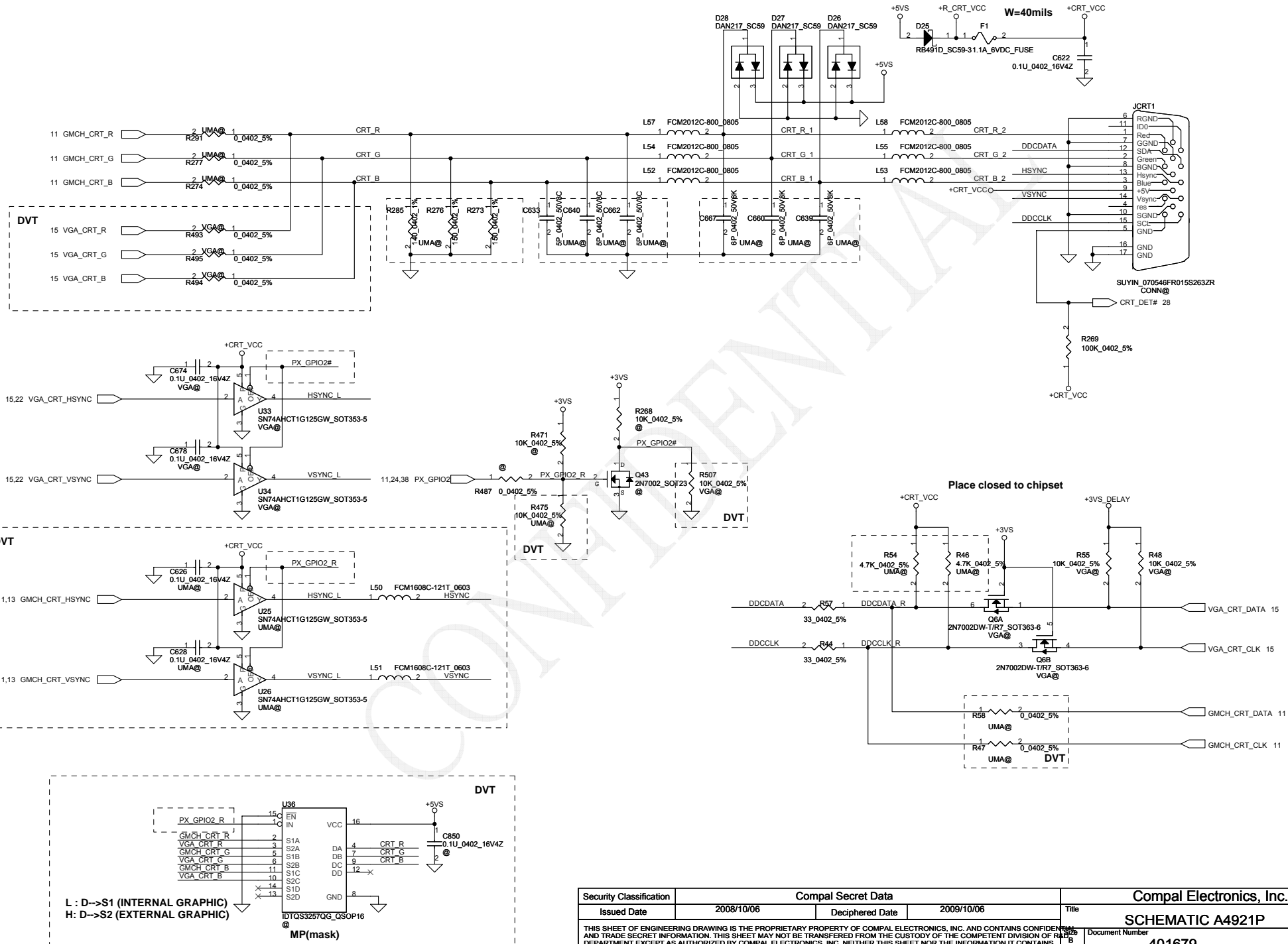


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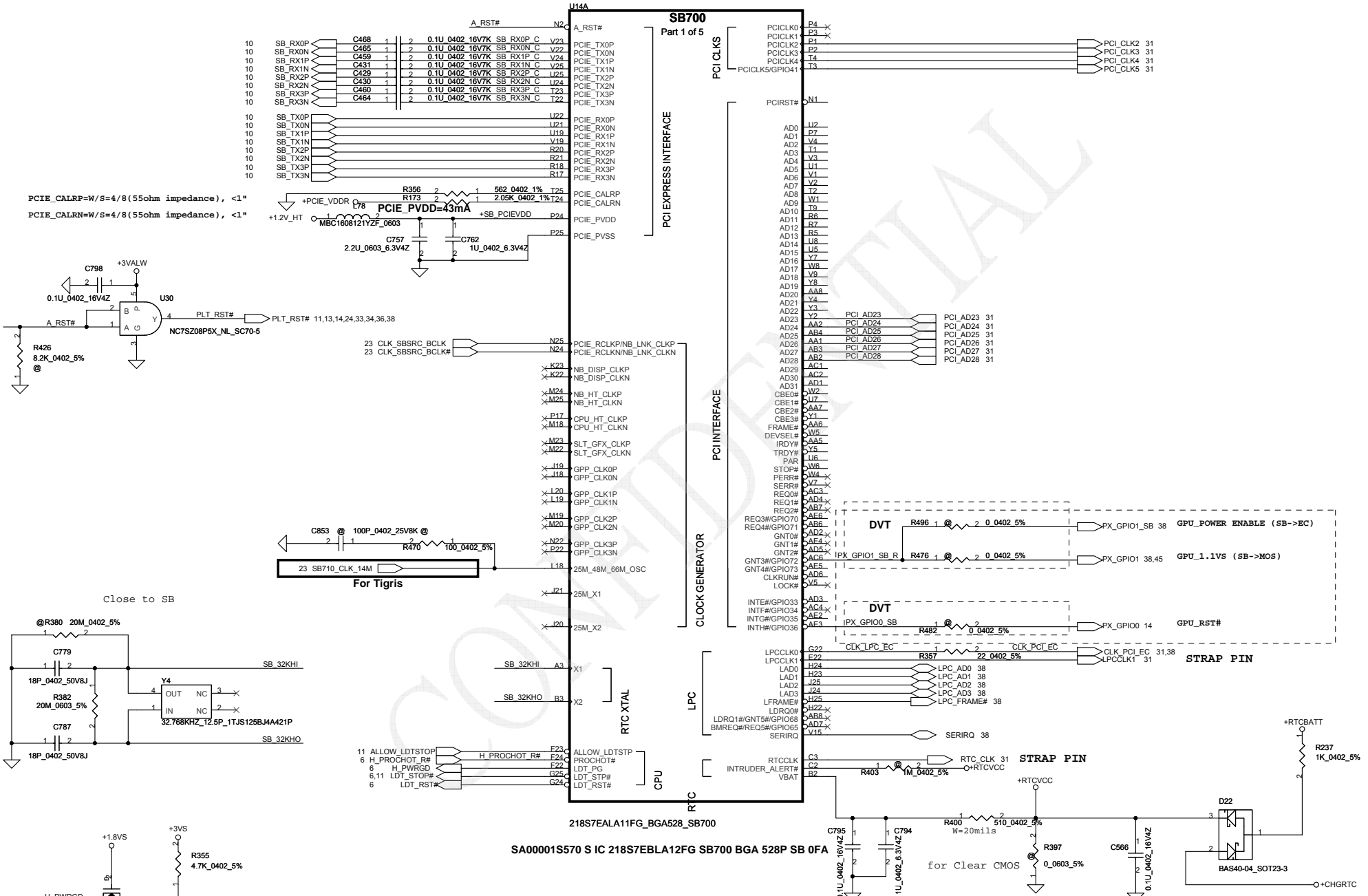


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CRT CONNECTOR



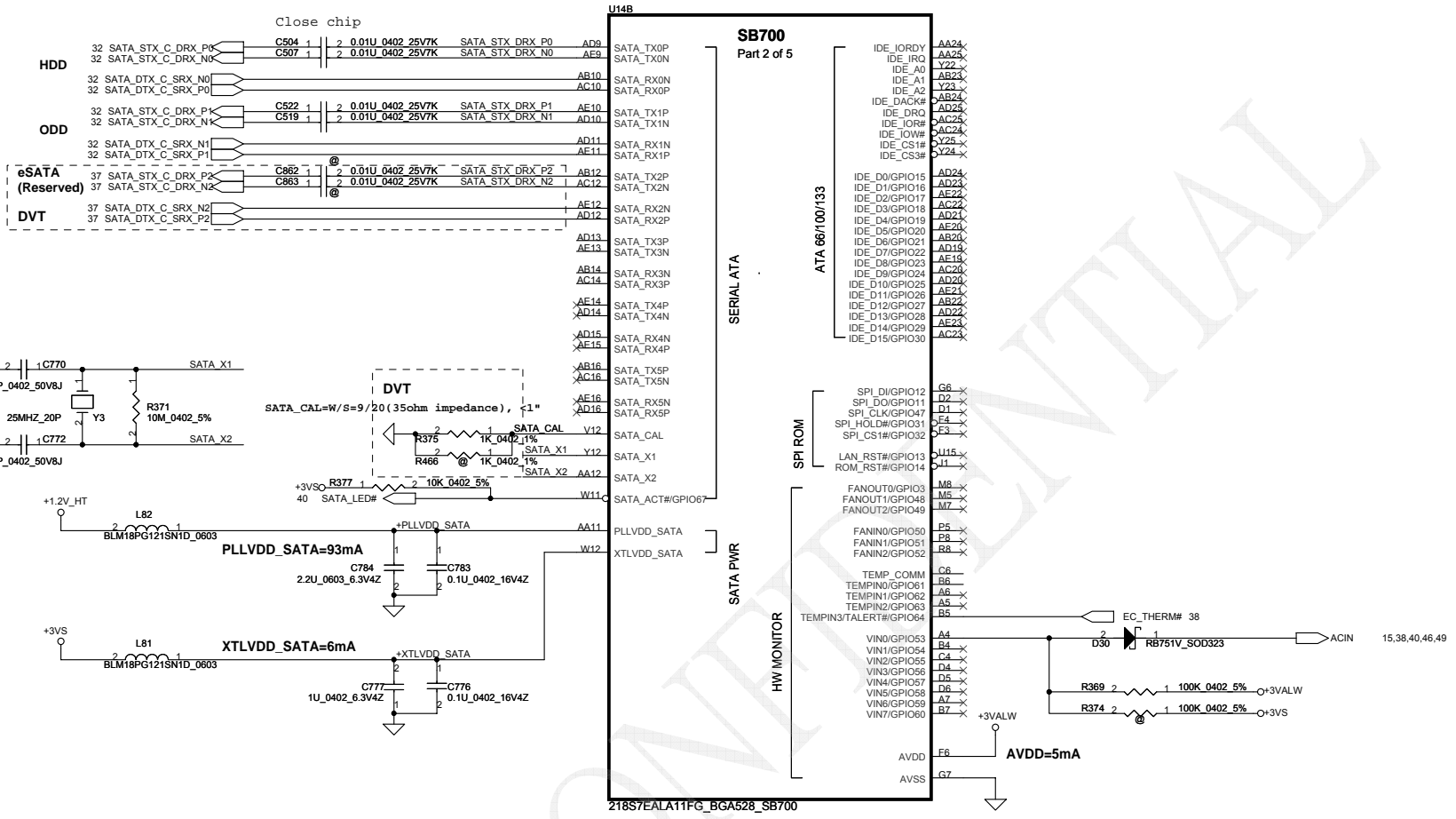
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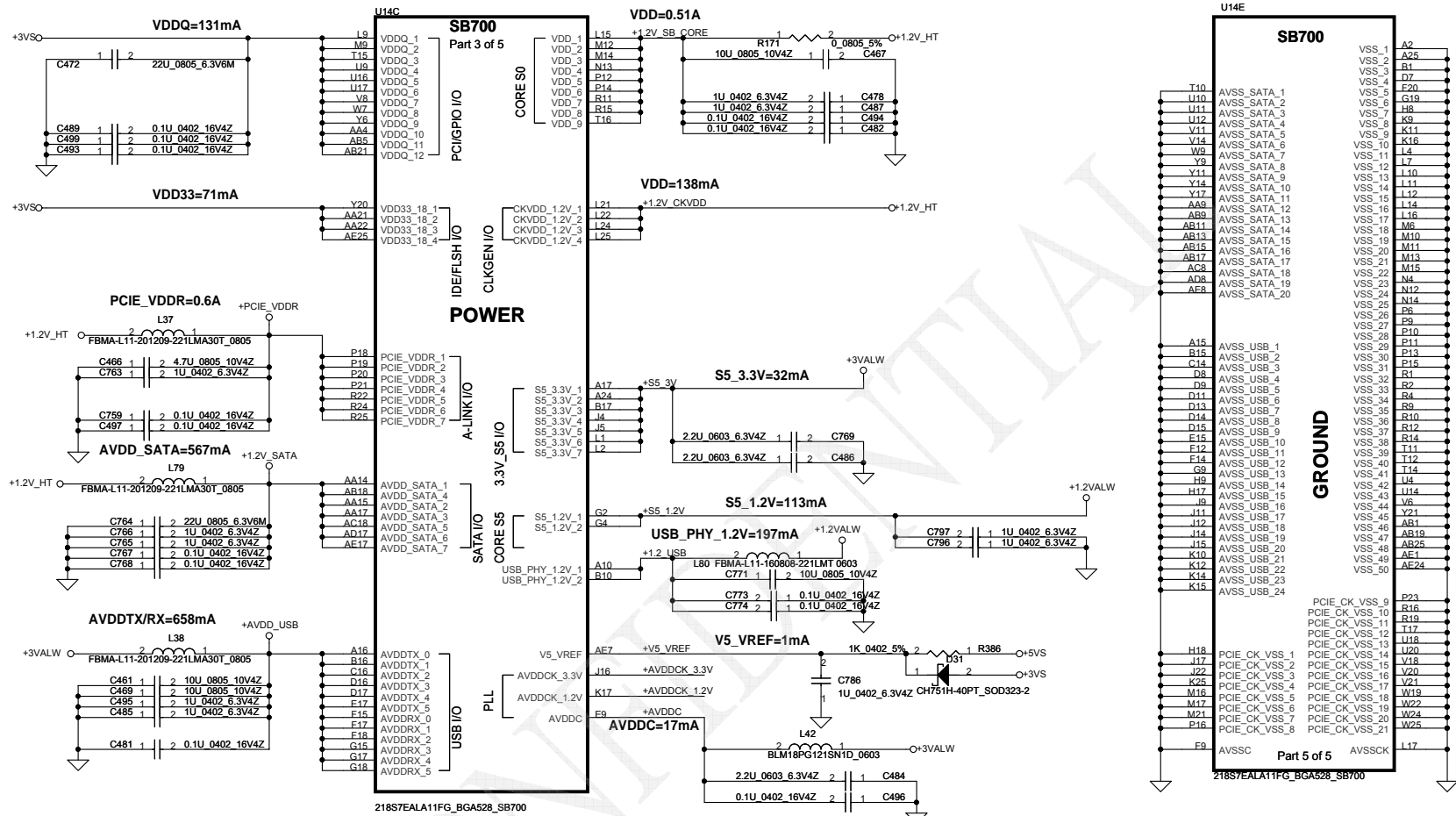
hexainf@hotmail.com
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level shift to ISL6265

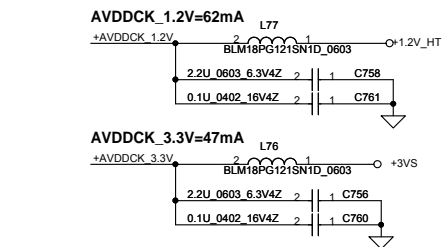


Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 1	Secondary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller
Port 4	Primary (Secondary) master	PATA controller
Port 5	Primary (Secondary) slave	PATA controller

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218S7EALA11FG_BGA528_SB700

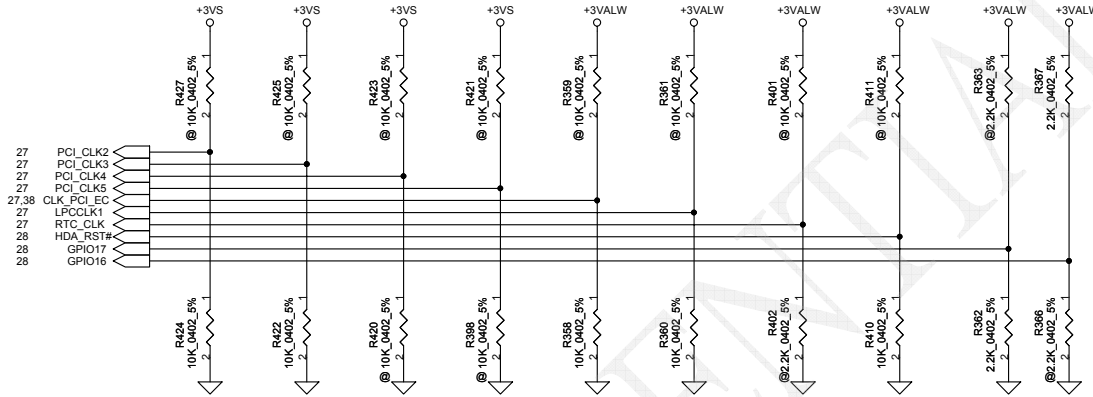


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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

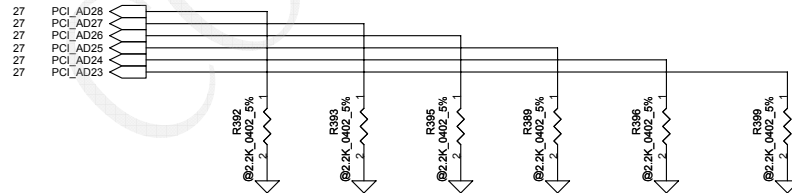
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default L,NC) L,L = FWH ROM



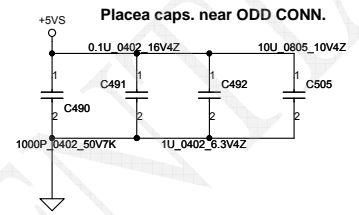
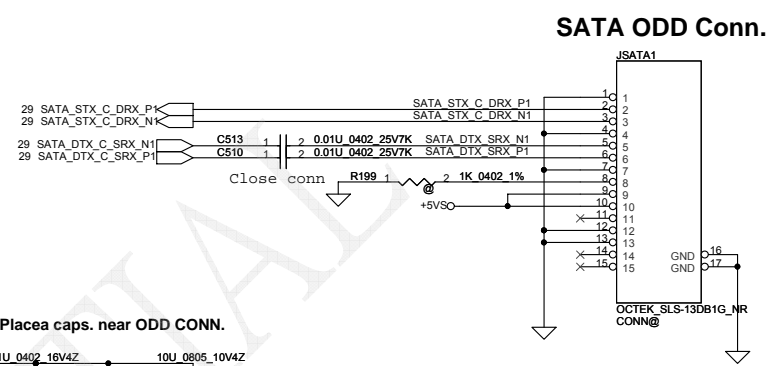
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

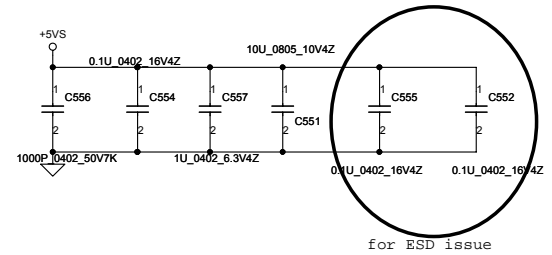
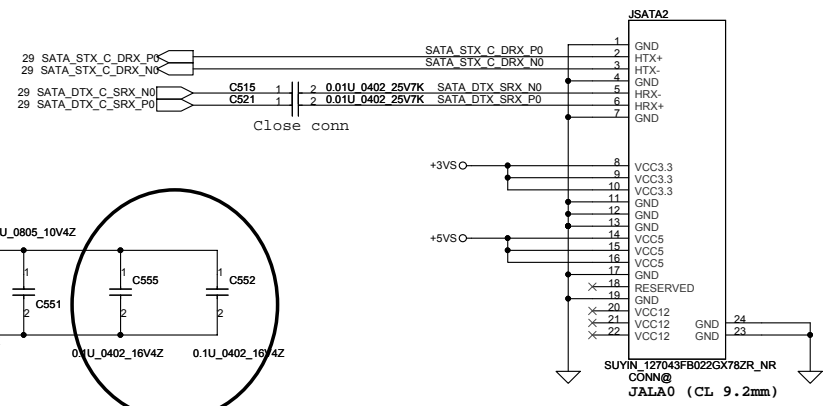
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



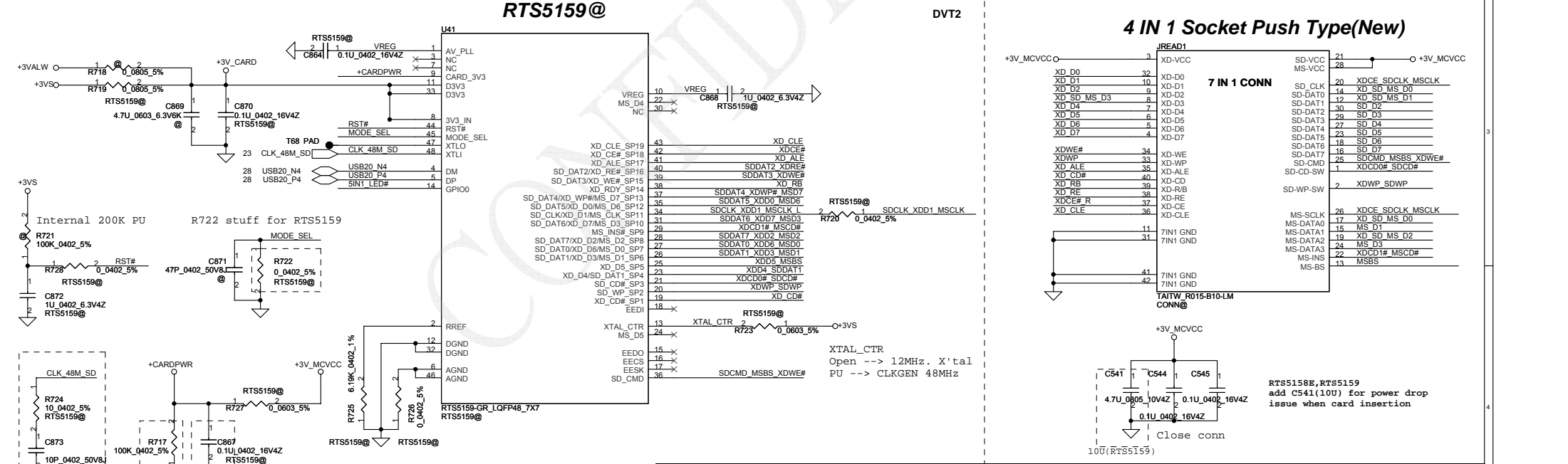
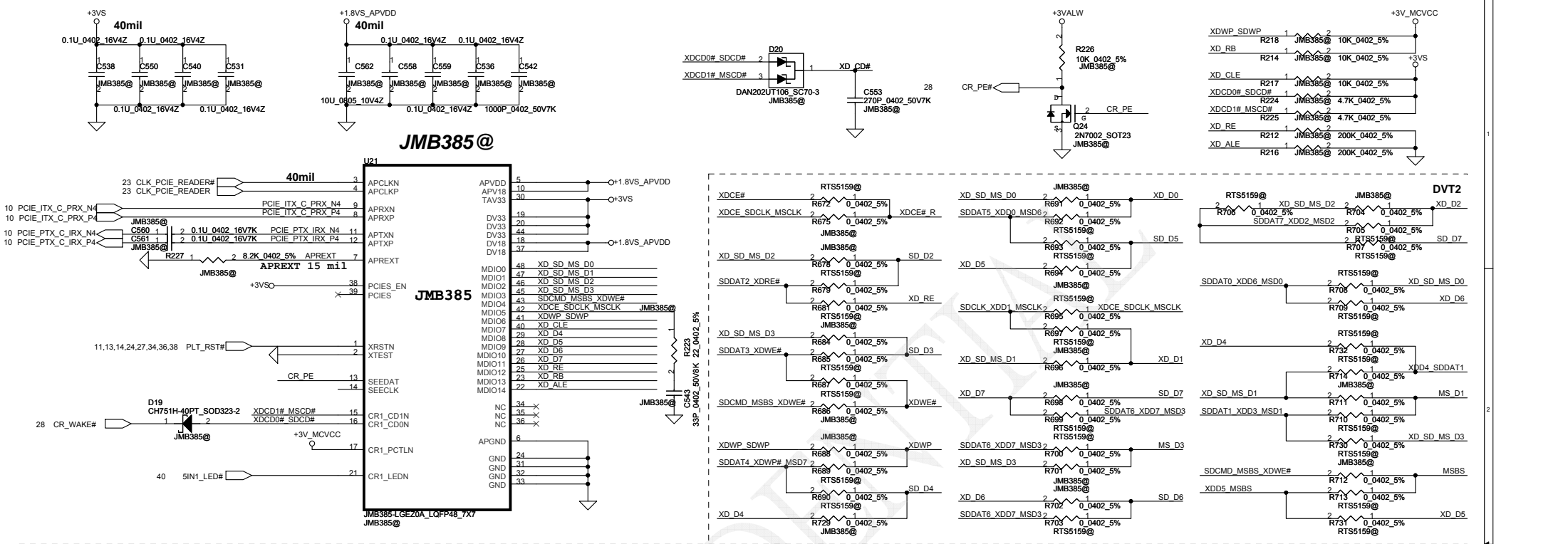
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SATA HDD Conn.



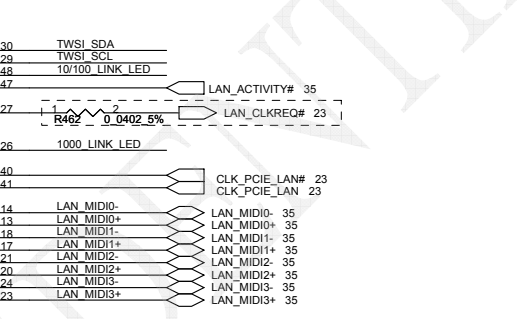
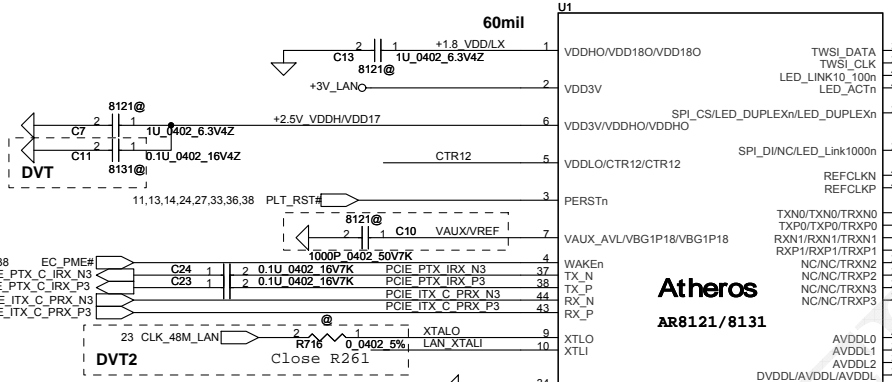
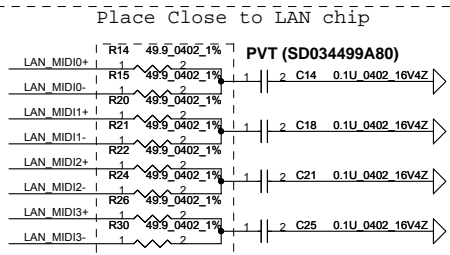
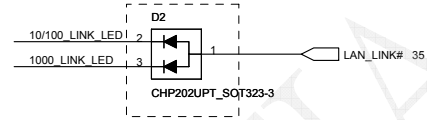
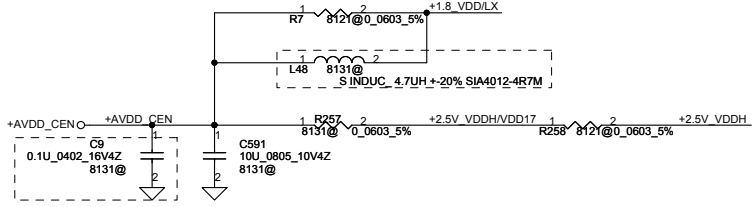
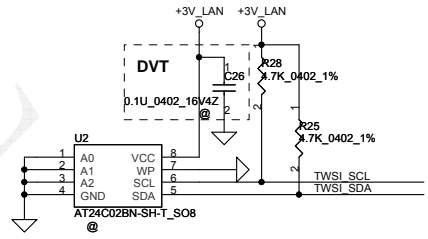
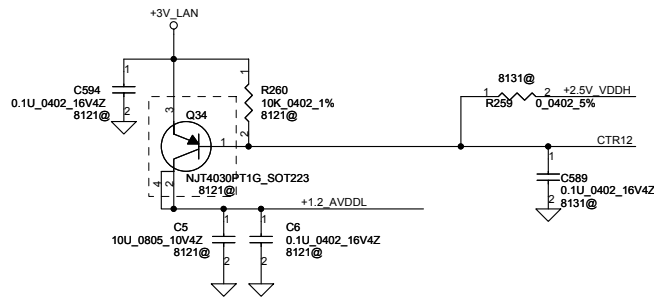
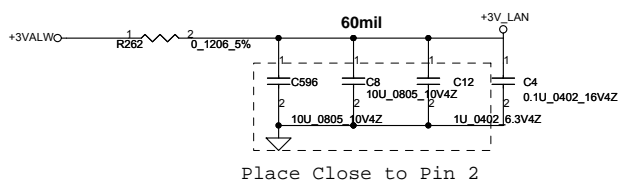
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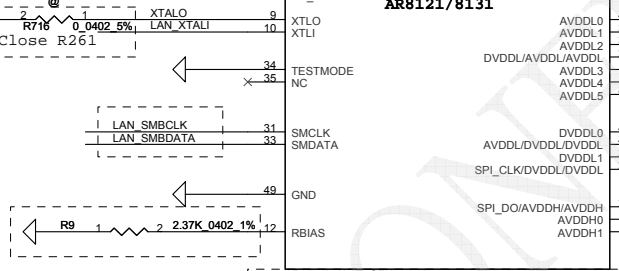
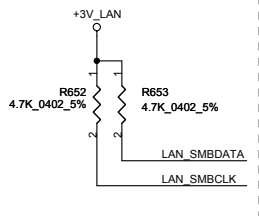
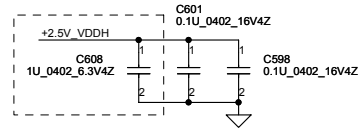
hexainf@hotmail.com
GRATIS - FOR FREE

SCHEMATIC A4921P

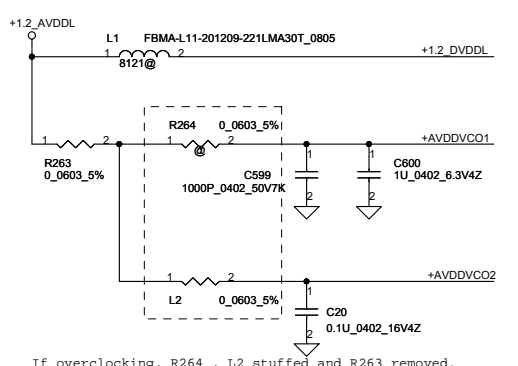
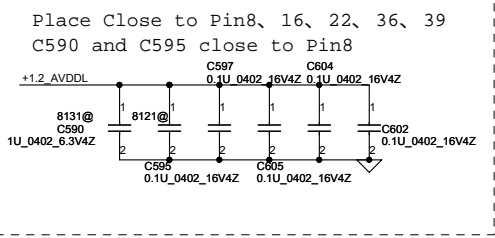
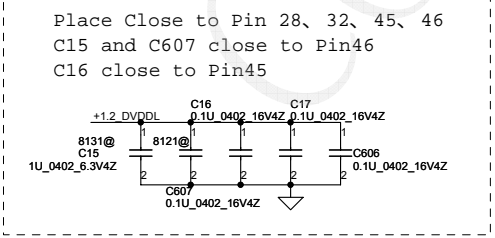


Atheros
AR8121/8131

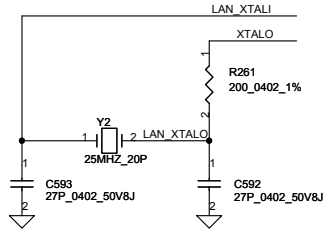
Place Close to Pin15, 19, 25
C608 close to Pin15



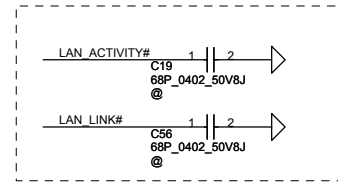
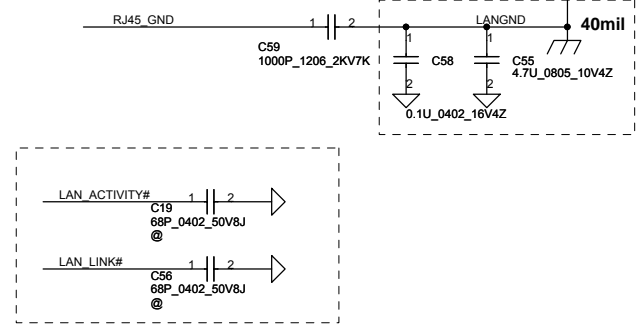
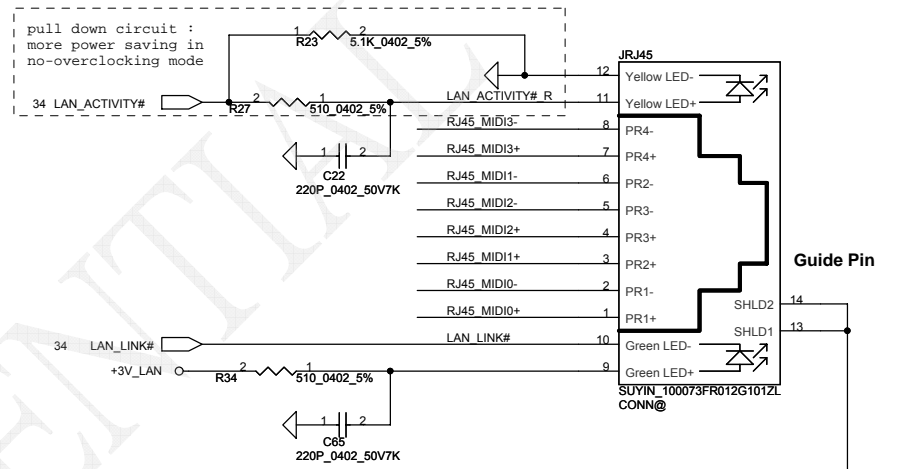
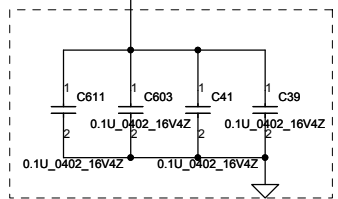
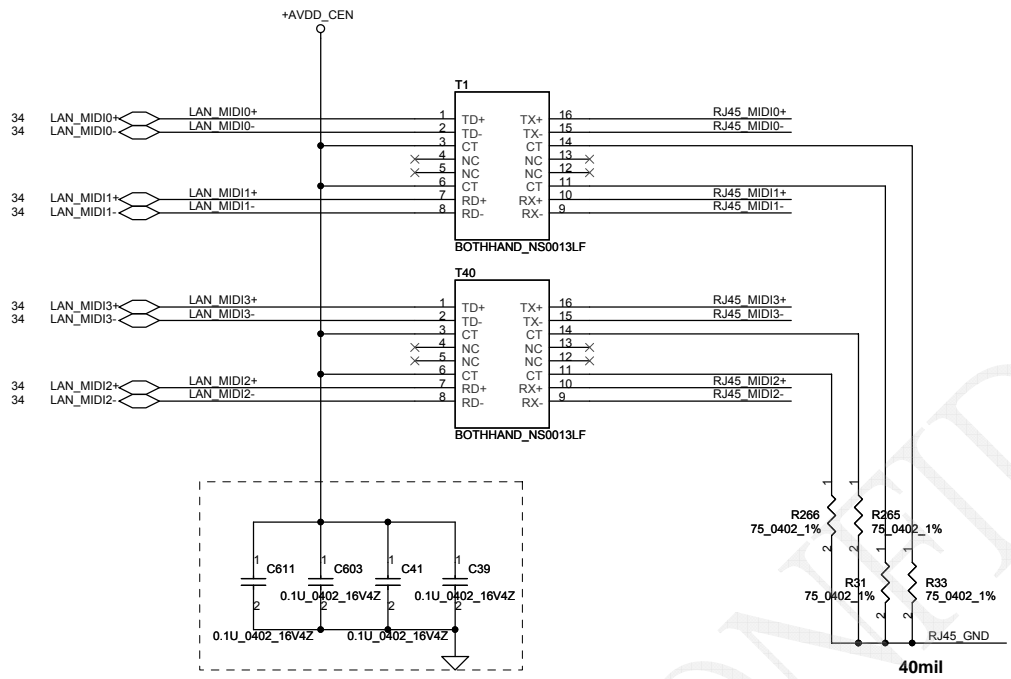
AR8131L-AL1E_QFN48_6X6
SA000038N00 S IC AR8131L-AL1E QFN 48P E-LAN CTRL PVT
SA000025M00 S IC AR8121-AL1E QFN 48P E-LAN CTRL



If overclocking, R264, L2 stuffed and R263 removed.
If not overclocking, R263, L2 stuffed and R264 removed.
AR8131:L2=0ohm (more power saving mode)



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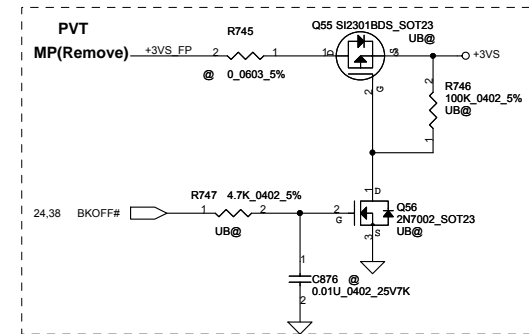
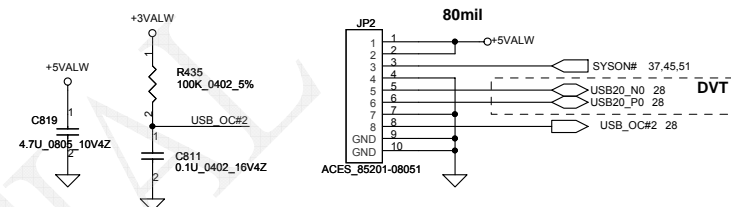
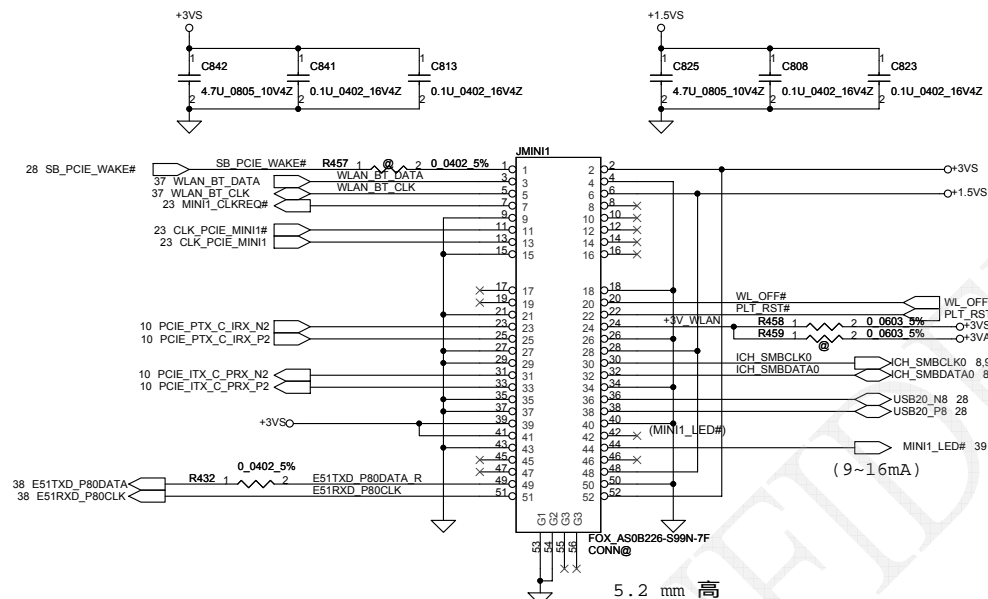
Place close to TCT pin

For EMI

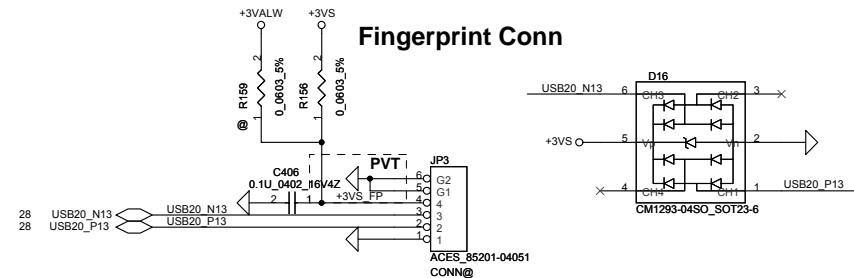
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For Wireless LAN

To USB/B Connector

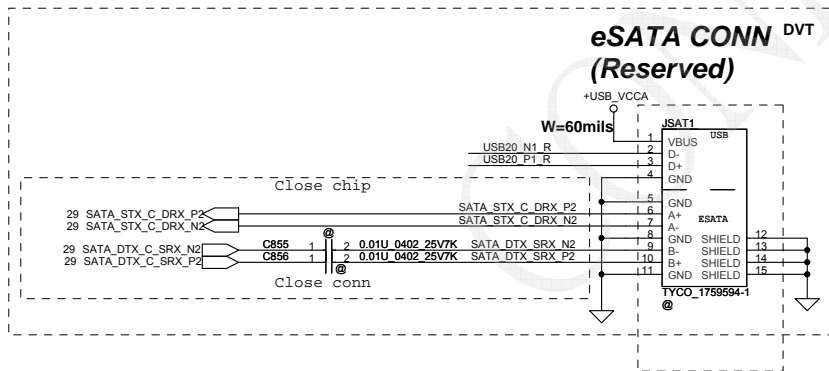
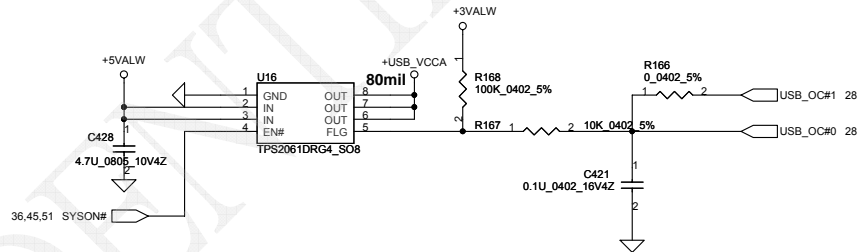
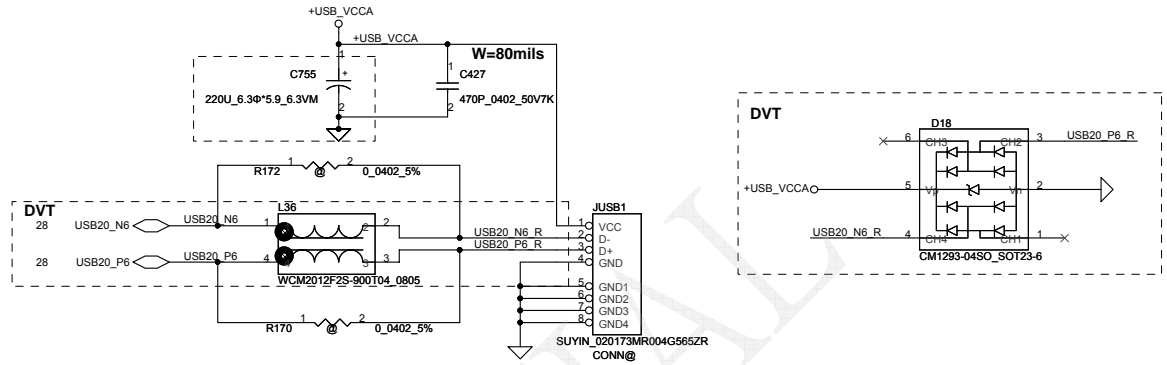
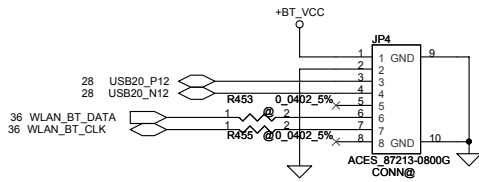
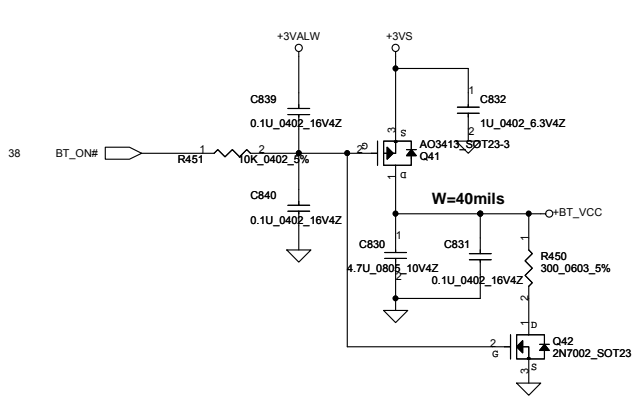


Fingerprint Conn

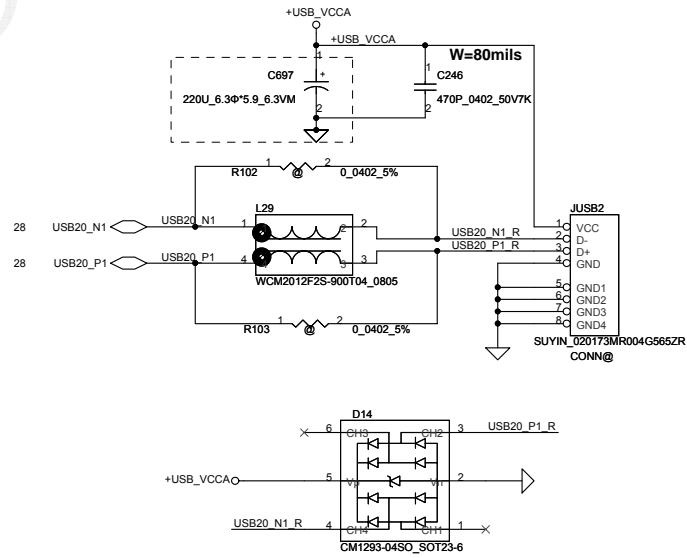


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	Normal
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

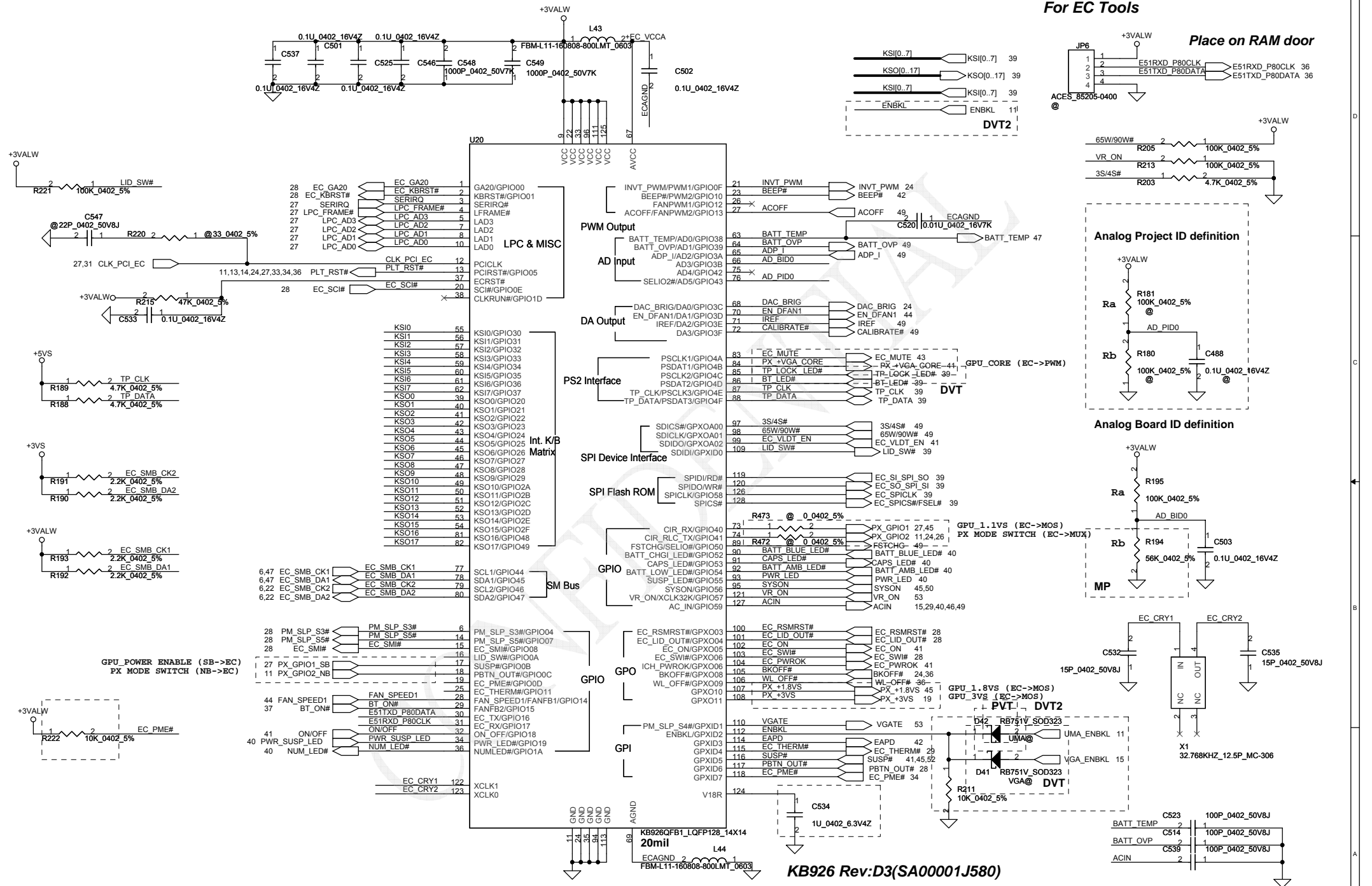
Bluetooth Conn.



DVT2
(PCB footprint : TYCO_1909574-1_11P-T)



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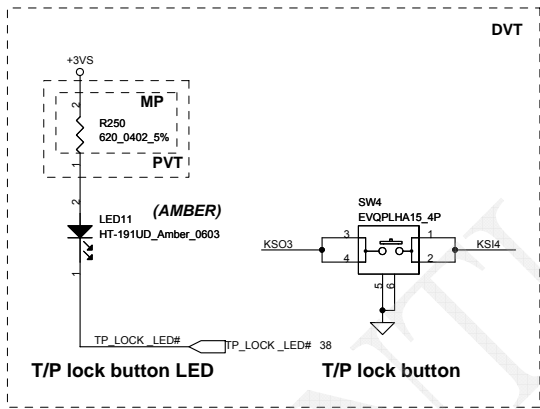
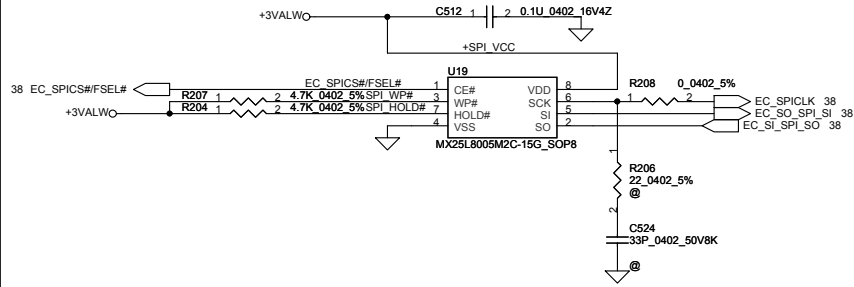
For EC Tools

Place on RAM door

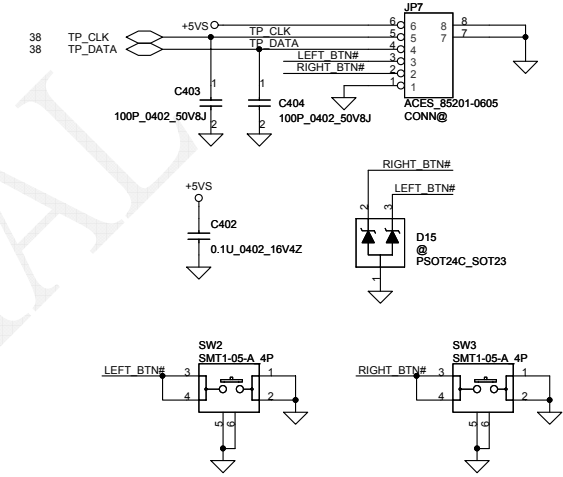
KB926 Rev:D3(SA00001J580)

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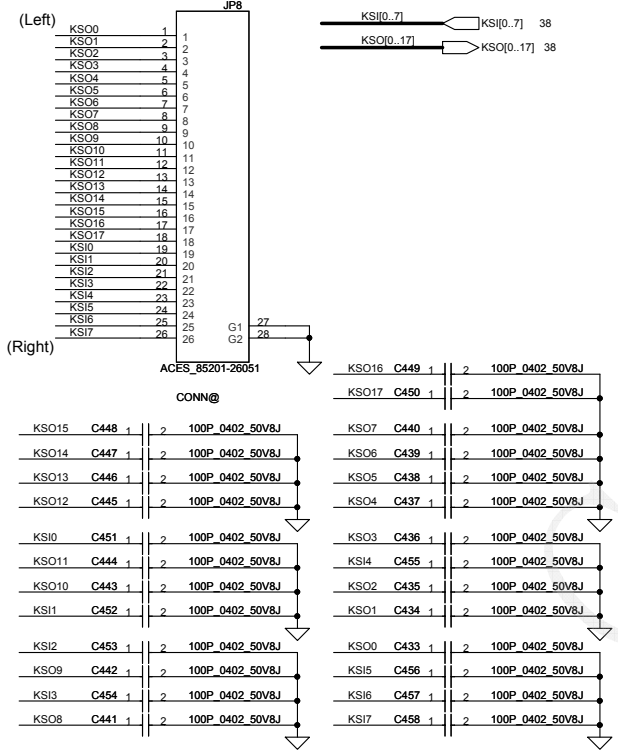
BIOS(SYS / EC / VGA)



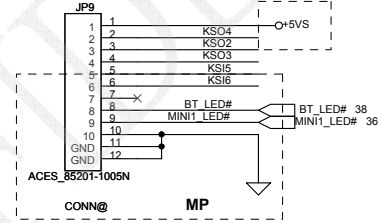
To TP/B Conn.



INT_KBD Conn.

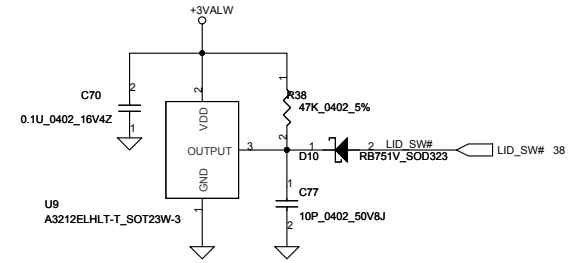


To FUN/B Conn (10PIN)



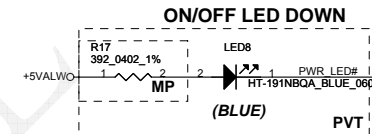
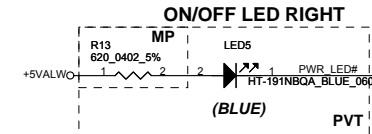
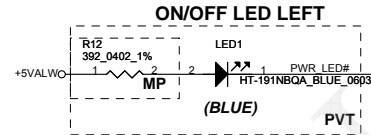
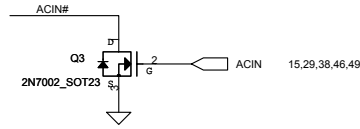
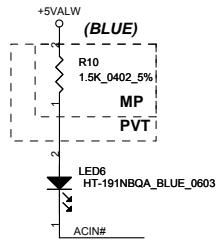
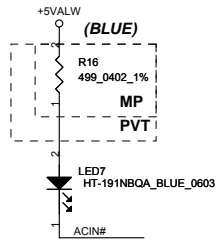
	KSO4	KSO2	KSO3
KSI5	WL_BTN#	Volume Down	Back Up
KSI6	BT_BTN#	Volume Up	Program (KBLG0) Battery (KALG0)
KSI4			T/P lock

Lid Switch (Hall Effect Switch)

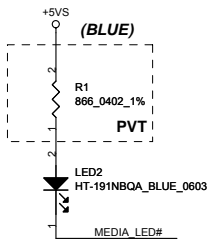


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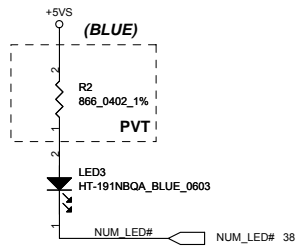
Enlightener LED



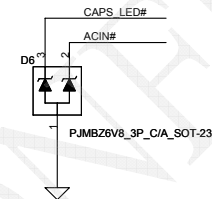
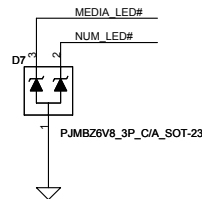
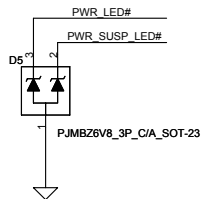
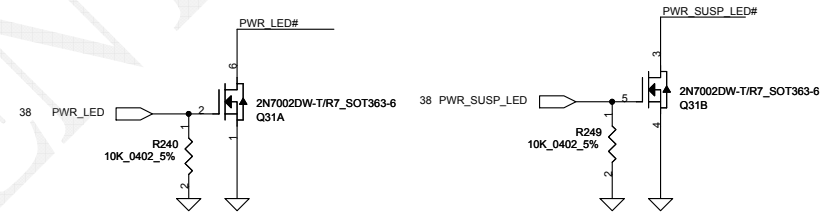
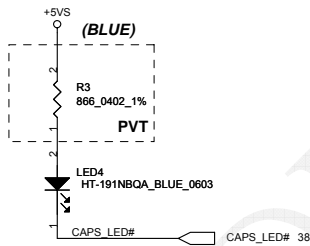
MEDIA_LED



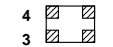
NUM_LED



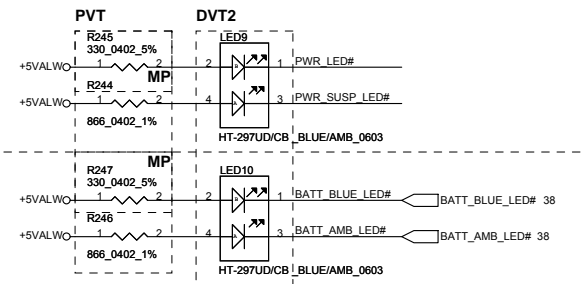
CAPS_LED



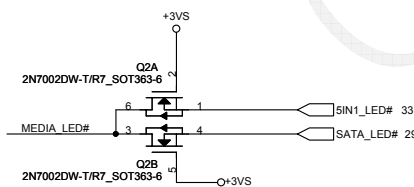
Compal Footprint



Footprint : LED_HT-297DQ-GQ_4P



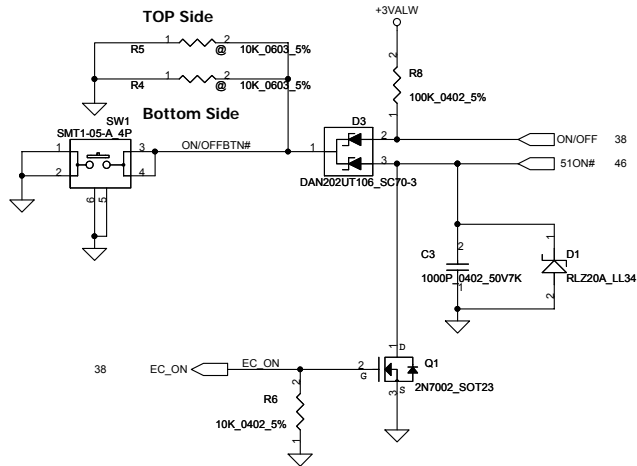
BLUE/AMBER



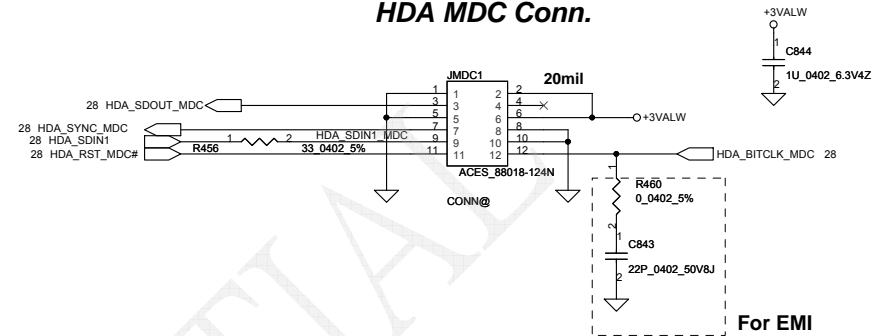
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Power Button

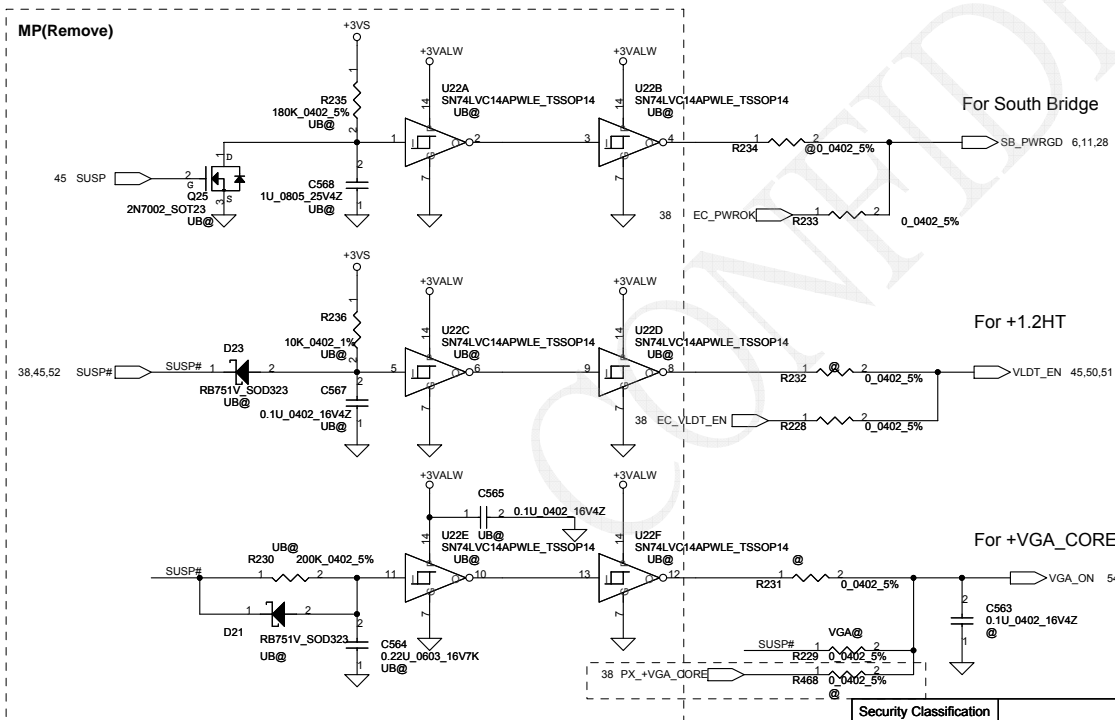
ON/OFF switch



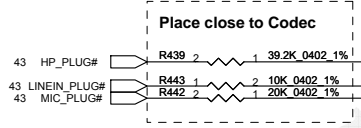
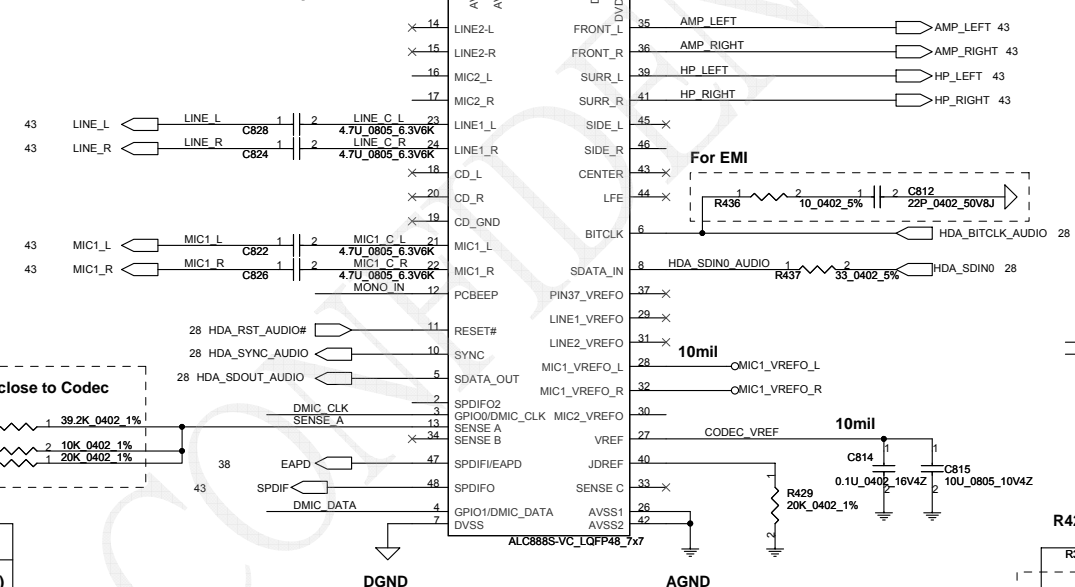
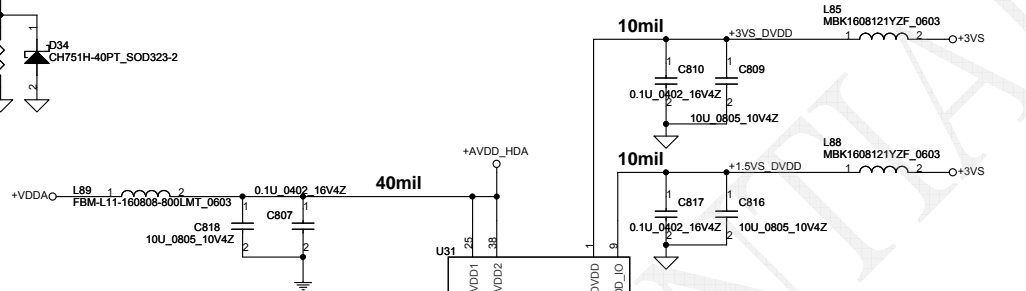
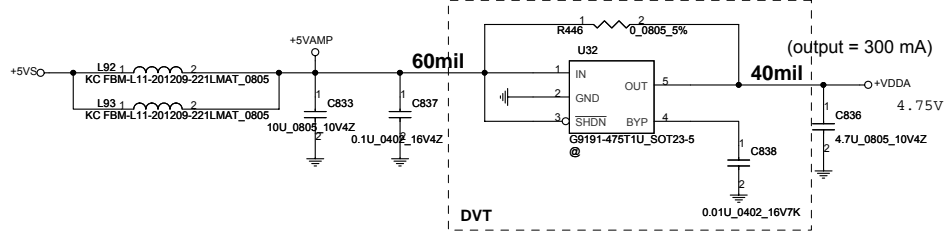
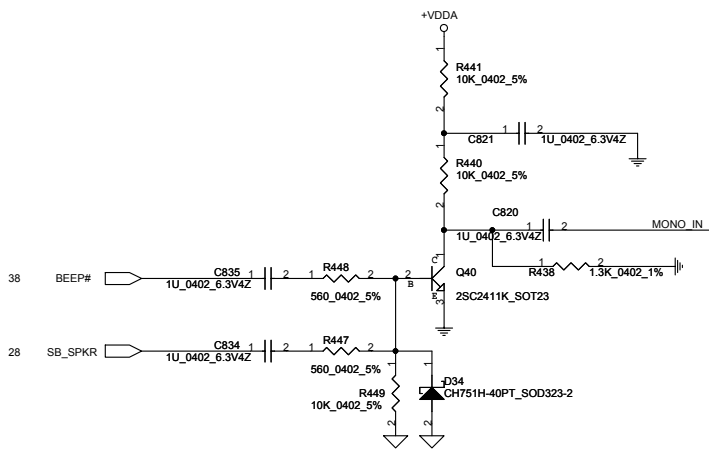
HDA MDC Conn.



Power ON Circuit

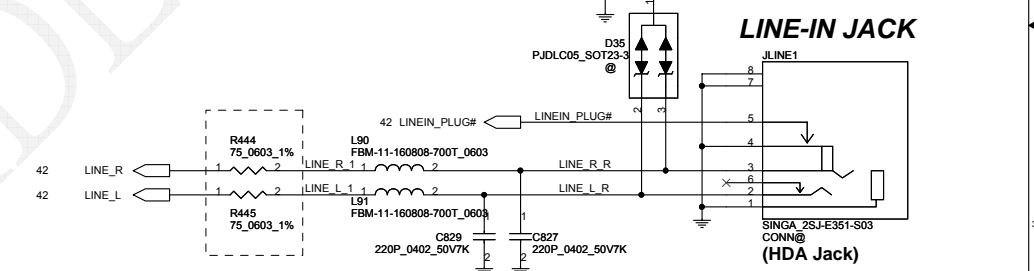
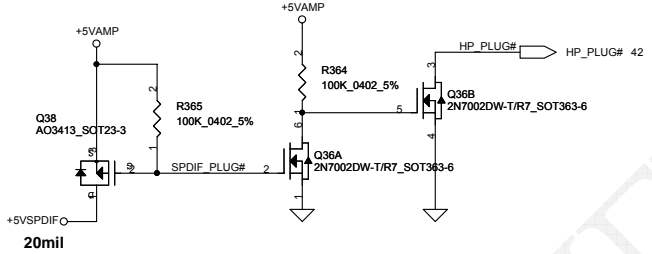
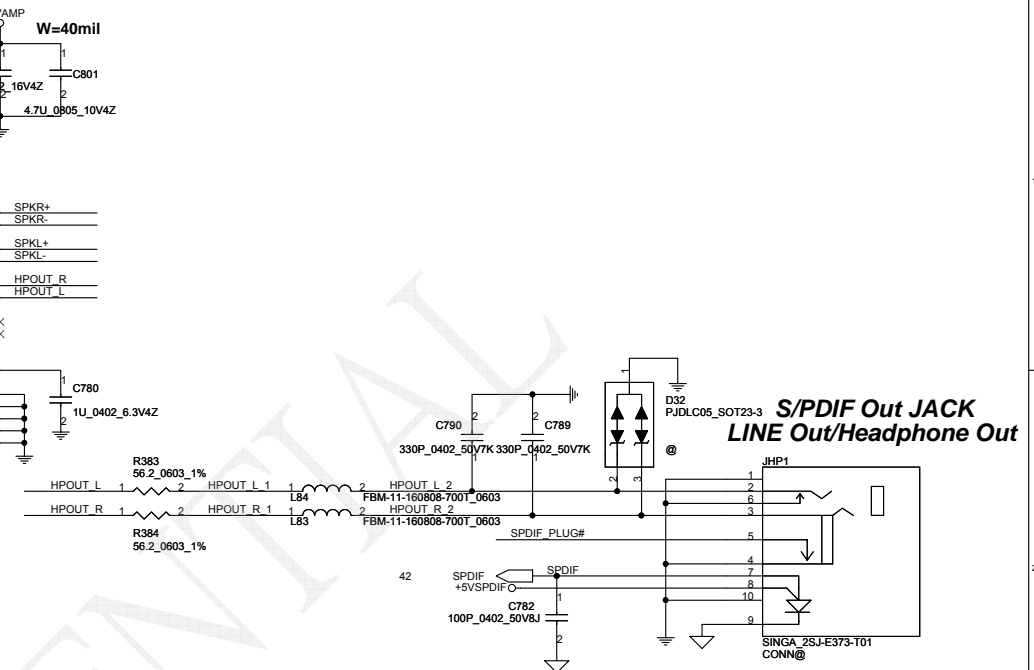
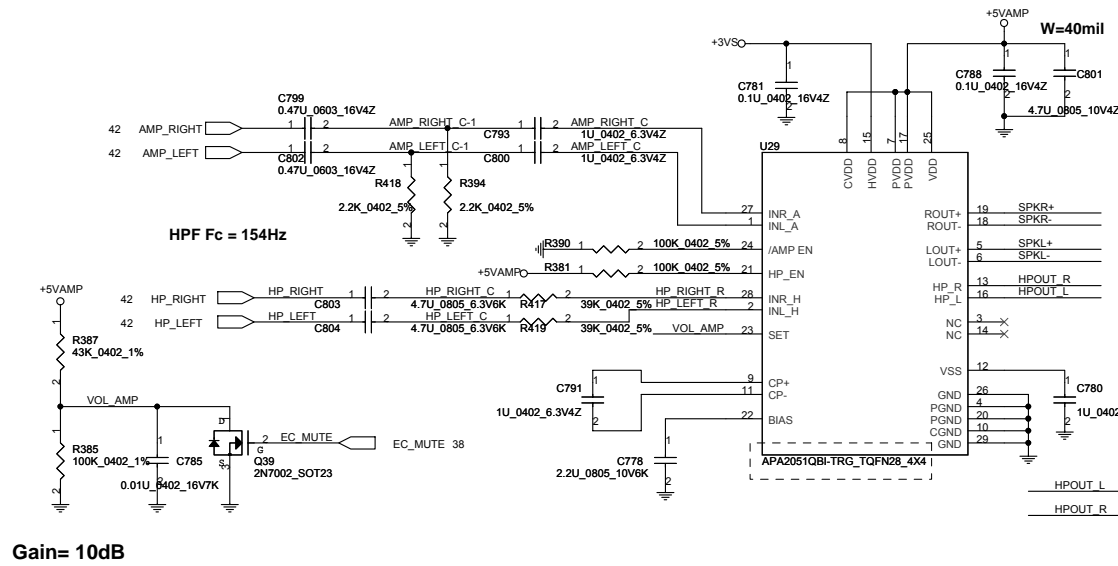


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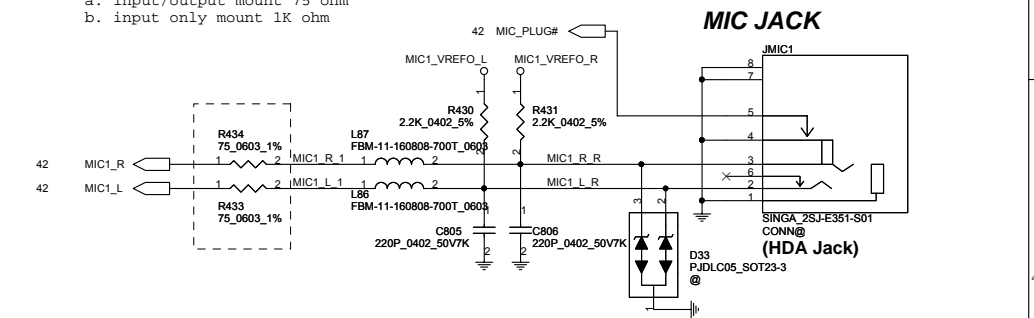


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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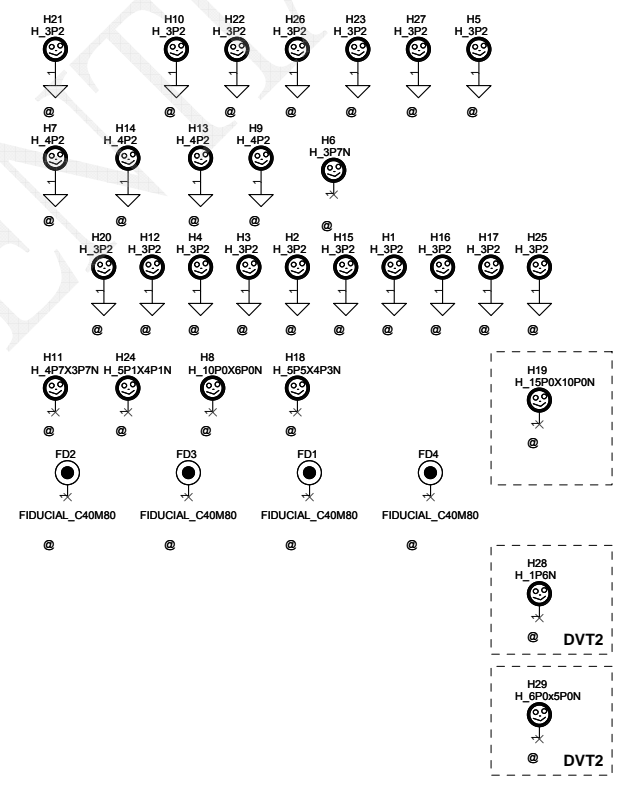
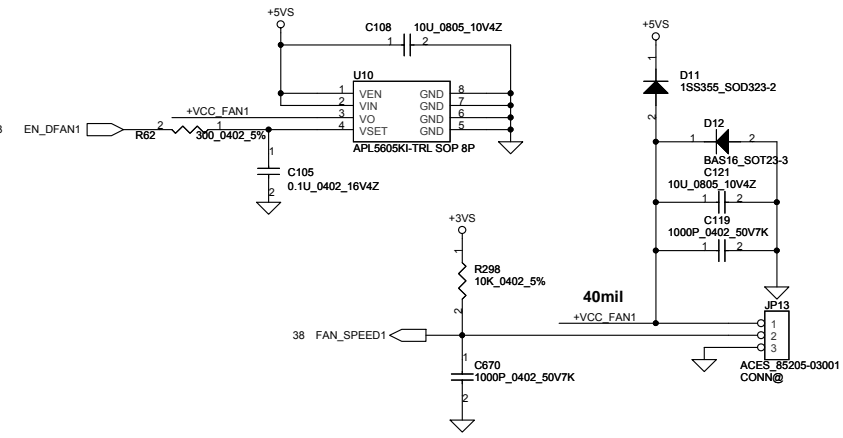


For ESD I/O status:
 a. input/output mount 75 ohm
 b. input only mount 1K ohm



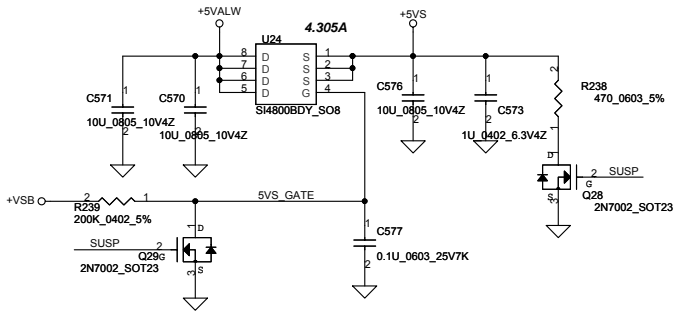
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FAN1 Conn

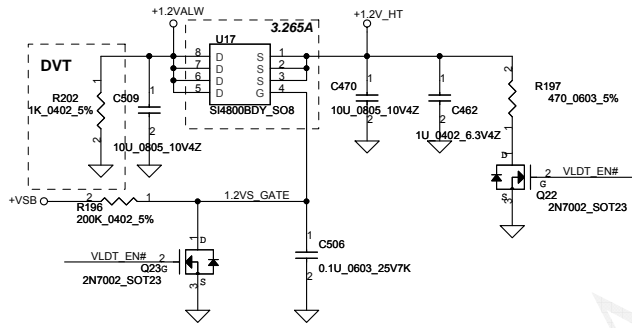


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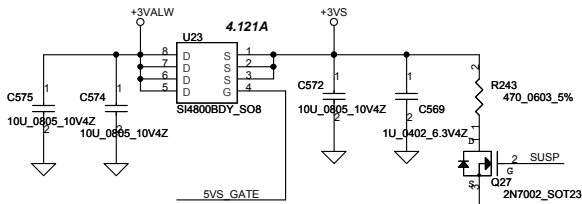
+5VALW TO +5VS



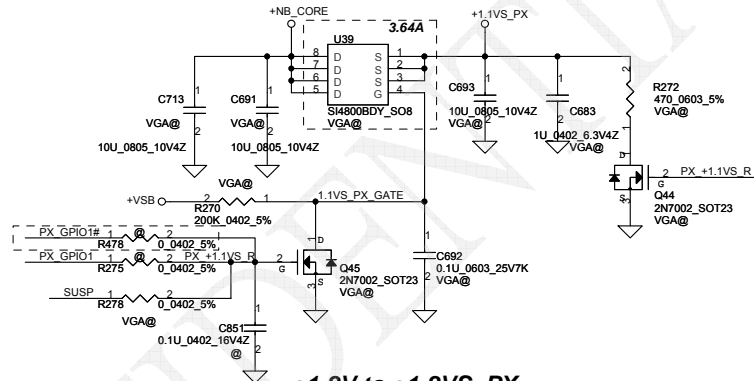
+1.2VALW TO +1.2V_HT



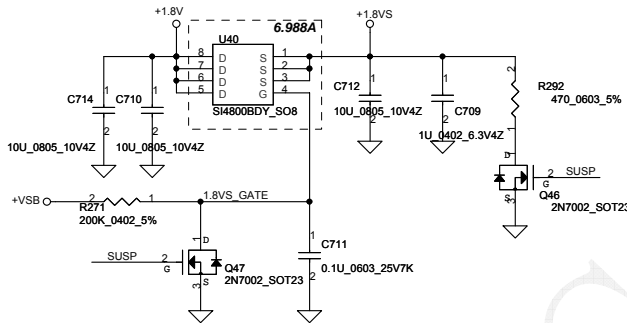
+3VALW TO +3VS



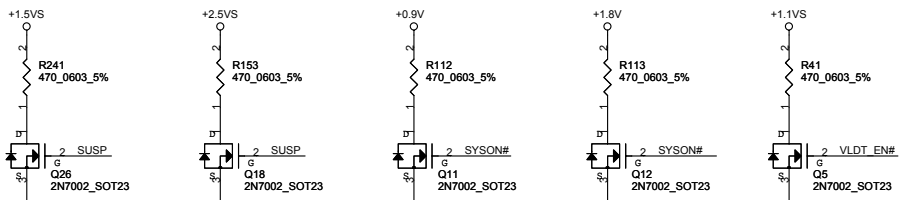
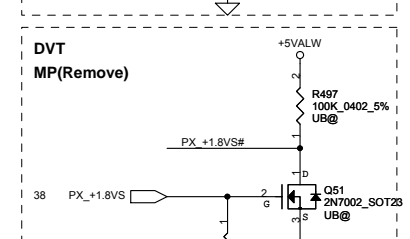
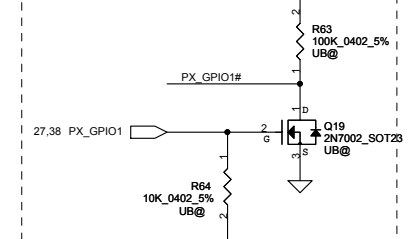
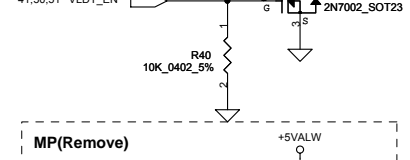
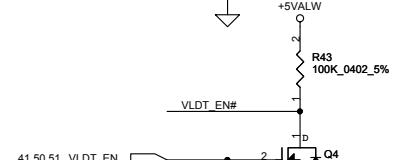
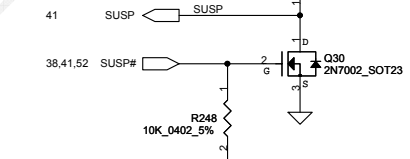
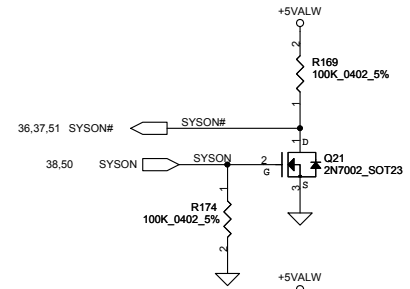
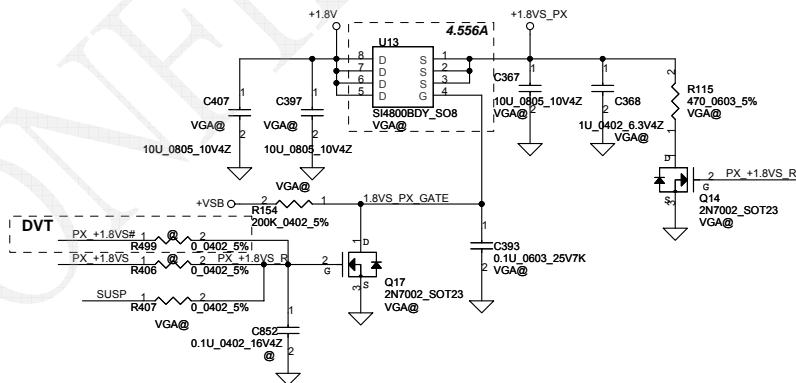
+NB_CORE TO +1.1VS_PX



+1.8V to +1.8VS



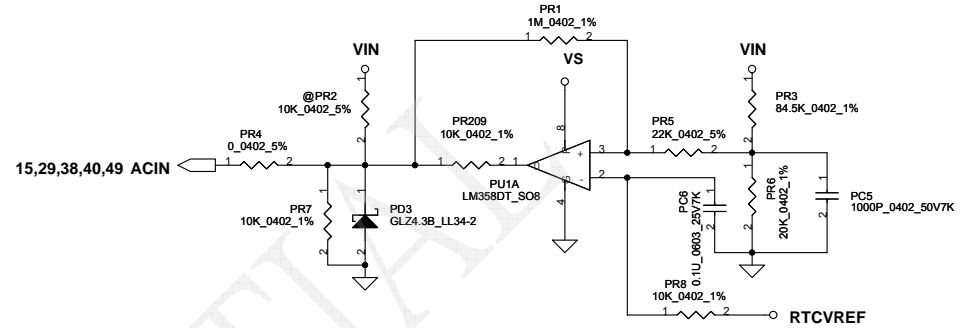
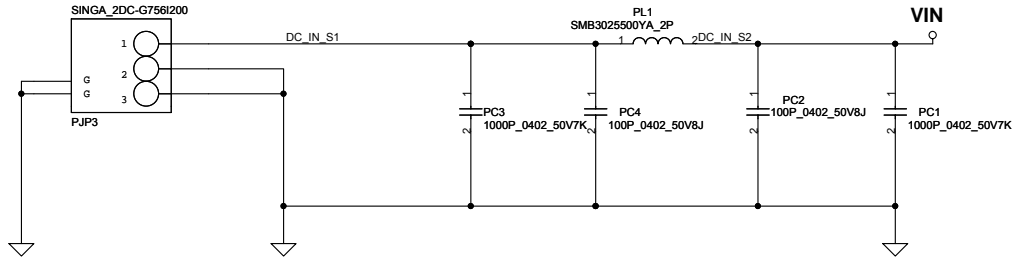
+1.8V to +1.8VS_PX



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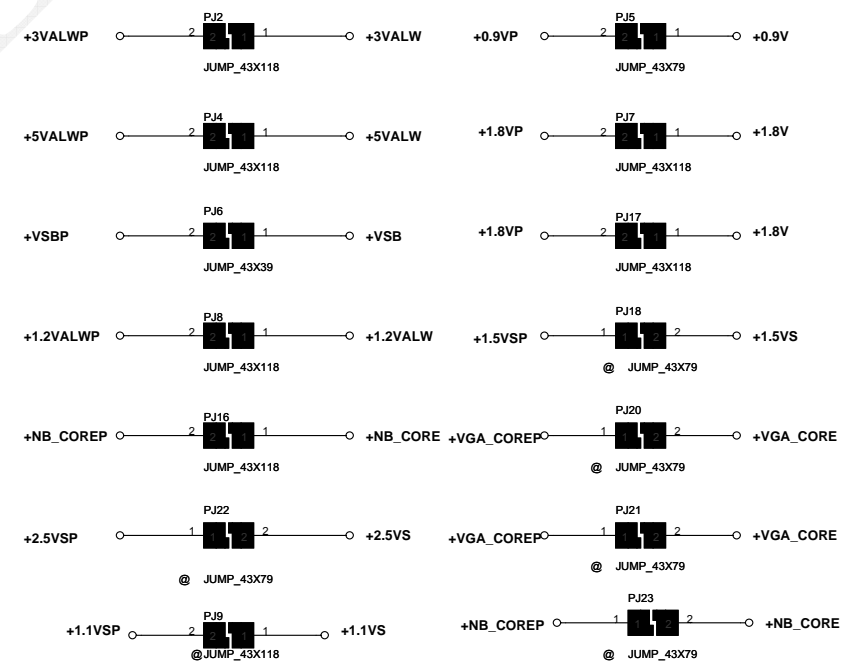
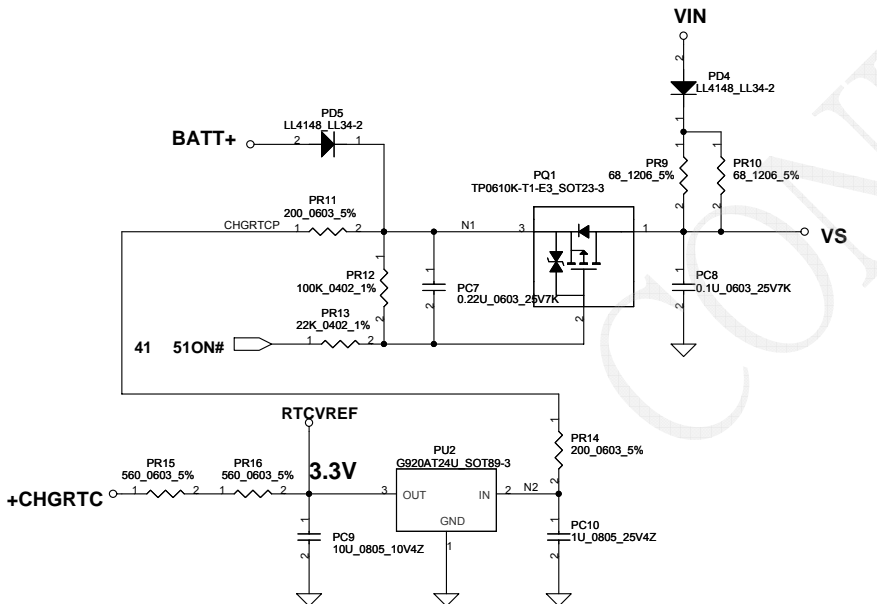
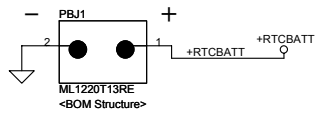
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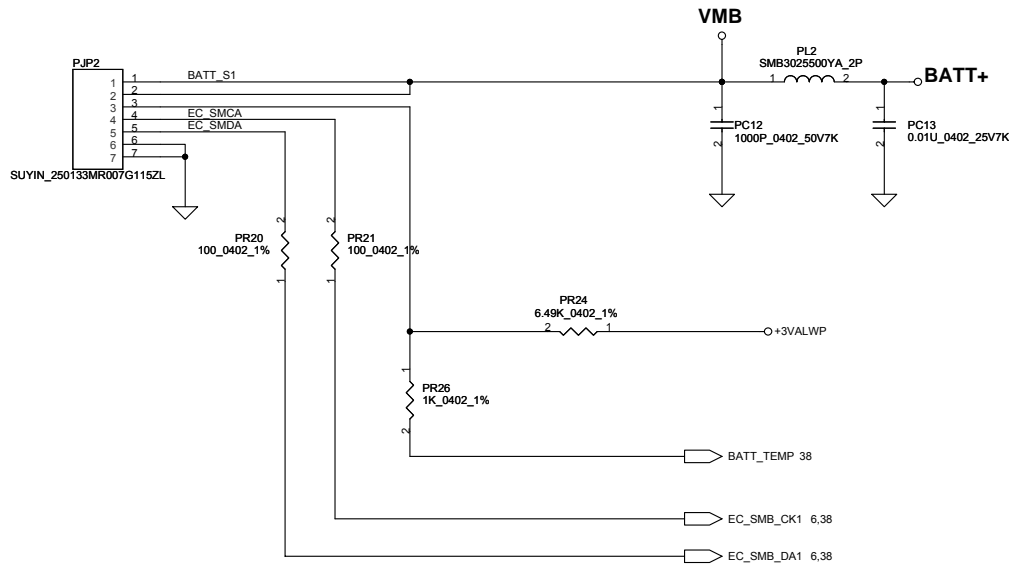
<BOM Structure>
SINGA_2DC-G756I200



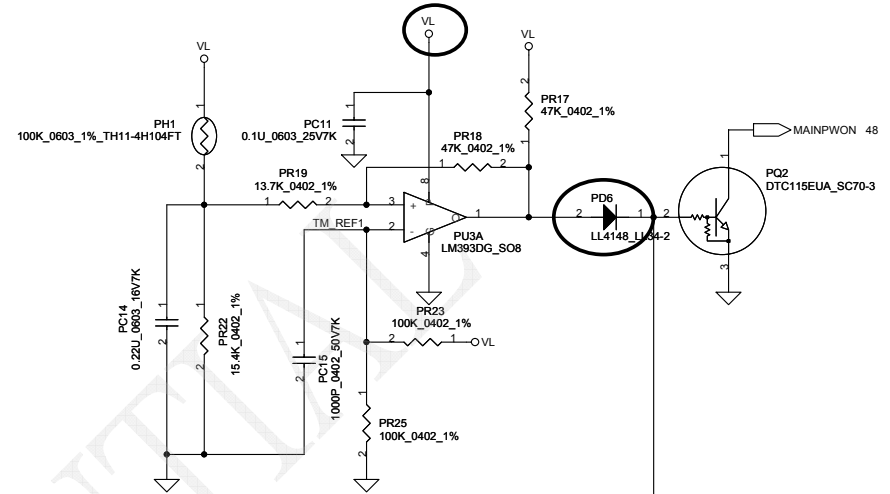
Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

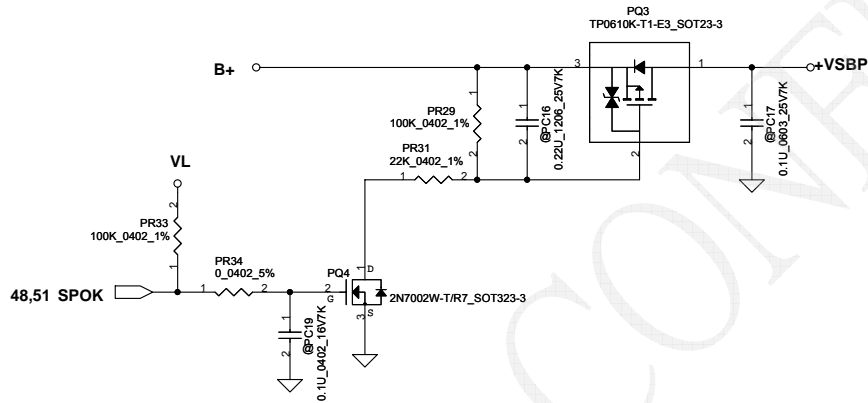
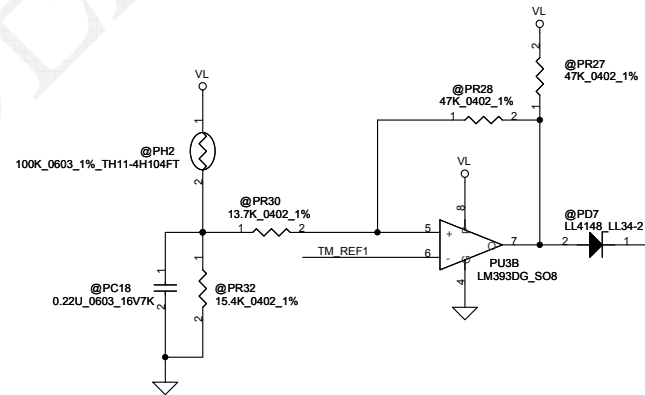




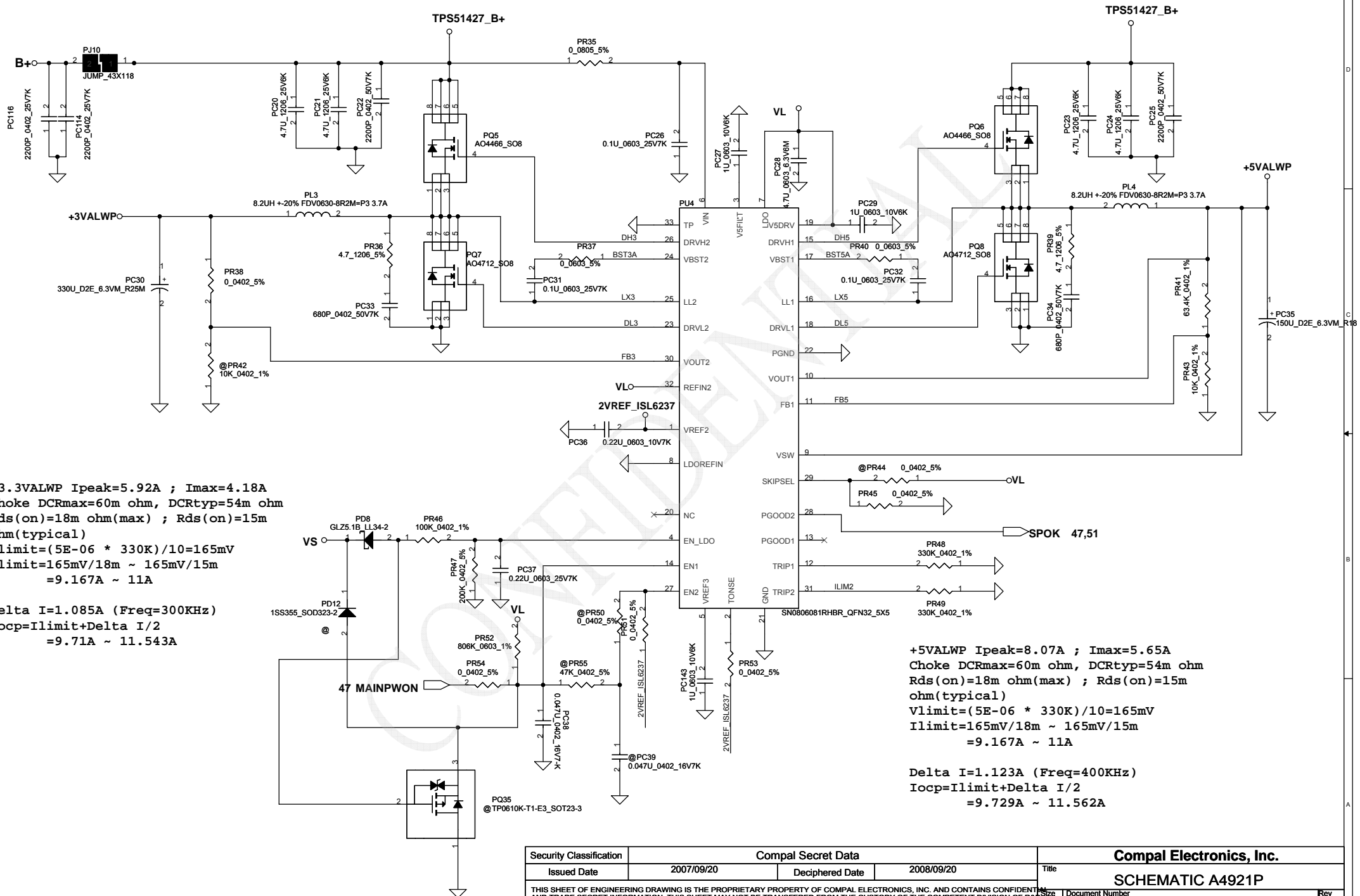
PH1 under CPU botten side :
 CPU thermal protection at 93 degree C
 Recovery at 57 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 47 degree C



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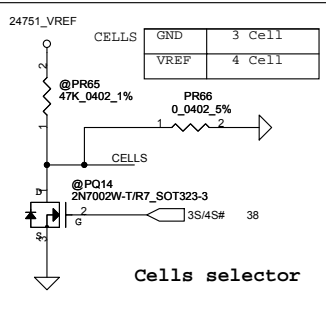
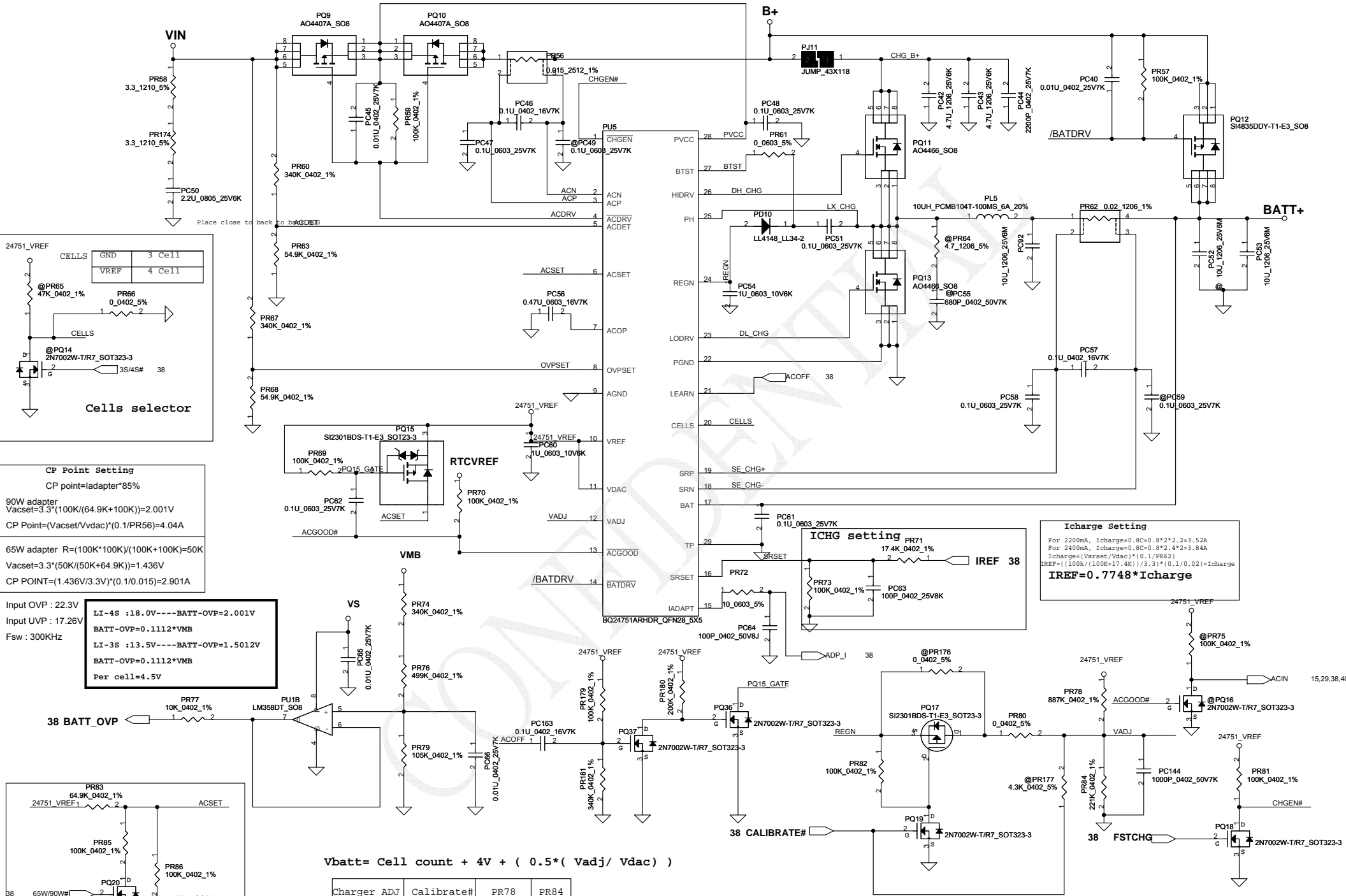
+3.3VALWP Ipeak=5.92A ; I_{max}=4.18A
 Choke DCR_{max}=60m ohm, DCR_{typ}=54m ohm
 R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
 V_{limit}=(5E-06 * 330K)/10=165mV
 I_{limit}=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A

 Delta I=1.085A (Freq=300KHz)
 I_{ocp}=I_{limit}+Delta I/2
 =9.71A ~ 11.543A

+5VALWP Ipeak=8.07A ; I_{max}=5.65A
 Choke DCR_{max}=60m ohm, DCR_{typ}=54m ohm
 R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
 V_{limit}=(5E-06 * 330K)/10=165mV
 I_{limit}=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A

 Delta I=1.123A (Freq=400KHz)
 I_{ocp}=I_{limit}+Delta I/2
 =9.729A ~ 11.562A

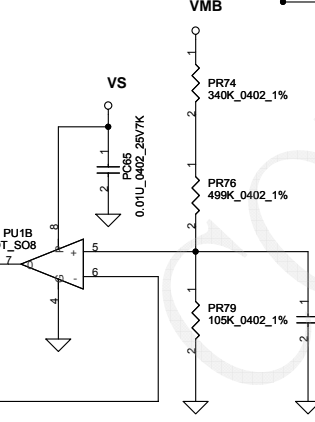
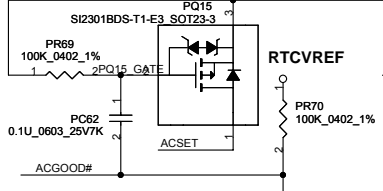
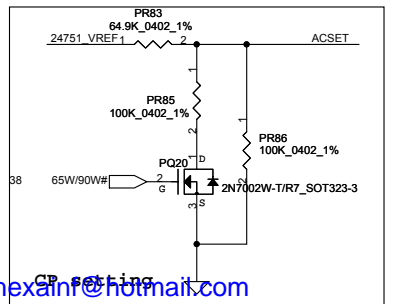
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CP Point Setting
 CP point=ladapter*85%
 90W adapter
 $V_{acset}=3.3 \cdot (100K/(64.9K+100K))=2.001V$
 $CP\ Point=(V_{acset}/V_{dca}) \cdot (0.1/PR56)=4.04A$
 65W adapter $R=(100K \cdot 100K)/(100K+100K)=50K$
 $V_{acset}=3.3 \cdot (50K/(50K+64.9K))=1.436V$
 $CP\ POINT=(1.436V/3.3V) \cdot (0.1/0.015)=2.901A$

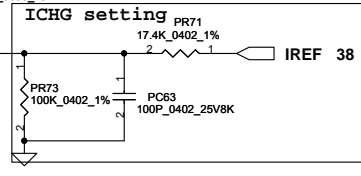
Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz

LI-4S : 18.0V----BATT-OVP=2.001V
 BATT-OVP=0.1112 * VMB
 LI-3S : 13.5V----BATT-OVP=1.5012V
 BATT-OVP=0.1112 * VMB
 Per cell=4.5V



$$V_{batt} = \text{Cell count} + 4V + (0.5 \cdot (V_{adj} / V_{dca}))$$

Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V(1.32)	H	@	@



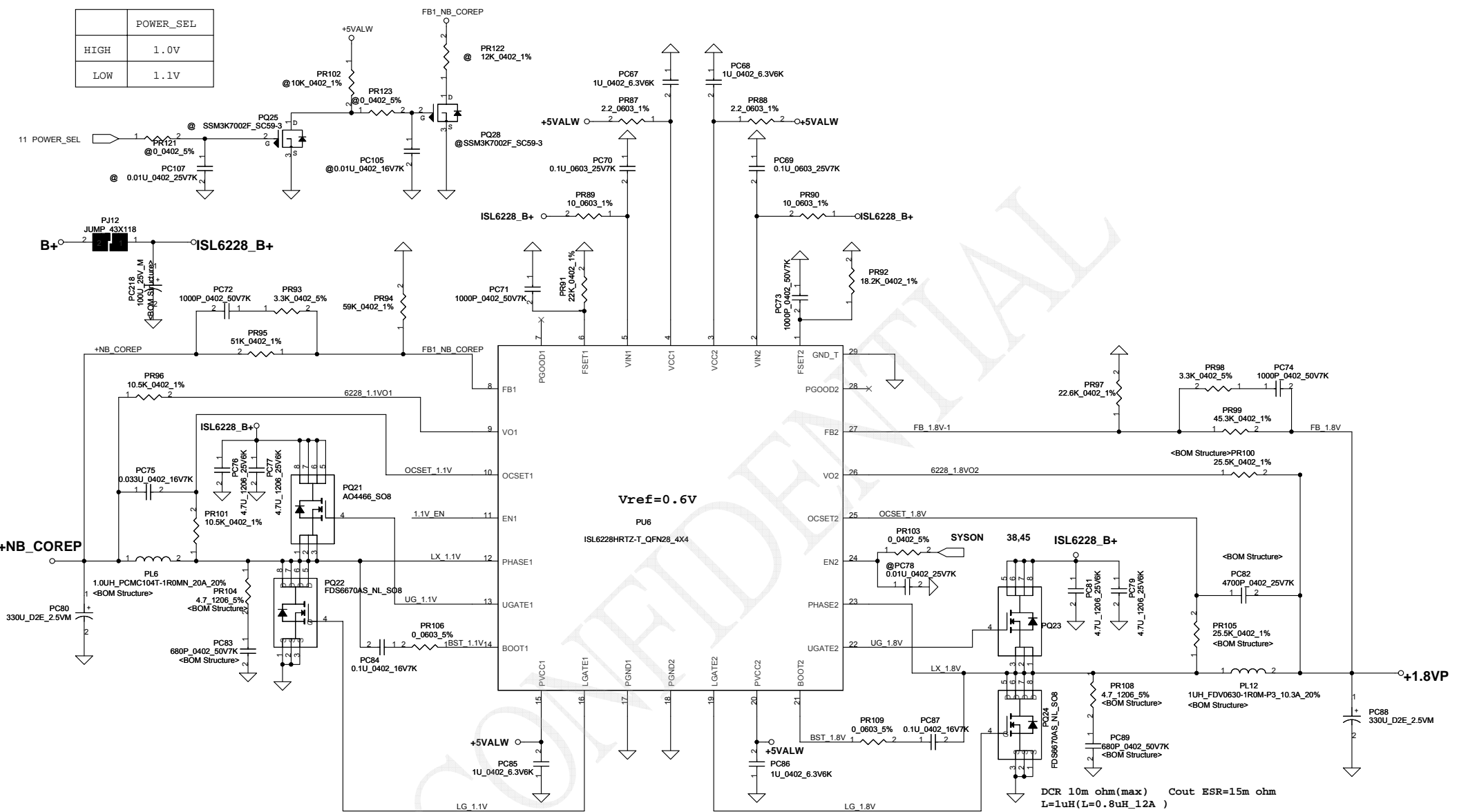
Icharge Setting
 For 2200mA, $I_{charge}=0.8C=0.8 \cdot 2.2=3.52A$
 For 2400mA, $I_{charge}=0.8C=0.8 \cdot 2.4=3.84A$
 $I_{charge}=(V_{acset}/V_{dca}) \cdot (0.1/PR62)$
 $I_{REF}=(100K/(100K+17.4K))/3.3 \cdot (0.1/0.02)=I_{charge}$
 $I_{REF}=0.7748 \cdot I_{charge}$

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	POWER_SEL
HIGH	1.0V
LOW	1.1V

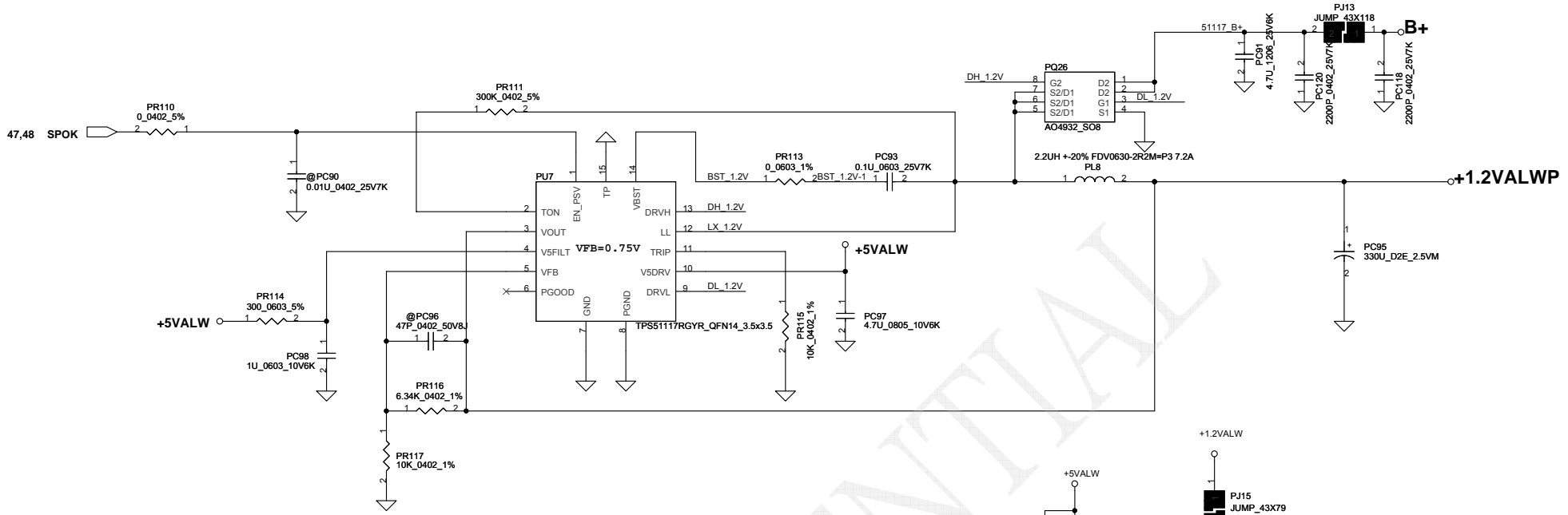


DCR=3.5m ohm(max) Cout ESR=15m ohm
 NB_CORE (1.1VSP) OCP Setting
 $Fsw=1/1.5E-10*22k = 303K$
 $Vo=Vref*((PR95+PR94)/PR94)$
 $Ipeak=17.53A, Imax=12.27A$
 $Iocp=17.53*1.2=21.04A$
 $Delta I=3.838A$
 $Iocp*DCR=(Rocset*9.5uA)=(21.04+1.92)*3.5m; Roset=8.44k$
 now chose Roset=8.66k
 $Csen=L/(DCR*Roset)=0.9uH/(3.5m*8.44k); Csen=0.031uF$
 now chose Csen=0.033uF
 $Iocp_min=(8.66K*9.5uA)/(3.5m\ ohm*1.3) = 18.08A$
 $Iocp_max=(8.66*10.5uA)/(3m\ ohm * 1.3) = 23.32A$

41,45,51 VLDT_EN

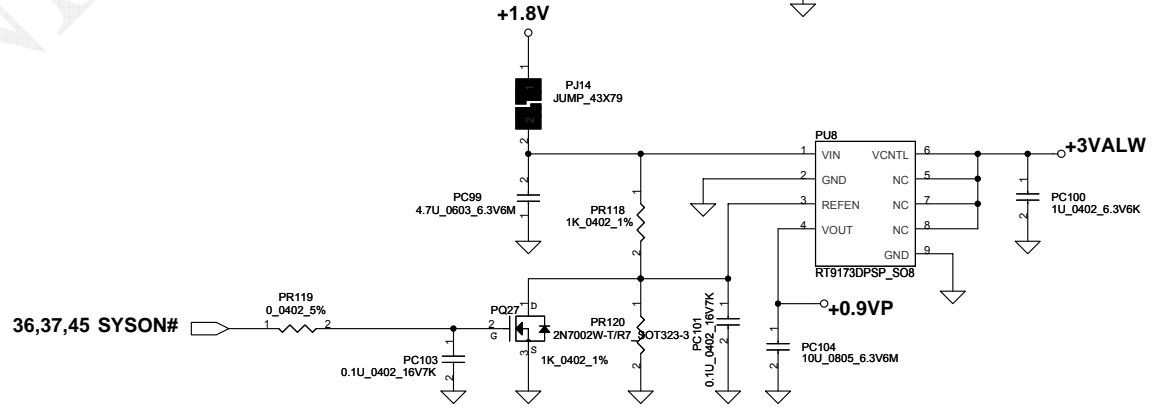
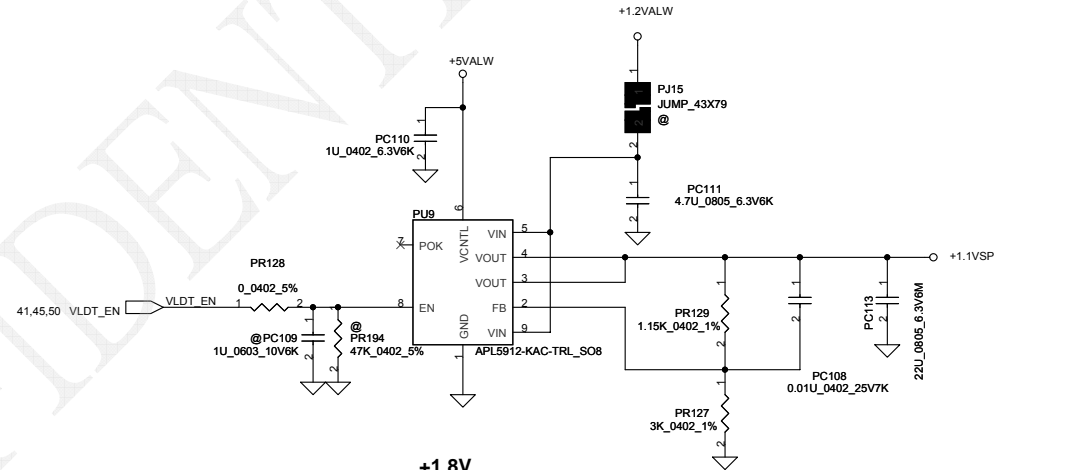
DCR 10m ohm(max) Cout ESR=15m ohm
 $L=1uH(L=0.8uH_{12A})$
 1.8VP $Ipeak=15.51A, Imax=10.86A$
 $Fsw=1/1.5E-10*18.2k = 366K$
 $Vo=Vref*((PR97+PR99)/PR97)$
 $Ipeak=15.51A, Imax=10.86A$
 $Iocp=15.51*1.2=18.61A$
 $Delta I=5.565A$
 $Iocp*DCR=(Rocset*9.5uA)=(18.61+2.7825)*10m; Roset=22.5K$
 now chose Roset=22.6K
 $Csen=L/(DCR*Roset)=0.8uH/(10m*22.5k); Csen=3.56nF$
 now chose Csen=3300pF
 $Iocp_min=(22.6K*9.5uA)/(10m\ ohm*1.3) = 16.52A$
 $Iocp_max=(22.6*10.5uA)/(10m\ ohm) = 23.73A$

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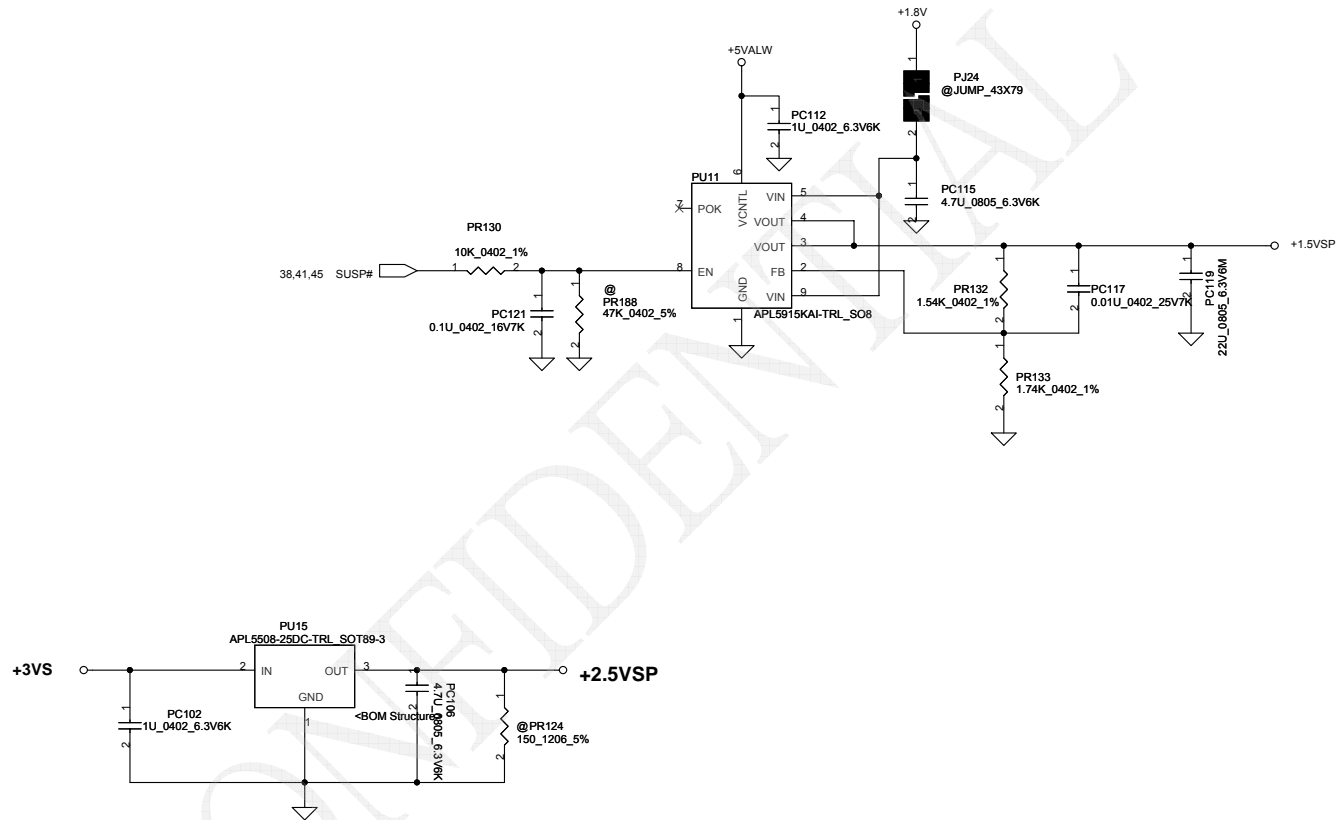
VFB=0.75V
 $V_o = VFB * (1 + PR116 / PR117) = 0.75 * (1 + 10K / 6.34K) = 1.5V$
 $Ton = 19E-12 * Ron * ((2/3) * V_o + 100mV) / v_{in} + 50ns = 3.2E-7$
 $Fsw = 200KHz$

$C_{out} ESR = 15m\ \Omega$
 $I_{peak} = 3.58A, I_{max} = 2.51A$
 $\Delta I = ((19-1.2) * (1.2/19)) / (L * Fsw) = 2.59A$
 $= > 1/2 \Delta I = 1.295A$
 $V_{trip} = R_{trip} * I_{peak} = 10K * 10uA = 0.1V$
 $I_{ocp_min} = V_{trip} / R_{dsonmax} * 1.4 + 1.295A = 0.1 / (0.0196 * 1.4) + 1.295 = 3.644A + 1.295A = 4.939A$
 $I_{ocpmax} = (0.1 / (0.016 * 1.2)) + 1.1.295A = 5.208A + 1.295A = 6.503A$
 $I_{ocp} = 6.503A - 4.939A$

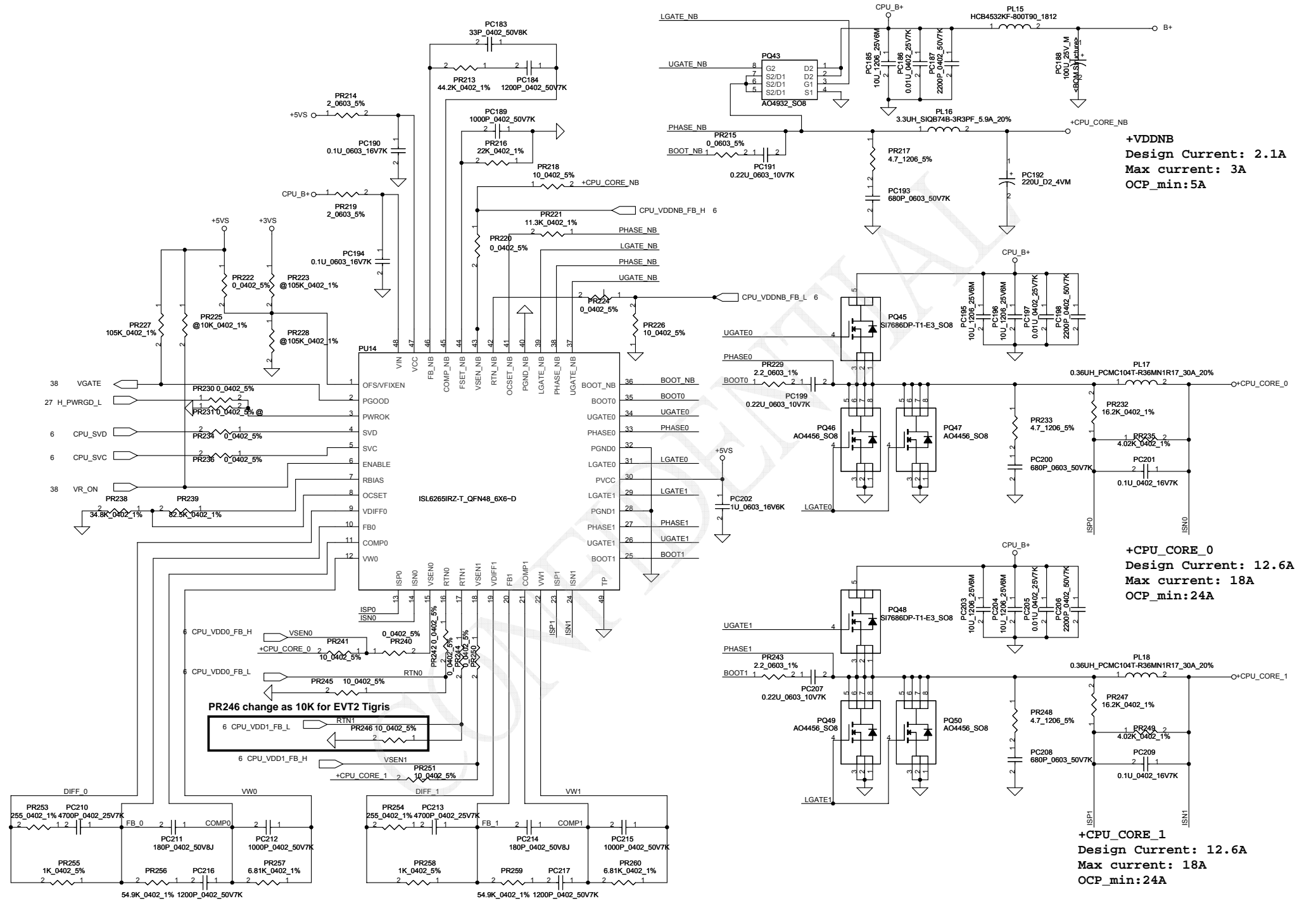


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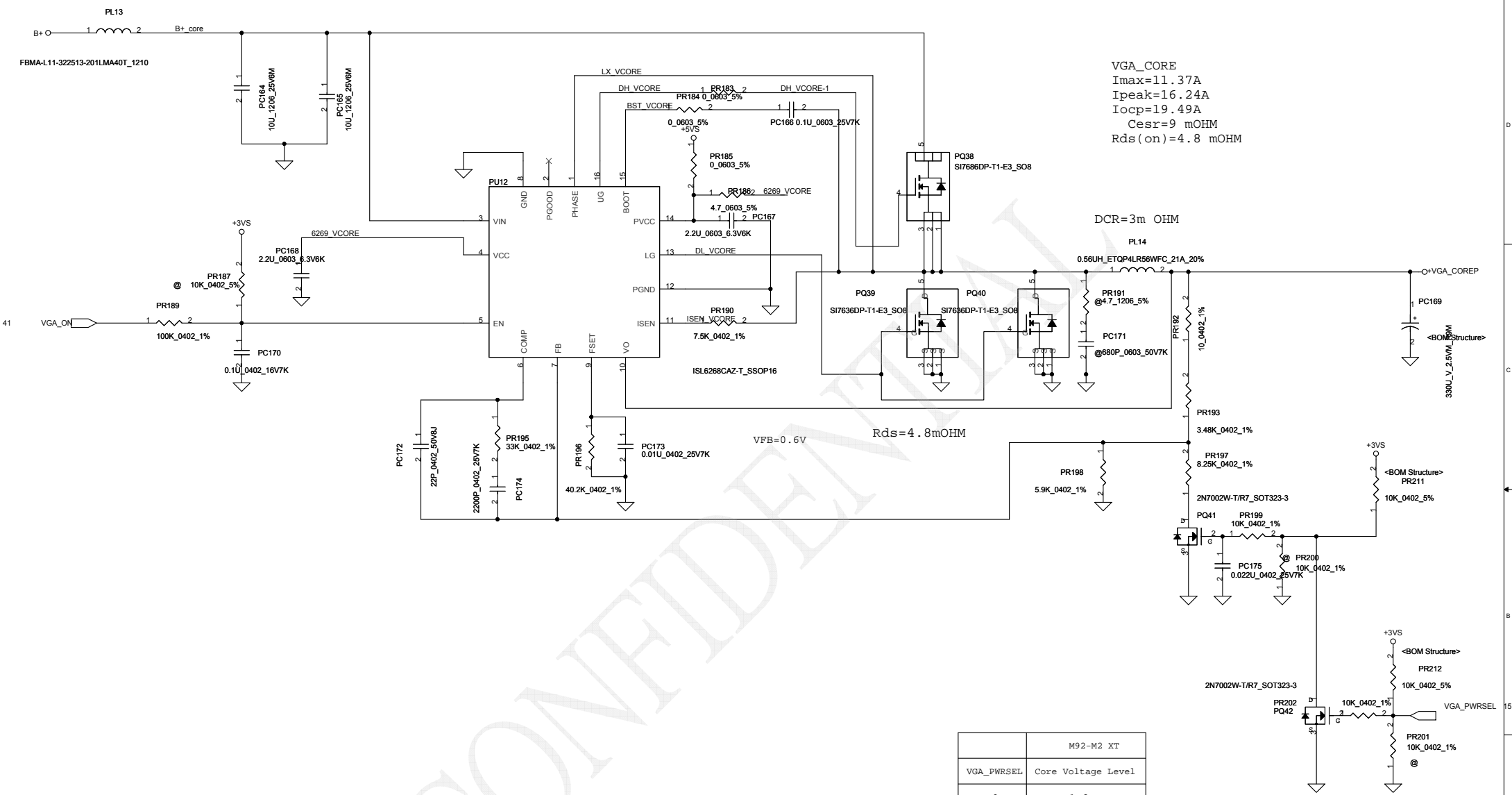


+VDDNB
 Design Current: 2.1A
 Max current: 3A
 OCP_min: 5A

+CPU_CORE_0
 Design Current: 12.6A
 Max current: 18A
 OCP_min: 24A

+CPU_CORE_1
 Design Current: 12.6A
 Max current: 18A
 OCP_min: 24A

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ADD circuit	Switch NB_core voltage	0.1	50	ADD PC107, PC105, PR121, PR123, PR122, PR102, PQ25, PQ28 at UMA Sku	2009/01/04	DVT
2	ADD circuit	Switch NB_core voltage	0.1	51	ADD PC110, PC111, PC108, PC109, PC1113, PR1128, PR194, PR129, PR127 at UMA Sku	2009/01/04	DVT
3	ADD snubber	EMI requestmnt	0.1	50	Add PR104 4.7 ohm and PC83 680p	2009/01/04	DVT
4	ADD snubber	EMI requestmnt	0.1	50	Add PR108 4.7 ohm and PC89 680p	2009/01/04	DVT
5	ADD CPU boot	EMI requestmnt	0.1	53	Add PR229 2.2 ohm	2009/01/04	DVT
6	ADD CPU boot	EMI requestmnt	0.1	53	Add PR243 2.2 ohm	2009/01/04	DVT
7	Change resistance value	Switch NB_core voltage	0.1	50	Change PR95 from 51 Kohm to 39.2 Kohm	2009/01/04	DVT
8	Change resistance value	Switch NB_core voltage	0.1	50	Change PR122 from 12 Kohm to 226 Kohm	2009/01/04	DVT
9	Change resistance value	soft start of Switch NB_core voltage	0.1	50	Change PR123 from 0 ohm to 10 Kohm	2009/01/04	DVT
10	Change capacitor value	soft start of Switch NB_core voltage	0.1	50	Change PC105 from 0.01 uF to 0.1 uF	2009/01/04	DVT
11	Change IC part number	Change IC part number	0.1	48	Change PU4 part number to SA00002V400	2009/01/04	DVT

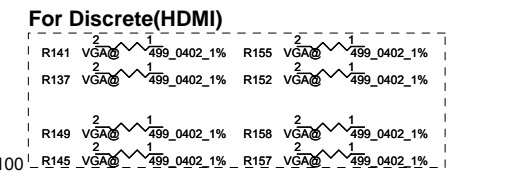
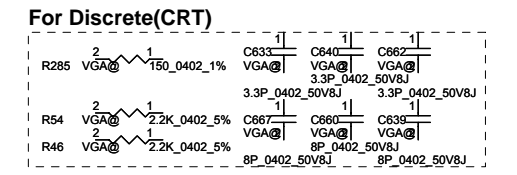
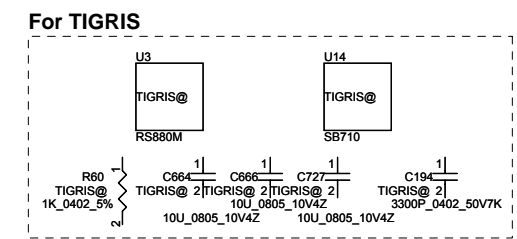
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PHASE	PAGE	MODIFICATION LIST	PURPOSE
DVT	P.6	Reserve R484/R485(0ohm_0402) for CPU SB temp sensor	Reserved EC SMBUS1 due to +3VS leakage when S3 entry with SMBUS2
	P.8	Add C174/C175/C176 (0.lu_0402)	EMI request
	P.10	C646/C647/C648/C649/C650/C651/C652/C653 with VGA@	BOM error
	P.11	Add R488/R489 (0ohm_0402) & reserve R491/R492 (0ohm_0402)	UMA HDMI I2C bus mainly to RS780MN DDC port1 & reserve to port0
	P.11	Reserve R490(0ohm_0402)	NA
	P.12	Change L6/L7 from 0ohm_0805 as 0ohm_1206 & with VGA@	For DIS +1.1VS power source from fixed +NB_CORE
	P.22	Remove VRAM Samsung(Q-die) & Qimonda type	Customer request
	P.24	U35/R464/R465/C845/C846/C847/C848/C849 with @ & RP15 with UMA@	Separately as DIS sku only & UMA sku only
	P.24	Add RP20/RP21/RP22/RP23(0ohm_0404_4P2R) with VGA@	For DIS sku only
	P.24	Reserve Q52/R501/R502/R503	Reserve for UMA sku white screen flash when boot issue check
	P.25	Change JHDMI1 from SMD type as DIP type(DC232000800)	DFX request
	P.25	Change single MOS as 2 dual N-ch MOS(Q53/Q54) & reserve R506	NA (Just no need to modify)
	P.26	R47/R58/U25/U26/C626/C628/R475 with UMA@ & R507 with VGA@ , U36/C850 with @ & delete R466 , add R493/R494/R495 with VGA@	Separately as DIS sku only & UMA sku only
	P.27	Add R496 with @ & R476/R482 with @	NA
	P.28	Add R509 with VGA@ & R510 with UMA@	Reserve SKU ID for SW even SW check device ID instead currently
	P.29	Reserve C862/C863/C855/C856	Reserve eSATA function for future request
	P.37	Change JUSB1 as SB700 USB port6	Dedicated HS port on lower-left position
	P.38	Change U20 as KB926 D3 version (SA00001J580)	NA
	P.38	D41 with VGA@ & D42 with UMA@	Separately as DIS sku only & UMA sku only
	P.38	U20.85 defined as TP_LOCK_LED# feature	LED control simultaneously with Tutch-Pad locked function
	P.38	Change R194 as 8.2kohm_0402	Change board ID as 1 (PCB revision : 0.2)

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PHASE	PAGE	MODIFICATION LIST	PURPOSE
	P.39	Add R250/LED11/SW4	Add T/P lock button & T/P lock button LED
	P.45	Reserve R499 , R497/R498/Q51	NA
	P.45	Stuff R202	+1.2VALW leakage 640mv pulse when AC insertion & then might cause OVP
	P.34	C26 with @ & C11 as SE070104Z80	NA
	P.42	Stuff R446(0ohm_0805) & un-stuff U32(Audio LDO)	NA
DVT2	P.6	Remove CPU side-band(internal) temp sensor function	NA
	P.11/38	Add U49/C857/R744 (Reserve U48) & D42 with @, remove D42	NA
	P.23/34	Add R676 for CLK_48M_SD , reserve R715 / R716 for CLK_48M_LAN	NA
	P.24	Add R508(2.7K_0402) for ENVDD of UMA sku	NA
	P.28	SB700 USB port 4 for Realtek RTS5159 card reader	NA
	P.33	Add(co-layout) Realtek RTS5159 card reader	NA
	P.37	Change JSAT1 PCB footprint as TYCO_1909574-1_11P-T	NA
	P.38	R194 change as 18K_0402	Change board ID as 2 (PCB revision : 0.3)
	P.40	LED1 / 5 / 8 / 9 /10 PCB footprint change as LED_HT-297DQ-GQ_4P	For DFX
	P.44	Add H28 & H29	For thermal
PVT	P.11	Add R511 with @ & U50	For LCD white screen flash when coldboot issue
	P.11	Add C874 / C875 (1u_0402)	For CRT(acer lab) flicker
	P.11/38	C857 / U49 with @ , R744 / D42 with UMA@	NA
	P.42	Add L94(SM010027780) close to audio codec	For EMI
	P.40	Modify LED 1 / 5 / 8 from dual Blue/Amber LED as single Blue LED	Follow acer spec
	P.39/40	Modify R12/R13/R17/R16 (300->220ohm) , modify R1/R2/R3 (1.2K->866ohm) , modify R10 (300->715ohm) , modify R245/R247 (4.99K->750ohm) , modify R244/R246 (4.99K->866ohm) , modify R250 (1.2K->5.1K)	For LED brightness test
	P.23	Change LAN_CLKREQ# from U18.51 to U18.24 output	NA
	NA	Change test pad (except T8/T13/T15/T17/T18/T24/T28 /T29/T33/T45/T46/T48/T50/T56/T57/T12) from TPC12 to TPC24	NA
	P.36	Reserve Q55 / Q56 / R745 / R746 / R747 / C876 to turn off power of finger printer	NA
	P.38	R194 change as 18K_0402 for change board ID as 3 (PCB revision : 0.4)	NA
MP		Search for MP font	NA



PCB

PCB 047 LA-4921P REV1 MIB

LA4921MB Rev0: DA80000DP00
 LA4921MB Rev1: DA80000DP10
 LA4921MB with Sub/B Rev1: DAZ07R00100

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