

Compal Confidential

PEW76/86/96 M/B Schematics Document

AMD Danube Only UMA

AMD Champlain Processor with RS880M/SB820M

2010-07-20

LA6552P REV: 1.0

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				Document Number	PEW76/86/96 LA-6552P
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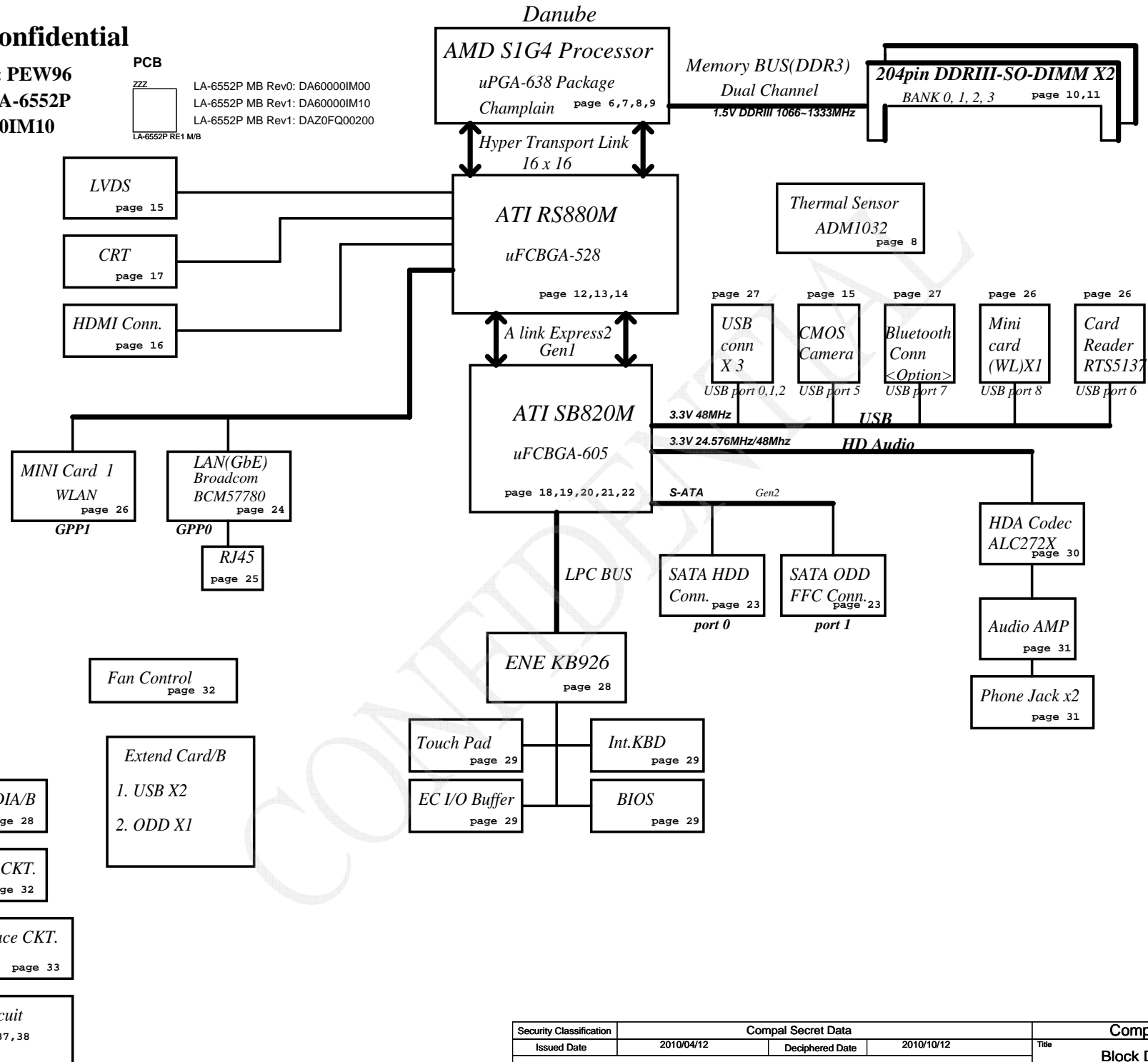
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Model Name : PEW96
 File Name : LA-6552P
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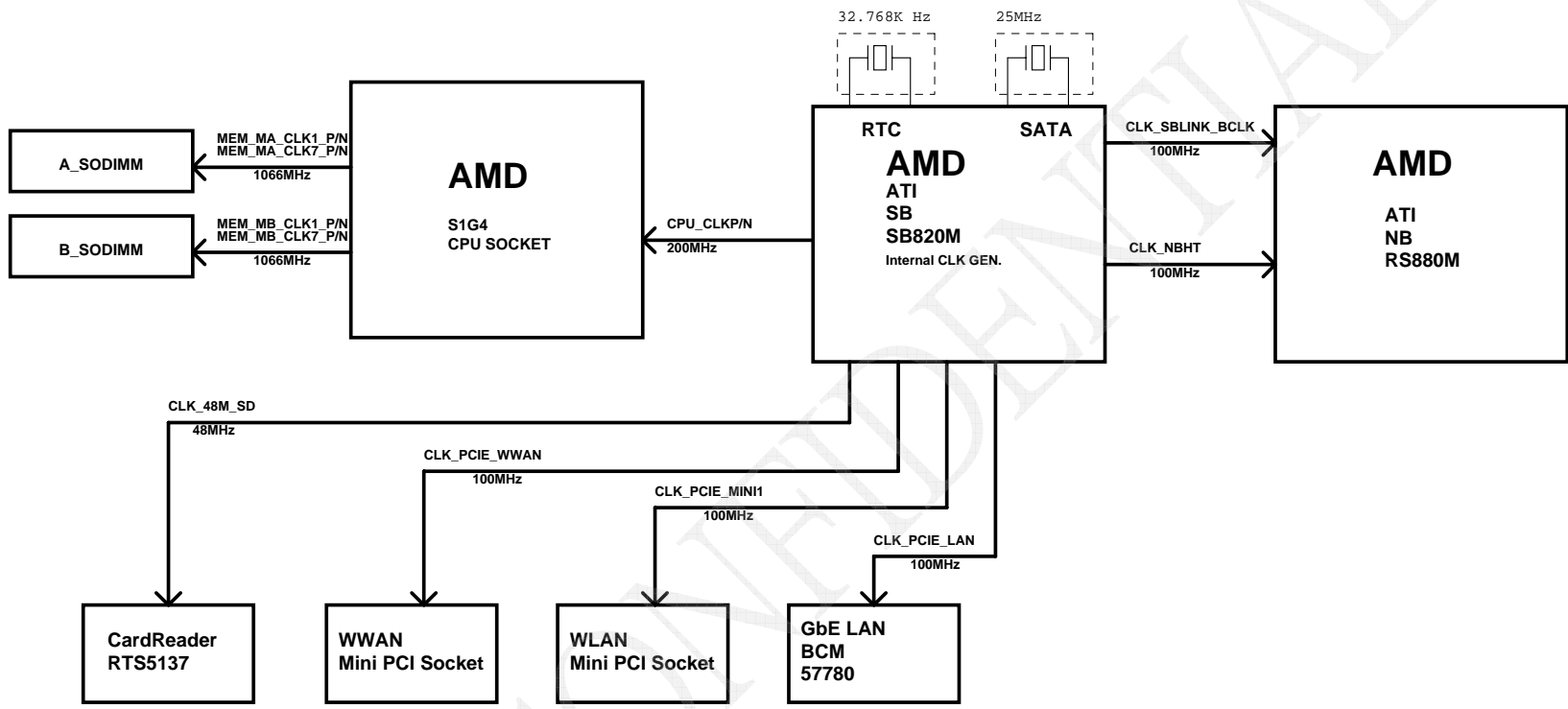
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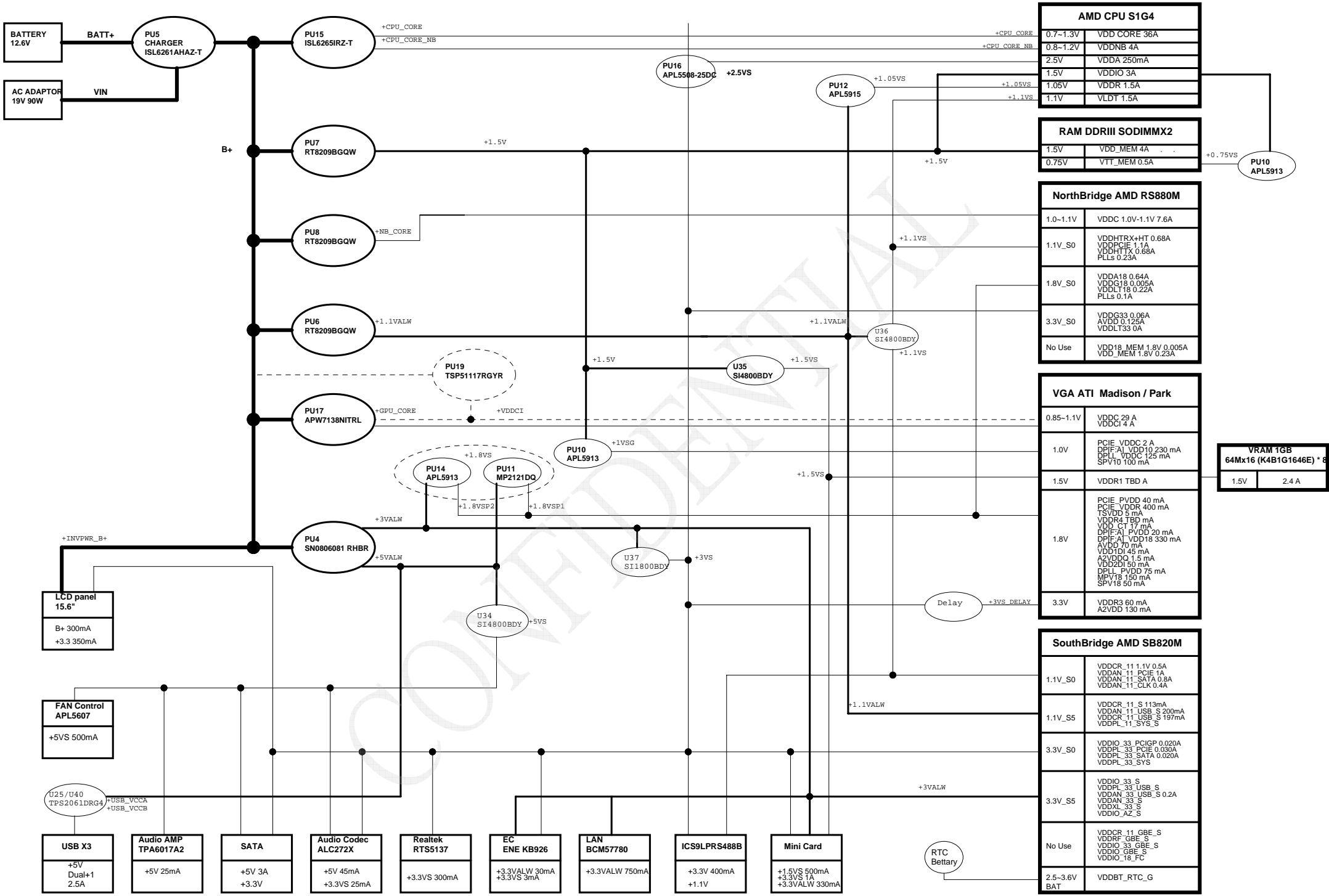
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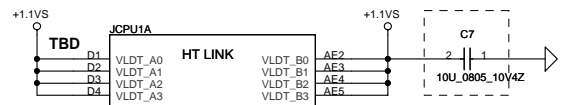
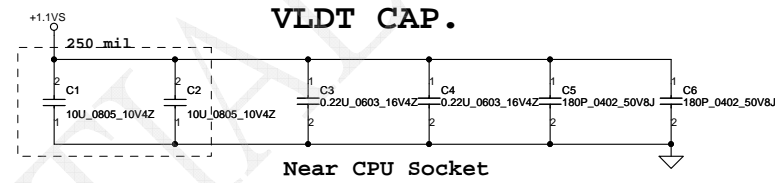


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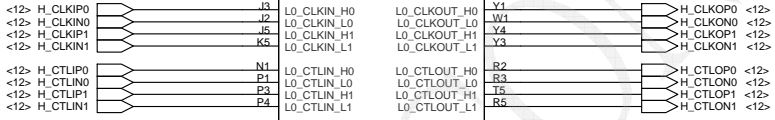


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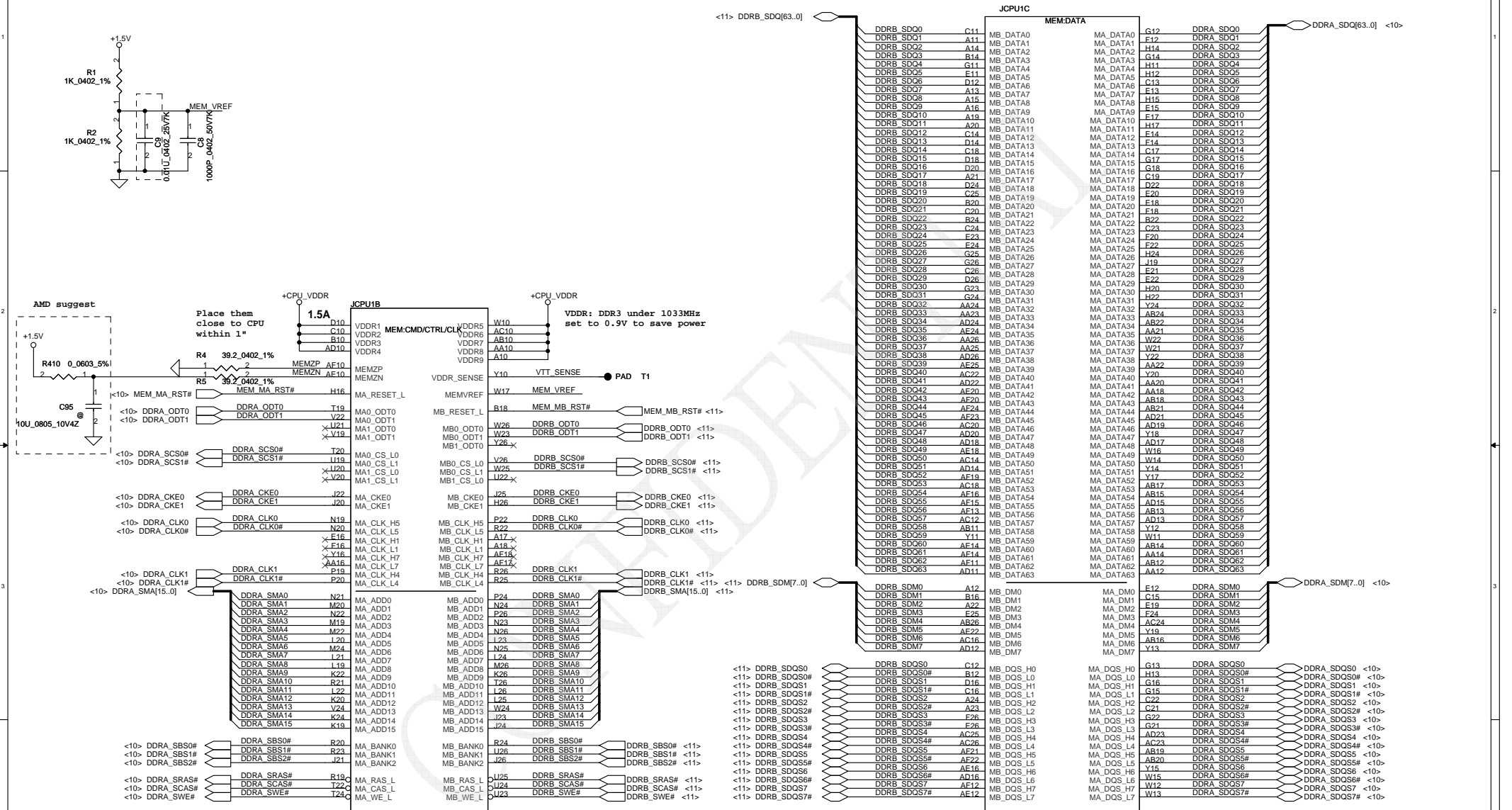
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H_CADIP1	F1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AA1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA2	H_CADON2
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H_CADIN3	H1	L0_CADIN_L3	L0_CADOUT_L3	W2	H_CADON3
H_CADIP4	J1	L0_CADIN_H4	L0_CADOUT_H4	W3	H_CADOP4
H_CADIN4	K1	L0_CADIN_L4	L0_CADOUT_L4	V1	H_CADON4
H_CADIP5	L3	L0_CADIN_H5	L0_CADOUT_H5	U1	H_CADOP5
H_CADIN5	L2	L0_CADIN_L5	L0_CADOUT_L5	U2	H_CADON5
H_CADIP6	L1	L0_CADIN_H6	L0_CADOUT_H6	U3	H_CADOP6
H_CADIN6	M1	L0_CADIN_L6	L0_CADOUT_L6	T1	H_CADON6
H_CADIP7	N3	L0_CADIN_H7	L0_CADOUT_H7	R1	H_CADOP7
H_CADIN7	N2	L0_CADIN_L7	L0_CADOUT_L7	AD4	H_CADON7
H_CADIP8	E5	L0_CADIN_H8	L0_CADOUT_H8	AD3	H_CADOP8
H_CADIN8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD5	H_CADON8
H_CADIP9	F3	L0_CADIN_H9	L0_CADOUT_H9	AC5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC6	H_CADON9
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H_CADIP14	J3	L0_CADIN_H14	L0_CADOUT_H14	V5	H_CADOP14
H_CADIN14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	H_CADON14
H_CADIP15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	H_CADOP15
H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	H_CADON15



FOX_P263823-284S-41F_Champlan

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Processor DDR3 Memory Interface



FOX_P263823-284S-41F_Champlian

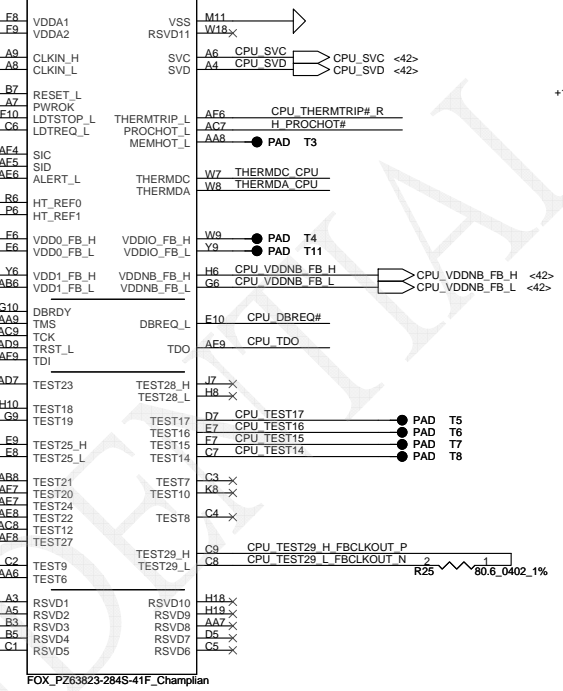
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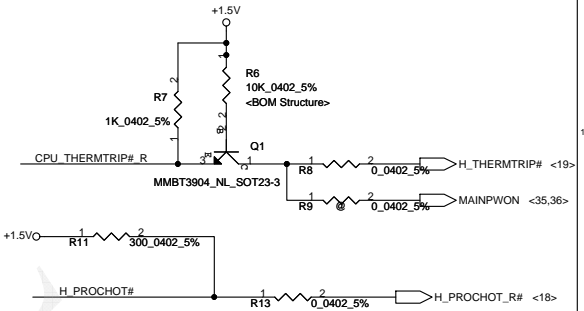
Champlain: C1E
 C1E: LDT_REQ# no connect
 CLMC: LDT_REQ# connect to NB

LDT_RES# / MEMHOT#
 no support in S1g4

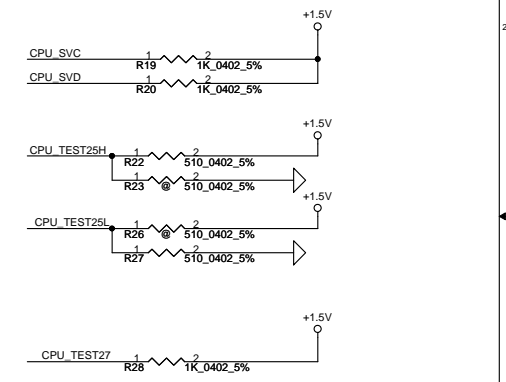
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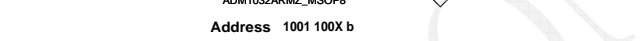
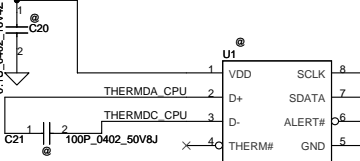
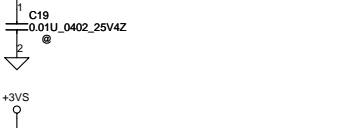
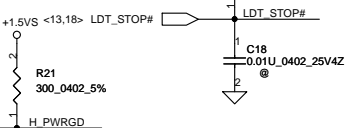
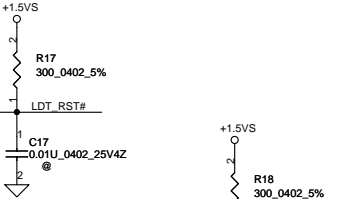
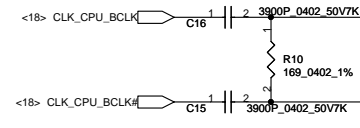
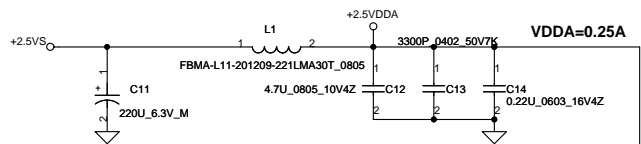
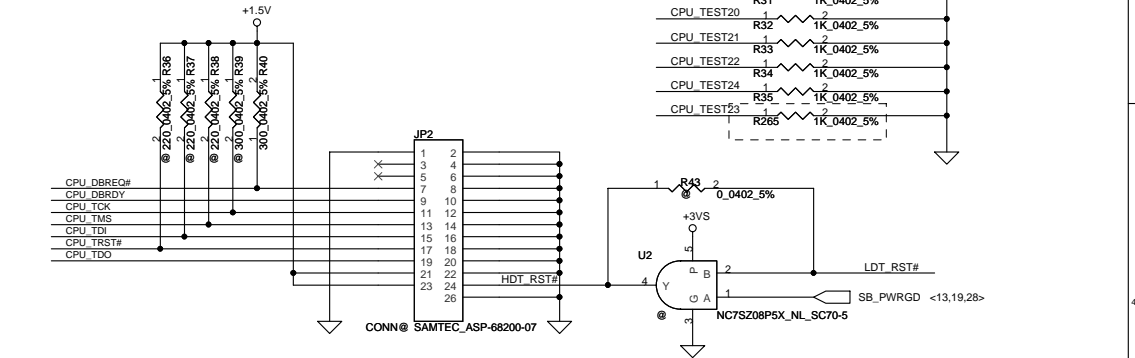
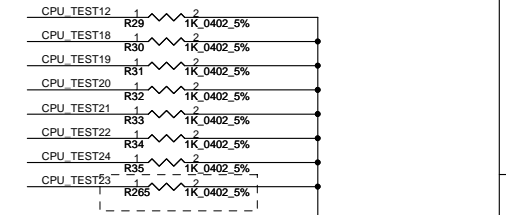
FOX_P263823-284S-41F Champlain



PROCHOT:
 Input: For HTC Function
 Output: Over Temperature Condition

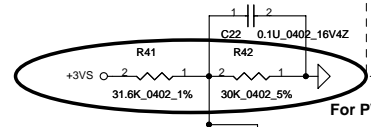


For SCAN connect use



Address 1001 100X b

CPU internal thermal sensor

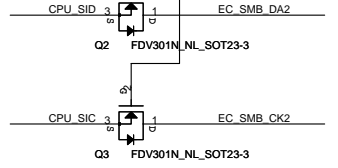


FDV301N, the Vgs is:
 min = 0.65V
 Typ = 0.85V
 Max = 1.5V

B5H111, the Vgs is:
 min = 0.4V
 Typ = 1.0V
 Max = 1.3V

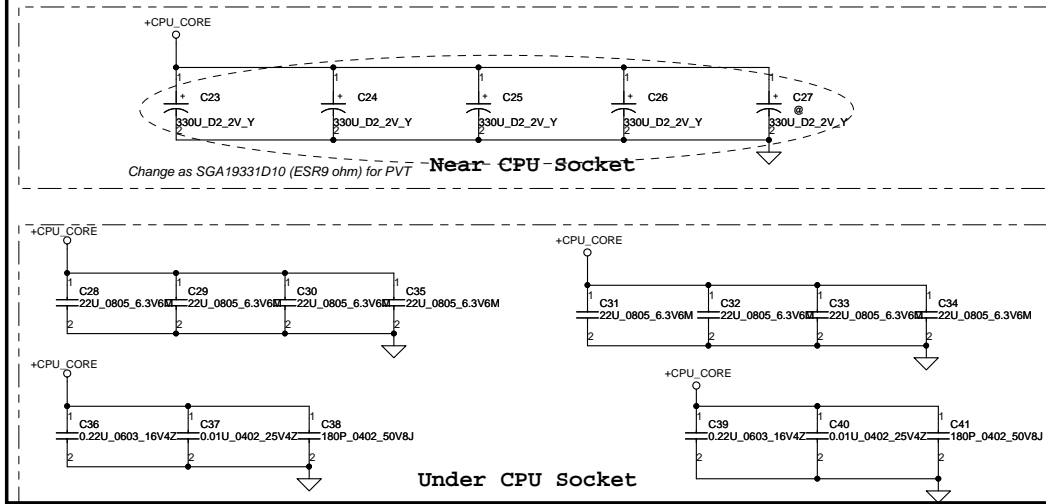
For PVT

1.607V for Gate

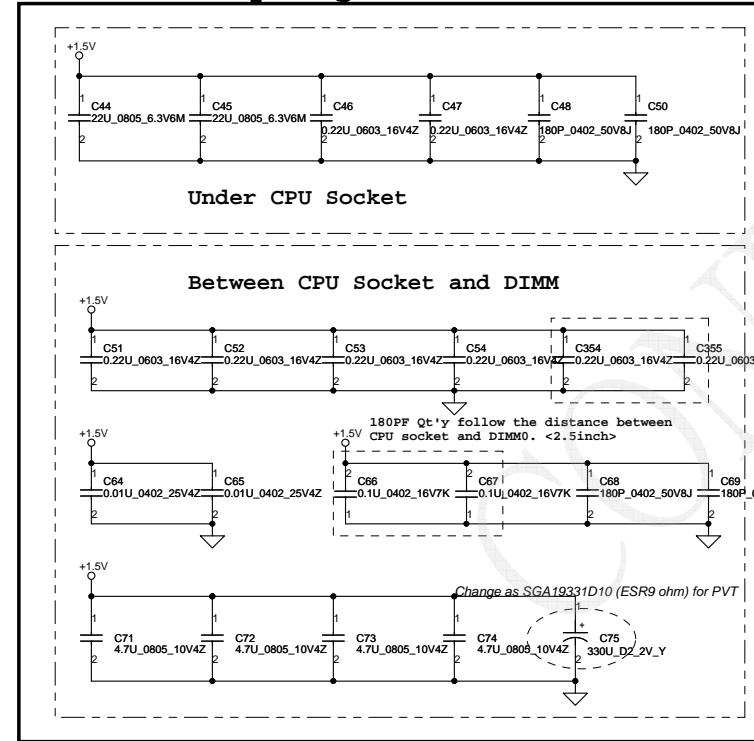


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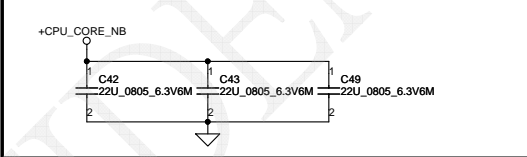
VDD(+CPU_CORE) decoupling.



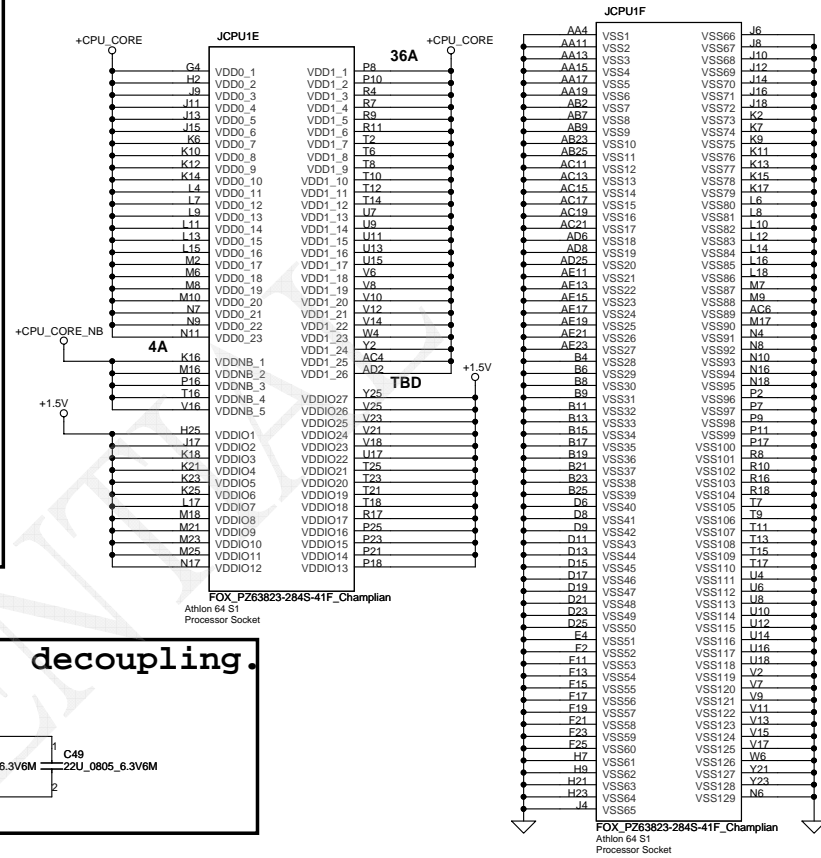
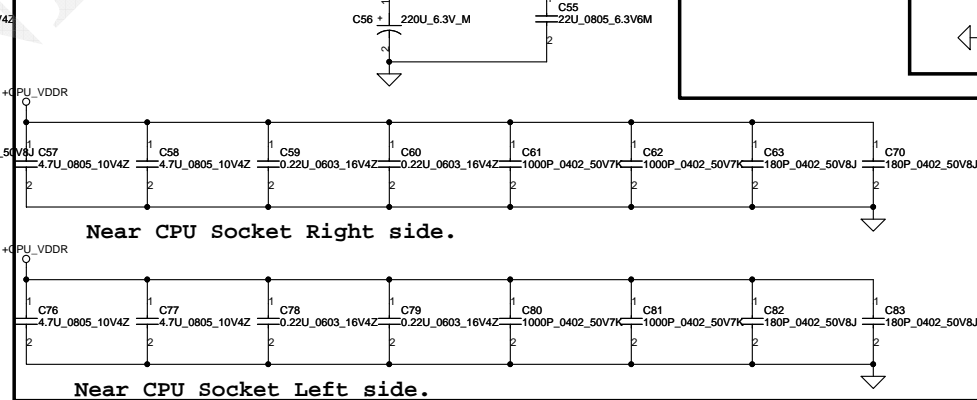
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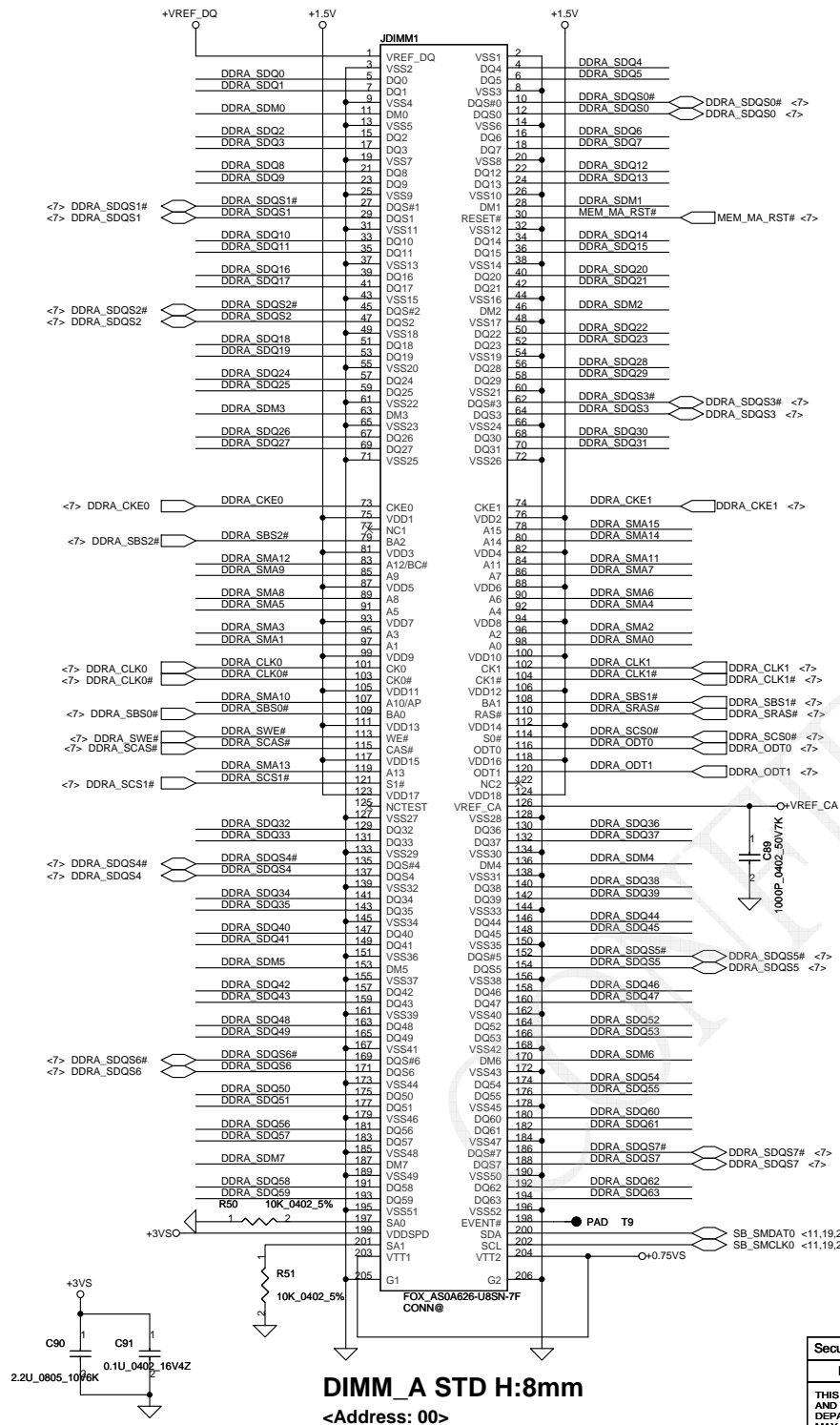


+CPU_CORE_NB decoupling.

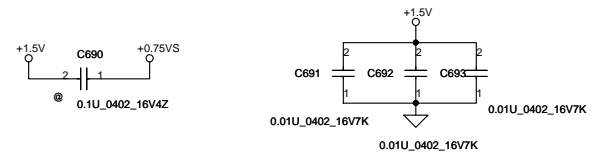
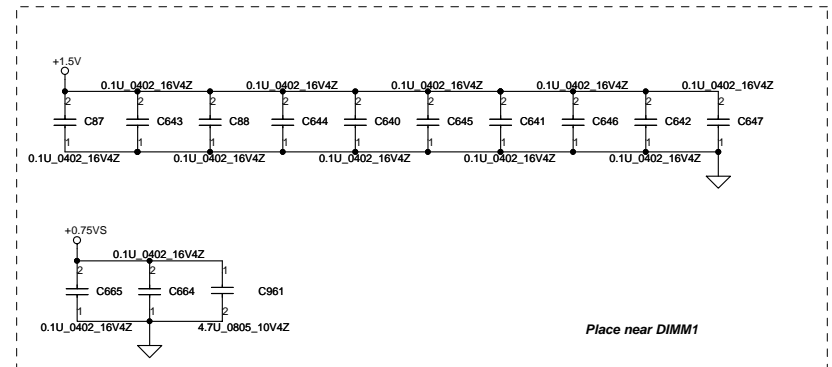
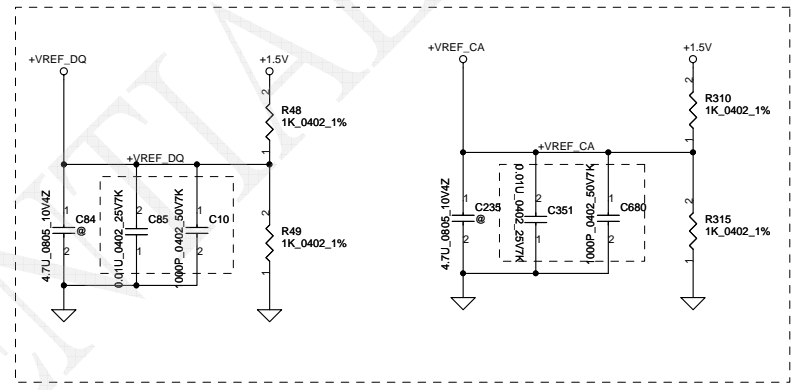


VDDR decoupling.

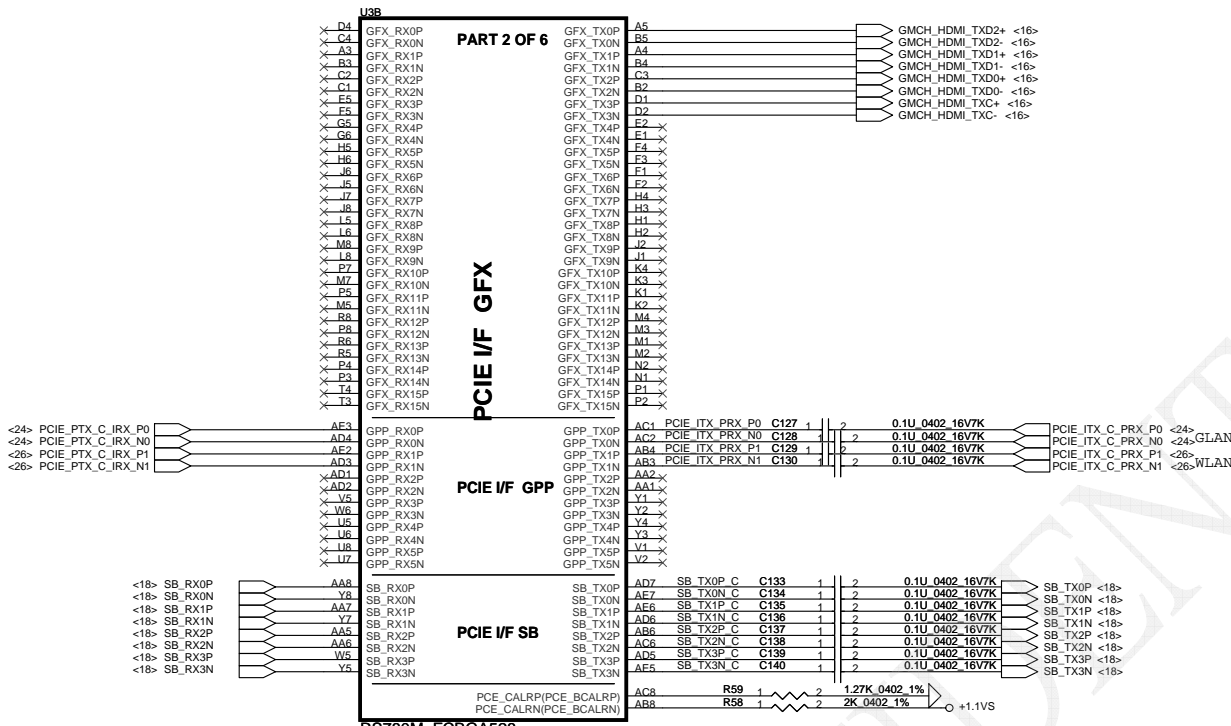




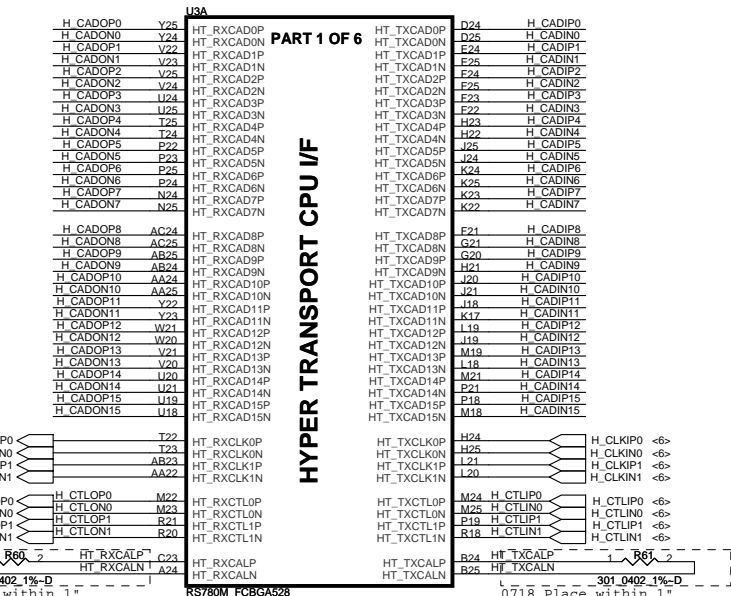
DIMM_A STD H:8mm
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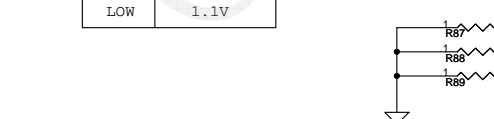
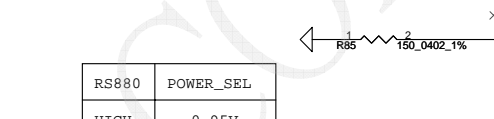
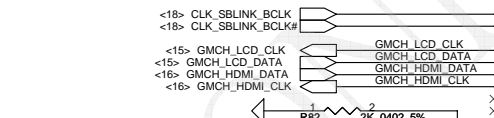
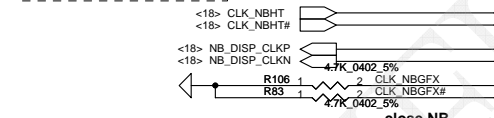
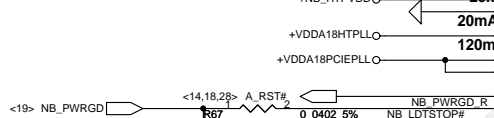
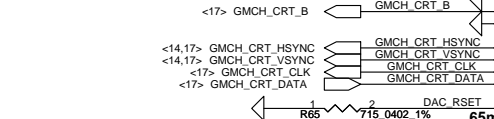
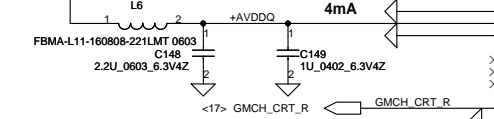
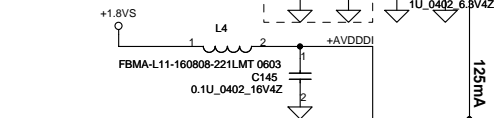
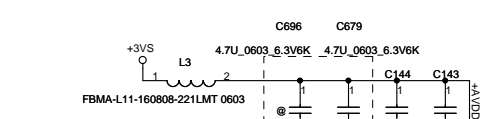
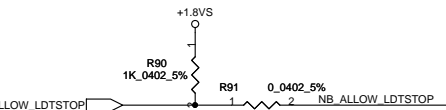
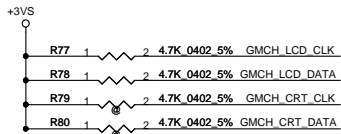
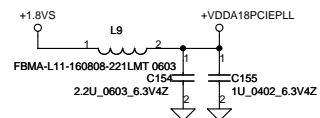
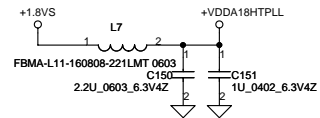
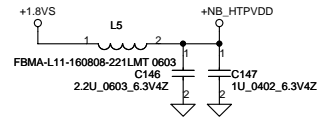
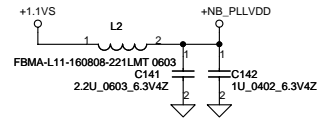


RS780M_FCBGA528
RS880 A11(SA000032710)

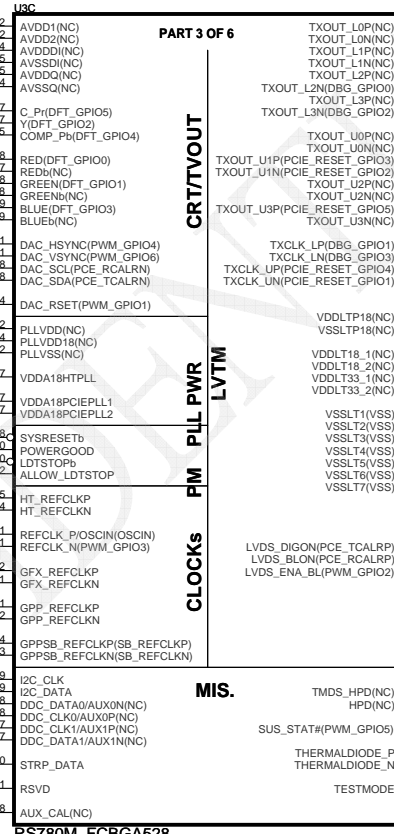


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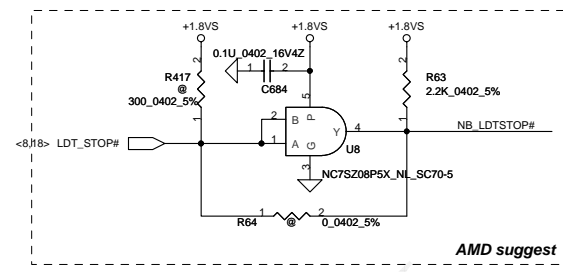
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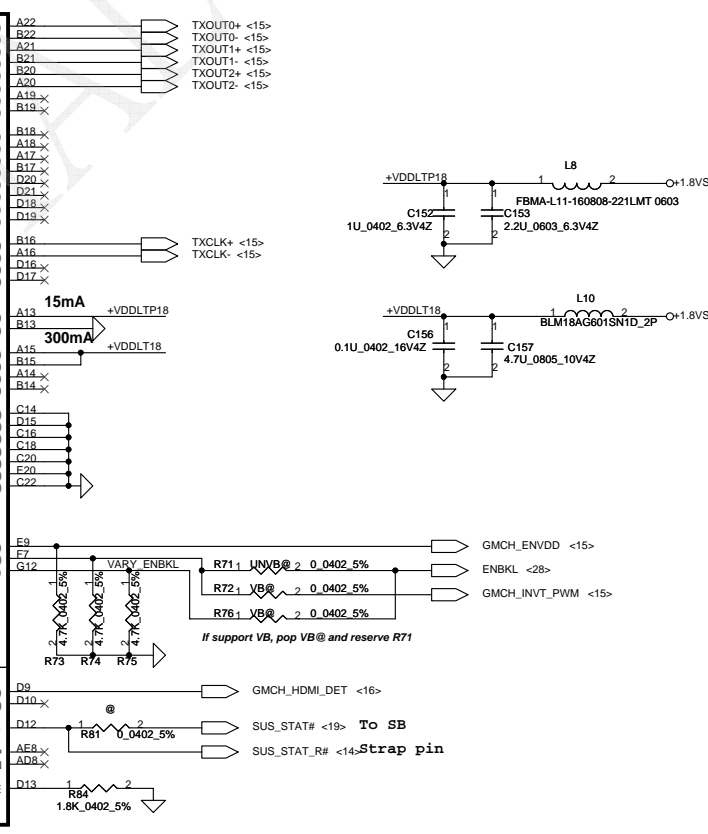
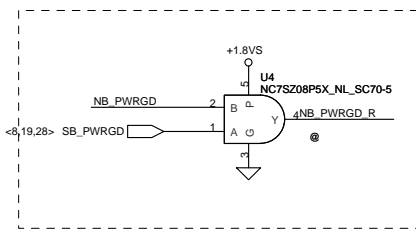
RS880	POWER_SEL
HIGH	0.95V
LOW	1.1V



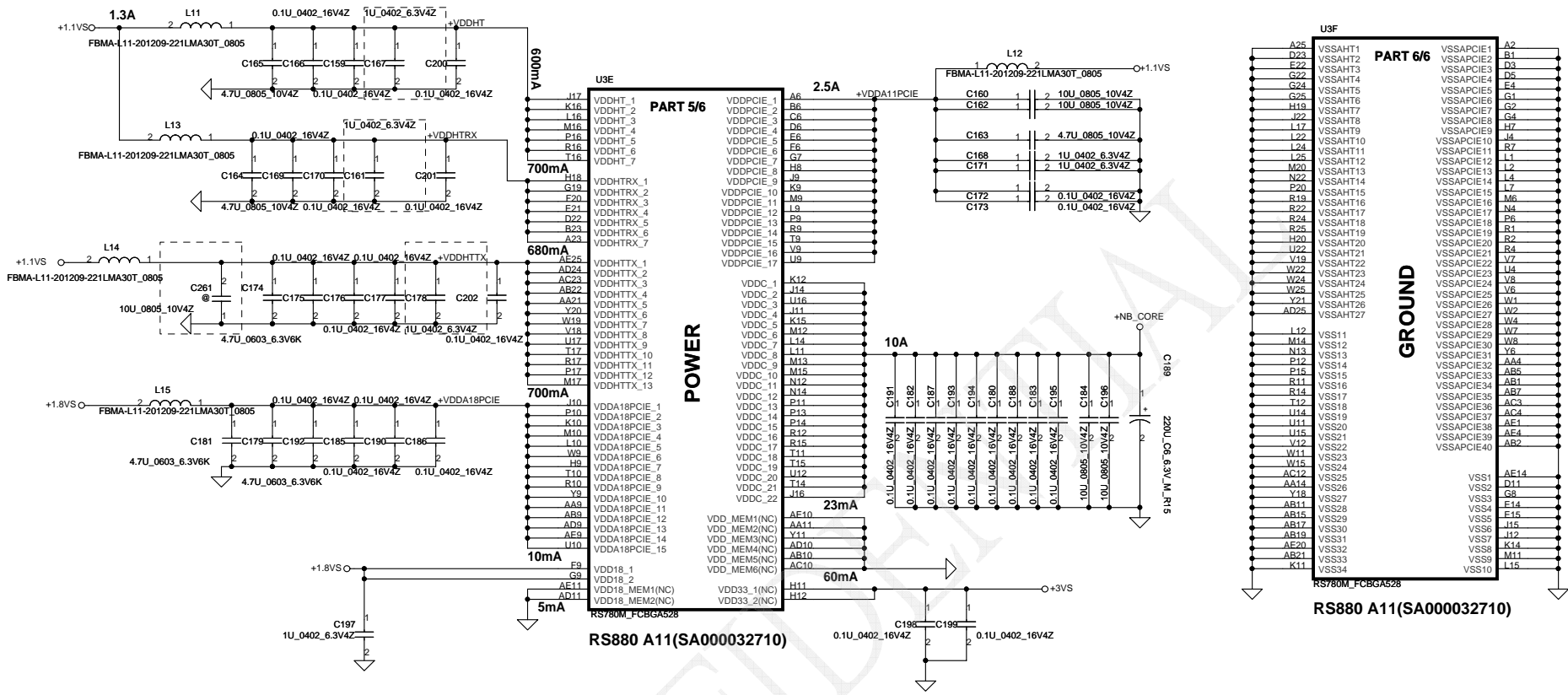
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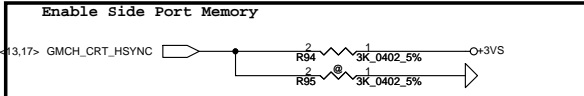
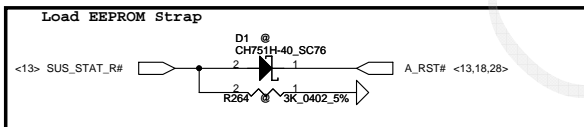
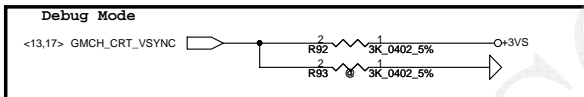
AMD suggest



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Side port and Strap setting



DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO. (VSYNC)

1 : Disable
0 : Enable

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

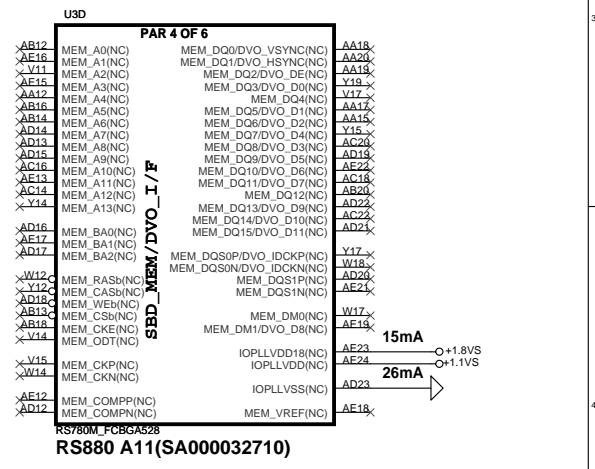
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

Enable Side Port Memory

RS880: HSYNC#

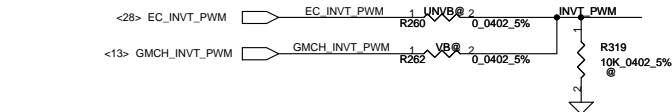
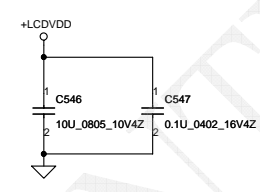
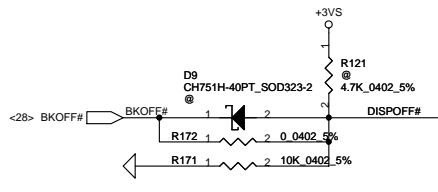
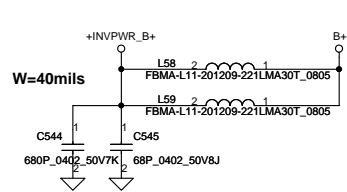
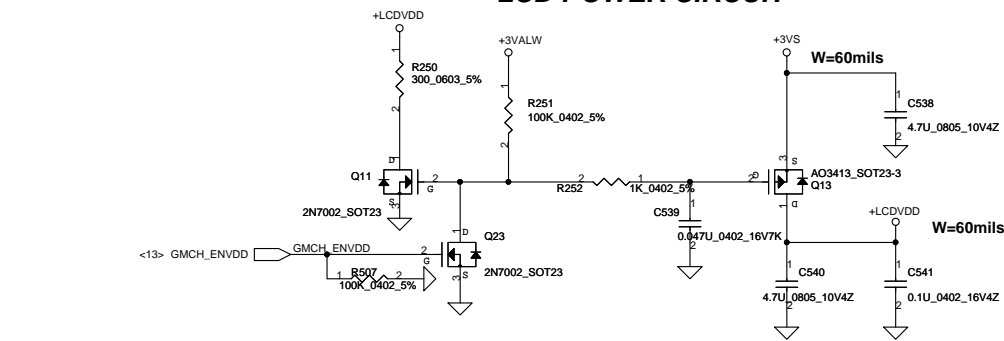
0 : Enable
1 : Disable

Register Readback of strap:
NB_CLKCFG:CLK_TOP_SPARE_D[1]



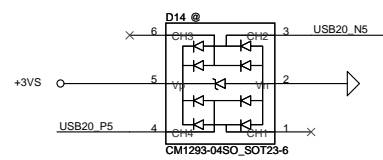
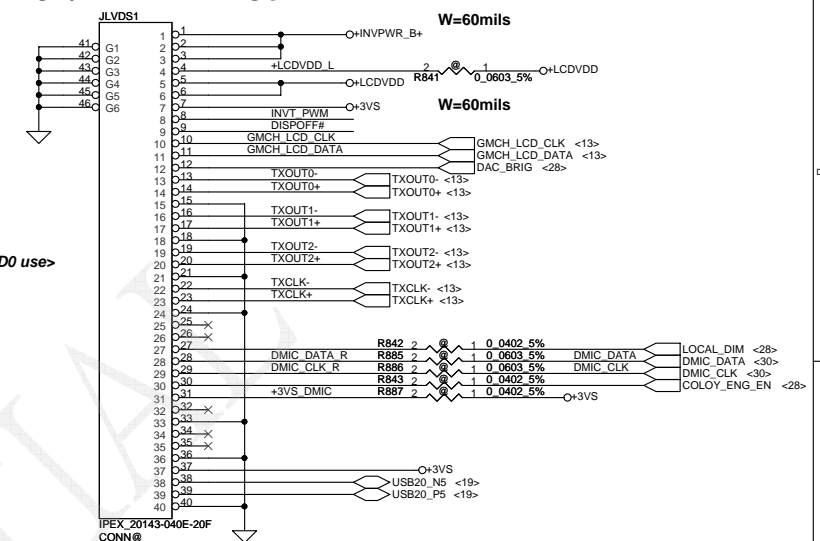
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Issued Date	2010/04/12	Deciphered Date	2010/10/12	Title
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Date:	Thursday, July 22, 2010	Sheet	14	of 45

LCD POWER CIRCUIT

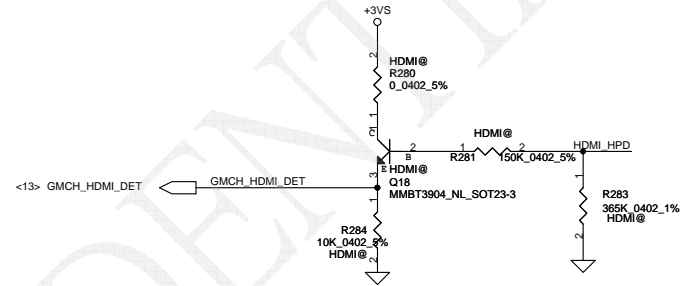
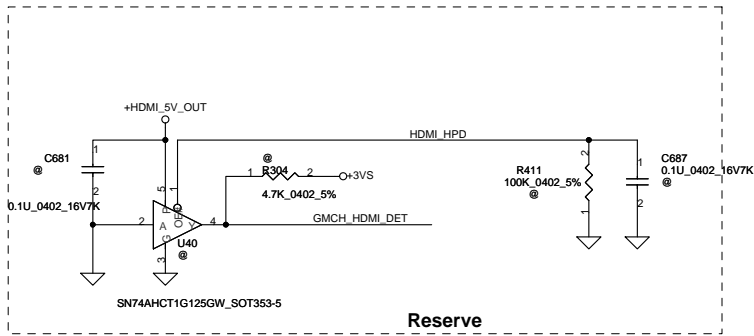
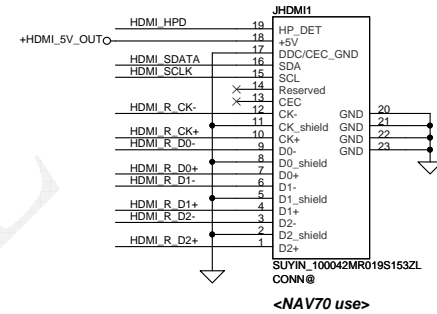
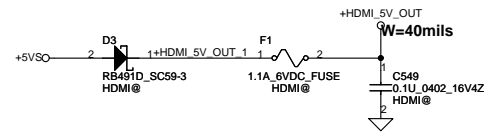
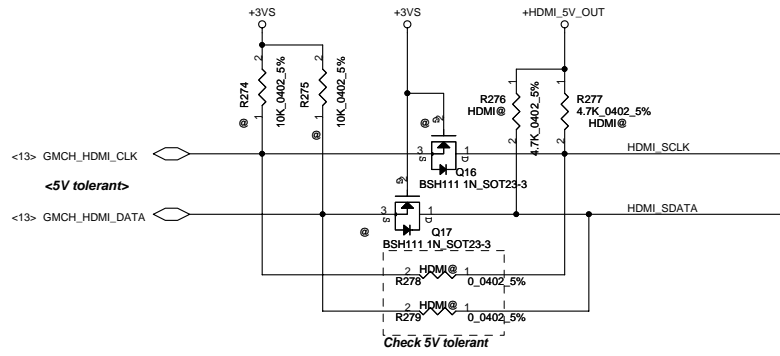


DMIC_DATA R	1	2	220P_0402_50V7K
DMIC_CLK R	1	2	220P_0402_50V7K
DAC_BRIG	1	2	220P_0402_50V7K
INVT_PWM	1	2	220P_0402_50V7K
DISPOFF#	1	2	220P_0402_50V7K

LCD/LED PANEL Conn.

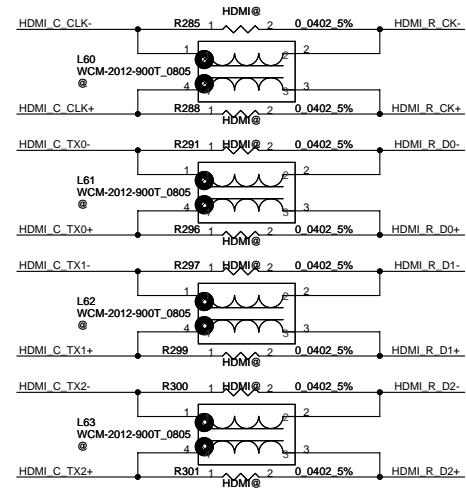
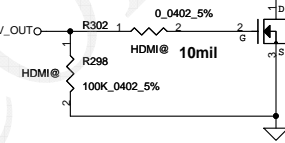


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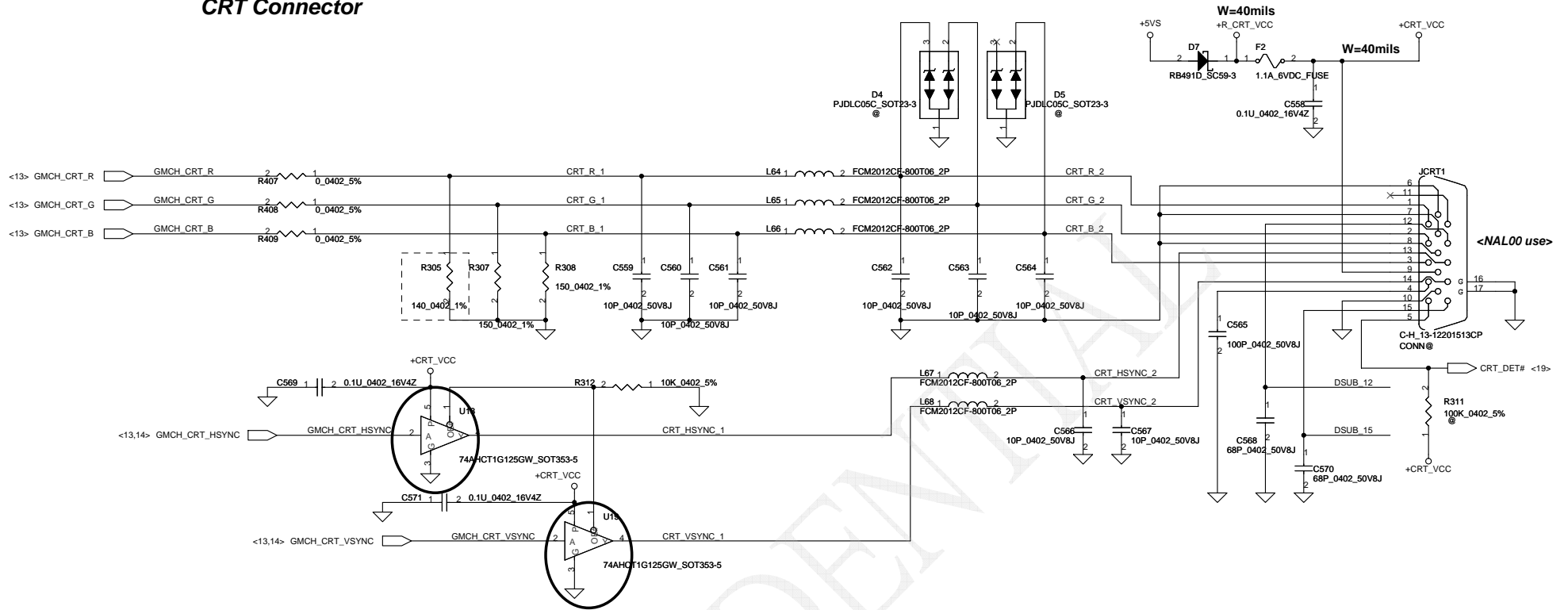
UMA 715 ohm

<12> GMCH_HDMI_TXD2-	C550 HDMI@	1	0.1U_0402_16V7K	HDMI C TX2-	R286	1	HDMI@	2	715_0402_1%
<12> GMCH_HDMI_TXD2+	C551 HDMI@	1	0.1U_0402_16V7K	HDMI C TX2+	R287	1	HDMI@	2	715_0402_1%
<12> GMCH_HDMI_TXD1-	C552 HDMI@	1	0.1U_0402_16V7K	HDMI C TX1-	R289	1	HDMI@	2	715_0402_1%
<12> GMCH_HDMI_TXD1+	C553 HDMI@	1	0.1U_0402_16V7K	HDMI C TX1+	R290	1	HDMI@	2	715_0402_1%
<12> GMCH_HDMI_TXD0-	C554 HDMI@	1	0.1U_0402_16V7K	HDMI C TX0-	R292	1	HDMI@	2	715_0402_1%
<12> GMCH_HDMI_TXD0+	C555 HDMI@	1	0.1U_0402_16V7K	HDMI C TX0+	R293	1	HDMI@	2	715_0402_1%
<12> GMCH_HDMI_TXC-	C556 HDMI@	1	0.1U_0402_16V7K	HDMI C CLK-	R294	1	HDMI@	2	715_0402_1%
<12> GMCH_HDMI_TXC+	C557 HDMI@	1	0.1U_0402_16V7K	HDMI C CLK+	R295	1	HDMI@	2	715_0402_1%



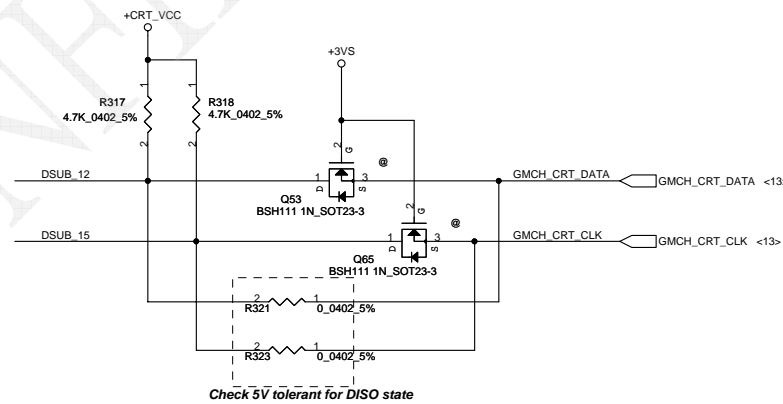
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CRT Connector

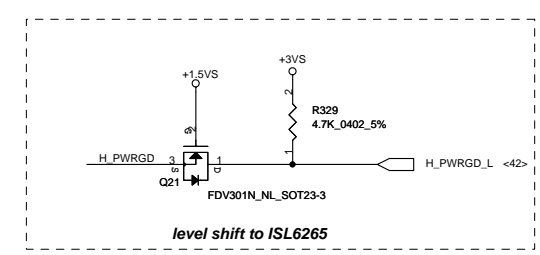
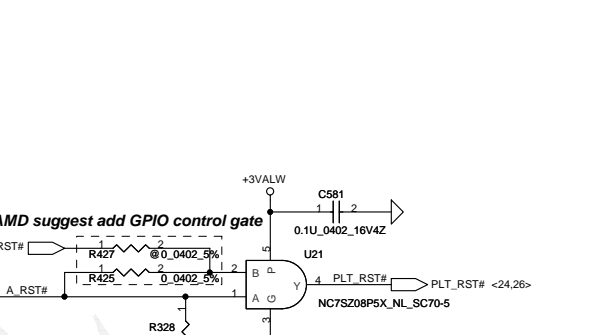
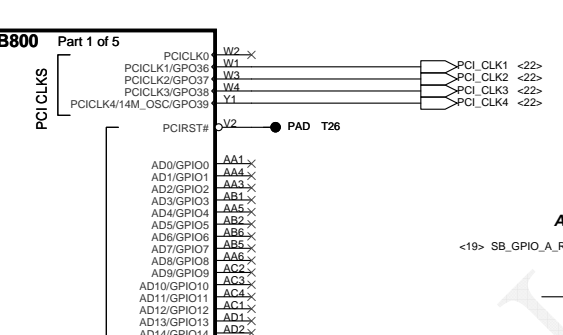
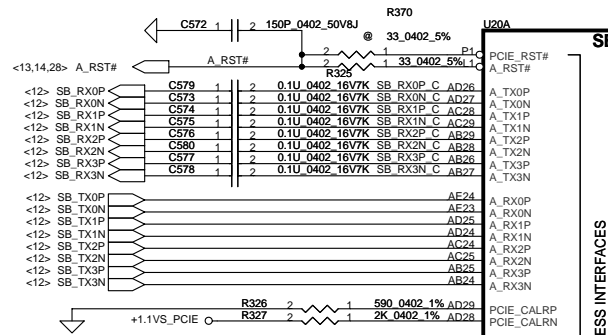


Change as SA411250110

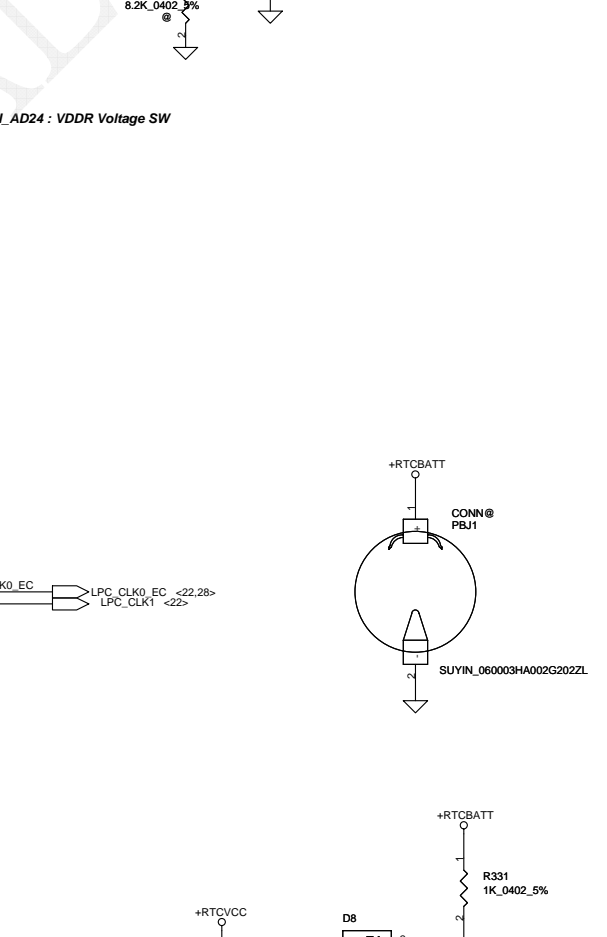
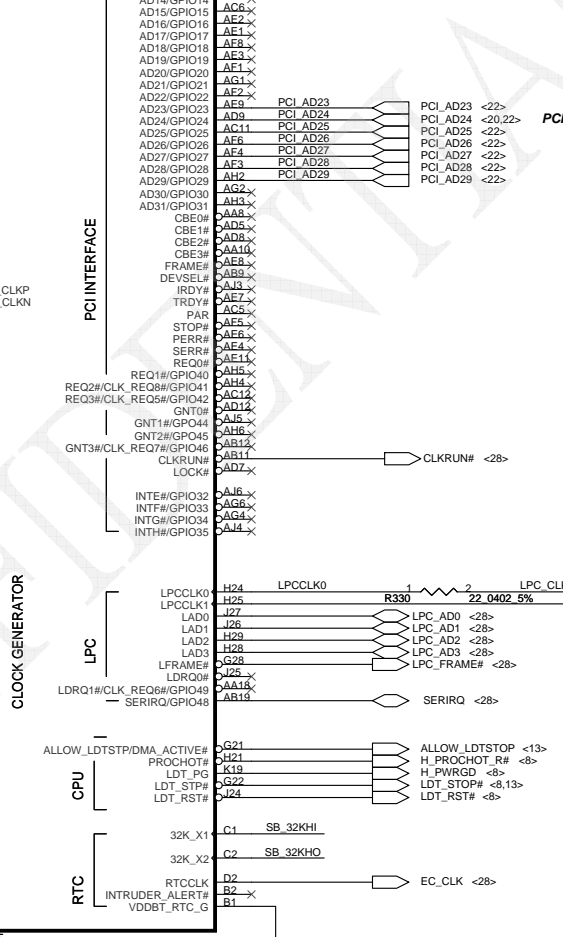
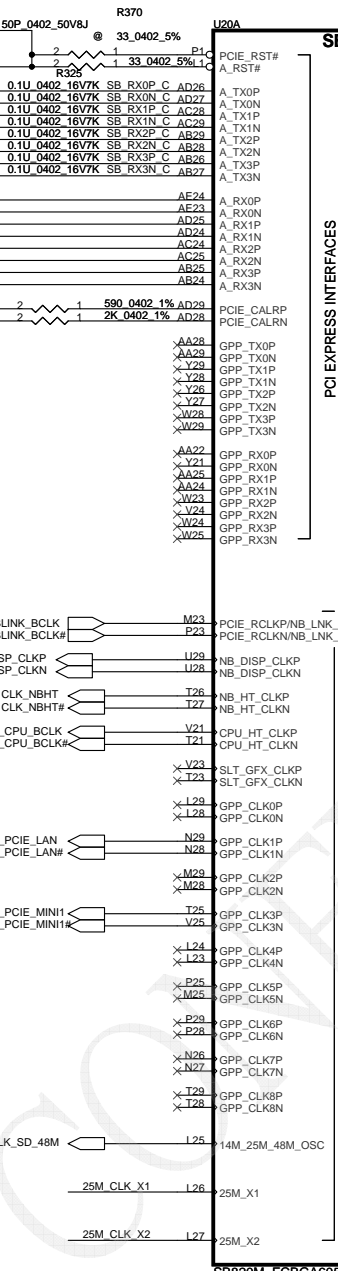
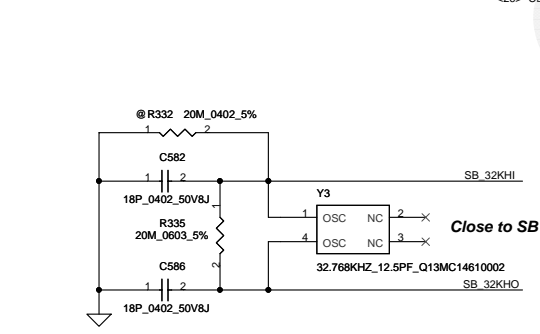
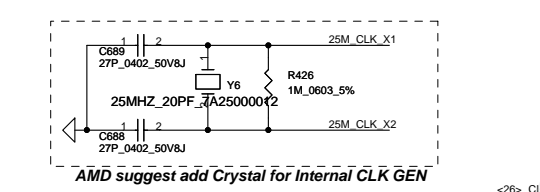
Close to Conn side



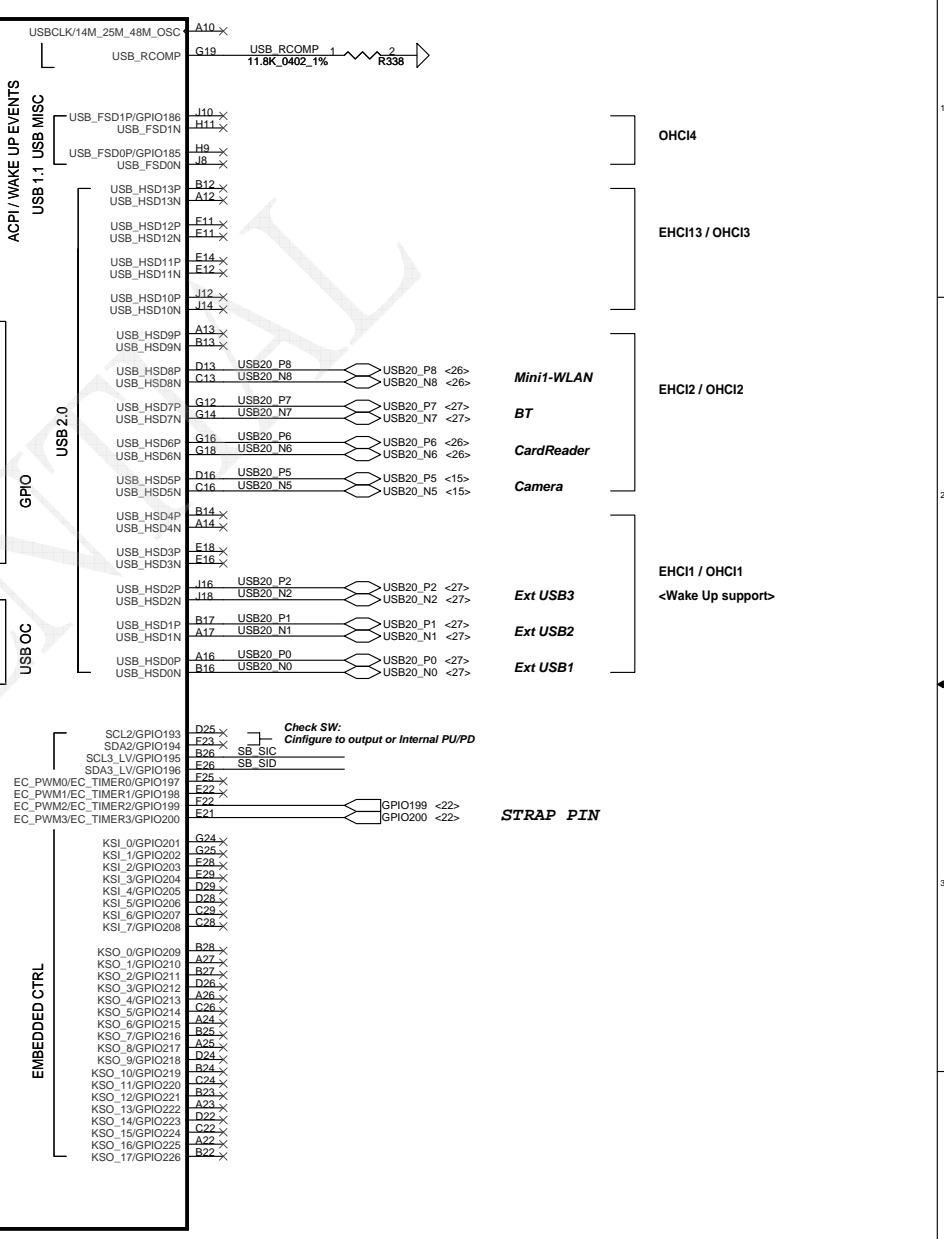
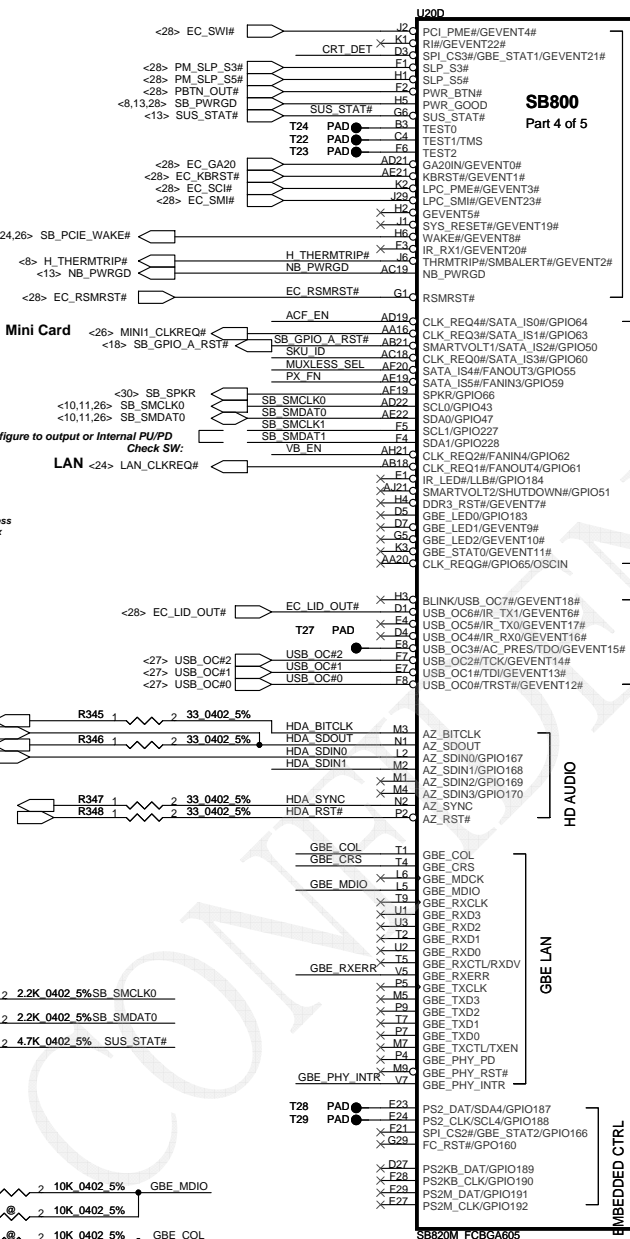
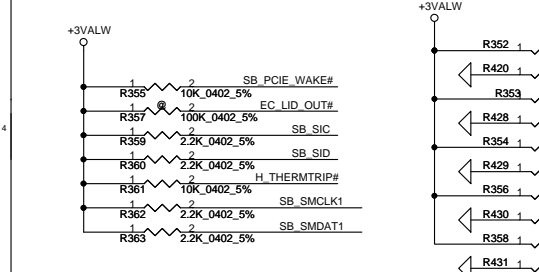
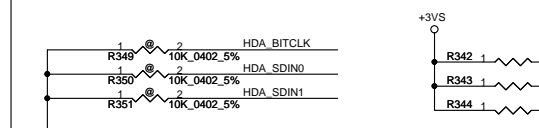
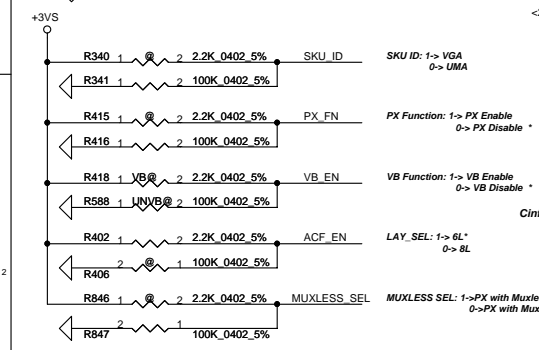
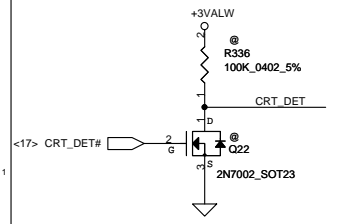
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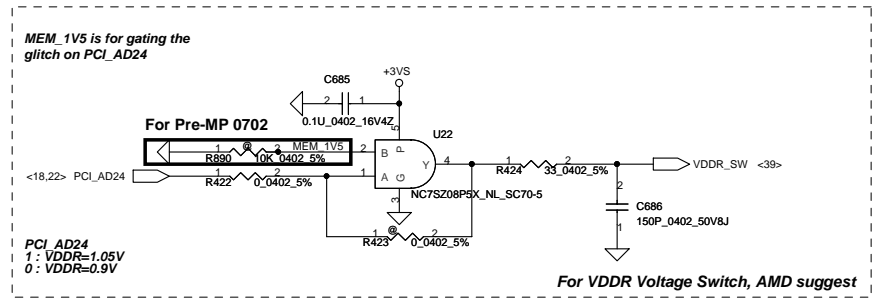
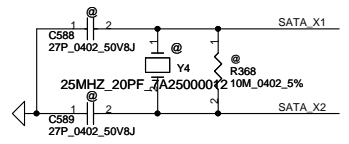
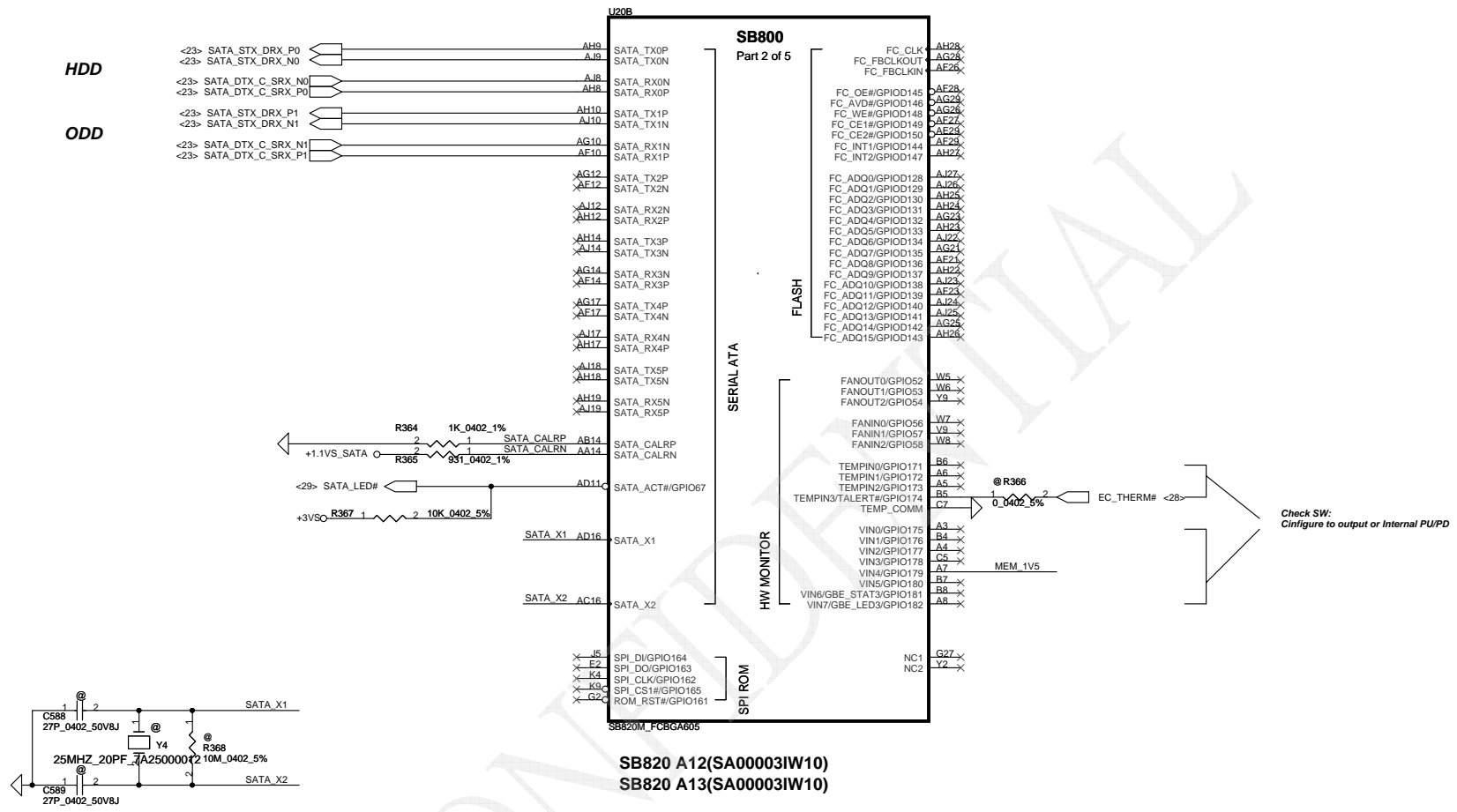
ISL6265 PWROK input, TTL level: 0.8V-2.0V
 When this pin is high, the SVI interface is active and I2C protocol is running. While this pin is low, the SVC, SVD, and VFIXEN input states determine the pre-PWROK metal VID or VFIX mode voltage. This pin must be low prior to the ISL6265 PGOOD output going high



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					SB820-PCIE/PCI/ACPI/LPC/RTC	
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<p>Document Number PEW/76/86/96 LA-6552P</p>			<p>Rev B</p>		
<p>Date: Thursday, July 22, 2010 Sheet 19 of 45</p>					

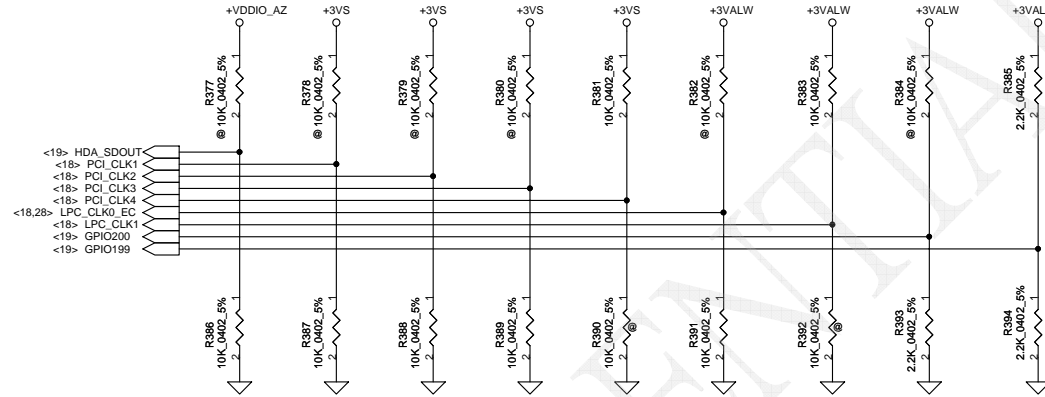


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				SB820 SATA/IDE/SPI	
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REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1		GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable	EC ENABLE	CLOCKGEN ENABLE		H,H = Reserved H,L = SPI ROM	
PULL LOW	Performance MODE	FORCE PCIE GEN1	WATCHDOG TIMER DISABLE	IGNORE DEBUG STRAP	Inter CLK Gen Mode Disable	EC DISABLE	CLOCKGEN DISABLE		L,H = LPC ROM (Default L,NC) L,L = FWH ROM	
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT			



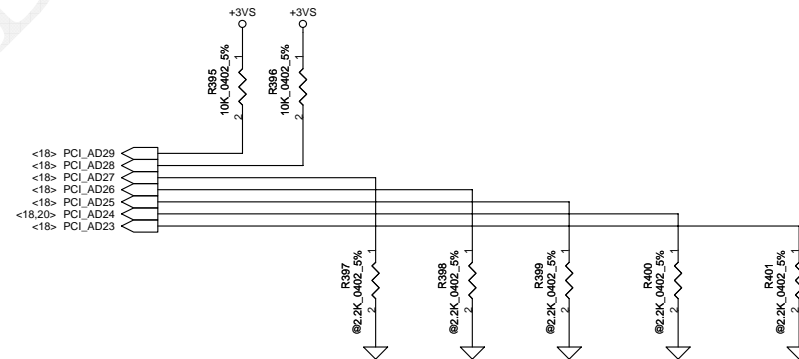
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

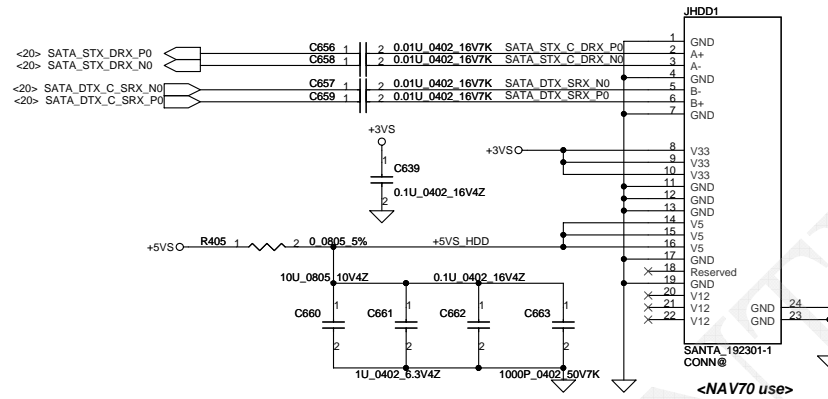
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Check AD29,AD28 strap function

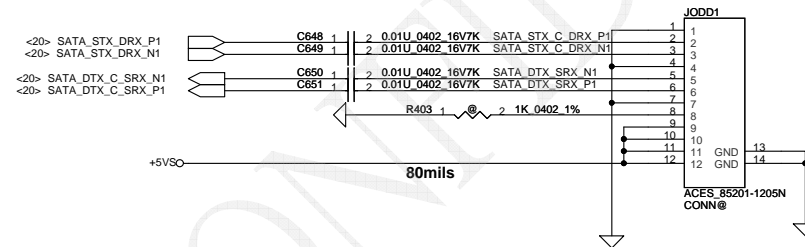
check default



SATA HDD Conn.

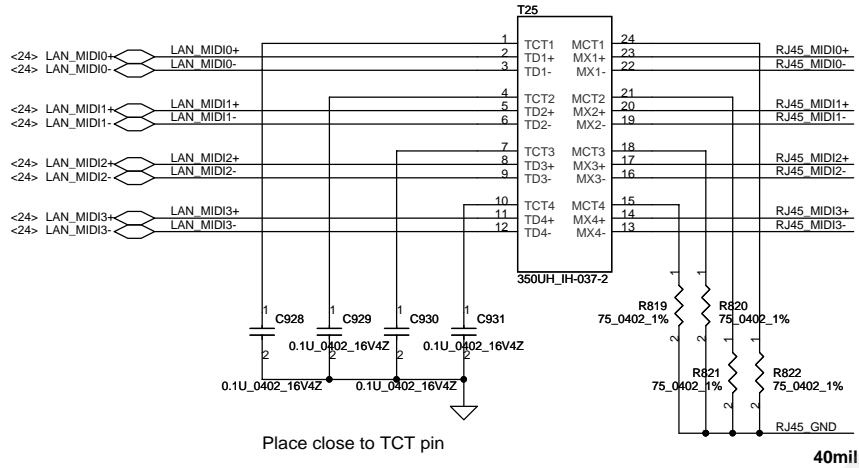


SATA ODD FFC Conn.

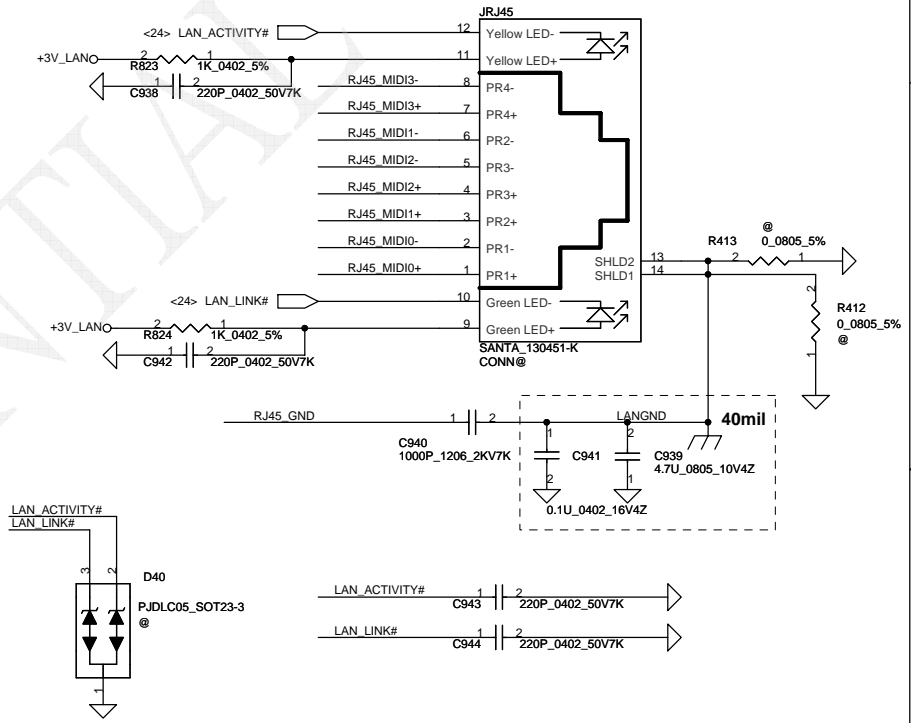


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BH GS5009-D <SP050006B00>

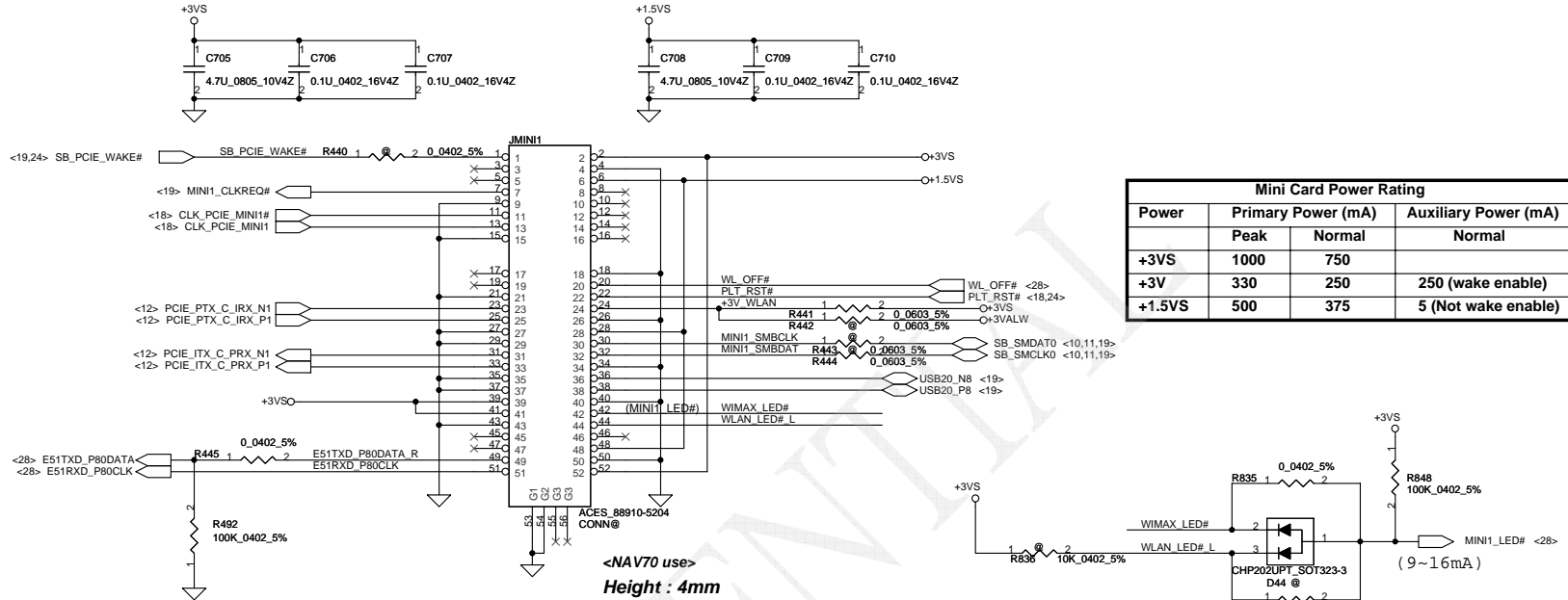


LAN Connector



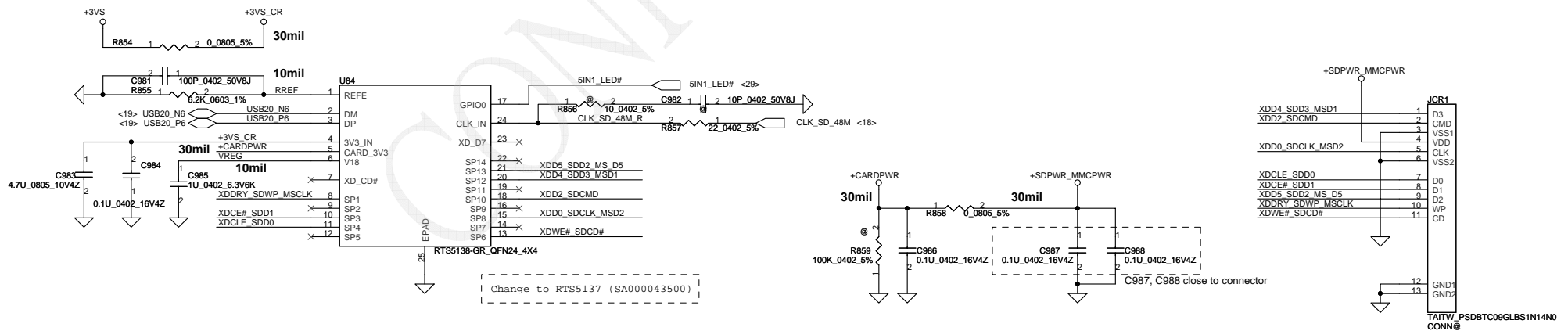
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Mini-Express Card for WLAN

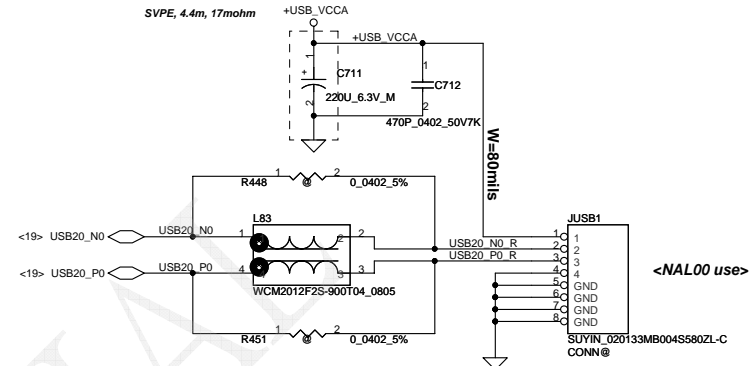
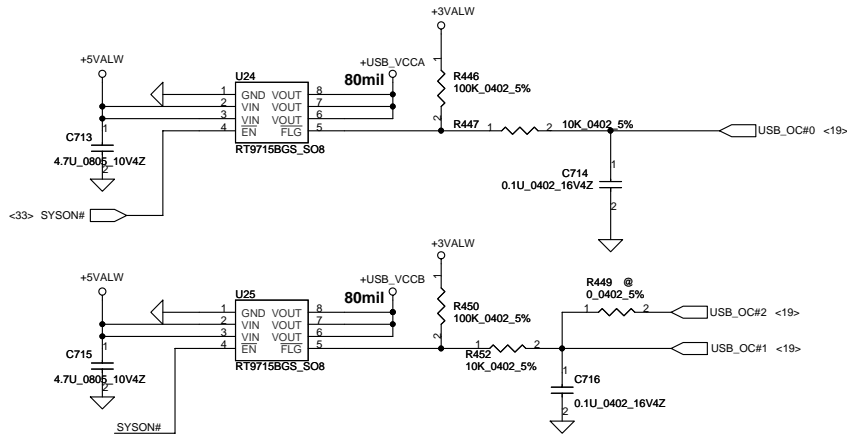


Card Reader RTS5138 / RTS5137 (only SD+MMC function)

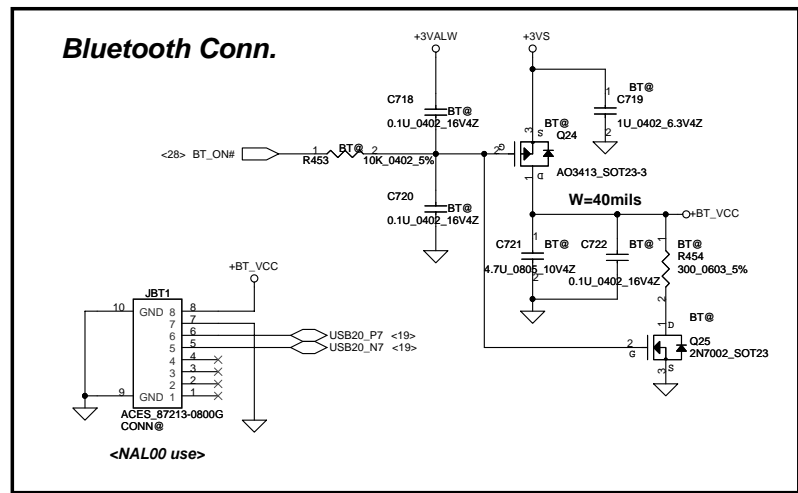
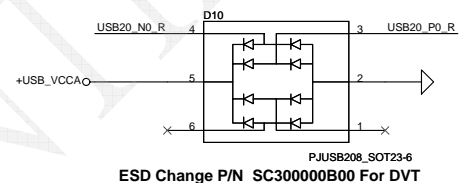
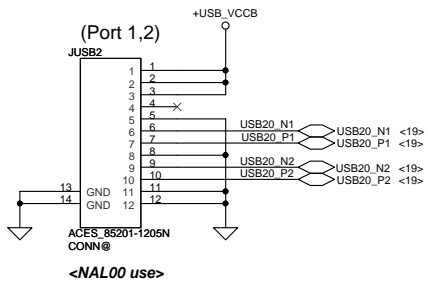
Card Reader Connector



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				Document Number
				PEW/76/86/96 LA-6552P
				Date: Thursday, July 22, 2010
				Sheet 26 of 45



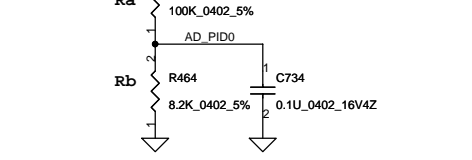
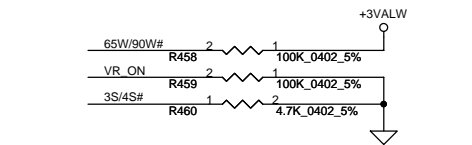
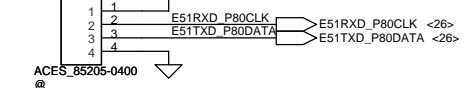
To USB/B Connector



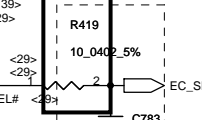
Security Classification		Compal Secret Data		Title	
Issued Date	2010/04/12	Deciphered Date	2010/10/12	Bluetooth / Int USB x2 / eSATA	
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For EC Tools

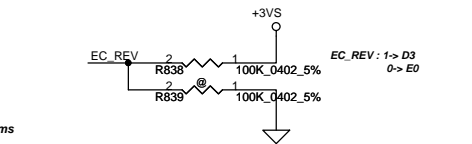
Place on MiniCard door



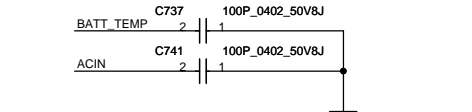
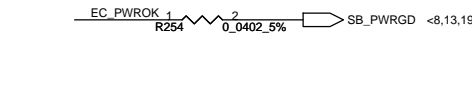
For Pre-MP 07/05



Reserve for EMI, close to EC



Delay SUSP# 10ms



KB926 Rev:D3(SA00001J580)
KB926 Rev:E0(SA00001J5A0)

Table with 4 columns: Security Classification, Compal Secret Data, Deciphered Date, Title. Row 1: Security Classification, 2010/04/12, 2010/10/12, EC ENE KB926. Row 2: Issued Date, 2010/04/12, Deciphered Date, 2010/10/12.

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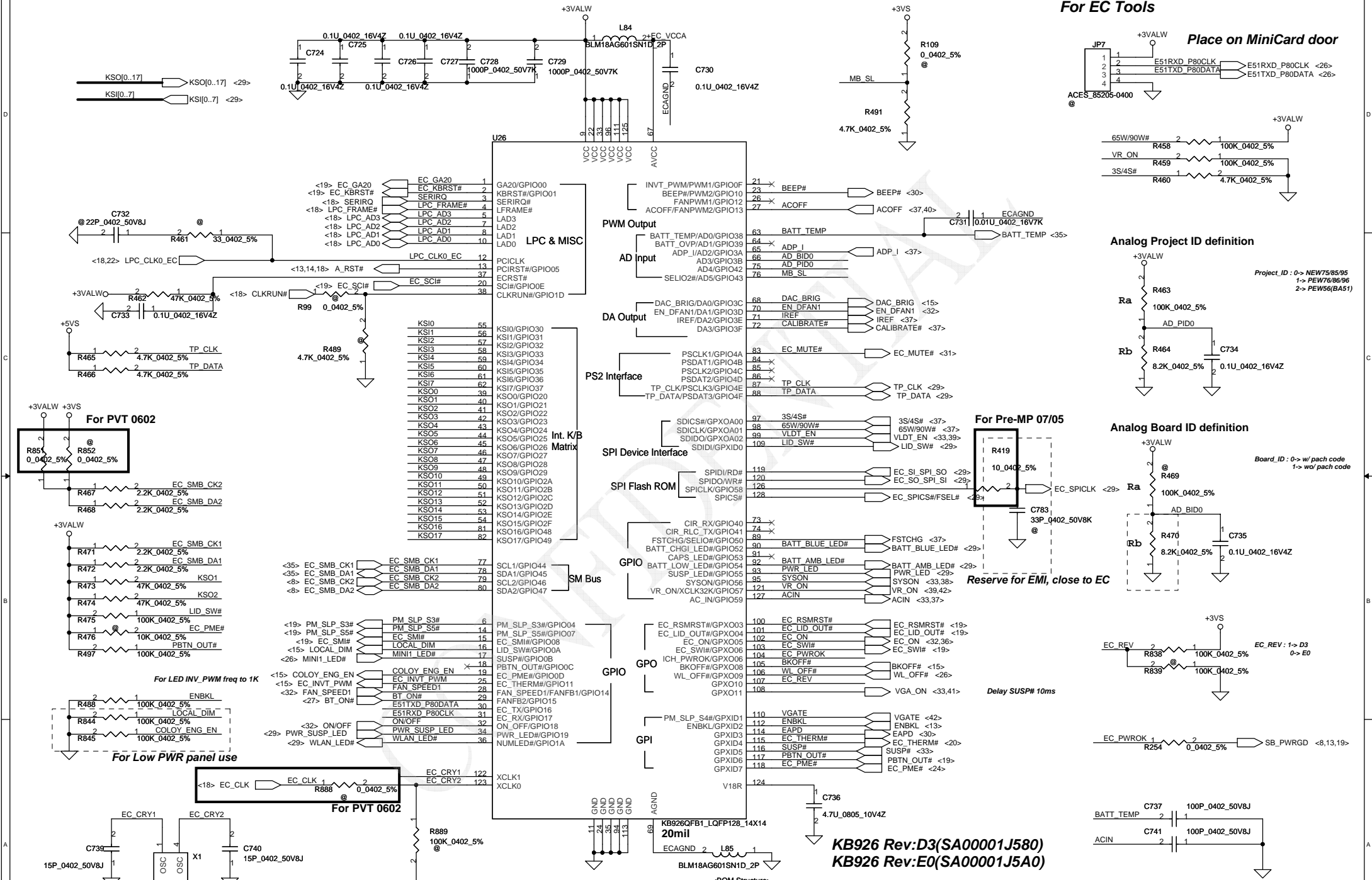
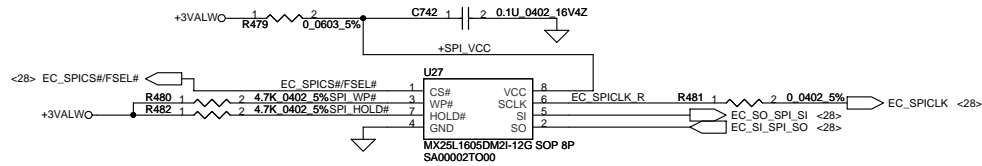
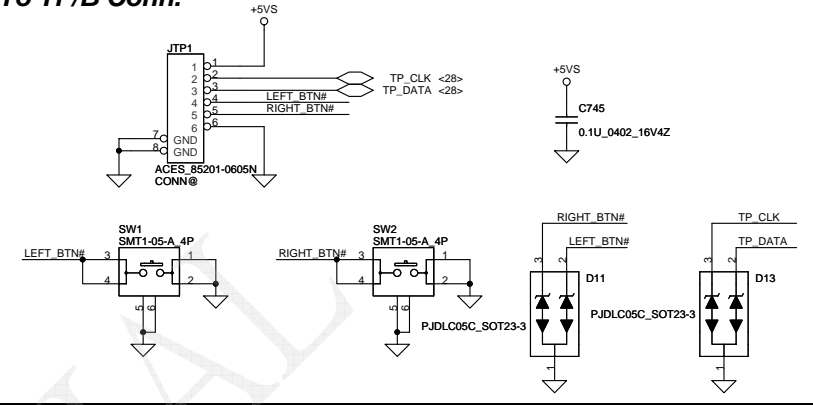


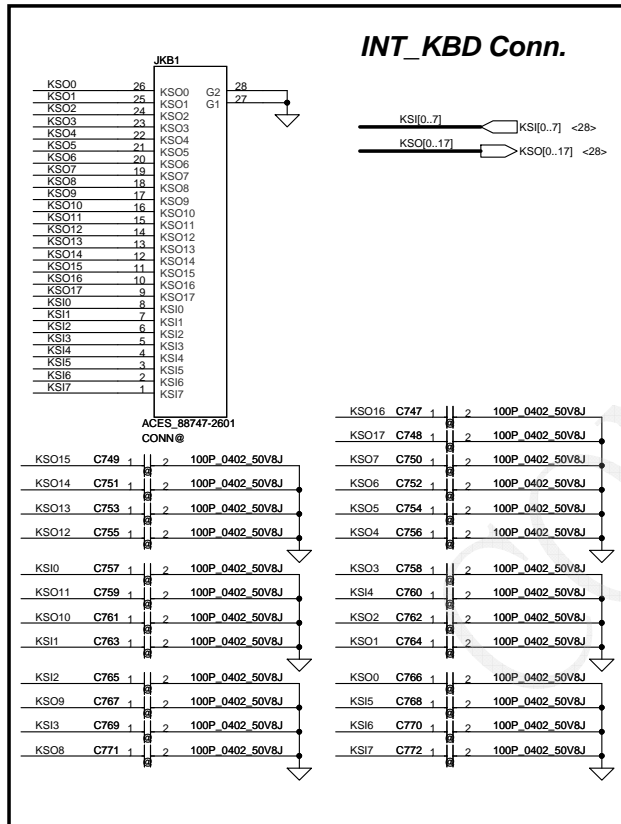
Table with 4 columns: Security Classification, Compal Secret Data, Deciphered Date, Title. Row 1: Security Classification, 2010/04/12, 2010/10/12, EC ENE KB926. Row 2: Issued Date, 2010/04/12, Deciphered Date, 2010/10/12.



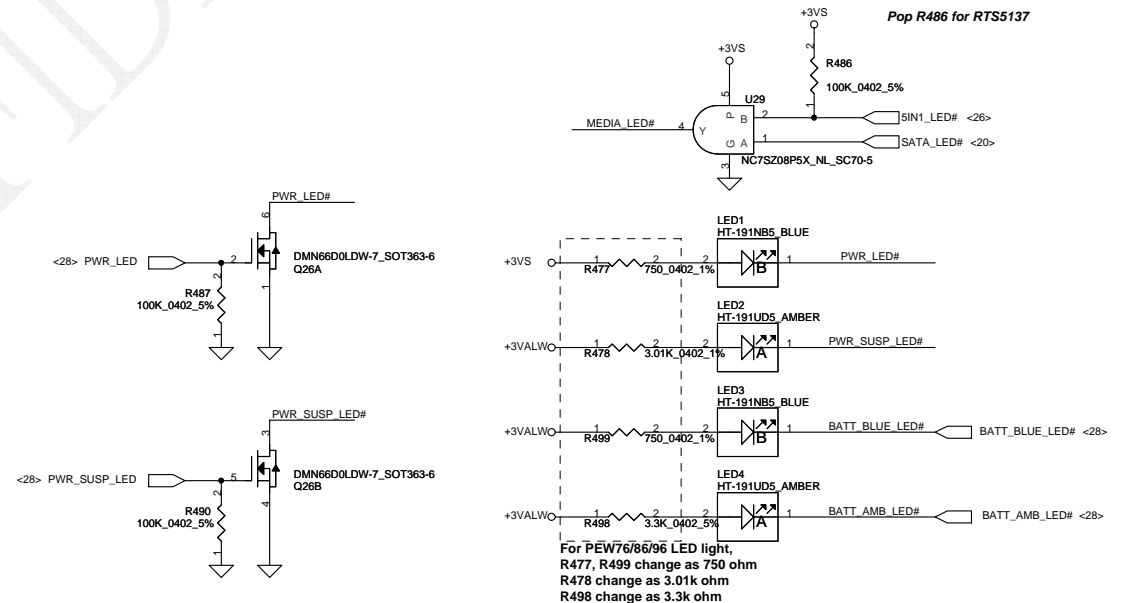
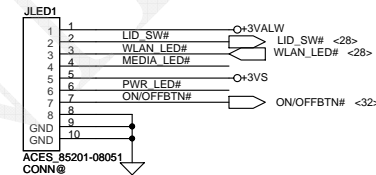
To TP/B Conn.



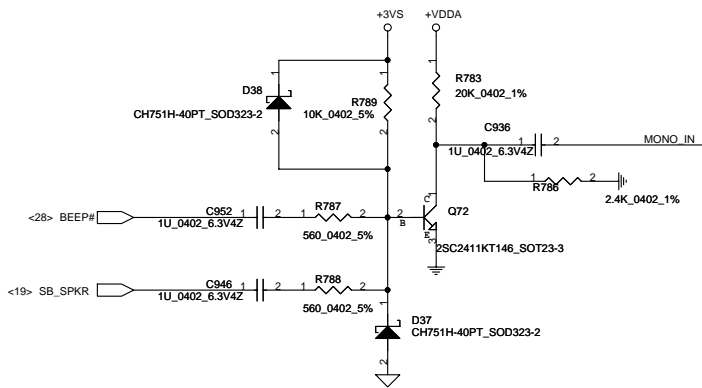
INT_KBD Conn.



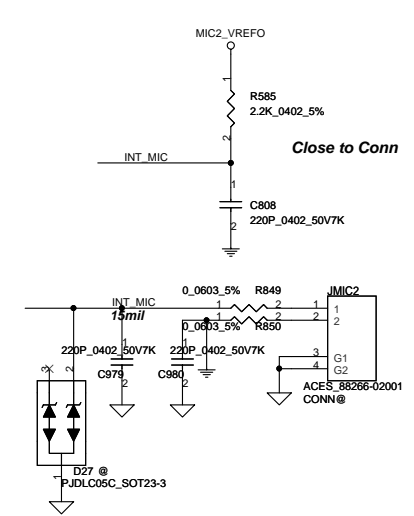
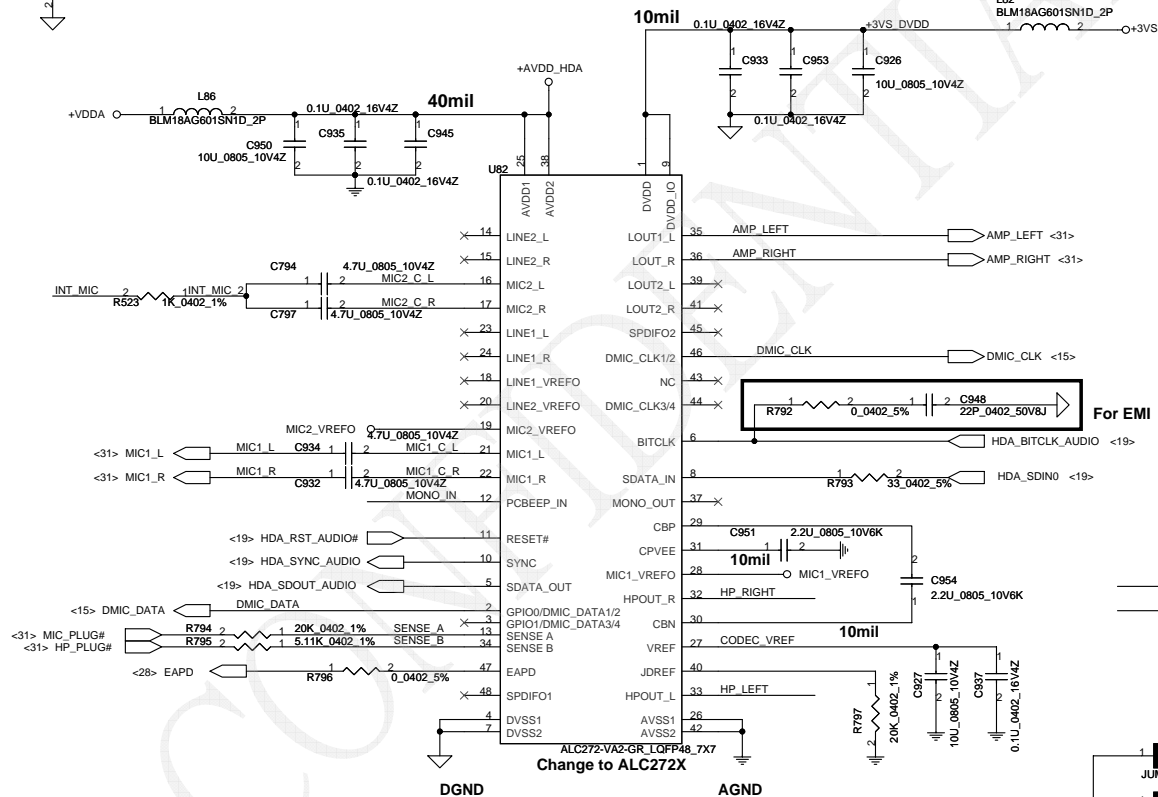
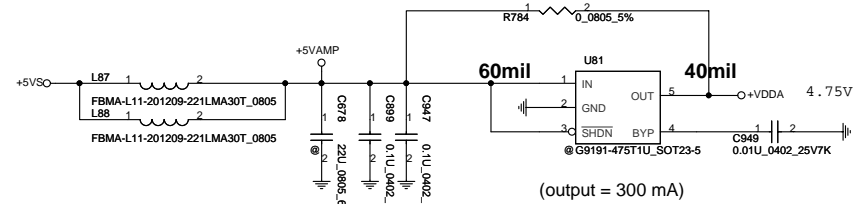
For PVT 0608 Unpop Cap.



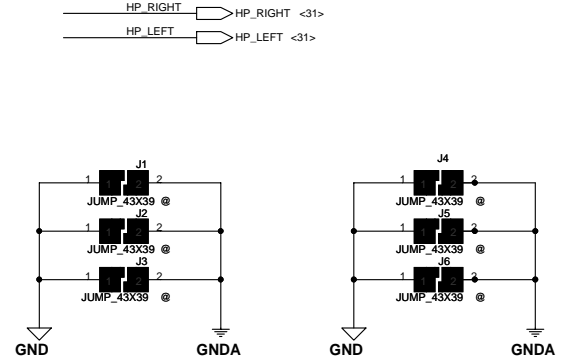
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/04/12	Deciphered Date	2010/10/12	Title	BIOS, I/O Port & K/B Connector
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HD Audio Codec

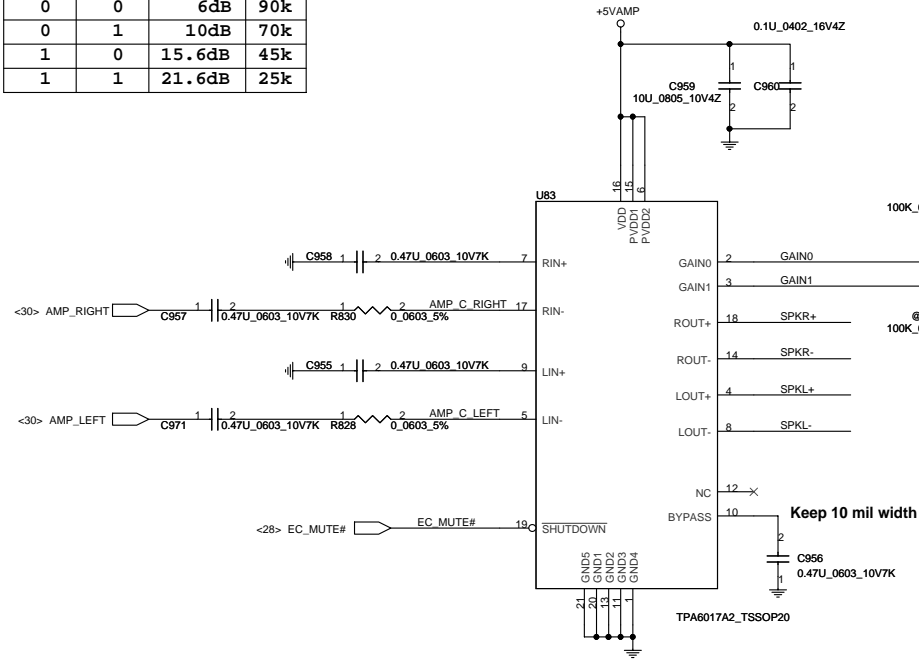


For EMI

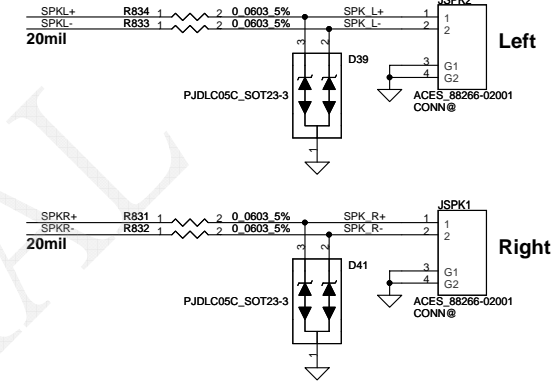


ALC272X			
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	LOUT2
	20K	PORT-B (PIN 21, 22)	MIC1
	10K	PORT-C (PIN 23, 24)	LINE1
	5.1K	PORT-D (PIN 35, 36)	LOUT1
SENSE B	39.2K	PORT-E (PIN 14, 15)	LINE2
	20K	PORT-F (PIN 16, 17)	MIC2
	5.1K	PORT-J (PIN 32, 33)	HP

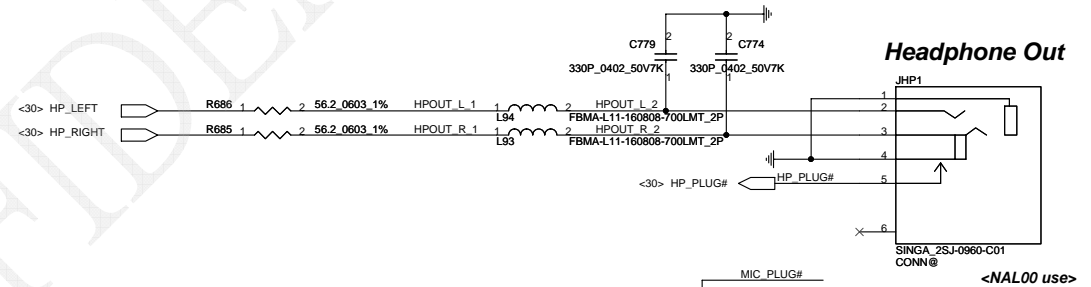
GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k



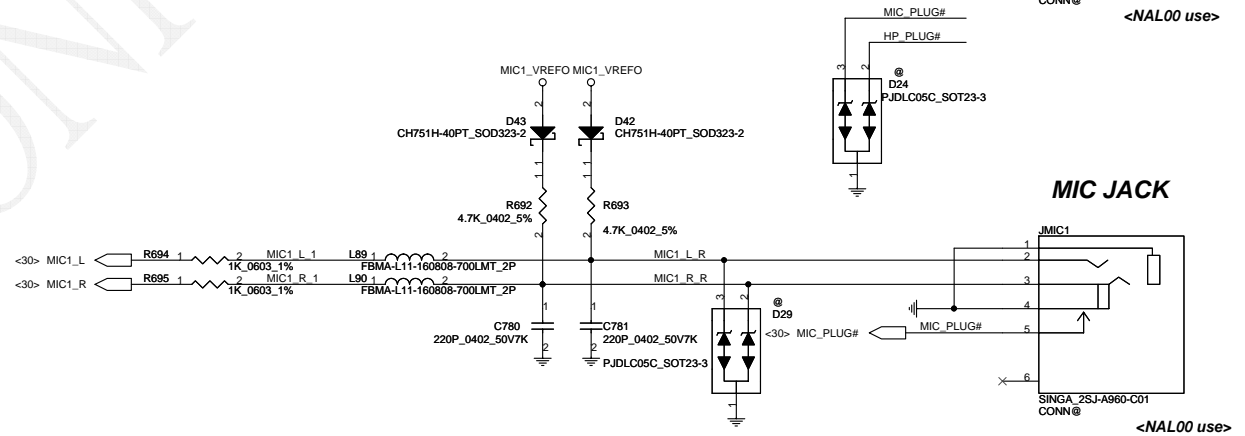
Int. Speaker Conn.



Headphone Out

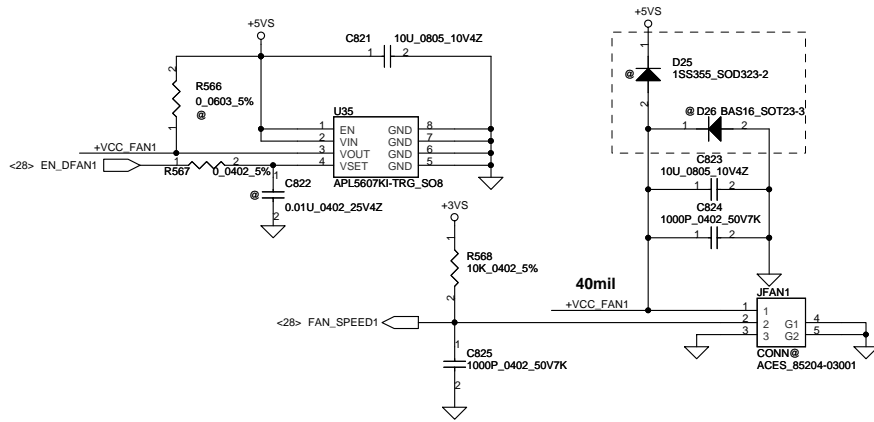


MIC JACK

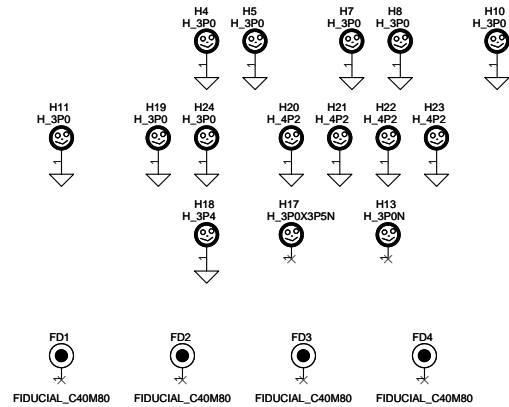
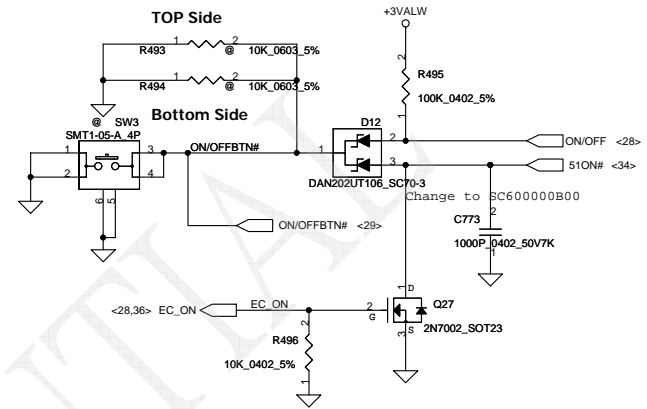


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Date: Thursday, July 22, 2010				Sheet 31 of 45

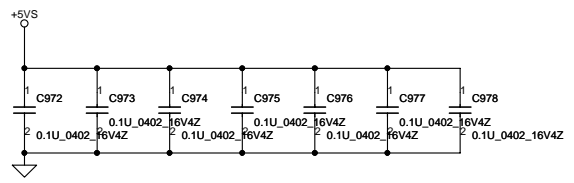
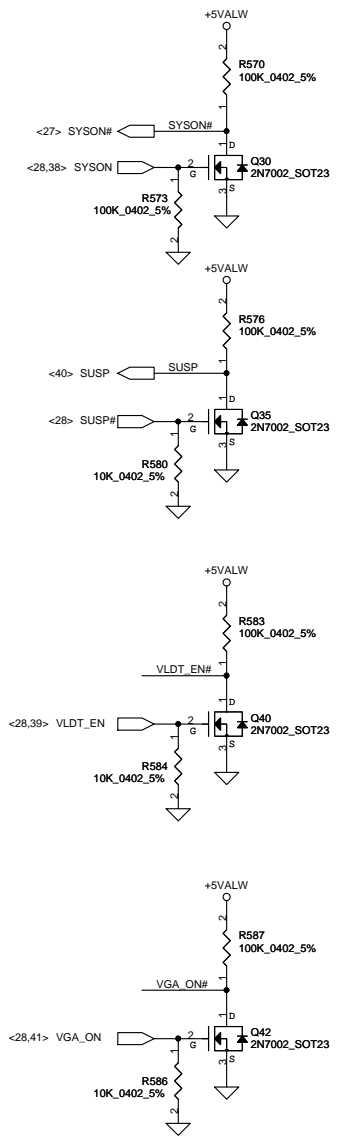
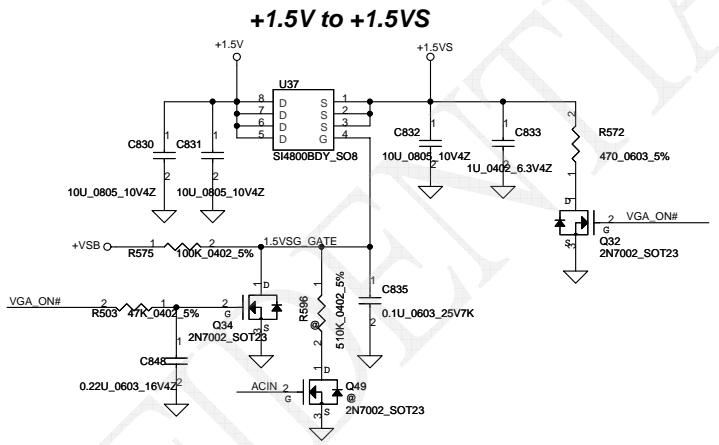
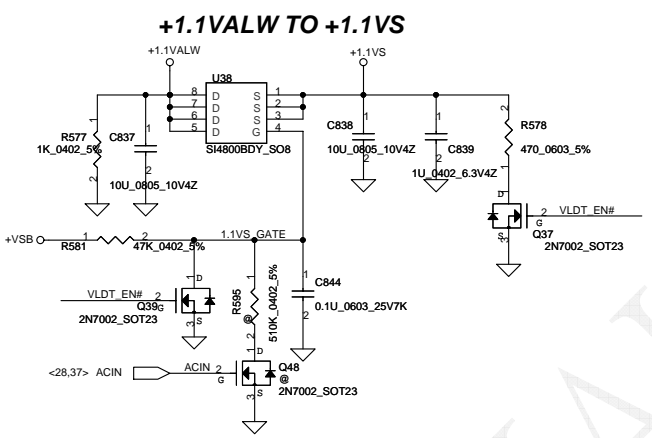
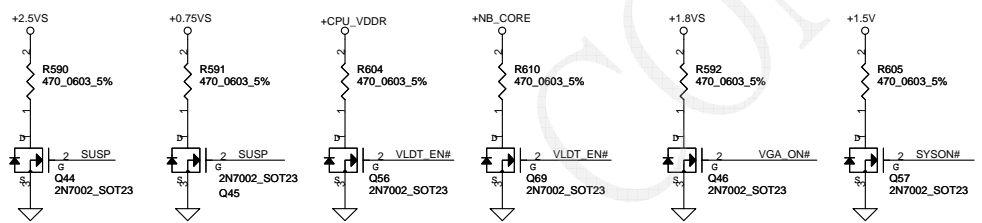
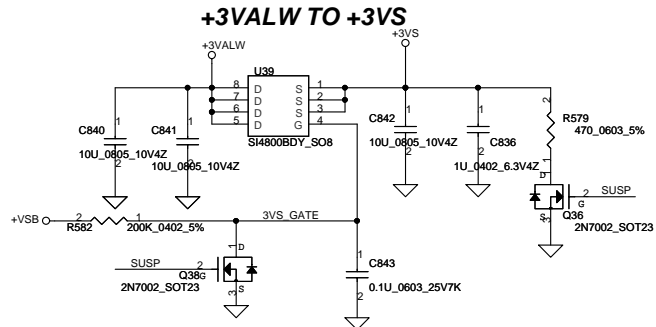
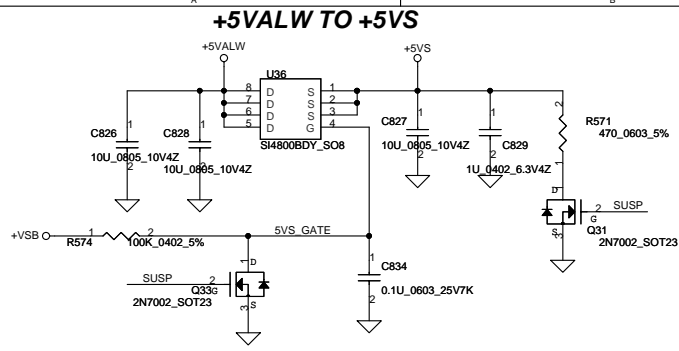
FAN1 Conn



ON/OFF switch *Power Button*



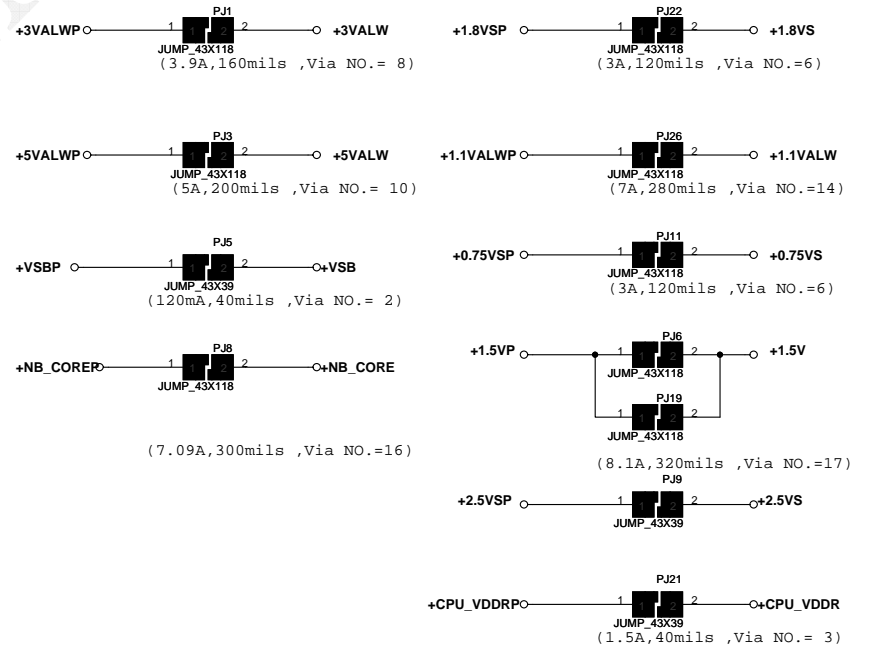
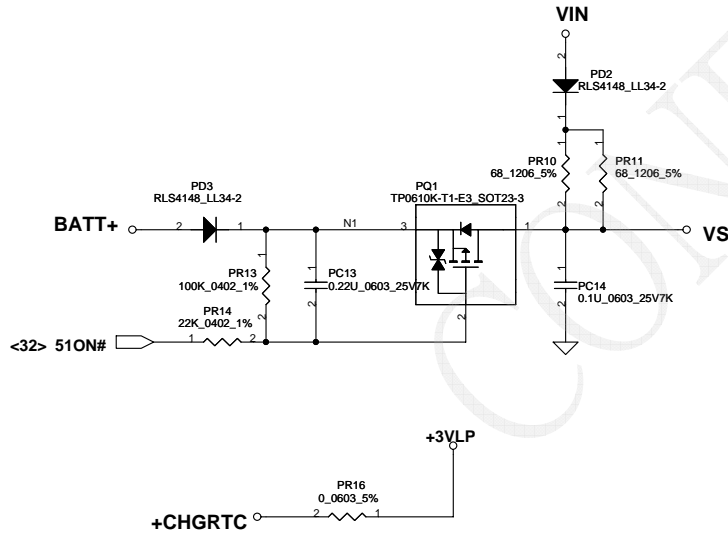
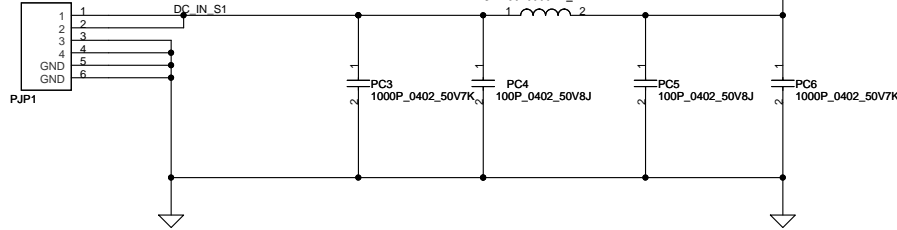
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/04/12	Deciphered Date	2010/10/12	Title	FAN & Screw Hole & PBTN
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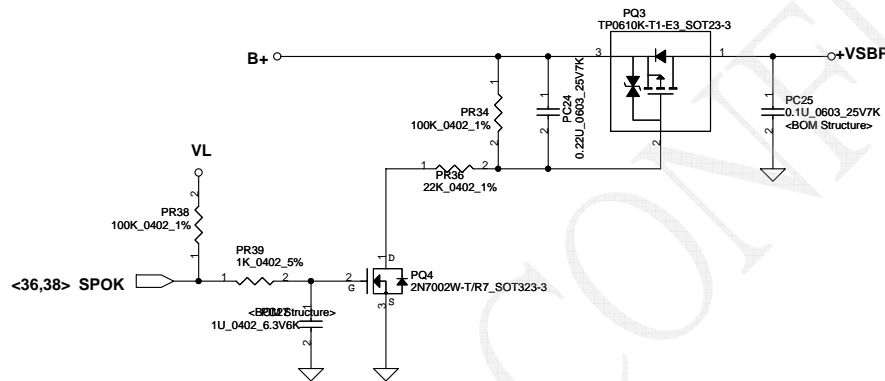
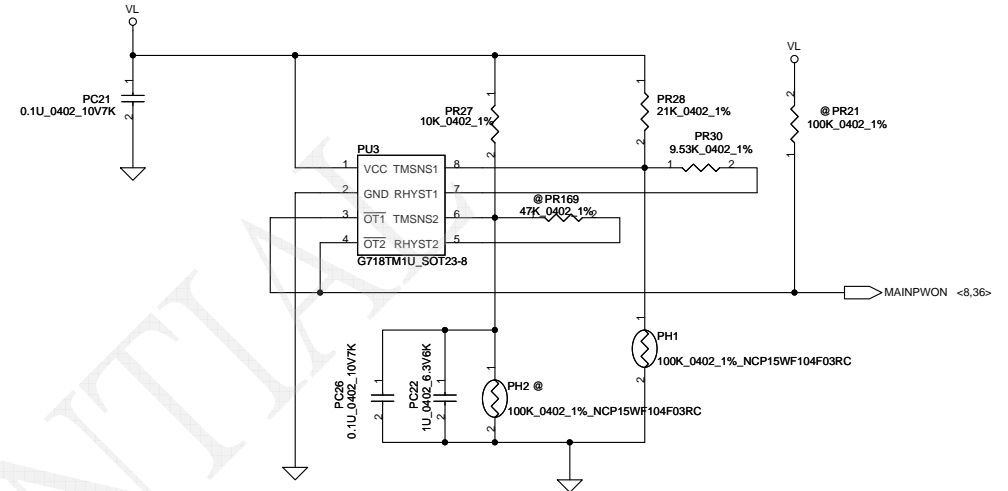
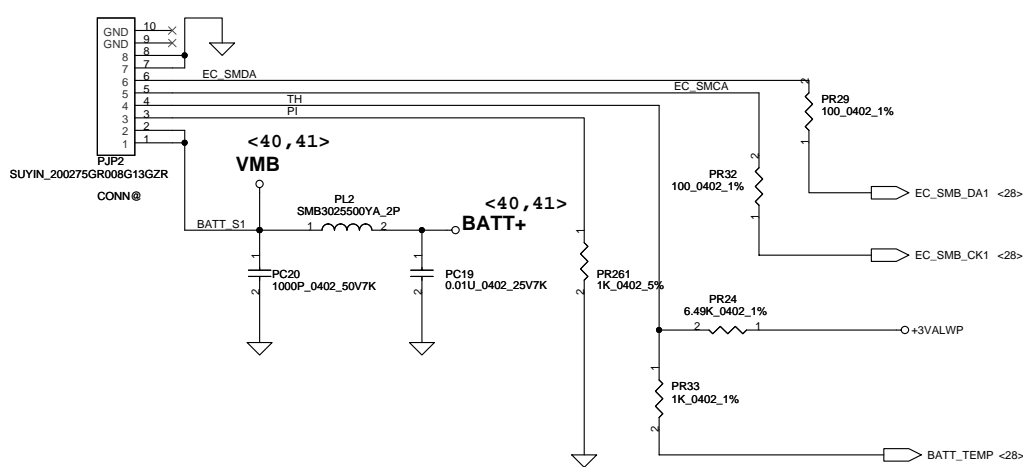
DC-IN cable: DC301009W00 (Yellow)

SP02000GC00
ACES_50305-00441-001



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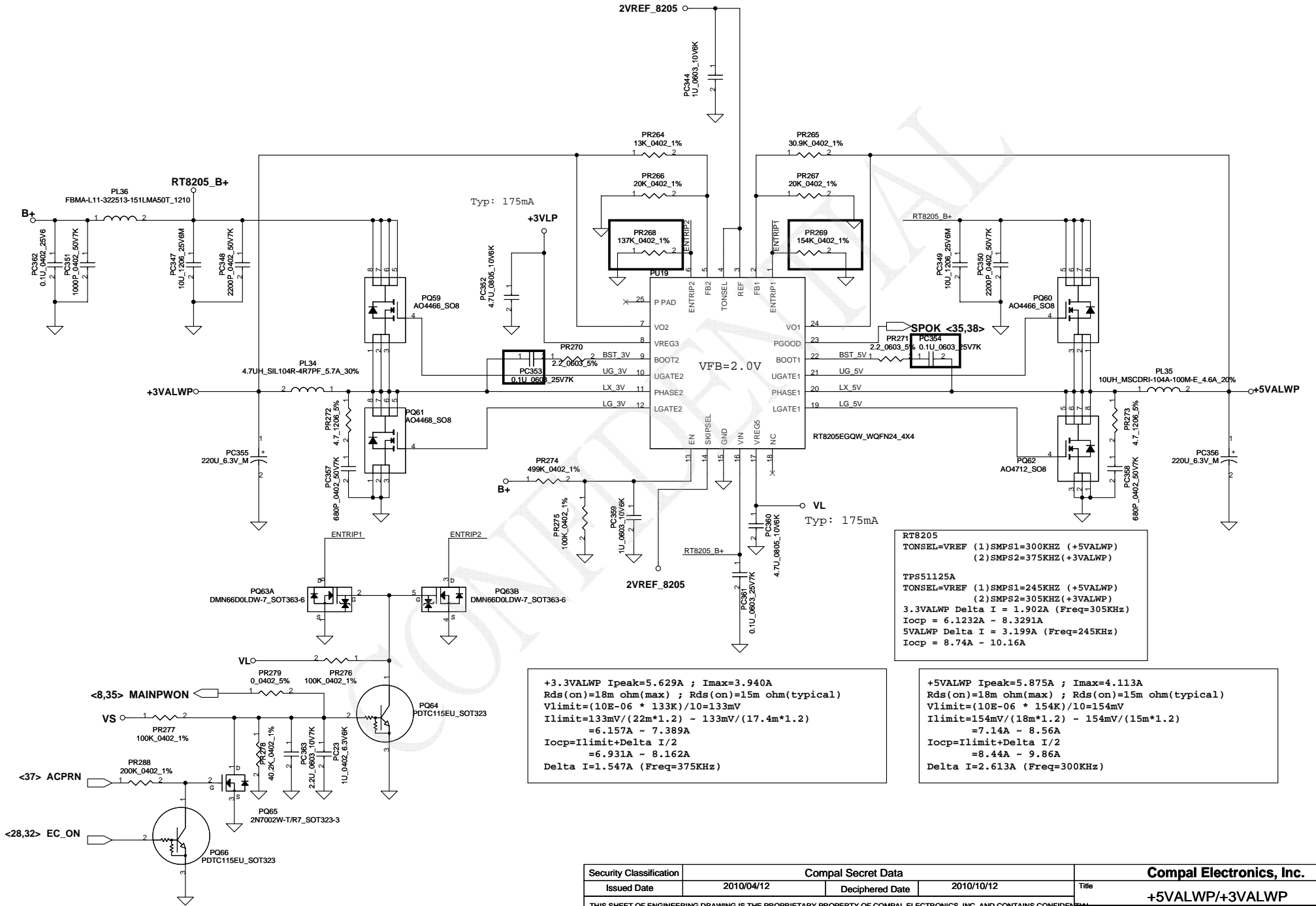
PH1 under CPU botten side : Not SPEC, reference only!
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO



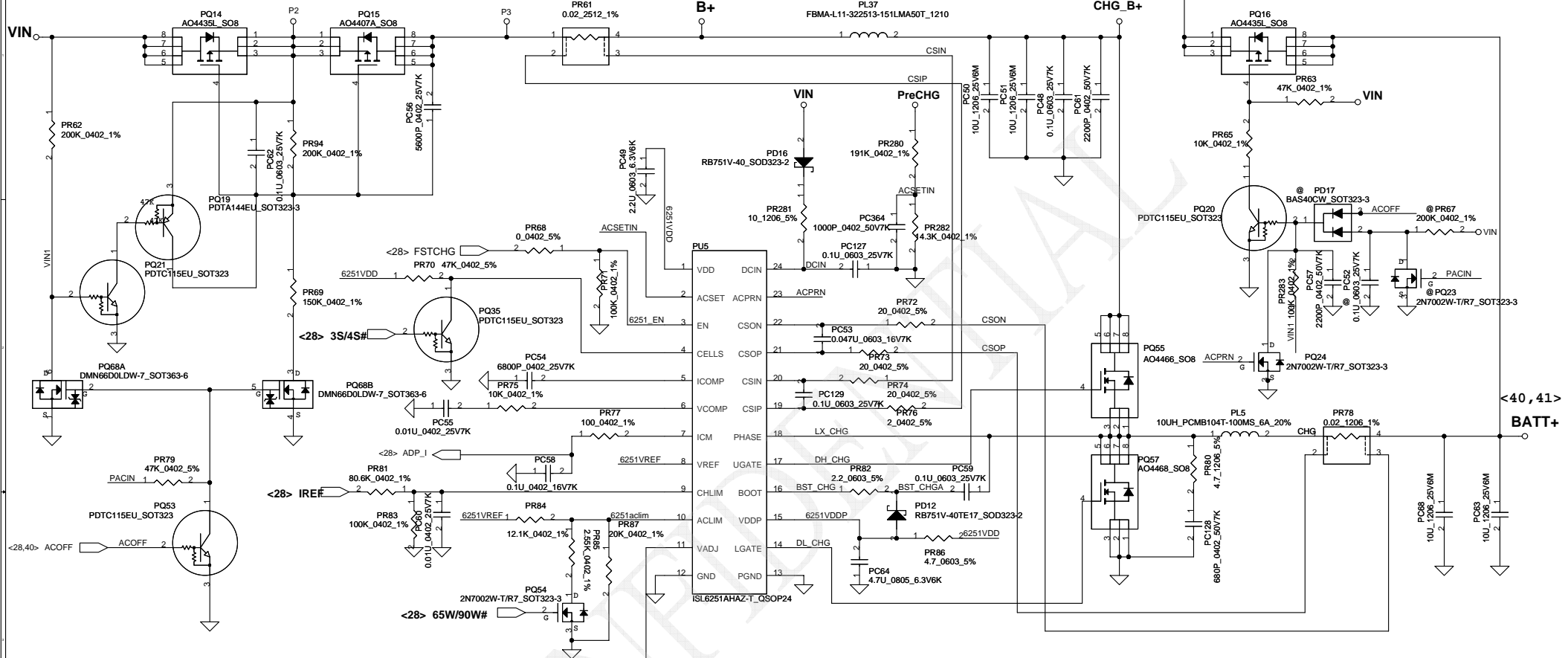
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Iada=0~3.42A(65W/19V=3.421A)

Iada=0~4.74A(90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 2.91A
 CP = 85%*Iada ; CP = 4.07A

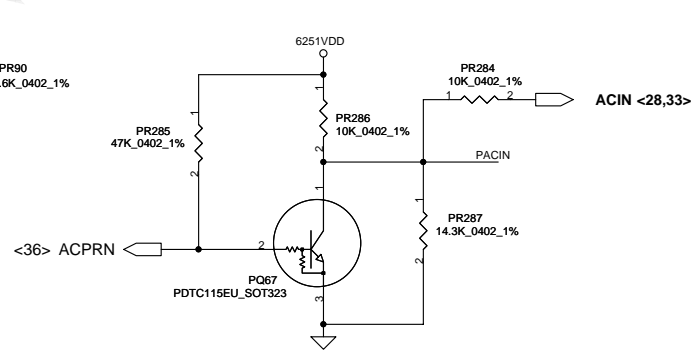


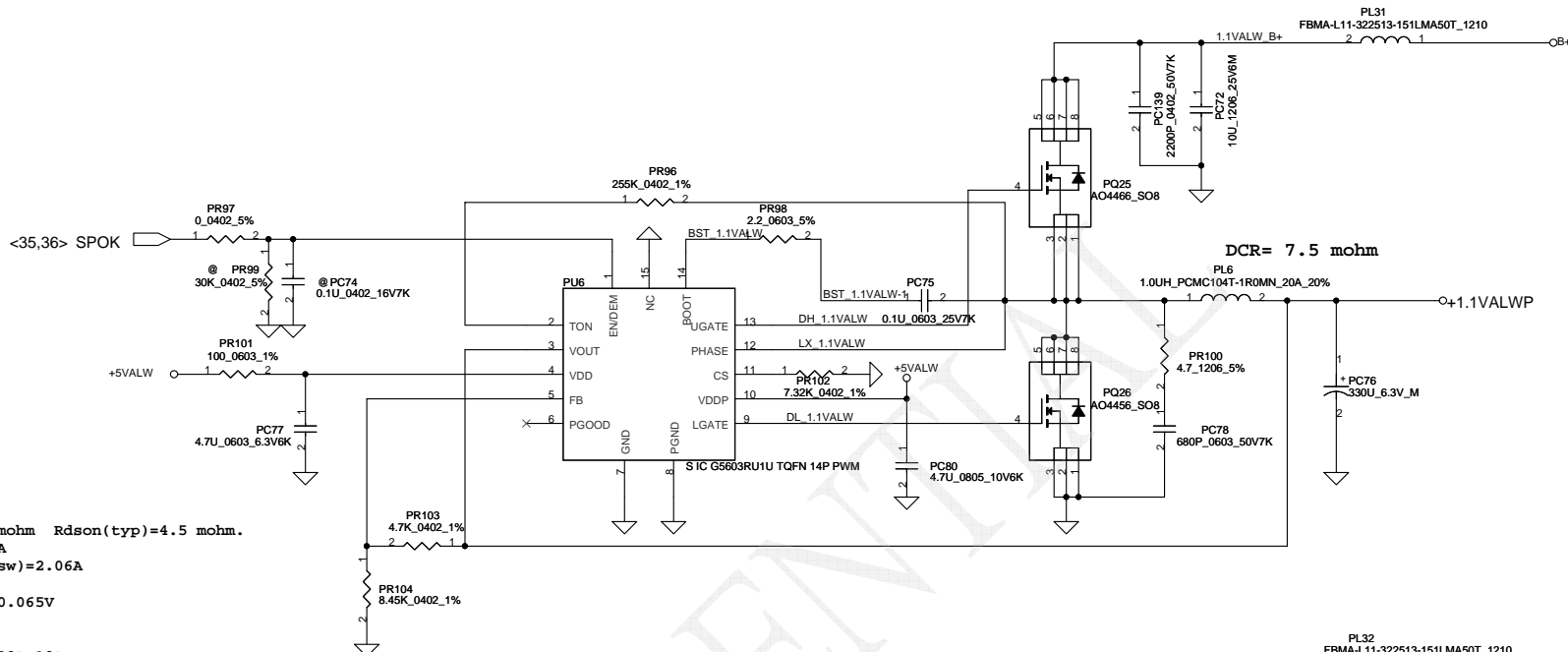
Iada=0~4.74A(90W) CP= 85%*Iada ; CP=4.03A
 Iada=0~3.42A(65W) CP= 85%*Iada ; CP=2.91A

CP mode
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
 where $V_{ac1m} = 1.464V$ (90W), $I_{input} = 4.03A$
 PR84=12.1K; PR87=20K
 where $V_{ac1m} = 0.391V$ (65W), $I_{input} = 2.91A$
 PR84=12.1K; PR85=2.55K

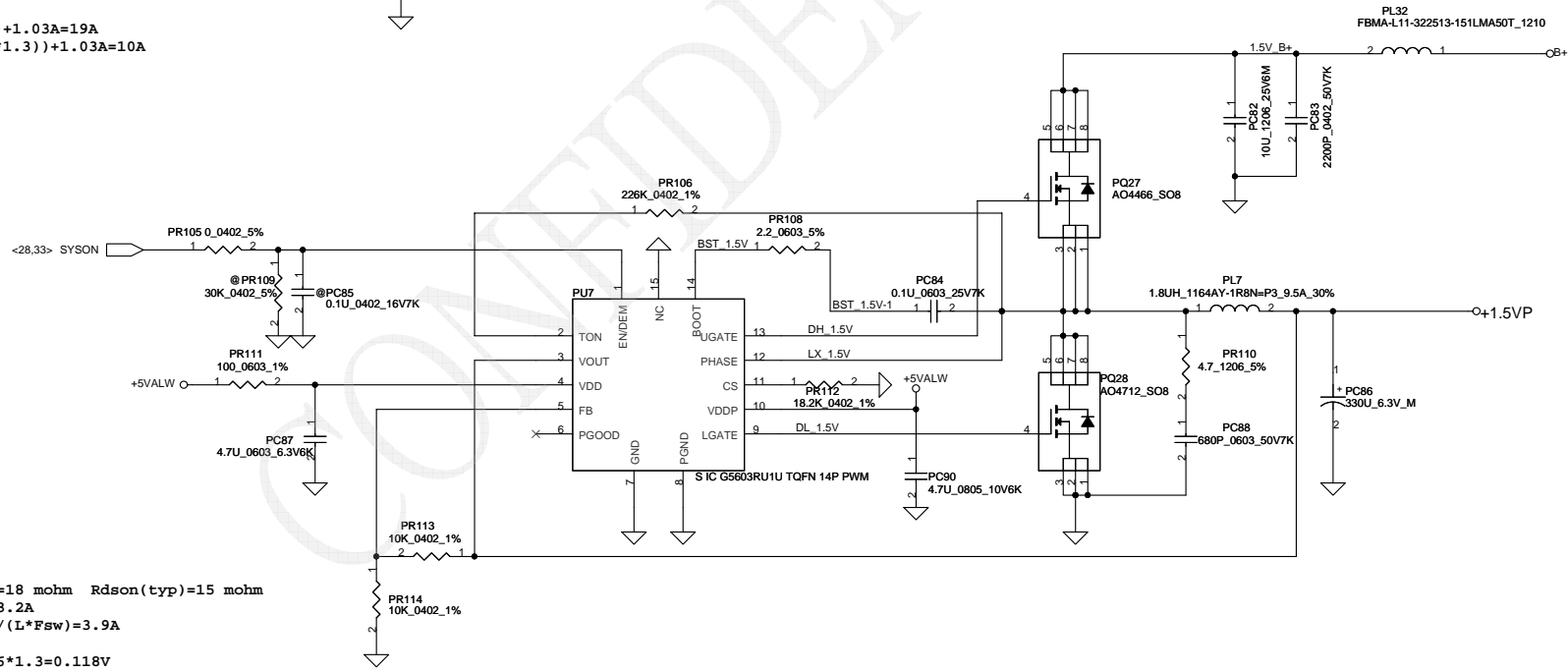
CC=0.6~4.48A
 IREF=1.016*Icharge
 IREF=0.43V~3.24V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V



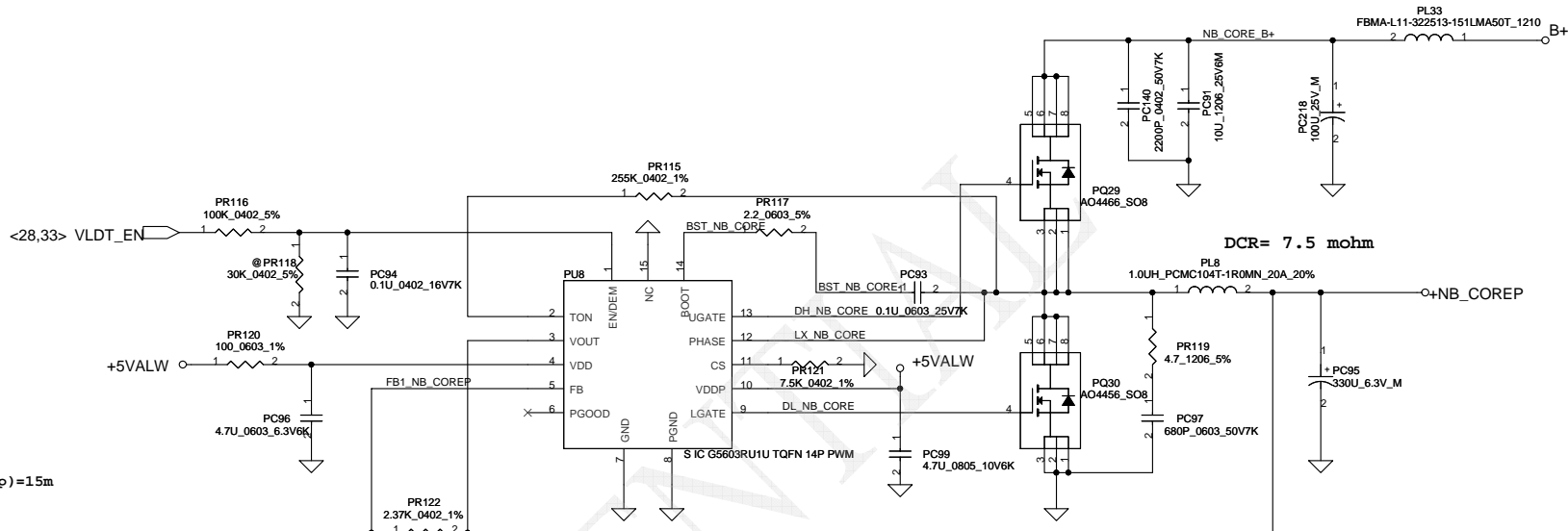


$<V_o=1.1V>$ $V_{FB}=0.75V$
 $V=0.75*(1+4.7K/10K)=1.1V$
 $F_{sw}=280KHz$
 $C_{out} ESR=15m\ \Omega$ $R_{dson(max)}=5.6\ m\Omega$ $R_{dson(typ)}=4.5\ m\Omega$
 $I_{peak}=7.42A$ $I_{max}=5.2A$ $I_{ocp}=8.9A$
 $\Delta I=((19-1.1)*(1.1/19))/(L*F_{sw})=2.06A$
 $\Rightarrow 1/2\Delta I=1.03A$
 $V_{tripmax}=I_{ocp}*R_{dson}=8.9*5.6*1.3=0.065V$
 $R_{cs}=V_{trip}/9\mu A=0.065V/9\mu A=7.2K$
 choose $R_{cs}=7.32K$
 $I_{ocpmax}=(7.32K*11\mu A)/0.0045+1.03A=19A$
 $I_{ocpmin}=(7.32K*9\mu A)/(0.0056*1.3)+1.03A=10A$
 $I_{ocp}=10A-19A$



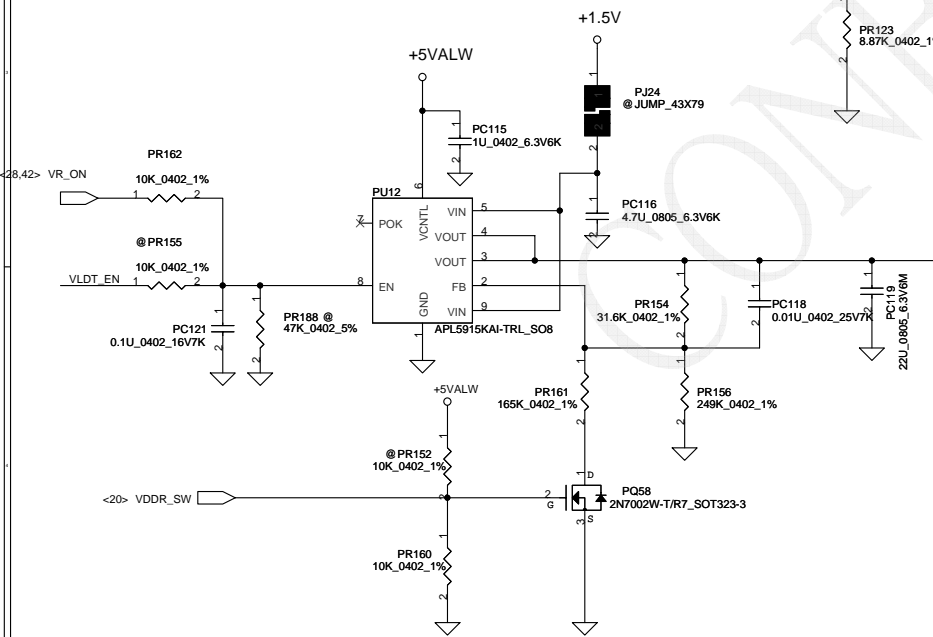
$<V_o=1.5V>$ $V_{FB}=0.75V$
 $V_o=0.75*(1+10K/10K)=1.5V$
 $F_{sw}=335KHz$
 $C_{out} ESR=17\ m\Omega$ $R_{dson(max)}=18\ m\Omega$ $R_{dson(typ)}=15\ m\Omega$
 $I_{peak}=7A$ $I_{max}=8.4A$ $I_{ocp}=13.2A$
 $\Delta I=((19-1.5)*(1.5/19))/(L*F_{sw})=3.9A$
 $\Rightarrow 1/2\Delta I=1.95A$
 $V_{tripmax}=I_{ocp}*R_{dson}=16.2*5.6*1.3=0.118V$
 $R_{cs}=V_{trip}/9\mu A=0.118V/9\mu A=13.1K$
 choose $R_{cs}=13K$
 $I_{ocpmax}=(13K*11\mu A)/0.0045+1.95A=32A$
 $I_{ocpmin}=(13K*9\mu A)/(0.0056*1.3)+1.95A=18A$
 $I_{ocp}=9.94A-13.2A$

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				1.1VALWP/1.5VP
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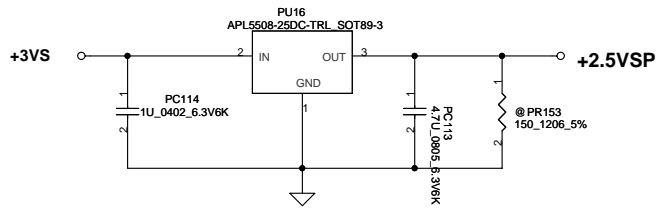


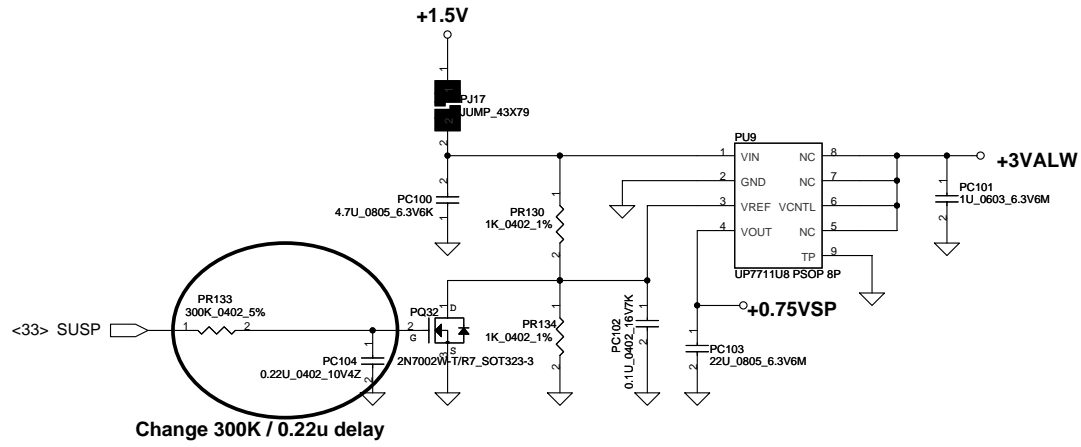
$\langle V_o=1.1V \rangle$ $V_{FB}=0.75V$
 $V=0.75 * (1+4.7K/10K)=1.1V$
 $F_{sw}=280KHz$
 $C_{out} ESR=15m\ ohm$ $R_{dson(max)}=18m$ $R_{dson(typ)}=15m$
 $I_{peak}=7.6A$, $I_{max}=5.4A$, $I_{ocp}=9.2A$
 $\Delta I = ((19-1.1) * (1.1/19)) / (L * F_{sw}) = 2.06A$
 $\Rightarrow 1/2 \Delta I$ $I=1.03A$
 $V_{tripmax} = I_{ocp} * R_{dson} = 9.2 * 5.6 * 1.3 = 0.067V$
 $R_{cs} = V_{trip} / 9\mu A = 0.067V / 9\mu A = 7.44K$
 choose $R_{cs}=7.5K$
 $I_{ocpmax} = ((7.5K * 11\mu A) / 0.0045) + 1.03A = 19.36A$
 $I_{ocpmin} = ((7.5K * 9\mu A) / (0.018 * 1.3)) + 1.03A = 10.3A$
 $I_{ocp}=10.3A-19.36A$

POWER_SEL	
HIGH	0.95V
LOW	1.1V

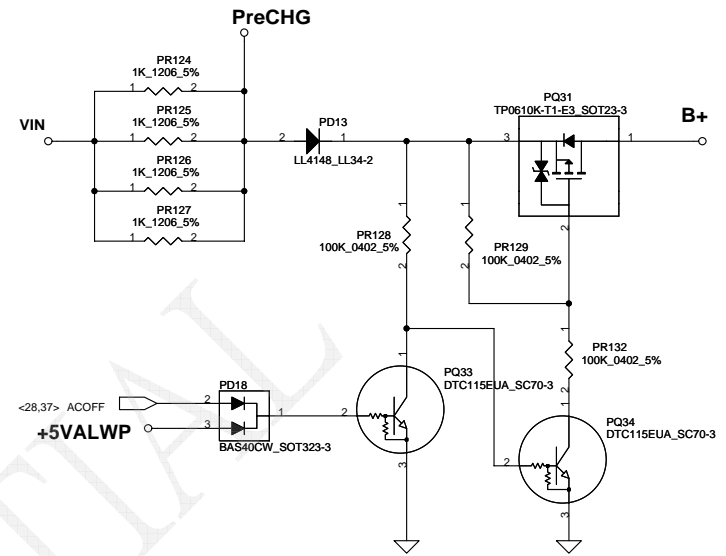


VDDR_SW	
HIGH	1.05V
LOW	0.9V

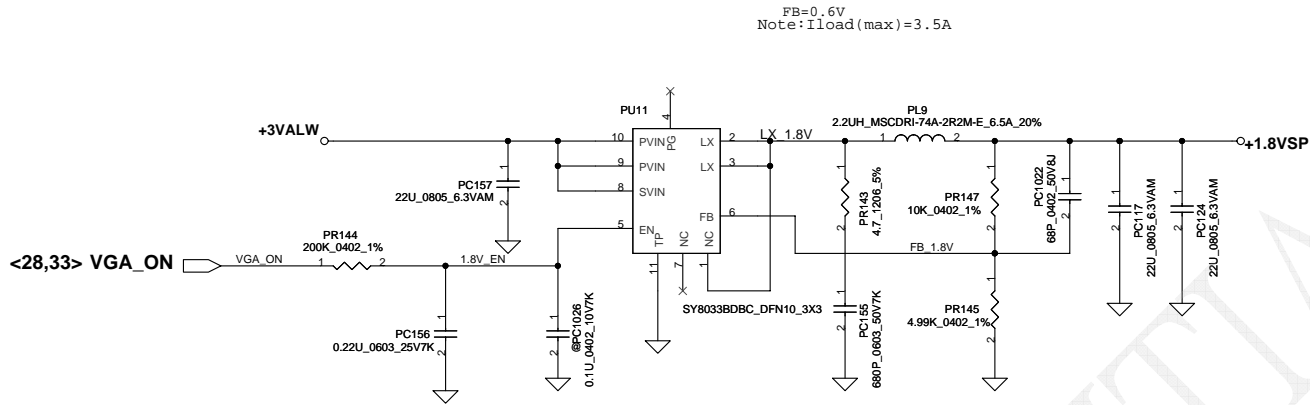




I_{peak}=1A, I_{max}=0.7A

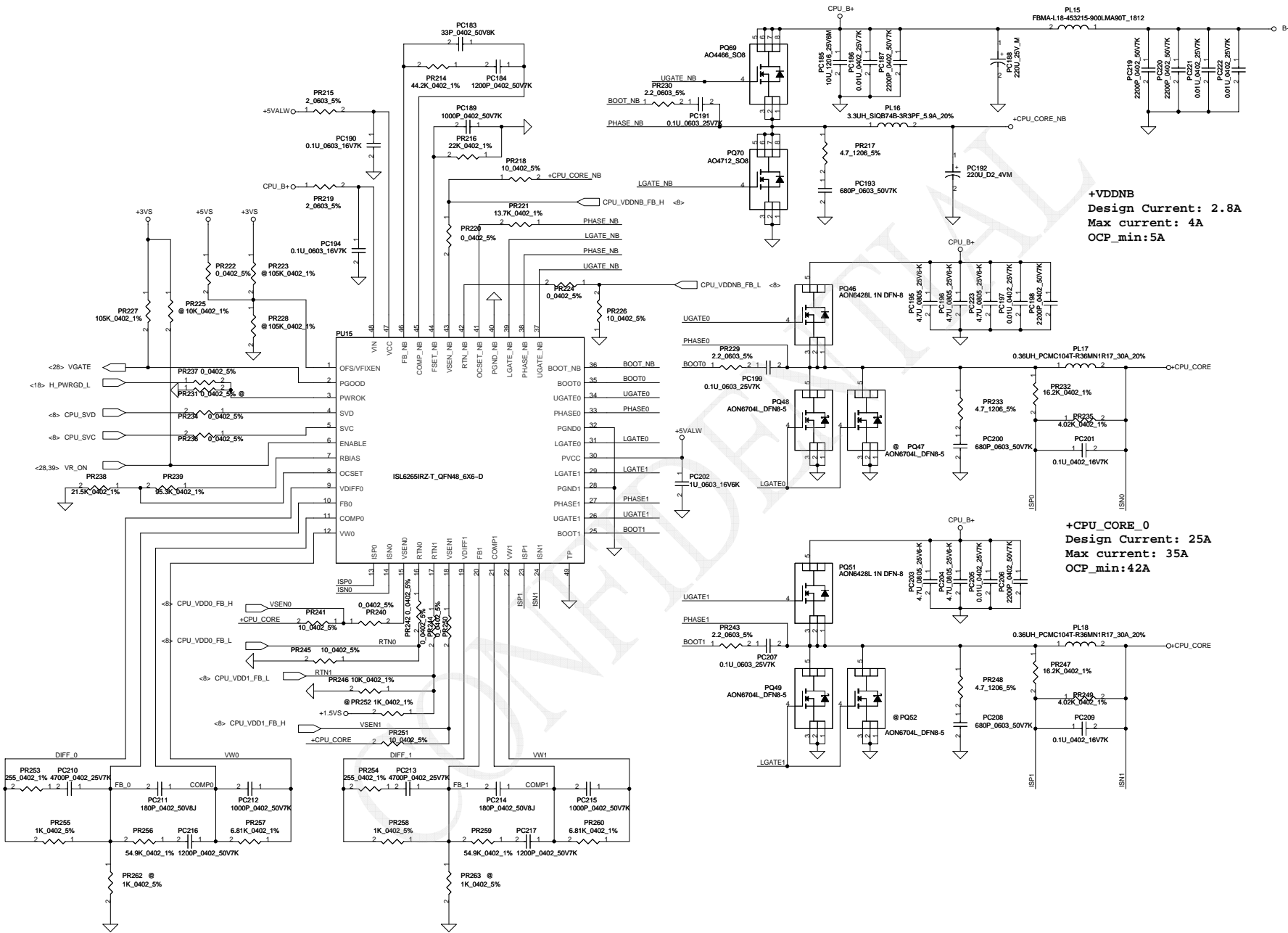


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+VDDNB
 Design Current: 2.8A
 Max current: 4A
 OCP_min:5A

+CPU_CORE_0
 Design Current: 25A
 Max current: 35A
 OCP_min:42A

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Title			+CPU_CORE			
Sheet			Document Number			
			NAV71			
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify Pre-charger				Add PR279,PR288,PC57 Change PR285 100K to 47K Change PR287 20K to 14.3K Change PQ67 2N7002 to PDTC115 Change PR62 47K to 200K Change PR79 22K to 47K Change PR283 0 to 100K	2010 0528	PVT
2	Meet common rule				Change PJ30 to PL36, PJ23 to PL37 Add PC361,PC362	2010 0602	PVT
3	HDMI test fail	5V voltage too low at test termial		36	Change PR265 from 30K to 30.9K	2010 0604	PVT
4	ESD test fail	ESD solution			Add PC22, PC23	2010 0608	PVT
5	EMI test fail	EMI solution			Enable 3V,5V,1.1V,1.5V,NB_CORE,CPU snubber	2010 0608	PVT
6	Power sequence tune			41	Change PR144 from 22K to 200K Change PC156 from 0.47u to 0.22u	2010 0609	PVT
7	Costdown	Costdown		38	Change PQ28 from AO4456 to AO4712 Change PR112 from 13K to 18.2K Change PL7 from 1.0uH to 1.8uH Change PQ61 from AO4712 to AO4468 PR268 from 133K to 137K PQ57 from AO4466 to AO4468	2010 0617	PVT
9	For DDR voltage default/HW YC	DDR 2 need 0.9V, DDR 3 need 1.05V But DDR2 voltage is critical then DDR 3		39	Disable PR152 Enable PR160	2010 0705	Pre MP
10	Aprove 200MHz~220MHz/EMI Chris	EMI solution		37	Enable PR80, PC128 Change PR82 from 0 to 2.2	2010 0705	Pre MP
11	Add a bypass path/ESD Chris	ESD solution		35	Add PC26 near PC22	2010 0705	Pre MP
12							
13							
14							
15							
16							

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
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05/10 First release

1. Change Cardreader chip (RTS5137/RTS5138)
2. ODD used to ODD sub/b
3. RTC Battery change (w/o charge)

06/11 PVT

1. P.28 Reserve R889 For EC_CLK, pop R851, unpop R852 For EC_SMBus leakage
2. P.26 Remove R853
3. P.28 project ID-->1 Board ID -->1, unstuff KSI, KSO Cap.
4. P.8 Change R41 as 31.6k ohm and R42 as 30k ohm for TSI

07/05 Pre-MP

1. P.19 Reserve R890 For MEM_1V5
2. P.28 Change R419 as 10 ohm For EMI

07/20

1. P.29 Change R477, R499 as 750 ohm; change R478 as 3.01k ohm; change R498 as 3.3k ohm for LED light

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