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# Compal Confidential

## HBL50 Schematics Document

Intel Yonah Processor with 945GM/945PM + DDRII + ICH7M  
(With nVIDIA G73M/72MV)

2005-11-08

REV: 0.3

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				Date:	Friday, November 11, 2005	Sheet 1 of 59

# Compal Confidential

Model Name : HBL50  
File Name : LA-2921

Fan Control  
page 47

Yonah  
uPGA-478 Package  
page 4,5

Thermal Sensor  
F75383M  
page 4

Clock Generator  
ICS9LPRS325  
page 14

DVI-D Conn.  
page 25

LCD Conn.  
page 23

CRT & TV-out  
page 24

PSB  
533/667MHz

H\_A#(3..31) H\_D#(0..63)

Intel 945PM/GM  
uFCBGA-1466  
page 6,7,8,9,10,11

Memory BUS(DDRII)  
Dual Channel

200pin DDRII-SO-DIMM X2  
BANK 0, 1, 2, 3  
page 12,13

CH7307C  
page 25

nVidia G73M/(72M)/72MV  
with 64/128/256MB VRAM  
page 15,16,17,18,19,20,21,22

New Card  
Socket page 37

LAN(GbE)  
BCM5789  
page 34

MINI CARD x2  
page 36

USB conn x4  
page 37

Bluetooth  
Conn page 42

Intel ICH7-M  
BGA-652  
page 26,27,28,29

PCI Express

3.3V 48MHz

3.3V 24.576MHz/48MHz

3.3V ATA-100 IDE

S-ATA

HD Audio

CDROM  
Conn. page 31

MDC 1.5  
Conn page 42

HDA Codec  
ALC883  
page 44

IDSEL:AU16  
(PIRQ#1,  
GNT#2,  
REQ#2)

IDSEL:AU18  
(PIRQ#1#,  
GNT#3,  
REQ#3)

IDSEL:AU17  
(PIRQ#3,  
GNT#3,  
REQ#3)

IDSEL:AU20  
(PIRQ#4,  
GNT#2,  
REQ#2)

IEEE 1394  
VT6311S  
page 38

Mini PCI  
socket  
(WLAN)  
(TV-Tuner)  
page 36

LAN (10/100)  
BCM4401E  
page 34

CardBus  
ENE CB714  
page 32

1394 Conn.  
page 38

RJ45  
page 35

Slot 0  
page 33

6 in 1  
socket  
page 33

S-ATA HDD  
Conn. page 30

SATA-to-IDE  
SPIF3811-HV096  
page 30

HDD  
Conn. page 30

Audio AMP  
page 45

Subwoofer  
page 46

RTC CKT.  
page 43

Power On/Off CKT.  
page 43

DC/DC Interface CKT.  
page 48

Power Circuit DC/DC  
page 49,50,51,52  
53,54,55,56

Switch/B Conn.  
USB port4, 6  
page 42

CD-PLAY/B Conn.  
page 42

MEDIA/B Conn.  
page 42

ENE KB910Q  
page 40

Super I/O  
SMsC LPC47N207  
page 39

TPM1.2  
SLB9635 TT 1.2  
page 39

Touch Pad  
page 43

Int.KBD  
page 41

EC I/O Buffer  
page 41

BIOS  
page 41

FIR  
TFDU6102-TR3  
page 39

CIR  
page 42

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Issued Date	2005/06/20	Deciphered Date
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Block Diagrams		
Size B	Document Number	Rev
	HBL50 LA-2921P	0.3
Date:	Friday, November 11, 2005	Sheet 2 of 59

## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

## EC SM Bus2 address

## ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

## SKU ID Table

SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

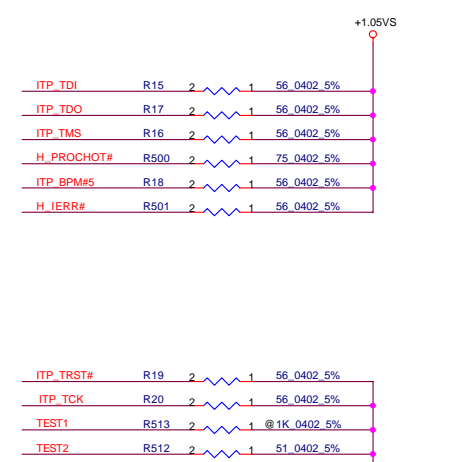
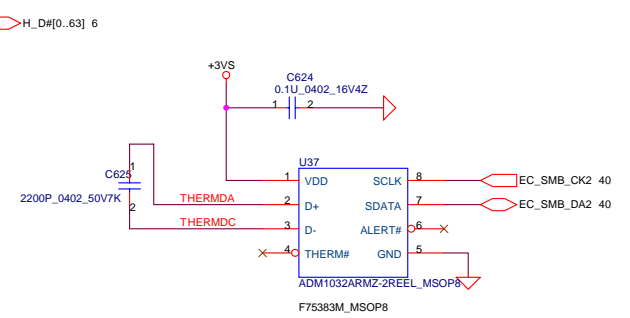
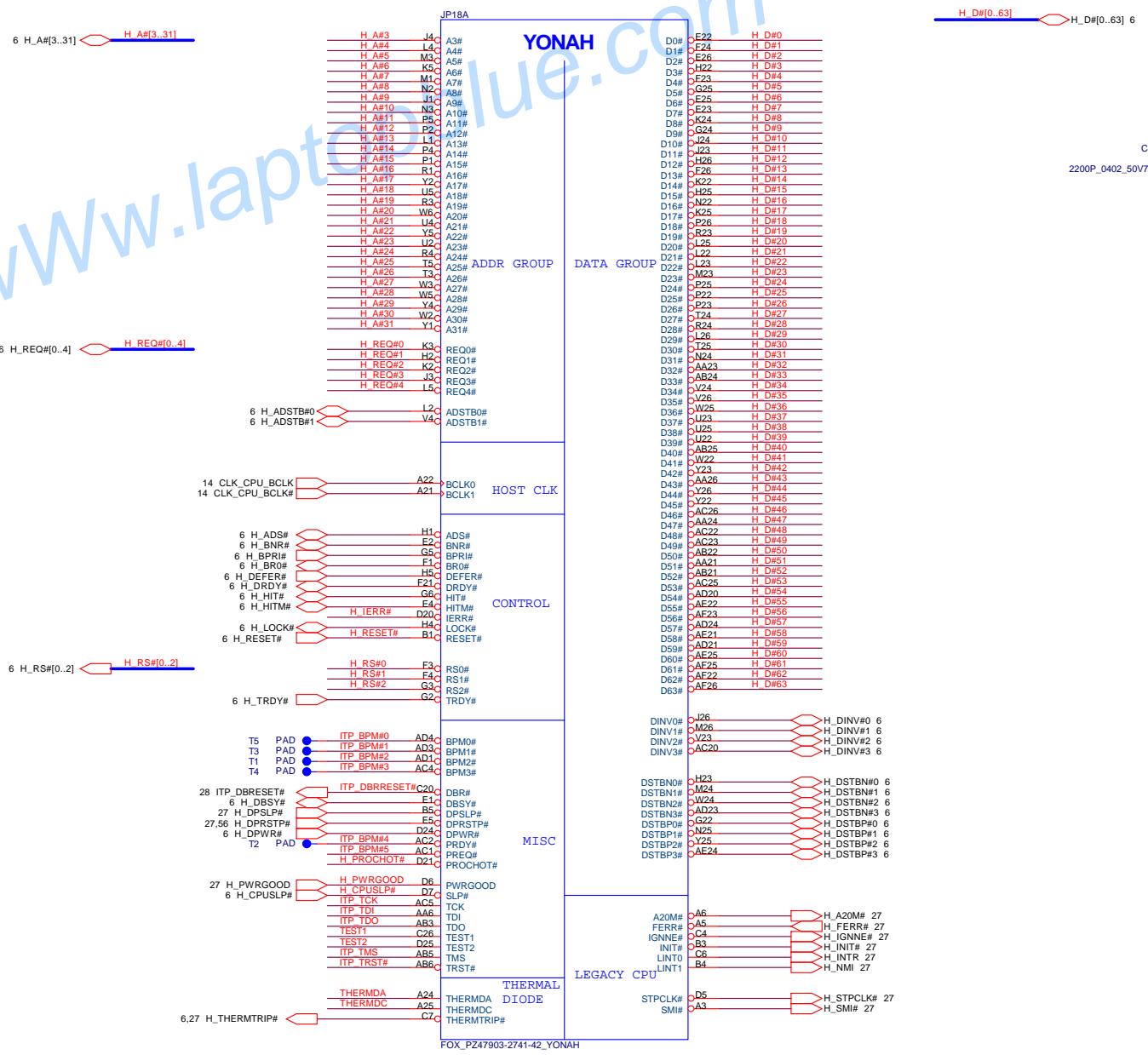
## BTO Option Table

BTO Item	BOM Structure
VGA	PM@ + VGA@
UMA	GM@
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI_CARD1	MINI1@
MINI_CARD2	MINI2@
SATA-to-IDE	3811@
PATA	PATA@
GRAPEVINE	GRA@
G72MV Only	G72@
G73 Only	G73@
VRAM	X76@
VRAM 64M	64@
VRAM 128M	64@+128@
VRAM 256M	64@+128@+256@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
LCM	LCM@
Sub-woofer	SUB@

5789&5787	8789@
4401&5789	0189@
VP1020	VP1020@
INTERNAL MIC	INTMIC@
1394	1394@
SATA HDD	SATA@

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				Rev 0.3 Sheet 3 of 59

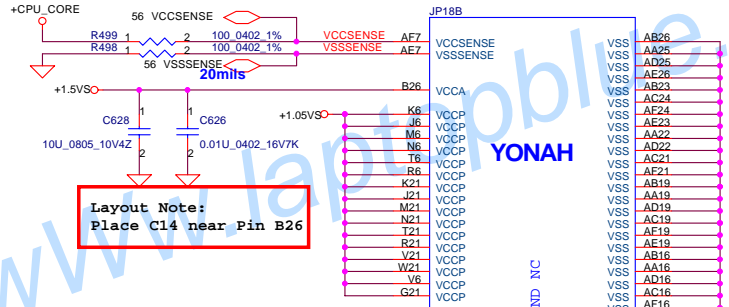
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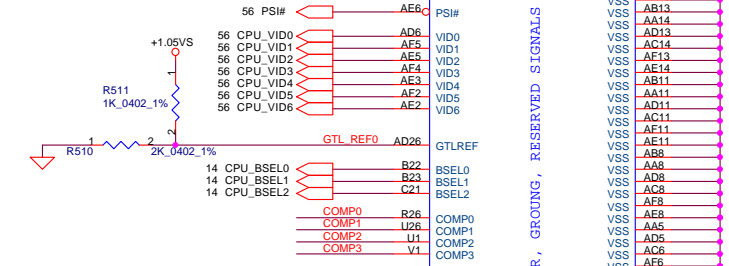
**Layout Note:**  
THERMDA & THERMDC Trace / Space = 10 / 10 mil

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Date:	Friday, November 11, 2005	Sheet	4	of	59

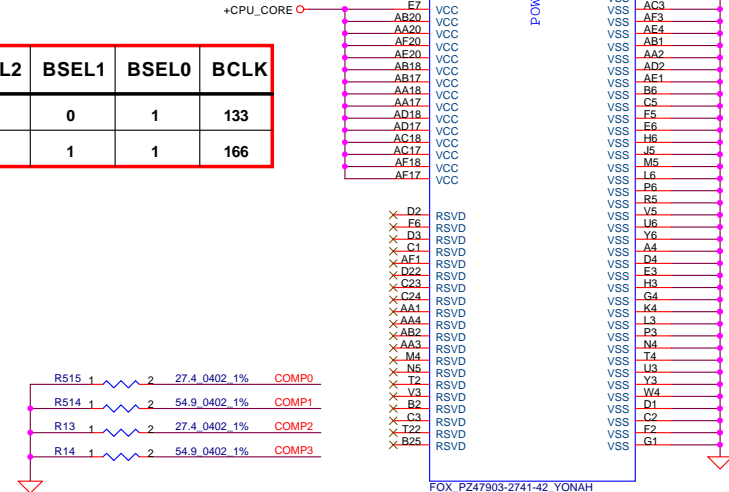
**Layout Note:**  
Route VCCSENSE and VSSSENSE traces at 27.4ohms with 50 mil spacing.  
Place PU and PD within 1 inch of CPU.



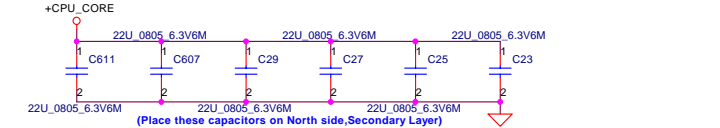
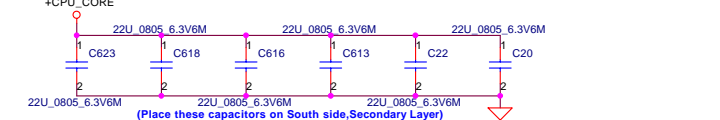
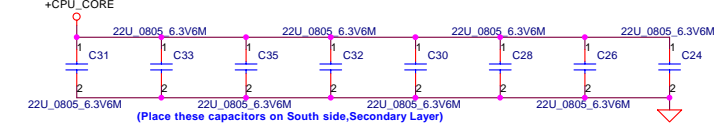
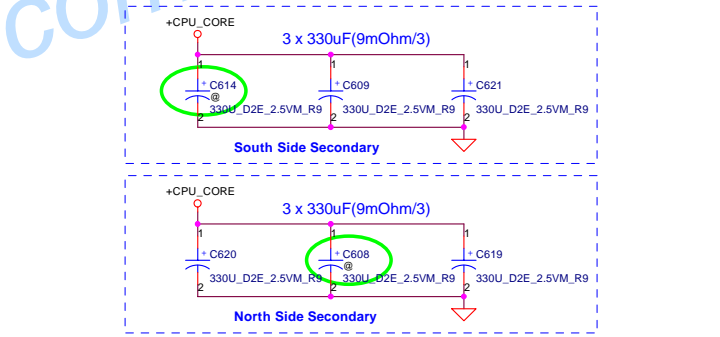
**Layout Note:**  
Place C14 near Pin B26



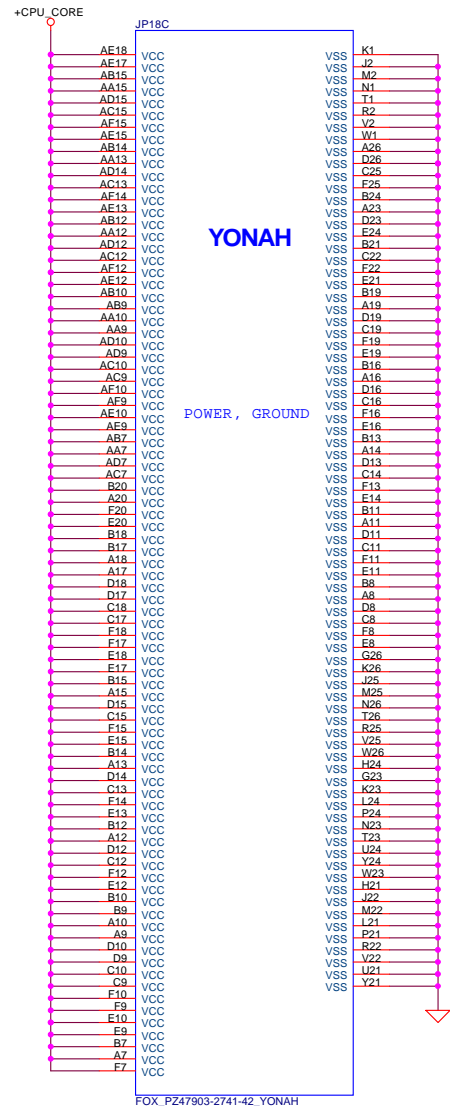
BSEL2	BSEL1	BSEL0	BCLK
0	0	1	133
0	1	1	166



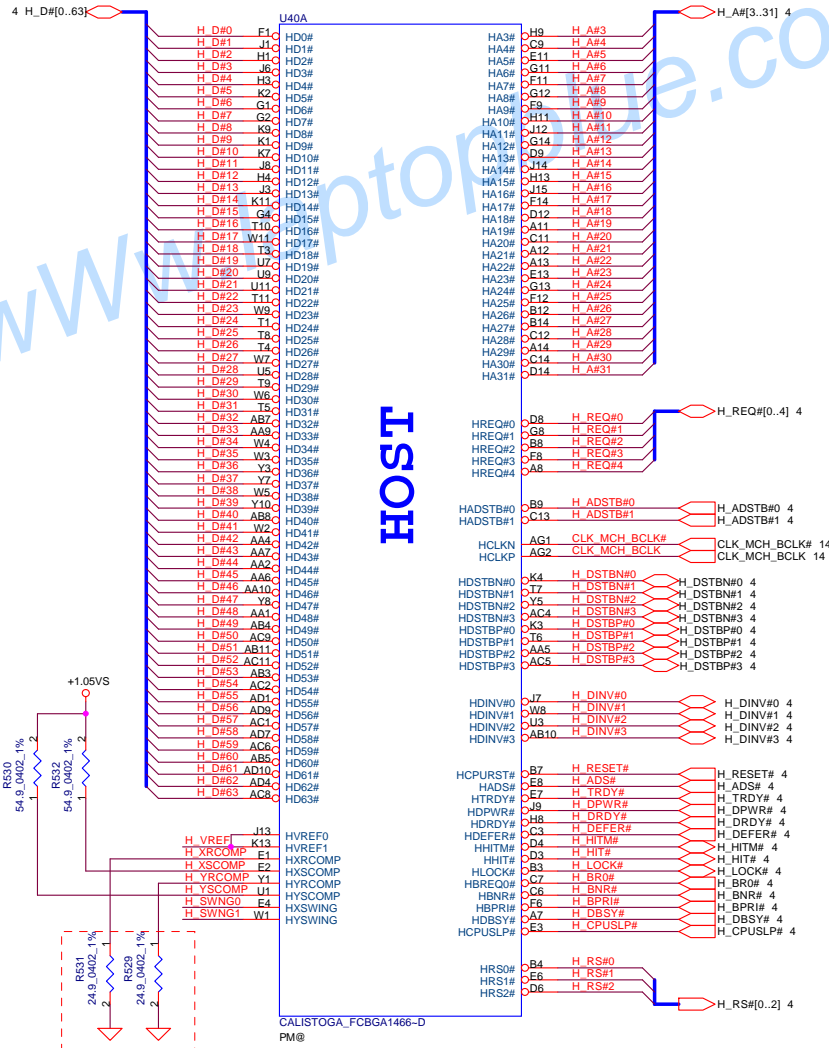
**TRACE CLOSELY CPU < 0.5'**  
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4ohms)  
COMP1, COMP3 layout : Space 25mils (55ohms)



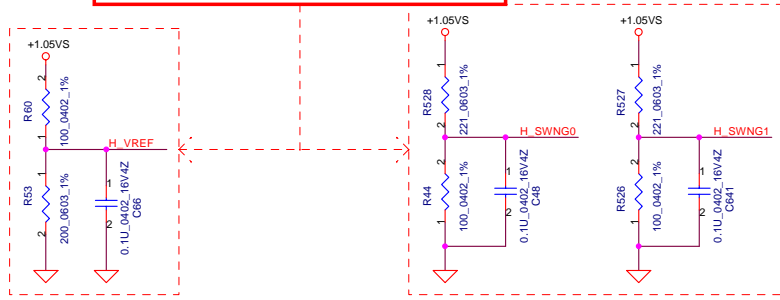
+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32



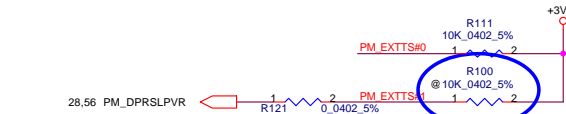
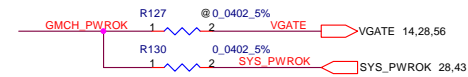
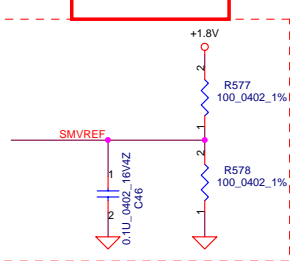
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				Date: Friday, November 11, 2005	Sheet 5 of 59



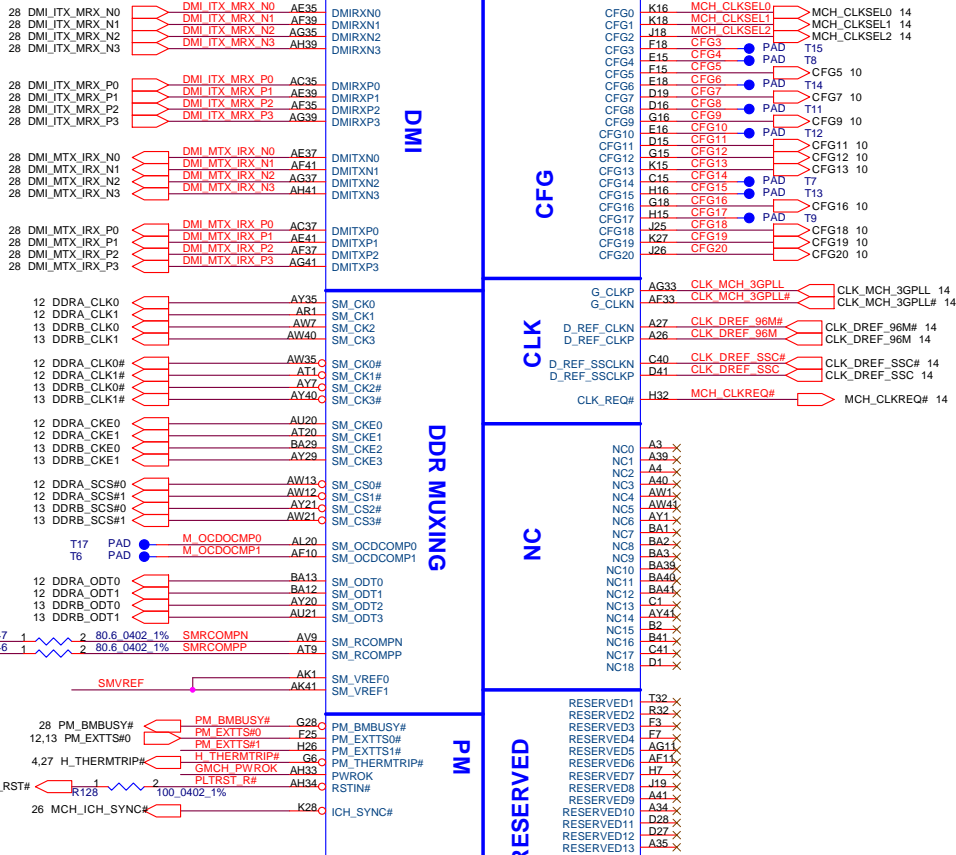
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 H\_SWNG1 trace width and spacing is 10/20.



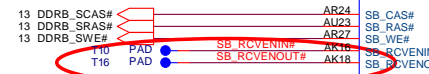
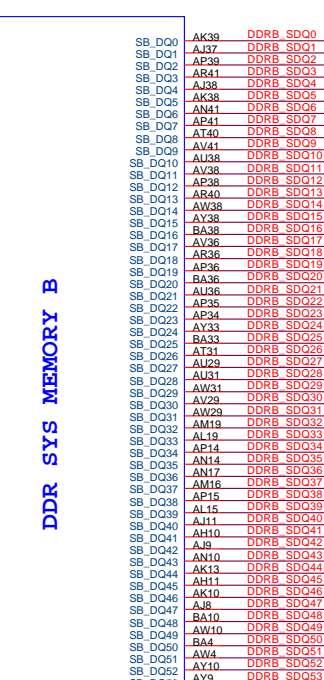
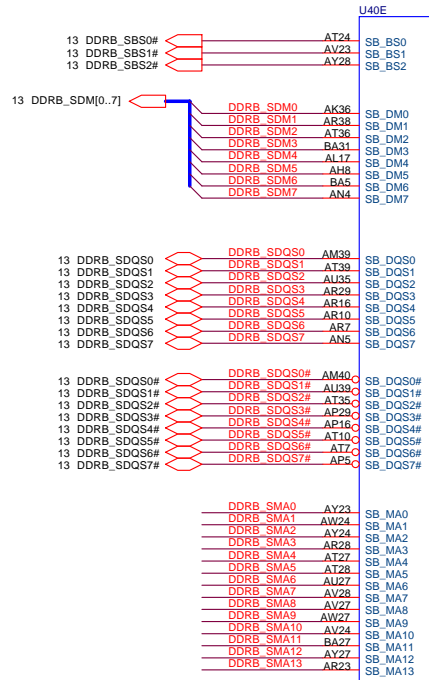
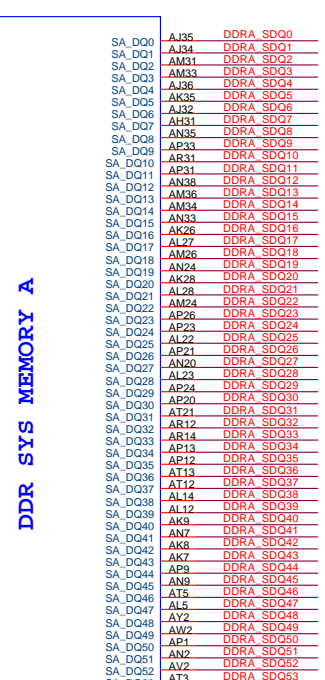
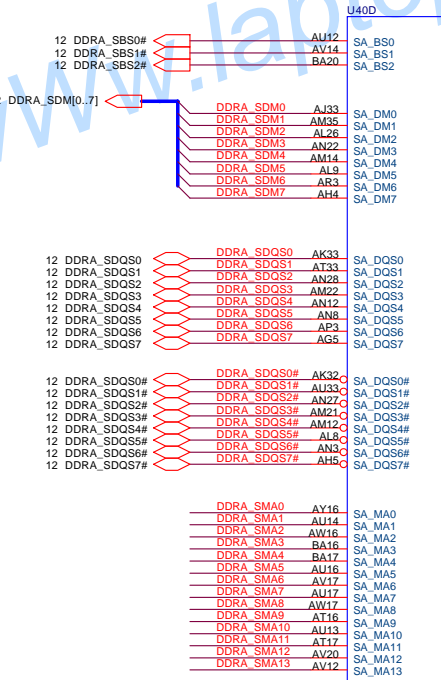
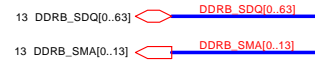
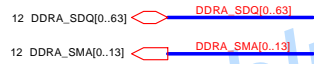
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Description at page10



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Size	Document Number	Rev		
B	HBL50 LA-2921P	0.3		
Date:	Friday, November 11, 2005	Sheet	6	of 59



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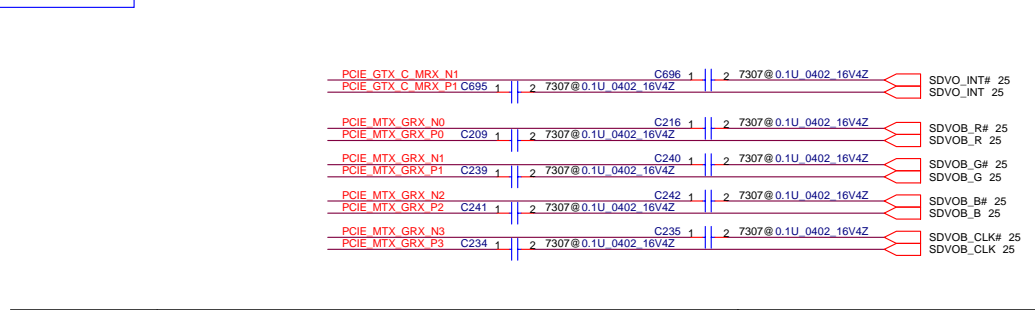
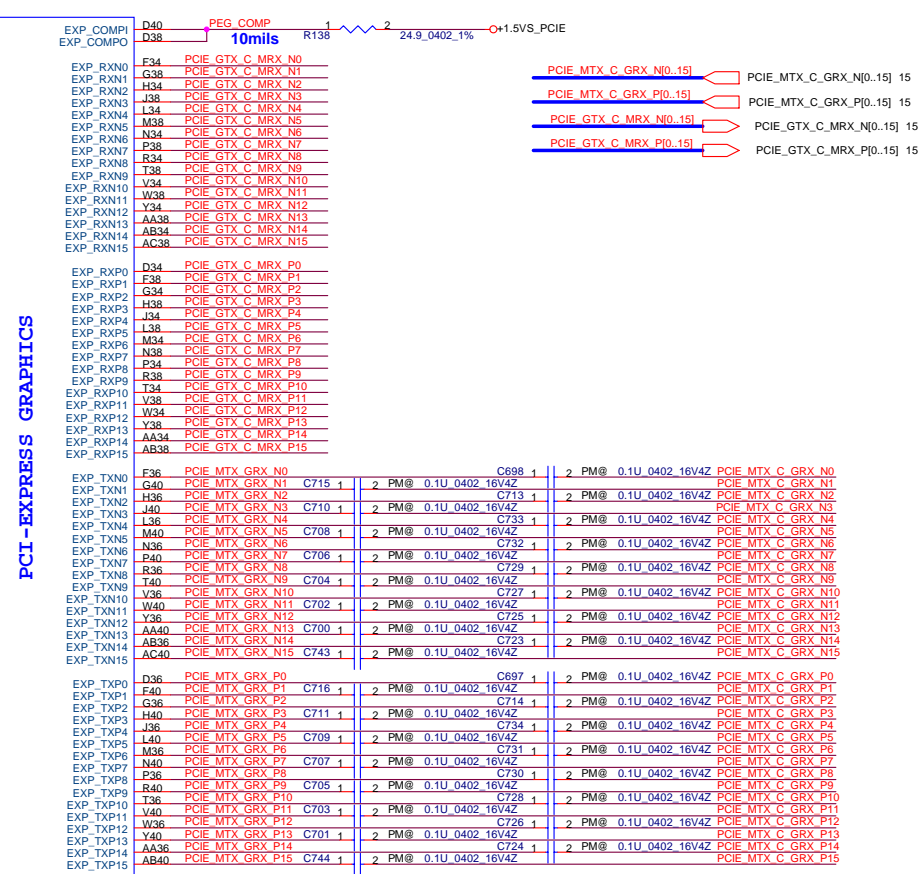
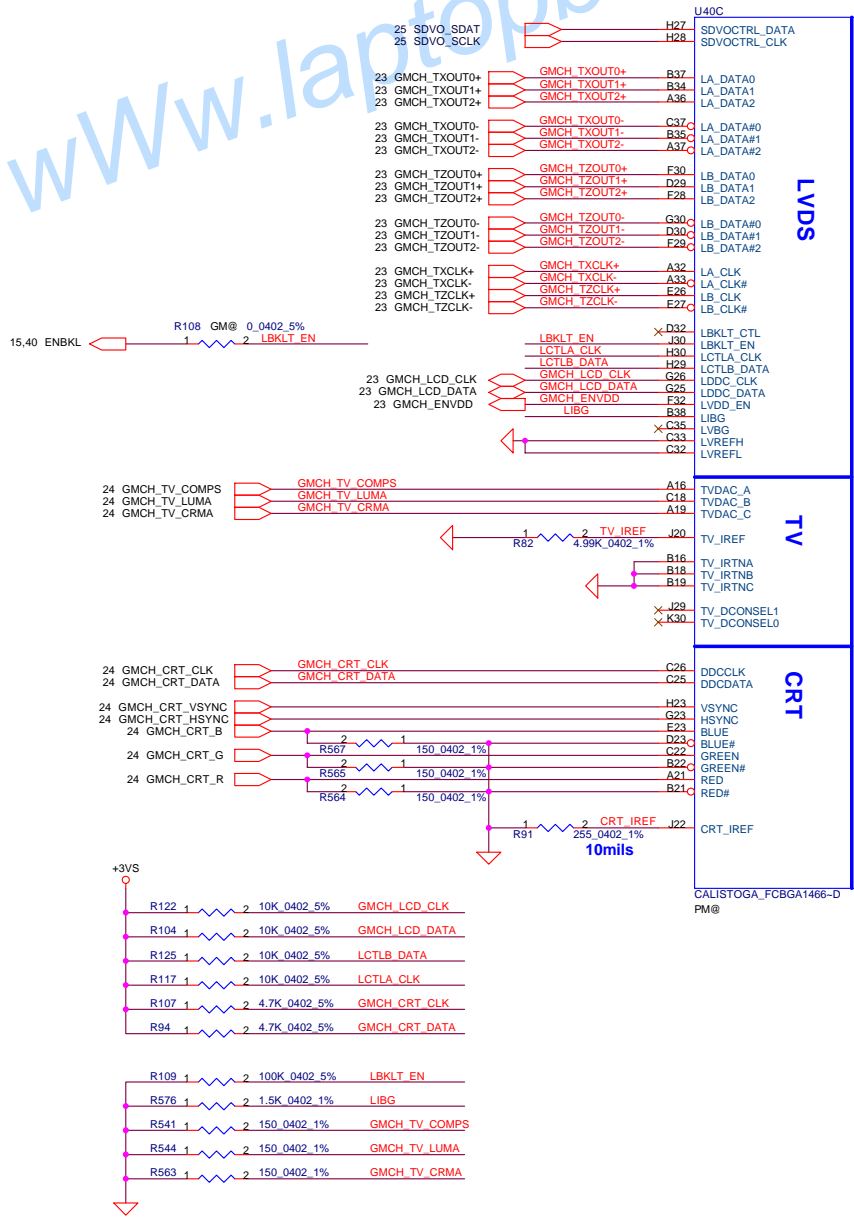
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				Rev 0.3 Sheet 7 of 59

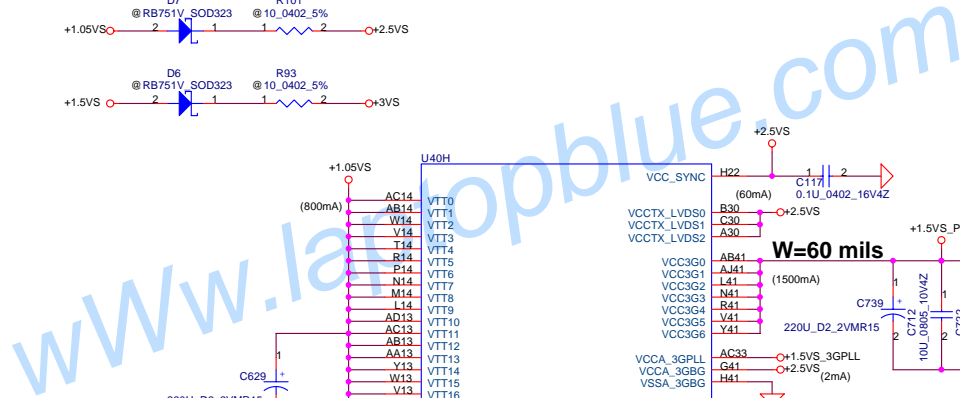
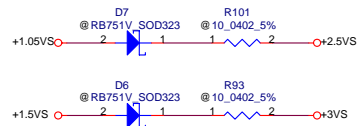


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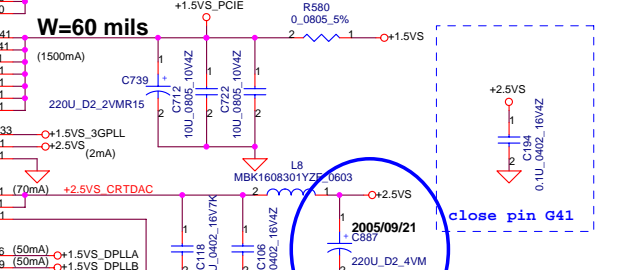


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				Date:	Friday, November 11, 2005
				Sheet	8 of 59
				Rev	0.3
				Calistoga (3/6)	

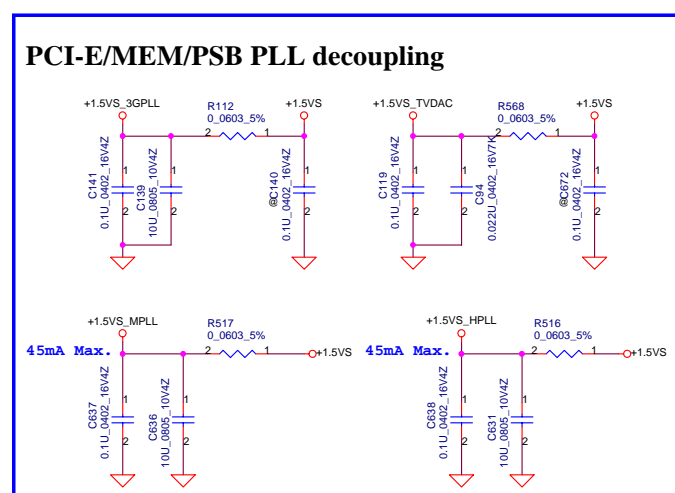
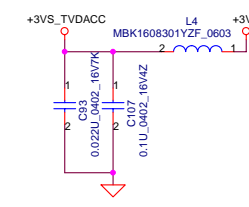
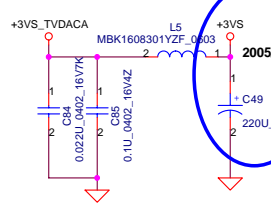
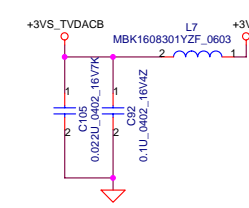
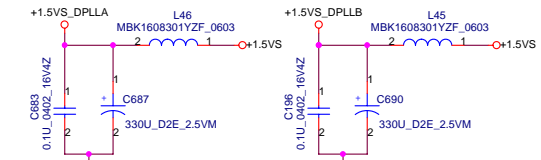
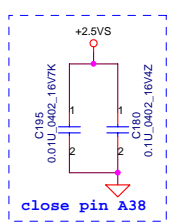




**POWER**



CR/DAC: Route caps within 25mil of Alviso. Route FB within 3" of Calistoga



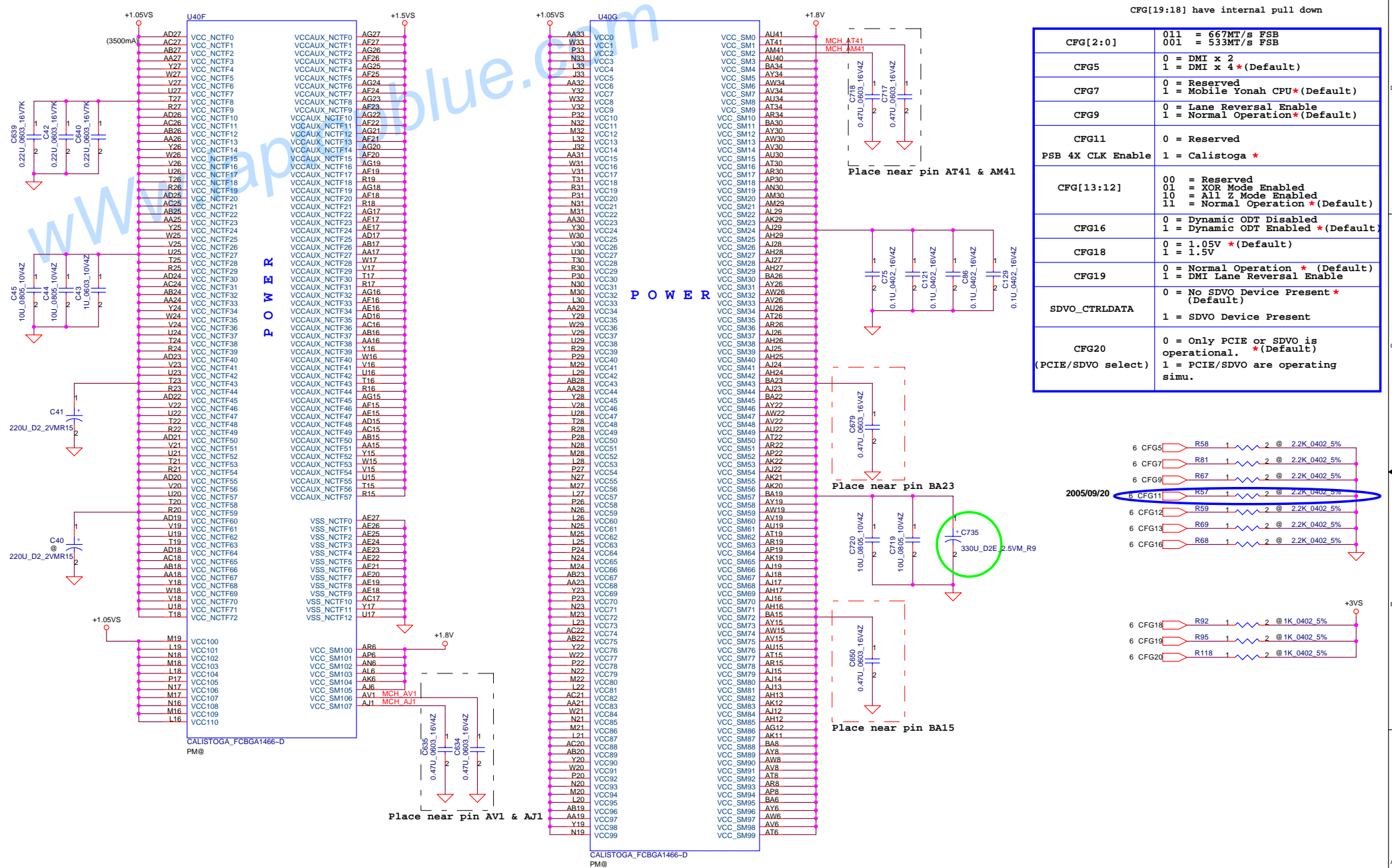
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	HBL50 LA-2921P	Friday, November 11, 2005		0.3
		Sheet 9	of 59	

# Strap Pin Table

CFG[3:17] have internal pull up  
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation*(Default)
CFG11	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



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				Rev 0.3 Sheet 10 of 59

U40I

AC41	VSS0	VSS100	AE34
AA41	VSS01	VSS101	AC34
W41	VSS2	VSS102	C34
P41	VSS3	VSS103	AW33
M41	VSS04	VSS104	AV33
VSS05	VSS05	VSS105	AR33
J41	VSS6	VSS106	AE33
F41	VSS7	VSS107	AB33
AV40	VSS8	VSS108	Y33
AP40	VSS9	VSS109	V33
AN40	VSS10	VSS110	T33
AK40	VSS11	VSS111	R33
AH40	VSS12	VSS112	M33
AG40	VSS13	VSS113	H33
AF40	VSS14	VSS114	G33
AE40	VSS15	VSS115	F33
AD40	VSS16	VSS116	D33
AC40	VSS17	VSS117	B33
AY39	VSS18	VSS118	AH32
AW39	VSS19	VSS119	AG32
AV39	VSS20	VSS120	AF32
AR39	VSS21	VSS121	AE32
AN39	VSS22	VSS122	AC32
AJ39	VSS23	VSS123	AB32
AC39	VSS24	VSS124	G32
AB39	VSS25	VSS125	D32
AA39	VSS26	VSS126	AY31
Y39	VSS27	VSS127	AV31
W39	VSS28	VSS128	AN31
V39	VSS29	VSS129	AM31
T39	VSS30	VSS130	AG31
R39	VSS31	VSS131	AB31
P39	VSS32	VSS132	Y31
N39	VSS33	VSS133	AE30
M39	VSS34	VSS134	E30
L39	VSS35	VSS135	AT29
J39	VSS36	VSS136	AN29
H39	VSS37	VSS137	AB29
G39	VSS38	VSS138	T29
F39	VSS39	VSS139	N29
D39	VSS40	VSS140	K29
AT38	VSS41	VSS141	G29
AM38	VSS42	VSS142	E29
AH38	VSS43	VSS143	C29
AG38	VSS44	VSS144	B29
AF38	VSS45	VSS145	A29
AE38	VSS46	VSS146	BA28
AC38	VSS47	VSS147	AW28
AK37	VSS48	VSS148	AU28
AH37	VSS49	VSS149	AP28
AG37	VSS50	VSS150	AM28
AA37	VSS51	VSS151	U28
Y37	VSS52	VSS152	AC28
W37	VSS53	VSS153	W28
V37	VSS54	VSS154	J28
T37	VSS55	VSS155	E28
R37	VSS56	VSS156	AP27
P37	VSS57	VSS157	AM27
N37	VSS58	VSS158	AK27
M37	VSS59	VSS159	J27
L37	VSS60	VSS160	G27
J37	VSS61	VSS161	F27
H37	VSS62	VSS162	C27
G37	VSS63	VSS163	B27
F37	VSS64	VSS164	AN26
D37	VSS65	VSS165	M26
AY36	VSS66	VSS166	K26
AW36	VSS67	VSS167	F26
AV36	VSS68	VSS168	D26
AR36	VSS69	VSS169	AK25
AN36	VSS70	VSS170	P25
AH36	VSS71	VSS171	H25
AG36	VSS72	VSS172	E25
AF36	VSS73	VSS173	D25
AE36	VSS74	VSS174	A25
AC36	VSS75	VSS175	BA24
AB36	VSS76	VSS176	AU24
AA36	VSS77	VSS177	AL24
Y35	VSS78	VSS178	AW23
W35	VSS79	VSS179	AT23
V35	VSS80	VSS180	AN23
T35	VSS81	VSS181	AM23
R35	VSS82	VSS182	AH23
P35	VSS83	VSS183	AC23
N35	VSS84	VSS184	W23
M35	VSS85	VSS185	K23
L35	VSS86	VSS186	J23
J35	VSS87	VSS187	F23
H35	VSS88	VSS188	C23
G35	VSS89	VSS189	AA22
F35	VSS90	VSS190	K22
D35	VSS91	VSS191	G22
AY34	VSS92	VSS192	F22
AW34	VSS93	VSS193	E22
AV34	VSS94	VSS194	D22
AR34	VSS95	VSS195	A22
AN34	VSS96	VSS196	BA21
AH34	VSS97	VSS197	AV21
AG34	VSS98	VSS198	AR21
AF34	VSS99	VSS199	

CALISTOGA\_FCBGA1466-D  
PM@

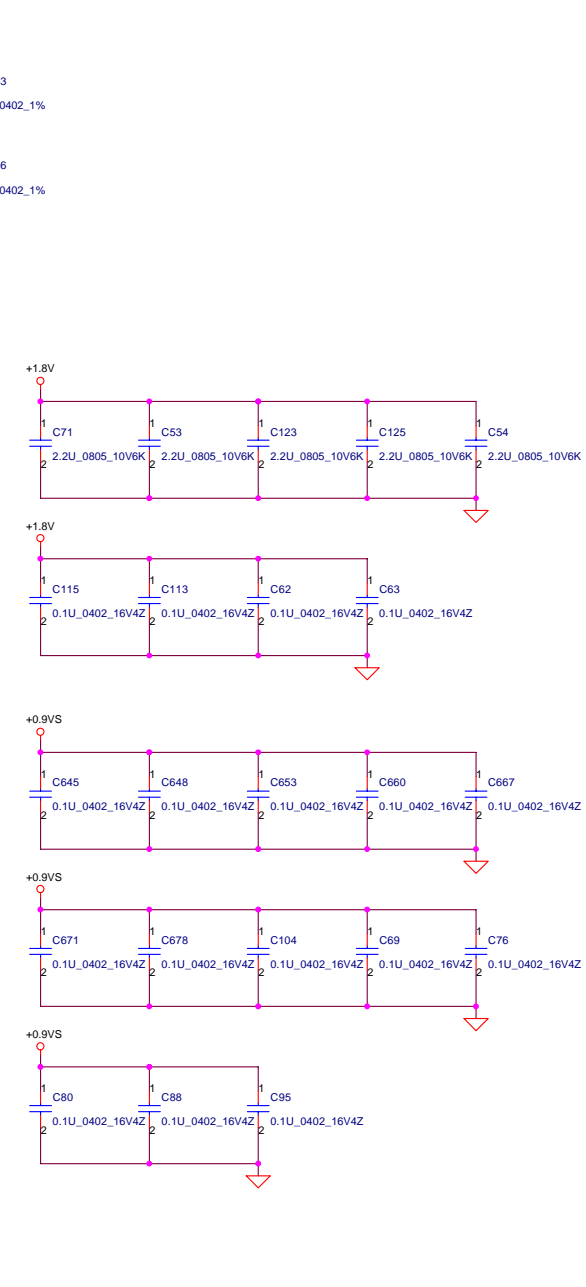
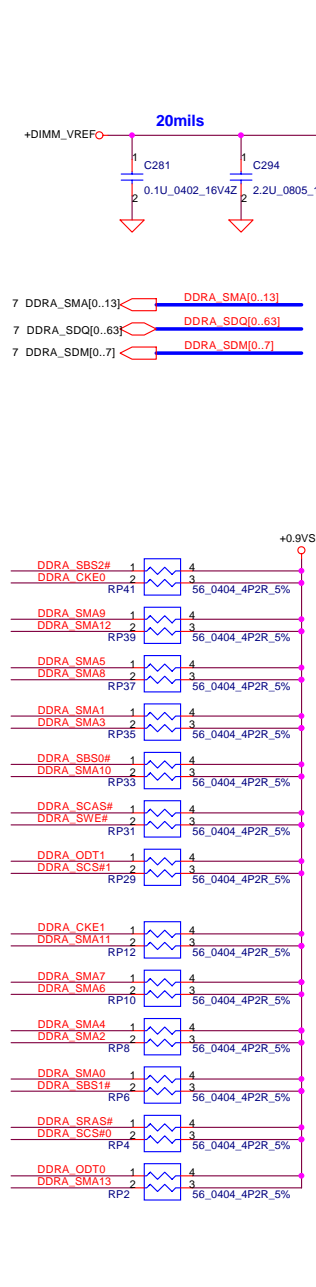
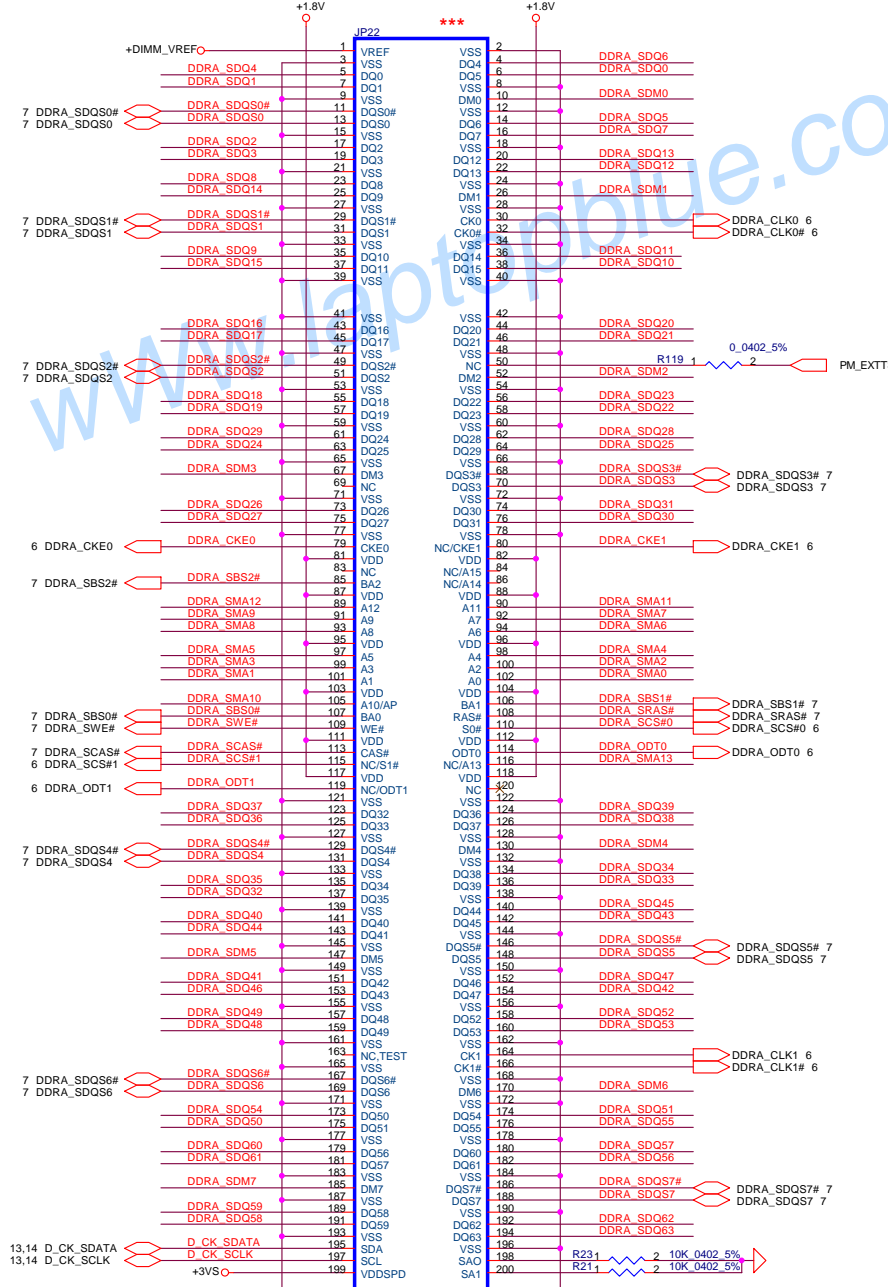
U40J

AN21	VSS200	VSS280	AG10
AL21	VSS201	VSS281	AC10
AB21	VSS202	VSS282	W10
Y21	VSS203	VSS283	U10
AV20	VSS204	VSS284	BA9
K21	VSS205	VSS285	AW9
J21	VSS206	VSS286	AR9
H21	VSS207	VSS287	AH9
G21	VSS208	VSS288	AB9
AW20	VSS209	VSS289	Y9
AR20	VSS210	VSS290	R9
AM20	VSS211	VSS291	G9
AJ20	VSS212	VSS292	E9
K20	VSS213	VSS293	A9
B20	VSS214	VSS294	AG8
A20	VSS215	VSS295	AD8
AN19	VSS216	VSS296	AA8
AC19	VSS217	VSS297	U8
W19	VSS218	VSS298	KA
K19	VSS219	VSS299	CA
G19	VSS220	VSS300	BA7
C19	VSS221	VSS301	AV7
AH18	VSS222	VSS302	AP7
P18	VSS223	VSS303	AL7
H18	VSS224	VSS304	AJ7
D18	VSS225	VSS305	AH7
A18	VSS226	VSS306	AE7
AY17	VSS227	VSS307	AC7
AR17	VSS228	VSS308	R7
AJ17	VSS229	VSS309	C7
AM17	VSS230	VSS310	D7
AK17	VSS231	VSS311	AG6
AV16	VSS232	VSS312	AD6
AM16	VSS233	VSS313	AB6
J16	VSS234	VSS314	Y6
F16	VSS235	VSS315	U6
C16	VSS236	VSS316	N6
T29	VSS237	VSS317	KA
AM15	VSS238	VSS318	BA
AK15	VSS239	VSS319	B6
N15	VSS240	VSS320	AV5
M15	VSS241	VSS321	AE5
L15	VSS242	VSS322	AD5
B15	VSS243	VSS323	AY4
A15	VSS244	VSS324	AR4
BA29	VSS245	VSS325	AP4
AT14	VSS246	VSS326	AL4
AK14	VSS247	VSS327	Y4
AD14	VSS248	VSS328	U4
AM28	VSS249	VSS329	R4
U14	VSS250	VSS330	J4
K14	VSS251	VSS331	F4
H14	VSS252	VSS332	C4
E14	VSS253	VSS333	AY3
AV13	VSS254	VSS334	AW3
AR13	VSS255	VSS335	AV3
AM13	VSS256	VSS336	AG3
AL13	VSS257	VSS337	AL3
AG13	VSS258	VSS338	AH3
P13	VSS259	VSS339	AG3
F13	VSS260	VSS340	AF3
D13	VSS261	VSS341	AD3
B13	VSS262	VSS342	AC3
AY12	VSS263	VSS343	AA3
AC12	VSS264	VSS344	G3
H12	VSS265	VSS345	AT2
E12	VSS266	VSS346	AR2
AD11	VSS267	VSS347	AP2
AK25	VSS268	VSS348	AK2
Y11	VSS269	VSS349	AJ2
J11	VSS270	VSS350	AD2
D11	VSS271	VSS351	AB2
B11	VSS272	VSS352	Y2
AV10	VSS273	VSS353	U2
AP10	VSS274	VSS354	T2
AL10	VSS275	VSS355	N2
AJ10	VSS276	VSS356	J2
	VSS277	VSS357	H2
	VSS278	VSS358	F2
	VSS279	VSS359	C2
		VSS360	AL1

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POWER

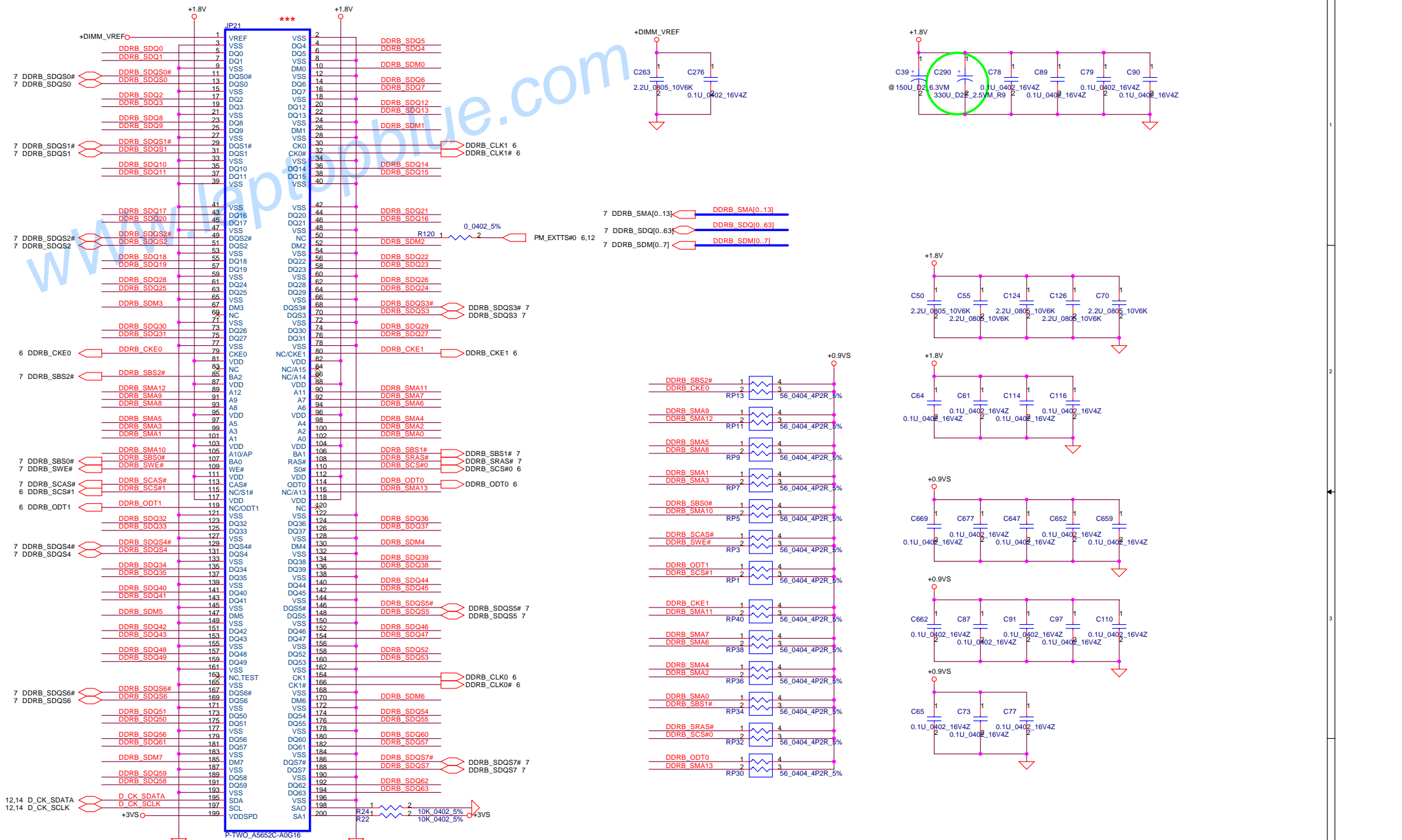
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				Rev 0.3 Sheet 11 of 59



**DIMM0 STD H:9.2mm (BOT)**

Change PCB Footprint

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				Date: Friday, November 11, 2005	Sheet 12 of 59



**DIMM1 STD H:5.2mm (BOT)**

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Date: Friday, November 11, 2005				Sheet 13 of 59

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**DDR II-SODIMM1**

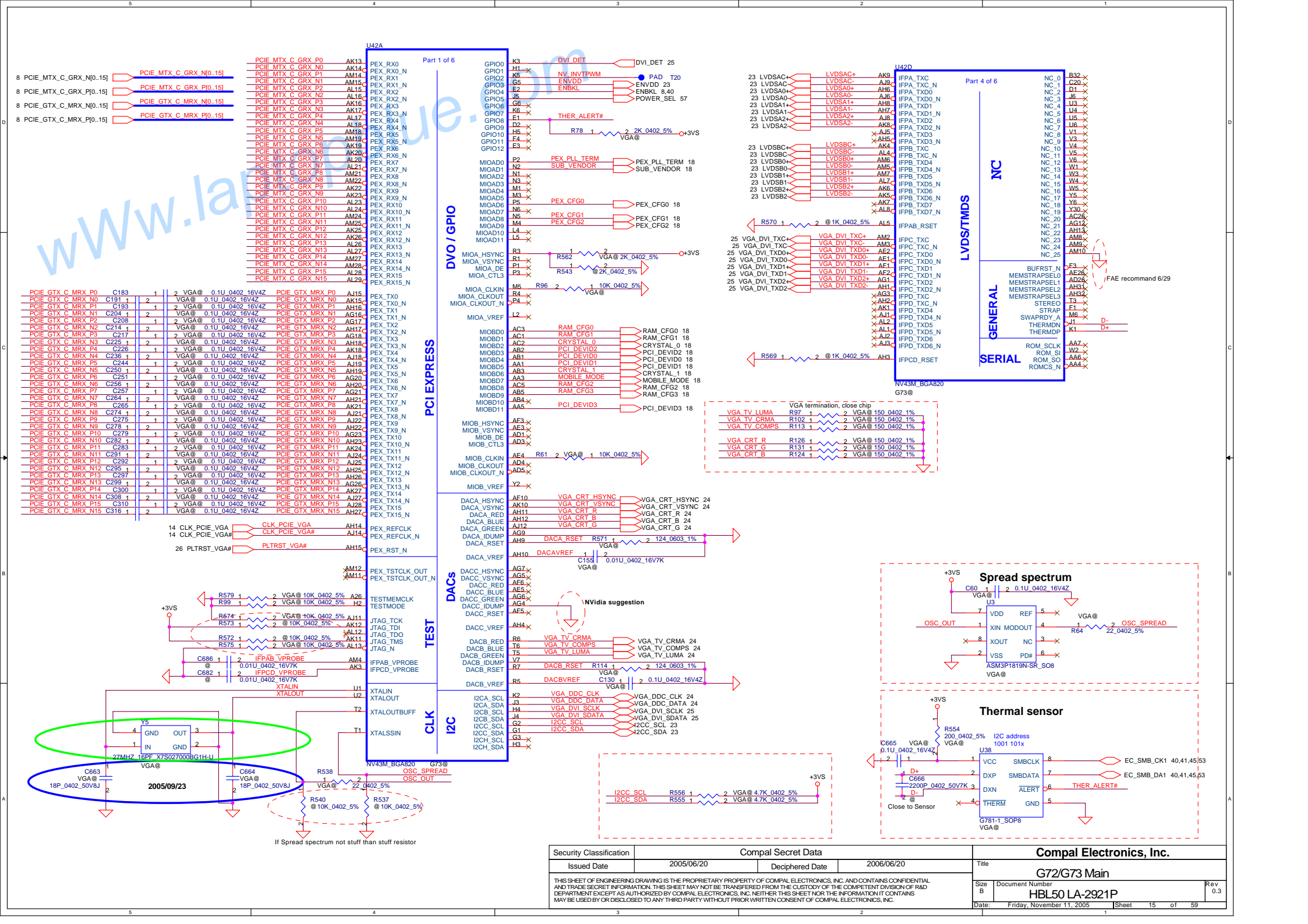
**HBL50 LA-2921P**

Rev 0.3









- 8 PCIE\_MTX\_C\_GRX\_N[0..15] → PCIE\_MTX\_C\_GRX\_N[0..15]
- 8 PCIE\_MTX\_C\_GRX\_P[0..15] → PCIE\_MTX\_C\_GRX\_P[0..15]
- 8 PCIE\_GTX\_C\_MRX\_N[0..15] → PCIE\_GTX\_C\_MRX\_N[0..15]
- 8 PCIE\_GTX\_C\_MRX\_P[0..15] → PCIE\_GTX\_C\_MRX\_P[0..15]

- PCIE GTX C MRX P0 C183 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX P0 AJ15
- PCIE GTX C MRX N0 C191 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX N0 AK15
- PCIE GTX C MRX P1 C193 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX P1 AH16
- PCIE GTX C MRX N1 C204 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX N1 AH16
- PCIE GTX C MRX P2 C208 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX P2 AG17
- PCIE GTX C MRX N2 C214 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX N2 AH17
- PCIE GTX C MRX P3 C217 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX P3 AG18
- PCIE GTX C MRX N3 C225 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX N3 AH18
- PCIE GTX C MRX P4 C226 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX P4 AH18
- PCIE GTX C MRX N4 C236 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX N4 AJ18
- PCIE GTX C MRX P5 C244 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX P5 AJ19
- PCIE GTX C MRX N5 C250 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX N5 AH19
- PCIE GTX C MRX P6 C251 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX P6 AH19
- PCIE GTX C MRX N6 C256 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX N6 AH20
- PCIE GTX C MRX P7 C257 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX P7 AG21
- PCIE GTX C MRX N7 C264 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX N7 AH21
- PCIE GTX C MRX P8 C265 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX P8 AK21
- PCIE GTX C MRX N8 C274 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX N8 AJ21
- PCIE GTX C MRX P9 C275 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX P9 AJ22
- PCIE GTX C MRX N9 C278 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX N9 AH22
- PCIE GTX C MRX P10 C279 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX P10 AK22
- PCIE GTX C MRX N10 C282 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX N10 AH23
- PCIE GTX C MRX P11 C283 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX P11 AK24
- PCIE GTX C MRX N11 C291 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX N11 AJ24
- PCIE GTX C MRX P12 C292 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX P12 AJ25
- PCIE GTX C MRX N12 C295 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX N12 AG26
- PCIE GTX C MRX P13 C297 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX P13 AH26
- PCIE GTX C MRX N13 C299 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX N13 AG26
- PCIE GTX C MRX P14 C300 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX P14 AK27
- PCIE GTX C MRX N14 C308 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX N14 AJ28
- PCIE GTX C MRX P15 C310 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX P15 AJ28
- PCIE GTX C MRX N15 C316 1 2 VGA@ 0.1U 0402 16V4Z PCIE GTX MRX N15 AH27

- 14 CLK\_PCIE\_VGA → CLK\_PCIE\_VGA AH14
- 14 CLK\_PCIE\_VGA# → CLK\_PCIE\_VGA# AH14
- 26 PLTRST\_VGA# → PLTRST\_VGA# AH15

- TESTMEMCLK → TESTMEMCLK AM11
- TESTMODE → TESTMODE AM11
- JTAG\_TCK → JTAG\_TCK AK12
- JTAG\_TDI → JTAG\_TDI AK12
- JTAG\_TDO → JTAG\_TDO AK11
- JTAG\_TMS → JTAG\_TMS AK13
- IFPAB\_VPROBE → IFPAB\_VPROBE AM4
- IFPCD\_VPROBE → IFPCD\_VPROBE AK3

- XTALIN → XTALIN U1
- XTALOUT → XTALIN U2
- XTALOUTBUFF → XTALOUTBUFF T1
- XTALSSIN → XTALSSIN T1

- I2CA\_SCL → I2CA\_SCL K2
- I2CA\_SDA → I2CA\_SDA K3
- I2CB\_SCL → I2CB\_SCL H4
- I2CB\_SDA → I2CB\_SDA J4
- I2CC\_SCL → I2CC\_SCL G2
- I2CC\_SDA → I2CC\_SDA G1
- I2CH\_SCL → I2CH\_SCL G3
- I2CH\_SDA → I2CH\_SDA H3

- DVI\_DET → DVI\_DET K3
- INV\_INTPWM → INV\_INTPWM J1
- ENVDV → ENVDV K5
- ENBK1 → ENBK1 E2
- POWER\_SEL → POWER\_SEL J6
- THER\_ALERT# → THER\_ALERT# G8
- PEX\_PLL\_TERM → PEX\_PLL\_TERM P2
- SUB\_VENDOR → SUB\_VENDOR N1
- PEX\_CFG0 → PEX\_CFG0 N6
- PEX\_CFG1 → PEX\_CFG1 N7
- PEX\_CFG2 → PEX\_CFG2 M4
- MIOA\_HSYNC → MIOA\_HSYNC R3
- MIOA\_VSYNC → MIOA\_VSYNC P1
- MIOA\_CT1N → MIOA\_CT1N P3
- MIOA\_CLKIN → MIOA\_CLKIN J5
- MIOA\_CLKOUT → MIOA\_CLKOUT R4
- MIOA\_CLKOUT\_N → MIOA\_CLKOUT\_N P4
- MIOA\_VREF → MIOA\_VREF L2

- RAM\_CFG0 → RAM\_CFG0 AC3
- RAM\_CFG1 → RAM\_CFG1 AC1
- CRYSTAL\_0 → CRYSTAL\_0 AB2
- PCI\_DEVID2\_0 → PCI\_DEVID2\_0 AB1
- PCI\_DEVID1\_0 → PCI\_DEVID1\_0 AB1
- CRYSTAL\_1 → CRYSTAL\_1 AB3
- MOBILE\_MODE → MOBILE\_MODE AC8
- RAM\_CFG2 → RAM\_CFG2 AB5
- RAM\_CFG3 → RAM\_CFG3 AB5
- PCI\_DEVID3\_0 → PCI\_DEVID3\_0 AB4
- PCI\_DEVID3\_1 → PCI\_DEVID3\_1 AB5
- MIOB\_HSYNC → MIOB\_HSYNC AE3
- MIOB\_VSYNC → MIOB\_VSYNC AE3
- MIOB\_DE → MIOB\_DE AD3
- MIOB\_CT1N → MIOB\_CT1N AD3
- MIOB\_CLKIN → MIOB\_CLKIN AE4
- MIOB\_CLKOUT → MIOB\_CLKOUT AD4
- MIOB\_CLKOUT\_N → MIOB\_CLKOUT\_N AD4
- MIOB\_VREF → MIOB\_VREF Y2

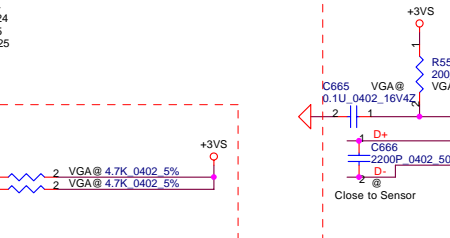
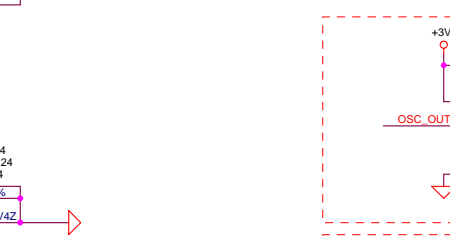
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- VGA CRT\_VSYNC → VGA CRT\_VSYNC AK10
- VGA CRT\_R → VGA CRT\_R AH11
- VGA CRT\_B → VGA CRT\_B AH12
- VGA CRT\_G → VGA CRT\_G AH12
- DACA\_RSET → DACA\_RSET AG9
- DACA\_VREF → DACA\_VREF AH10
- DACC\_HSYNC → DACC\_HSYNC AG7
- DACC\_VSYNC → DACC\_VSYNC AG8
- DACC\_RED → DACC\_RED AE8
- DACC\_BLUE → DACC\_BLUE AE8
- DACC\_IDUMP → DACC\_IDUMP AG4
- DACC\_RSET → DACC\_RSET AE4
- DACB\_RED → DACB\_RED R6
- DACB\_BLUE → DACB\_BLUE R6
- DACB\_GREEN → DACB\_GREEN T5
- DACB\_IDUMP → DACB\_IDUMP V7
- DACB\_RSET → DACB\_RSET R7
- DACB\_VREF → DACB\_VREF R5
- VGA DDC\_CLK → VGA DDC\_CLK K2
- VGA DDC\_DATA → VGA DDC\_DATA J3
- VGA DVI\_SCLK → VGA DVI\_SCLK H4
- VGA DVI\_SDATA → VGA DVI\_SDATA J4
- I2CC\_SCL → I2CC\_SCL G2
- I2CC\_SDA → I2CC\_SDA G1

- OSC\_SPREAD → OSC\_SPREAD R538
- OSC\_OUT → OSC\_OUT R537
- I2CC\_SCL → I2CC\_SCL R556
- I2CC\_SDA → I2CC\_SDA R555

- LVDSAC+ → LVDSAC+ AK9
- LVDSAC- → LVDSAC- AJ9
- LVDSA0+ → LVDSA0+ AH6
- LVDSA0- → LVDSA0- AJ6
- LVDSA1+ → LVDSA1+ AH7
- LVDSA1- → LVDSA1- AJ7
- LVDSA2+ → LVDSA2+ AJ8
- LVDSA2- → LVDSA2- AK8
- LVDSBC+ → LVDSBC+ AL4
- LVDSBC- → LVDSBC- AL4
- LVDSB0+ → LVDSB0+ AM6
- LVDSB0- → LVDSB0- AM7
- LVDSB1+ → LVDSB1+ AL7
- LVDSB1- → LVDSB1- AL7
- LVDSB2+ → LVDSB2+ AK6
- LVDSB2- → LVDSB2- AK5
- VGA DVI\_TXC+ → VGA DVI\_TXC+ AM2
- VGA DVI\_TXC- → VGA DVI\_TXC- AM2
- VGA DVI\_TXD0+ → VGA DVI\_TXD0+ AE2
- VGA DVI\_TXD0- → VGA DVI\_TXD0- AE1
- VGA DVI\_TXD1+ → VGA DVI\_TXD1+ AE1
- VGA DVI\_TXD1- → VGA DVI\_TXD1- AE2
- VGA DVI\_TXD2+ → VGA DVI\_TXD2+ AG1
- VGA DVI\_TXD2- → VGA DVI\_TXD2- AG3
- VGA DVI\_TXD3+ → VGA DVI\_TXD3+ AH2
- VGA DVI\_TXD3- → VGA DVI\_TXD3- AH2
- VGA DVI\_TXD4+ → VGA DVI\_TXD4+ AK1
- VGA DVI\_TXD4- → VGA DVI\_TXD4- AK1
- VGA DVI\_TXD5+ → VGA DVI\_TXD5+ AL1
- VGA DVI\_TXD5- → VGA DVI\_TXD5- AL1
- VGA DVI\_TXD6+ → VGA DVI\_TXD6+ AJ2
- VGA DVI\_TXD6- → VGA DVI\_TXD6- AJ2
- IFPCD\_RSET → IFPCD\_RSET AH3

- VGA TV\_LUMA → VGA TV\_LUMA R97
- VGA TV\_CRMA → VGA TV\_CRMA R102
- VGA TV\_COMPS → VGA TV\_COMPS R113
- VGA CRT\_R → VGA CRT\_R R126
- VGA CRT\_G → VGA CRT\_G R131
- VGA CRT\_B → VGA CRT\_B R124

- DACA\_VREF → DACA\_VREF R571
- DACB\_VREF → DACB\_VREF R5
- VGA@ → VGA@ C130

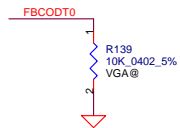
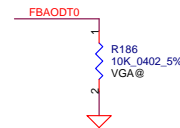
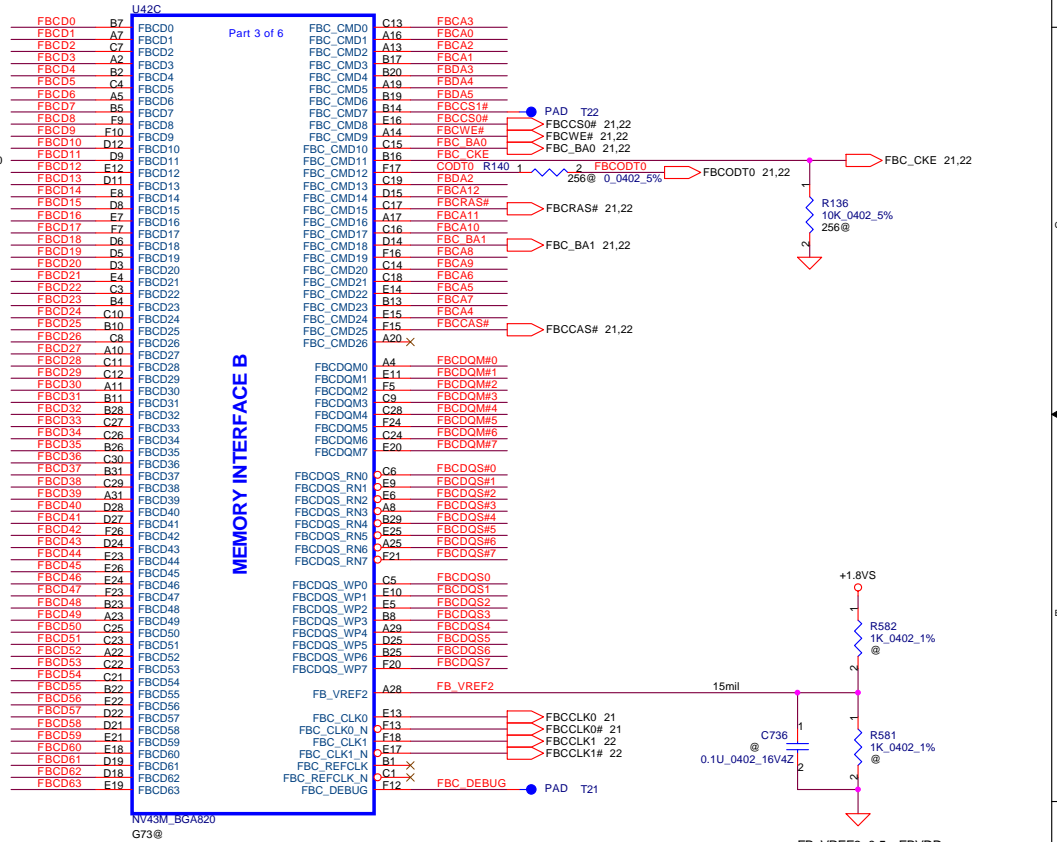
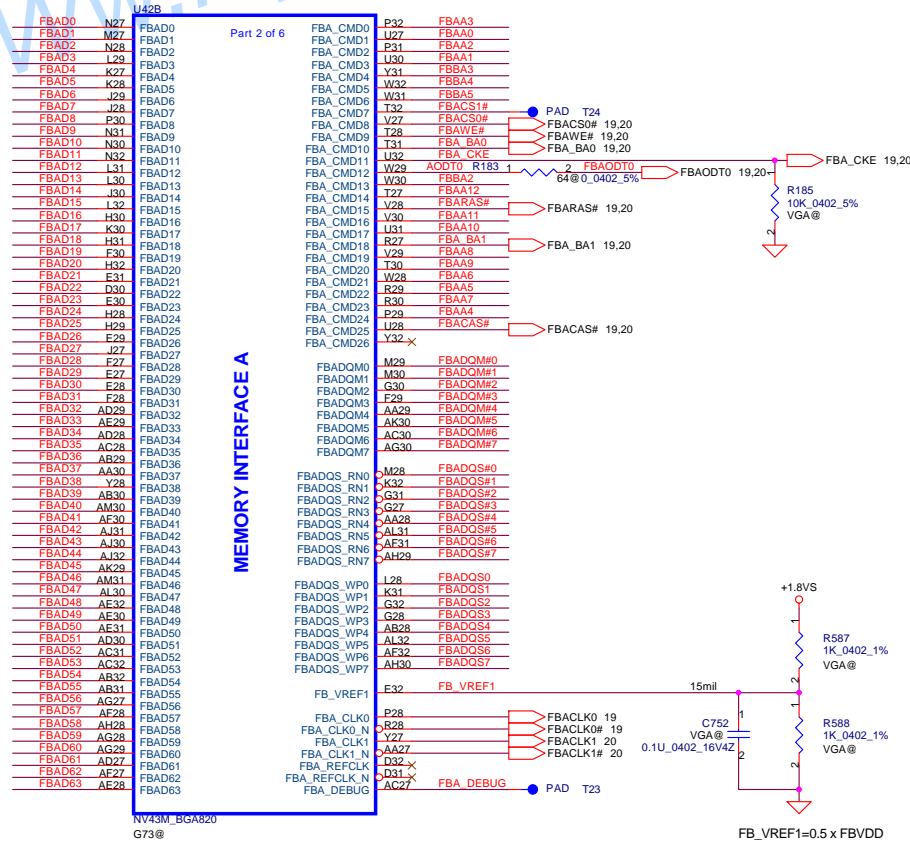
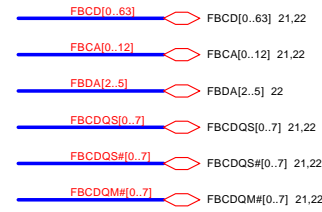
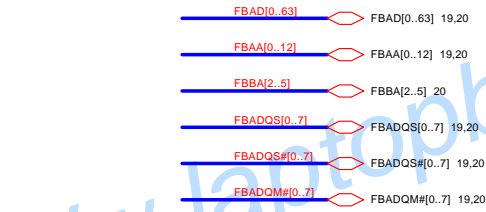


- IFPA\_TXC → IFPA\_TXC NC 0
- IFPA\_TXC\_N → IFPA\_TXC\_N NC 1
- IFPA\_TXD → IFPA\_TXD NC 2
- IFPA\_TXD0\_N → IFPA\_TXD0\_N NC 3
- IFPA\_TXD1 → IFPA\_TXD1 NC 4
- IFPA\_TXD1\_N → IFPA\_TXD1\_N NC 5
- IFPA\_TXD2 → IFPA\_TXD2 NC 6
- IFPA\_TXD2\_N → IFPA\_TXD2\_N NC 7
- IFPA\_TXD3 → IFPA\_TXD3 NC 8
- IFPA\_TXD3\_N → IFPA\_TXD3\_N NC 9
- IFPB\_TXC → IFPB\_TXC NC 10
- IFPB\_TXD → IFPB\_TXD NC 11
- IFPB\_TXD4 → IFPB\_TXD4 NC 12
- IFPB\_TXD4\_N → IFPB\_TXD4\_N NC 13
- IFPB\_TXD5 → IFPB\_TXD5 NC 14
- IFPB\_TXD5\_N → IFPB\_TXD5\_N NC 15
- IFPB\_TXD6 → IFPB\_TXD6 NC 16
- IFPB\_TXD6\_N → IFPB\_TXD6\_N NC 17
- IFPB\_TXD7 → IFPB\_TXD7 NC 18
- IFPB\_TXD7\_N → IFPB\_TXD7\_N NC 19
- IFPAB\_RSET → IFPAB\_RSET NC 20
- IFPC\_TXC → IFPC\_TXC NC 21
- IFPC\_TXC\_N → IFPC\_TXC\_N NC 22
- IFPC\_TXD → IFPC\_TXD NC 23
- IFPC\_TXD0 → IFPC\_TXD0 NC 24
- IFPC\_TXD0\_N → IFPC\_TXD0\_N NC 25
- IFPC\_TXD1 → IFPC\_TXD1 NC 26
- IFPC\_TXD1\_N → IFPC\_TXD1\_N NC 27
- IFPC\_TXD2 → IFPC\_TXD2 NC 28
- IFPC\_TXD2\_N → IFPC\_TXD2\_N NC 29
- IFPC\_TXD3 → IFPC\_TXD3 NC 30
- IFPC\_TXD3\_N → IFPC\_TXD3\_N NC 31
- IFPC\_TXD4 → IFPC\_TXD4 NC 32
- IFPC\_TXD4\_N → IFPC\_TXD4\_N NC 33
- IFPC\_TXD5 → IFPC\_TXD5 NC 34
- IFPC\_TXD5\_N → IFPC\_TXD5\_N NC 35
- IFPC\_TXD6 → IFPC\_TXD6 NC 36
- IFPC\_TXD6\_N → IFPC\_TXD6\_N NC 37
- IFPCD\_RSET → IFPCD\_RSET NC 38

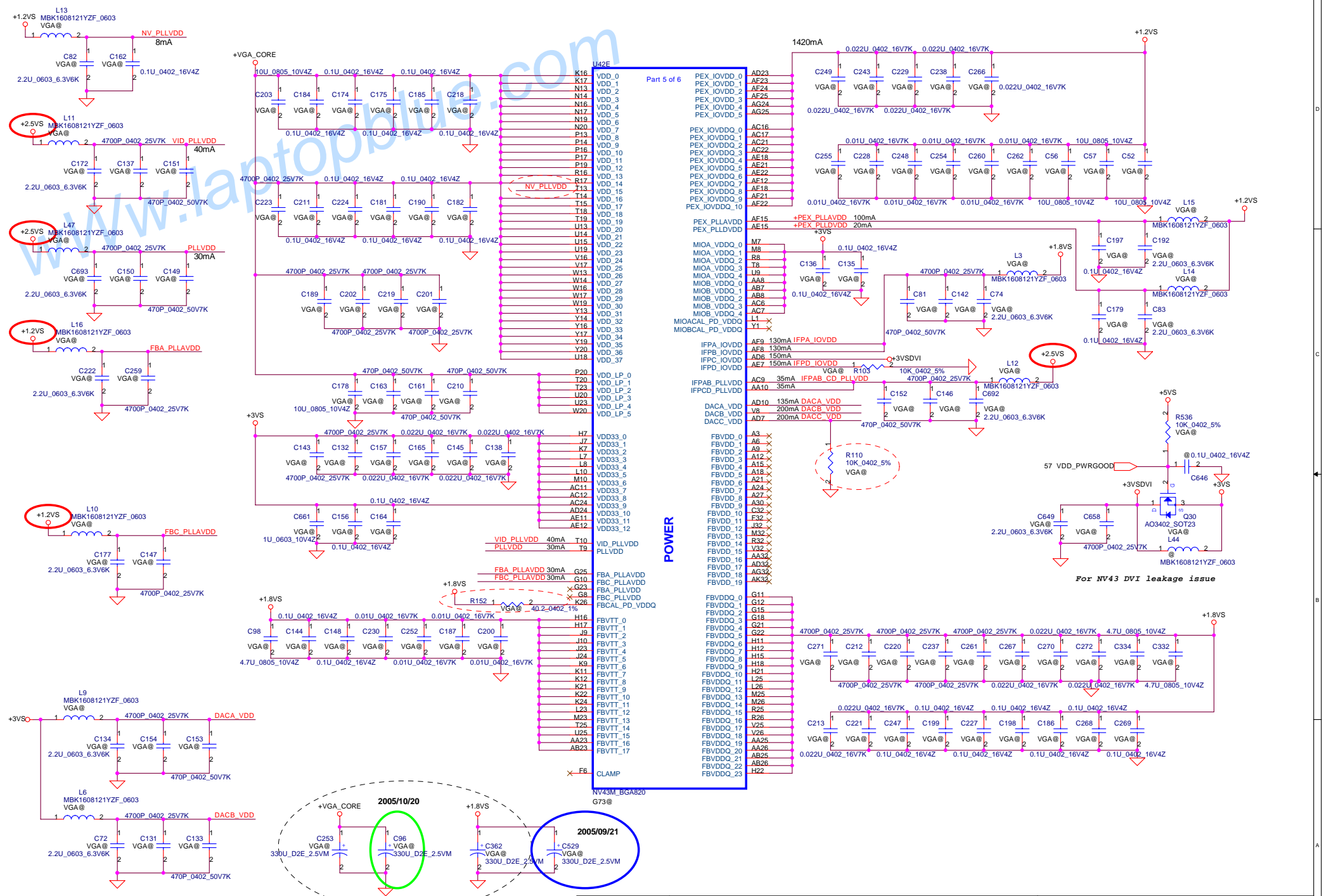
- MEMSTRAPSEL0 → MEMSTRAPSEL0 F3
- MEMSTRAPSEL1 → MEMSTRAPSEL1 AE26
- MEMSTRAPSEL2 → MEMSTRAPSEL2 AD26
- MEMSTRAPSEL3 → MEMSTRAPSEL3 AH32
- STEREO → STEREO F1
- STRAP → STRAP X1
- SWAPRDY → SWAPRDY X1
- THERMDN → THERMDN K1
- THERMUP → THERMUP K1
- ROM\_SI → ROM\_SI AW2
- ROM\_SO → ROM\_SO AW2
- ROM\_CS → ROM\_CS AW6
- ROMCS\_N → ROMCS\_N AW4

- EC\_SMB\_CLK → EC\_SMB\_CLK 40,41,45,53
- EC\_SMB\_DA1 → EC\_SMB\_DA1 40,41,45,53
- THER\_ALERT# → THER\_ALERT#

Security Classification	Compal Secret Data		Title	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	G72/G73 Main
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Size	Document Number	Date:		Rev
B	HBL50 LA-2921P	Friday, November 11, 2005		0.3
			Sheet	15 of 59



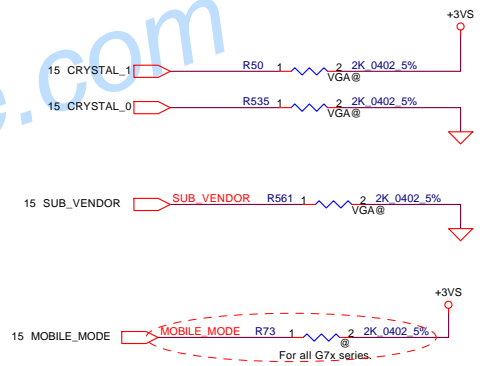
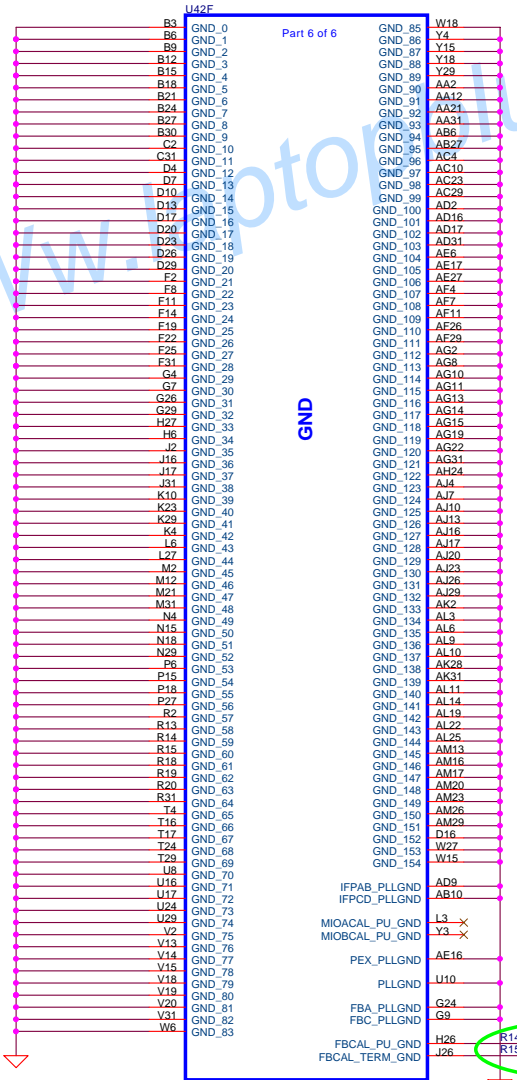
Security Classification	Compal Secret Data		Title
Issued Date	2005/06/20	Deciphered Date	2006/06/20
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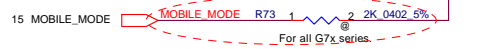
Security Classification	Compal Secret Data	
Issued Date	2005/06/20	Deciphered Date
		2006/06/20

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Compal Electronics, Inc.		
Title		
G72/G73 Power		
Size	Document Number	Rev
B	HBL50 LA-2921P	0.3
Date:	Friday, November 11, 2005	Sheet 17 of 59



G73M : SA00000QZ00  
 G72M : SA00000QY00  
 G72MV : SA00000QY20

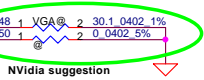


STRAPS	PIN	DESCRIPTION	Value	Value
CRYSTAL[1:0]	MIOBD[6,2]	27MHz=10, 14.318MHz=01, 13.5MHz=00	10	
ROM_TYPE[1:0]	MIOBD [11:10]	Parallel=00, SERIAL M25P10=01, Serial SST45VF=10	01	
SUB_VENDOR	MIOAD1	VBIOs on card (pull high) VBIOs with system BIOS (pull down)	0	
PEX_PLL_TERM	MIOAD0		0	
PEX_CFG[2:0]	MIOAD [9,8,6]	Recommended for G7x	010	
RAM_CFG[3:0]	MIOAD[5:2]	16Mx16x4 1.8V (128bit G73M)	0001	Samsung
		16Mx16x4 1.8V (128bit G73M)	0011	Hynix
		16Mx16x4 1.8V (64bit G73M)	1001	Samsung
		16Mx16x4 1.8V (64bit G73M)	1011	Hynix
		16Mx16x4 1.8V (64bit G72MV)	0001	Samsung
PCI_DEVID[3:0]	VIPD[5:3] MIOA_HSYNC	G73M-xxxxx8 G72M-0x01D8	1000	
		G72MV-0x01D7 TBD/TBD	0111	
MOBILE_MODE	MIOBD7	For NV44M/G7x		0

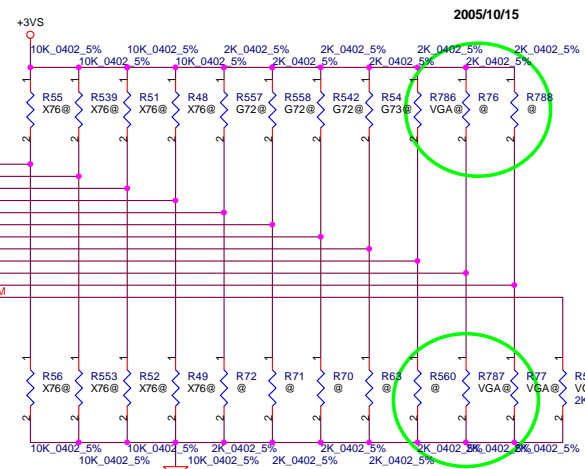
RAM\_CFG[1:0]  
 (Manufacture)  
 (01=Sam, 10=Inf, 11=Hyn)

RAM\_CFG[2] (0=16M or 1=32M)

RAM\_CFG[3] (Bandwidth 0=Full, 1=Half)



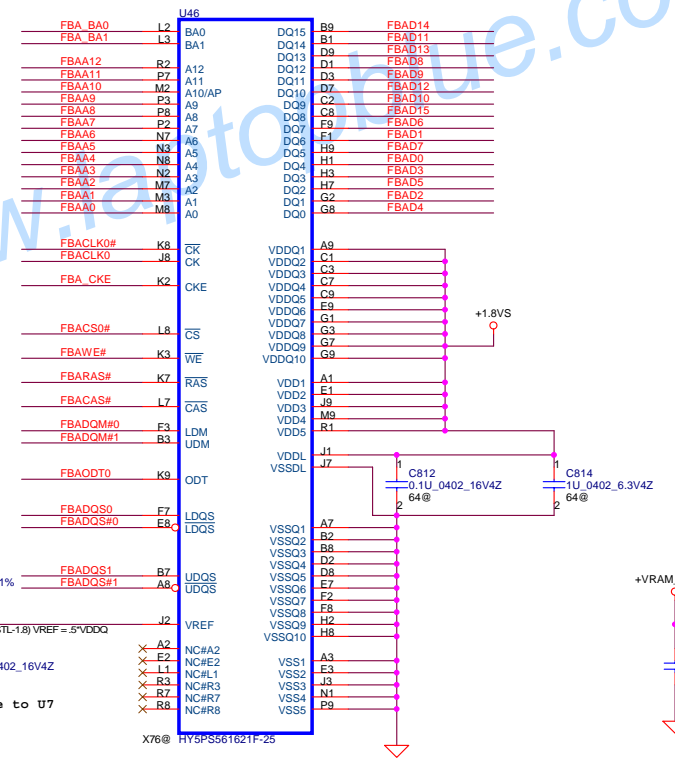
Bandwidth	RAM Type	Vendor
FULL R49	32M R51	Samsung R553, R55
HALF R48	16M R52	Hynix R539, R55
		Infineon R553, R56



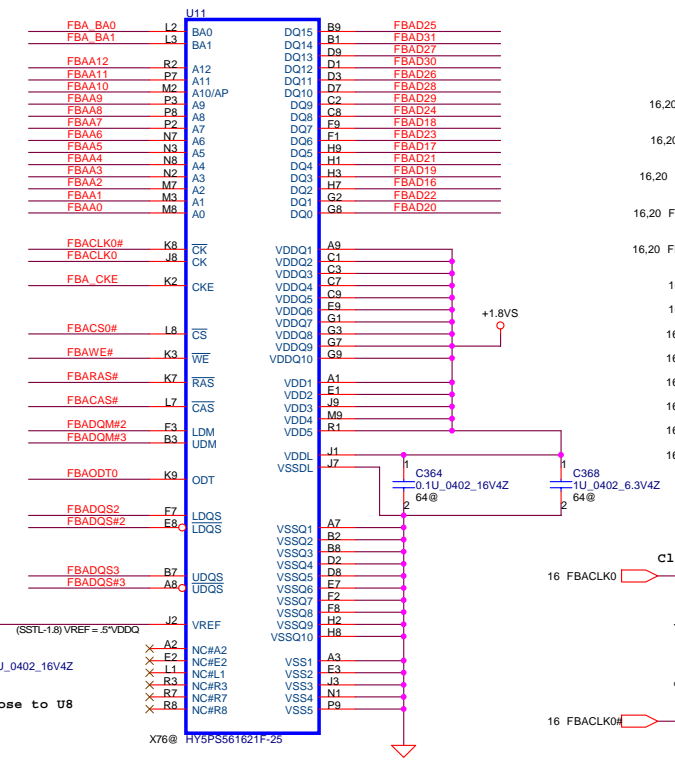
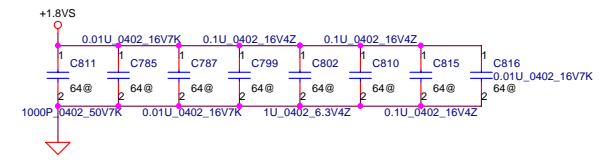
Package	Part Number	Manufacturer
(10*12.5)	Infineon GDDR2(400): SA00000S800 (HYB18T256161AFL-25)	Infineon GDDR2(350): SA00000T700 (HYB18T256161AF-28)
(11*13)	Samsung GDDR2 (400): SA00000FG10 (K4N56163QF-ZC25)	Samsung GDDR2 (350): SA00000TB00 (K4N56163QF-ZC2A)
(8*13)	Hynix GDDR2 (400): SA00000FF10 (HY5PS561621AFP-25)	Hynix GDDR2 (350): SA00000TJ00 (HY5PS561621AFP-28)

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				Rev 0.3 Sheet 18 of 59

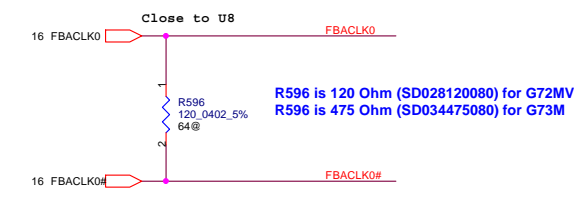
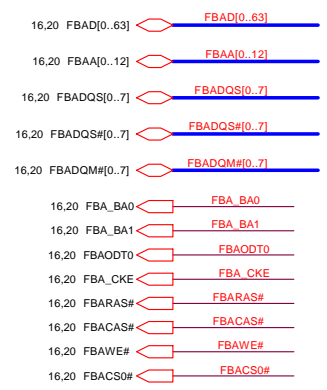
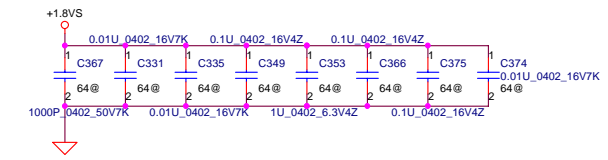
www.totoku.com



DDR2 BGA MEMORY



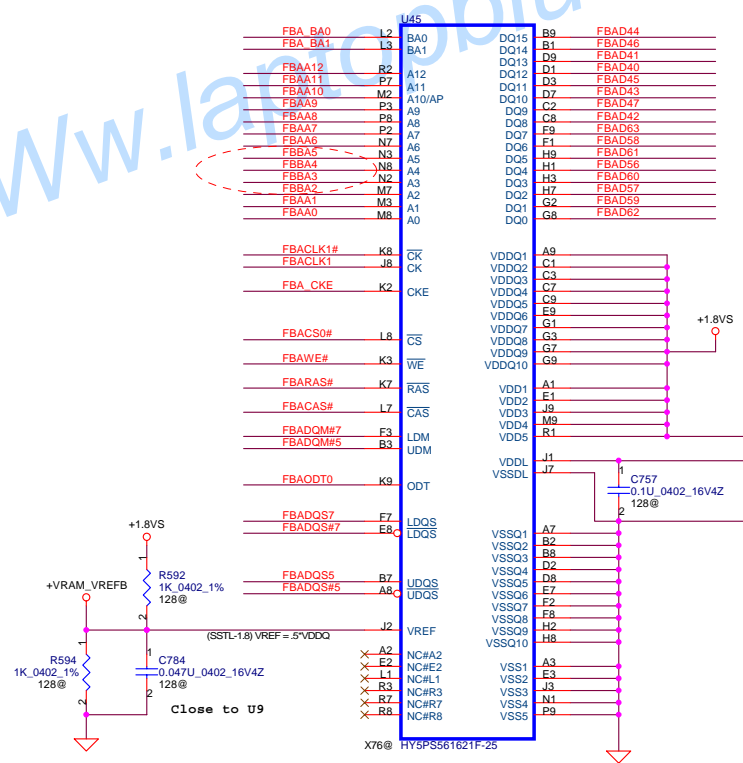
DDR2 BGA MEMORY



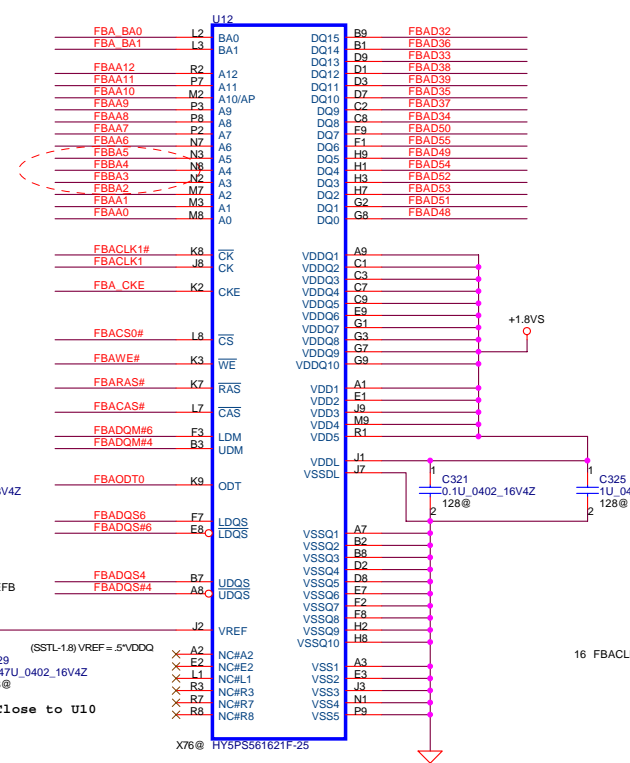
Security Classification	Compal Secret Data		Title	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	VRAM DDRA
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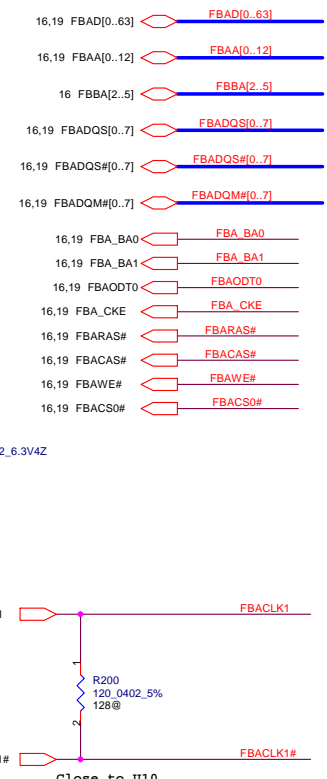
www.lancomblue.com



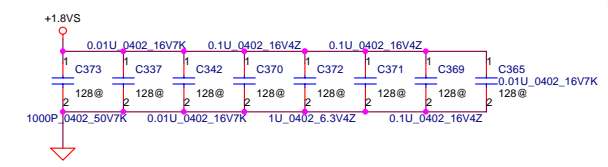
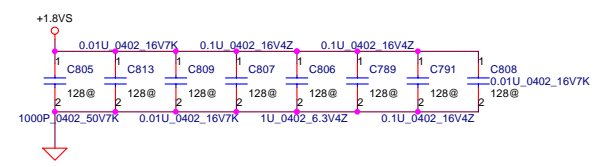
DDR2 BGA MEMORY



DDR2 BGA MEMORY



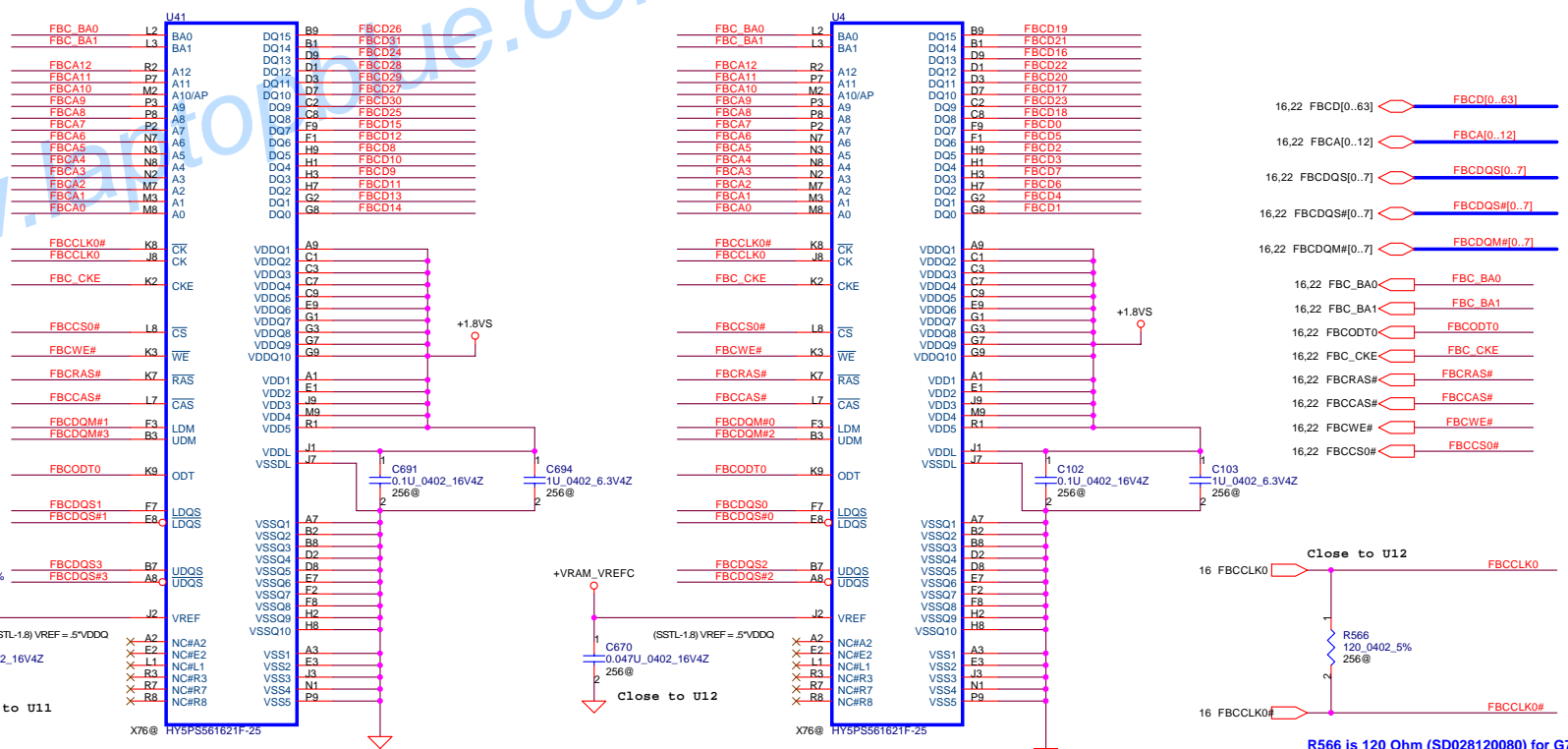
R200 is 120 Ohm (SD028120080) for G72MV  
R200 is 481 Ohm (SD00000CA80) for G73M



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				VRAM DDRB
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Date:	Friday, November 11, 2005	Sheet	20 of 59	

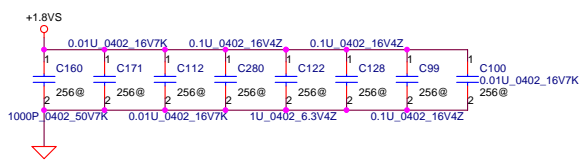
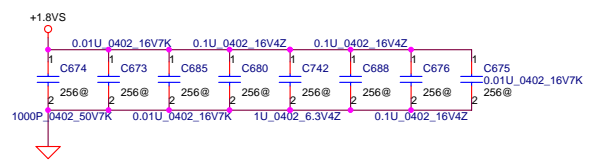


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DDR2 BGA MEMORY

DDR2 BGA MEMORY



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Issued Date	2005/06/20	Deciphered Date	2006/06/20	VRAM DDRC
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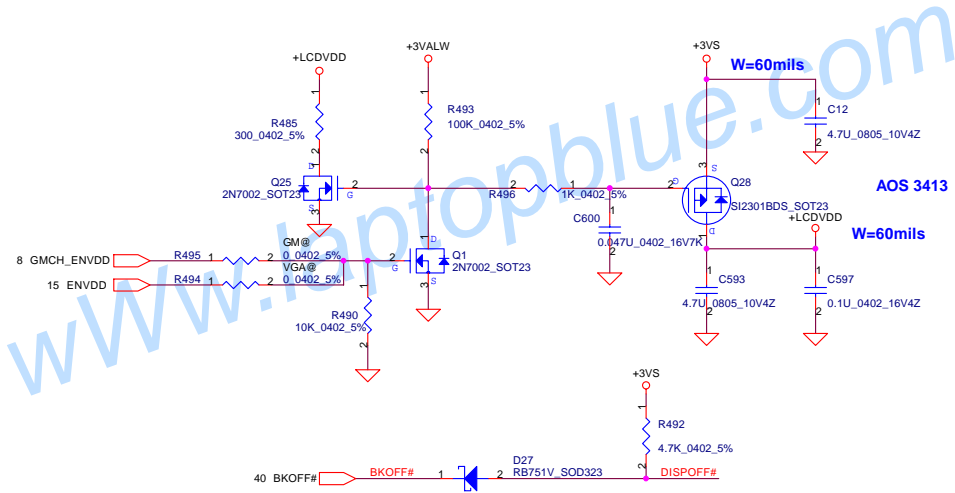
Compal Electronics, Inc.

VRAM DDRC

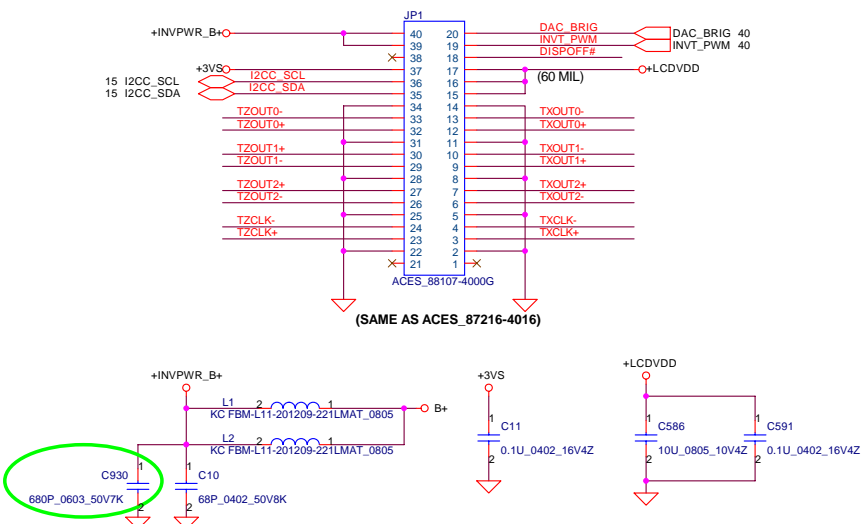
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# LCD POWER CIRCUIT



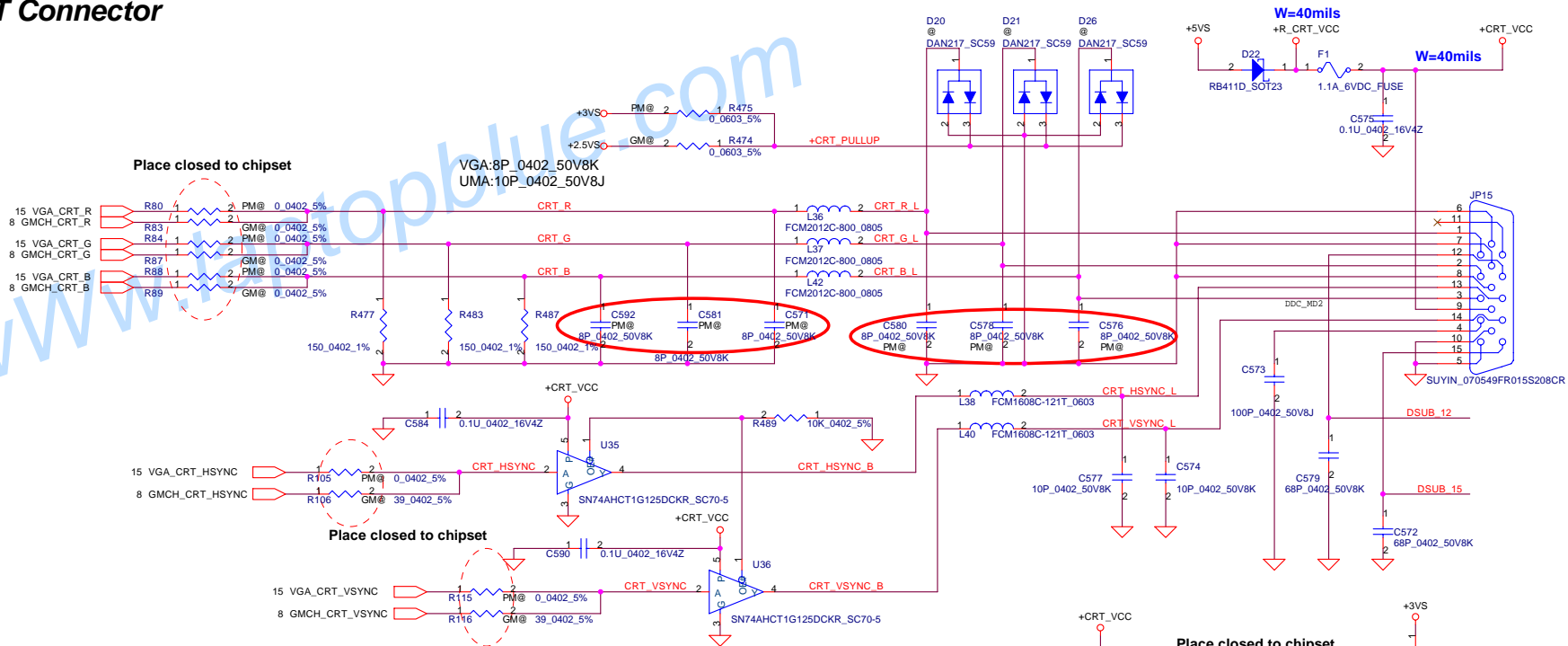
## LCD/PANEL BD. Conn.



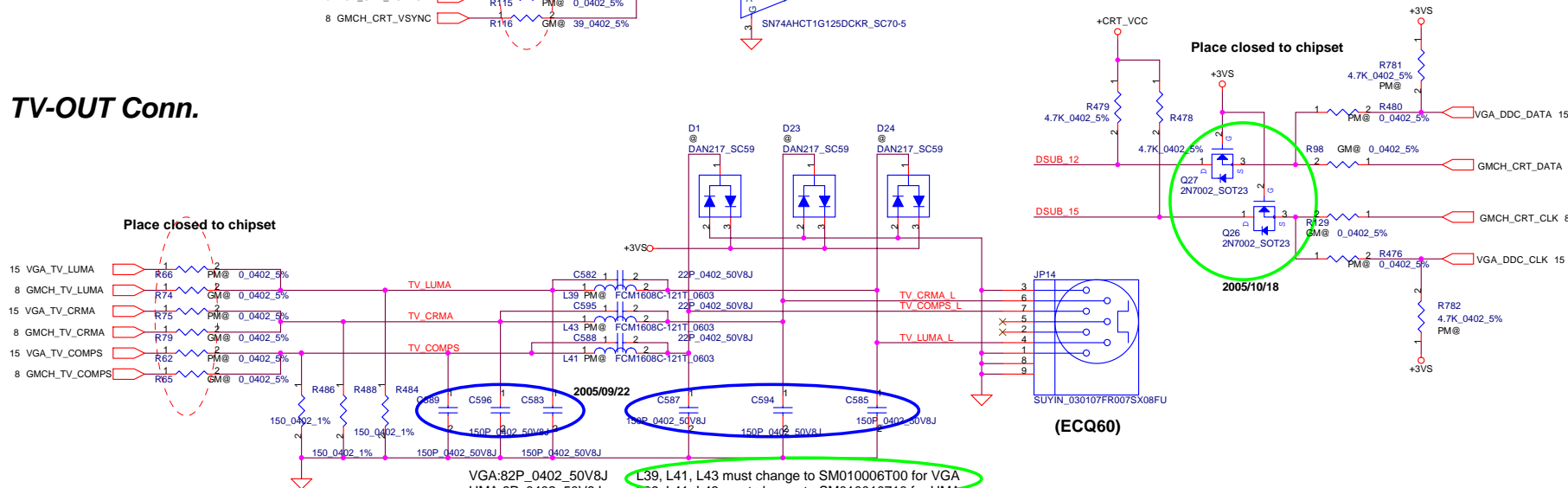
TXOUT0-	R25	1	2	VGA@ 0.0402 5%	LVDSA0-	LVDSA0-	15
TXOUT0+	R26	1	2	VGA@ 0.0402 5%	LVDSA0+	LVDSA0+	15
TXOUT1-	R27	1	2	VGA@ 0.0402 5%	LVDSA1-	LVDSA1-	15
TXOUT1+	R28	1	2	VGA@ 0.0402 5%	LVDSA1+	LVDSA1+	15
TXOUT2-	R29	1	2	VGA@ 0.0402 5%	LVDSA2-	LVDSA2-	15
TXOUT2+	R30	1	2	VGA@ 0.0402 5%	LVDSA2+	LVDSA2+	15
TXCLK-	R31	1	2	VGA@ 0.0402 5%	LVDSAC-	LVDSAC-	15
TXCLK+	R32	1	2	VGA@ 0.0402 5%	LVDSAC+	LVDSAC+	15
TZOUT0-	R33	1	2	VGA@ 0.0402 5%	LVDSB0-	LVDSB0-	15
TZOUT0+	R34	1	2	VGA@ 0.0402 5%	LVDSB0+	LVDSB0+	15
TZOUT1-	R35	1	2	VGA@ 0.0402 5%	LVDSB1-	LVDSB1-	15
TZOUT1+	R36	1	2	VGA@ 0.0402 5%	LVDSB1+	LVDSB1+	15
TZOUT2-	R37	1	2	VGA@ 0.0402 5%	LVDSB2-	LVDSB2-	15
TZOUT2+	R38	1	2	VGA@ 0.0402 5%	LVDSB2+	LVDSB2+	15
TZCLK-	R39	1	2	VGA@ 0.0402 5%	LVDSBC-	LVDSBC-	15
TZCLK+	R40	1	2	VGA@ 0.0402 5%	LVDSBC+	LVDSBC+	15
I2CC_SCL	R41	1	2	GM@ 0.0402 5%	GMCH_LCD_CLK	GMCH_LCD_CLK	8
I2CC_SDA	R42	1	2	GM@ 0.0402 5%	GMCH_LCD_DATA	GMCH_LCD_DATA	8
TXOUT0-	R509	1	2	GM@ 0.0402 5%	GMCH_TXOUT0-	GMCH_TXOUT0-	8
TXOUT0+	R508	1	2	GM@ 0.0402 5%	GMCH_TXOUT0+	GMCH_TXOUT0+	8
TXOUT1-	R507	1	2	GM@ 0.0402 5%	GMCH_TXOUT1-	GMCH_TXOUT1-	8
TXOUT1+	R506	1	2	GM@ 0.0402 5%	GMCH_TXOUT1+	GMCH_TXOUT1+	8
TXOUT2-	R505	1	2	GM@ 0.0402 5%	GMCH_TXOUT2-	GMCH_TXOUT2-	8
TXOUT2+	R504	1	2	GM@ 0.0402 5%	GMCH_TXOUT2+	GMCH_TXOUT2+	8
TXCLK-	R503	1	2	GM@ 0.0402 5%	GMCH_TXCLK-	GMCH_TXCLK-	8
TXCLK+	R502	1	2	GM@ 0.0402 5%	GMCH_TXCLK+	GMCH_TXCLK+	8
TZOUT0-	R525	1	2	GM@ 0.0402 5%	GMCH_TZOUT0-	GMCH_TZOUT0-	8
TZOUT0+	R524	1	2	GM@ 0.0402 5%	GMCH_TZOUT0+	GMCH_TZOUT0+	8
TZOUT1-	R523	1	2	GM@ 0.0402 5%	GMCH_TZOUT1-	GMCH_TZOUT1-	8
TZOUT1+	R522	1	2	GM@ 0.0402 5%	GMCH_TZOUT1+	GMCH_TZOUT1+	8
TZOUT2-	R521	1	2	GM@ 0.0402 5%	GMCH_TZOUT2-	GMCH_TZOUT2-	8
TZOUT2+	R520	1	2	GM@ 0.0402 5%	GMCH_TZOUT2+	GMCH_TZOUT2+	8
TZCLK-	R519	1	2	GM@ 0.0402 5%	GMCH_TZCLK-	GMCH_TZCLK-	8
TZCLK+	R518	1	2	GM@ 0.0402 5%	GMCH_TZCLK+	GMCH_TZCLK+	8

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				LCD Connector	
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				Date: Friday, November 11, 2005	Rev 0.3
				Sheet 23 of 59	

# CRT Connector

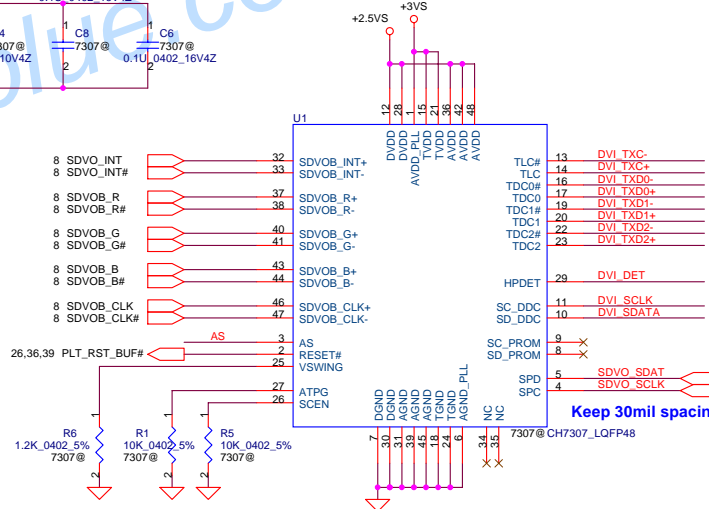
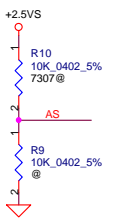
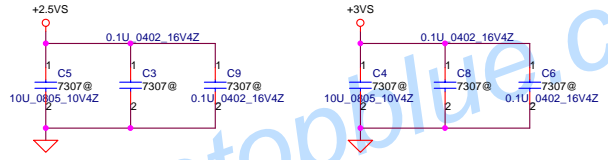


# TV-OUT Conn.



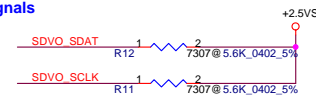
Security Classification		Compal Secret Data		Title	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	Compal Electronics, Inc.	
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Size	Document Number	Date		Rev	
B	HBL50 LA-2921P	Friday, November 11, 2005		0.3	
Date				Sheet	of
				24	59

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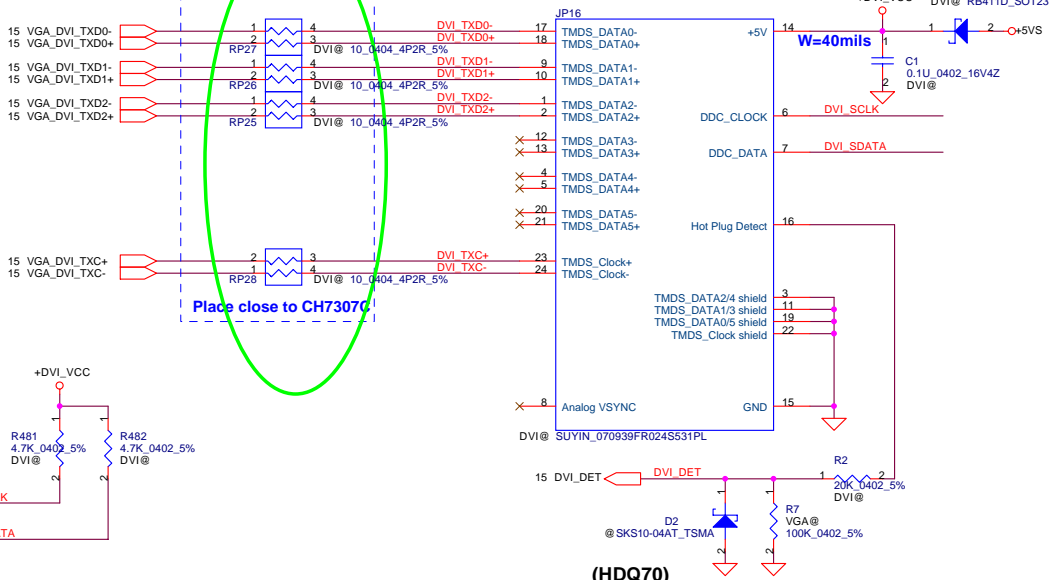


BOM structure	DVI from SDVO	DVI from Discrete VGA
7307@	Stuff	No_Stuff
VGA@	No_Stuff	Stuff
@	No_Stuff	No_Stuff

Keep 30mil spacing to other signals



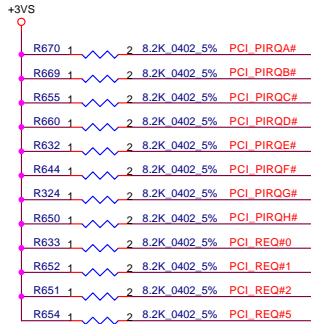
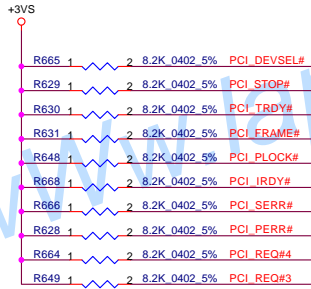
### DVI-D Connector



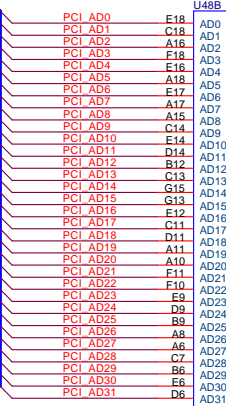
(HDQ70)

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Size B	Document Number	HBL50 LA-2921P		Rev	0.3
Date:	Friday, November 11, 2005	Sheet	25 of 59		

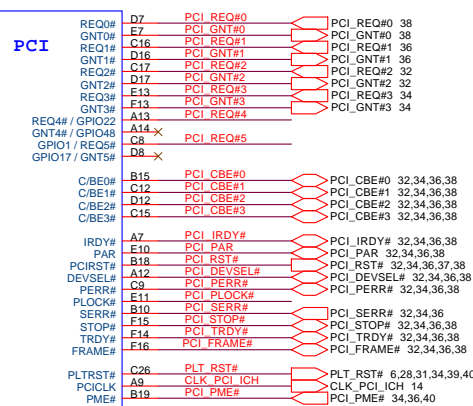
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 ICH7M-DH(B-0) (QK17) [QS]:SA00000JK60



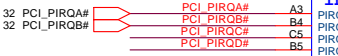
32,34,36,38 PCI\_AD[0..31]



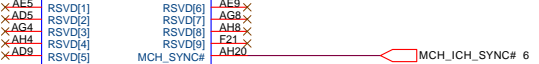
**PCI**



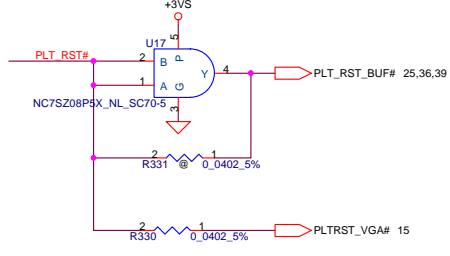
**Interrupt I/F**



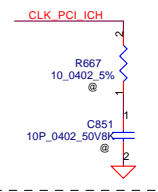
**MISC**



CH7\_BGA652-D

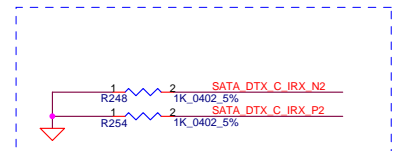
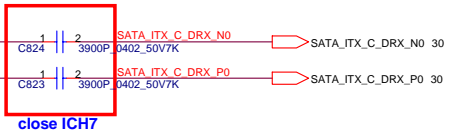
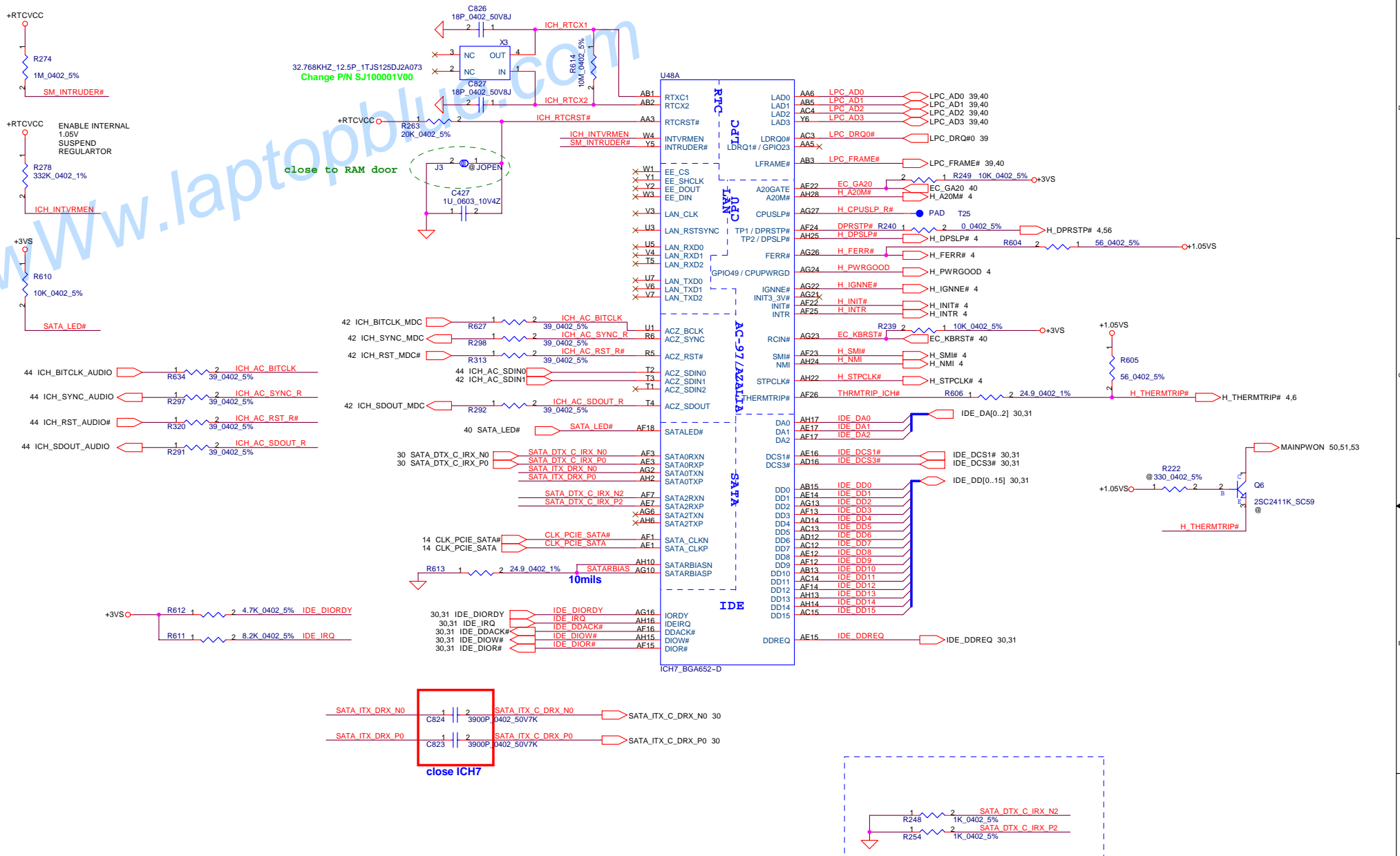


Place closely pin A9

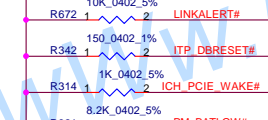
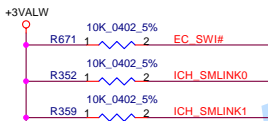
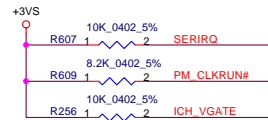


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				Rev 0.3

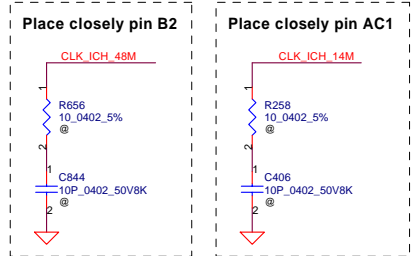
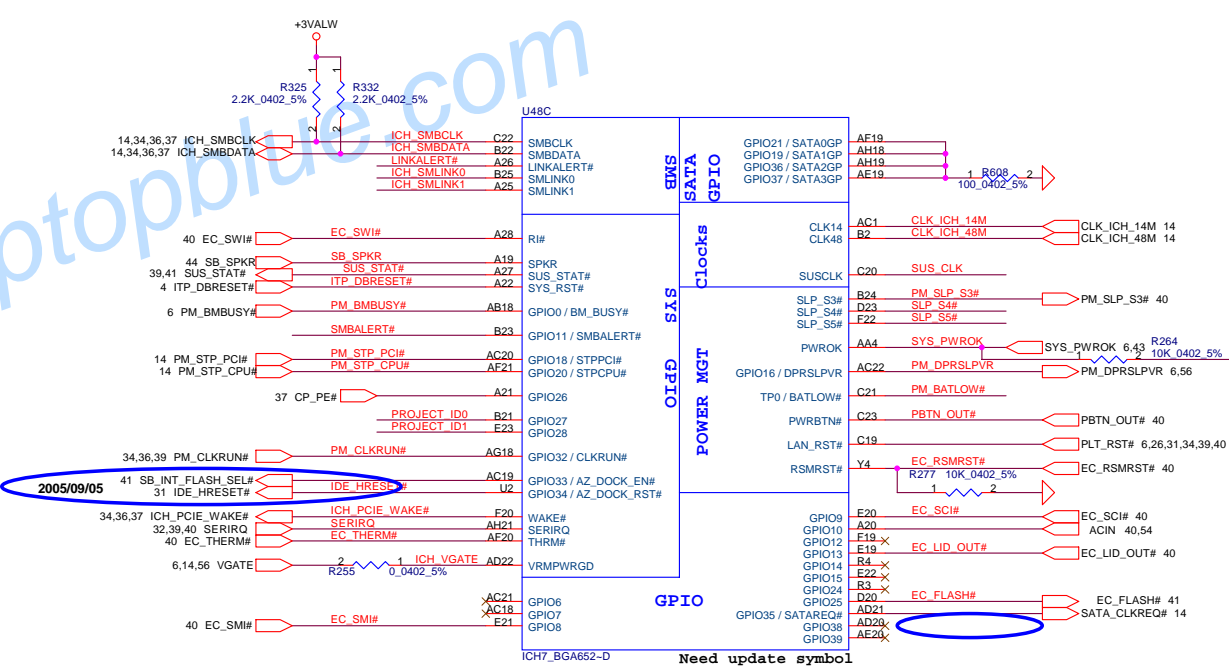




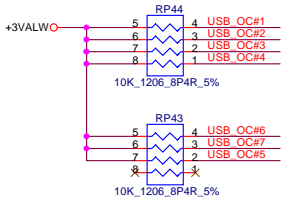
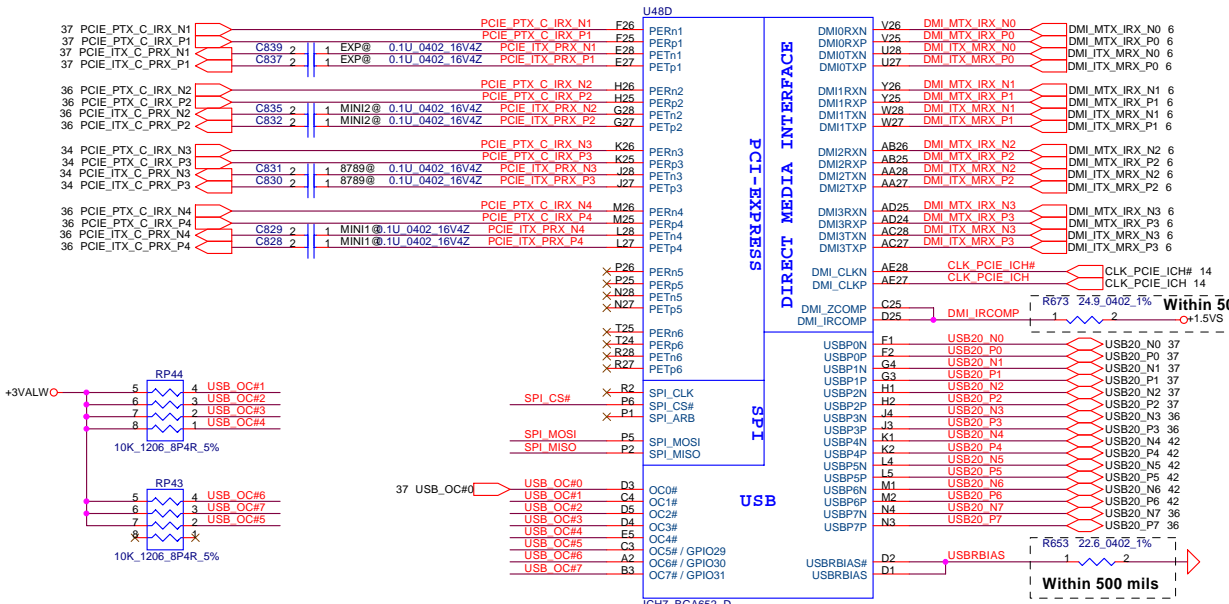
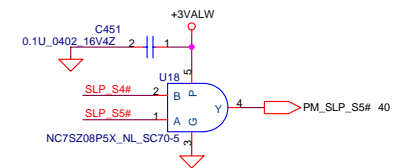
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			Custom	HBL50 LA-2921P	0.3
			Date:	Friday, November 11, 2005	Sheet 27 of 59



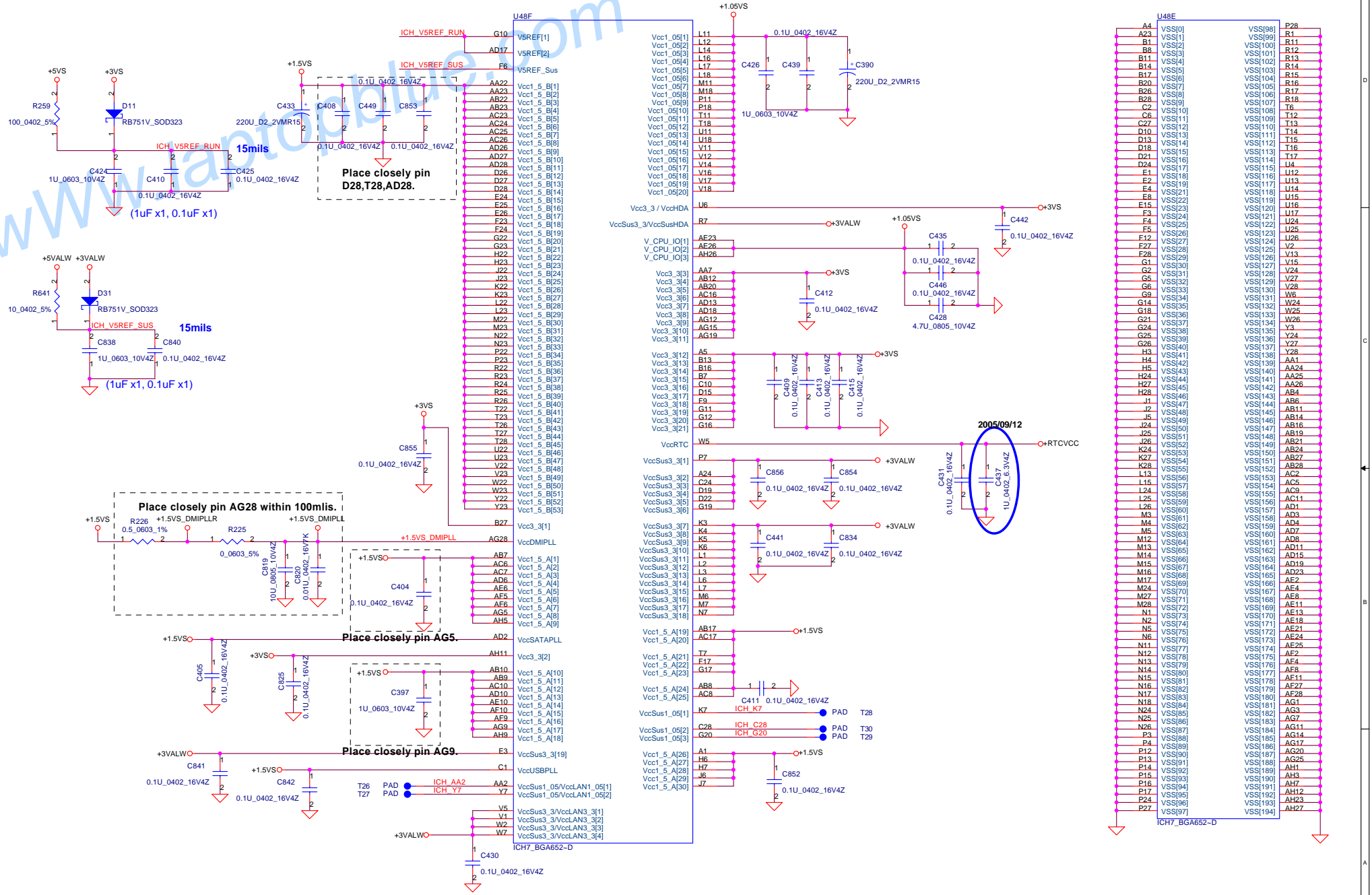
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01	= Geneva



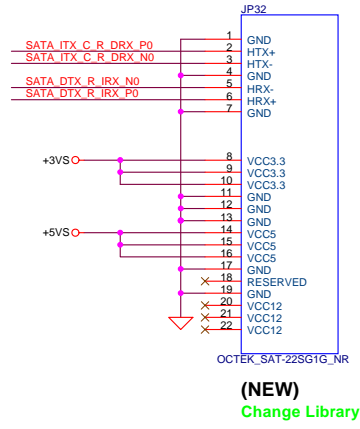
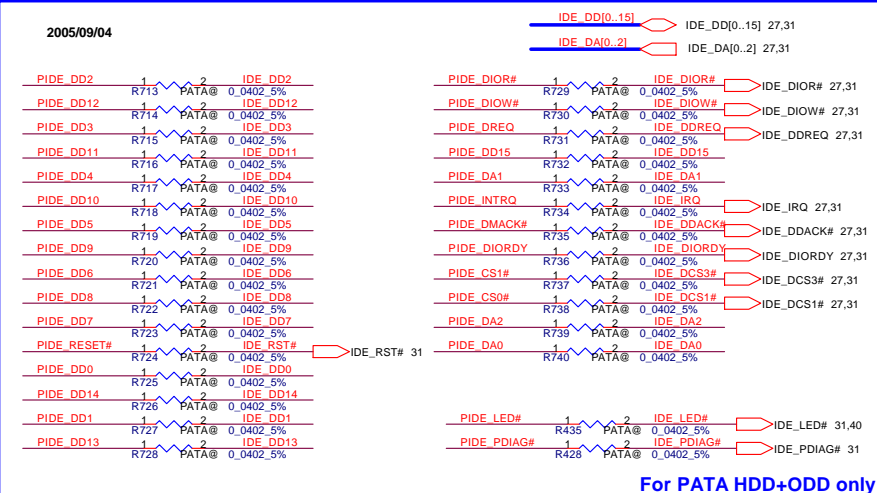
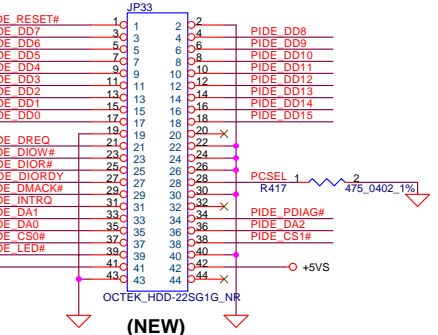
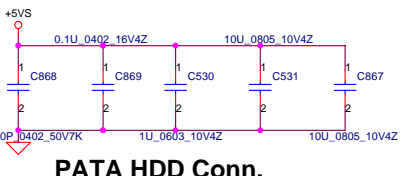
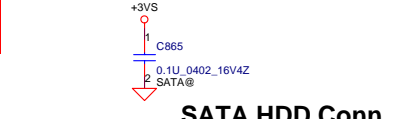
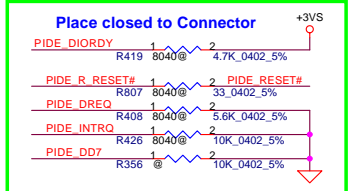
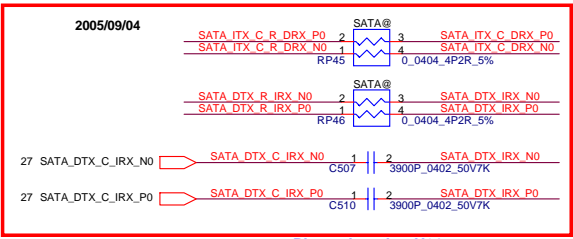
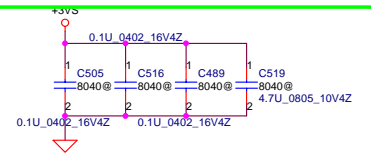
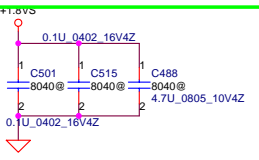
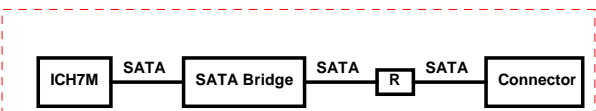
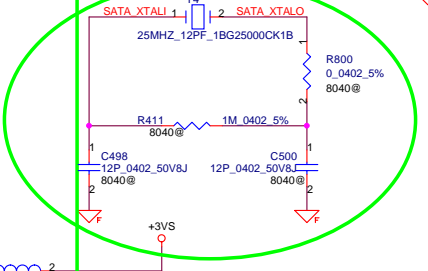
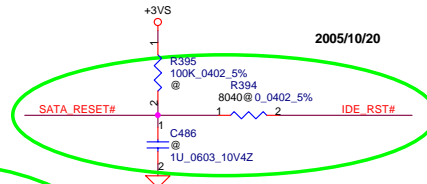
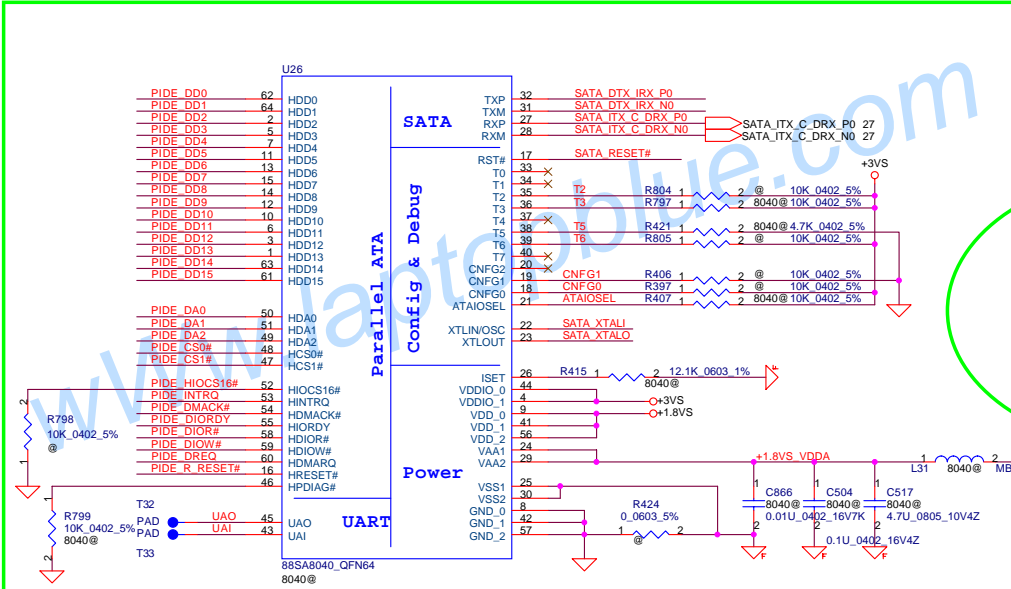
PM\_DPRSPLVPR : Need to series a 500Ohm resistor to IMVP6



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Date:	Friday, November 11, 2005	Sheet	28	of 59

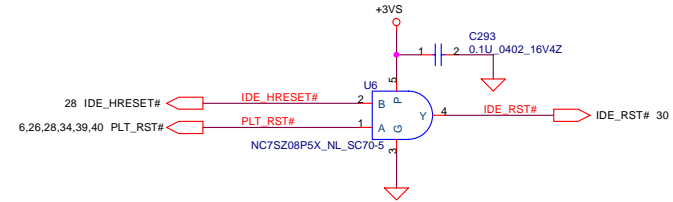
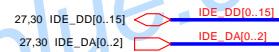
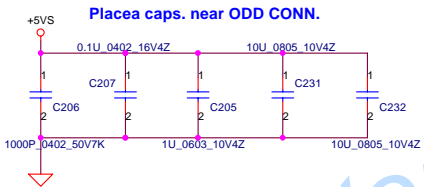


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				B	HBL50 LA-291P
				Date:	Friday, November 11, 2005
				Sheet	29 of 59
				Rev	0.3

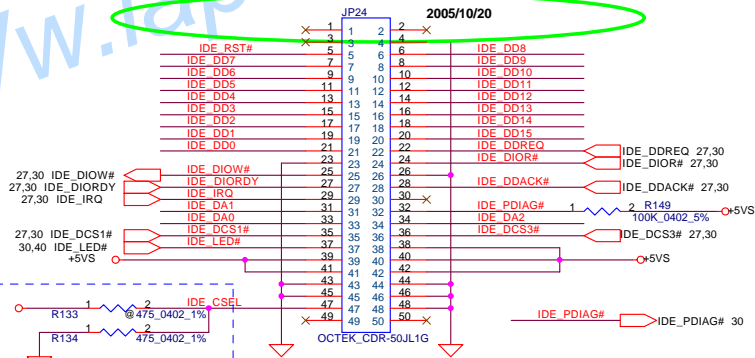


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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title		
				SATA Bridge		
				HBL50 LA-2921P		
				Date:	Friday, November 11, 2005	Sheet 30 of 59
				Rev	0.3	

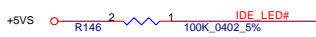
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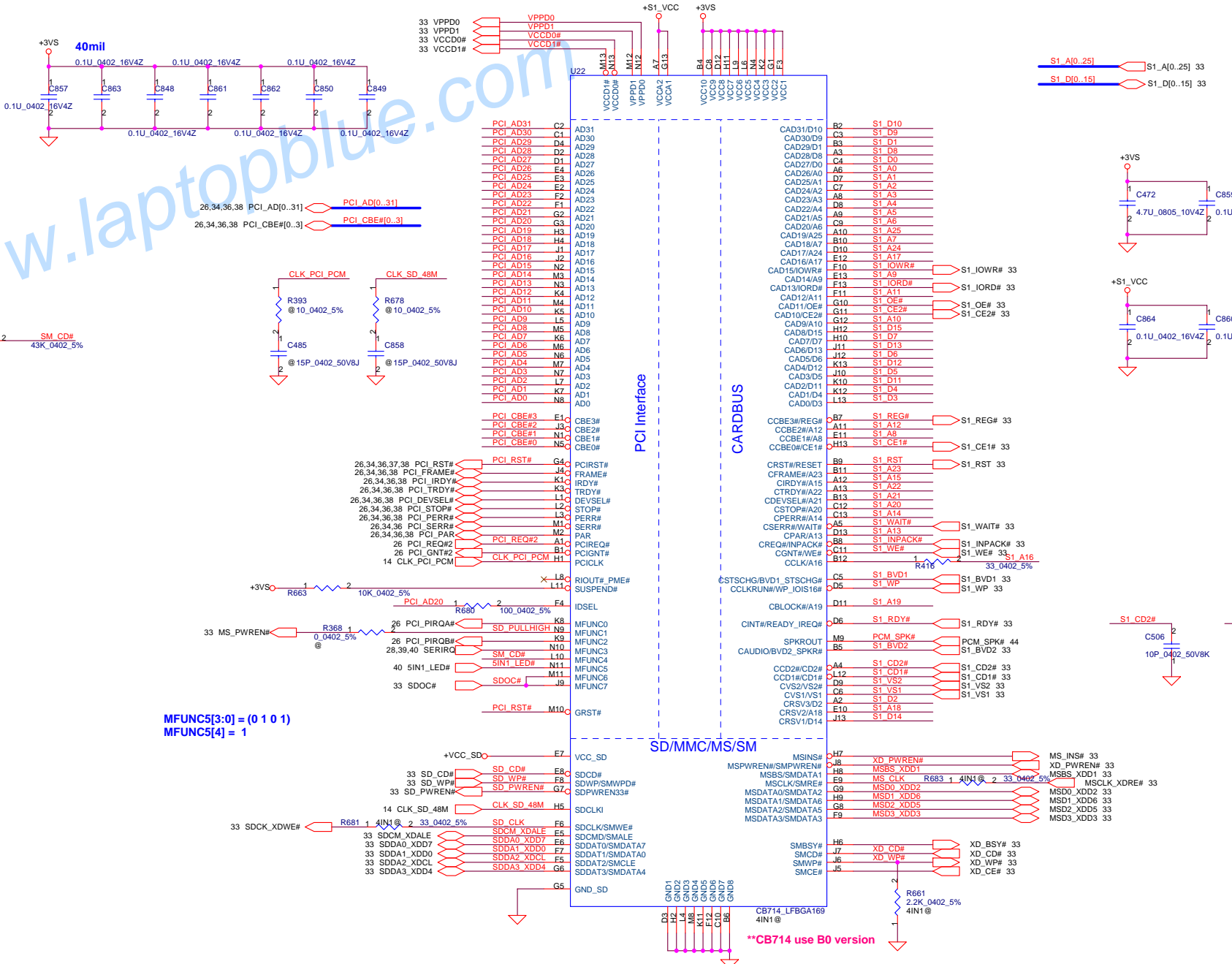
2005/10/20



**IDE\_CSEL**  
 Grounding for Master (When use SATA HDD)  
 Open or High for Slaver (Normal)



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				ODD & SATA HDD Connector
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			Document Number	Rev
			HBL50 LA-2921P	0.3
			Date: Friday, November 11, 2005	Sheet 31 of 59



S1\_A[0..25] S1\_A[0..25] 33  
 S1\_D[0..15] S1\_D[0..15] 33

26,34,36,38 PCI\_AD[0..31] PCI\_AD[0..31]  
 26,34,36,38 PCI\_CBE[0..3] PCI\_CBE[0..3]

CLK PCI\_PCM CLK\_S1\_PCM  
 CLK SD\_48M CLK\_S1\_48M

MFUNC5[3:0] = (0 1 0 1)  
 MFUNC5[4] = 1

PCI Interface

CARDBUS

SD/MMC/MS/SM

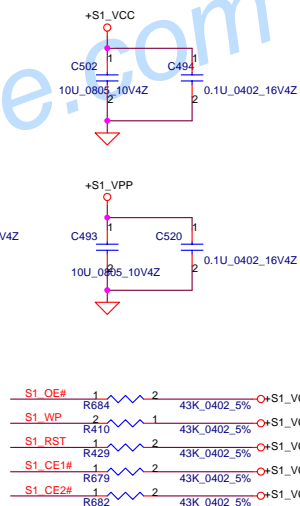
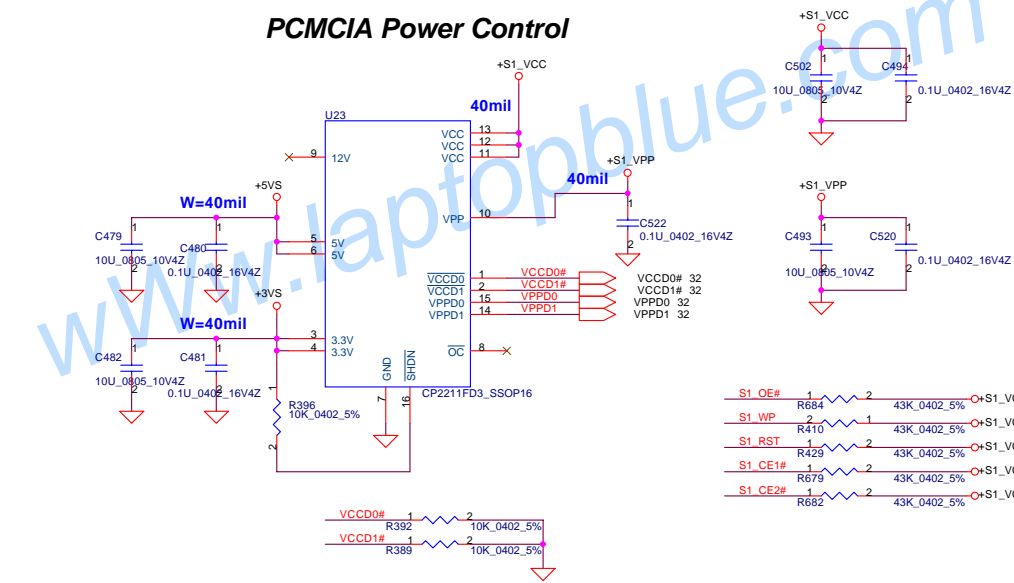
\*\*CB714 use B0 version

CB714 P/N: SA007140B50  
 CB1410 P/N: SA014100310

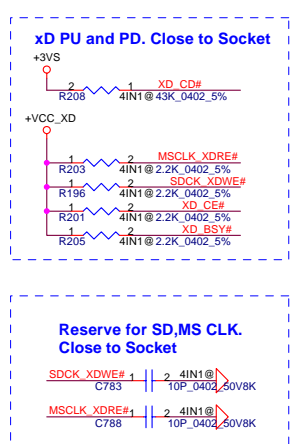
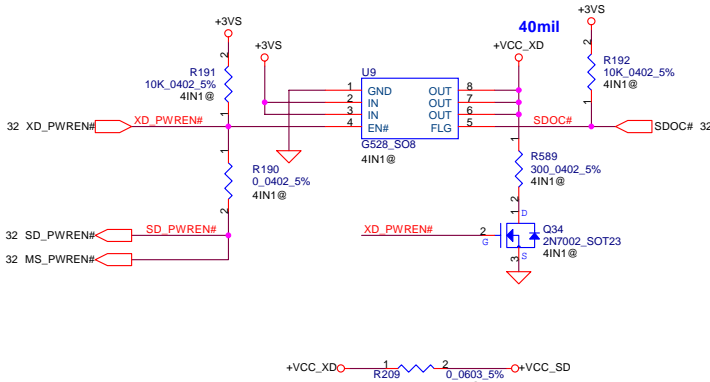
Security Classification	Compal Secret Data		Title	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	Cardbus Controller CB714
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSMITTED FROM THE CUSTOMER TO THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				
Date:	Friday, November 11, 2005	Sheet	32 of 59	Rev 0.3



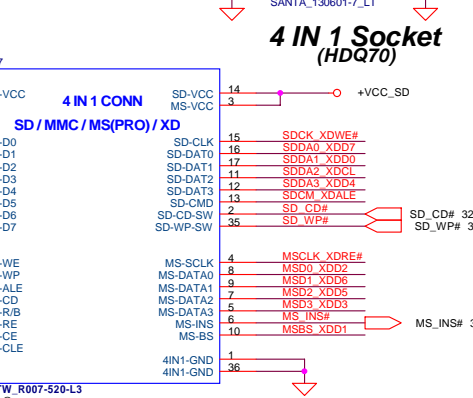
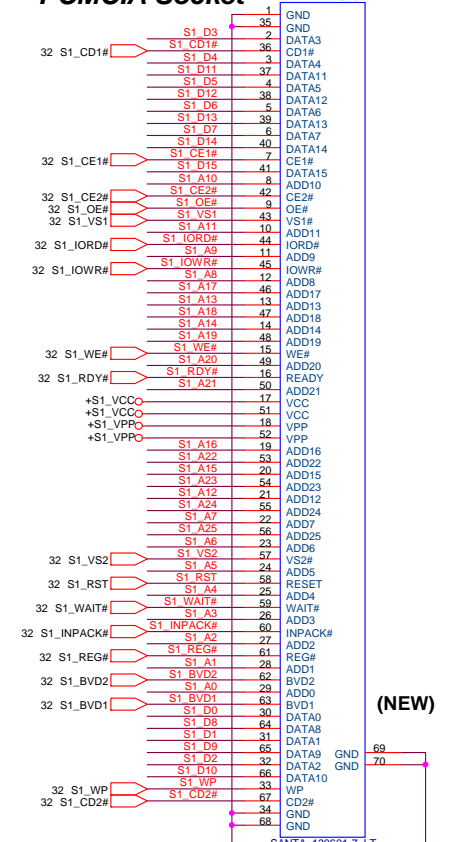
### PCMCIA Power Control



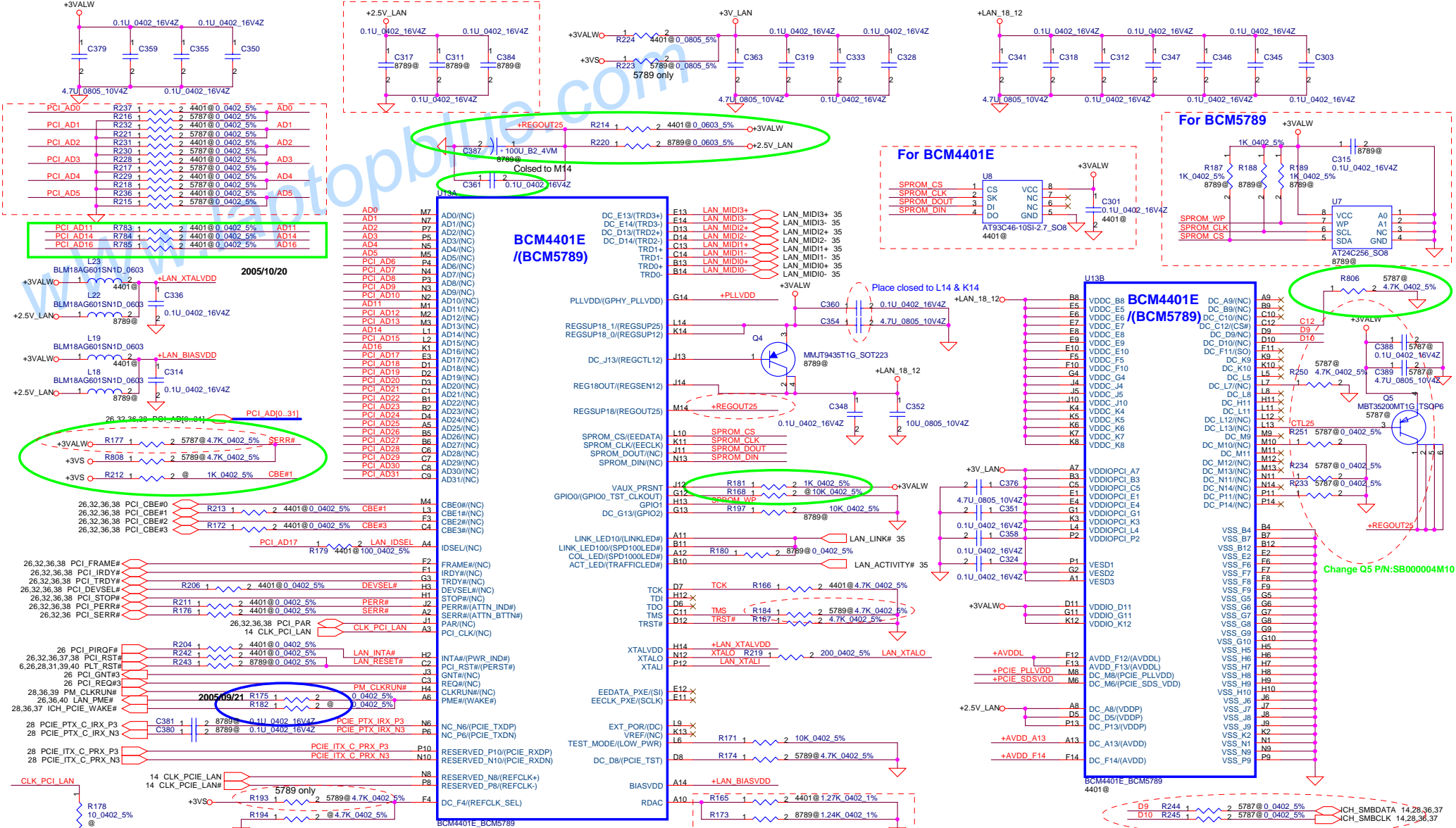
### SD/MS Power Control XD Power Control



### PCMCIA Socket



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	(SA00000D10)	(SA00000SZ00)	(SA00000YJ00)
FN	4401E(10/100 LAN)	5789(10/100/1000 LAN)	5787(10/100/1000 LAN)
RDAC	1.27K	1.24K	1.24K

BOM structure	4401E(10/100 LAN)	5789(10/100/1000 LAN)	5787(10/100/1000 LAN)
4401@	Stuff	No_Stuff	No_Stuff
5789@	No_Stuff	Stuff	No_Stuff
5787@	No_Stuff	No_Stuff	Stuff
8789@	No_Stuff	Stuff	Stuff
@	No_Stuff	No_Stuff	No_Stuff

Security Classification	Compal Secret Data	
Issued Date	2005/06/20	Deciphered Date
		2006/06/20

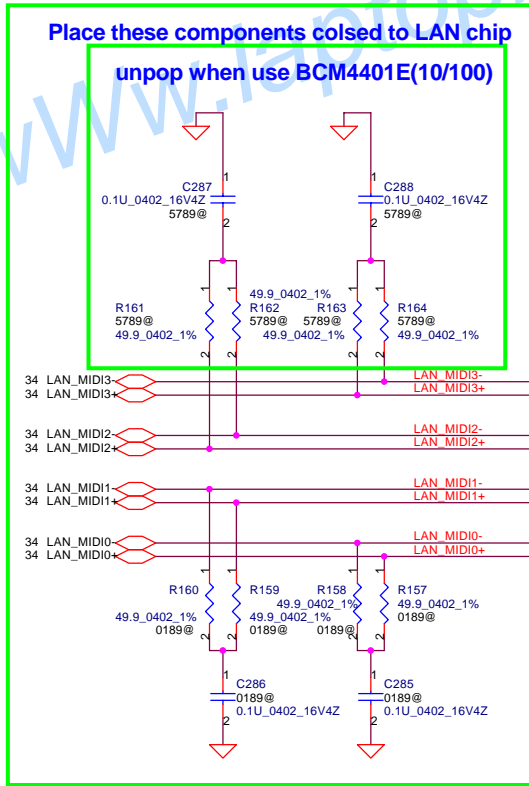
Compal Electronics, Inc.			
LAN BCM4401E/Jade15			
Size	Document Number		
B	HBL50 LA-2921P		
Date:	Friday, November 11, 2005	Sheet	34 of 59

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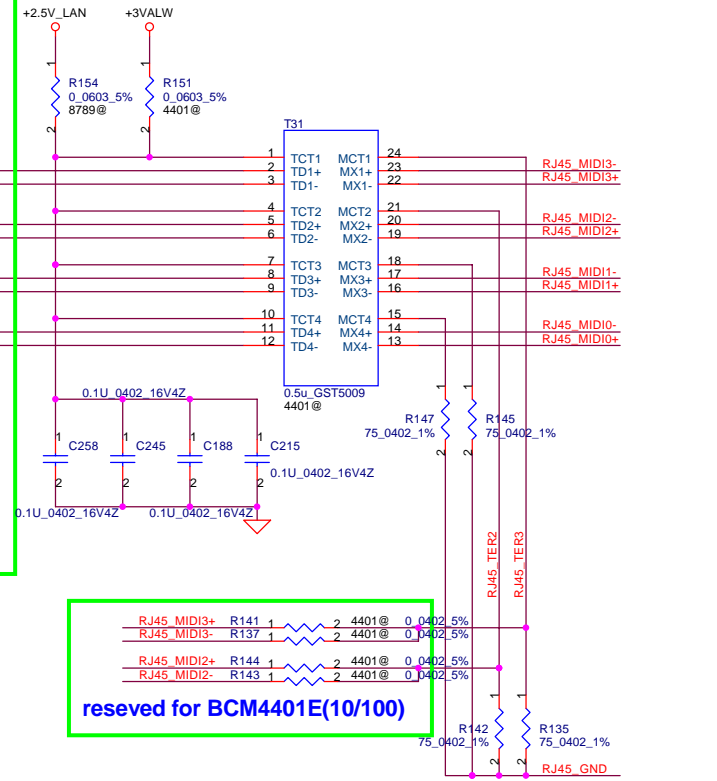
# LAN BCM4401E/ BCM5789

Place these components colsed to LAN chip

unpop when use BCM4401E(10/100)

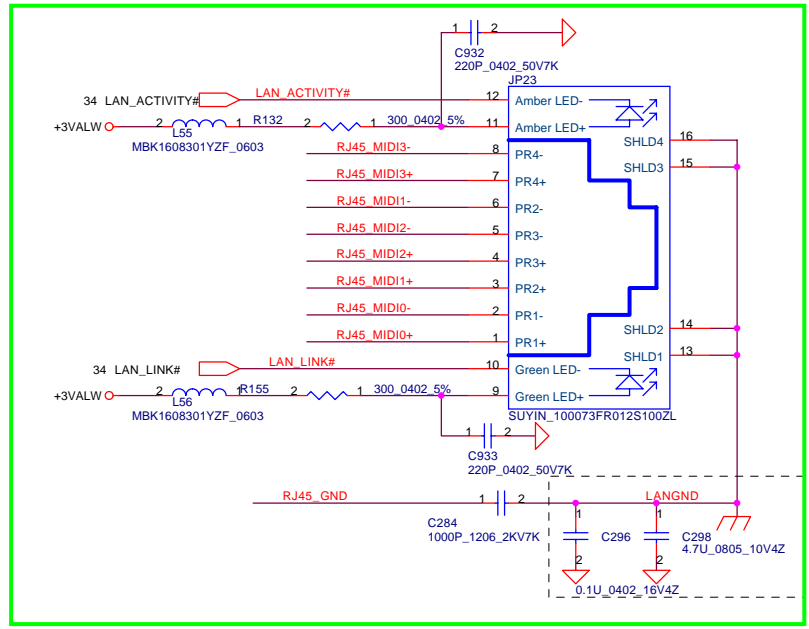


GbE Transformer: GST5009 (SP050005610)  
10/100 Transformer : TST1284-LF (SP050001X10)

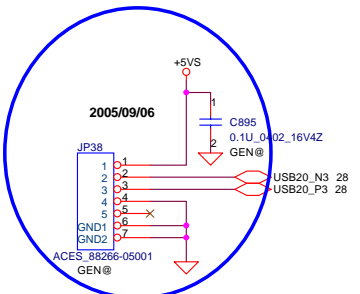
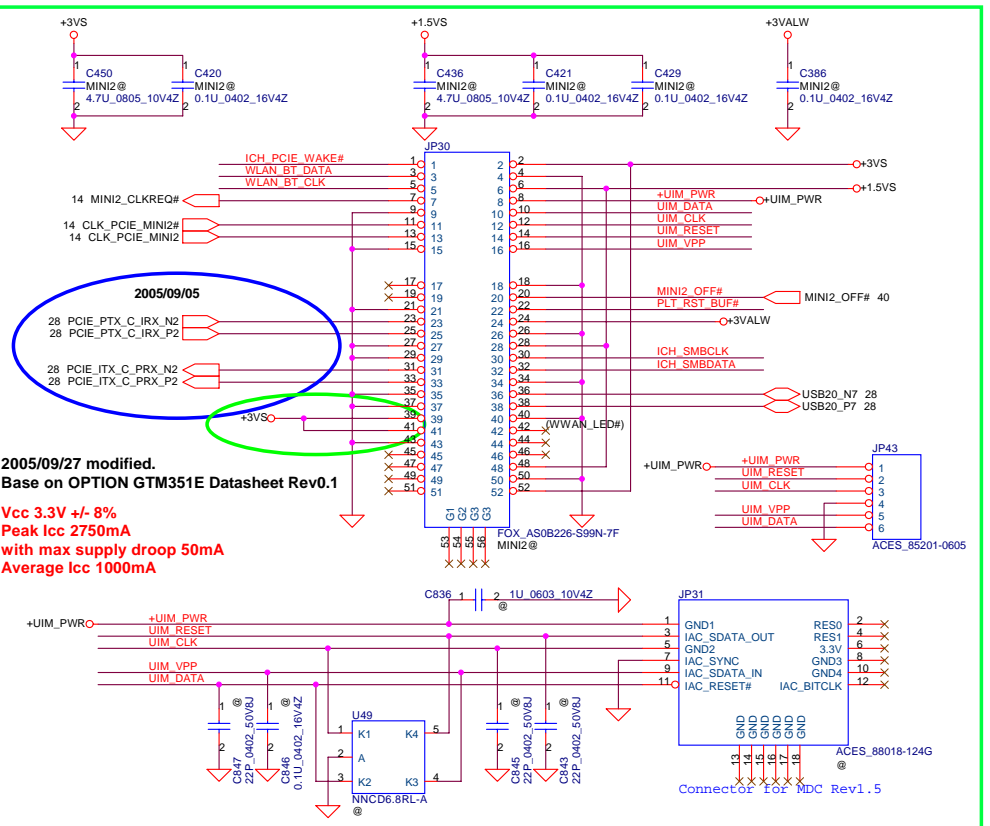
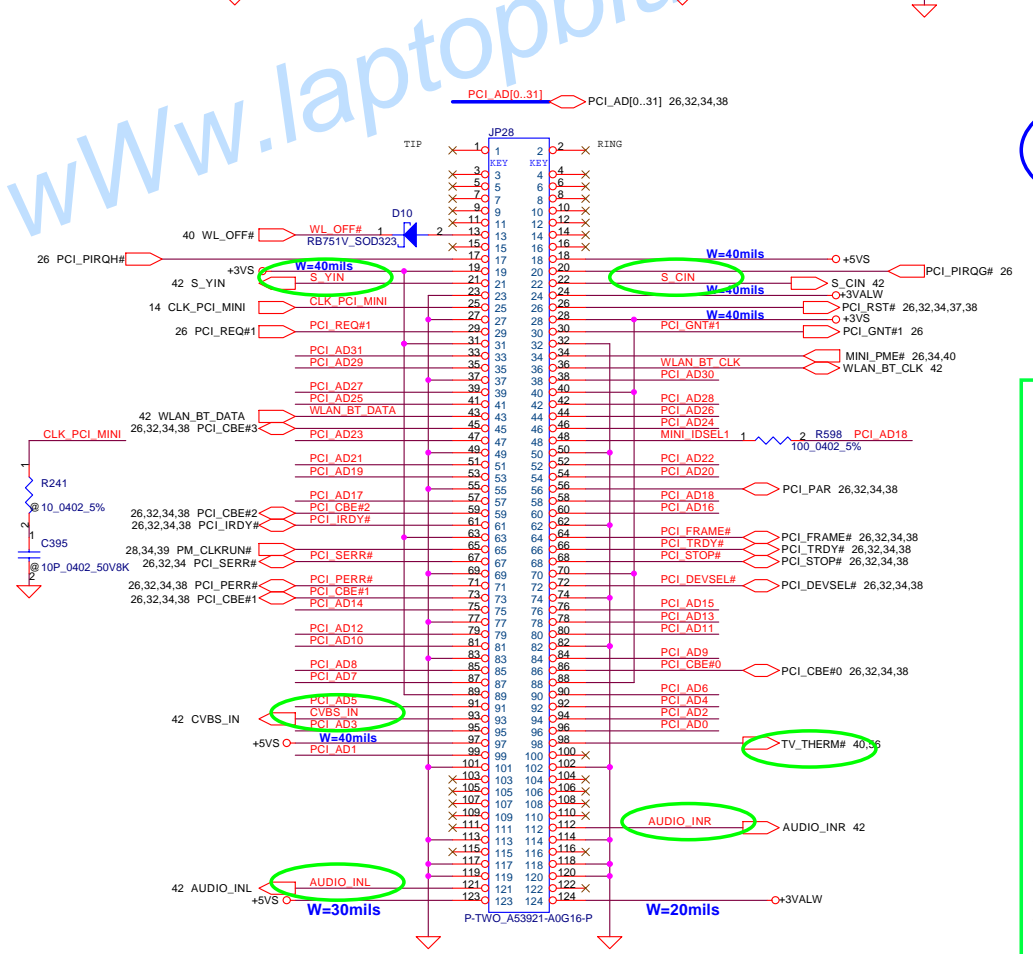
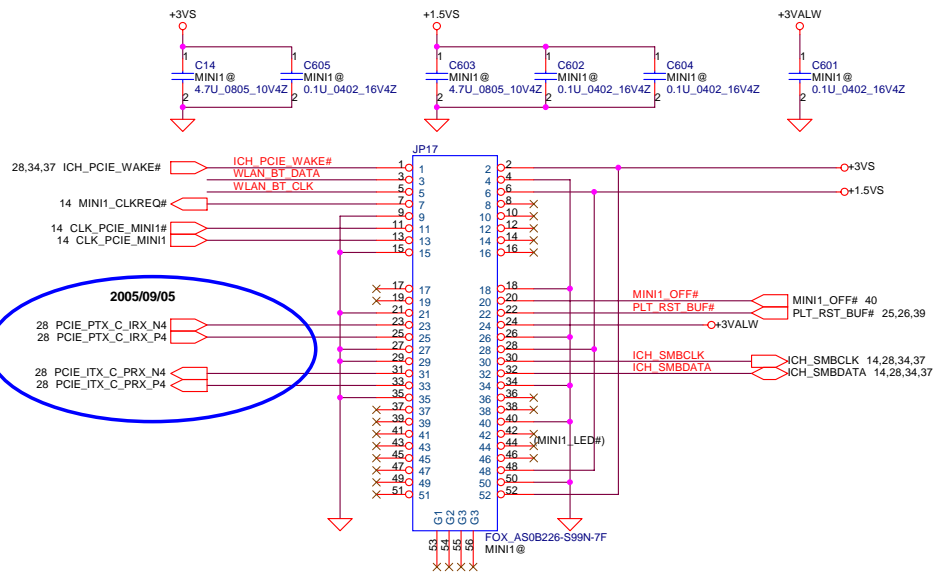
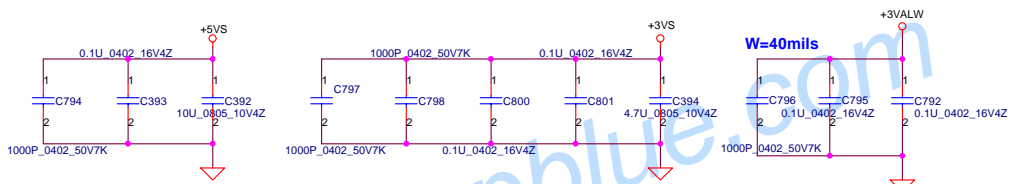


revised for BCM4401E(10/100)

- RJ45\_MIDI3+ R141 1 2 4401@ 0.0402 5%
- RJ45\_MIDI3- R137 1 2 4401@ 0.0402 5%
- RJ45\_MIDI2+ R144 1 2 4401@ 0.0402 5%
- RJ45\_MIDI2- R143 1 2 4401@ 0.0402 5%



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Size	Document Number	Rev		0.3	
B	HBL50 LA-2921P				
Date:	Friday, November 11, 2005	Sheet	35	of	59

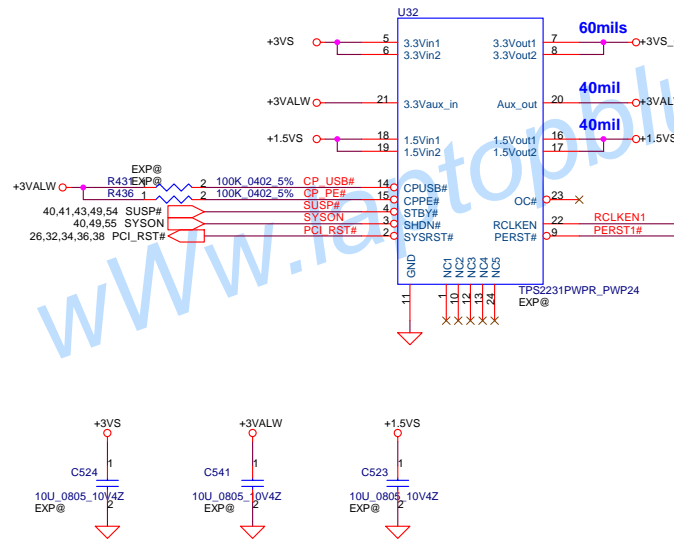


**Mini Card Power Rating**

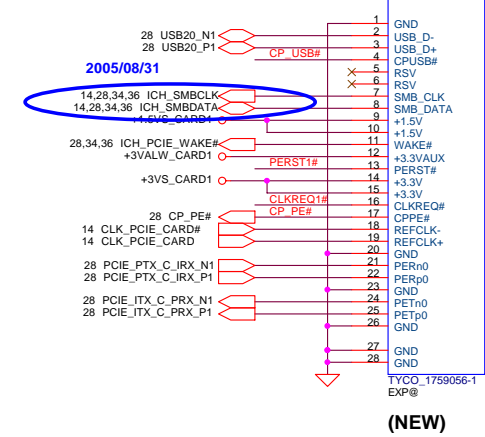
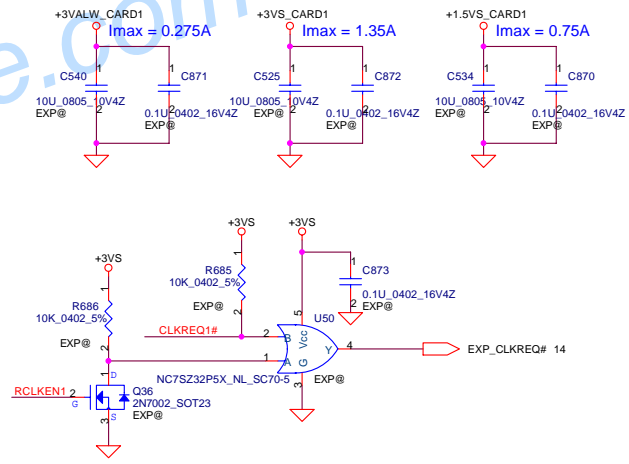
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	Normal
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

2005/09/27 modified.  
 Base on OPTION GTM351E Datasheet Rev0.1  
**Vcc 3.3V +/- 8%**  
**Peak Icc 2750mA**  
**with max supply droop 50mA**  
**Average Icc 1000mA**

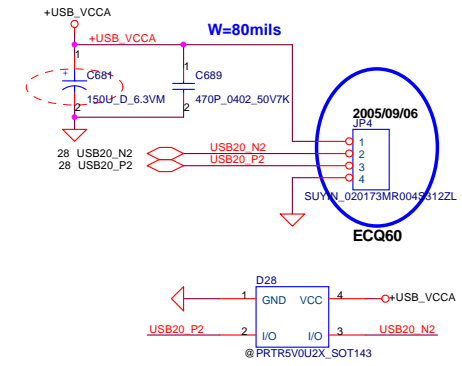
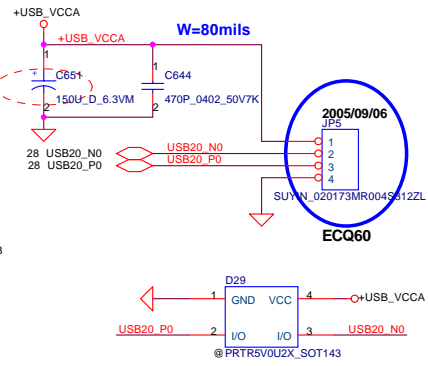
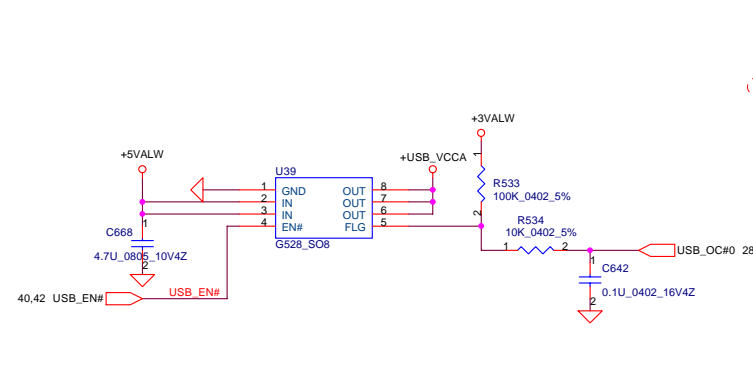
# New Card Power Switch



# New Card Socket (Left)

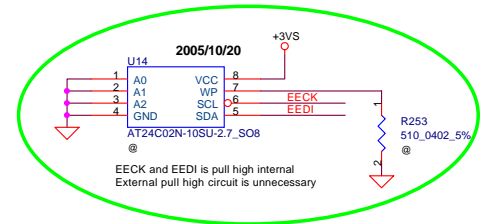
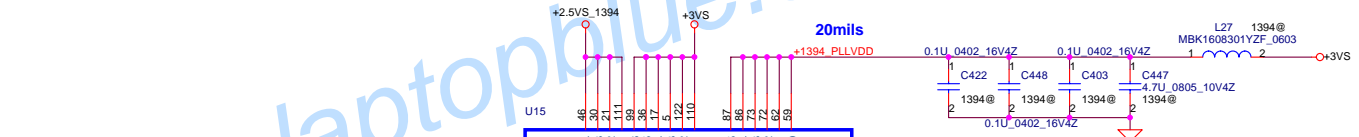
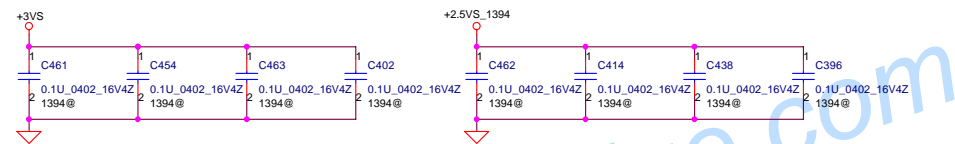


# USB CONN. 1 & 2

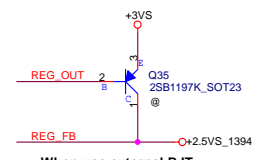
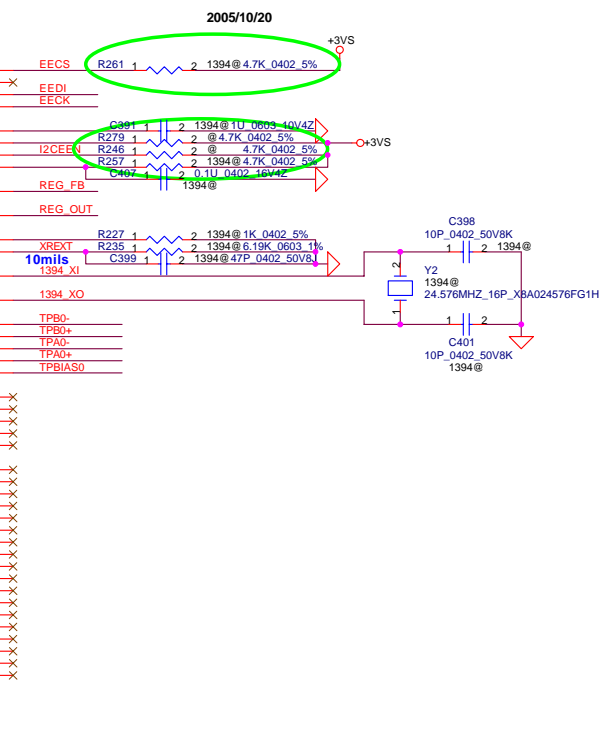
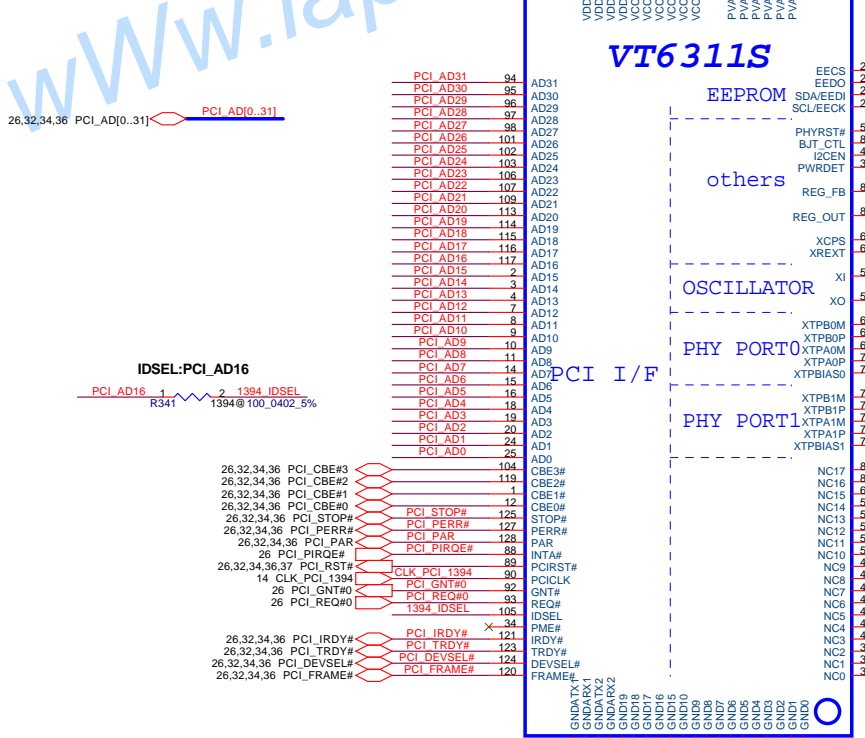


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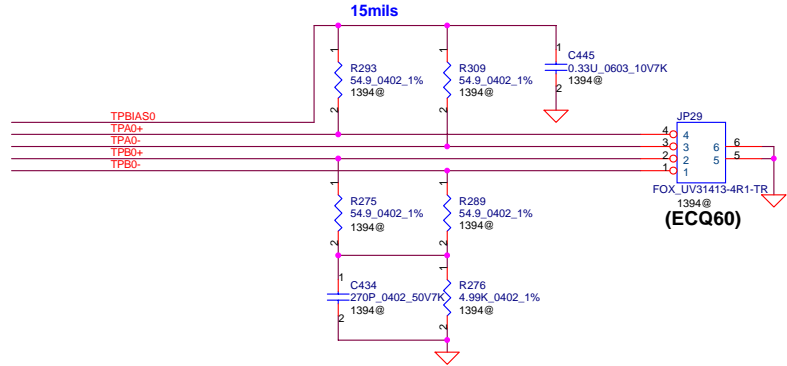
Compal Electronics, Inc.		
Title NEW CARD SOCKET		
Size B	Document Number HBL50 LA-2921P	Rev 0.3
Date:	Friday, November 11, 2005	Sheet 37 of 59



When use external EEPROM  
Populate U14, R246, R253  
Un-populate R261



When use external BJT  
Populate Q35, R279

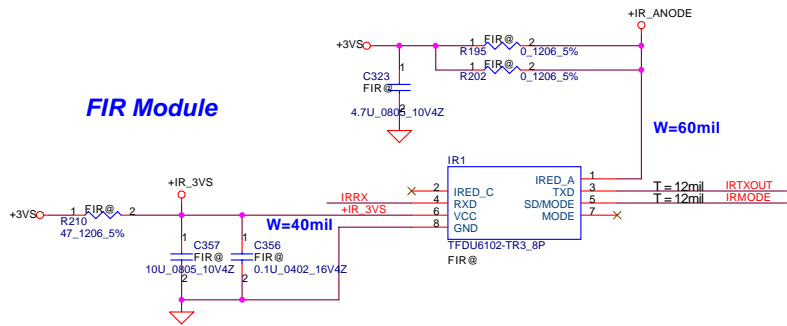
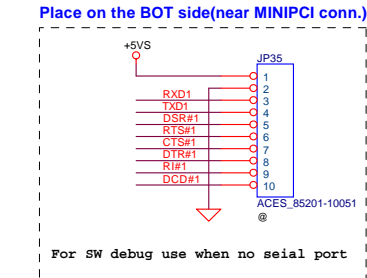
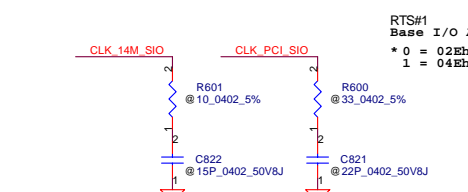
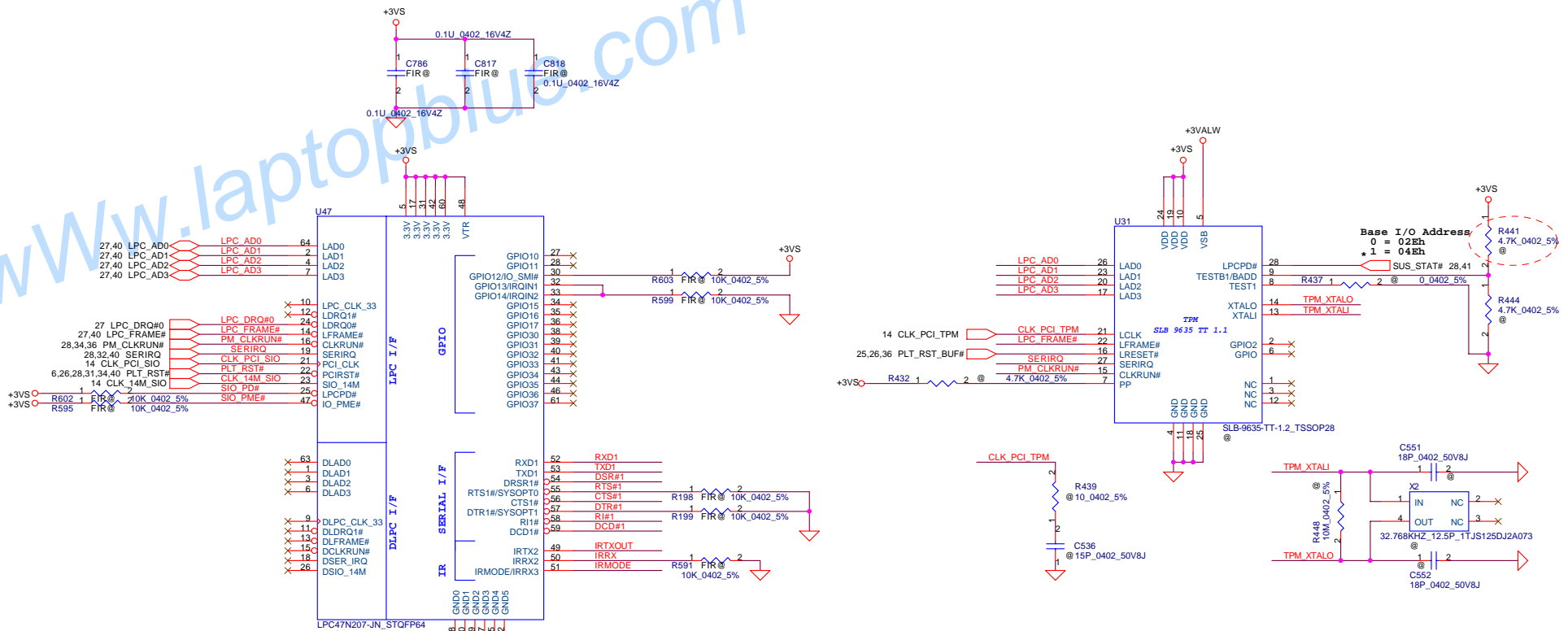


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			B	HBL50 LA-2921P	0.3
			Date:	Friday, November 11, 2005	Sheet 38 of 59



# SUPER I/O SMsC LPC47N207

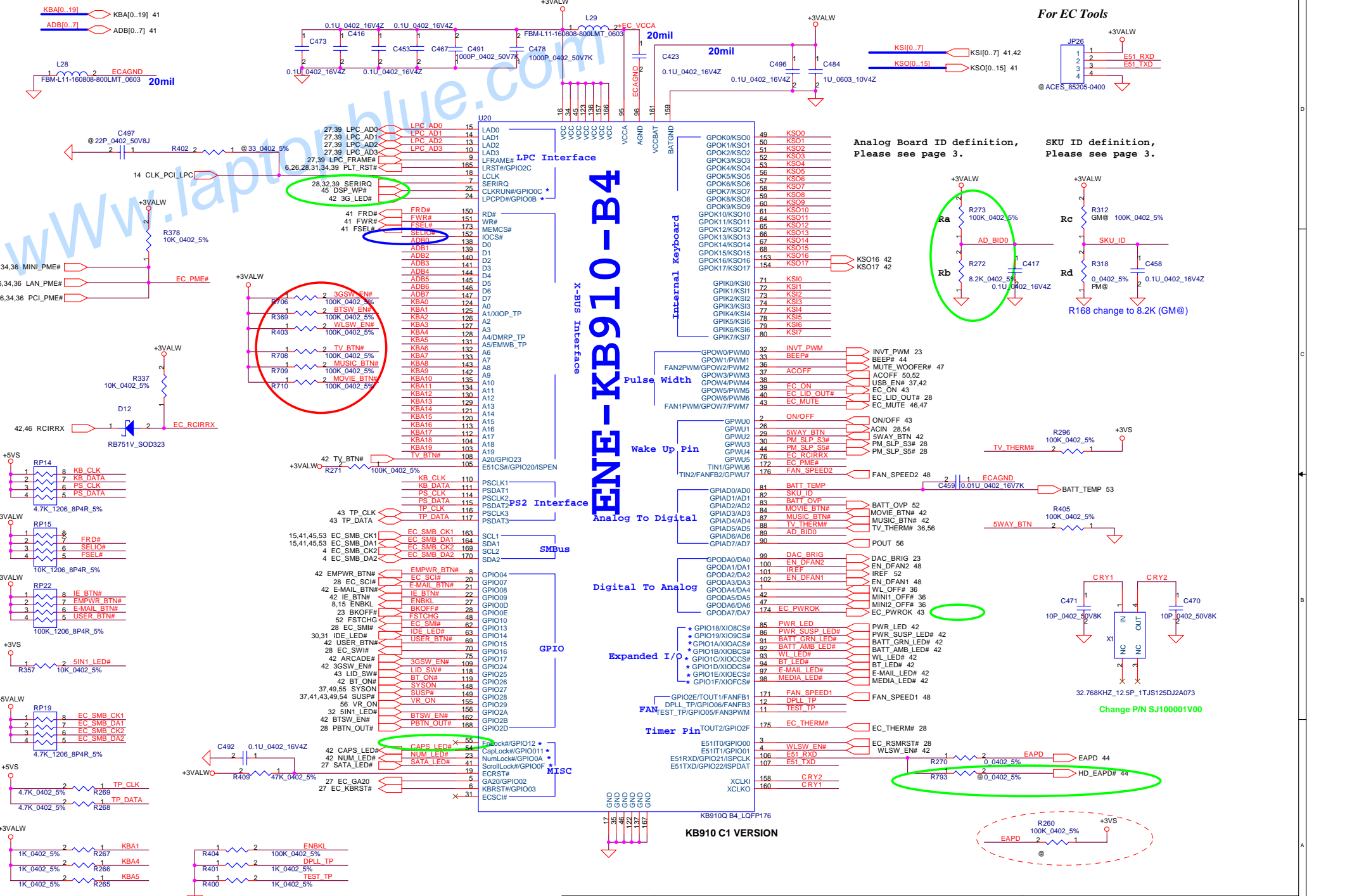
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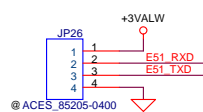
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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title
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Date: Friday, November 11, 2005				Sheet 39 of 59

# ENE-KB910-B4

- Xbus Interface

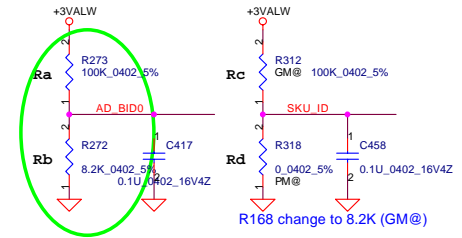


For EC Tools



Analog Board ID definition, Please see page 3.

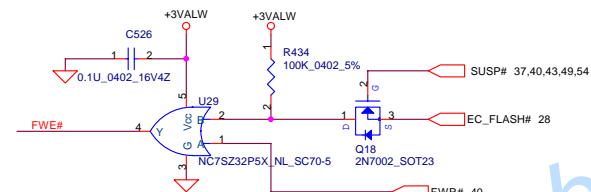
SKU ID definition, Please see page 3.



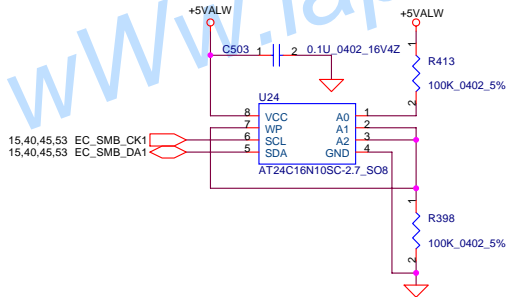
R168 change to 8.2K (GM@)

KB910 C1 VERSION

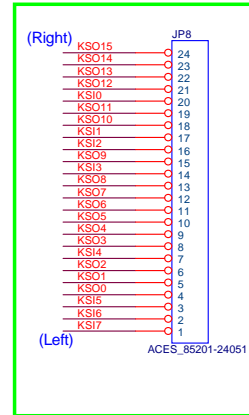
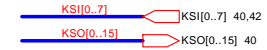
Security Classification	Compal Secret Data			Title	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	EC ENE KB910	
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Size	Document Number	Rev			
B	HBL50 LA-2921P	0.3			
Date:	Friday, November 11, 2005	Sheet	40	of	59



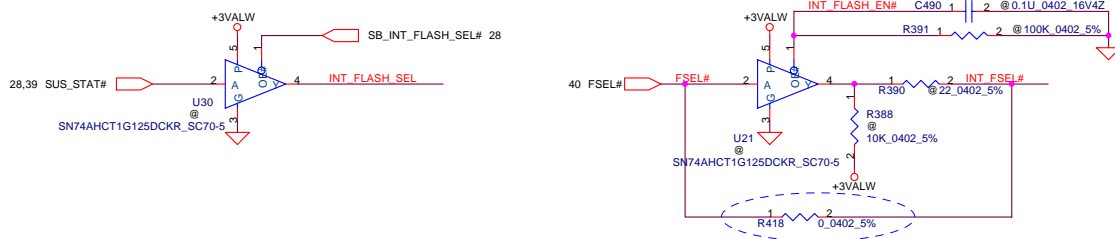
Check PCB Footprint



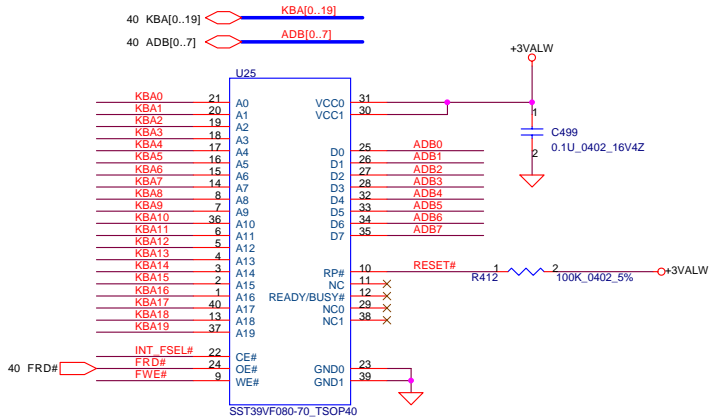
INT\_KBD Conn.



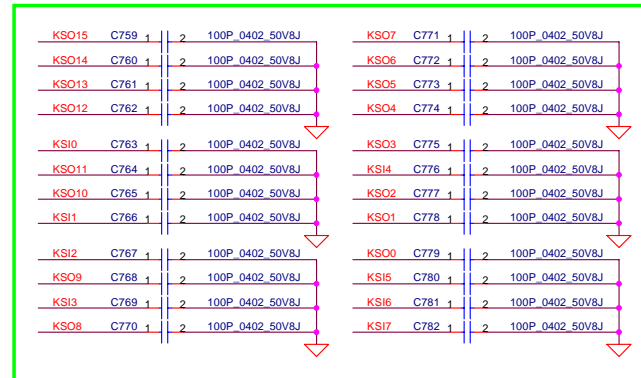
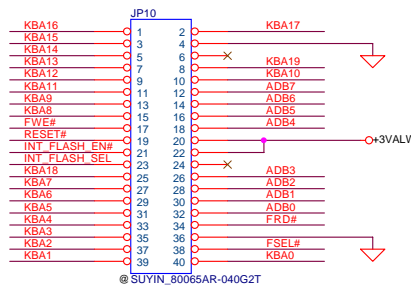
FOR DEBUG ONLY



1MB Flash ROM

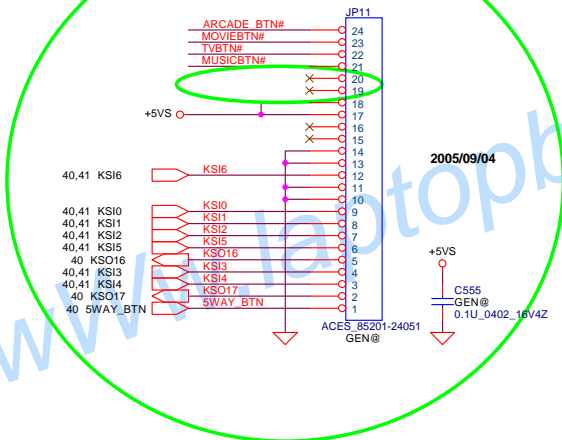


1MB ROM Socket

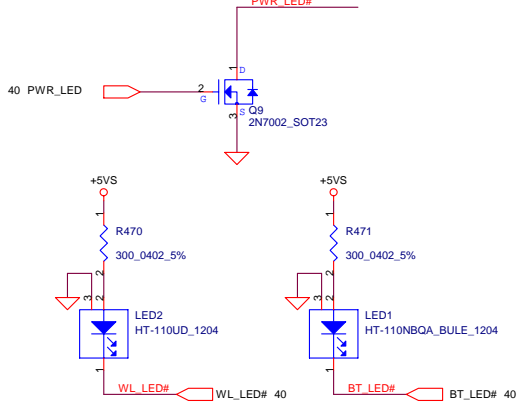
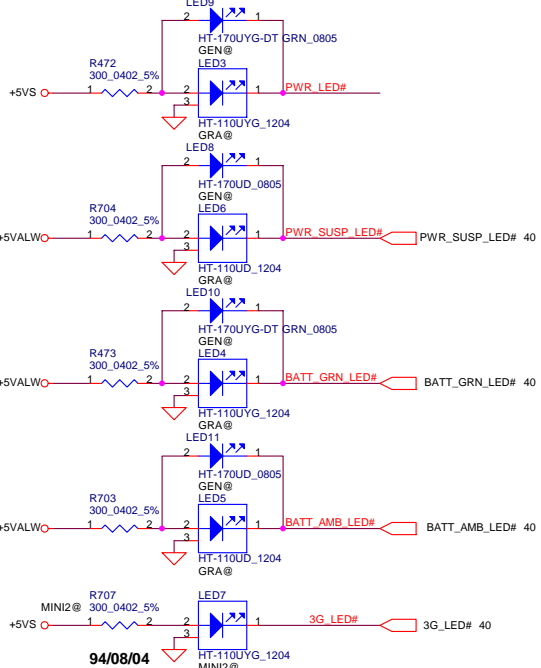
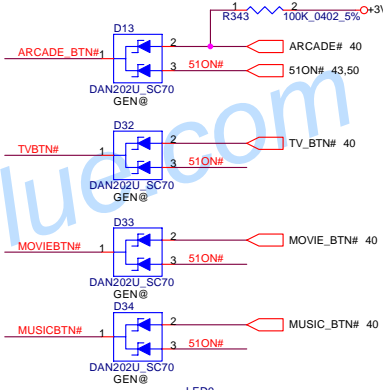


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Size	Document Number	Rev		Date	
B	HBL50 LA-2921P	0.3		Friday, November 11, 2005	
		Sheet		41 of 59	

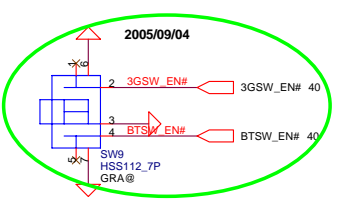
**To CD-PLAY/B Conn.**



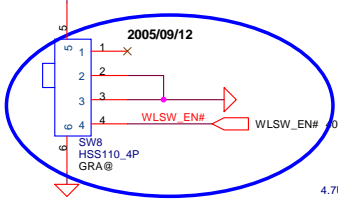
2005/09/04



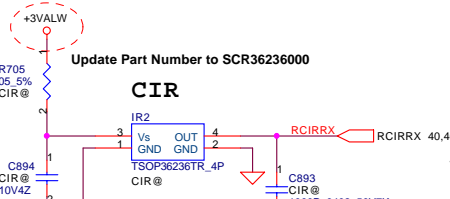
**BT\_SW & 3G\_SW**



**WL\_SW**

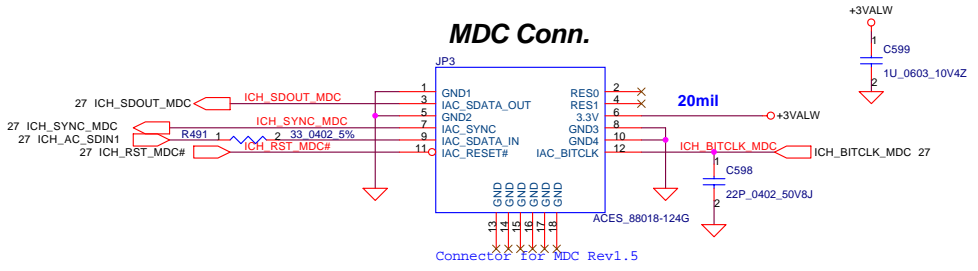


94/08/04

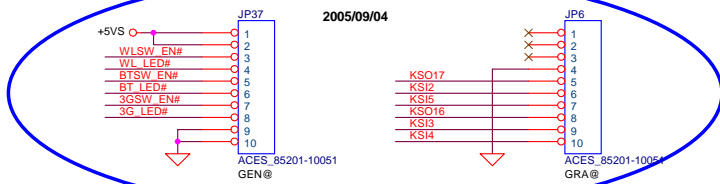


Update Part Number to SCR36236000

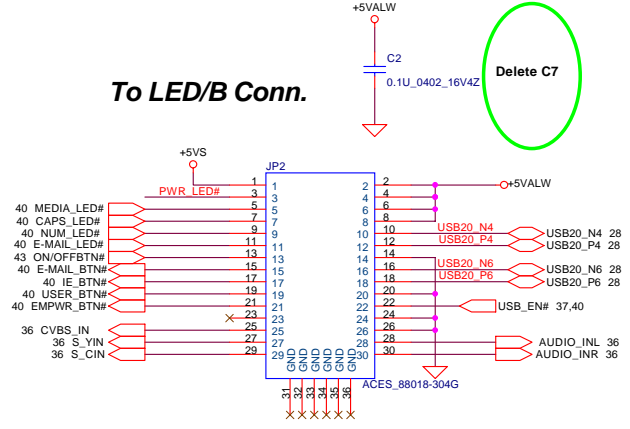
**MDC Conn.**



2005/09/04

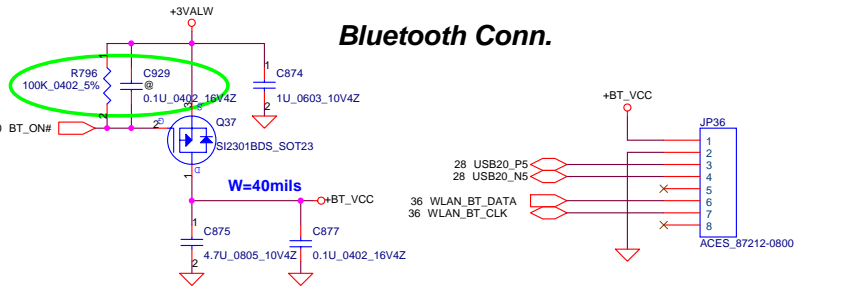


**To LED/B Conn.**



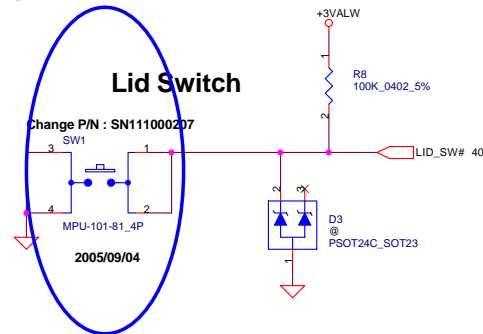
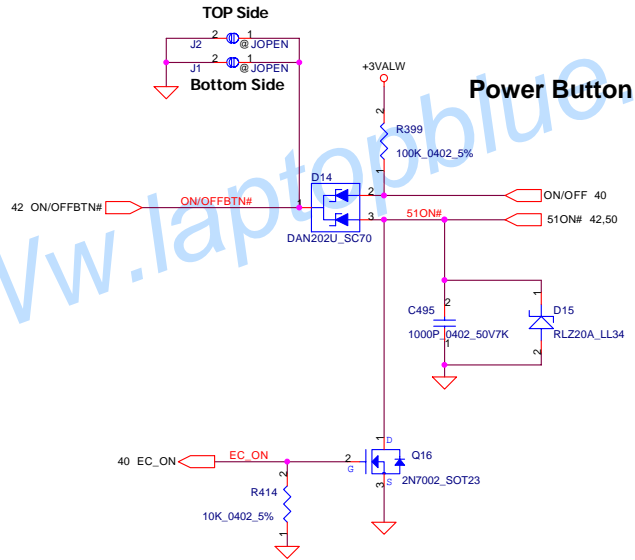
Delete C7

**Bluetooth Conn.**



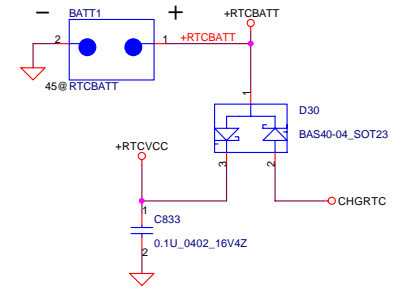
Geneva		Grapevine	
KSO16	KSO17	KSO16	KSO17
KSIO VOL_UP	KSIO7 LEFT		
KSII RIGHT	VOL_DOWN		
KSII2 PLAY	ENTER	KSII2 PLAY	
KSII3 STOP		KSII3 STOP	VOL_UP
KSII4 NEXT		KSII4 NEXT	VOL_DOWN
KSII5 REV		KSII5 REV	ARCADE_TV
KSII6	RECORD		

**ON/OFF switch**

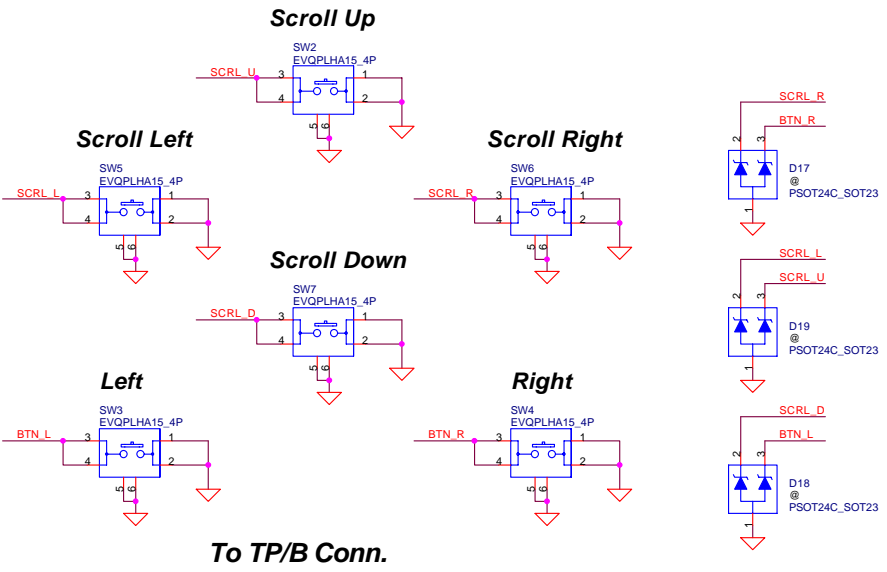
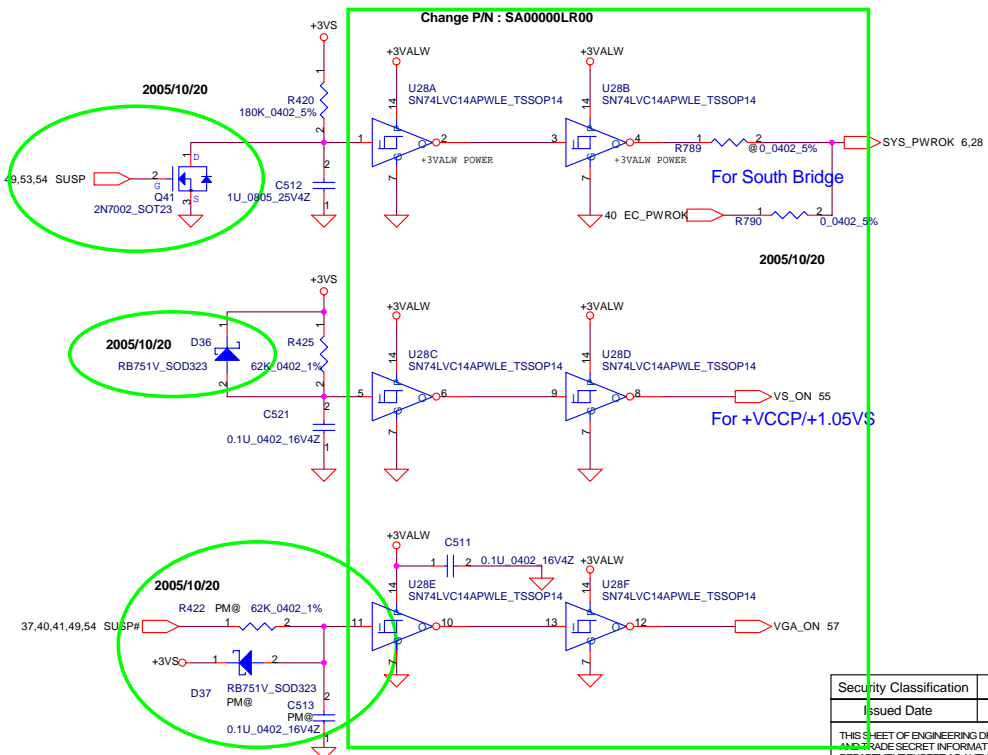


Change BATT1 P/N : SP093PA0200 (Panasonic)  
SP093MX0000 (MAXELL)

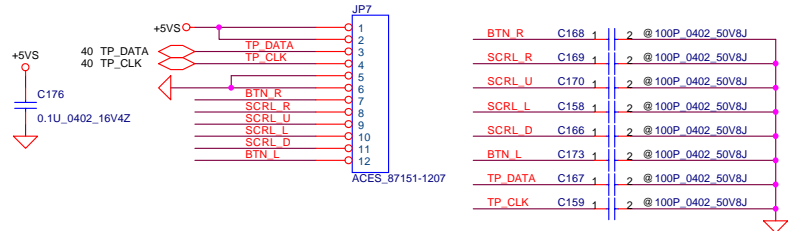
**RTC Battery**



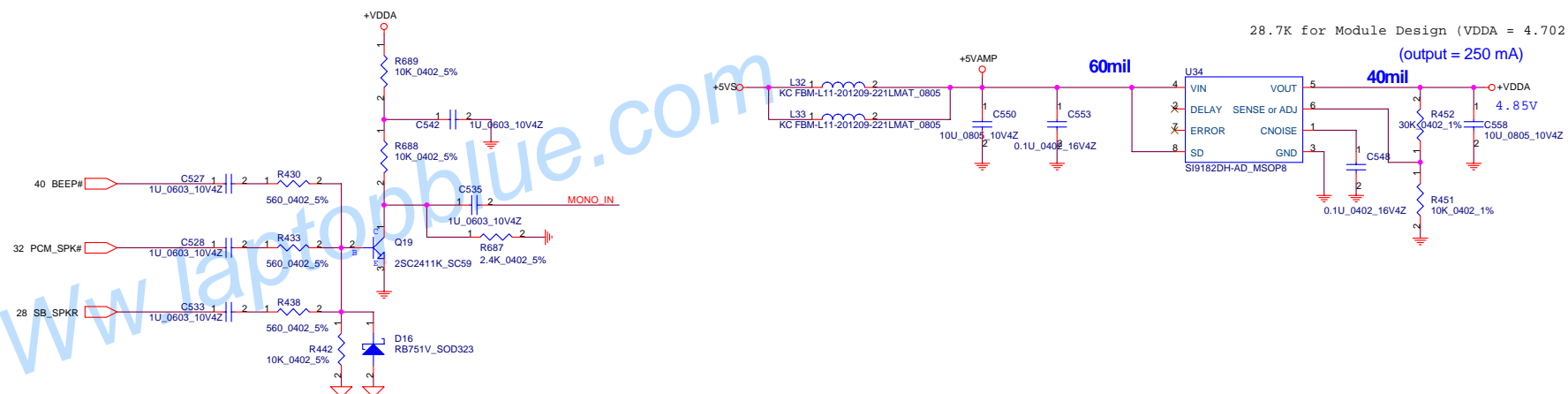
**Power ON Circuit**



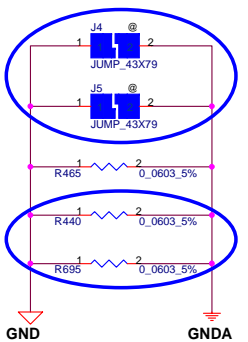
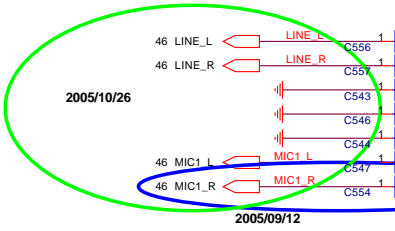
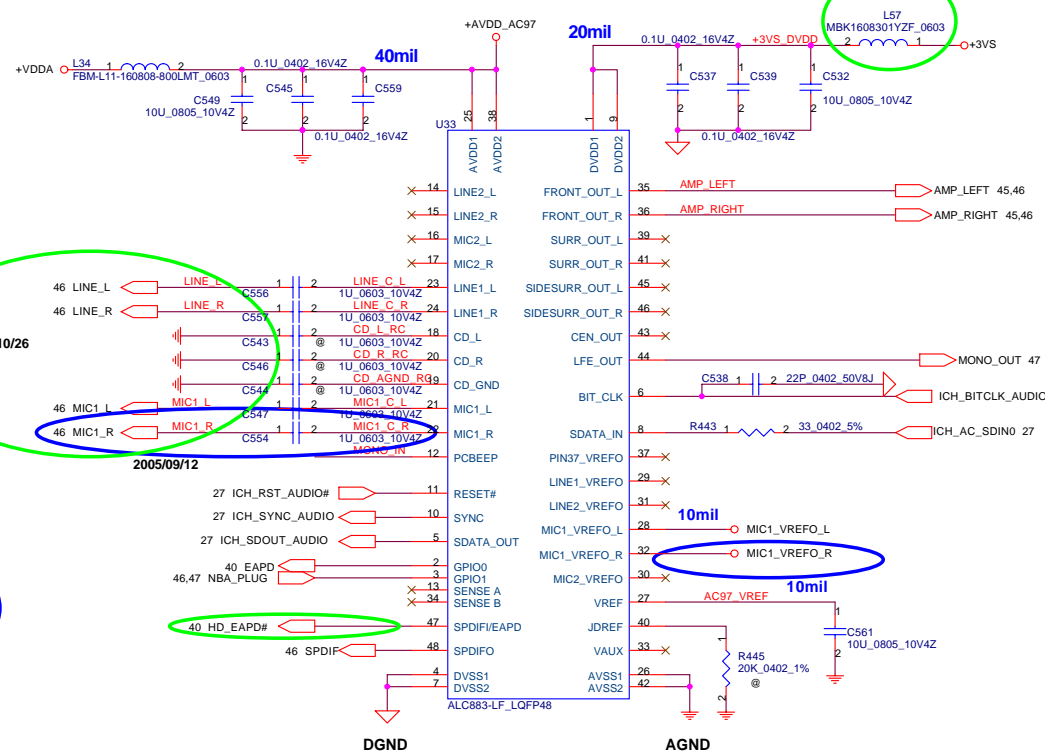
**To TP/B Conn.**



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	Deciphered Date	2006/06/20	
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Size B	Document Number	HBL50 LA-2921P	
Date:	Friday, November 11, 2005	Sheet	43 of 59
Rev	0.3		



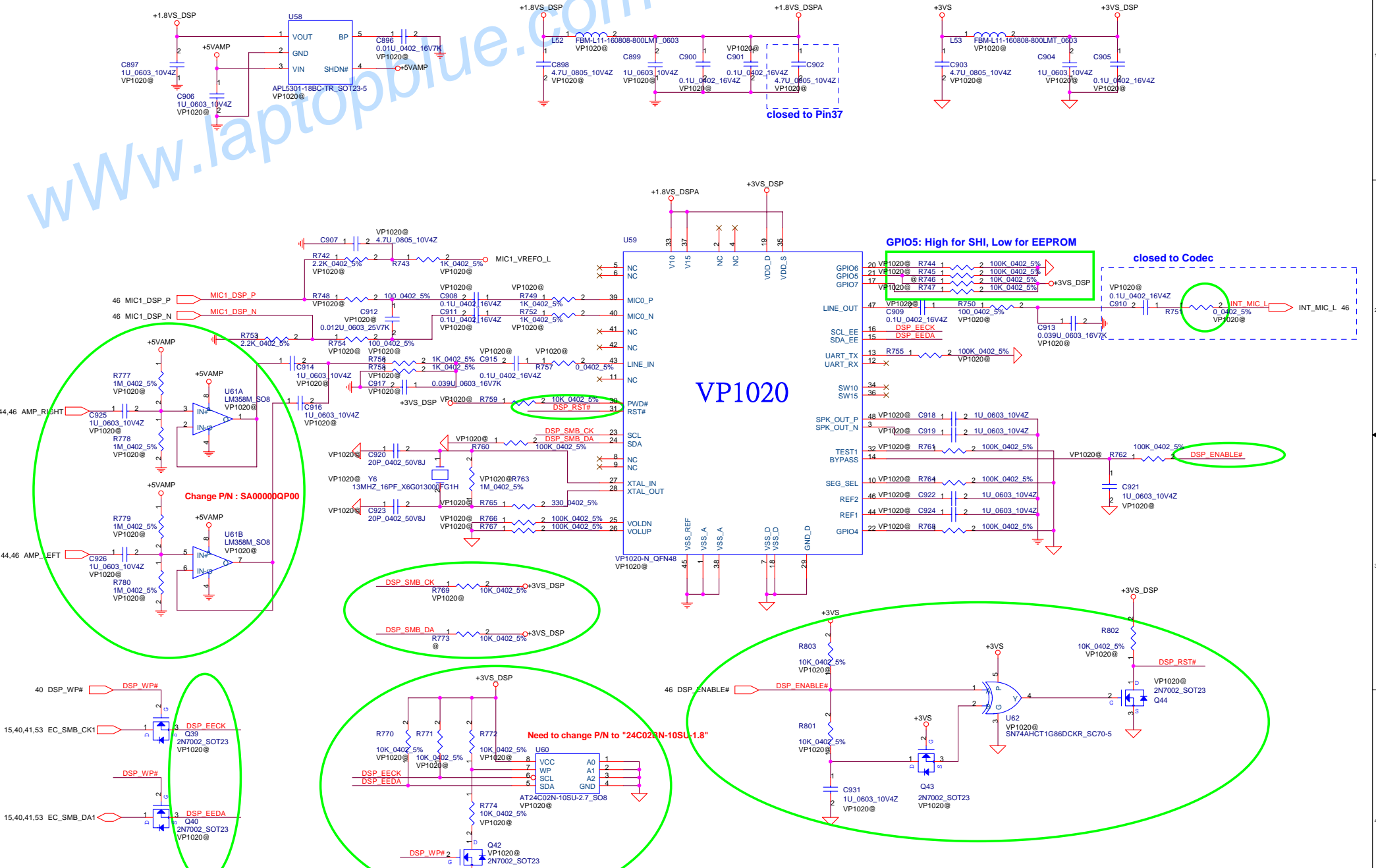
### HD Audio Codec



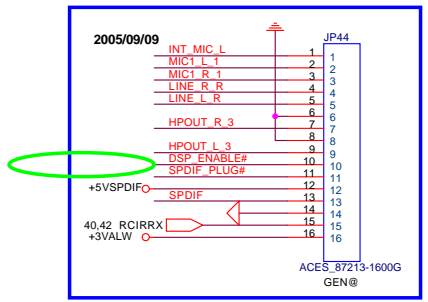
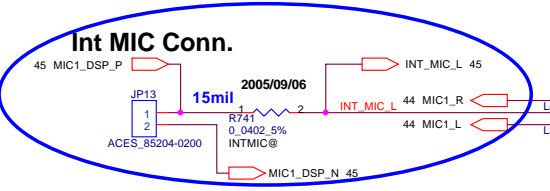
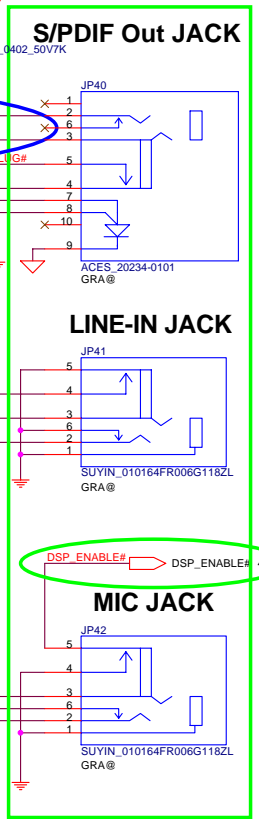
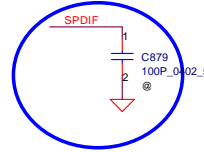
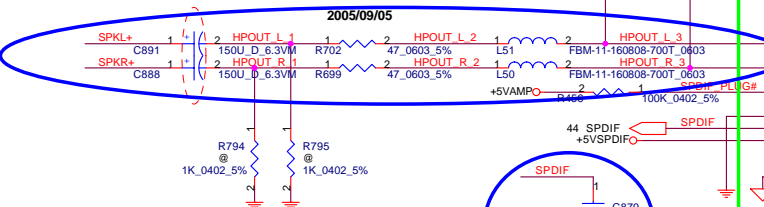
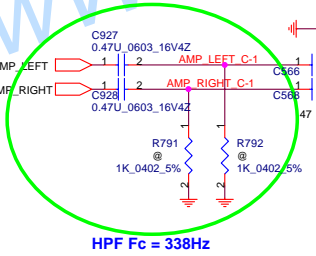
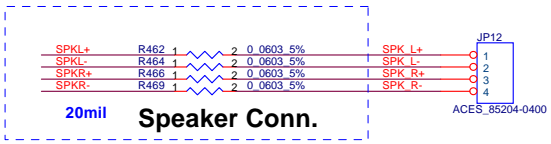
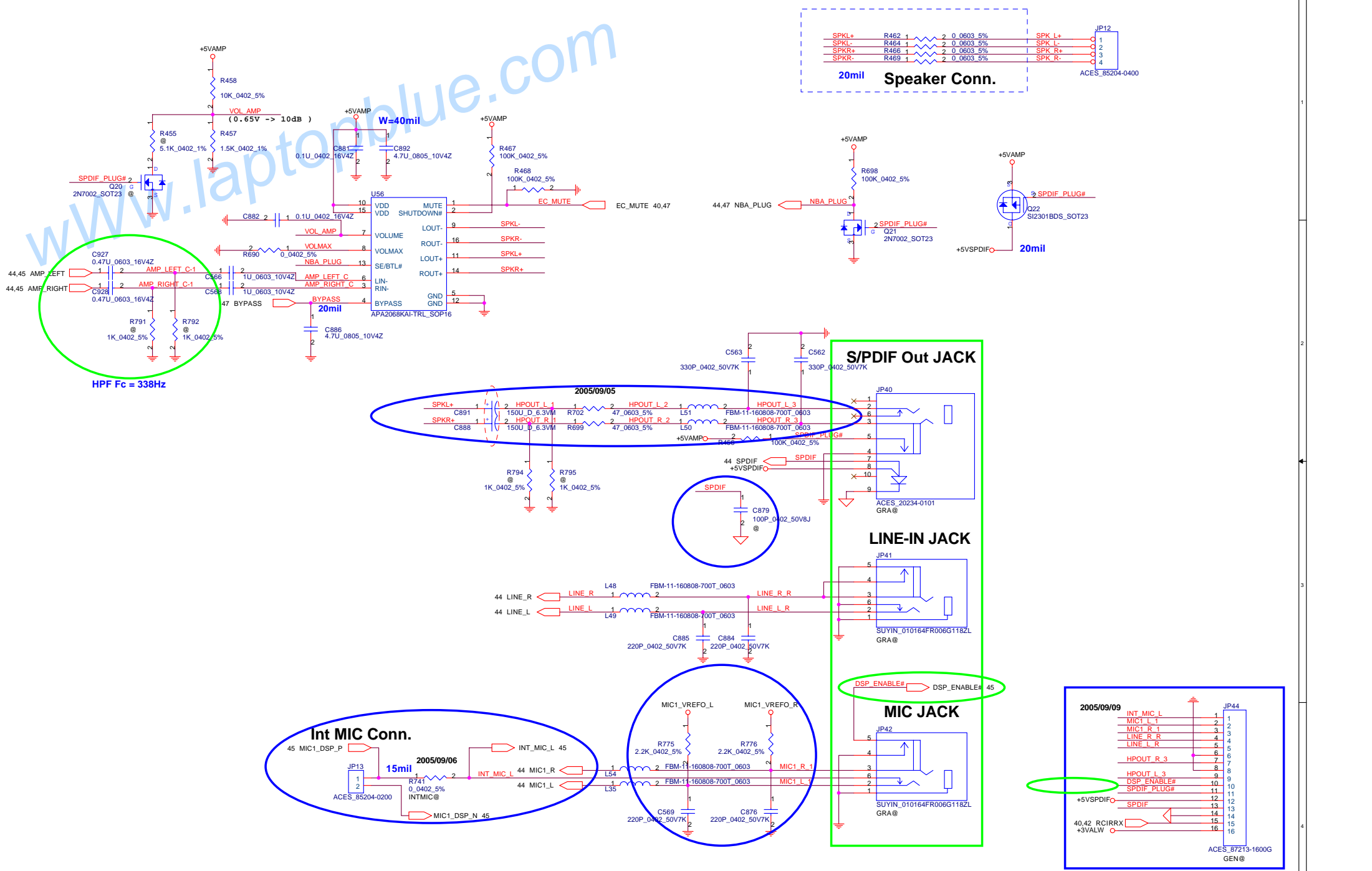
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Issued Date	2005/06/20	Deciphered Date	2006/06/20	HD Audio Codec ALC883
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Document Number			Rev	0.3
HBL50 LA-2921P			Date:	Friday, November 11, 2005
Sheet 44			of 59	



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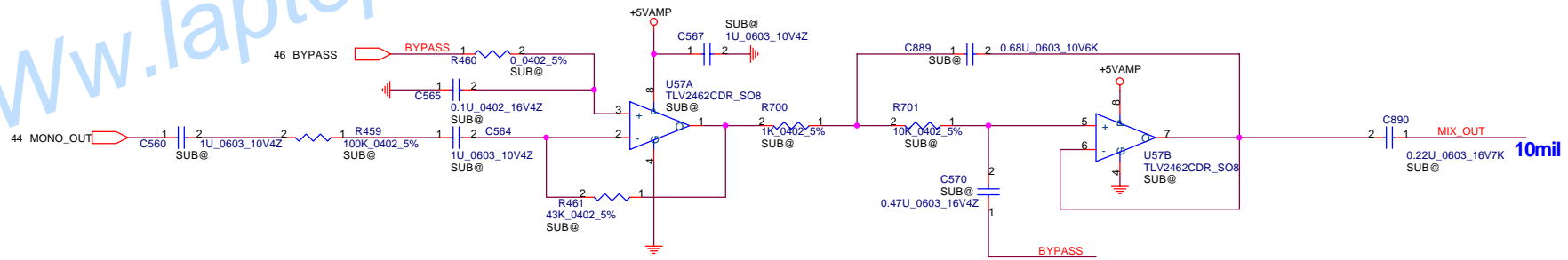


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				B	HBL50 LA-2921P
				Date:	Friday, November 11, 2005
				Sheet	45 of 59
				Rev	0.3



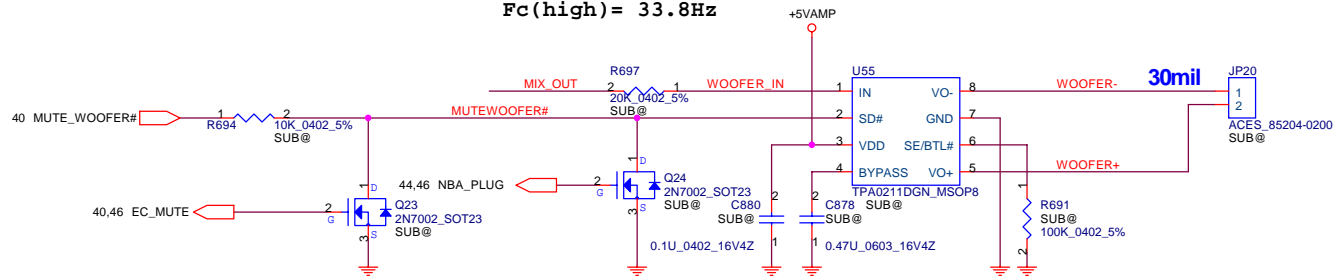
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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Amplifier & Audio Jack	
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Size	B	Document Number	HBL50 LA-2921P	Rev	0.3
Date:	Friday, November 11, 2005	Sheet	46	of	59

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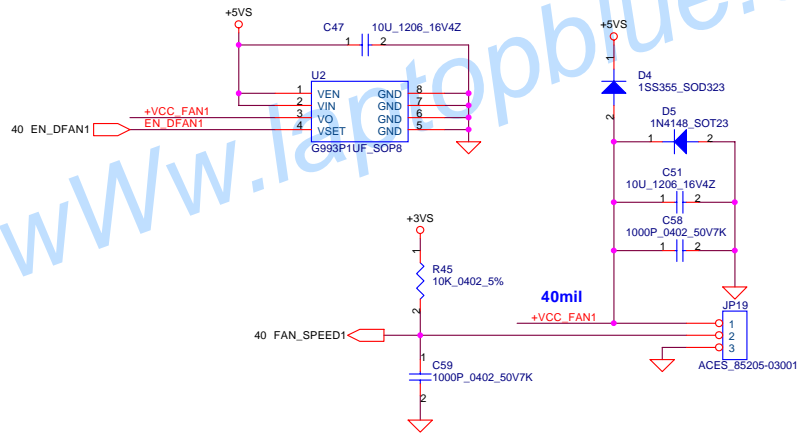
$f_o = 725 \text{ Hz}$

$F_c(\text{high}) = 33.8 \text{ Hz}$

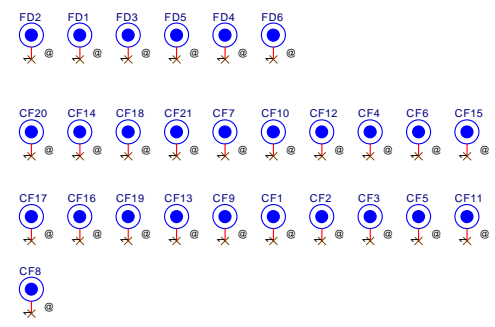
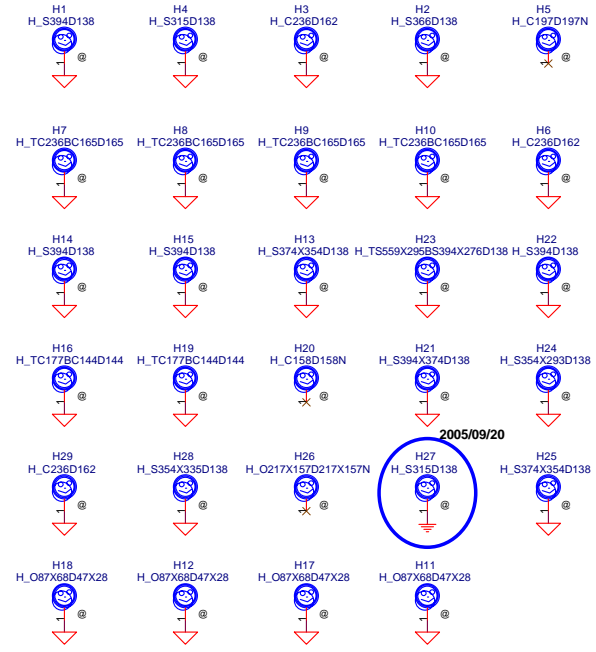
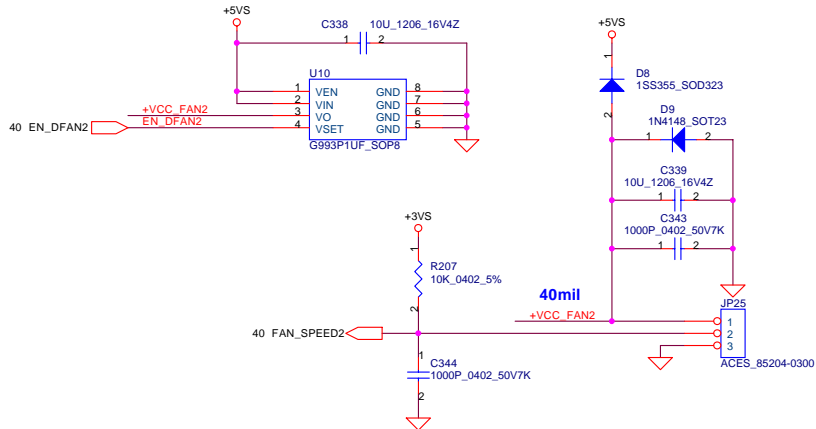


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Size B	Document Number			Rev	
	HBL50 LA-2921P			0.3	
Date:	Friday, November 11, 2005			Sheet	47 of 59

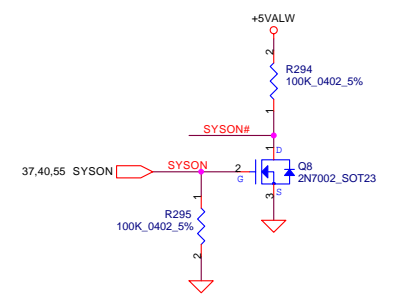
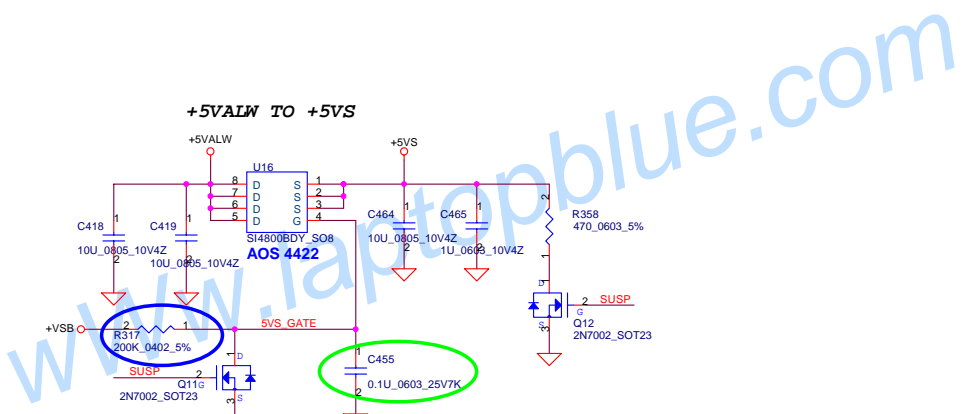
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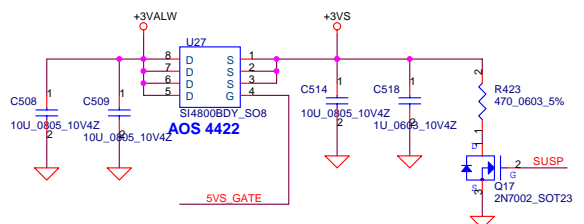
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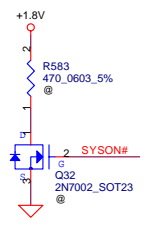
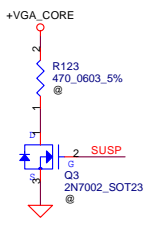
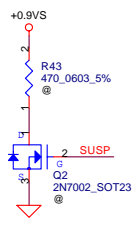
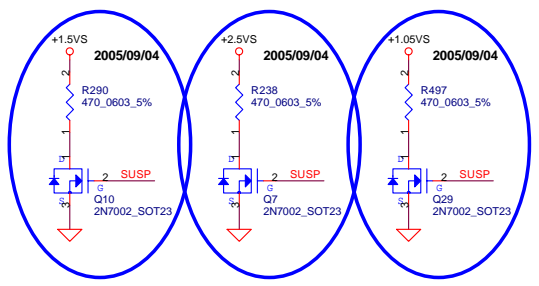
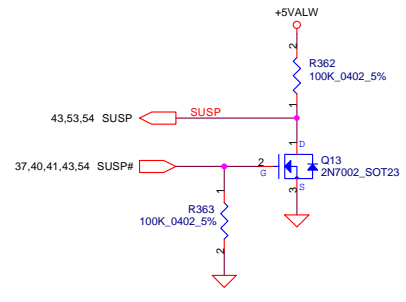
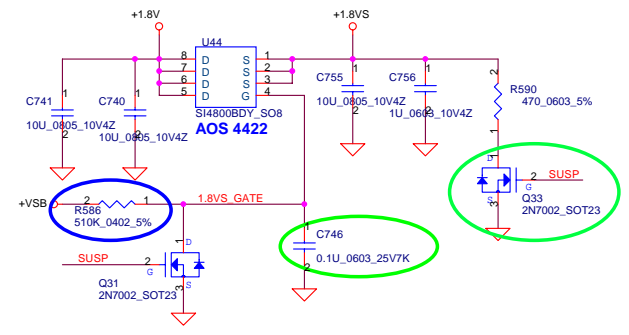
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Size	Document Number	Rev.		
B	HBL50 LA-2921P	0.3		
Date:	Friday, November 11, 2005	Sheet	48 of 59	



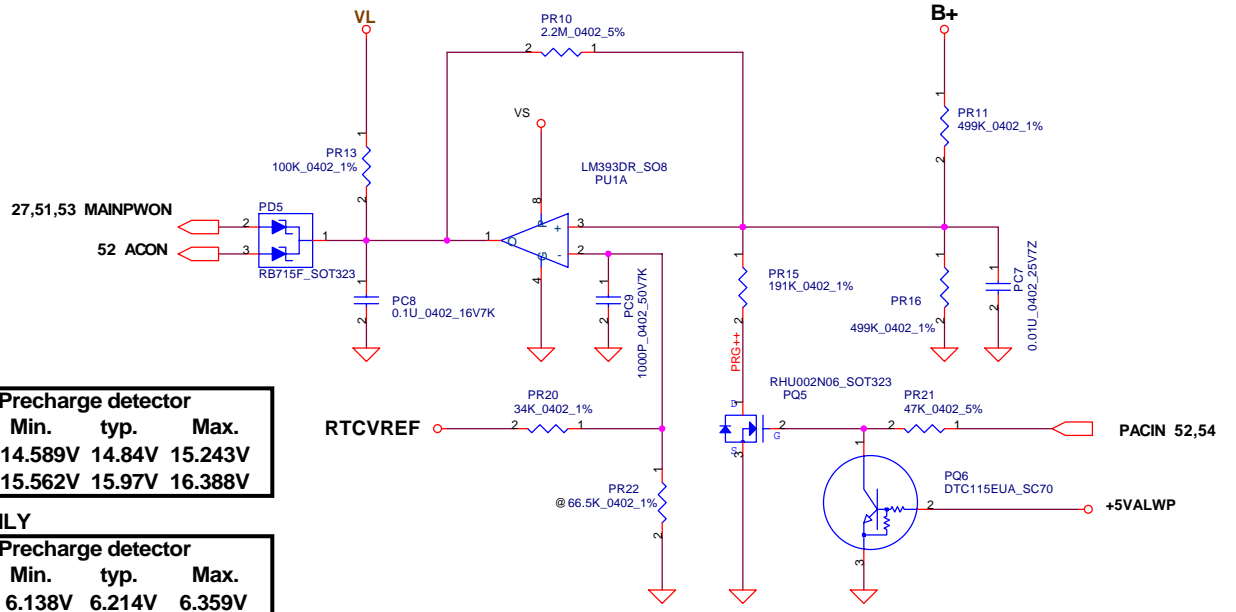
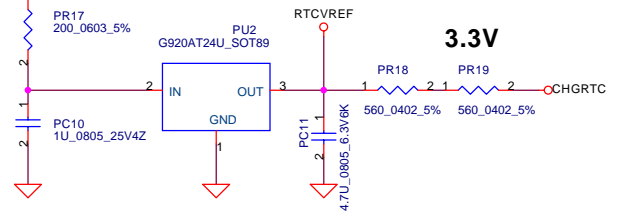
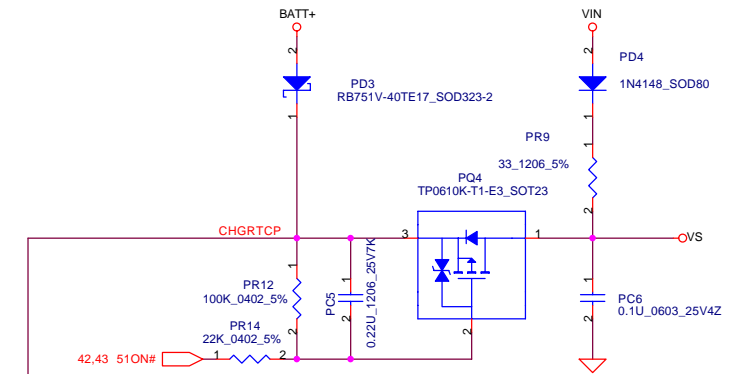
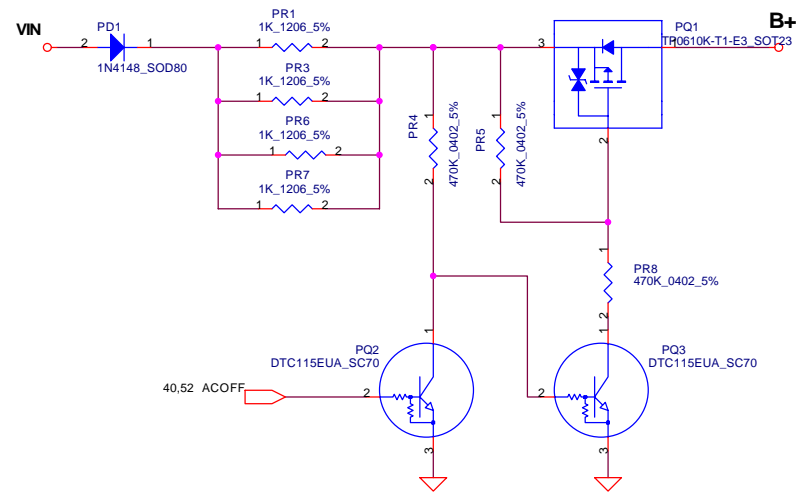
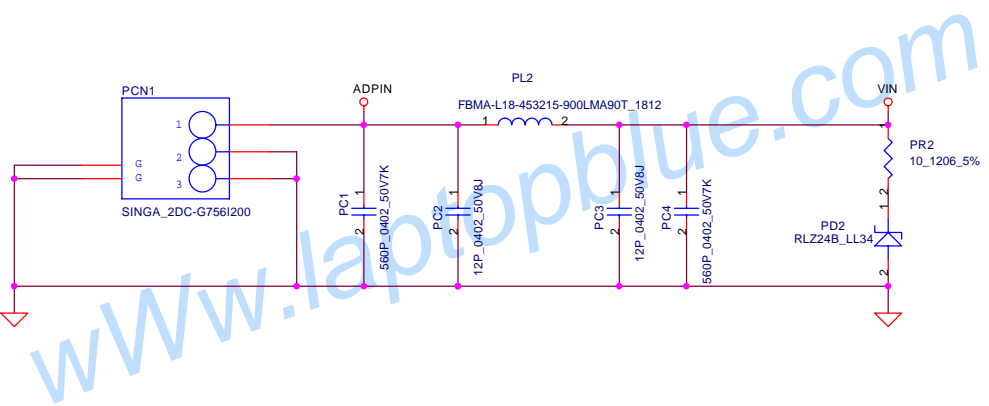
**+3VALW TO +3VS**



**+1.8V to +1.8VS**



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Size B	Document Number	HBL50 LA-2921P		Rev	0.3
Date:	Friday, November 11, 2005		Sheet	49	of 59



ACIN			
Precharge detector			
	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

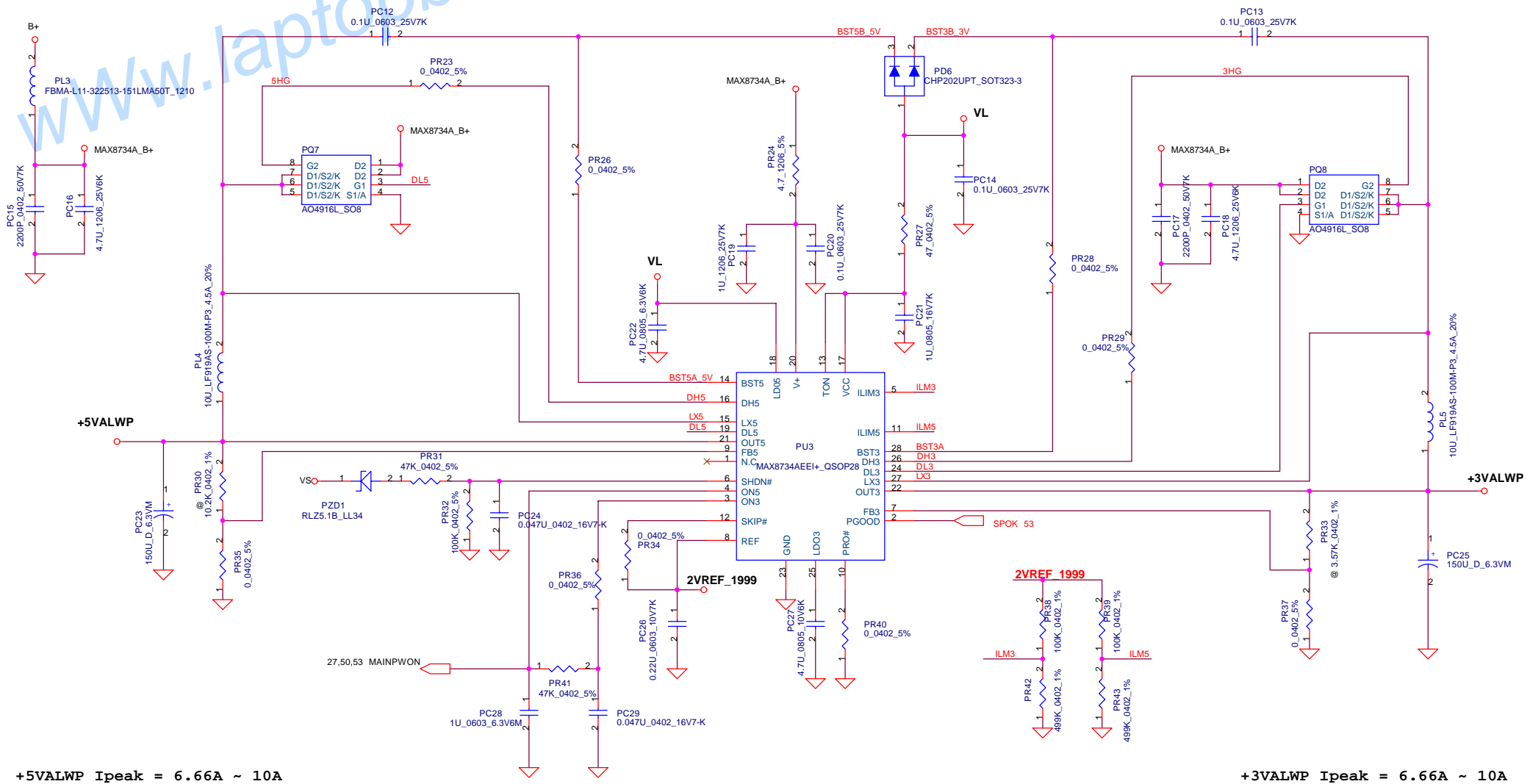
  

BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V

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				HBL50 LA-2921P
				Rev 0.2
				Date: Friday, November 11, 2005
				Sheet 50 of 59



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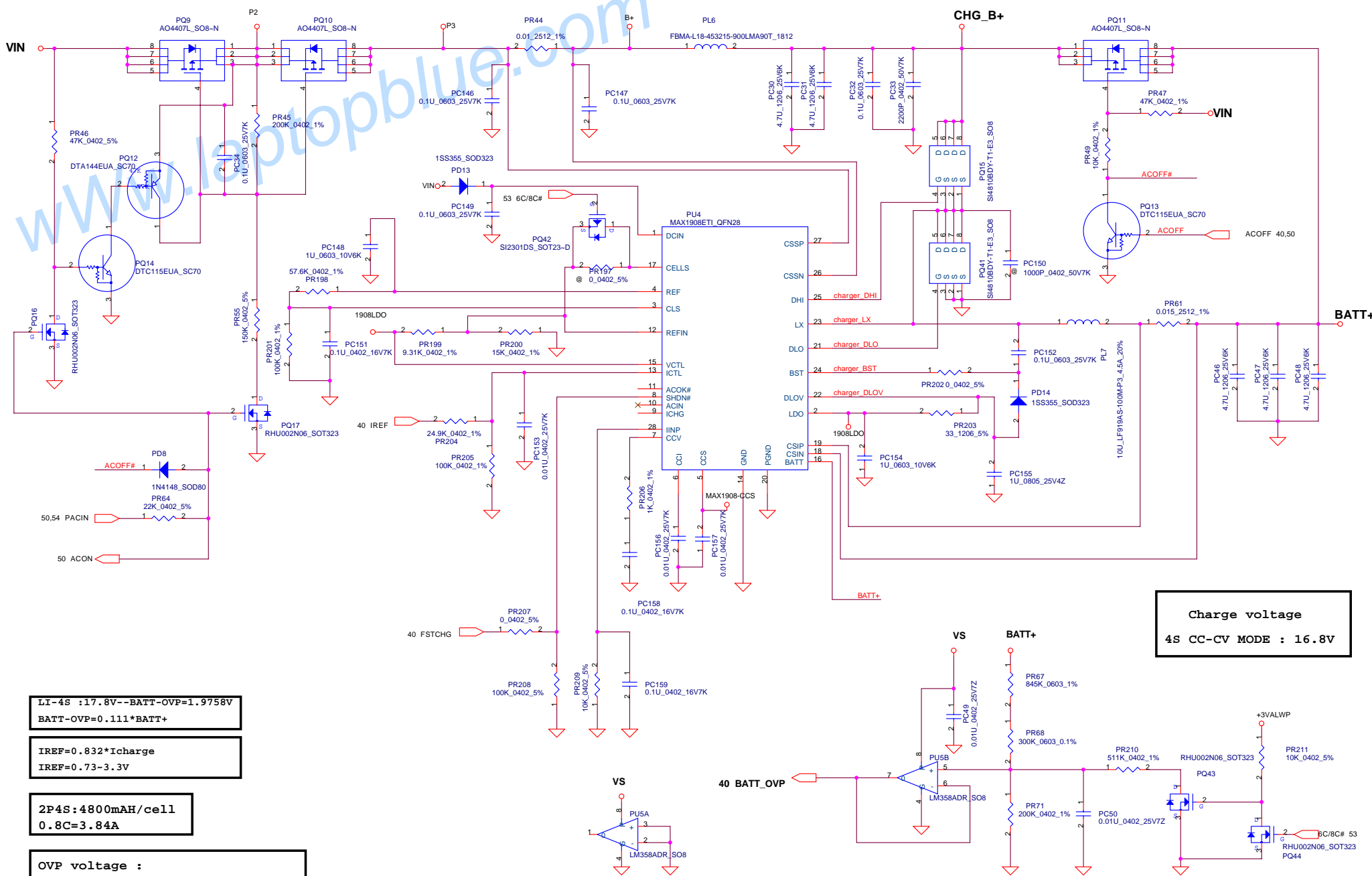


**+5VALWP Ipeak = 6.66A ~ 10A**

**+3VALWP Ipeak = 6.66A ~ 10A**

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				Custom	HBL50 LA-2921P
				Date:	Friday, November 11, 2005
				Sheet	51 of 59
				Rev	0.2

I<sub>adp</sub>=0~4.74A (90W)



Charge voltage  
4S CC-CV MODE : 16.8V

LI-4S : 17.8V--BATT-OVP=1.9758V  
BATT-OVP=0.111\*BATT+

IREF=0.832\*Icharge  
IREF=0.73~3.3V

2P4S: 4800mAh/cell  
0.8C=3.84A

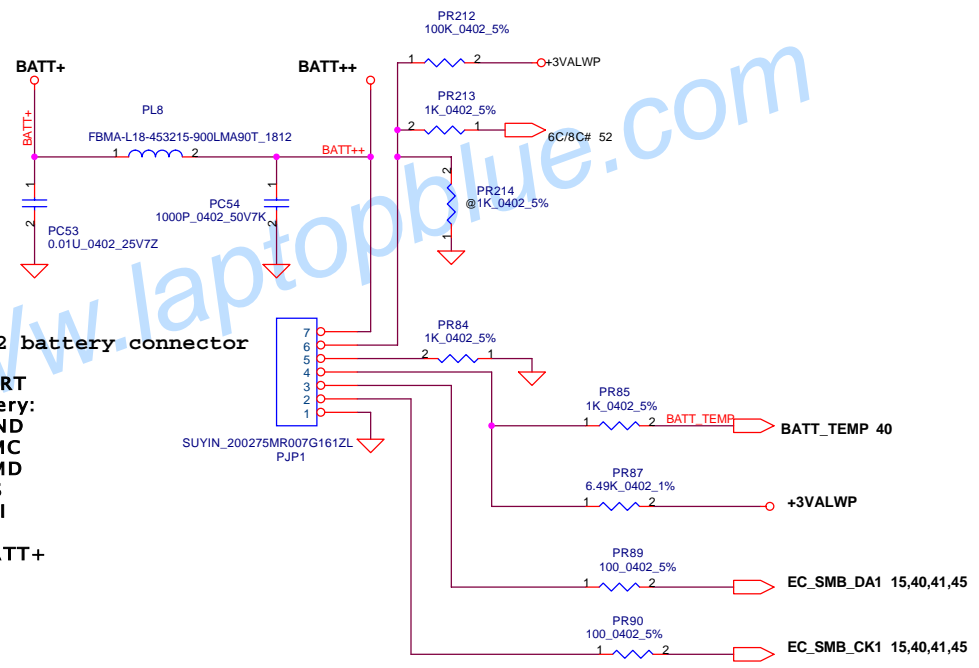
OVP voltage :  
LI-3S : 17.8V---BATT-OVP=1.9758V  
BATT-OVP=0.111\*BATT+

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Size	Document Number		Rev
B	HBL50 LA-2921P		0.2
Date:	Friday, November 11, 2005	Sheet	52 of 59

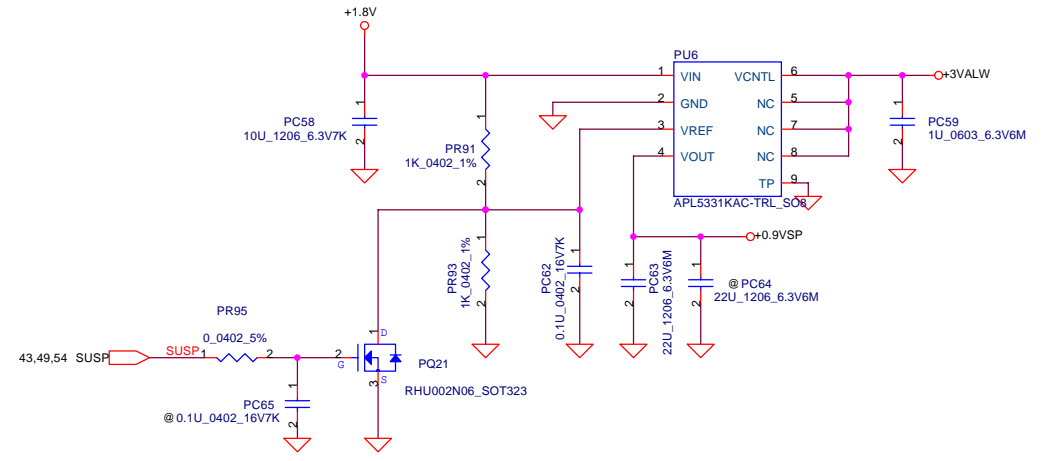
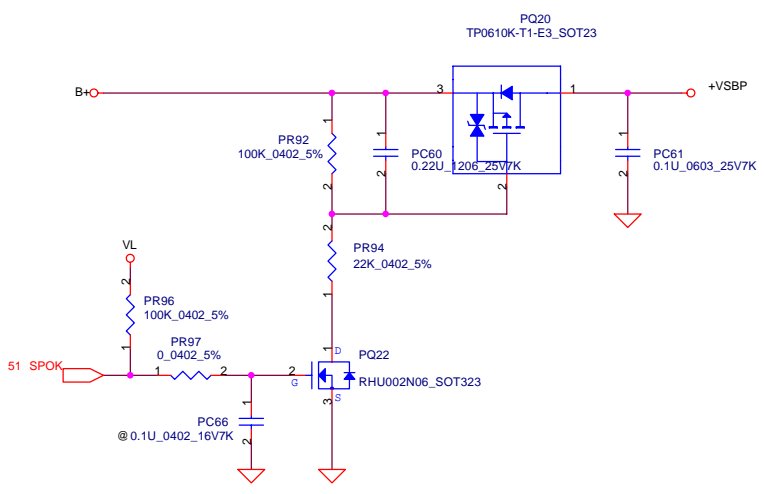
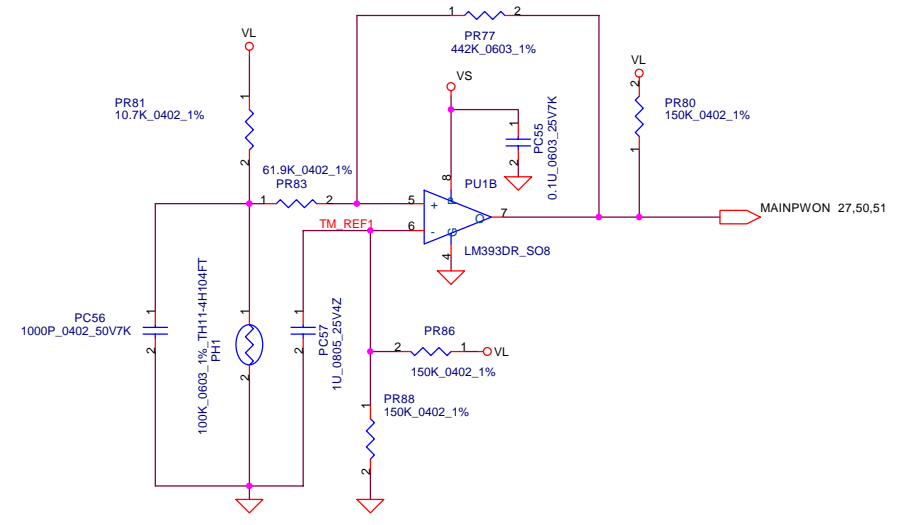
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**PJP2 battery connector**

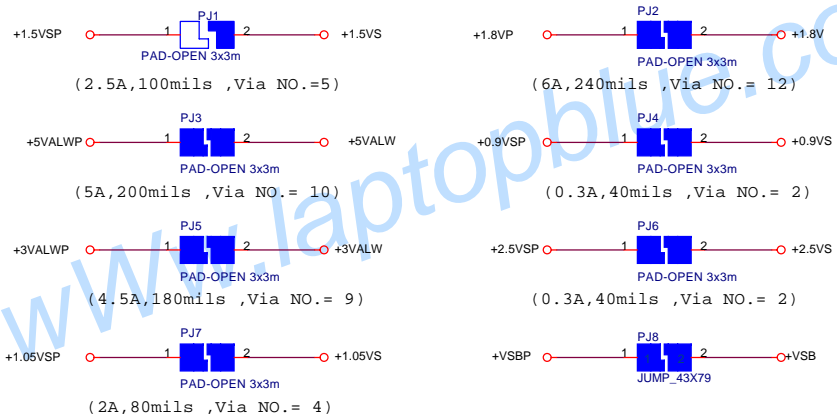
- SMART Battery:**  
 1.GND  
 2.SMC  
 3.SMD  
 4.TS  
 5.B/I  
 6.ID  
 7.BATT+



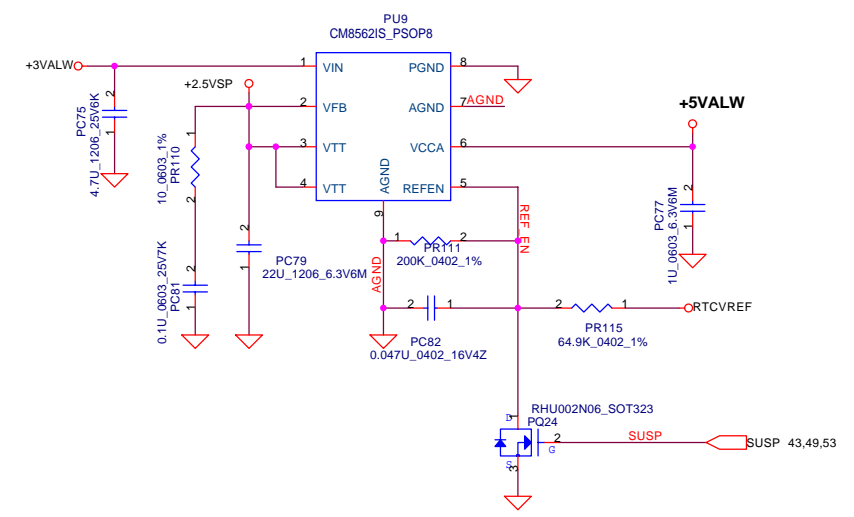
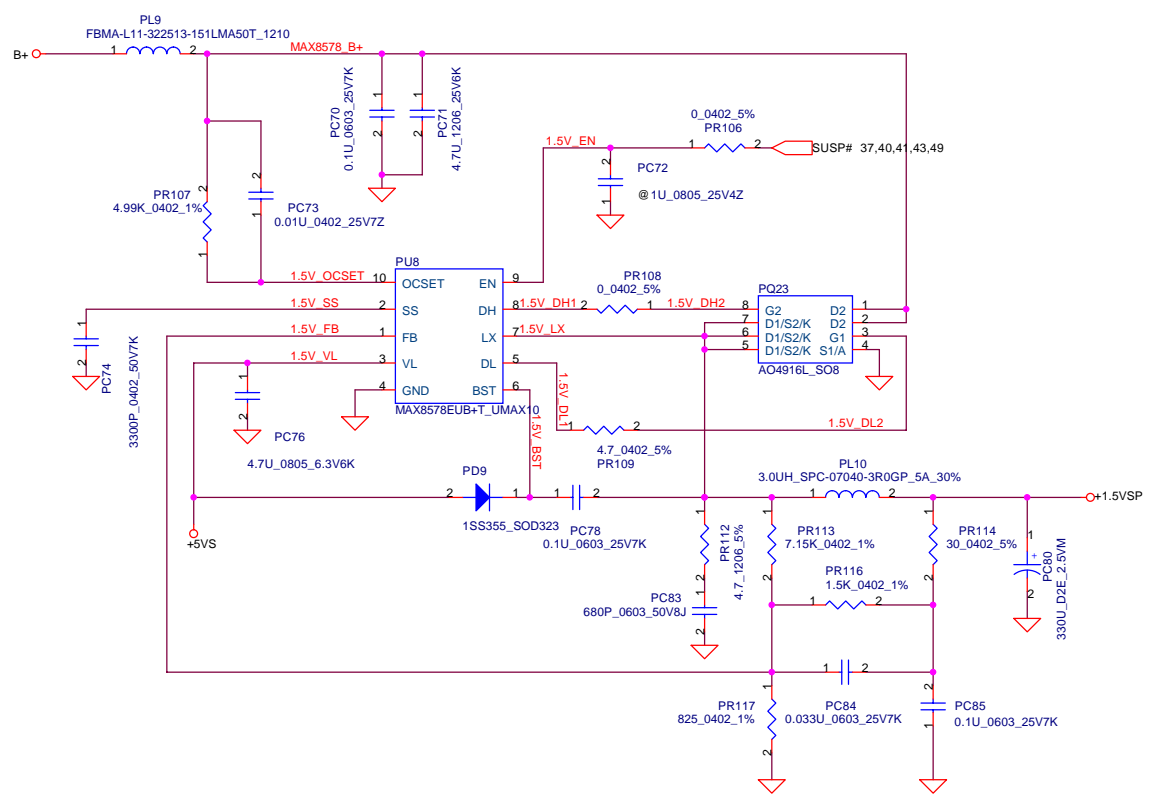
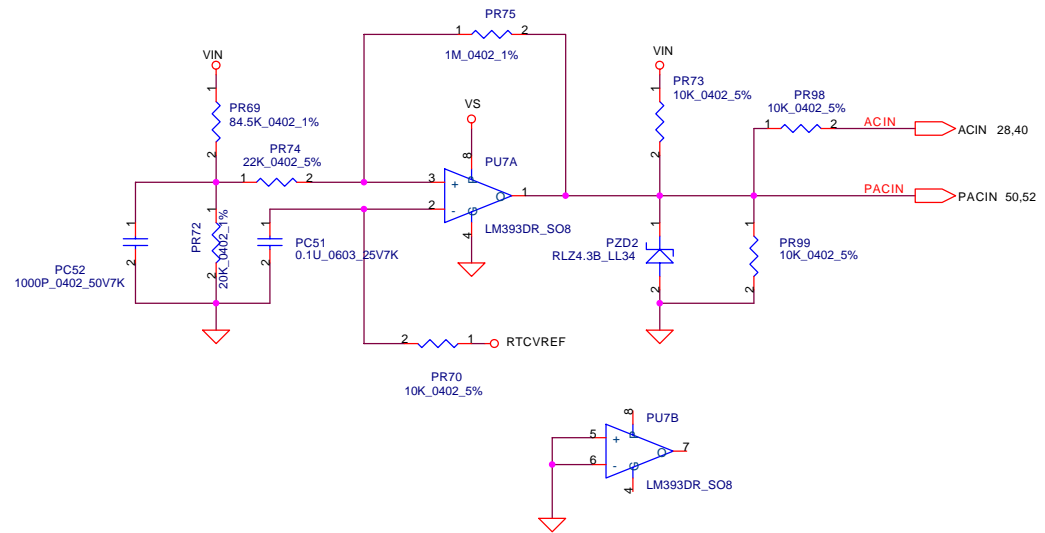
**PH1 under CPU bottom side :**  
 CPU thermal protection at 80 degree C  
 Recovery at 44(45) degree C



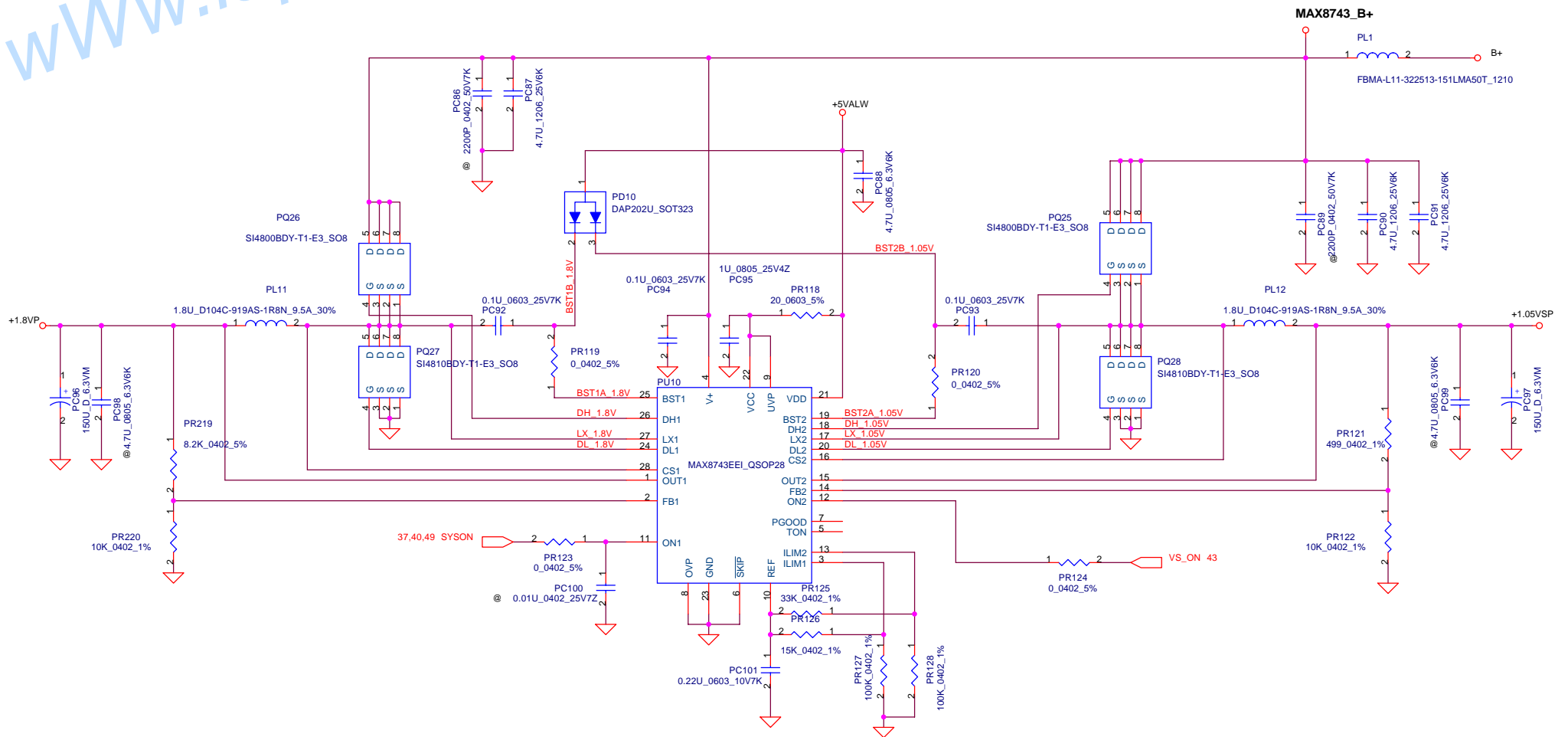
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Date:	Friday, November 11, 2005	Sheet	53	of	59



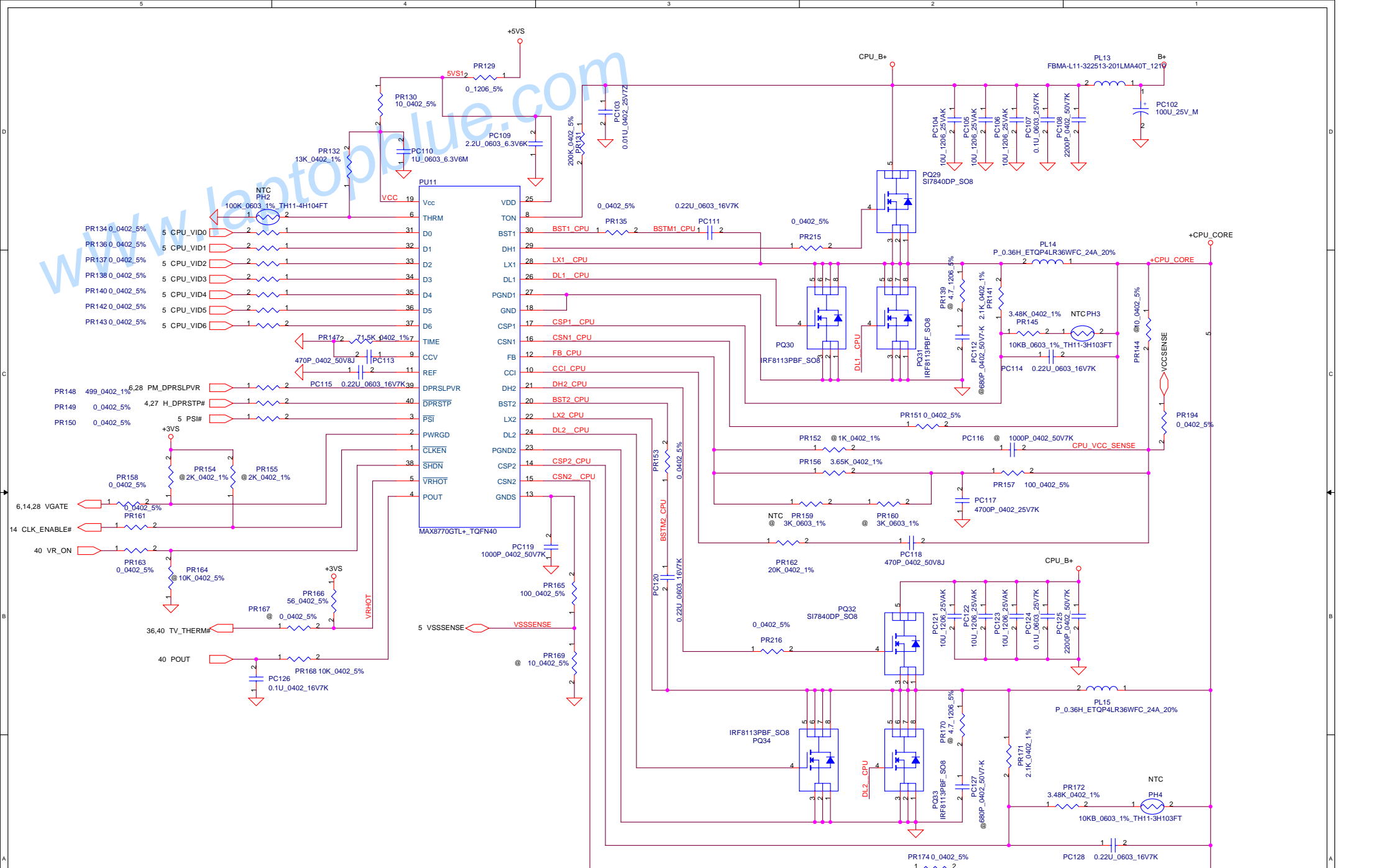
**Vin Detector**  
17.90V/17.24V



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				HBL50 LA-2921P	
				Date:	Friday, November 11, 2005
				Sheet	54 of 59
				Rev	0.2



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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title	
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				HBL50 LA-2921P	
				Date:	Rev
				Friday, November 11, 2005	0.2
				Sheet	55 of 59

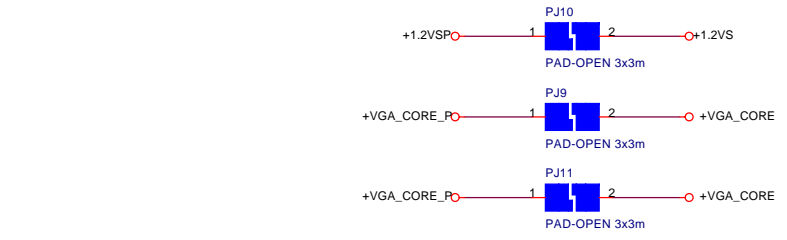
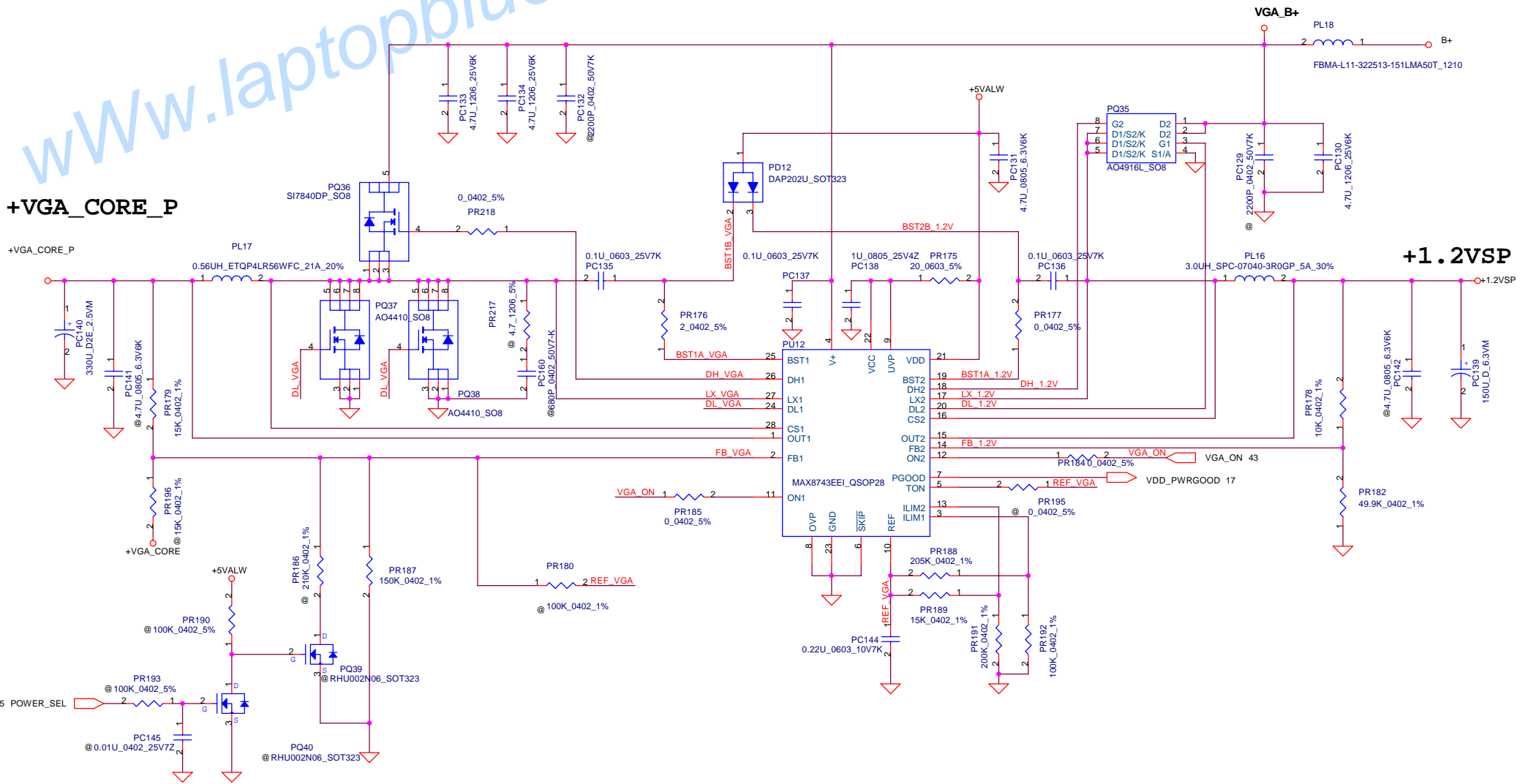


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Date:	Friday, November 11, 2005	Sheet	56	of 59



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POWER_SEL	H	L
+VGA_CORE FOR G73.	+0.95V(VGA@+G72@)	+1.025V
+VGA_CORE FOR G72.	+1.1V(VGA@)	



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Compal Electronics, Inc.			
Title: +VGA_CORE_P/+1.2VSP			
Size B	Document Number	Rev	
	HBL50 LA-2921P	0.2	
Date:	Friday, November 11, 2005	Sheet	57 of 59

## A --> B Change List

1. Page06 : No stuff R100 10K\_0402\_5%
2. Page09 : Add C49 & C887 220U\_D2\_4VM
3. Page10 : No stuff R57 2.2K\_0402\_5%
4. Page14 : Add R711 10K\_0402\_5% to set 96MHz output  
Change Q14 & Q15 pin1 net name to connect to ICH7M  
Change U19 ICS9LPRS325CKLFT part number to SA00000RE20
5. Page15 : Change C663, C664 from 22P\_0402\_50V8J to 18P\_0402\_50V8J.
6. Page18 : Modify VGA Device ID for G72MV & G73.
7. Page24 : Change VGA\_DDC\_CLK & VGA\_DDC\_DATA to Q26 & Q27 Level shift.  
Add R781 & R782 4.7K\_0402\_5%  
Change C589, C596, C583, C587, C594, C585 to 150P\_0402\_50V8J
8. Page28 : Change SB\_INT\_FLASH\_SEL# from ICH7M GPIO38 to GPIO33.
9. Page29 : Change C437 from 0.1U\_0402\_16V4Z to 1U\_0402\_6.3V4Z
10. Page30 : Change PATA HDD+ODD select resistor form RP to R\_0402 (0\_0402\_5%)
11. Page34 : Stuff R175 & no stuff R182 (0\_0402\_5%) for BCM4401E/BCM5789M/BCM5787M
12. Page35 : Modify LAN\_ACTIVITY# & LAN\_LINK# LED color
13. Page 36 : Add JP38 & C895 for CAMERA.  
Swap JP17 PCIE TX & RX Signal.  
Swap JP30 PCIE TX & RX Signal.
14. Page37 : Connect JP34 SMBus interface to ICH7M  
Change JP4 & JP5 USB connector to BOTTOM.
15. Page38 : Add 1394 @ BOM Structure.
16. Page41 : Delete LCM interface Extension I/O.  
No stuff R390 & Stuff R418 for Flash ROM interface.
17. Page42 : Change JP11 from 34 pin to 24 pin.  
Change SW8 & SW9.  
Add JP37.
18. Page43 : Change U28 Part Number.  
Change SW1 Part Number.  
Change R425 from 10K\_0402\_5% to 62K\_0402\_1%  
Change R422 from 10K\_0402\_5% to 62K\_0402\_1% & add C513 0.1U\_0402\_16V4Z
19. Page44 : Add C554 for MIC\_R  
Add R440, R695 (0\_0603\_5%) & J4, J5 for EMI request.
20. Page45 : Add Echo Cancellation function.
21. Page46 : Correct Headphone L & R signal.  
Reserved C879 for EMI request  
Modify MIC Jack circuit. add R741, R775, R776, L54, C876  
Change JP44 from 14 pin to 16 pin
22. Page48 : H27 connect to GNDA.
23. Page49 : Add R290, R238, R497, Q10, Q7, Q29  
Change R317 to 200K\_0402\_5%  
Change R586 to 510K\_0402\_5%

## B --> C Change List

1. Page05 : No stuff C608, C614
2. Page12 : Change JP22 Footprint
3. Page14 : Change R620 from 2K\_0402\_5% to 10K\_0402\_5% & add Q38
4. Page15 : Delete DVI pull high resistor
5. Page17 : AddC96 330U for +VGA\_CORE
6. Page18 : Modify PEX\_CFG[0..2] setting from 02 to 01.
7. Page30 : Delete R395 & C486, add R394 for SATA bridge reset timing  
Modify SATA HDD connector library
8. Page31 : Delete IDE\_CD\_L, IDE\_CD\_R & CD\_GNDA
9. Page34 : Add R783, R784, R785 for BCM5787M, stuff R214 when use BCM4401E,  
Del R168, change Q5 P/N
10. Page36 : Add +3VS, GND at JP30 for 3G device
11. Page38 : No stuff U14, R253, R246 & stuff R261
12. Page40 : Reserved R793 for ALC883 pin47 EAPD, & define KB910 Pin174 as EC\_PWROK
13. Page41 : No stuff U21, U30, C490, R391, R390, R388 & stuff R418
14. Page42 : Modify SW9 Pin1, Pin5 as NC, no stuff C7
15. Page43 : Modify Power OK circuit. add R790 for EC\_PWROK, reserved Q41, R420, C512  
add D35, D37, Change BATT1 P/N to SP093PA0200
16. Page44 : Delete ALC883 CD input circuit, add HD\_EAPD# signal
17. Page46 : Add C927, C928, reserved R791, R792
18. Page49 : Stuff Q33

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				Date: Friday, November 11, 2005		

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				B	HBL50 LA-2921P
Date:				Friday, November 11, 2005	Sheet 59 of 59

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