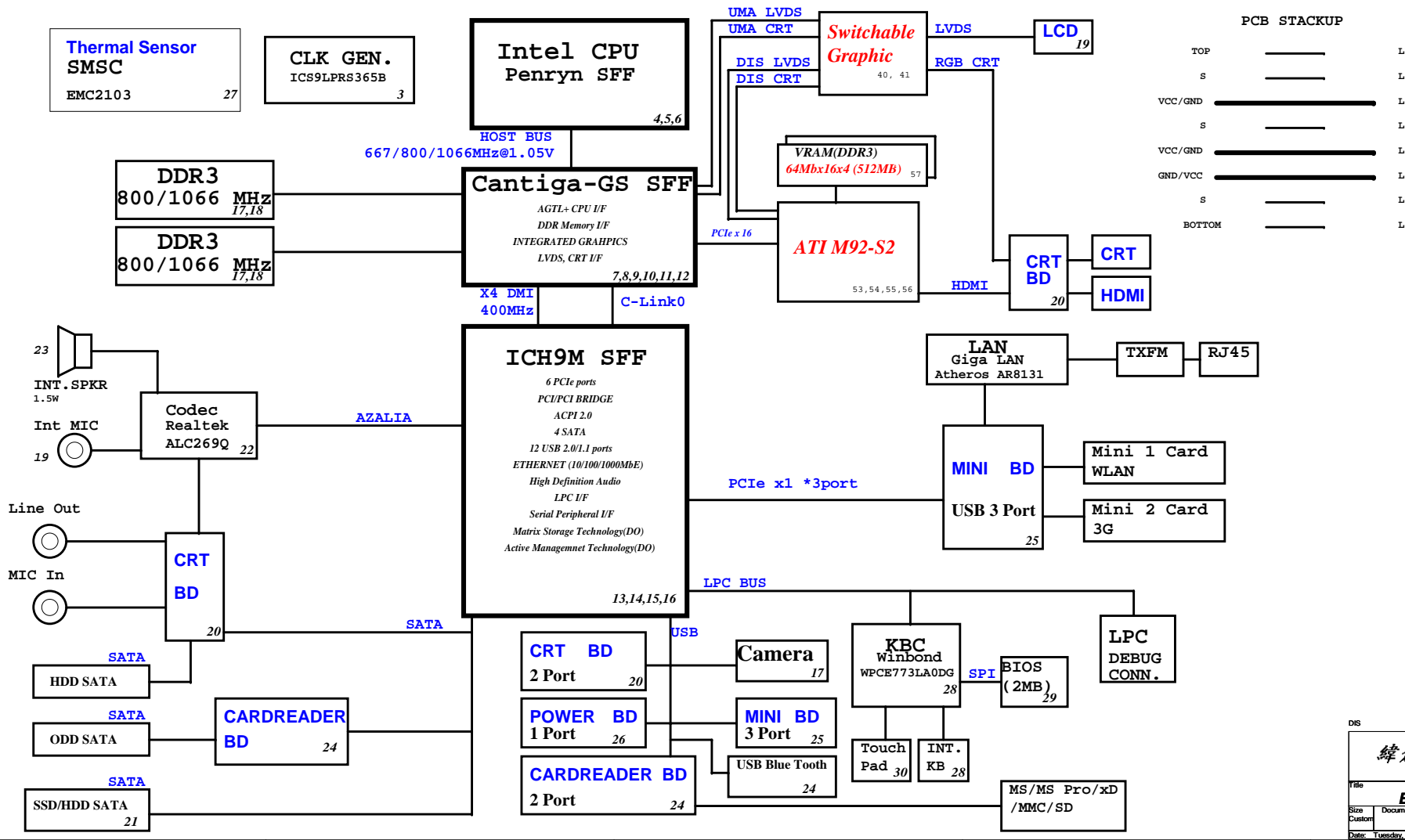


JM41/JM51 Discrete Block Diagram

Project code: 91.4CQ01.001
 PCB P/N : 48.4CQ01.0SB
 REVISION : 08274-1



SYSTEM DC/DC TPS51125		36
INPUTS	OUTPUTS	
DCBATOUT	5V_S5(6A) 3D3V_S5(5A) 5V_AUX_S5 3D3V_AUX_S5	
RT8202		37
INPUTS	OUTPUTS	
DCBATOUT	LD05V_S0(10A)	
RT8202		38
INPUTS	OUTPUTS	
DCBATOUT	LD5V_S3(11A)	
RT9026		39
INPUTS	OUTPUTS	
5V_S5	DDR_VREF_S3 (1.2A)	
CHARGER MAX8731A		
INPUTS	OUTPUTS	
DCBATOUT	CHG_PWR 18V 6.0A	
CPU DC/DC ADP3207A		
35		
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE 0~1.3V 64A	
VGA ISL6263A		
40		
INPUTS	OUTPUTS	
DCBATOUT	VCC GFXCORE (7A)	

DIS

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

File

BLOCK DIAGRAM

Size Customer Document Number Rev

JM41 Discrete -1

Date: Tuesday, April 07, 2009 Sheet 1 of 48

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRS LPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native LAN DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH [3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

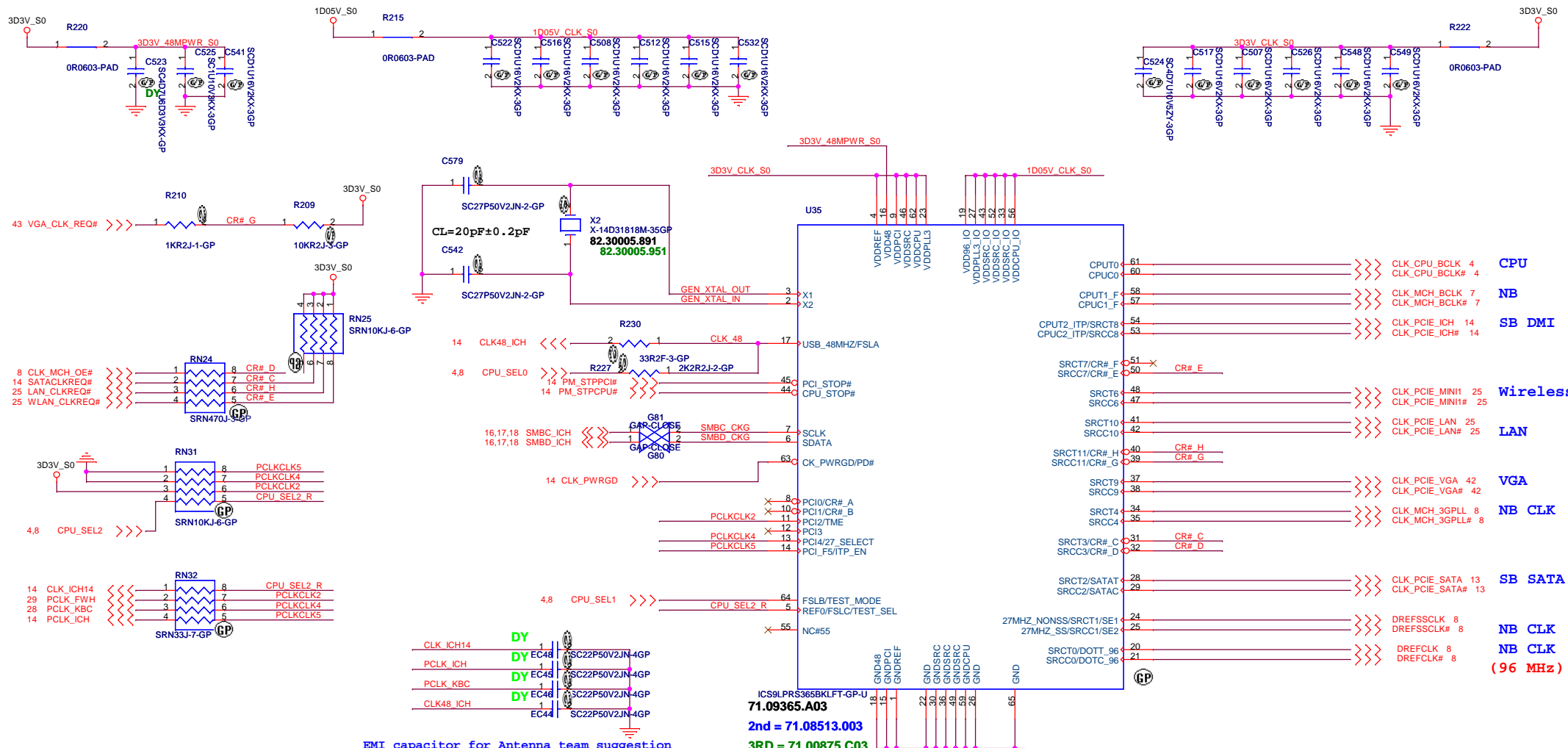
Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIe Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3 DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIe disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

DIS

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Reference			
Size A3	Document Number	Rev	
	JM41 Discrete	-1	
Date: Monday, April 06, 2009	Sheet 2	of	48



ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1 = CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1 = CR#_C controls SRC2 pair

EMI capacitor for Antenna team suggestion

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1 = CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1 = CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1 = CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1 = CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1 = CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1 = CR#_H controls SRC10

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

DIS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

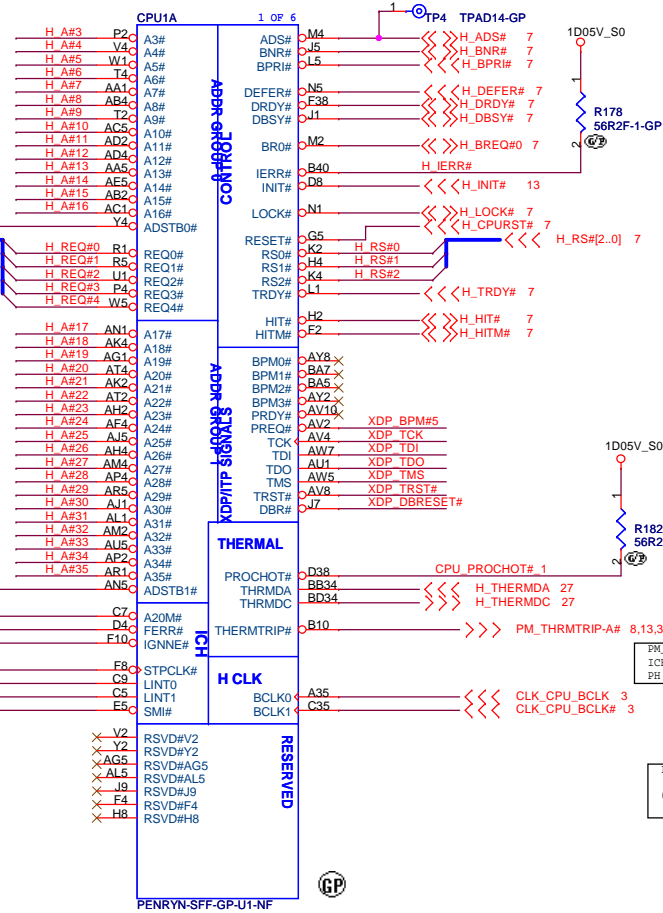
Title: **Clock Generator**

Size: Document Number **JM41 Discrete** Rev **-1**

Date: Monday, April 06, 2009 Sheet 3 of 48

7 H_A#(35..3) <<<>>> H_A#(35..3)

H_DINV#(3..0) <<>>> H_DINV#(3..0) 7
H_DSTBN#(3..0) <<>>> H_DSTBN#(3..0) 7
H_DSTBP#(3..0) <<>>> H_DSTBP#(3..0) 7
H_D#(63..0) <<>>> H_D#(63..0) 7



Place testpoint on H_IERR# with a GND 0.1" away

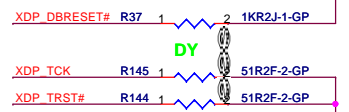
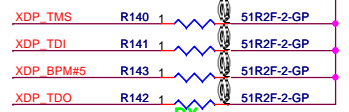
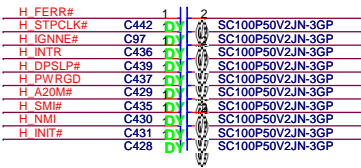
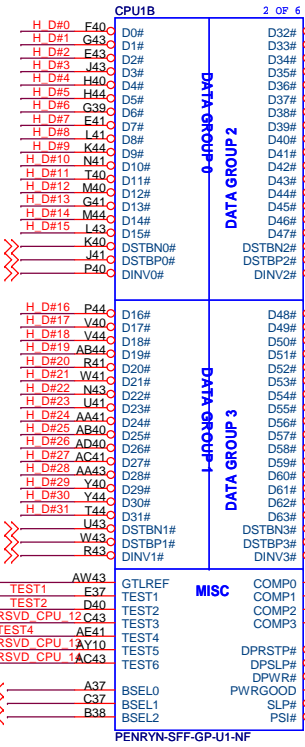
Close to NB

Layout Note: *CPU_CTLREFP* 0.5" max length.

Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5"

Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals

Place these TP on button-side, easy to measure.



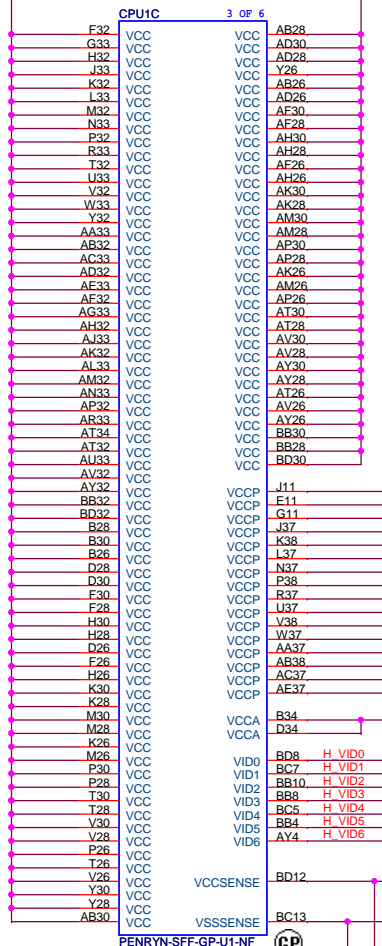
All place within 2" to CPU

Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5"

Wistron Corporation logo and title block information including 'CPU (1 of 3)', 'JM41 Discrete', and 'Sheet 4 of 48'.

VCC_CORE

VCC_CORE

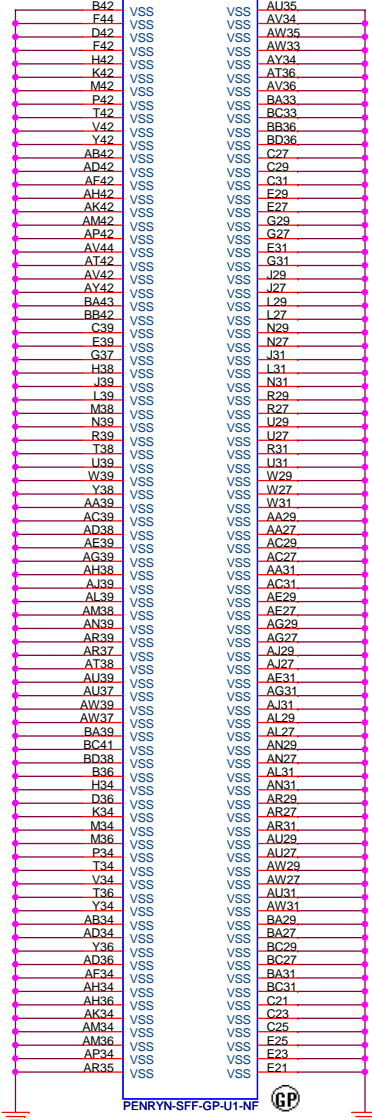


layout note: "1D5V_VCCA_S0" as short as possible

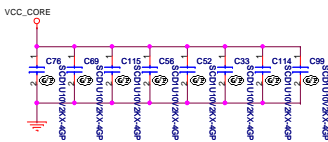
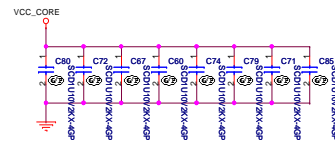
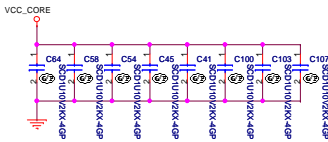
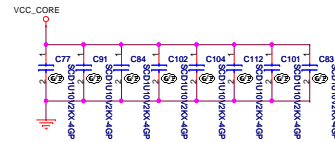
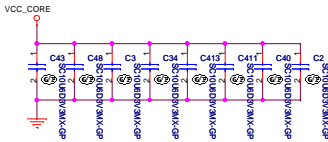
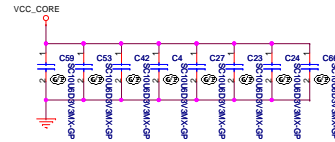
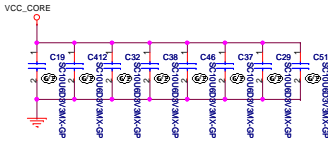
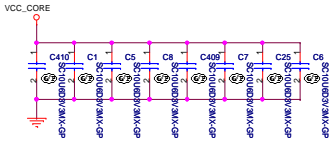
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

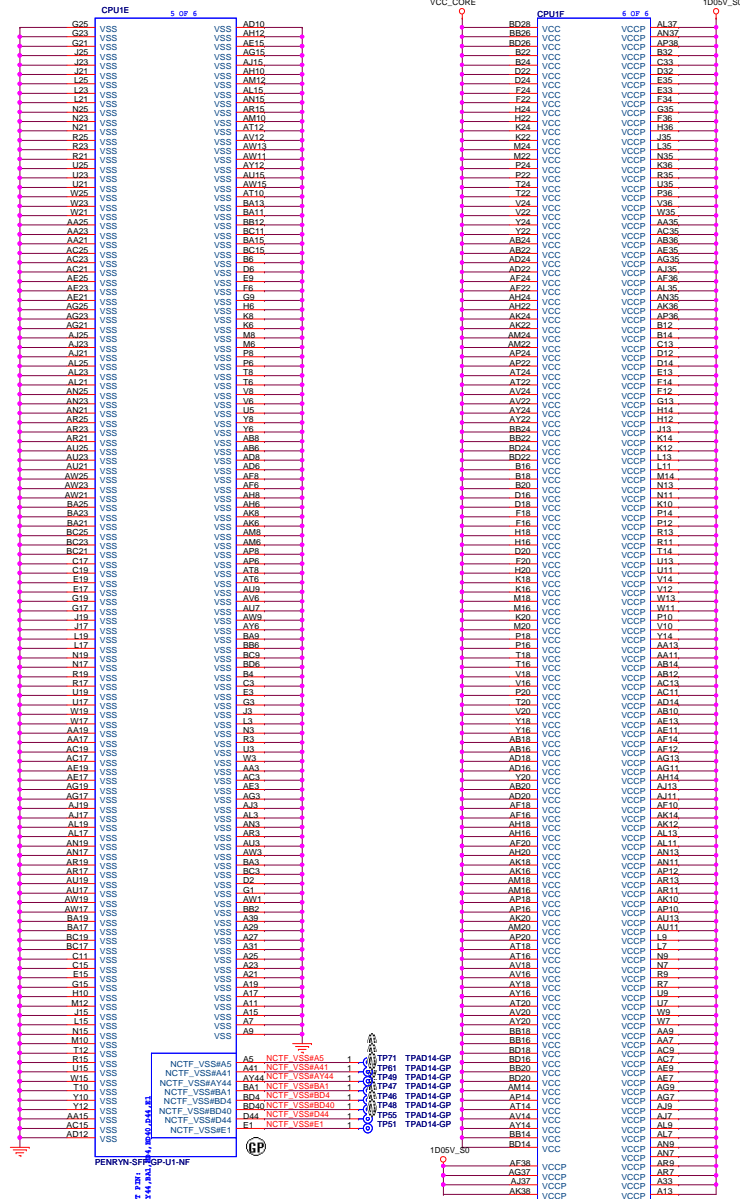
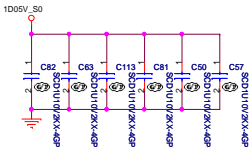
CPU1D 4 OF 6



Place these inside socket cavity on L8(North side Secondary)



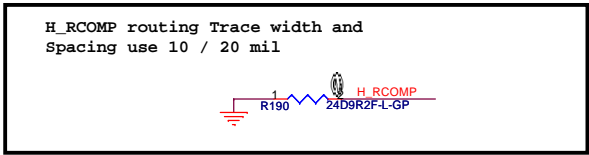
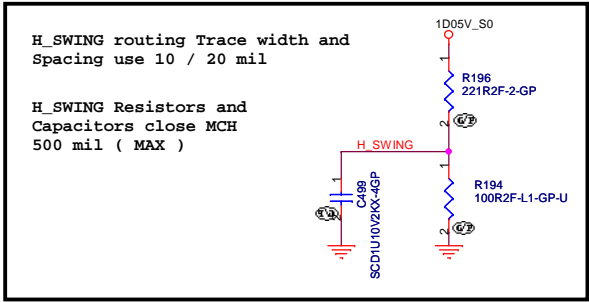
Place these inside socket cavity on L8(North side Secondary)



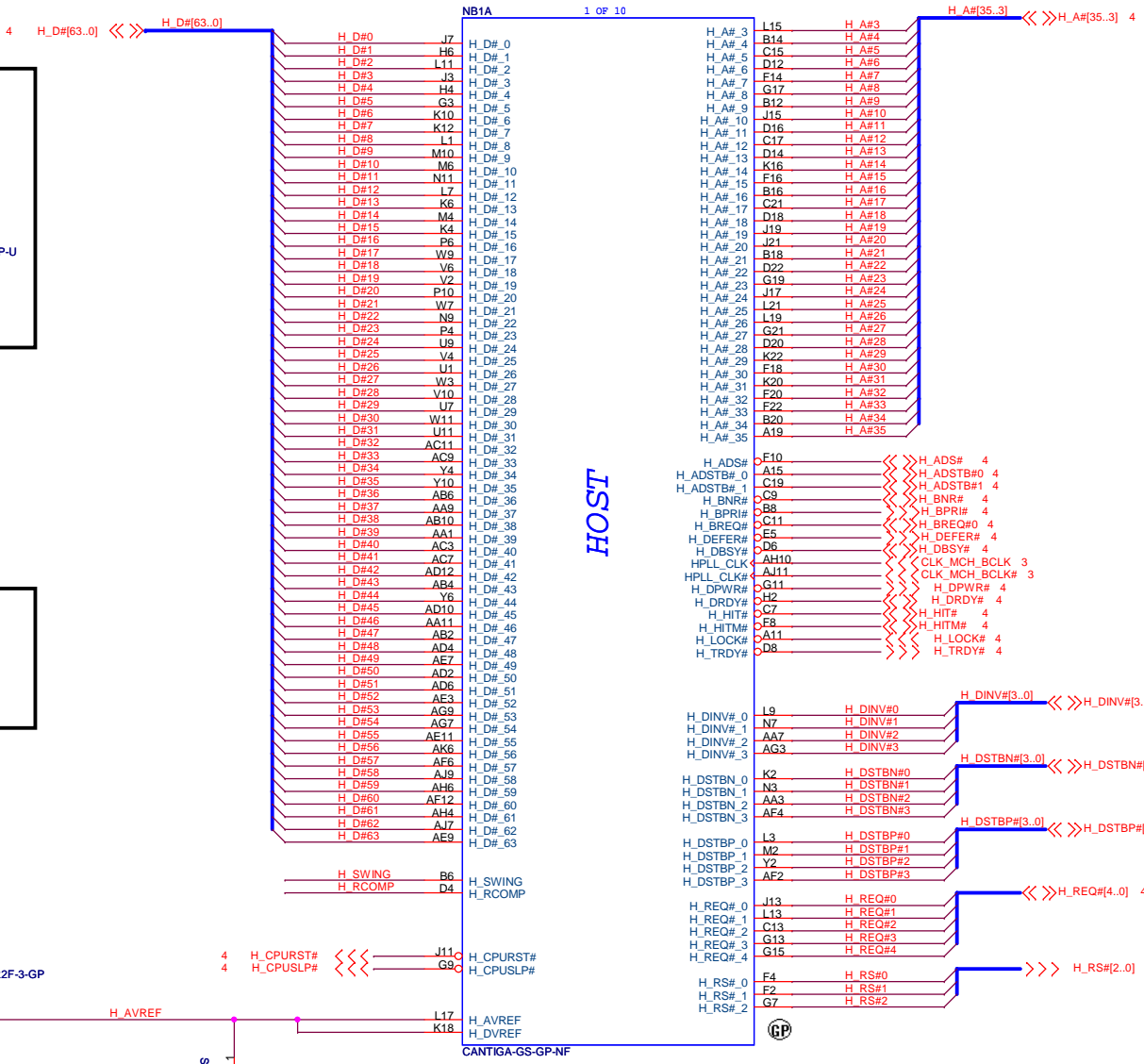
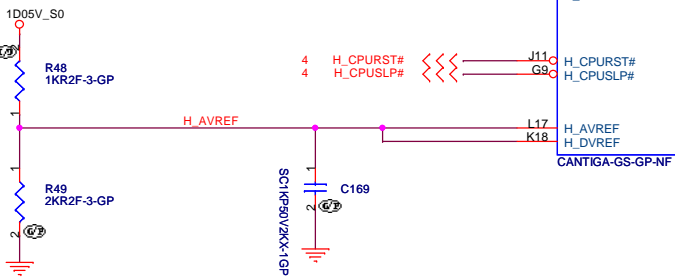
PENRYN-SFF-GP-U1-NF
NCTF_VSS#A4
NCTF_VSS#A1
NCTF_VSS#A4
NCTF_VSS#A4
NCTF_VSS#A1
NCTF_VSS#B4
NCTF_VSS#B4
NCTF_VSS#B4
NCTF_VSS#D4
NCTF_VSS#E1

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

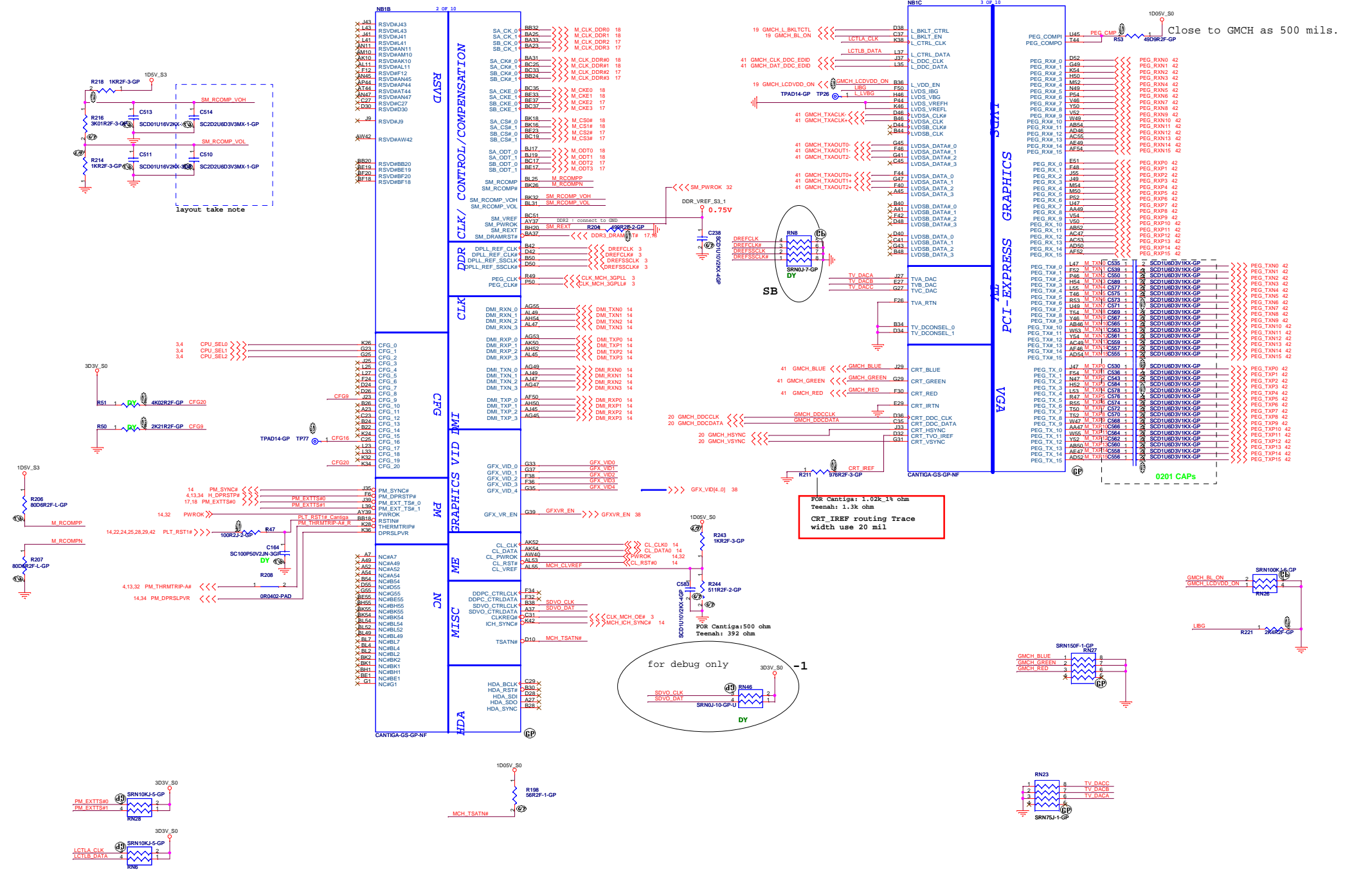
File
Size Document Number
Date: Monday, April 08, 2008
CPU (3 of 3)
JM41 Discrete
Rev -1
Page 9 of 48



Place them near to the chip (< 0.5")



HOST



18 M_A_DQ[63.0] <<< M_A_DQ[63.0]

M A DQ0 AP46 SA_DQ_0
 M A DQ1 AU47 SA_DQ_1
 M A DQ2 AT46 SA_DQ_2
 M A DQ3 AR45 SA_DQ_3
 M A DQ4 AR45 SA_DQ_3
 M A DQ5 AN49 SA_DQ_4
 M A DQ6 AV50 SA_DQ_5
 M A DQ7 AP50 SA_DQ_7
 M A DQ8 AW47 SA_DQ_8
 M A DQ9 BD50 SA_DQ_9
 M A DQ10 AW49 SA_DQ_10
 M A DQ11 BA49 SA_DQ_11
 M A DQ12 BC49 SA_DQ_12
 M A DQ13 AV46 SA_DQ_13
 M A DQ14 BA47 SA_DQ_14
 M A DQ15 AY50 SA_DQ_15
 M A DQ16 BF49 SA_DQ_16
 M A DQ17 BC47 SA_DQ_17
 M A DQ18 BF50 SA_DQ_18
 M A DQ19 BF48 SA_DQ_19
 M A DQ20 BC43 SA_DQ_20
 M A DQ21 BE49 SA_DQ_21
 M A DQ22 BA43 SA_DQ_22
 M A DQ23 BF47 SA_DQ_23
 M A DQ24 BF42 SA_DQ_24
 M A DQ25 BC39 SA_DQ_25
 M A DQ26 BF44 SA_DQ_26
 M A DQ27 BF40 SA_DQ_27
 M A DQ28 BB40 SA_DQ_28
 M A DQ29 BF43 SA_DQ_29
 M A DQ30 BF38 SA_DQ_30
 M A DQ31 BE41 SA_DQ_31
 M A DQ32 BA15 SA_DQ_32
 M A DQ33 BE11 SA_DQ_33
 M A DQ34 BE15 SA_DQ_34
 M A DQ35 BE14 SA_DQ_35
 M A DQ36 BB14 SA_DQ_36
 M A DQ37 BC15 SA_DQ_37
 M A DQ38 BE13 SA_DQ_38
 M A DQ39 BF16 SA_DQ_39
 M A DQ40 BF10 SA_DQ_40
 M A DQ41 BC11 SA_DQ_41
 M A DQ42 BE9 SA_DQ_42
 M A DQ43 BC7 SA_DQ_43
 M A DQ44 BC7 SA_DQ_43
 M A DQ45 BC9 SA_DQ_45
 M A DQ46 BD6 SA_DQ_46
 M A DQ47 BF12 SA_DQ_47
 M A DQ48 AV6 SA_DQ_48
 M A DQ49 BE6 SA_DQ_49
 M A DQ50 AW7 SA_DQ_50
 M A DQ51 AY6 SA_DQ_51
 M A DQ52 AT10 SA_DQ_52
 M A DQ53 AW11 SA_DQ_53
 M A DQ54 AU11 SA_DQ_54
 M A DQ55 AW9 SA_DQ_55
 M A DQ56 AR11 SA_DQ_56
 M A DQ57 AT6 SA_DQ_57
 M A DQ58 AP6 SA_DQ_58
 M A DQ59 AL7 SA_DQ_59
 M A DQ60 AR7 SA_DQ_60
 M A DQ61 AT12 SA_DQ_61
 M A DQ62 AM6 SA_DQ_62
 M A DQ63 AU7 SA_DQ_63

NB1D 4 OF 10

SA_BS_0 BC21 M A BS#0 18
 SA_BS_1 BJ21 M A BS#1 18
 SA_BS_2 BJ41 M A BS#2 18

SA_RAS# BH22 M A_RAS# 18
 SA_CAS# BK20 M A_CAS# 18
 SA_WE# BL15 M_A_WE# 18

SA_DM_0 AT50 M A DM0 M A DM[7.0] 18
 SA_DM_1 BB50 M A DM1
 SA_DM_2 BB46 M A DM2
 SA_DM_3 BE39 M A DM3
 SA_DM_4 BB12 M A DM4
 SA_DM_5 BF7 M A DM5
 SA_DM_6 AV10 M A DM6
 SA_DM_7 AR9 M A DM7

SA_DQS_0 AR47 M A DQS0 M A DQS[7.0] 18
 SA_DQS_1 BA45 M A DQS1
 SA_DQS_2 BE45 M A DQS2
 SA_DQS_3 BC41 M A DQS3
 SA_DQS_4 BC13 M A DQS4
 SA_DQS_5 BB10 M A DQS5
 SA_DQS_6 BA7 M A DQS6
 SA_DQS_7 AN7 M A DQS7

SA_DQS#_0 AR49 M A DQS#0 M A DQS#[7.0] 18
 SA_DQS#_1 AW45 M A DQS#1
 SA_DQS#_2 BC45 M A DQS#2
 SA_DQS#_3 BA41 M A DQS#3
 SA_DQS#_4 BA13 M A DQS#4
 SA_DQS#_5 BA11 M A DQS#5
 SA_DQS#_6 BA9 M A DQS#6
 SA_DQS#_7 AN9 M A DQS#7

SA_MA_0 BC23 M A A0 M A A[14.0] 18
 SA_MA_1 BF22 M A A1
 SA_MA_2 BE31 M A A2
 SA_MA_3 BC31 M A A3
 SA_MA_4 BH25 M A A4
 SA_MA_5 BJ35 M A A5
 SA_MA_6 BB34 M A A6
 SA_MA_7 BH32 M A A7
 SA_MA_8 BB26 M A A8
 SA_MA_9 BF32 M A A9
 SA_MA_10 BA21 M A A10
 SA_MA_11 BC25 M A A11
 SA_MA_12 BH34 M A A12
 SA_MA_13 BH18 M A A13
 SA_MA_14 BE25 M A A14

DDR SYSTEM MEMORY A

CANTIGA-GS-GP-NF



17 M_B_DQ[63.0] <<< M_B_DQ[63.0]

M B DQ0 AP54 SB_DQ_0
 M B DQ1 AM52 SB_DQ_1
 M B DQ2 AR55 SB_DQ_2
 M B DQ3 AV54 SB_DQ_3
 M B DQ4 AM54 SB_DQ_4
 M B DQ5 AN53 SB_DQ_5
 M B DQ6 AT52 SB_DQ_6
 M B DQ7 AU53 SB_DQ_7
 M B DQ8 AW53 SB_DQ_8
 M B DQ9 AV52 SB_DQ_9
 M B DQ10 BB52 SB_DQ_10
 M B DQ11 BC53 SB_DQ_11
 M B DQ12 AV52 SB_DQ_12
 M B DQ13 AW55 SB_DQ_13
 M B DQ14 BD52 SB_DQ_14
 M B DQ15 BC55 SB_DQ_15
 M B DQ16 BF54 SB_DQ_16
 M B DQ17 BE51 SB_DQ_17
 M B DQ18 BH48 SB_DQ_18
 M B DQ19 BK48 SB_DQ_19
 M B DQ20 BE53 SB_DQ_20
 M B DQ21 BH52 SB_DQ_21
 M B DQ22 BK46 SB_DQ_22
 M B DQ23 BJ47 SB_DQ_23
 M B DQ24 BL45 SB_DQ_24
 M B DQ25 BJ45 SB_DQ_25
 M B DQ26 BL41 SB_DQ_26
 M B DQ27 BH44 SB_DQ_27
 M B DQ28 BH44 SB_DQ_28
 M B DQ29 BK40 SB_DQ_29
 M B DQ30 BJ39 SB_DQ_30
 M B DQ31 BK10 SB_DQ_31
 M B DQ32 BK10 SB_DQ_32
 M B DQ33 BH10 SB_DQ_33
 M B DQ34 BK6 SB_DQ_34
 M B DQ35 BH6 SB_DQ_35
 M B DQ36 BJ9 SB_DQ_36
 M B DQ37 BL11 SB_DQ_37
 M B DQ38 BG5 SB_DQ_38
 M B DQ39 BJ5 SB_DQ_39
 M B DQ40 BG3 SB_DQ_40
 M B DQ41 BF4 SB_DQ_41
 M B DQ42 BD4 SB_DQ_42
 M B DQ43 BA3 SB_DQ_43
 M B DQ44 BE5 SB_DQ_44
 M B DQ45 BF2 SB_DQ_45
 M B DQ46 BB4 SB_DQ_46
 M B DQ47 AY4 SB_DQ_47
 M B DQ48 BA1 SB_DQ_48
 M B DQ49 AP2 SB_DQ_49
 M B DQ50 AU1 SB_DQ_50
 M B DQ51 AT2 SB_DQ_51
 M B DQ52 AT4 SB_DQ_52
 M B DQ53 AV4 SB_DQ_53
 M B DQ54 AU3 SB_DQ_54
 M B DQ55 AR3 SB_DQ_55
 M B DQ56 AN1 SB_DQ_56
 M B DQ57 AP4 SB_DQ_57
 M B DQ58 AL3 SB_DQ_58
 M B DQ59 AJ1 SB_DQ_59
 M B DQ60 AK4 SB_DQ_60
 M B DQ61 AM4 SB_DQ_61
 M B DQ62 AH2 SB_DQ_62
 M B DQ63 AK2 SB_DQ_63

NB1E 5 OF 10

SB_BS_0 BJ13 M B BS#0 17
 SB_BS_1 BK12 M B BS#1 17
 SB_BS_2 BK38 M B BS#2 17

SB_RAS# BE21 M B_RAS# 17
 SB_CAS# BH14 M B_CAS# 17
 SB_WE# BK14 M_B_WE# 17

SB_DM_0 AP52 M B DM0 M_B DM[7.0] 17
 SB_DM_1 AY54 M B DM1
 SB_DM_2 BJ49 M B DM2
 SB_DM_3 BJ43 M B DM3
 SB_DM_4 BH12 M B DM4
 SB_DM_5 BD2 M B DM5
 SB_DM_6 AY2 M B DM6
 SB_DM_7 AJ3 M B DM7

SB_DQS_0 AR53 M B DQS0 M_B DQS[7.0] 17
 SB_DQS_1 BA53 M B DQS1
 SB_DQS_2 BH50 M B DQS2
 SB_DQS_3 BK42 M B DQS3
 SB_DQS_4 BHH M B DQS4
 SB_DQS_5 BB2 M B DQS5
 SB_DQS_6 AV2 M B DQS6
 SB_DQS_7 AM2 M B DQS7

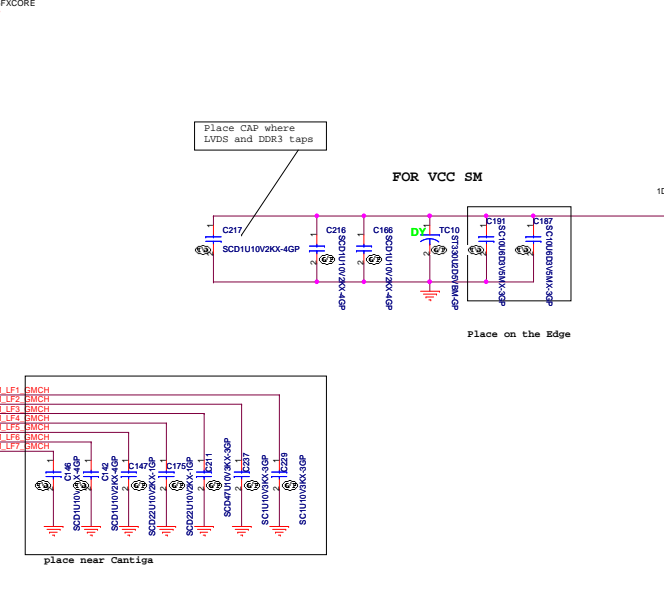
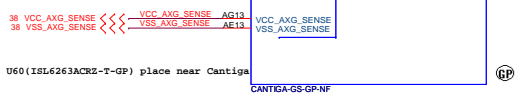
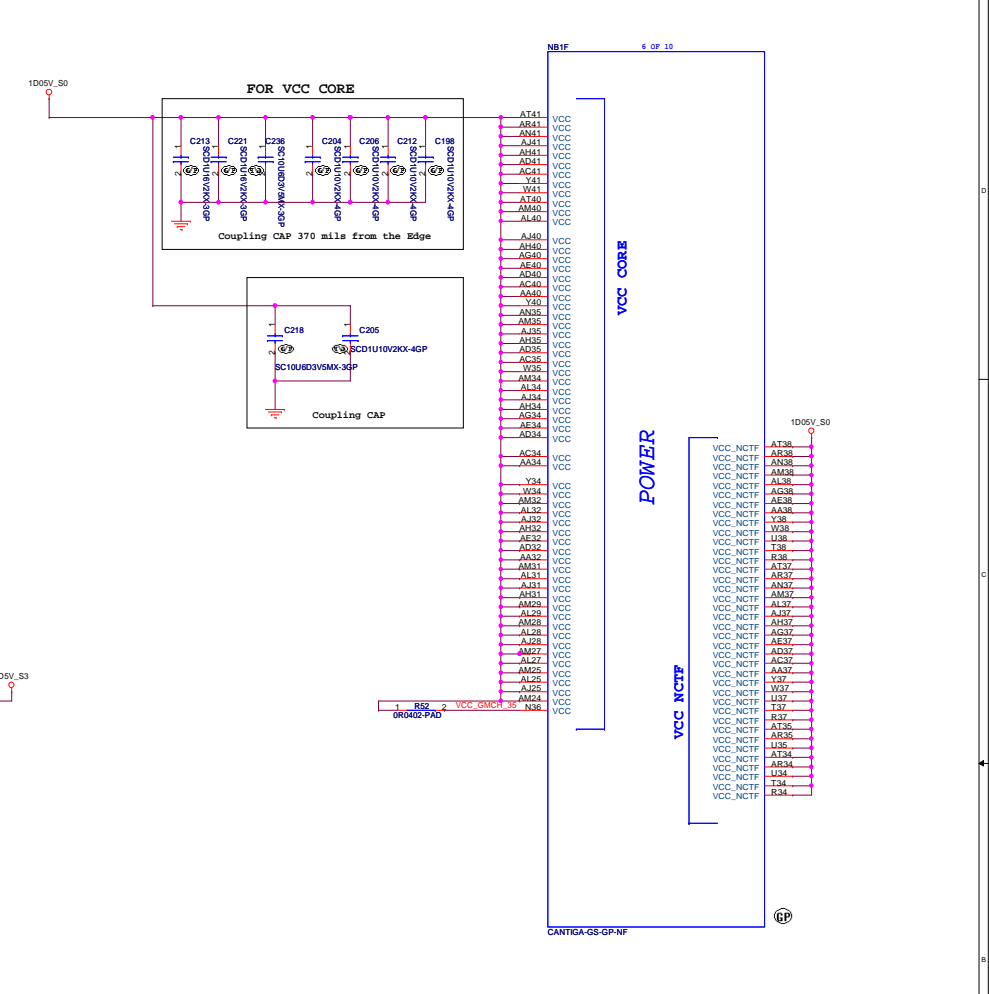
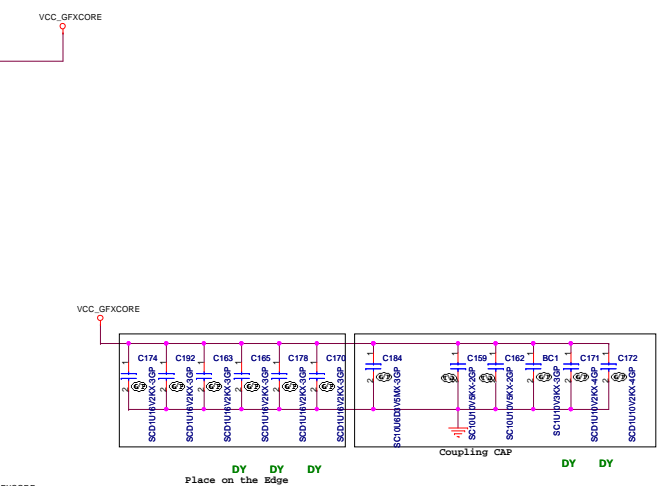
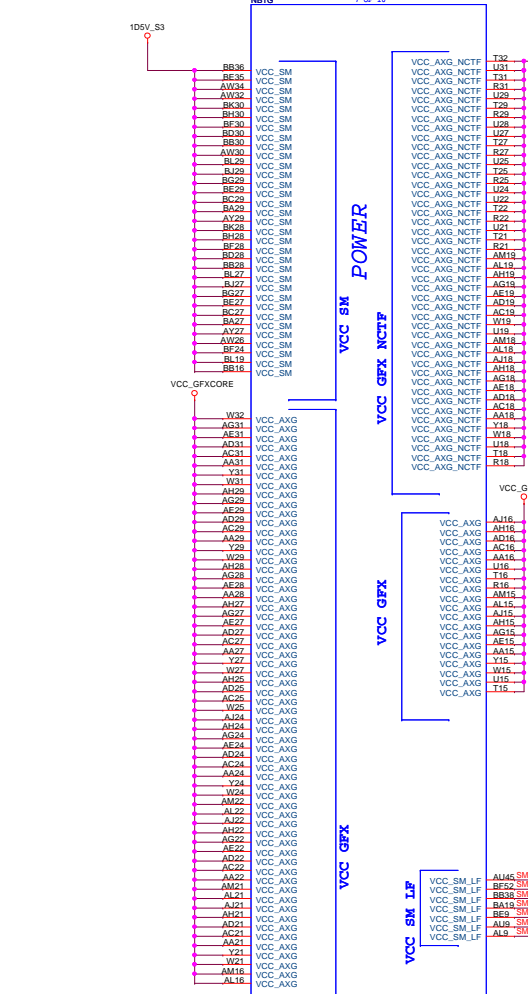
SB_DQS#_0 AT54 M B DQS#0 M_B DQS#[7.0] 17
 SB_DQS#_1 BB54 M B DQS#1
 SB_DQS#_2 BJ51 M B DQS#2
 SB_DQS#_3 BH42 M B DQS#3
 SB_DQS#_4 BK8 M B DQS#4
 SB_DQS#_5 BC3 M B DQS#5
 SB_DQS#_6 AW3 M B DQS#6
 SB_DQS#_7 AN3 M B DQS#7

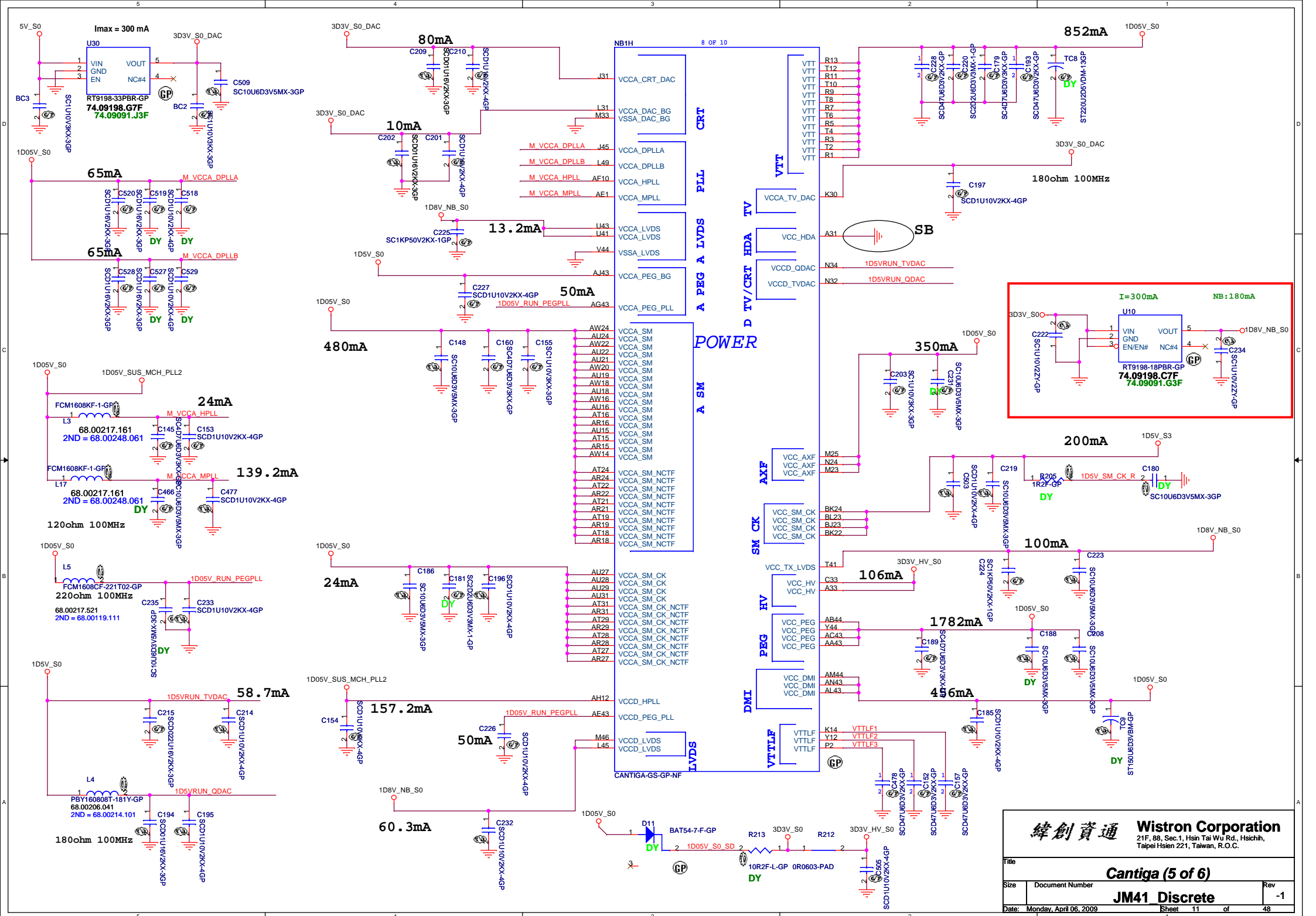
SB_MA_0 BJ15 M B A0 M_B A[14.0] 17
 SB_MA_1 BJ33 M B A1
 SB_MA_2 BH24 M B A2
 SB_MA_3 BA17 M B A3
 SB_MA_4 BF36 M B A4
 SB_MA_5 BH36 M B A5
 SB_MA_6 BF34 M B A6
 SB_MA_7 BK34 M B A7
 SB_MA_8 BJ37 M B A8
 SB_MA_9 BH40 M B A9
 SB_MA_10 BH16 M B A10
 SB_MA_11 BK36 M B A11
 SB_MA_12 BH38 M B A12
 SB_MA_13 BJ11 M B A13
 SB_MA_14 BL37 M B A14

DDR SYSTEM MEMORY B

CANTIGA-GS-GP-NF

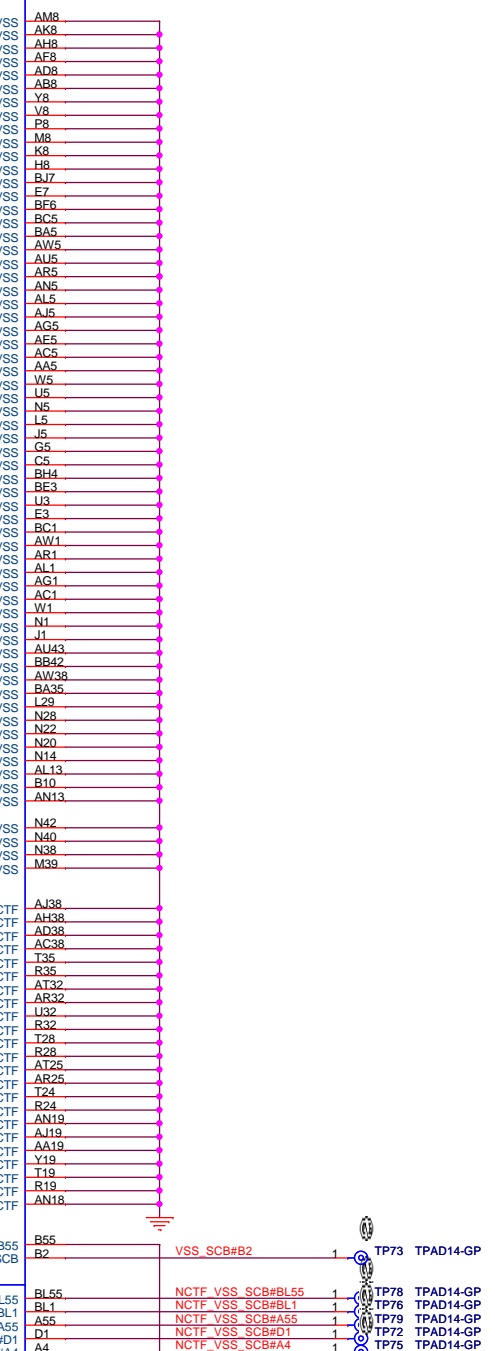
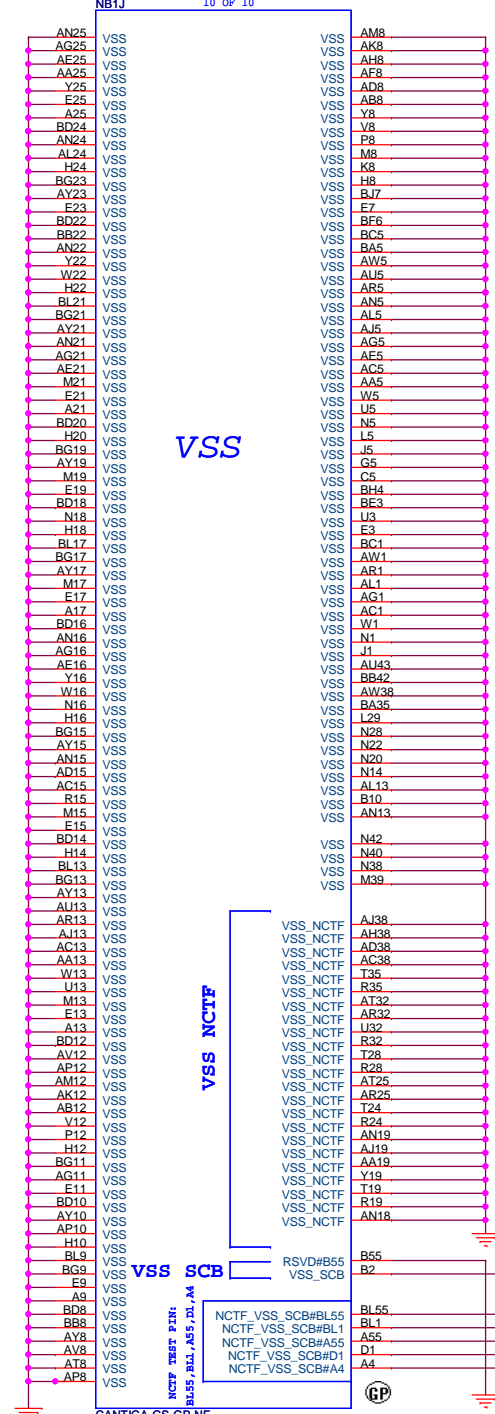
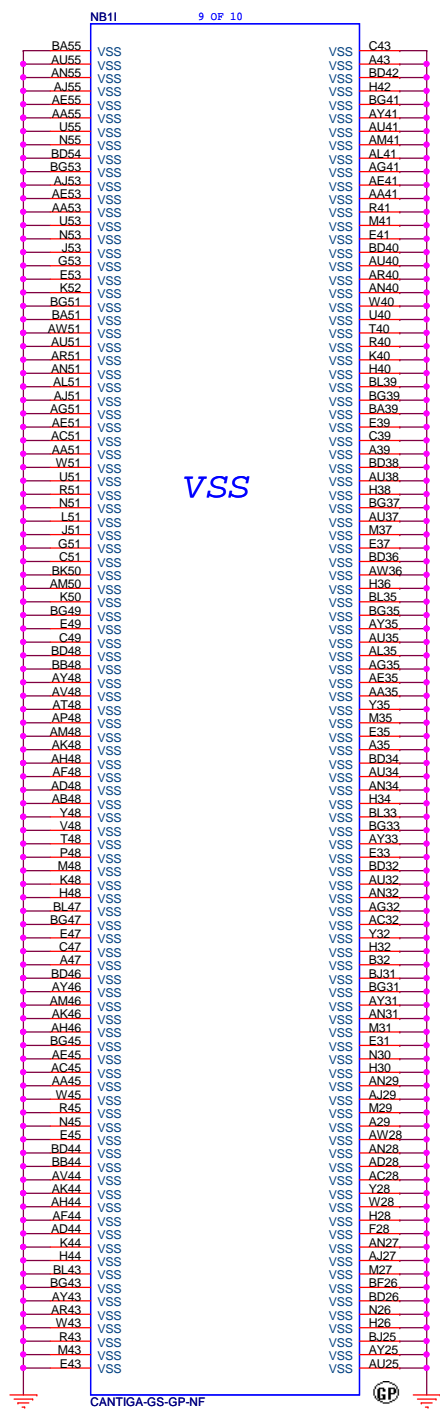






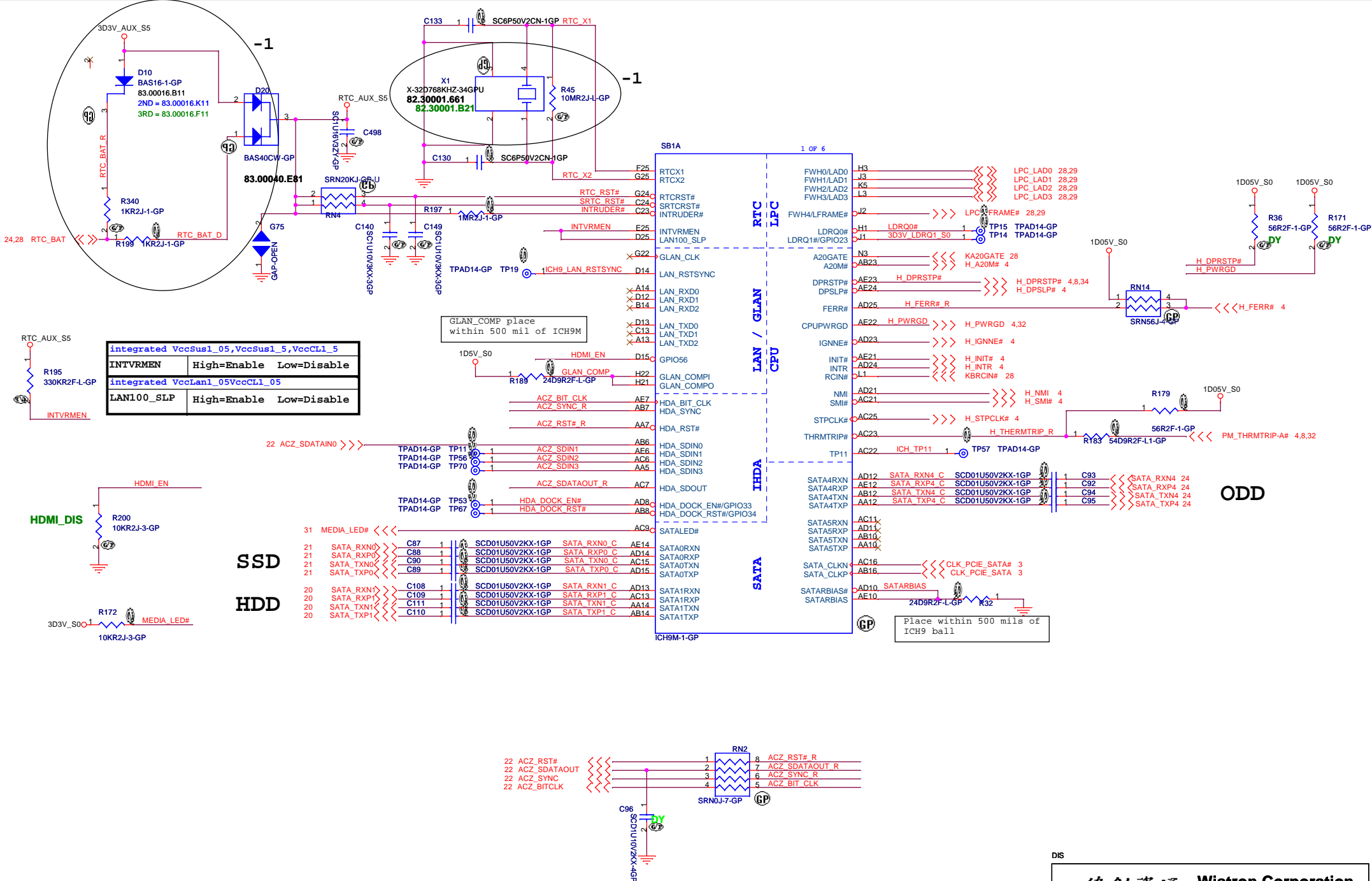
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		
Cantiga (5 of 6)		
Size	Document Number	Rev
JM41 Discrete		-1
Date: Monday, April 06, 2009	Sheet 11	of 48

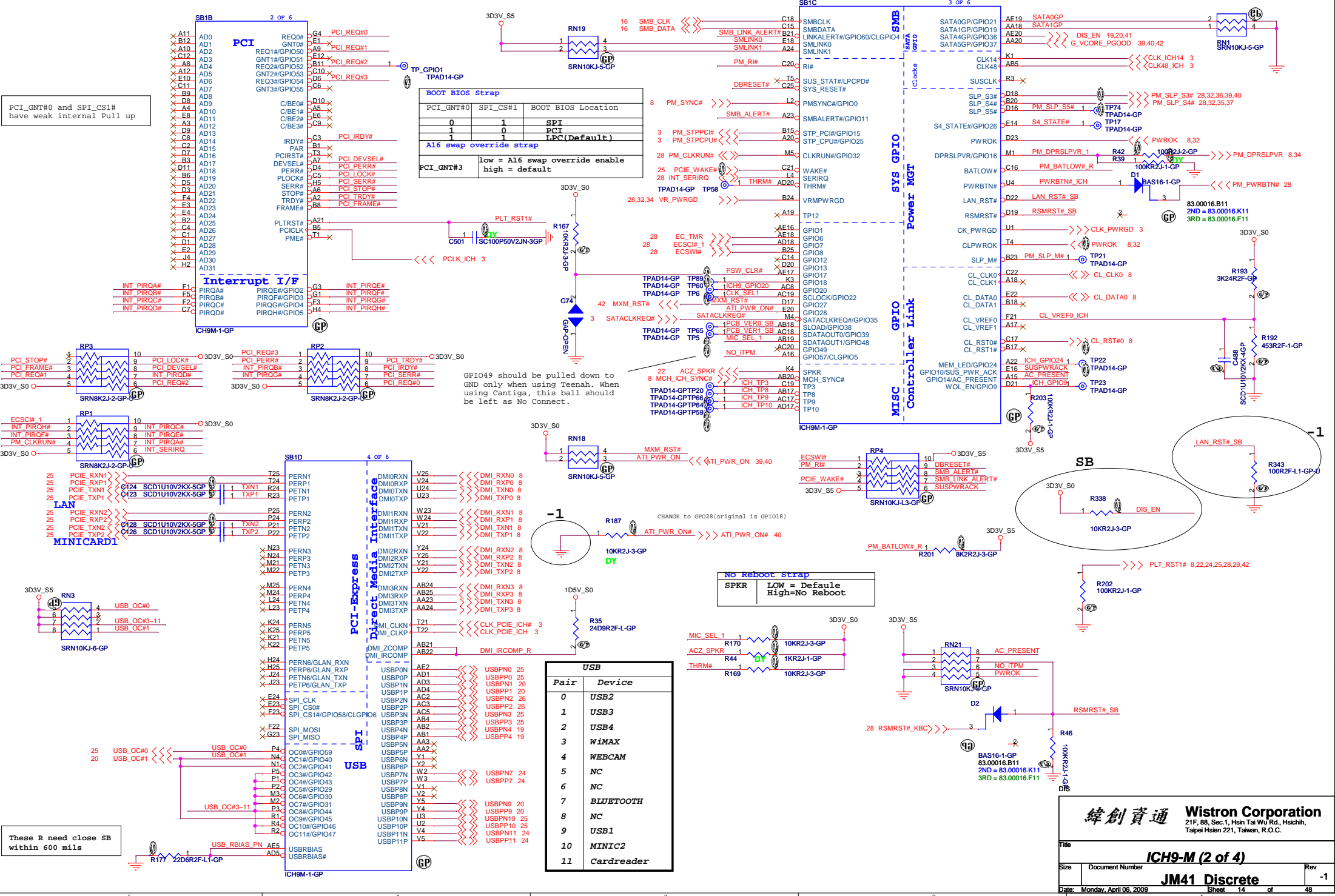


緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		Cantiga (6 of 6)	
Size	Document Number	Rev	-1
Date: Monday, April 06, 2009		Sheet 12 of 48	



PCI_GNT#0 and SPD_CS1# have weak internal Pull up



BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI

A16 swap override strap

low = A16 swap override enable
high = default

USB

Pair	Device
0	USB2
1	USB3
2	USB4
3	WIMAX
4	WEBCAM
5	NC
6	NC
7	BLUETOOTH
8	NC
9	USB1
10	MINIC2
11	Cardreader

No Reboot Strap

SPKR LOW = Default
High = No Reboot

緯創資通 **Wistron Corporation**
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH9-M (2 of 4)**

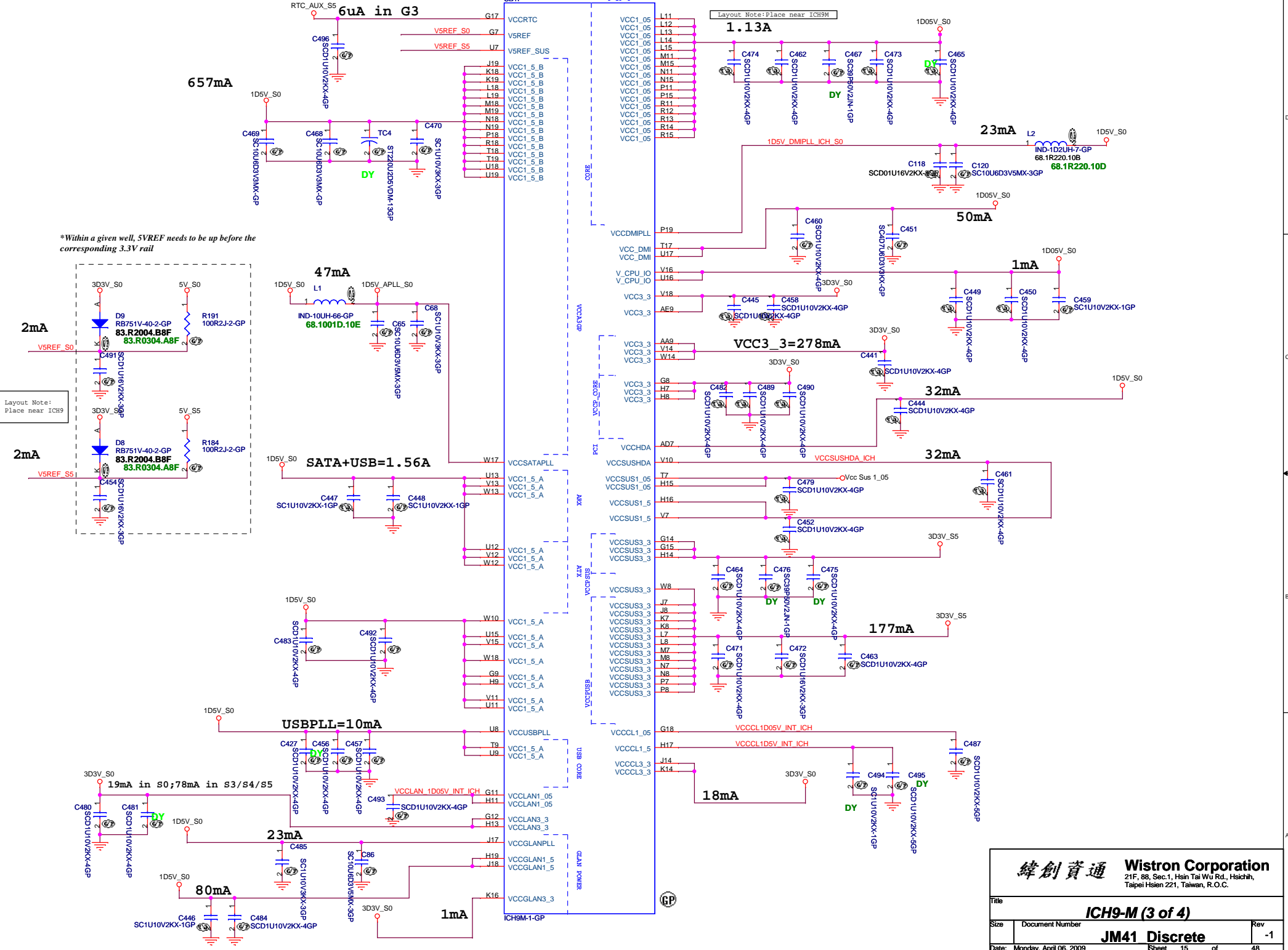
Size: Document Number: Rev: -1

Date: Monday, April 06, 2009 Sheet 14 of 48

These R need close SB within 600 mils

GPI049 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.

CHANGE to GP028(original is GPI018)

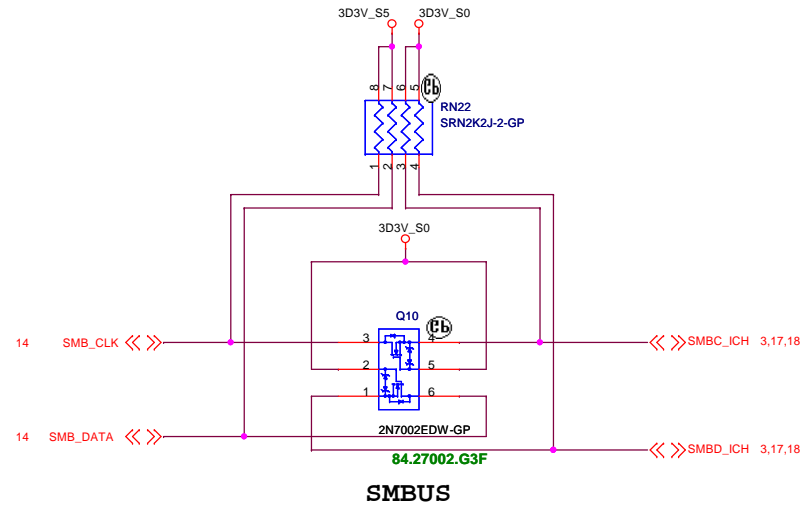
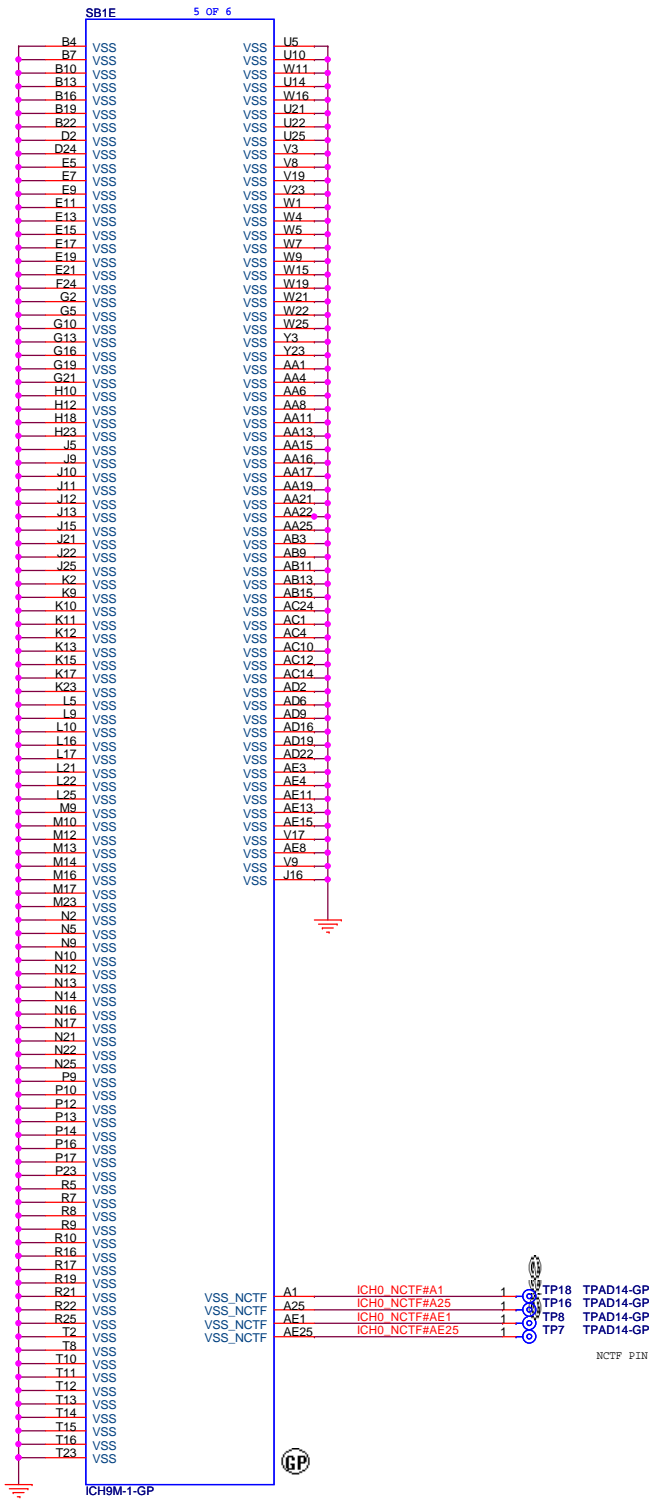


*Within a given well, VSREF needs to be up before the corresponding 3.3V rail

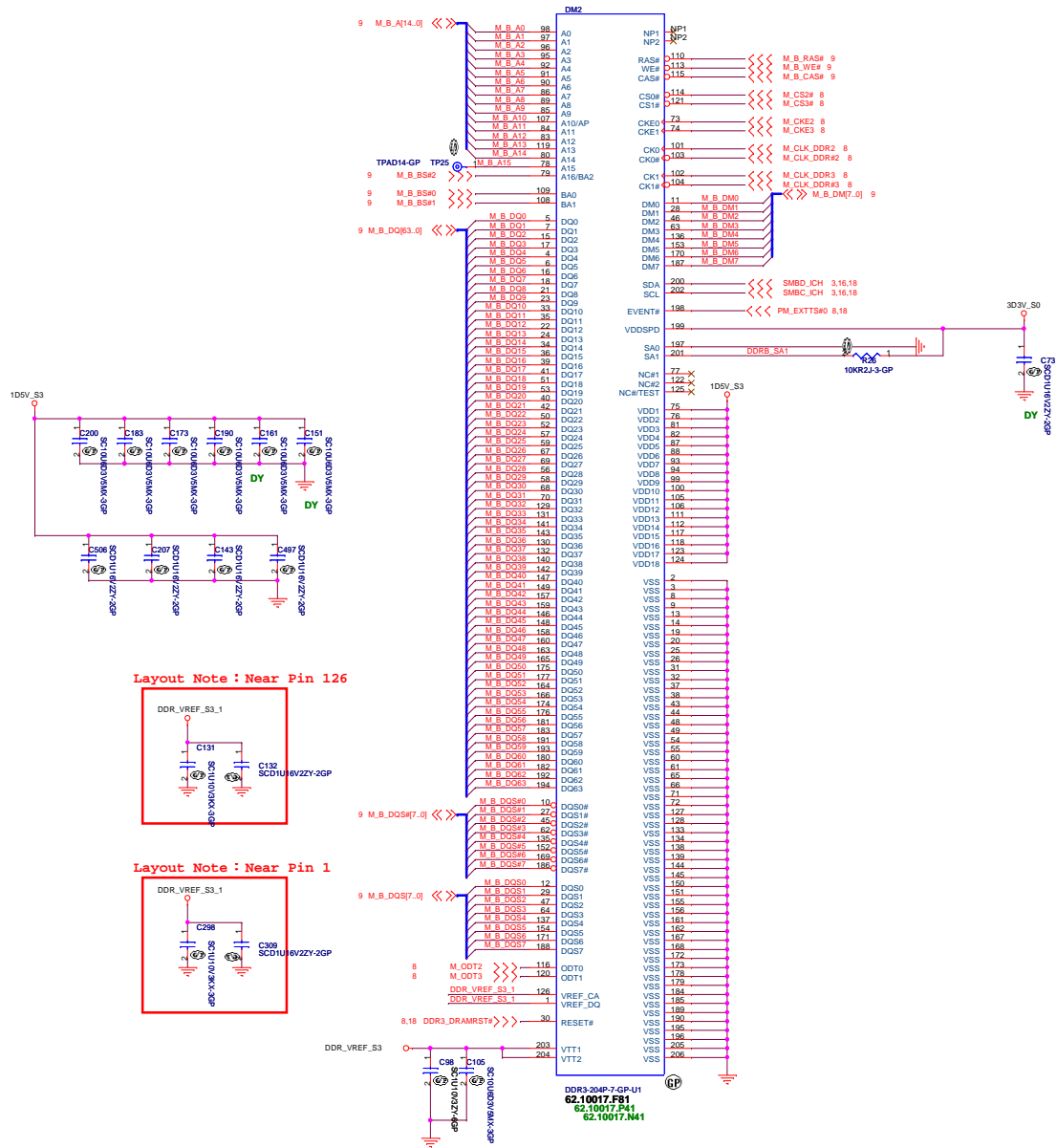
Layout Note:
Place near ICH9

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

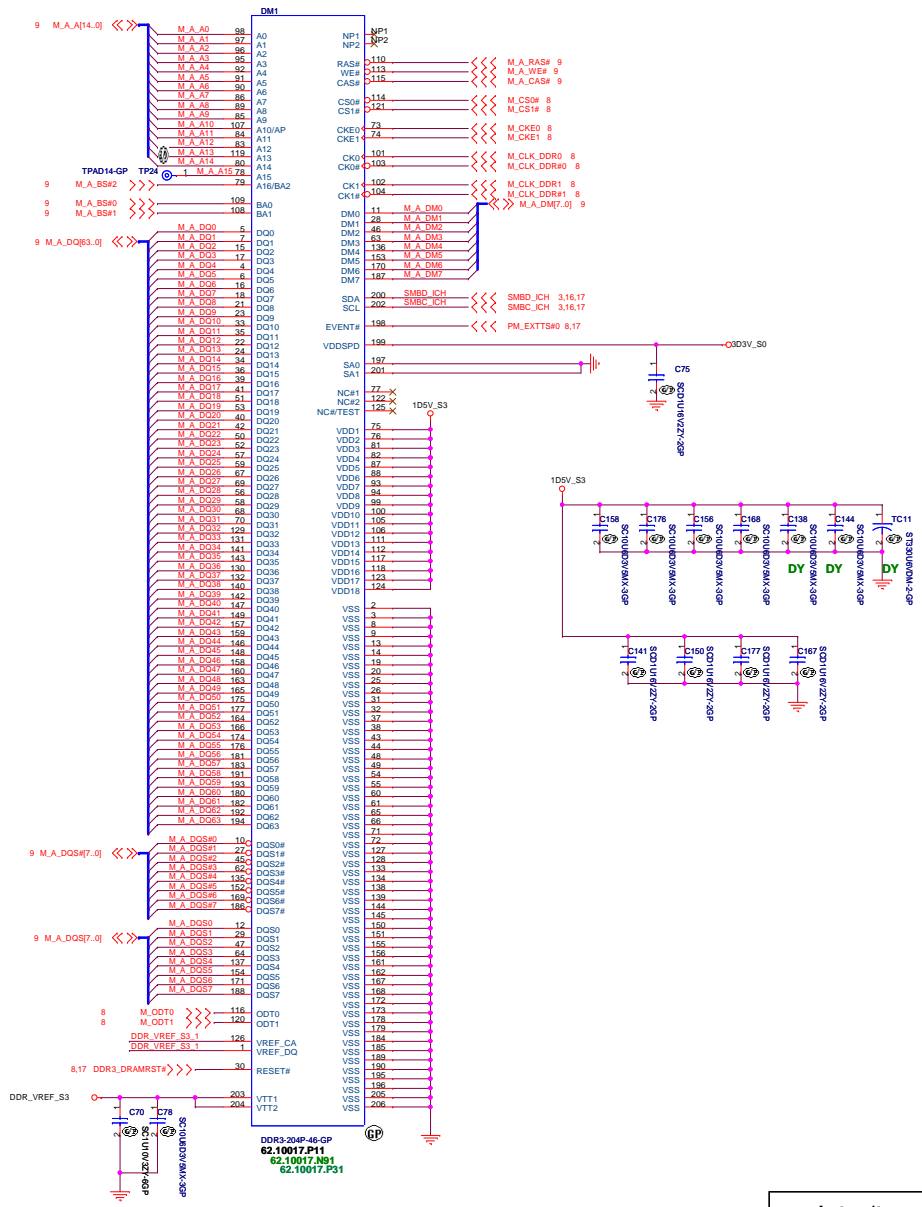
Title			Rev
ICH9-M (3 of 4)			-1
Size	Document Number	JM41 Discrete	
Date:	Monday, April 06, 2009	Sheet	15 of 48



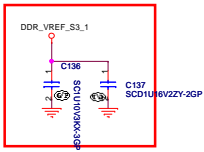
DDR3 SOCKET_1



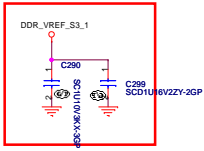
DDR3 SOCKET_2



Layout Note : Near Pin 126



Layout Note : Near Pin 1



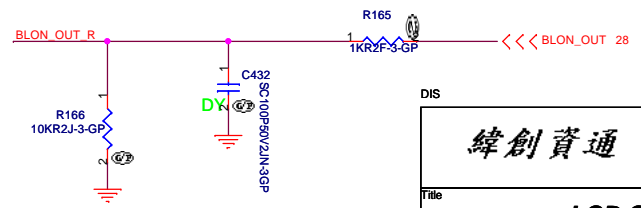
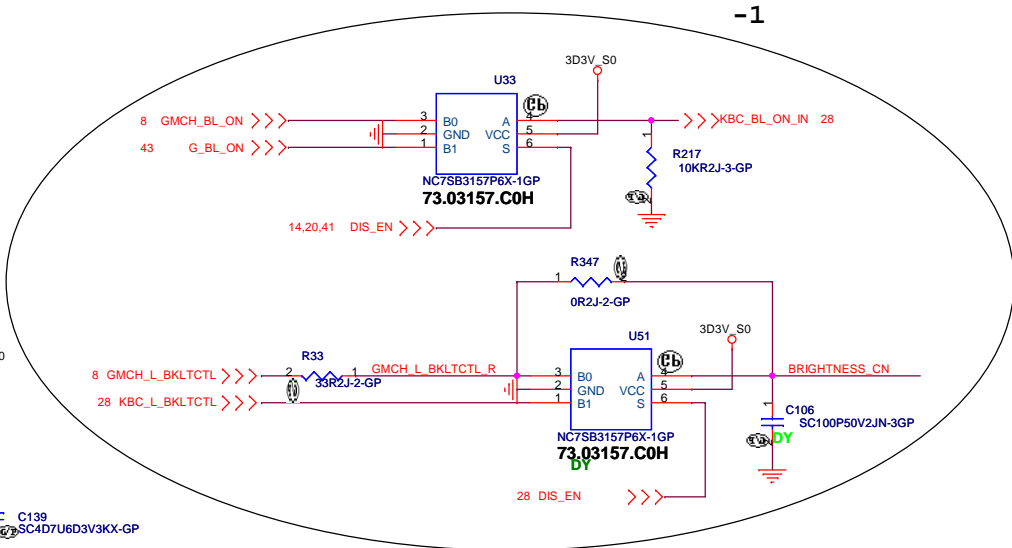
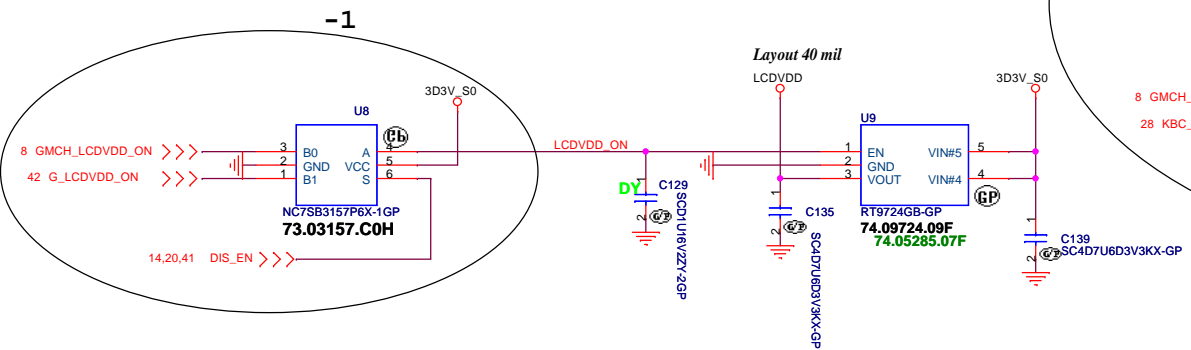
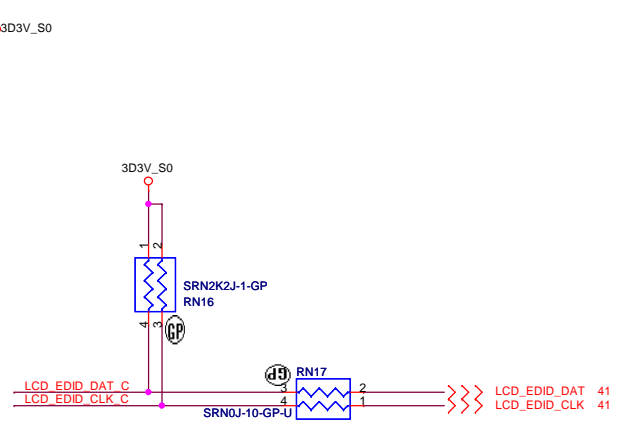
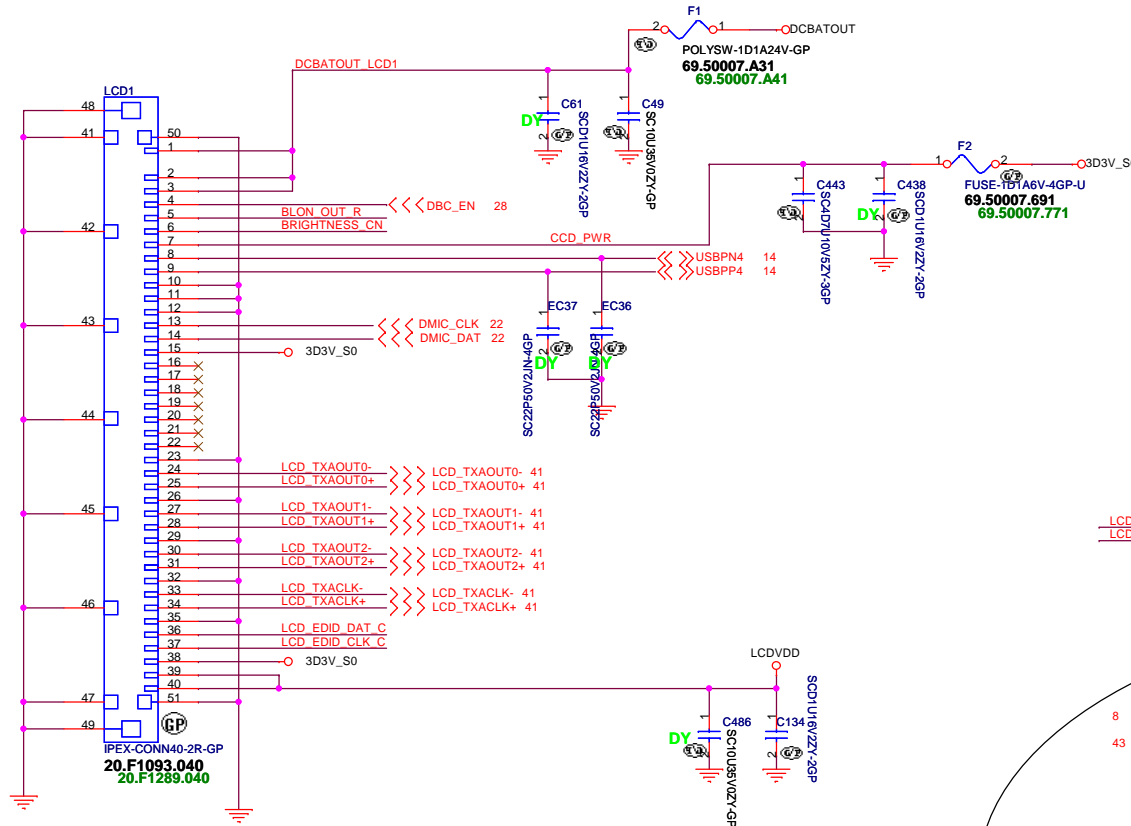
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

DDR3 Socket2
JM41 Discrete

File: **DDR3 Socket2**
 Size: Document Number
 Date: Thursday, April 09, 2009 Sheet 18 of 48

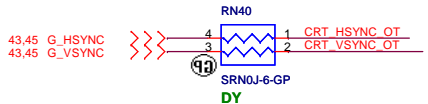
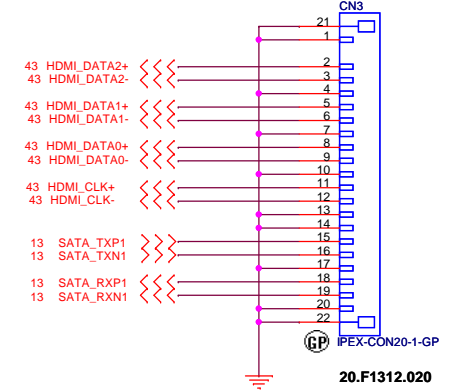
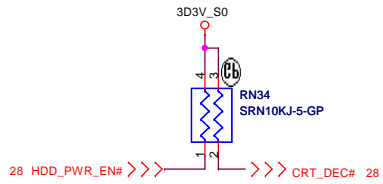
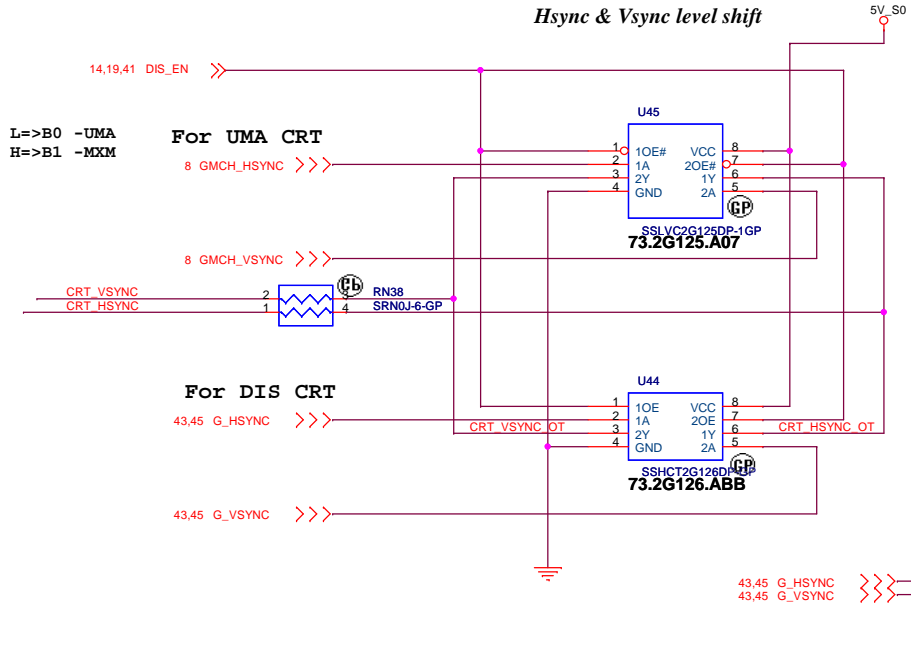
LCD/CCD CONN

Internal MIC

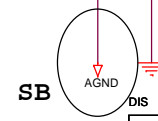
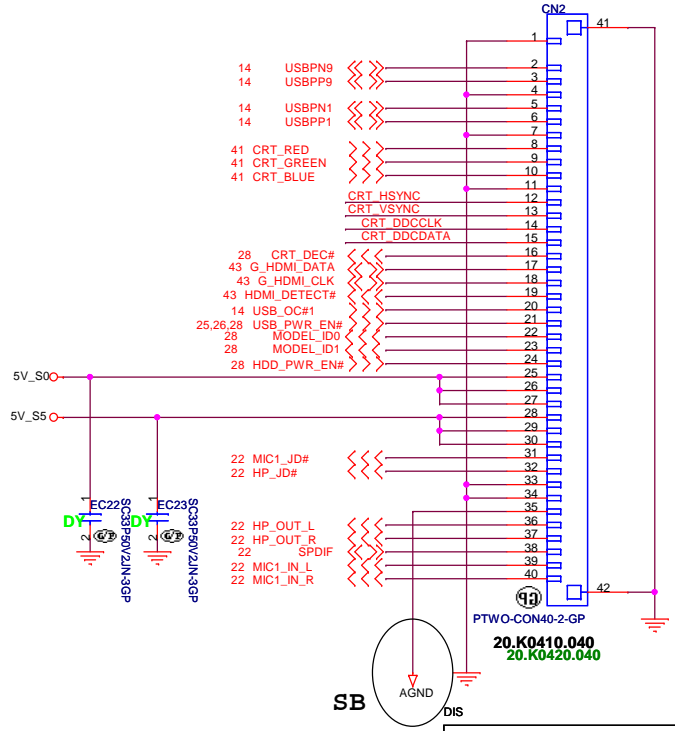
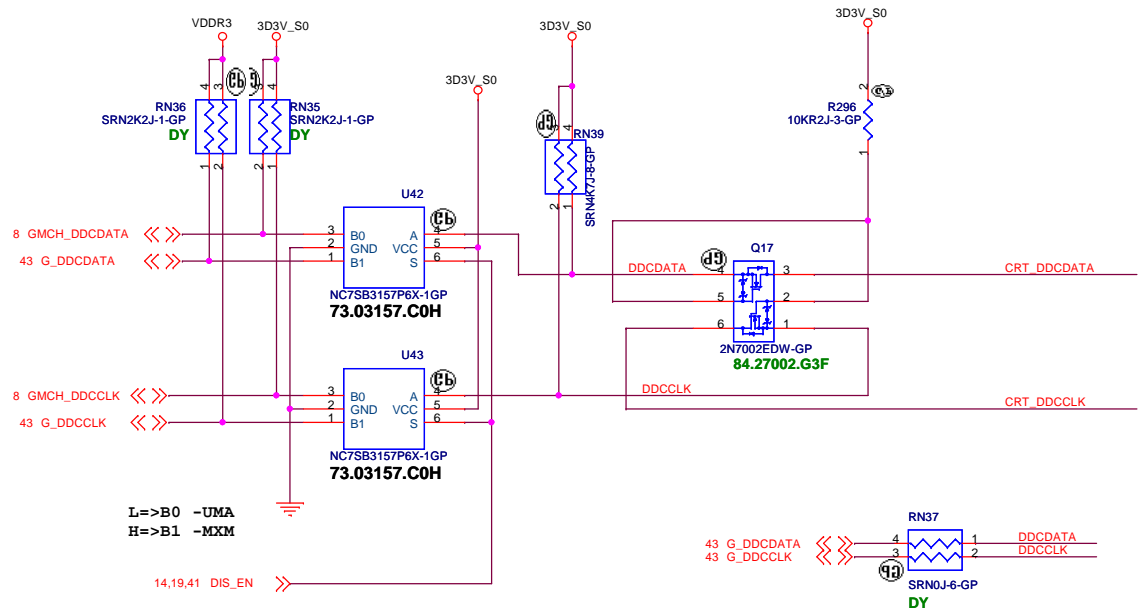


Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LCD CONN	
Size Document Number	Rev -1
JM41 Discrete	
Date: Monday, April 06, 2009 Sheet 19 of 48	

Hsync & Vsync level shift

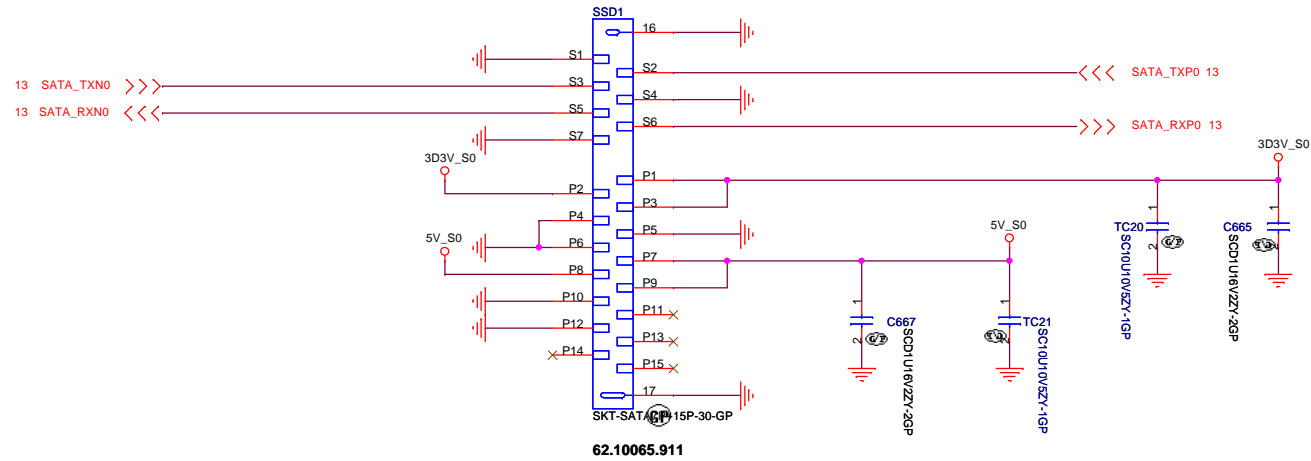


DDC_CLK & DATA level shift

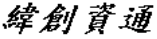


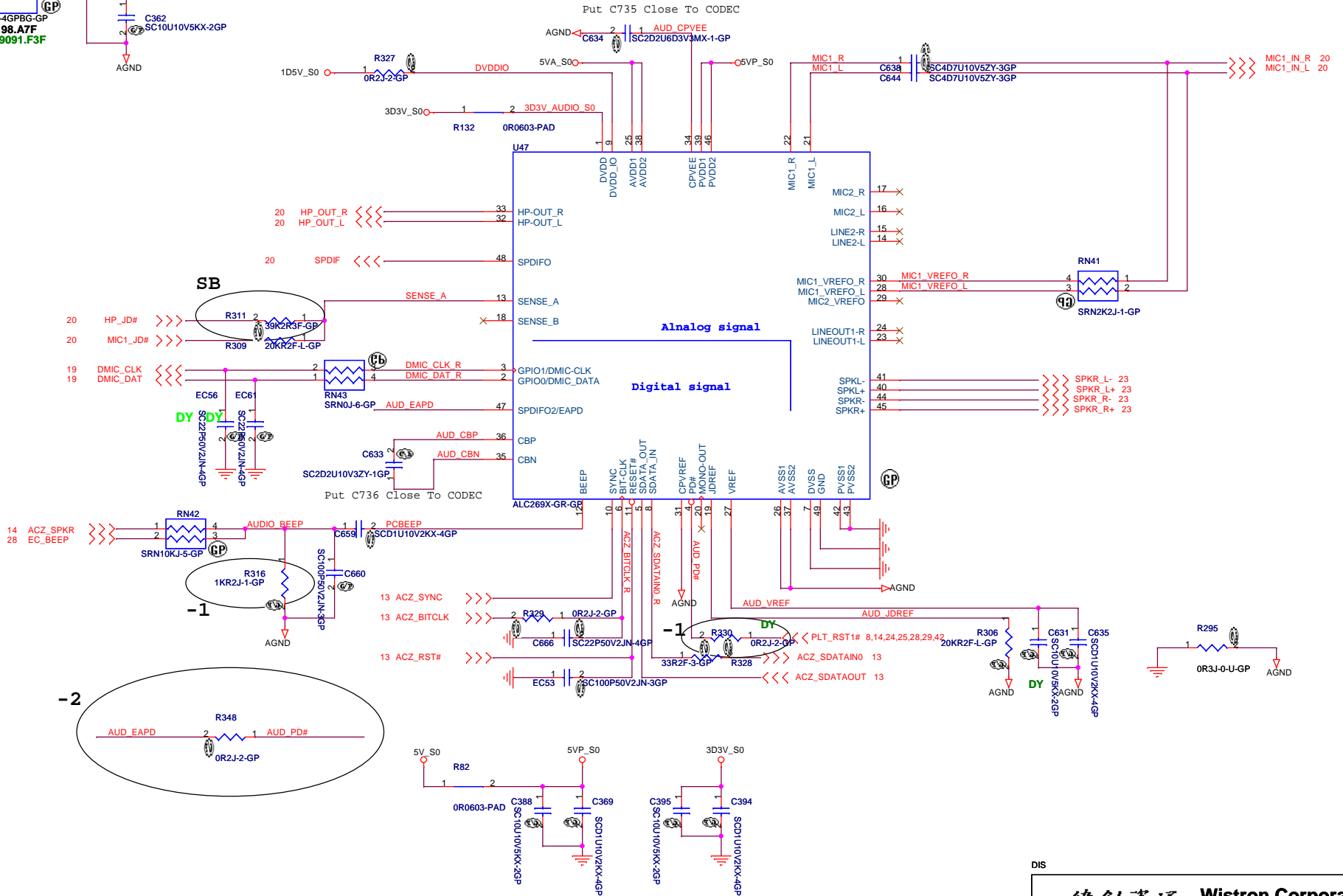
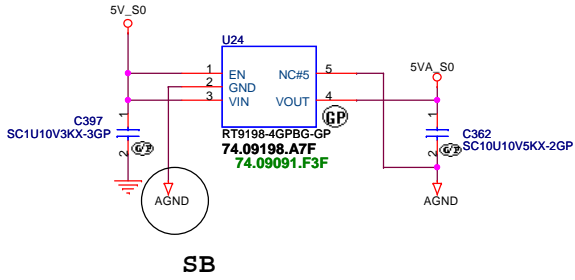
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

SSD SATA Connector

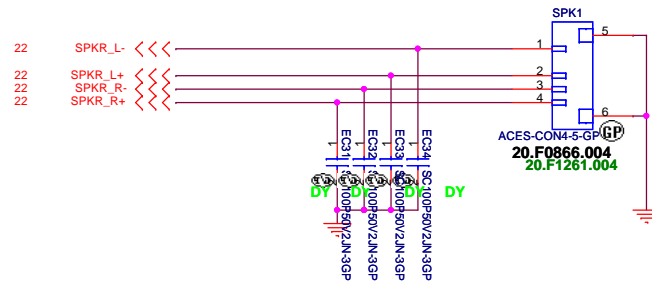


DIS

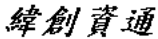
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
HDD CONN		
Size	Document Number	Rev
	JM41 Discrete	-1
Date:	Monday, April 06, 2009	Sheet 21 of 48

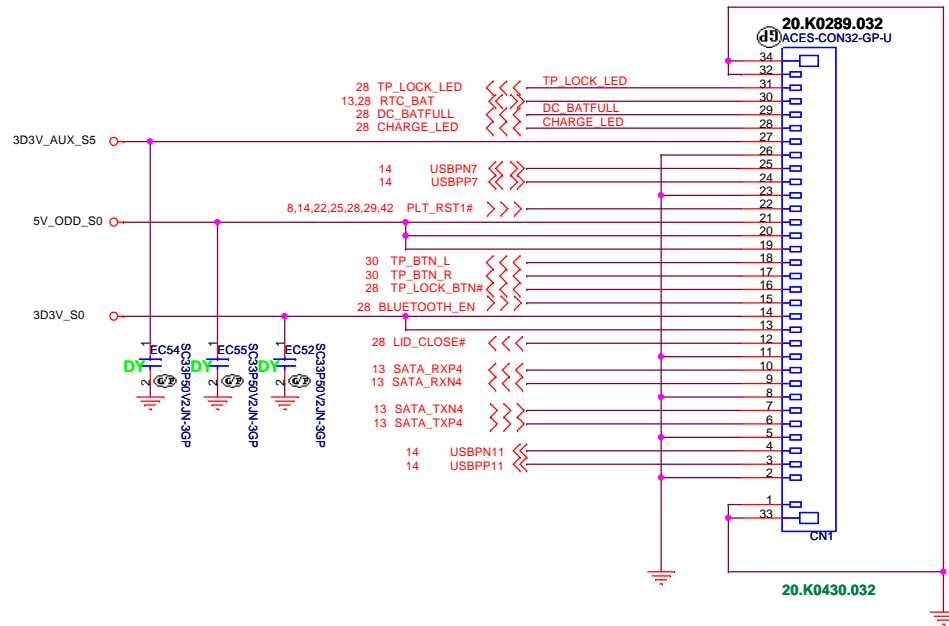


Internal Speaker

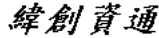


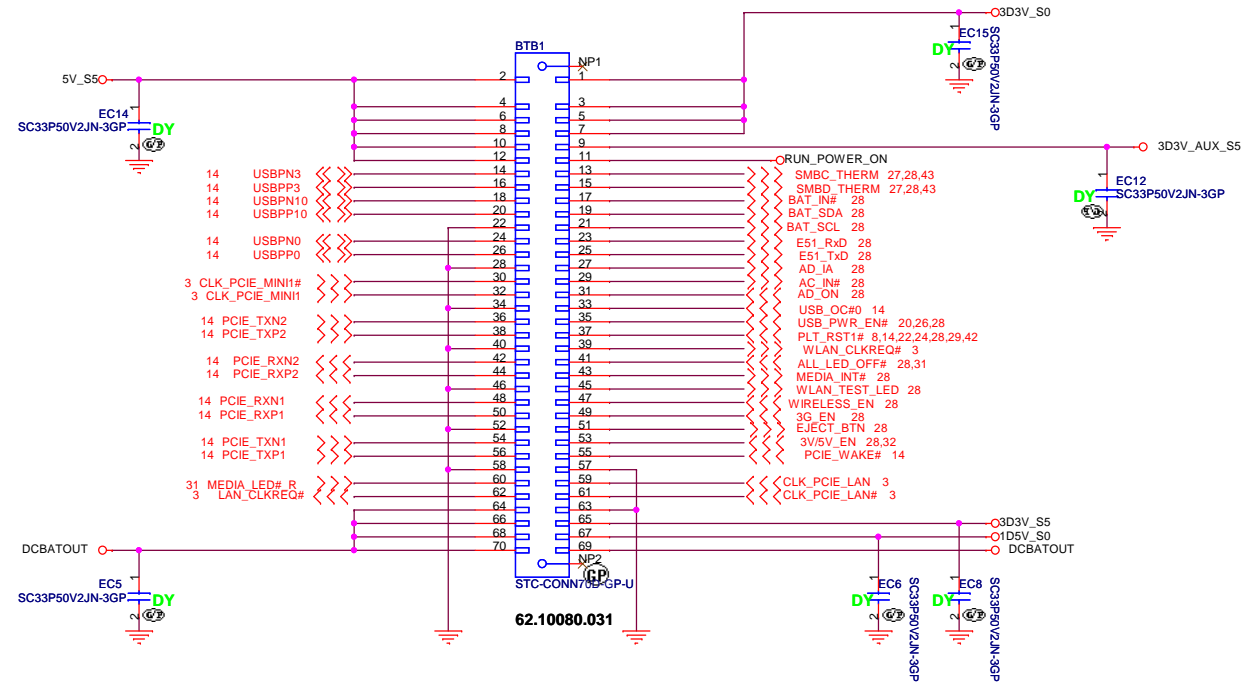
DIS

 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
AUDIO JACK	
Size	Document Number
JM41_Discrete	
Date: Monday, April 06, 2009	Rev -1
Sheet 23 of 48	



DIS

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Cardreader BD Conn		
Size	Document Number	Rev
	JM41 Discrete	-1
Date: Thursday, April 09, 2009		Sheet 24 of 48



DIS

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

MINI BD CONN

Size
A3

Document Number

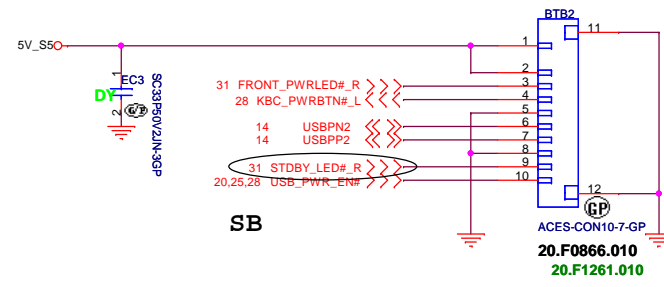
JM41_Discrete

Rev

-1

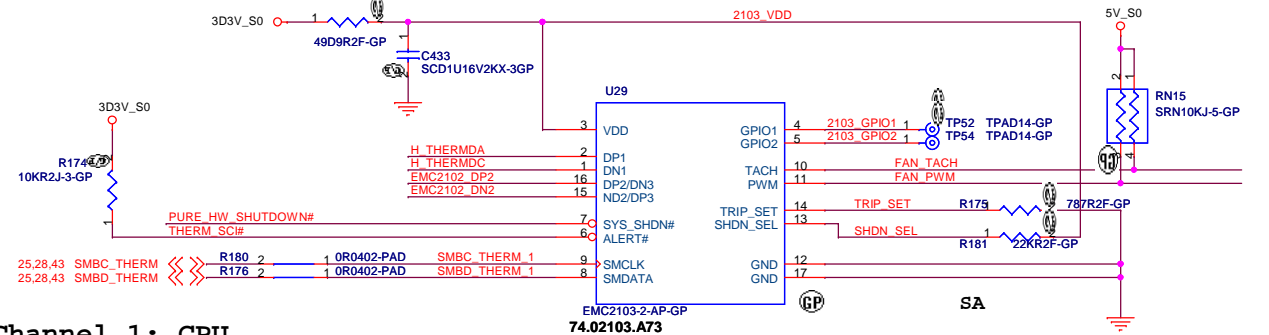
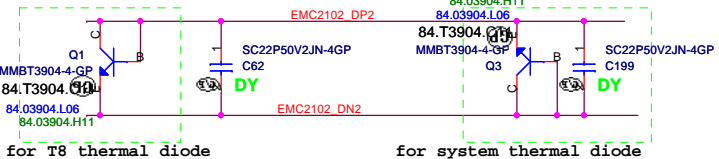
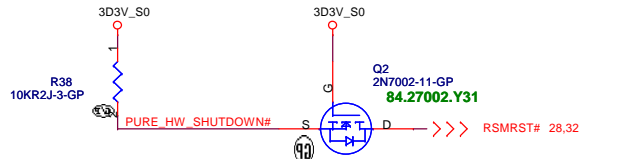
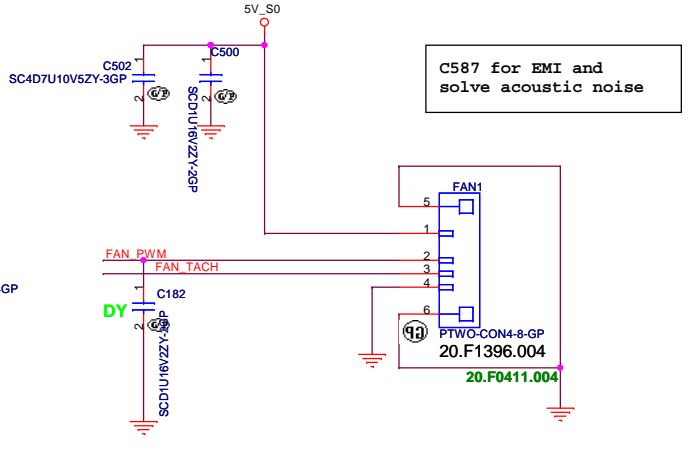
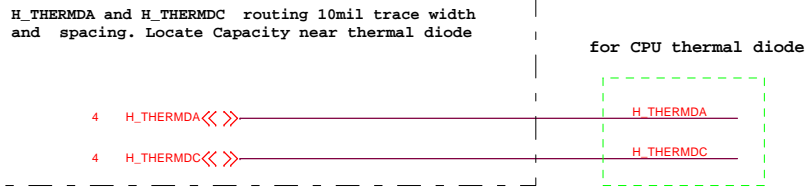
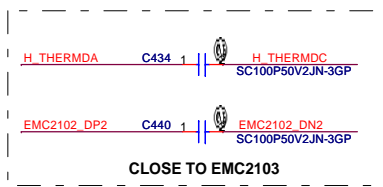
Date: Monday, April 06, 2009

Sheet 25 of 48



DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
POWER BUTTON CONN			
Size	Document Number	Rev	
A3	JM41_Discrete	-1	
Date:	Monday, April 06, 2009	Sheet	26 of 48



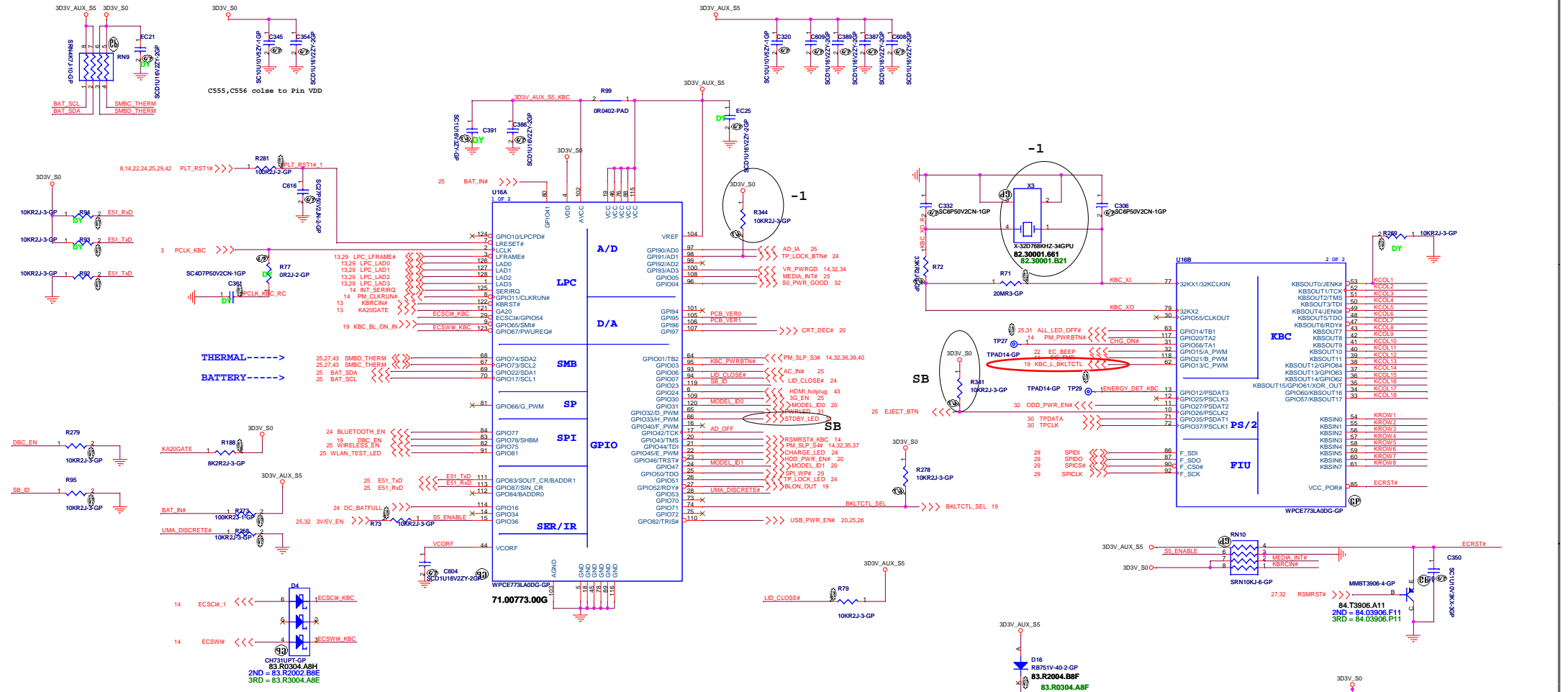
Channel 1: CPU
 Channel 2: Palmrest
 Channel 3: T8

SHDN SEL

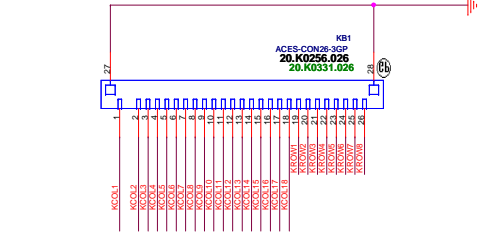
PULL UP RESISTOR	MODE OF OPERATION
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED, REC DISABLED
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED, REC ENABLED
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED
15K OHM	INTERNAL DIODE
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED

TRIP SET

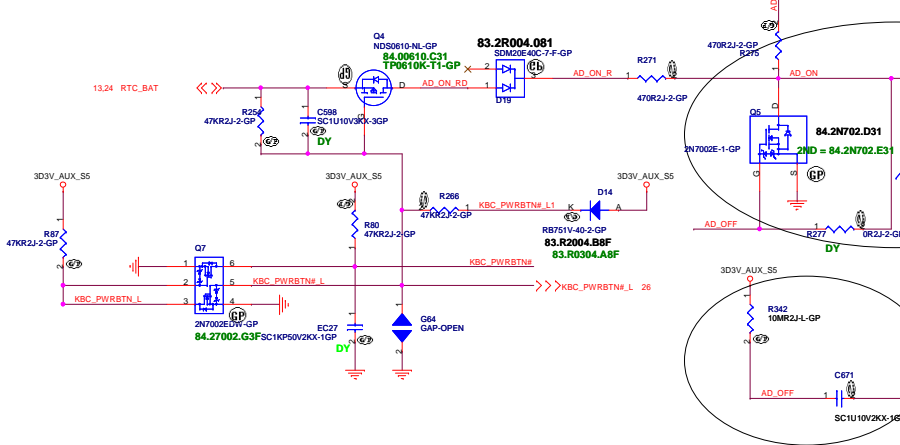
Ttrip(degree)	RSET(1%)
85	562
86	604
87	649
88	698
89	750
90	787
91	845
92	909
93	953
94	1020
95	1100

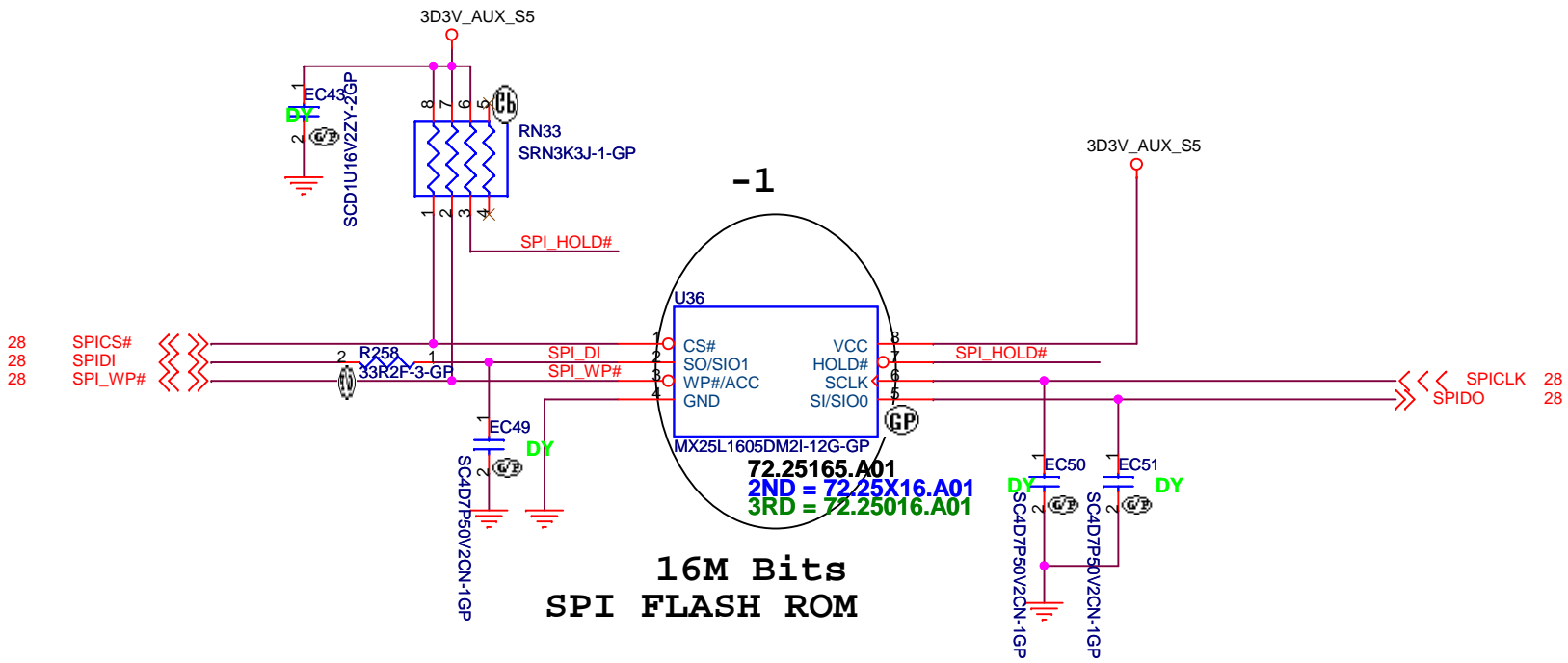


Internal Keyboard Connector

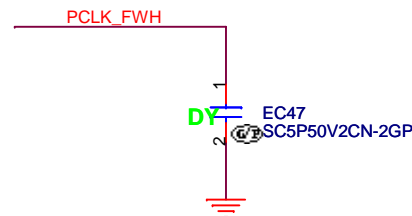
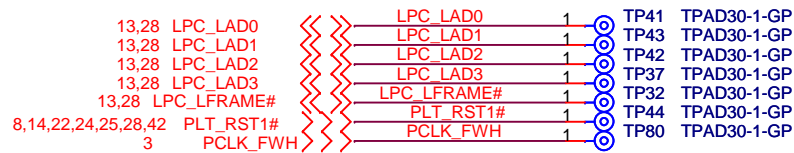


GREEN ADAPTER CIRCUIT





GOLDEN FINGER FOR DEBUG BOARD



DIS

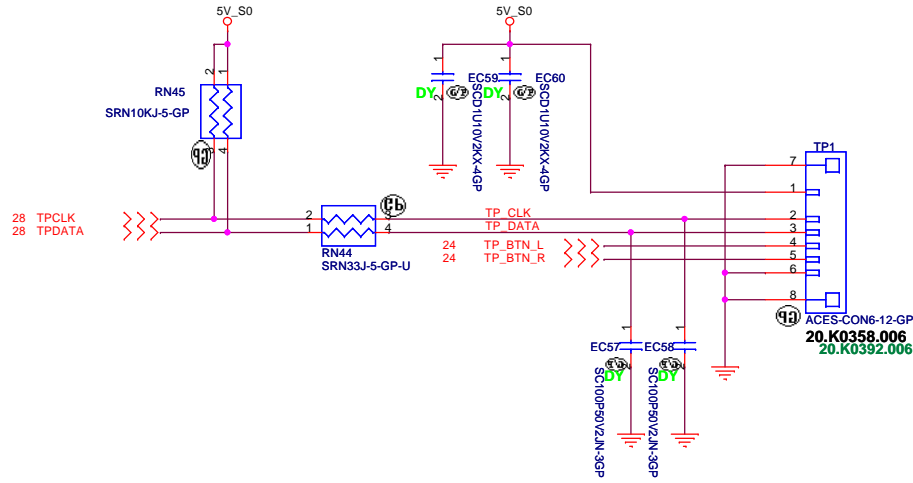
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **BIOS**

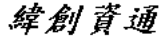
Size Document Number Rev
JM41_Discrete -1

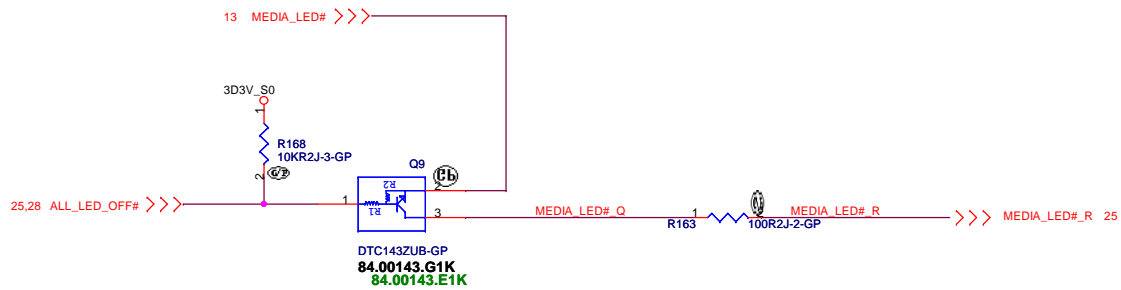
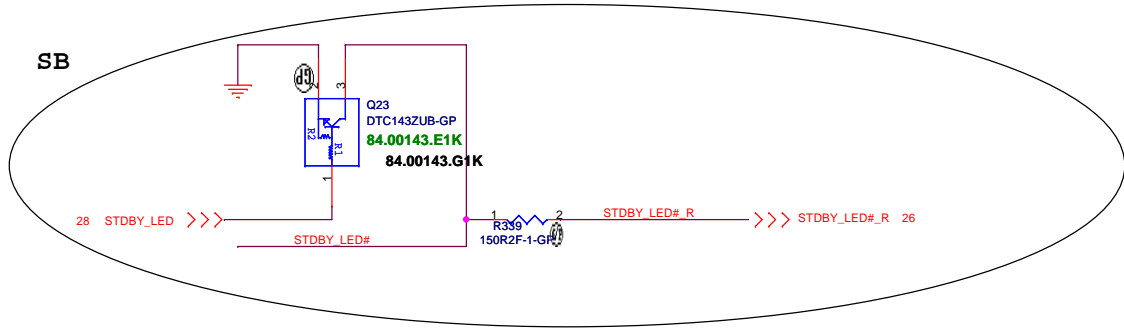
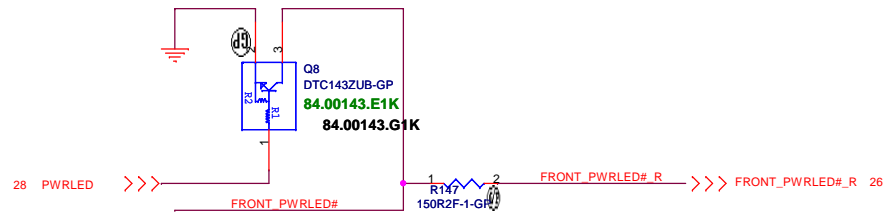
Date: Monday, April 06, 2009 Sheet 29 of 48

TOUCH PAD



DIS

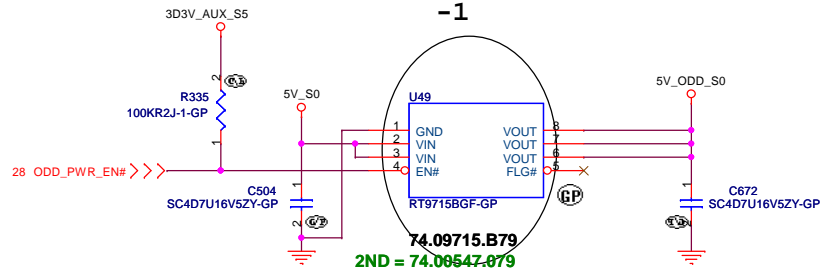
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Touch PAD		
Size	Document Number	Rev
	JM41 Discrete	-1
Date: Thursday, April 09, 2009		Sheet 30 of 48



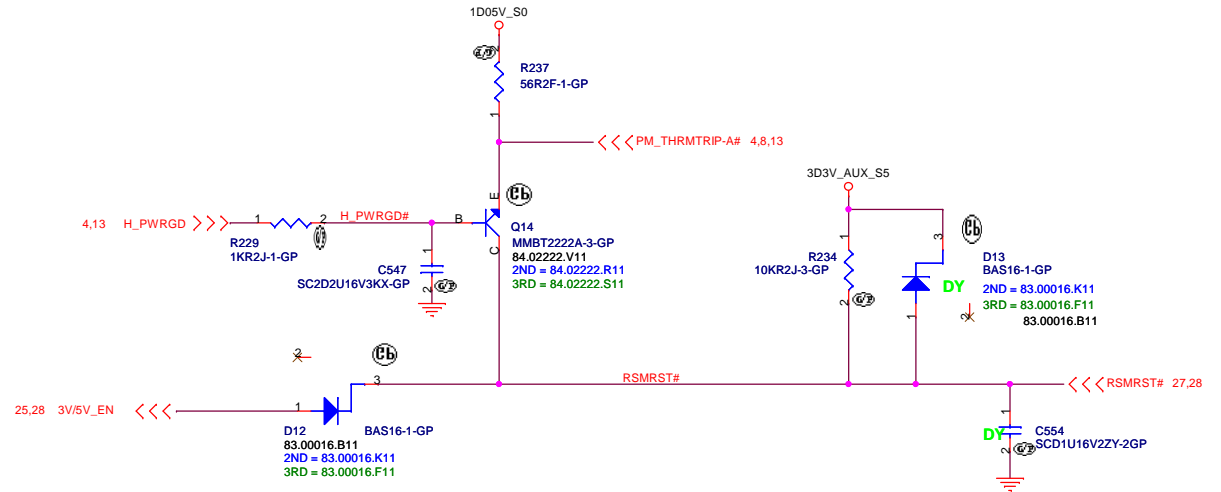
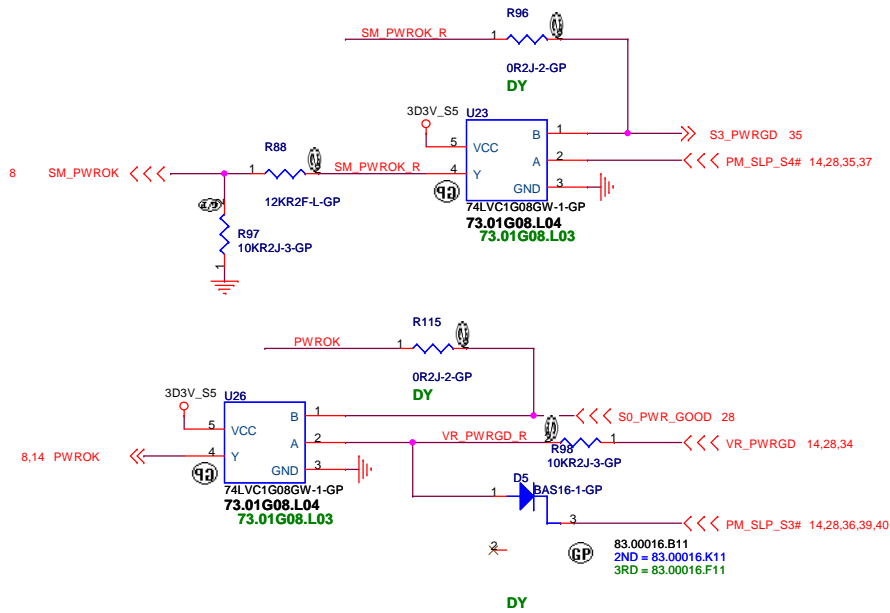
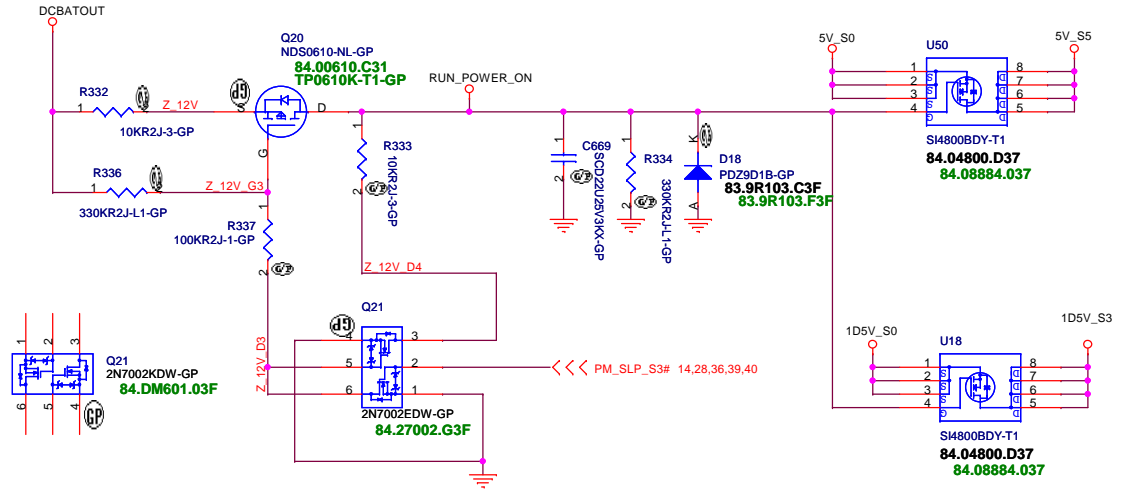
DIS

緯創資通		Wistron Corporation	
		<small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title			
LED			
Size	Document Number	Rev	
	JM41_Discrete	-1	
Date: Monday, April 06, 2009		Sheet 31 of 48	

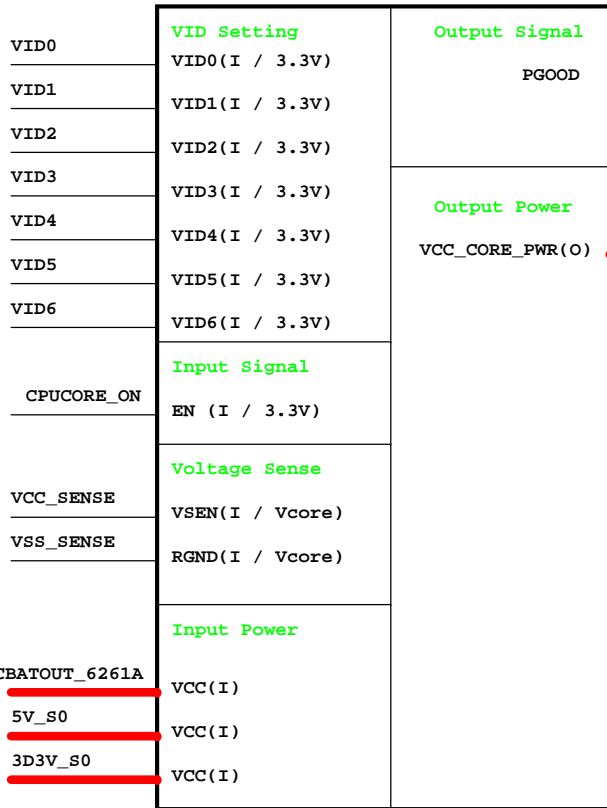
ODD Power



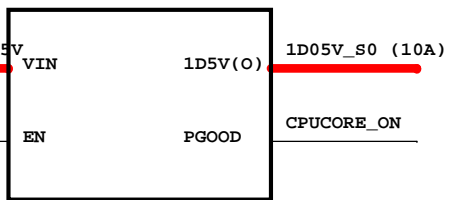
Run Power



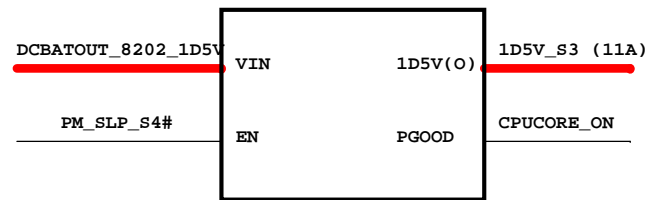
CPU_CORE
ISL6261A



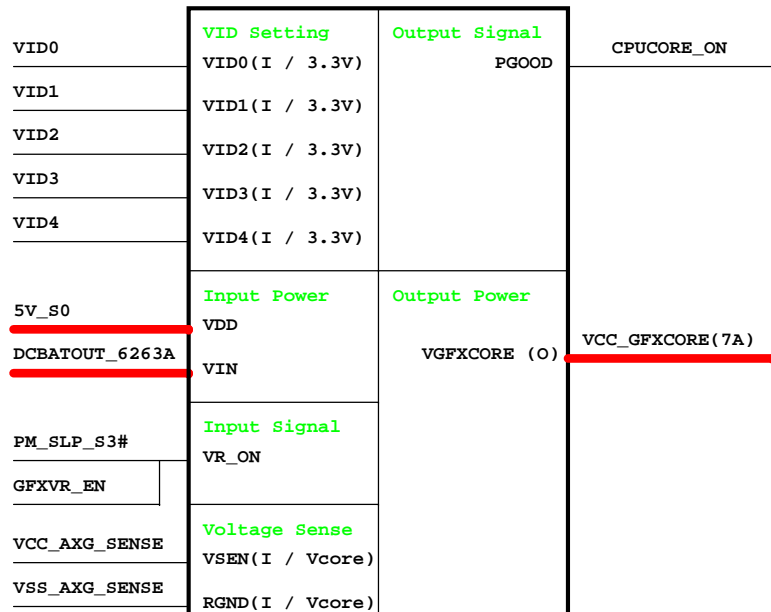
RT8202 1D05V_S0



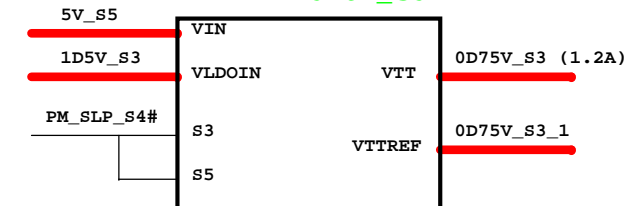
RT8202 1D5V_S3



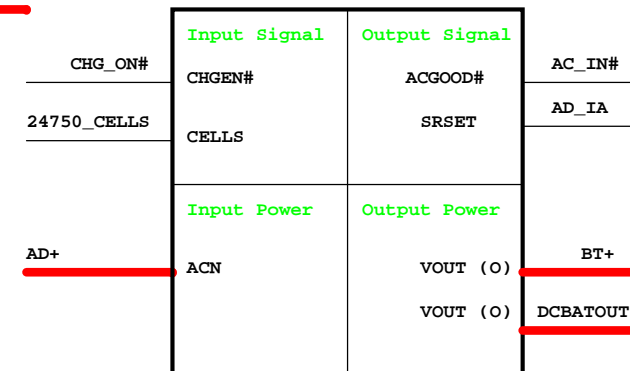
GFX_CORE
ISL6263A



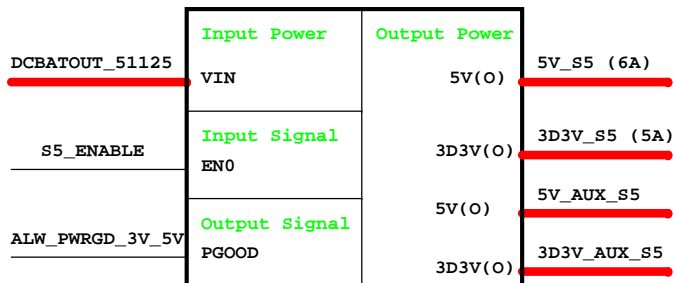
RT9026 0D9V_S0



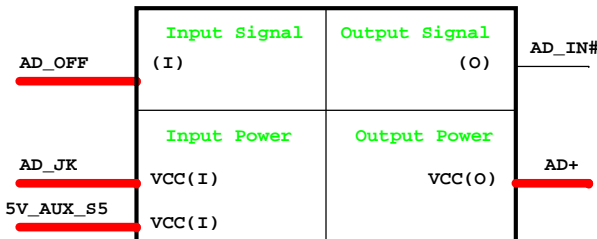
Charger MAX8731A



TPS51125
5V/3D3V

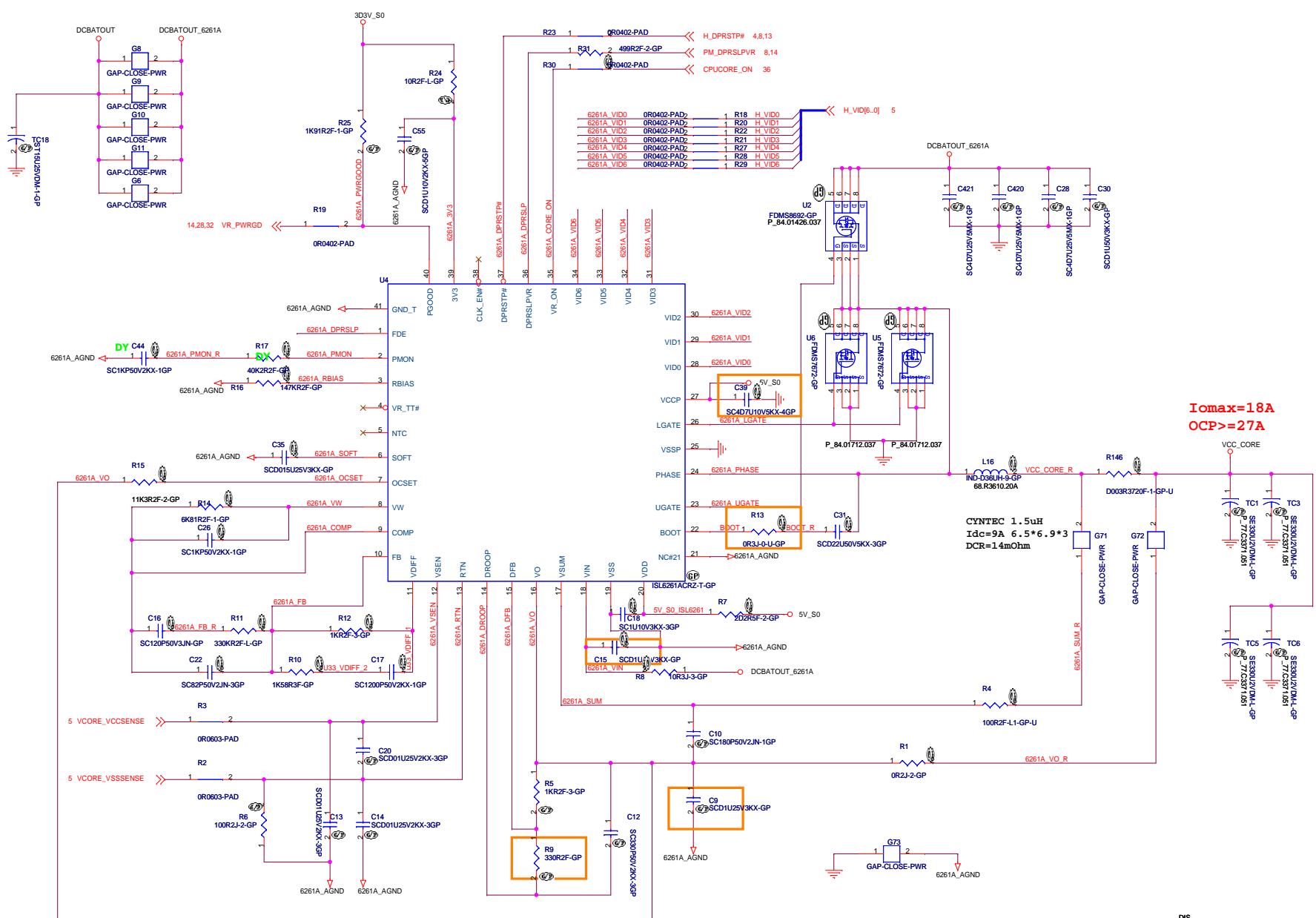


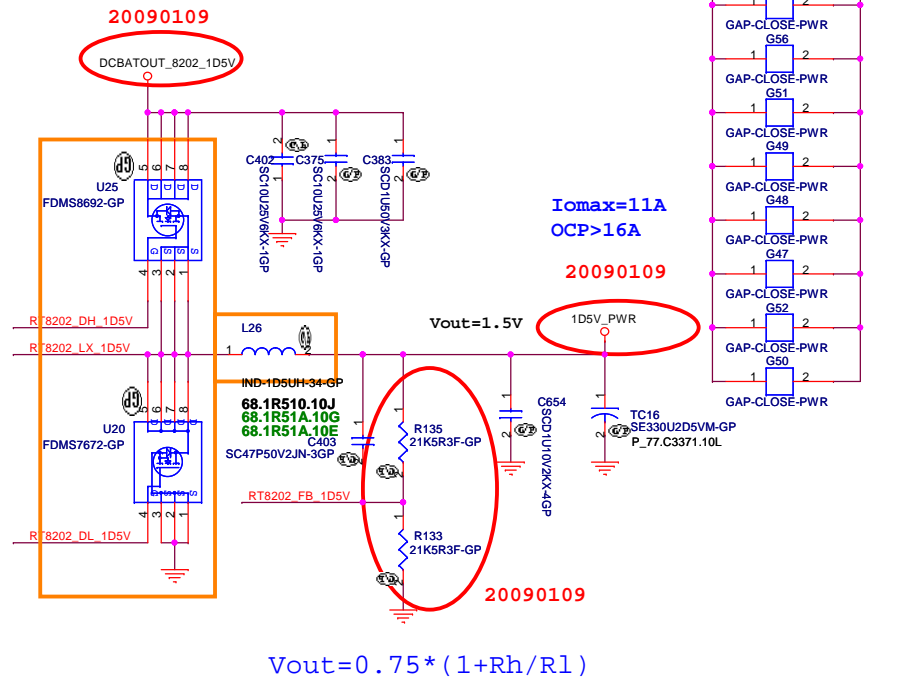
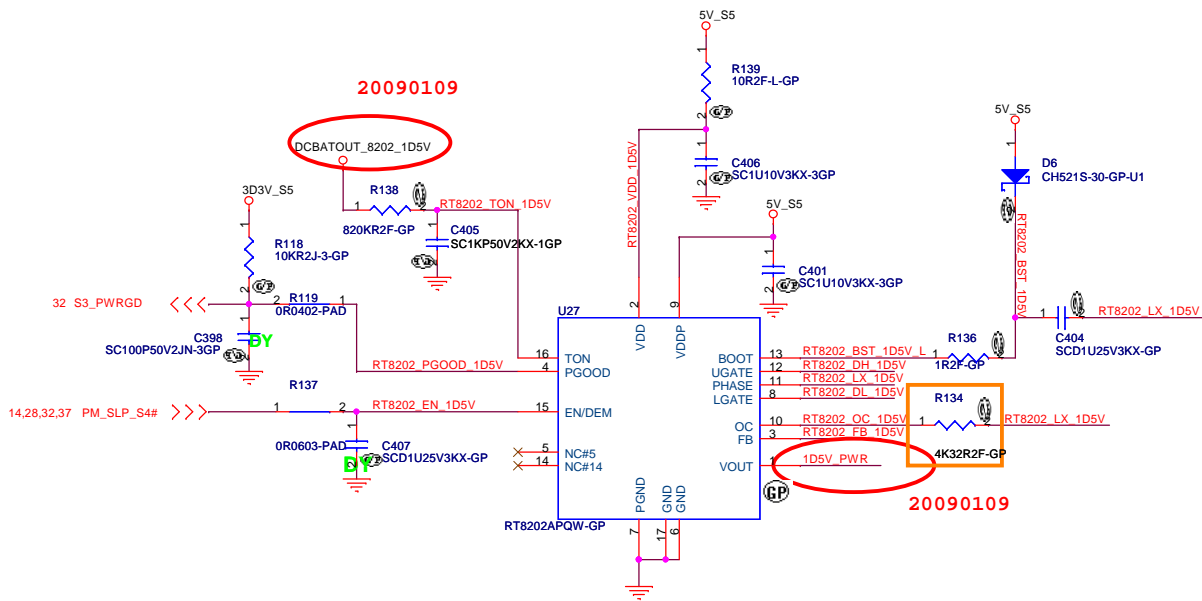
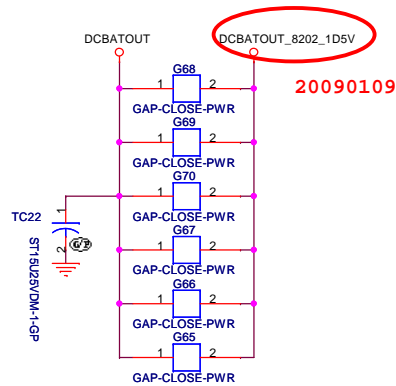
Adapter

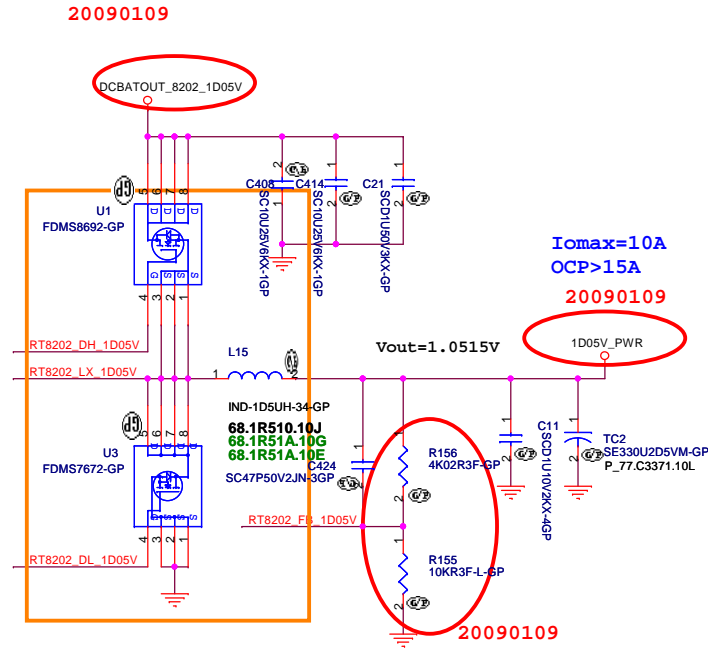
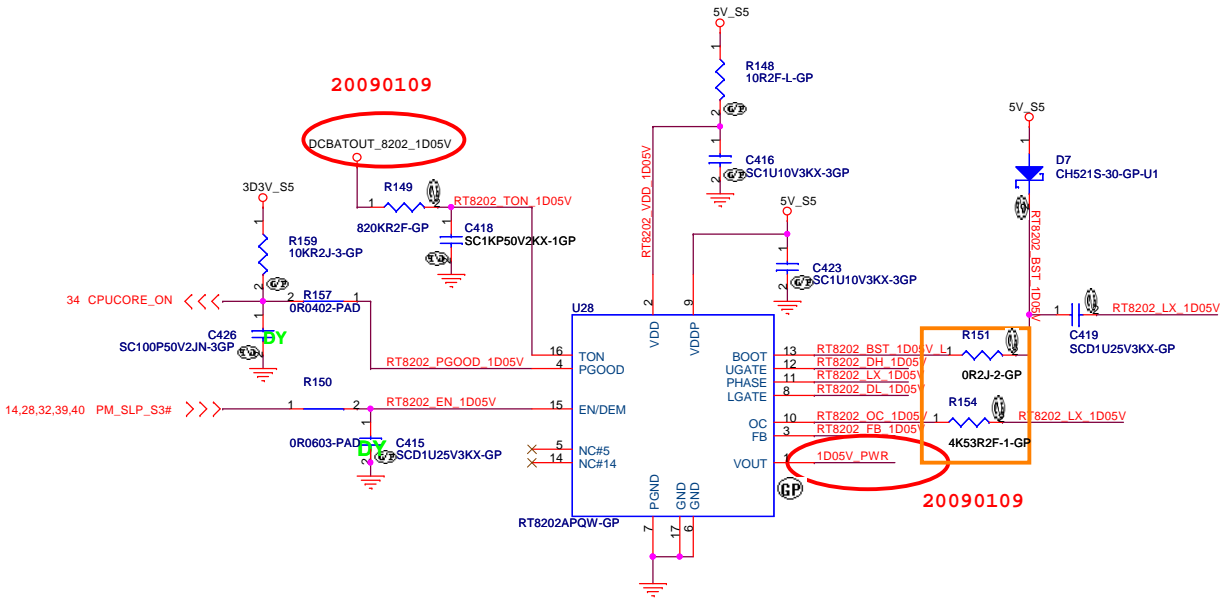
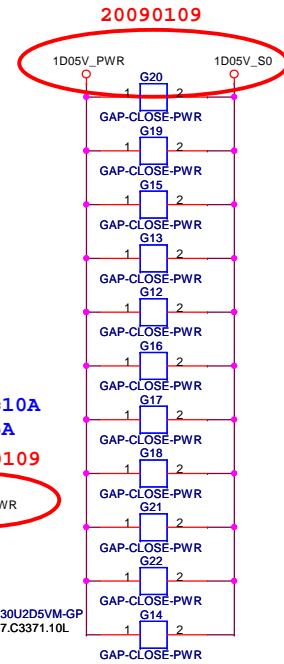
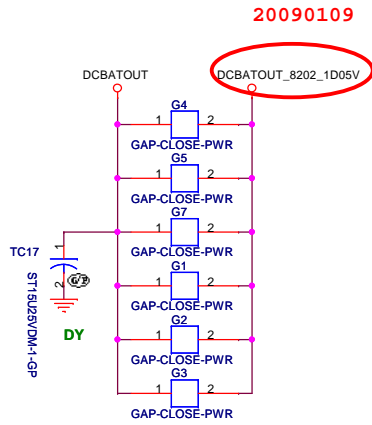


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wuj Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

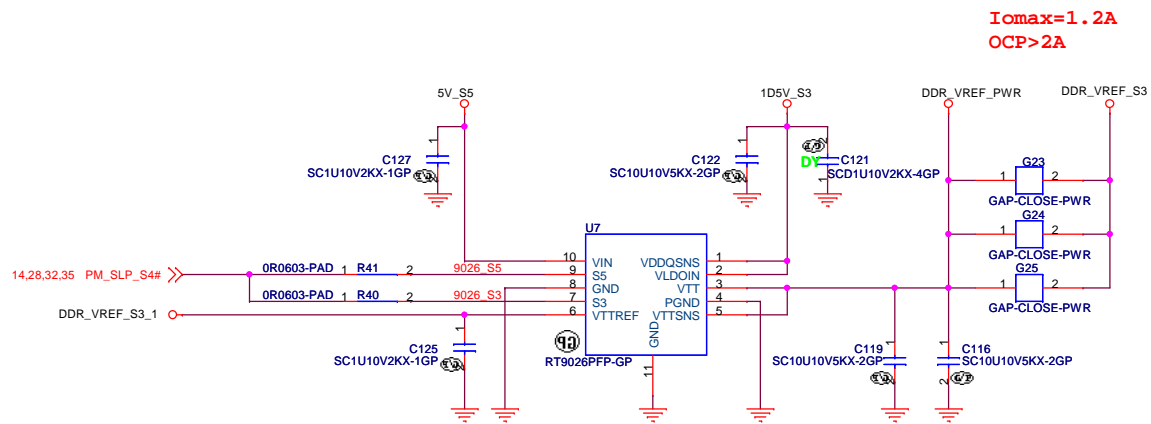
Title **Power Sequence Logic**
Size B Document Number **JM41_Discrete** Rev -1
Date: Monday, April 06, 2009 Sheet 33 of 48



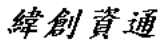


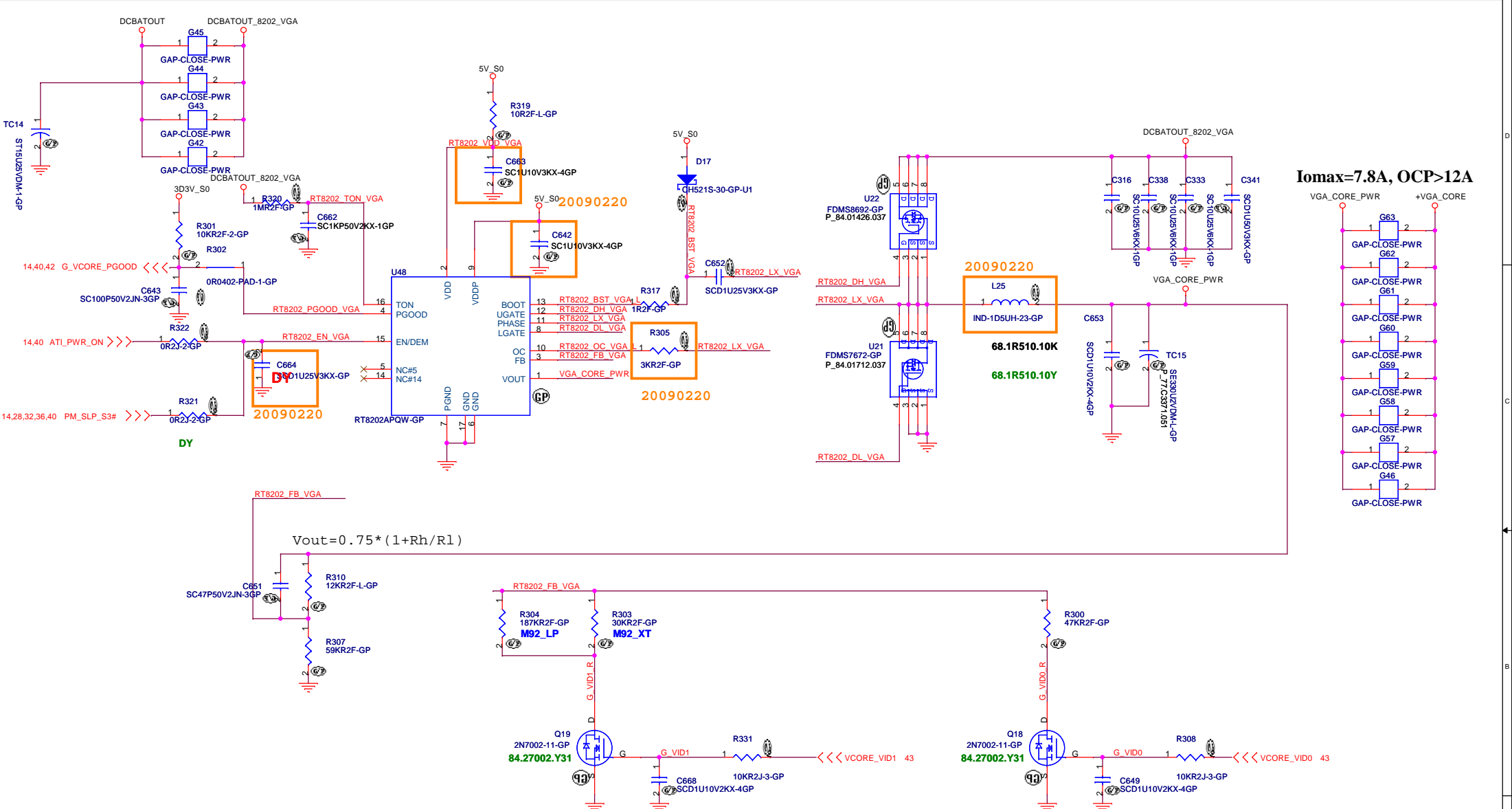


$V_{out} = 0.75 * (1 + R_h/R_l)$



DIS

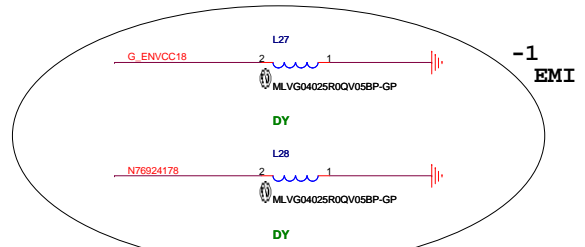
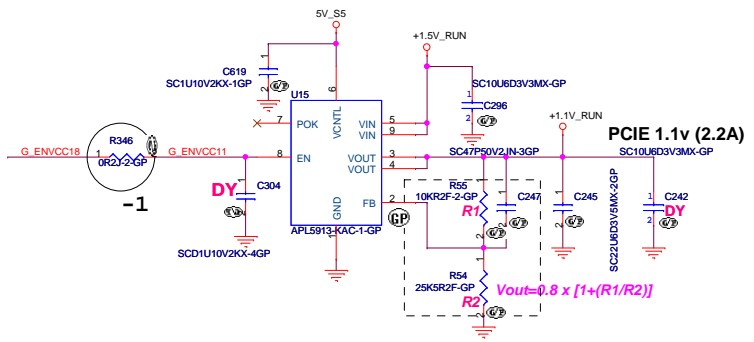
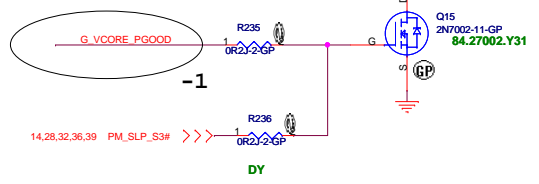
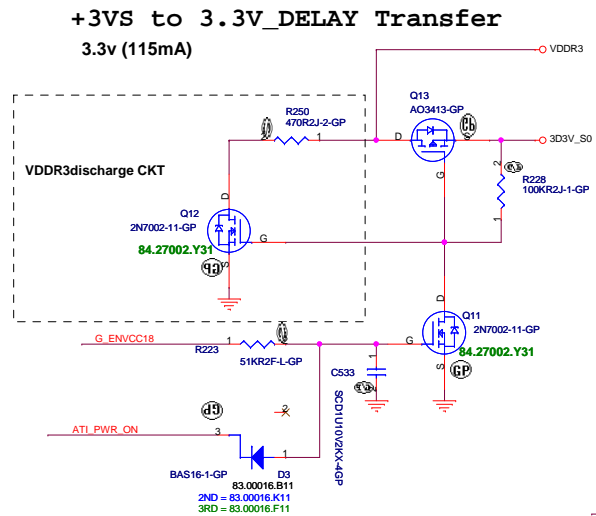
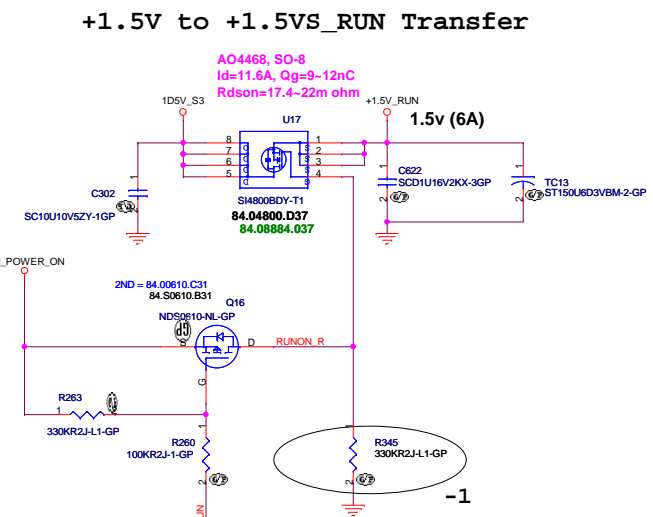
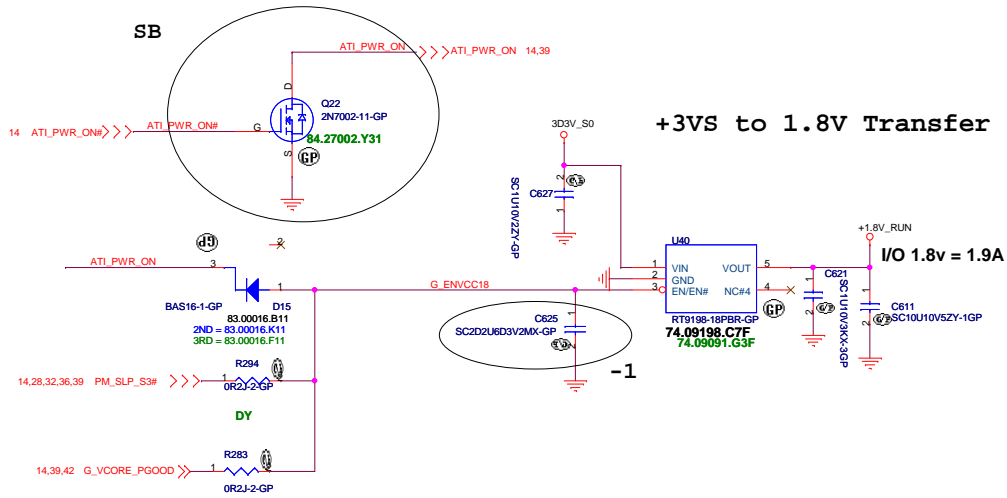
 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
RT9026 0D75V		
Size A3	Document Number JM41 Discrete	Rev -1
Date: Monday, April 06, 2009		Sheet 37 of 48



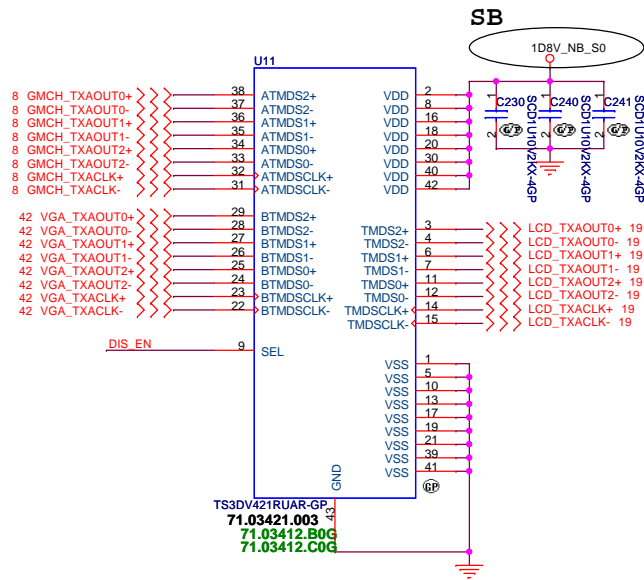
Iomax=7.8A, OCP>12A

$$V_{out} = 0.75 * (1 + R_h/R_l)$$

M92_LP core power			M92_XT core power		
ALTV1	ALTV0	Vout	ALTV1	ALTV0	Vout
0	0	0.90V	0	0	0.90V
0	1	1.09V	0	1	1.09V
1	0	0.95V	1	0	1.2V

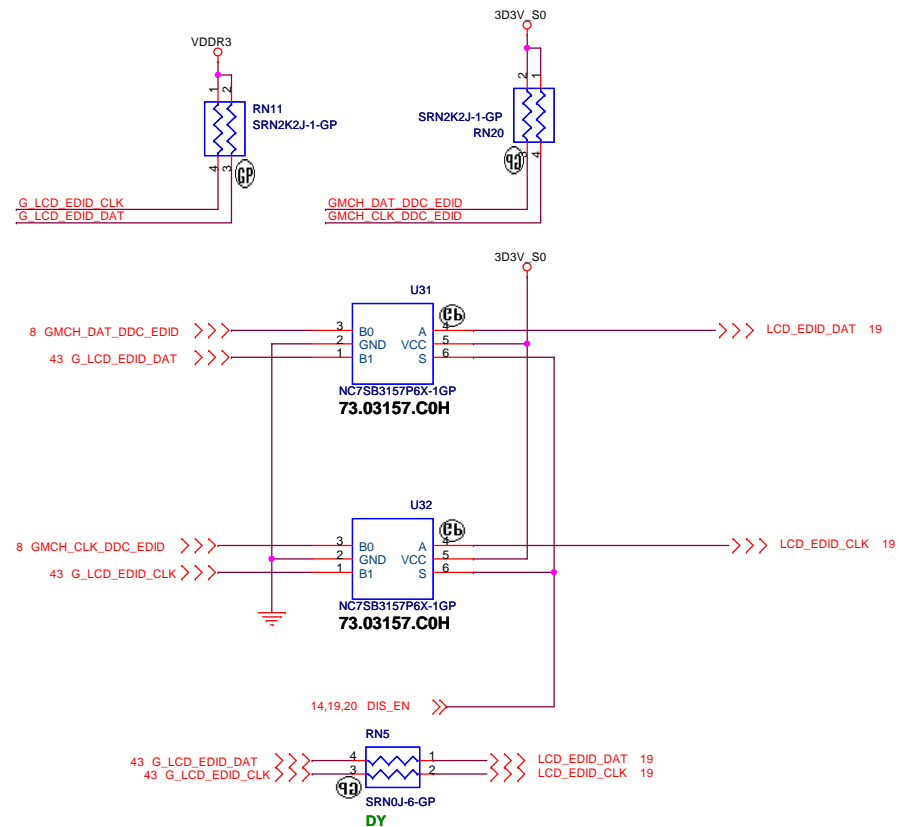


緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.	
Title	
M92S2 power	
Size	Document Number
Custom	JM41_Discrete
Date: Monday, April 13, 2009	Sheet 40 of 48
	Rev -1

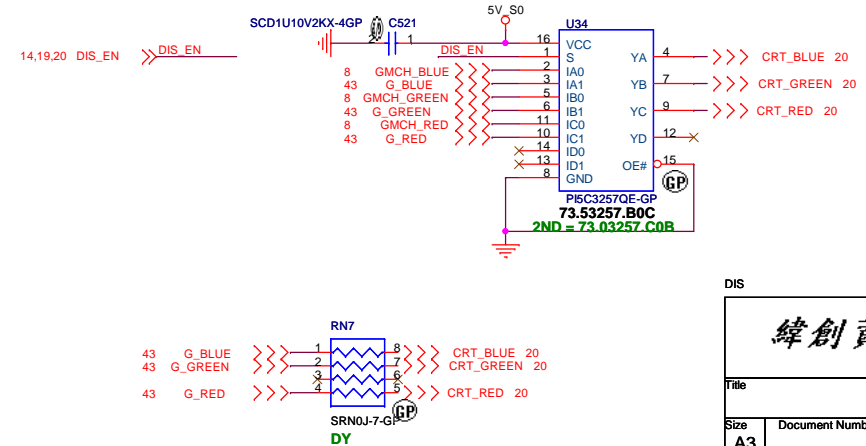


FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-



\bar{E}	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1



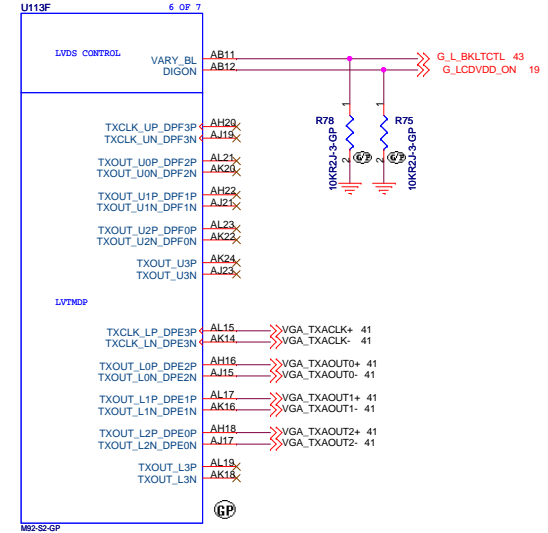
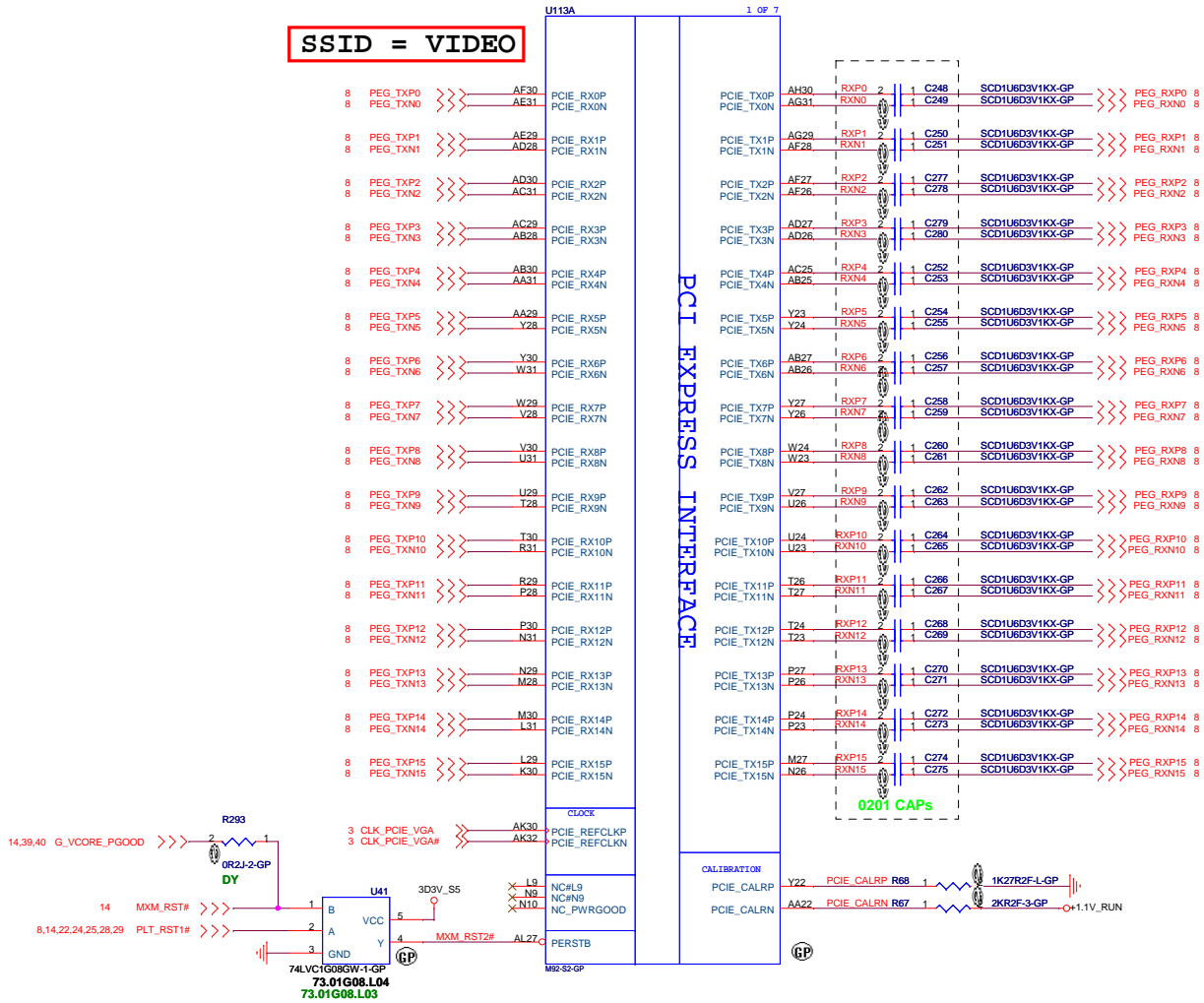
DIS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PX SWITCH**

Size: A3	Document Number:	Rev: -1
Date: Monday, April 06, 2009	Sheet: 41	of: 48

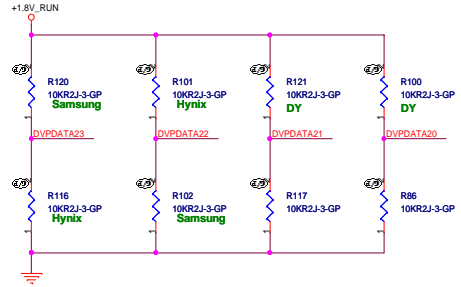
SSID = VIDEO



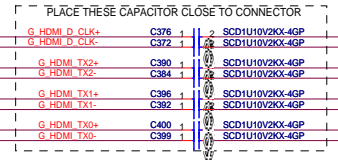
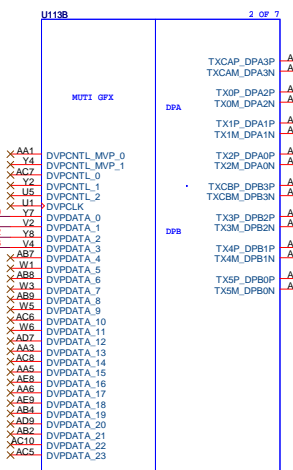
DIS

SSID = VIDEO

DVPDATA [3:0]
 0100 64Mx16 Hynix
 1000 64Mx16 Samsung



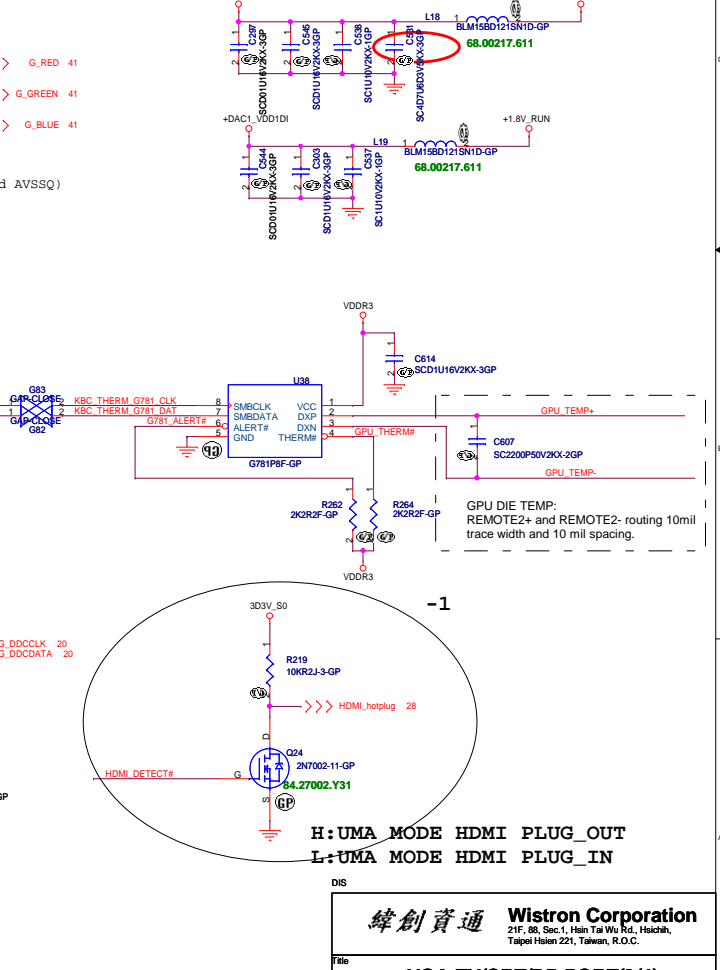
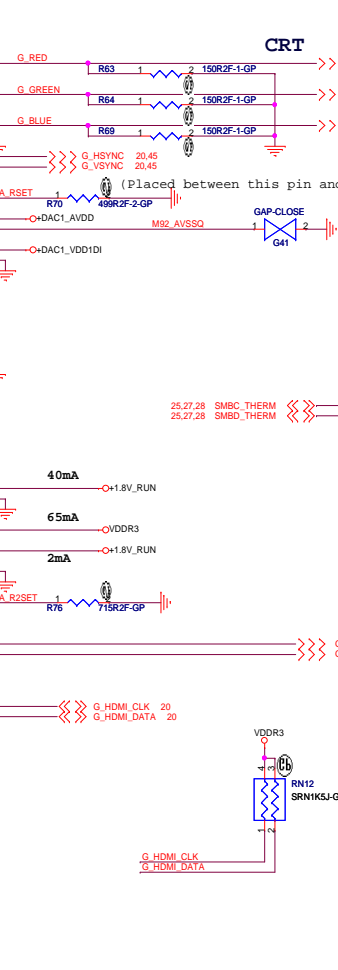
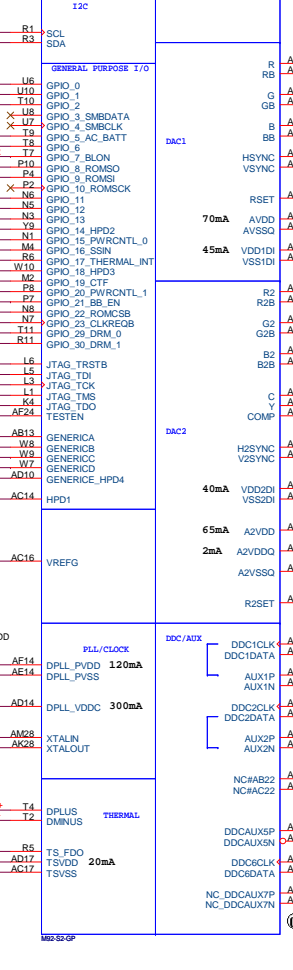
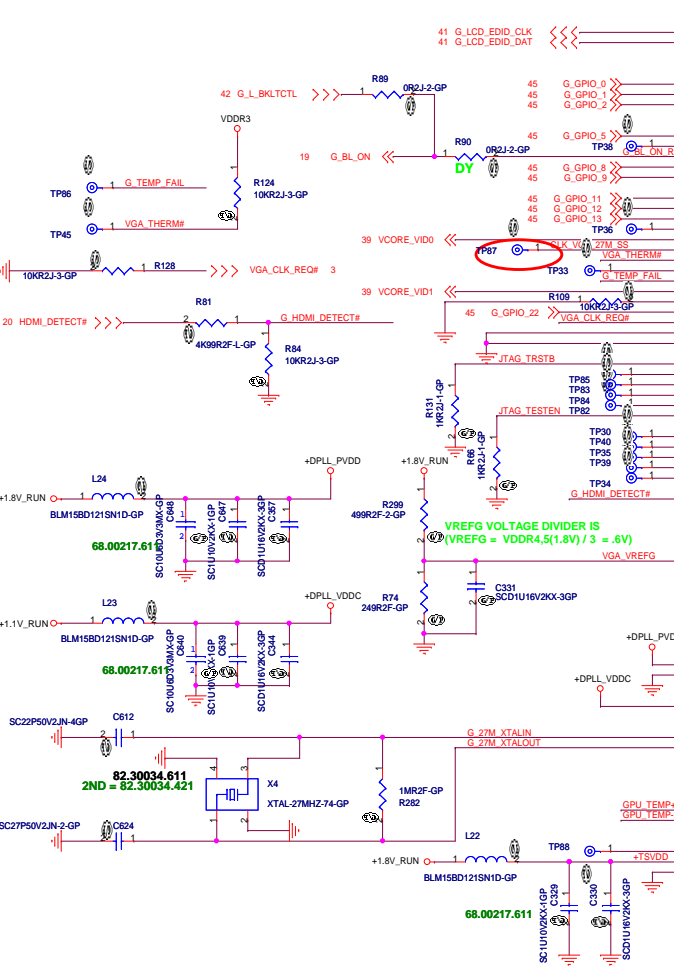
STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPDATA(23:20)	MEMORY TYPE, MAKE AND SIZE INFO
	(Internal PD)	
	0000	- GDDR3 16Mx32 Qimonda
	0001	- GDDR3 32Mx32 Hynix
	0010	- GDDR3 32Mx32 Qimonda
	0011	- GDDR3 32Mx32 Samsung



PLACE THESE CAPACITORS CLOSE TO CONNECTOR

PLACE THESE RESISTORS CLOSE TO DIFF. PAIRS AND AVOID STUBS TO ALL DIFF. TRACES.

MINIMIZE THE DISTANCE BETWEEN THESE RES. AND 100nF AC CAPS

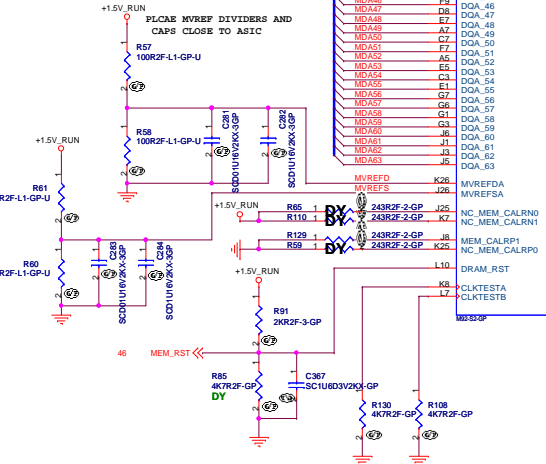


H:UMA MODE HDMI PLUG_OUT
 L:UMA MODE HDMI PLUG_IN

SSID = VIDEO

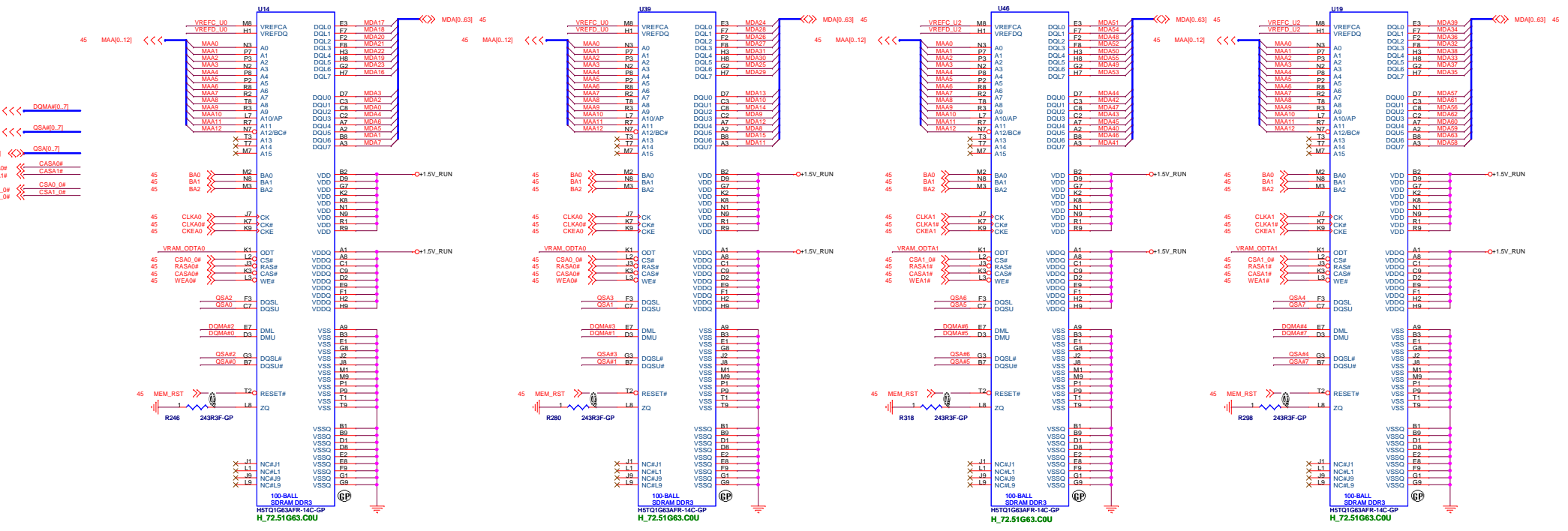
MVDDQ=1.5V FOR DDR3 MEMORY

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
BIF_CLK_PM_EN	GPIO8	0= Disable CLKREQ# power management capability 1= Enable CLKREQ# power management capability
ROMIDCFG[3:0]	GPIO[13,12,11]	if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type (Internal PD) if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1]	VGA_HS2SYNC	AUD[1:0] 00: No audio function
AUD[0]	VGA_VS2SYNC	01: Audio for DisplayPort and HDMI (if adapter is detected) 10: Audio for DisplayPort only 11: Audio for both DisplayPort and HDMI

512MB DDR3

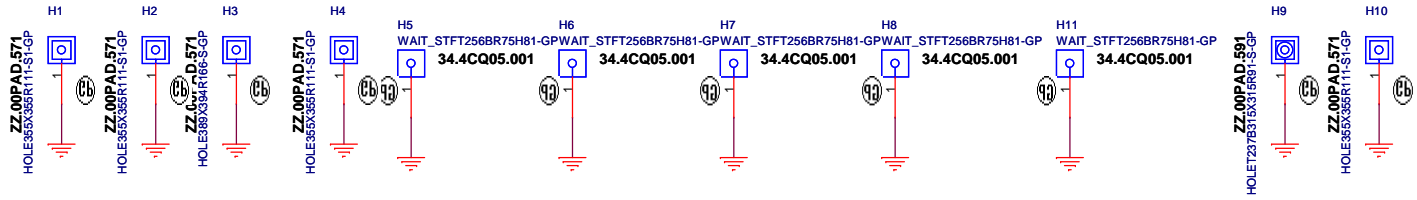
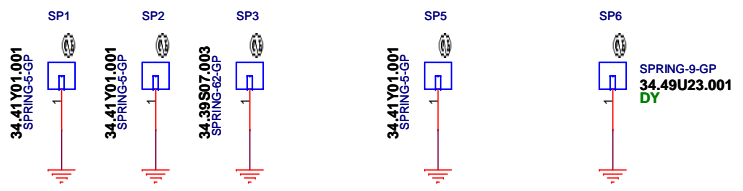
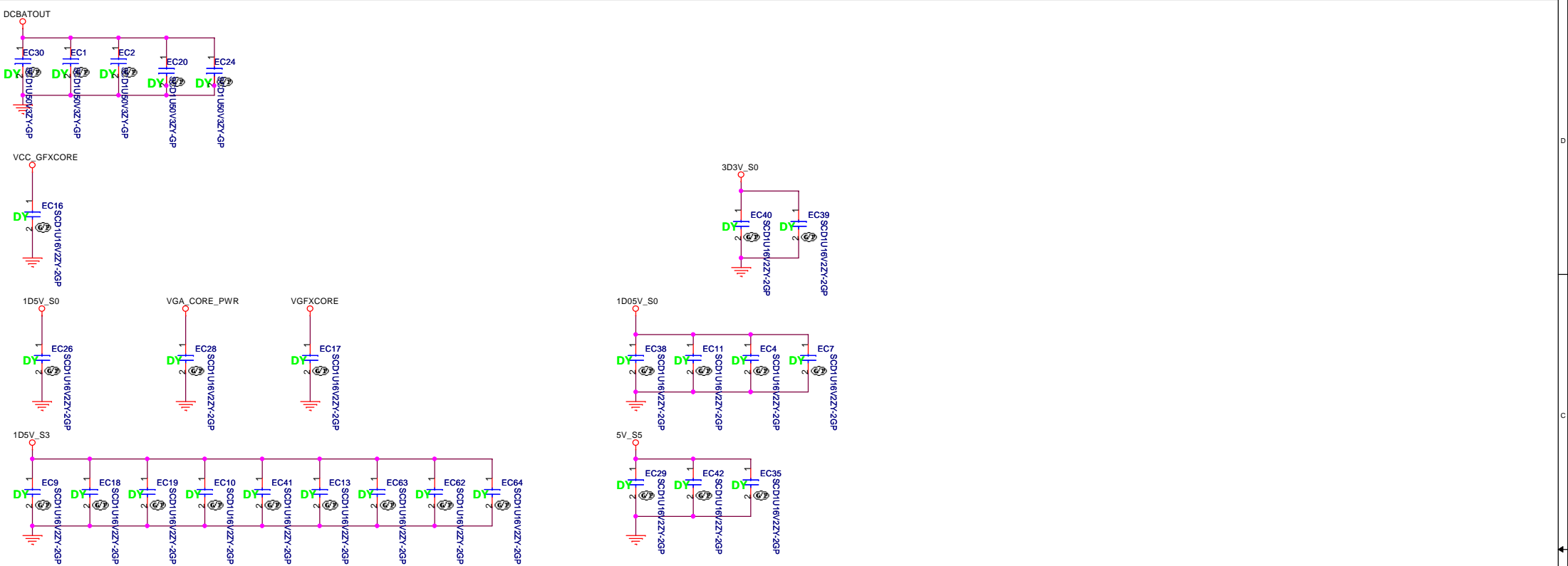


Samsung : K4W1G1646E-EC12

Hynix : H5TQ1G63BFR-12C



Wistron Corporation 21F, 88, Sec. 1, Hsien Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
File	VRAM
Size	Document Number
JM41 Discrete	
Date: Tuesday, April 07, 2009	Rev -1
Sheet 46 of 48	



DIS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **EMI/Spring/Boss**

Size: Document Number: **JM41_Discrete** Rev: -1

Date: Monday, April 06, 2009 Sheet 47 of 48

JM41/JM51 DIS Schematic EC Tracking Record
EC # / Page / Description / Part Affected

- EC SC01/11/connect NB1.A31 to GND(For power save)
- EC SC02/14/net DIS_EN pull high 10K to 3D3V_S0
- EC SC03/20/CN2.pin35 change to AGND
- EC SC04/22/R311 change to 39.2K
- EC SC05/22/U24.pin2 change to AGND
- EC SC06/26/BTB2.pin9 add stand by led control signal
- EC SC07/28/U16.pin66 add stand by led control signal
- EC SC08/28/add circuit to support green adapter
- EC SC09/28/net EJECT_BTN pull high 10K to 3D3V_S0
- EC SC10/31/add circuit to stand by led control
- EC SC11/40/change GPU power enable signal to ATI_PWR_ON#(low active)
- EC SC12/41/change U11 power plane to 1D8V_NB_S0

DIS	
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
HISTORY	
Size K2	Document Number JM41 Discrete
Date Wednesday, April 16, 2008	Rev -1
Sheet 50 of 50	