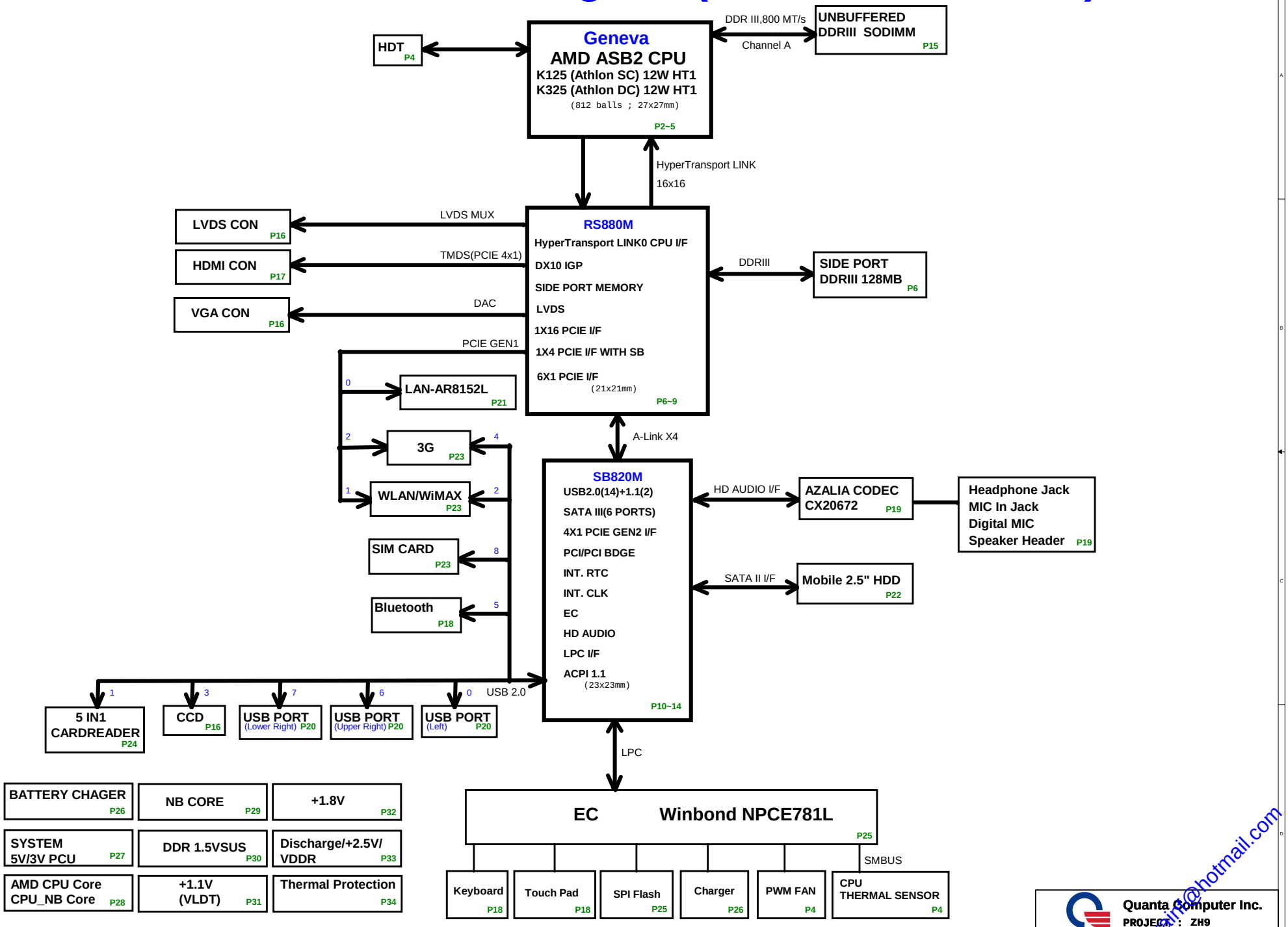
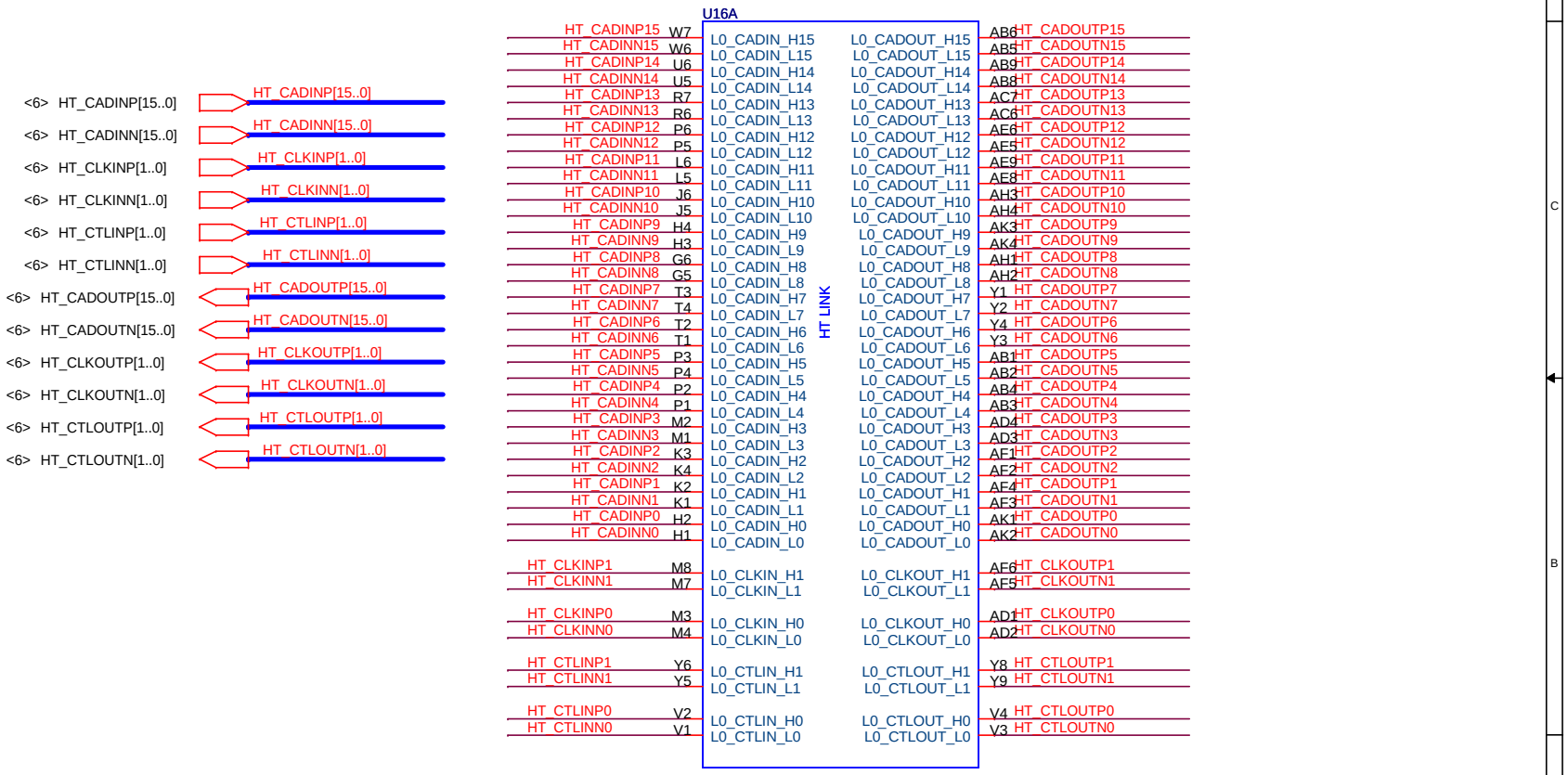
ZH9 Block Diagram (AMD Nile Platform)



Quanta Computer Inc.
PROJECT : ZH9
Size | Document Number | Rev 4A
Block Diagram
Date: Sunday, March 28, 2010 | Sheet 1 of 40

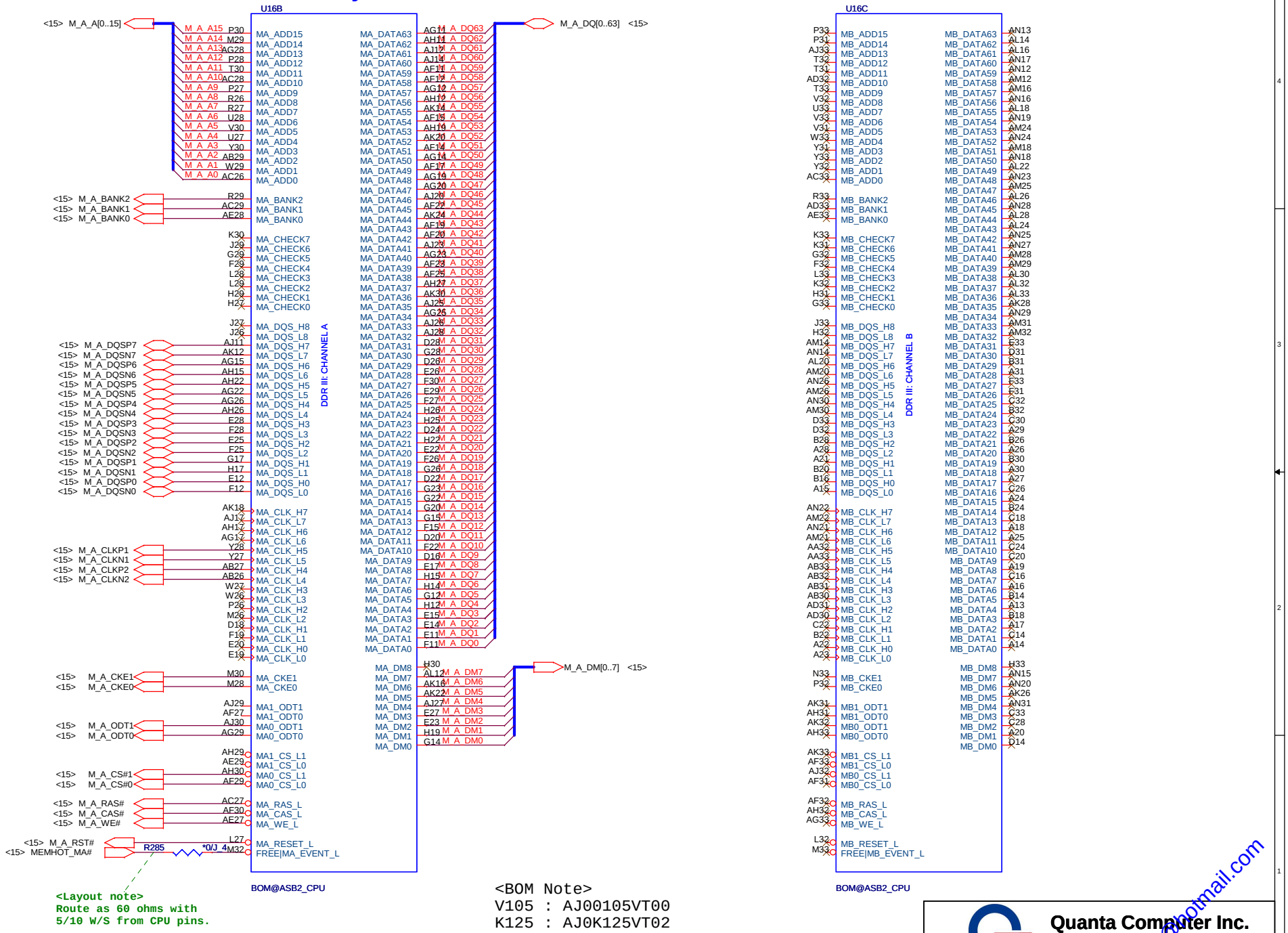


Quanta Computer Inc.

PROJECT : ZH9

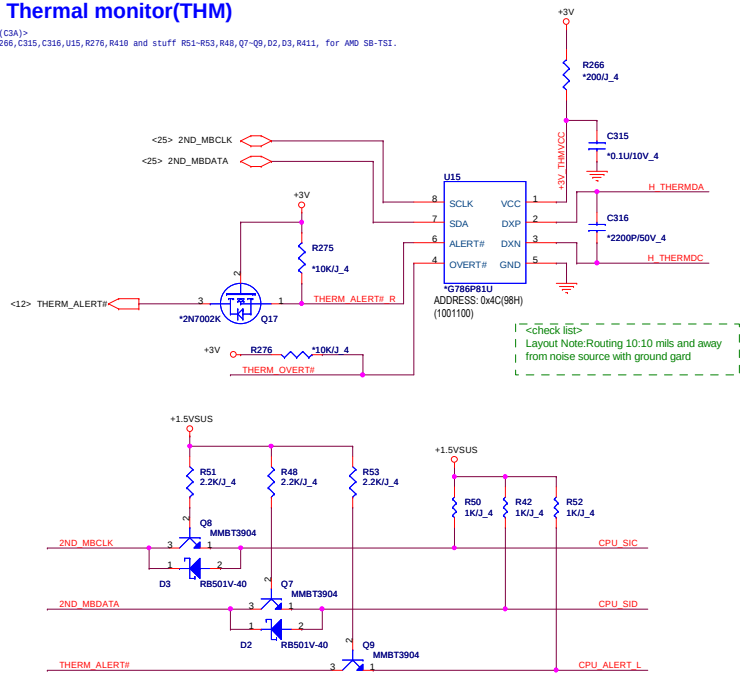
Size	Document Number	Rev
	ASB2 HT I/F 1/4	4A
Date: Sunday, March 28, 2010	Sheet 2 of 40	

Processor Memory Interface

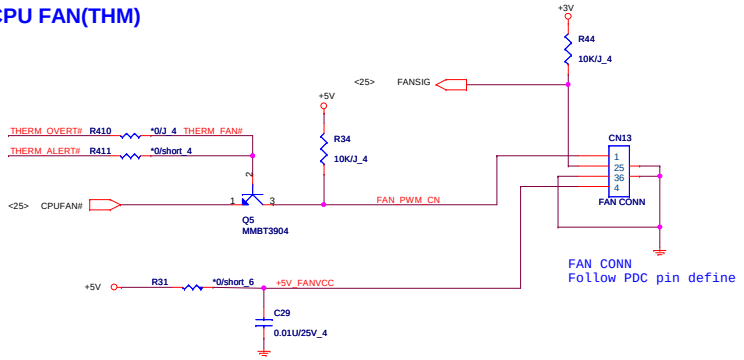


CPU Thermal monitor(THM)

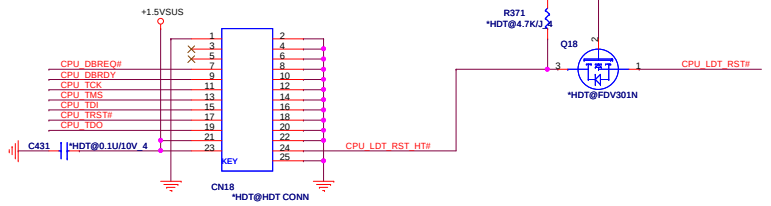
<20100303(C3A)>
Reserve R266,C315,C316,U15,R276,R410 and stuff R51~R53,R48,Q7~Q9,D2,D3,R411, for AMD SB-TSI.

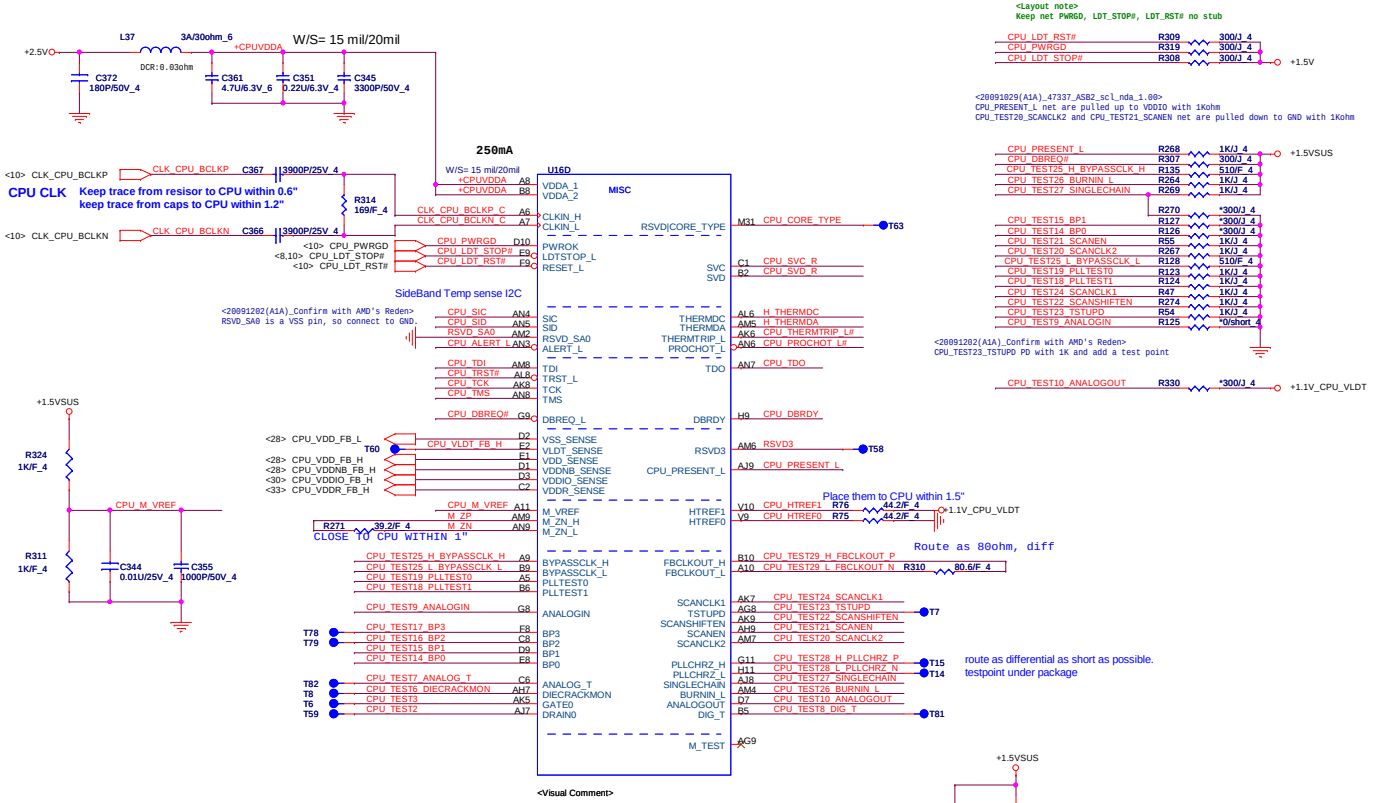


CPU FAN(THM)



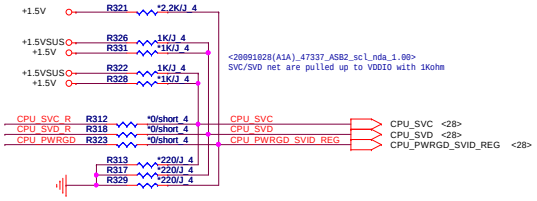
HDT Connector





Serial VID

To override VID,
Remove three 0ohms and install 220ohm of CPU_PWRGD to GND



Pre-PWROK Metal MODE / VFIX MODE(Don't Support)

SVC	SVD	Voltage Output	Voltage Output
0	0	1.1V	1.4V
0	1	1.0V	1.2V
1	0	0.9V	1.0V
1	1	0.8V	0.8V

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PROJECT : ZH9

Size	Document Number	Rev
	ASB2 CTRL & DEBUG 3/4	4A

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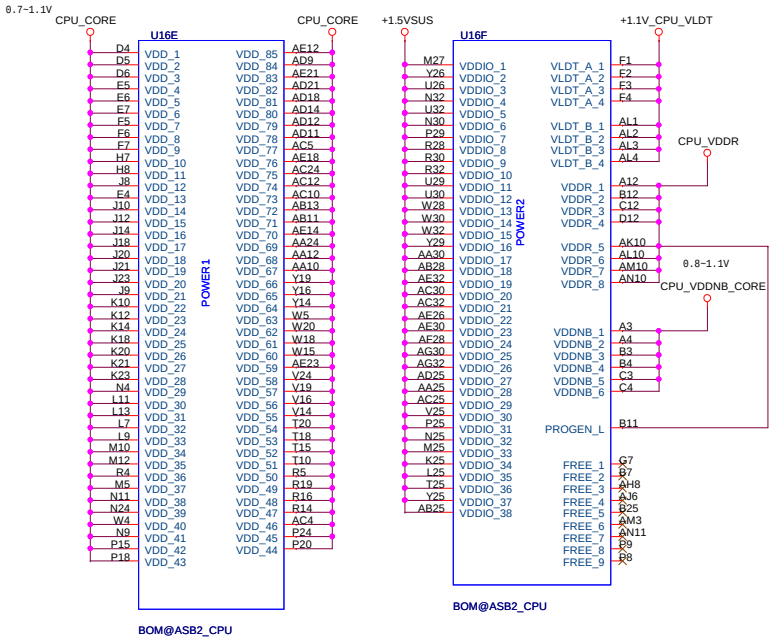
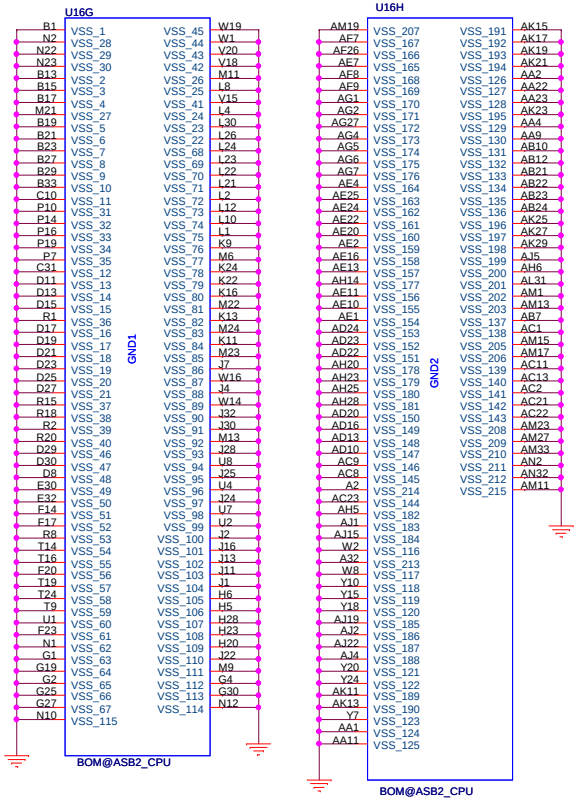
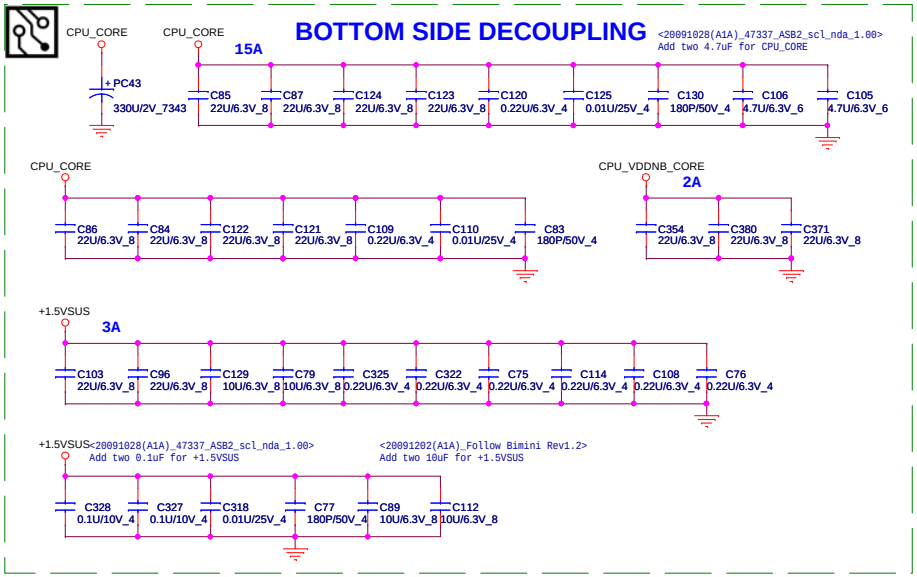
PROCESSOR POWER AND GROUND

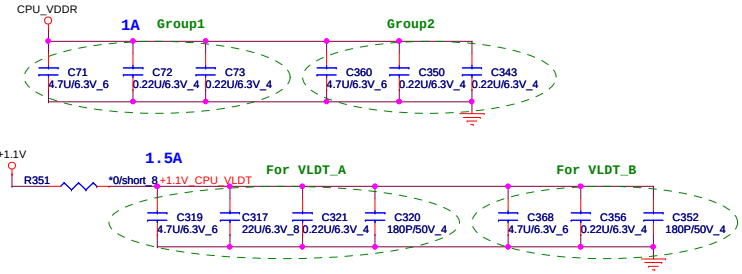




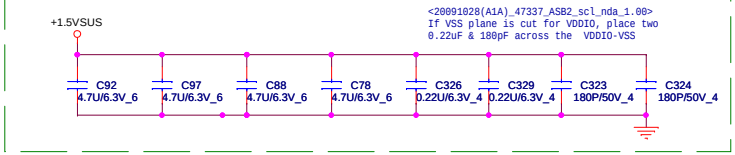
BOTTOM SIDE DECOUPLING



PLACE CLOSE TO PROCESSOR AS POSSIBLE



DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



Quanta Computer Inc.
PROJECT : ZH9

Size	Document Number	Rev
	ASB2 PWR & GND 4/4	4A
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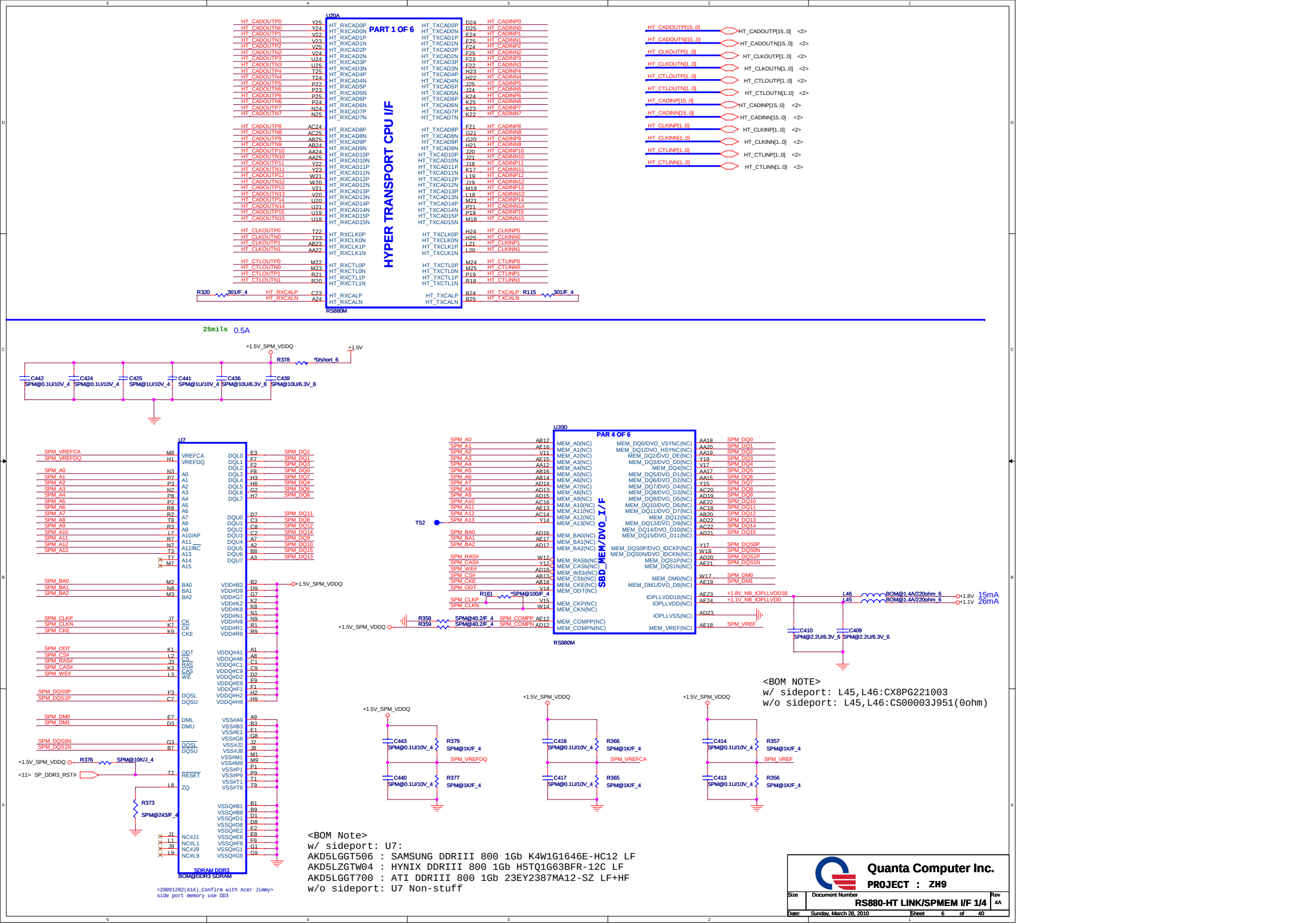

<BOM NOTE>
w/ sideport: L45,L46:CX8PG221003
w/o sideport: L45,L46:CS00003J951(0ohm)

<BOM Note>
w/ sideport: U7:
AKD5LGGT506 : SAMSUNG DDRIII 800 1Gb K4W1G1646E-HC12 LF
AKD5LZGTW04 : HYNIX DDRIII 800 1Gb H5TQ1G63BFR-12C LF
AKD5LGGT700 : ATI DDRIII 800 1Gb 23EY2387MA12-SZ LF+HF
w/o sideport: U7 Non-stuff

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PROJECT : ZH9

Size	Document Number	Rev
	RS880-HT LINK/SPMEM I/F 1/4	4A
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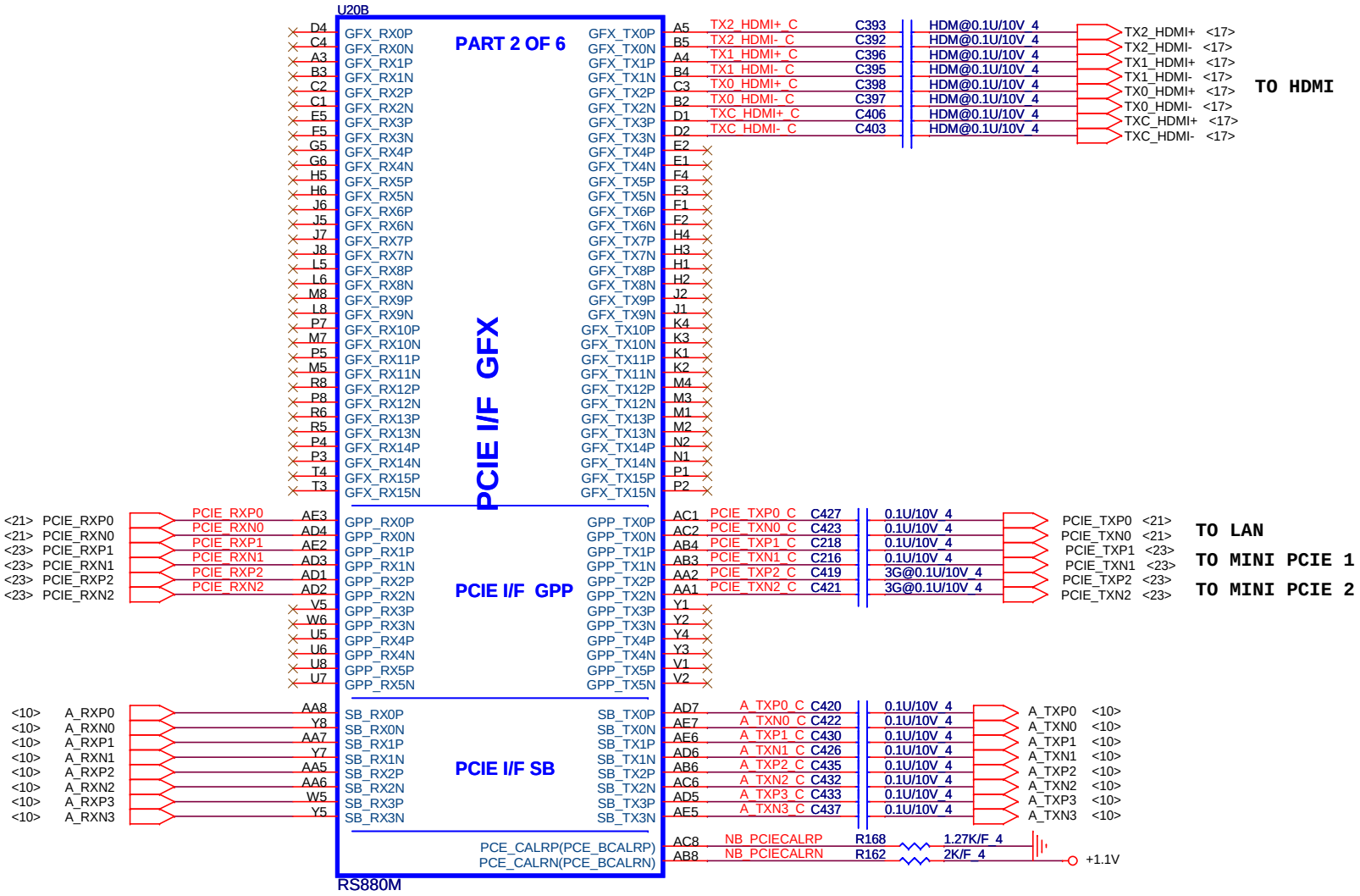

RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

Quanta Computer Inc.

PROJECT : ZH9

Size	Document Number	Rev
	RS880-PCIE I/F 2/4	4A
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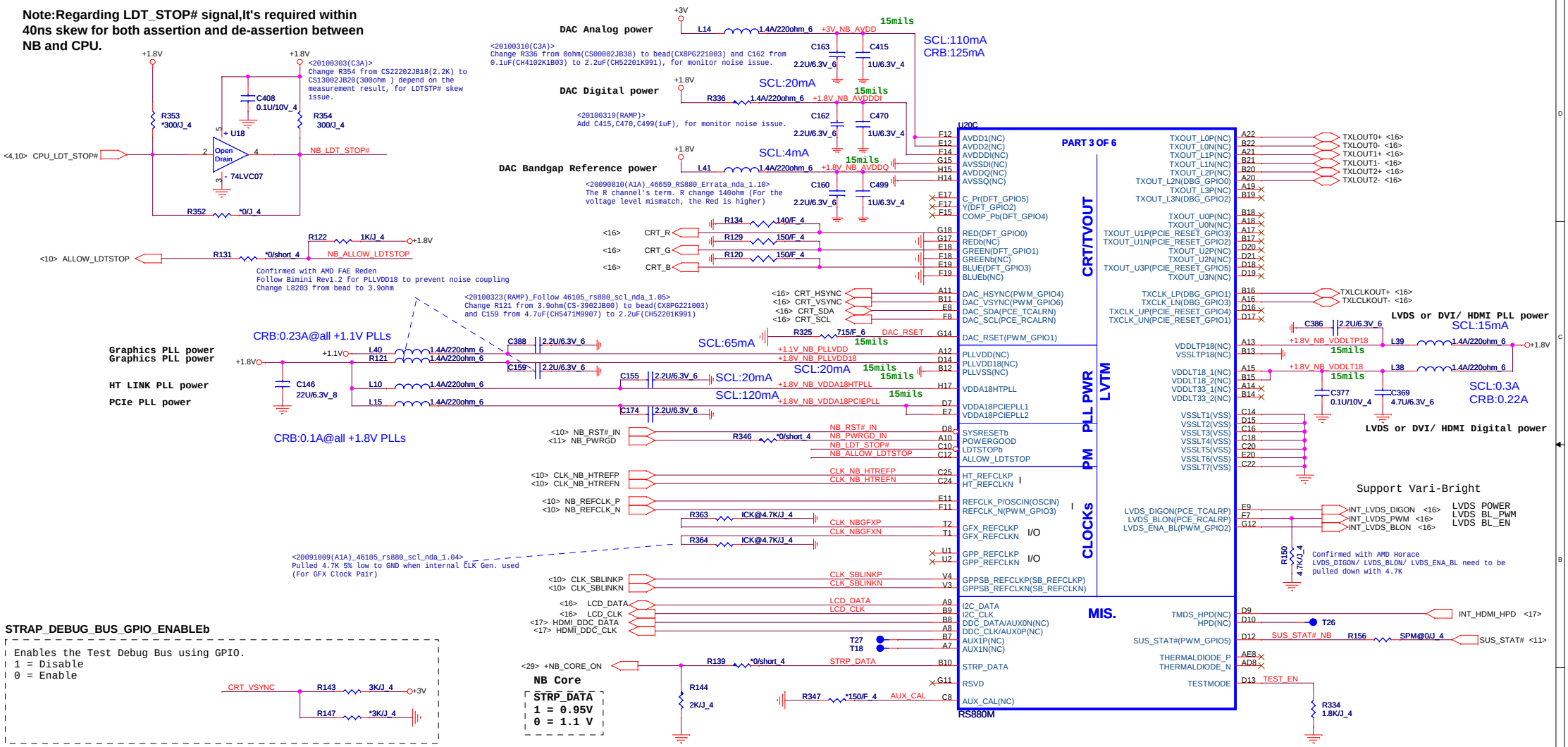
Note:Regarding LDT_STOP# signal,It's required within 40ns skew for both assertion and de-assertion between NB and CPU.



STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 = Disable
0 = Enable

RS880M: Enables Side port memory

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available

<BOM NOTE>
w/ sideport: R142 non-stuff
w/o sideport: R142 stuff

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

EEPROM not implemented

Quanta Computer Inc.
PROJECT : ZH9

Size	Document Number	Rev
	RS880-SYSTEM I/F 3/4	4A
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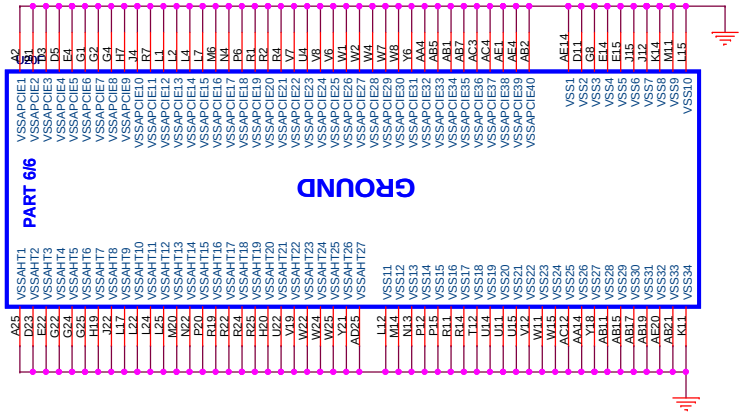
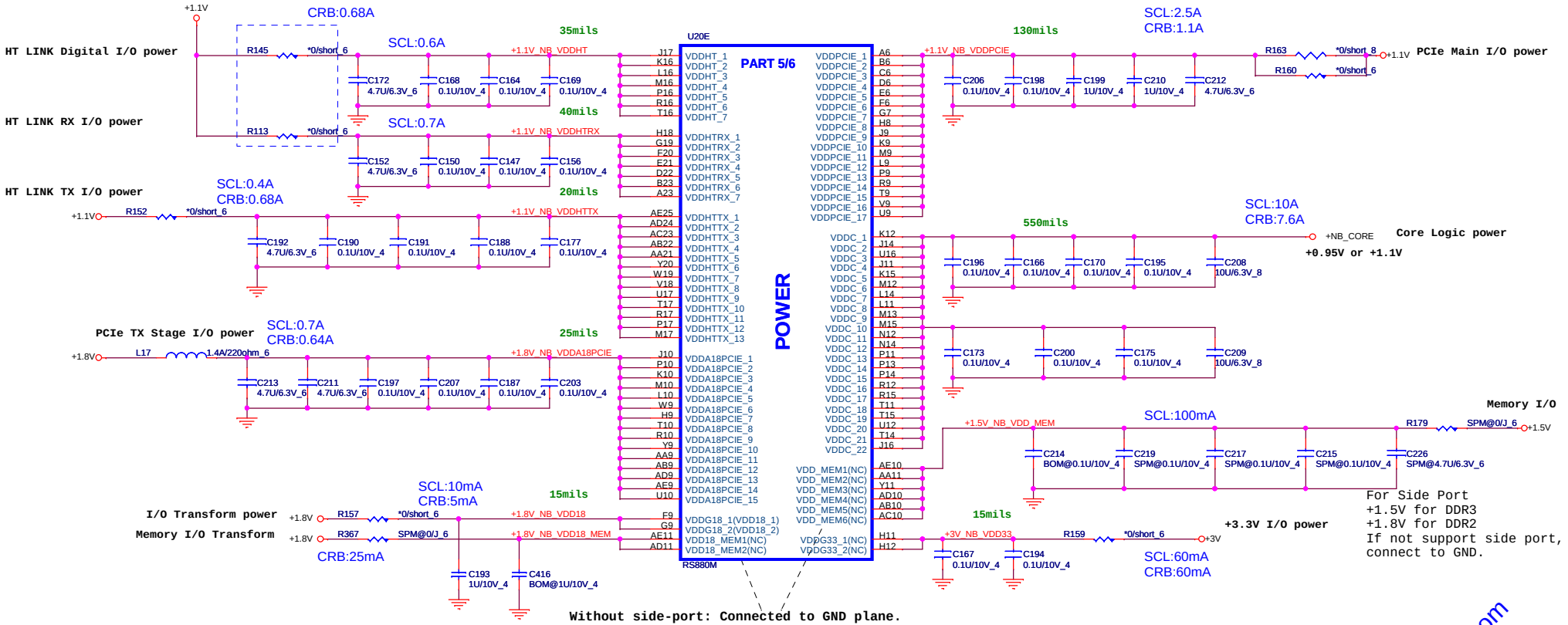


RX881/RS880 POWER DIFFERENCE TABLE

PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	IOPLLVDD	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	GND	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	GND	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	GND	+1.8V
VDD18	+1.8V	+1.8V	PLLVDD	GND	+1.1V
VDD18_MEM	GND	+1.8V	PLLVDD18	GND	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+0.95V~+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	GND	+1.8V/1.5V	VDDLTP18	GND	+1.8V
VDD33	+3.3V	+3.3V	VDDLT18	GND	+1.8V
IOPLLVDD18	+1.8V	+1.8V	VDDLT33	NC	NC



<BOM NOTE>
w/ sideport: C214:CH4102K1B03 ; C416:CH5102K9B06
w/o sideport: C214,C416:CS00002JB38(0ohm)

Quanta Computer Inc.
PROJECT : ZH9

Size	Document Number	Rev
	RS880-POWER 4/4	4A
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PCIE_RST#: Reset PCIe Slot/Device (PCIe interface from SB)
A_RST#: Reset NB, MXM, EC, PCIe Slot/Device (PCIe interface from NB)

NB
EC

<8> NB_RST#_IN — R73 *0/short_4 — C102 150P/50V_4 — A_RST# — R89 33/J_4 — A_RST#_SB_C — P1 — L1 — A_RST#_SB

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB820

<7> A_RXP0	C179	0.1U/10V_4	A_RXP0_C	AD26	A_TX0P
<7> A_RXN0	C180	0.1U/10V_4	A_RXN0_C	AD27	A_TX0N
<7> A_RXP1	C182	0.1U/10V_4	A_RXP1_C	AC28	A_TX1P
<7> A_RXN1	C181	0.1U/10V_4	A_RXN1_C	AC29	A_TX1N
<7> A_RXP2	C183	0.1U/10V_4	A_RXP2_C	AB29	A_TX2P
<7> A_RXN2	C184	0.1U/10V_4	A_RXN2_C	AB28	A_TX2N
<7> A_RXP3	C186	0.1U/10V_4	A_RXP3_C	AB26	A_TX3P
<7> A_RXN3	C185	0.1U/10V_4	A_RXN3_C	AB27	A_TX3N

<7> A_TXP0			A_TXP0	AE24	A_RX0P
<7> A_TXN0			A_TXN0	AE23	A_RX0N
<7> A_TXP1			A_TXP1	AD25	A_RX1P
<7> A_TXN1			A_TXN1	AD24	A_RX1N
<7> A_TXP2			A_TXP2	AC24	A_RX2P
<7> A_TXN2			A_TXN2	AC25	A_RX2N
<7> A_TXP3			A_TXP3	AB25	A_RX3P
<7> A_TXN3			A_TXN3	AB24	A_RX3N

+1.1V_SB_VDDAN_11_PCIE — R350 590/F_4 — R349 2K/F_4 — PCIE_CALRP_SB — AD29 — PCIE_CALRP
PCIE_CALRN_SB — AD28 — PCIE_CALRN

GPP_TX0P AA28, GPP_TX0N AA29, GPP_TX1P Y29, GPP_TX1N Y28, GPP_TX2P Y26, GPP_TX2N Y27, GPP_TX3P W28, GPP_TX3N W29
GPP_RX0P AA22, GPP_RX0N Y21, GPP_RX1P AA25, GPP_RX1N AA24, GPP_RX2P W23, GPP_RX2N V24, GPP_RX3P W24, GPP_RX3N W25

<20100325(RAMP)>
Change RP1~RP4,RP6~RP8 to shortpad.

<Layout note>
Share pad with other resisters and close to external CLK Gen.

to NB for A-LINK/PCIe REF CLK
<8> CLK_SBLINKP
<8> CLK_SBLINKN
RP7 4 3 2 1 *ICK@0/short_4P2R
CLK_SBSRCP M23
CLK_SBSRCN P23
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN

to NB Display Eng
<8> NB_REFCLK_P
<8> NB_REFCLK_N
RP2 4 3 2 1 *ICK@0/short_4P2R SB_NB_REFCLKP U29 NB_DISP_CLKP
SB_NB_REFCLKN U28 NB_DISP_CLKN
<8> CLK_NB_HTREFP
<8> CLK_NB_HTREFN
RP1 4 3 2 1 *ICK@0/short_4P2R SB_NB_HTCLKP T26 NB_HT_CLKP
SB_NB_HTCLKN T27 NB_HT_CLKN
<4> CLK_CPU_BCLKP
<4> CLK_CPU_BCLKN
RP8 4 3 2 1 *ICK@0/short_4P2R SB_CPU_CLKP V21 CPU_HT_CLKP
SB_CPU_CLKN T21 CPU_HT_CLKN
V23 SLT_GFX_CLKP
T23 SLT_GFX_CLKN

to MINI PCIE 2
<23> CLK_PCIE_MNC_P
<23> CLK_PCIE_MNC_N
RP4 4 3 2 1 *3G@ICK@0/short_4P2R SB_MNC_CLKP L29 GPP_CLK0P
SB_MNC_CLKN L28 GPP_CLK0N
N29 GPP_CLK1P
N28 GPP_CLK1N

to LAN
<21> CLK_PCIE_LANP
<21> CLK_PCIE_LANN
RP6 2 4 1 3 *ICK@0/short_4P2R SB_LAN_CLKP M29 GPP_CLK2P
SB_LAN_CLKN M28 GPP_CLK2N
T25 GPP_CLK3P
V25 GPP_CLK3N
L24 GPP_CLK4P
L23 GPP_CLK4N
P25 GPP_CLK5P
M25 GPP_CLK5N
P29 GPP_CLK6P
P28 GPP_CLK6N
N26 GPP_CLK7P
N27 GPP_CLK7N

to MINI PCIE 1
<23> CLK_PCIE_MPC_P
<23> CLK_PCIE_MPC_N
RP3 4 3 2 1 *ICK@0/short_4P2R SB_MPC_CLKP T29 GPP_CLK8P
SB_MPC_CLKN T28 GPP_CLK8N

to LAN chip 25MHz
<21> CLK_25M_LAN — R345 *ICK@22/J_4 — SB_CLK_25M_LAN — L25 — 14M_25M_48M_OSC

<20100129(B2A)>
Stuff R345. (CLK for LAN from crystal change to internal CLK.)

<20100310(C3A)>
Non-Stuff R345. (14M_25M_48M_OSC is S0 plane, doesn't support WoL.)

C411 27P/50V_4 — Y4 25MHz-SB820M — C412 27P/50V_4
25M_X1 L26 — R355 1M/J_4 — 25M_X2 L27

<20100303(C3A)>
Change C411,C412 from CH02206JB08(22pF) to CH02706JB06(27pF), for Y4.

U5A
SB800 Part 1 of 5
SB820M

PCIE_RST#
A_RST#

PCI EXPRESS INTERFACES
A_TX0P A_TX0N A_TX1P A_TX1N A_TX2P A_TX2N A_TX3P A_TX3N
A_RX0P A_RX0N A_RX1P A_RX1N A_RX2P A_RX2N A_RX3P A_RX3N
PCIE_CALRP PCIE_CALRN
GPP_TX0P GPP_TX0N GPP_TX1P GPP_TX1N GPP_TX2P GPP_TX2N GPP_TX3P GPP_TX3N
GPP_RX0P GPP_RX0N GPP_RX1P GPP_RX1N GPP_RX2P GPP_RX2N GPP_RX3P GPP_RX3N

PCI CLKS
PCICLK0 W2 — PCI_CLK0 — T64
PCICLK1/GPO36 W1 — PCI_CLK1
PCICLK2/GPO37 W3 — PCI_CLK2
PCICLK3/GPO38 W4 — PCI_CLK3
PCICLK4/14M_OSC/GPO39 Y1 — PCI_CLK4
PCI_CLK1 <14>
PCI_CLK2 <14>
PCI_CLK3 <14>
PCI_CLK4 <14>

PCIRST# V2 — PCIRST#_L — R69 33/J_4 — PCIRST# — PCIRST# <23>
C98 150P/50V_4

AD0/GPIO0 AA1 — BOARD_ID0
AD1/GPIO1 AA4 — BOARD_ID1
AD2/GPIO2 AA3 — BOARD_ID2
AD3/GPIO3 AB1 — BOARD_ID3
AD4/GPIO4 AA5 — BOARD_ID4
AD5/GPIO5 AB2
AD6/GPIO6 AB6
AD7/GPIO7 AB5
AD8/GPIO8 AA6
AD9/GPIO9 AC2
AD10/GPIO10 AC3
AD11/GPIO11 AC4
AD12/GPIO12 AC1
AD13/GPIO13 AD1
AD14/GPIO14 AD2
AD15/GPIO15 AC6
AD16/GPIO16 AE2
AD17/GPIO17 AE1
AD18/GPIO18 AF8
AD19/GPIO19 AE3
AD20/GPIO20 AF1
AD21/GPIO21 AG1
AD22/GPIO22 AF2
AD23/GPIO23 AE9 — AD23 — AD23 <14>
AD24/GPIO24 AD9 — AD24 — AD24 <14>
AD25/GPIO25 AC11 — AD25 — R300 *0/J_4 — AD25 <14>
AD26/GPIO26 AF6 — AD26 — AD26 <14>
AD27/GPIO27 AF4 — AD27 — AD27 <14>
AD28/GPIO28 AF3
AD29/GPIO29 AH2 — SB820_MEMHOT#
AD30/GPIO30 AG2
AD31/GPIO31 AH3

<BOM Note>

ID0/1/2	P/N	Model
000	AKD5LGGT506	SAM DDR3-800 1Gb K4W1G1646E-HC12
001	AKD5LZGTW04	HYN DDR3-800 1Gb H5TQ1G63BFR-12C
010	AKD5LGGT700	ATI DDR3-800 1Gb 23EY2387MA12-SZ

+3V
R78 *10K/J_4 — BOARD_ID0 — R77 SPM@10K/J_4
R296 BOM@10K/J_4 — BOARD_ID1 — R295 BOM@10K/J_4
R283 BOM@10K/J_4 — BOARD_ID2 — R284 BOM@10K/J_4
R63 *10K/J_4 — BOARD_ID3 — R64 *10K/J_4
R302 *10K/J_4 — BOARD_ID4 — R303 *10K/J_4

+3V
R95 *2.2K/J_4
R94 *2.2K/J_4
Q10 *MMBT3904
CPU_MEMHOT# <11,15>

VDDR_1.2_EN="0" is for DDRIII-1066, VDDR=0.9V
VDDR_1.2_EN="1" is for DDRIII-1333, VDDR=1.05V

PCI INTERFACE
CBE0# CBE1# CBE2# CBE3# FRAME# DEVSEL# IRDY# TRDY# PAR STOP# PERR# SERR# REQ0#
REQ1#/GPIO40
REQ2#/CLK_REQ8#/GPIO41
REQ3#/CLK_REQ5#/GPIO42 AC12 — T74
GNT0#
GNT1#/GPO44
GNT2#/GPO45
GNT3#/CLK_REQ7#/GPIO46 AB12 — T76
CLKRUN# AB11 — CLKRUN# <25>
LOCK# AD7
INTE#/GPIO32 AJ6
INTF#/GPIO33 AG6
INTG#/GPIO34 AG4
INTH#/GPIO35 AJ4
INT_CLKREQ_MPC# R293 *0/short_4 — CLKREQ_MPC# <23>

From MINI PCIE 1

LPC
LPCCLK0 H24 — LPC_CLK0 — R342 22/J_4 — LPC_CLK0 <14>
LPCCLK1 H25 — LPC_CLK1 — R141 22/J_4 — LPC_CLK1 <14>
LCLK_EC <25>
LCLK_DEBUG <23>
LAD0 J27 — LAD0 — LAD0 <23,25>
LAD1 J26 — LAD1 — LAD1 <23,25>
LAD2 H29 — LAD2 — LAD2 <23,25>
LAD3 H28 — LAD3 — LAD3 <23,25>
LFRAME# G28 — LFRAME# — LFRAME# <23,25>
LDRQ0# J25 — LDRQ0# SB — T85
LDRQ1#/CLK_REQ6#/GPIO49 AA18 — LDRQ1# SB — T83
SERIRQ AB19 — SERIRQ <25>

CPU
ALLOW_LDTSTP/DMA_ACTIVE# G21 — ALLOW_LDTSTOP — ALLOW_LDTSTOP <8>
PROCHOT# H21 — CPU_PROCHOT# — CPU_PROCHOT# <4>
K19 — CPU_PWRGD — CPU_PWRGD <4>
LDT_STP# G22 — CPU_LDT_STOP# — CPU_LDT_STOP# <4,8>
LDT_RST# J24 — CPU_LDT_RST# — CPU_LDT_RST# <4>

RTC
32K_X1 C1 — RTC_X1
32K_X2 C2 — RTC_X2
RTCCLK D2 — RTC_CLK — RTC_CLK <25>
INTRUDER_ALERT# B2 — INTRUDER_ALERT# — T62
VCCRTC_SB B1 — R93 510/J_4 — VCCRTC
INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).
VDDBT_RTC_G
20MIL — C115 *0.1U/10V_4 — C116 1U/10V_4

CLOCK GENERATOR
14M_25M_48M_OSC

IC CTRL(605P)SB820M 218-0697014(FCBGA)
P/N : AJ069700T01

For AMD RST
+3V_S5
C80 0.1u/10V_4
<21,23,24> PLTRST# — R56 33/J_4 — A_RST#_AND
MINI-PCIE
LAN chip
Card reader
C81 10p/50V_4
U4 TC7SH08FU
A_RST#_SB — A_RST#_SB <25>
SB_GPIO_PCIE_RST# <11>
R59 *0/J_4

For VDDR
<20100119(B2A)_Bimini Rev1.4>
Non-stuff U21,C429,C428,R372,R300 (Nile doesn't support +1.05V for DDR3-1333)
The Nile VDDR should be 0.9V all the time. The 1.05V is only for DDR3_1333 which is not supported on Nile.
MEM_1V5 is for gating the glitch on VDDR_1.2_EN
+3V
C429 *0.1U/10V_4
<12> MEM_1V5 — VDDR_1.2_EN — U21 *TC7SH08FU
R372 *33/J_4 — VDDR_OPT <33>
C428 *150P/50V_4
R368 *0/J_4
VDDR_1.2_EN:
1 : VDDR =1.05V
0: VDDR = 0.90V (Default)

RTC(RTC)
VCCRTC
+3VPCU
D19 CH500H-40
D20 CH500H-40
VCCRTC_4
G1 *SHORT_PAD
R97 *0/short_4
R202 1K/J_4
20MIL
20MIL
VCCRTC_3 — Q12 MMBT3904 — VCCRTC_2 — R213 8.06K/F_4 — VCCRTC_1 — R219 8.06K/F_4
R = (5V - 0.2V-2V)/0.2mA = 14k
R220 68.1K/F_4
R221 150K/F_4
+5VPCU
BT1 RTC BATT
<20100303(C3A)>
Delete CN5 and Add BT1, for Battery SMT type.
<20100310(C3A)>
Swap BT1's pin, for pin define error

<BOM Note>
RTC BATTERY
AHL03001033 : JHT (18mAh)
AHL03001032 : MAT (17mAh)
AHL03001035 : FDK (15mAh)

RTC_X1
Y2
RTC_X2
32.768KHZ
20M/J_6 R72
C111 18P/50V_4
C93 18P/50V_4
<20100303(C3A)>
Change C93,C111 from CH02206JB08(22pF) to CH01806JB07(18pF), for Y2.

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NC only ,Can't be install

+3V_S5
R100 *2.2K/J_4 SB_TEST0
R98 *2.2K/J_4 SB_TEST1
R280 *2.2K/J_4 SB_TEST2

SCL0/SDATA0 is +3.3V_S0 domain
To Clock gen/DDR/WLAN
+3V
R338 2.2K/J_4 SB_SCLK0
R335 2.2K/J_4 SB_SDATA0

SMBUS1~3 is +3.3V_S5 domain
If SMBUS and GPIO not implemented
10K PU to +3V_S5 or 10K PD
R279 10K/J_4 SB_SCLK1
R92 10K/J_4 SB_SDATA1
R133 10K/J_4 SB_SCLK2
R337 10K/J_4 SB_SDATA2
R136 10K/J_4 SB_SCLK3
R148 10K/J_4 SB_SDATA3

+1.8V
R340 300/J_4 NB_PWRGD

<20100129(B2A)>
Stuff R110. (CLK for Cardreader from crystal change to internal CLK.)

U5D
SB800
Part 4 of 5
SB820M

<10,15> CPU_MEMHOT# R91 *0/J_4
T9
<25> SUSB#
<25> SUSC#
<25> DNBSWON#
<25> ECPWROK
<8> SUS_STAT#
R294 *0/short_4 SB_PWRGD
SUS_STAT#
SB_TEST0
SB_TEST1
SB_TEST2
<25> GA20
<25> KBRST#
<25> EC_SMI#
<25> EC_SCI#
T13 SYS_RST#
<21,23> PCIE_WAKE#
<4> CPU_THERMTRIP#
<8> NB_PWRGD
CPU_THERMTRIP#
NB_PWRGD
<25> EC_RSMRST#
RSMRST#

PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS
USB 1.1 USB MISC

USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N

A10 SB_CLK_48M_CR R110 ICK@22/J_4 CLK_48M_CR <24> to CARD READER 48MHz
G19 USB_RCOMP_SB R332 11.8K/F_6
J10 USB_FSD13P T75
H11 USB_FSD13N T77
H9 USB_FDS12P T72
J8 USB_FSD12N T71

OHCI (dev-20, fun-5)

Controller Ports mapping
OHCI0 (dev-18, fun-0) Port 0 - 4
EHCI (dev-18, fun-2) Port 0 - 4
OHCI0 (dev-19, fun-0) Port 5 - 9
EHCI (dev-19, fun-2) Port 5 - 9
OHCI0 (dev-22, fun-0) Port 10 - 14
EHCI (dev-22, fun-2) Port 10 - 14

USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N

USB+_SIM <23> MM-SIM
USB-_SIM <23>
USBP7+ <20> CONN (Lower Right)
USBP7- <20>
USBP6+ <20> CONN (Upper Right)
USBP6- <20>
USBP5+ <18> BT
USBP5- <18>
USBP4+ <23> MNC
USBP4- <23>
USBP3+ <16> CCD
USBP3- <16>
USBP2+ <23> MPC
USBP2- <23>
USBP1+ <24> Card reader
USBP1- <24>
USBP0+ <20> CONN (Left)
USBP0- <20>

USB 2.0

From MINI PCIE 2
<10> SB_GPIO_PCIE_RST# SB_GPIO_PCIE_RST#
<23> CLKREQ_MNC# R341 *0/short_4 INT_CLKREQ_MNC#
<19> SB_BEEP
<15,23> SB_SCLK0 SB_SCLK0
<15,23> SB_SDATA0 SB_SDATA0
SB_SCLK1
SB_SDATA1
From LAN
<21> CLKREQ_LAN# R333 *0/short_4 INT_CLKREQ_LAN#
T10 LLB#
T19 SHUTDOWN#
<6> SP_DDR3_RST# R281 SPM@0/J_4

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN

GPIO

<20091202(A1A)_Confirm with AMD's Horace>
IDLEEXIT#(Multi function of Pin AA20) is used for server CPU.

<20> USBOC#R R277 *0/J_4 USBOC#67
<20> USBOC#L R278 *0/J_4 USBOC#0
T73 SB_JTAG_TDO
T69 SB_JTAG_TCK
T68 SB_JTAG_TDI
T70 SB_JTAG_RST#

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#

USB OC

HD audio interface is +3V_S5 voltage

<14> ACZ_SDOUT
ACZ_BCLK
ACZ_SDOUT
ACZ_SDIN0
ACZ_SYNC
ACZ_RST#

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#

HD AUDIO

SCL2/GPIO193 D25 SB_SCLK2
SDA2/GPIO194 F23 SB_SDATA2
SCL3_LV/GPIO195 B26 SB_SCLK3
SDA3_LV/GPIO196 E26 SB_SDATA3
EC_PWM0/EC_TIMER0/GPIO197 F25
EC_PWM1/EC_TIMER1/GPIO198 E22
EC_PWM2/EC_TIMER2/GPIO199 F22 EC_PWM2 <14>
EC_PWM3/EC_TIMER3/GPIO200 E21 EC_PWM3 <14>

KSI_0/GPIO201 G24
KSI_1/GPIO202 G25
KSI_2/GPIO203 E28
KSI_3/GPIO204 E29
KSI_4/GPIO205 D29
KSI_5/GPIO206 D28
KSI_6/GPIO207 C29
KSI_7/GPIO208 C28
KSO_0/GPIO209 B28
KSO_1/GPIO210 A27
KSO_2/GPIO211 B27
KSO_3/GPIO212 D26
KSO_4/GPIO213 A26
KSO_5/GPIO214 C26
KSO_6/GPIO215 A24
KSO_7/GPIO216 B25
KSO_8/GPIO217 A25
KSO_9/GPIO218 D24
KSO_10/GPIO219 B24
KSO_11/GPIO220 C24
KSO_12/GPIO221 B23
KSO_13/GPIO222 A23
KSO_14/GPIO223 D22
KSO_15/GPIO224 C22
KSO_16/GPIO225 A22
KSO_17/GPIO226 B22

EMBEDDED CTRL

+3V_S5
R70 10K/J_4
R84 10K/J_4
R286 10K/J_4
R83 10K/J_4
R282 10K/J_4

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR

GBE LAN

T17 PS2_DAT/SDA4/GPIO187
T22 PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

EMBEDDED CTRL

To Azalia

ACZ_SDOUT R85 33/J_4 C99 *10P/50V_4 ACZ_SDOUT_AUDIO <19>
ACZ_SYNC R86 33/J_4 C100 *10P/50V_4 ACZ_SYNC_AUDIO <19>
<20091030(A1A)_EMI's Suggest>
Add one 10pF to GND for BITCLK
ACZ_BCLK R87 33/J_4 C101 *10P/50V_4 ACZ_BITCLK_AUDIO <19>
R88 *10K/J_4
ACZ_RST# R71 33/J_4 ACZ_RST#_AUDIO <19>
ACZ_SDIN0 R90 *10K/J_4 ACZ_SDIN0 <19>

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SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO SB820

SATA HDD

<22> SATA_TXP0
<22> SATA_TXN0
C141 0.01U/25V_4 SATA_TXP0_C
C142 0.01U/16V_4 SATA_TXN0_C
<22> SATA_RXN0
<22> SATA_RXP0
C140 0.01U/25V_4 SATA_RXN0_C
C137 0.01U/25V_4 SATA_RXP0_C

U5B

SB800
Part 2 of 5

SERIAL ATA

AH9 SATA_TX0P
AJ9 SATA_TX0N
AJ8 SATA_RX0N
AH8 SATA_RX0P
AH10 SATA_TX1P
AJ10 SATA_TX1N
AG10 SATA_RX1N
AE10 SATA_RX1P
AG12 SATA_TX2P
AF12 SATA_TX2N
AJ12 SATA_RX2N
AH12 SATA_RX2P
AH14 SATA_TX3P
AJ14 SATA_TX3N
AG14 SATA_RX3N
AF14 SATA_RX3P
AG17 SATA_TX4P
AF17 SATA_TX4N
AJ17 SATA_RX4N
AH17 SATA_RX4P
AJ18 SATA_TX5P
AH18 SATA_TX5N
AH19 SATA_RX5N
AJ19 SATA_RX5P

PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

+1.1V_SB_VDDAN_11_SATA
R316 1K/F_4 SATA_CALRP
R315 931/F_4 SATA_CALRN
AB14 SATA_CALRP
AA14 SATA_CALRN

To meet SB800 SCL1.02:
DNI SATA XTAL circuit's parts

<22> SATALED#
+3V R304 10K/J_4
AD11 SATA_ACT#/GPIO67

C151 *22P/50V_4 SATA_X1
Y3 *25MHz-SATA
R114 *1M/J_4
C145 *22P/50V_4 SATA_X2
AD16 SATA_X1
AC16 SATA_X2

T67 J5 SPI_DI/GPIO164
T12 E2 SPI_DO/GPIO163
T11 K4 SPI_CLK/GPIO162
T65 K9 SPI_CS1#/GPIO165
T66 G2 ROM_RST#/GPIO161

SPI ROM

SB820M

The flash controller function is NOT
supported by the SB820M.

FLASH

FC_CLK AH28 T45
FC_FBCLKOUT AG28 T31
FC_FBCLKIN AF26 T39
FC_OE#/GPIOD145 AF28 T38
FC_AVD#/GPIOD146 AG29 T37
FC_WE#/GPIOD148 AG26 T36
FC_CE1#/GPIOD149 AF27 T43
FC_CE2#/GPIOD150 AE29 T44
FC_INT1/GPIOD144 AF29 T32
FC_INT2/GPIOD147 AH27 T33
FC_ADQ0/GPIOD128 AJ27 T42
FC_ADQ1/GPIOD129 AJ26 T30
FC_ADQ2/GPIOD130 AH25 T29
FC_ADQ3/GPIOD131 AH24 T28
FC_ADQ4/GPIOD132 AG23 T23
FC_ADQ5/GPIOD133 AH23 T24
FC_ADQ6/GPIOD134 AJ22 T21
FC_ADQ7/GPIOD135 AG21 T16
FC_ADQ8/GPIOD136 AF21 T80
FC_ADQ9/GPIOD137 AH22 T20
FC_ADQ10/GPIOD138 AJ23 T25
FC_ADQ11/GPIOD139 AF23 T84
FC_ADQ12/GPIOD140 AJ24 T34
FC_ADQ13/GPIOD141 AJ25 T35
FC_ADQ14/GPIOD142 AG25 T40
FC_ADQ15/GPIOD143 AH26 T41

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

+3V
R106 10K/J_4
R105 10K/J_4
Q11 MMBT3904
SB_PROCHOT# <4>

HW MONITOR

FANOUT0/GPIO52 W5
FANOUT1/GPIO53 W6
FANOUT2/GPIO54 Y9 SB_PROCHOT#_C
FANIN0/GPIO56 W7
FANIN1/GPIO57 V9
FANIN2/GPIO58 W8
TEMPIN0/GPIO171 B6 TEMPIN0 R109 10K/J_4
TEMPIN1/GPIO172 A6 TEMPIN1 R108 10K/J_4
TEMPIN2/GPIO173 A5 TEMPIN2 R103 10K/J_4
TEMPIN3/TALERT#/GPIO174 B5
TEMP_COMM C7 TEMP_COMM
R107 10K/J_4 +3V_S5
THERM_ALERT# <4>

<20100119(B2A)_Bimini Rev1.4>
Non-stuff R408 ; stuff R409
(Nile doesn't support VDDR = +1.05V for DDR3-1333)

VIN0/GPIO175 A3 VIN0 R290 10K/J_4
VIN1/GPIO176 B4 VIN1 R289 10K/J_4
VIN2/GPIO177 A4 VIN2 R288 10K/J_4
VIN3/GPIO178 C5 VIN3 R102 10K/J_4
VIN4/GPIO179 A7 VIN4 R409 10K/J_4
VIN5/GPIO180 B7 VIN5 R298 10K/J_4
VIN6/GBE_STAT3/GPIO181 B8 VIN6 R301 10K/J_4
VIN7/GBE_LED3/GPIO182 A8 VIN7 R297 10K/J_4
VIN4 R408 *0/J_4 MEM_1V5 <10>

NC1 G27
NC2 Y2

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PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

3.3V I/O power

131mA

Not used: Connected to GND through a 0Ω.

1.8V GPIOD I/O Power

A-Link Express III/PCIe PLL power

43mA 15mils

A-Link Express III/PCIe analog power

600mA 100mils

Check

SATA PHY PLL power

93mA 15mils

SATA PHY analog / I/O Power

567mA 50mils

USB PHY analog / I/O Power

658mA 50mils

Support S3 wake up

USB PHY DLL analog power

xx mA 20mils

Support S3 wake up

SB820M

Core logic power

100mils 510mA

Check

xx mA

System Clock Gen analog/output power

<45484_sb800_dg_nda_1.02>
Not use interal CLK Gen: Connected to +1.1V directly.

Not support GBE: Connected to GND.

20mils 32mA

S5 I/O Power

15mils 113mA

S5 Core logic standby power

20mils xx mA HD Audio I/O Power

15mils 197mA

USB PHY core power

15mils 47mA System CLK Gen PLLs analog power

15mils 62mA System CLK Gen PLLs analog power

17mA USB PHY PLL analog power

5mA Hardware monitor analog / I/O power

25-MHz XTAL I/O Power

WoL--> +3.3V_S5 rail
Non-WoL--> +3.3V_S0 rail

15mils xx mA

Part 5 of 5

SB820M

WoL--> +1.1V_S5 rail
Non-WoL--> +1.1V_S0 rail

Support S3 wake up

<20100310(C3A)_Follow CRB>
Connect +3VSUS_SB_VDDPL_33_USB_S to
+3VSUS directly.

Support S3 wake up

As GPIOs: Stuff 0.1uF

nexaxin@hotmail.com

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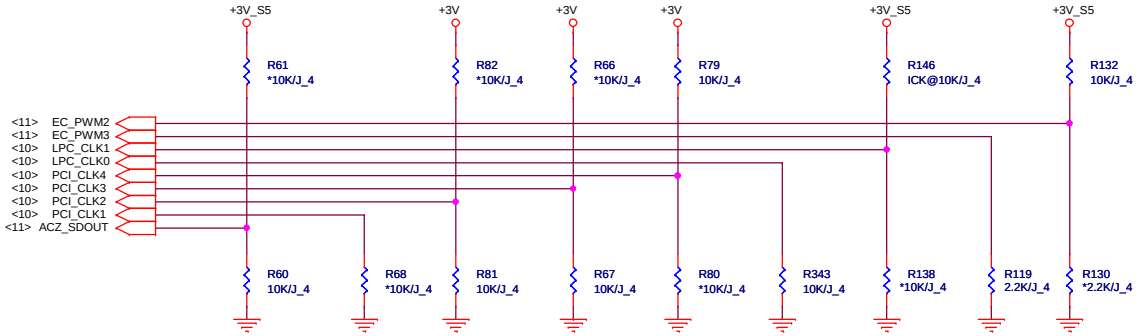
STANDARD STRAPS

<20091202(A1A)_Confirm with AMD's Horace>
PCI_CLK4 PU with 10K for both internal and external CLK Gen.



	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM3 EC_PWM2
PULL HIGH	LOW POWER MODE	PCIe Gen II	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLK MODE ICK@DEFAULT	EC ENABLED	CLKGEN ENABLED ICK@DEFAULT	H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	PCIe Gen I	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	FUSION CLK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED ECK@DEFAULT	L, H=LPC ROM DEFAULT L, L=Reserved

This is required as the low power mode is not supported on the SB8xx.

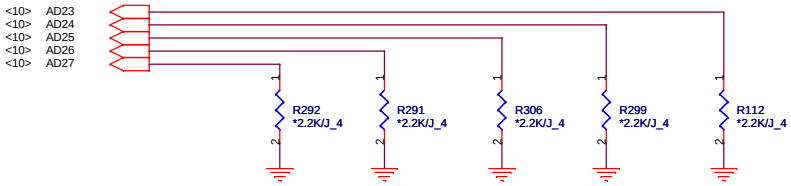
Not Applicable to SB820M--Leave provision for PD.

PCICLK4:
CPU/NB HT Clock Selection
This strap is not used if the strap CLKGEN is configured for external clock generator mode.

internal have pull Hi 10K

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

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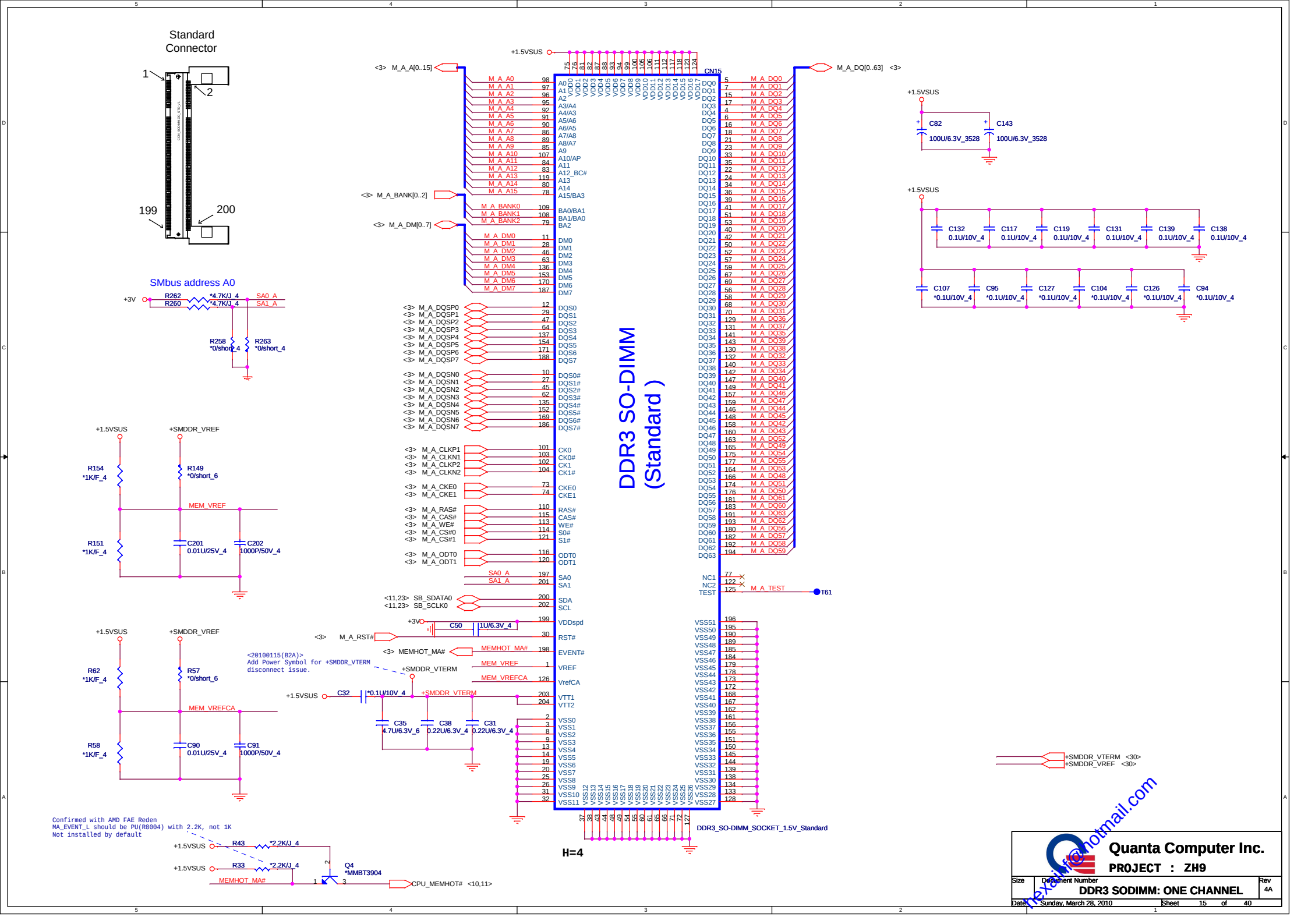
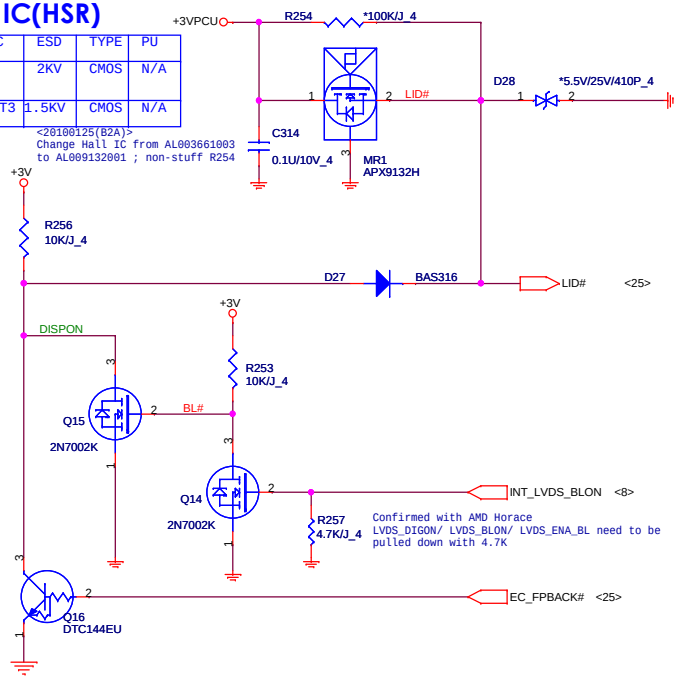
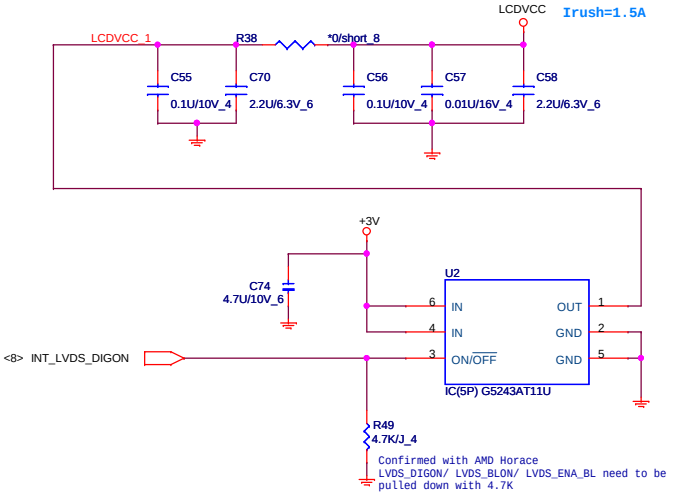

Standard Connector
1
2
199
200
SMbus address A0
+3V
R262 *4.7K/J_4
R260 *4.7K/J_4
SA0_A
SA1_A
R258 *0/short_4
R263 *0/short_4
+1.5VSUS
+SMDDR_VREF
R154 *1K/F_4
R149 *0/short_6
MEM_VREF
R151 *1K/F_4
C201 0.01U/25V_4
C202 1000P/50V_4
R62 *1K/F_4
R57 *0/short_6
MEM_VREFCA
R58 *1K/F_4
C90 0.01U/25V_4
C91 1000P/50V_4
<20100115(B2A)>
Add Power Symbol for +SMDDR_VTERM
disconnect issue.
+SMDDR_VTERM
C32 *0.1U/10V_4
C35 4.7U/6.3V_6
C38 0.22U/6.3V_4
C31 0.22U/6.3V_4
Confirmed with AMD FAE Reden
MA_EVENT_L should be PU(R8004) with 2.2K, not 1K
Not installed by default
R43 *2.2K/J_4
R33 *2.2K/J_4
Q4 *MMBT3904
MEMHOT_MA#
CPU_MEMHOT# <10,11>
<3> M_A_A[0..15]
<3> M_A_BANK[0..2]
<3> M_A_DM[0..7]
<3> M_A_DQSP0
<3> M_A_DQSP1
<3> M_A_DQSP2
<3> M_A_DQSP3
<3> M_A_DQSP4
<3> M_A_DQSP5
<3> M_A_DQSP6
<3> M_A_DQSP7
<3> M_A_DQSN0
<3> M_A_DQSN1
<3> M_A_DQSN2
<3> M_A_DQSN3
<3> M_A_DQSN4
<3> M_A_DQSN5
<3> M_A_DQSN6
<3> M_A_DQSN7
<3> M_A_CLKP1
<3> M_A_CLKN1
<3> M_A_CLKP2
<3> M_A_CLKN2
<3> M_A_CKE0
<3> M_A_CKE1
<3> M_A_RAS#
<3> M_A_CAS#
<3> M_A_WE#
<3> M_A_CS#0
<3> M_A_CS#1
<3> M_A_ODT0
<3> M_A_ODT1
<11,23> SB_SDATA0
<11,23> SB_SCLK0
+3V
C50 1U/6.3V_4
<3> M_A_RST#
<3> MEMHOT_MA#
DDR3 SO-DIMM (Standard)
CN15
M_A_DQ[0..63] <3>
NC1
NC2
TEST
M_A_TEST
T61
DDR3_SO-DIMM_SOCKET_1.5V_Standard
H=4
C82 100U/6.3V_3528
C143 100U/6.3V_3528
C132 0.1U/10V_4
C117 0.1U/10V_4
C119 0.1U/10V_4
C131 0.1U/10V_4
C139 0.1U/10V_4
C138 0.1U/10V_4
C107 *0.1U/10V_4
C95 *0.1U/10V_4
C127 *0.1U/10V_4
C104 *0.1U/10V_4
C126 *0.1U/10V_4
C94 *0.1U/10V_4
+SMDDR_VTERM <30>
+SMDDR_VREF <30>
Quanta Computer Inc.
PROJECT : ZH9
Size
Document Number
DDR3 SODIMM: ONE CHANNEL
Rev 4A
Date: Sunday, March 28, 2010
Sheet 15 of 40
nexus.fi@hotmail.com

HALL IC(HSR)

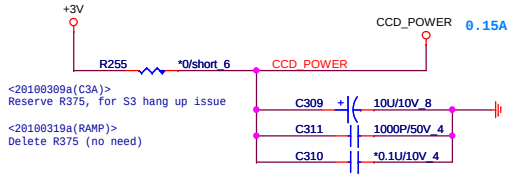
Hall IC	ESD	TYPE	PU
APX9132H AI-TRG	2KV	CMOS	N/A
EM-6781-T3	1.5KV	CMOS	N/A



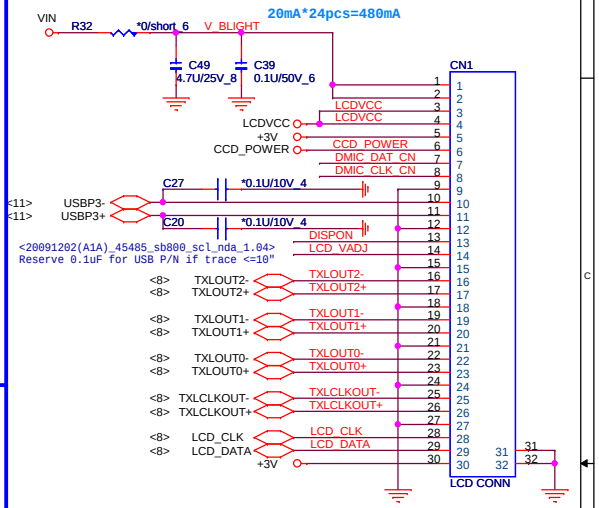
LCD POWER SWITCH(LDS)



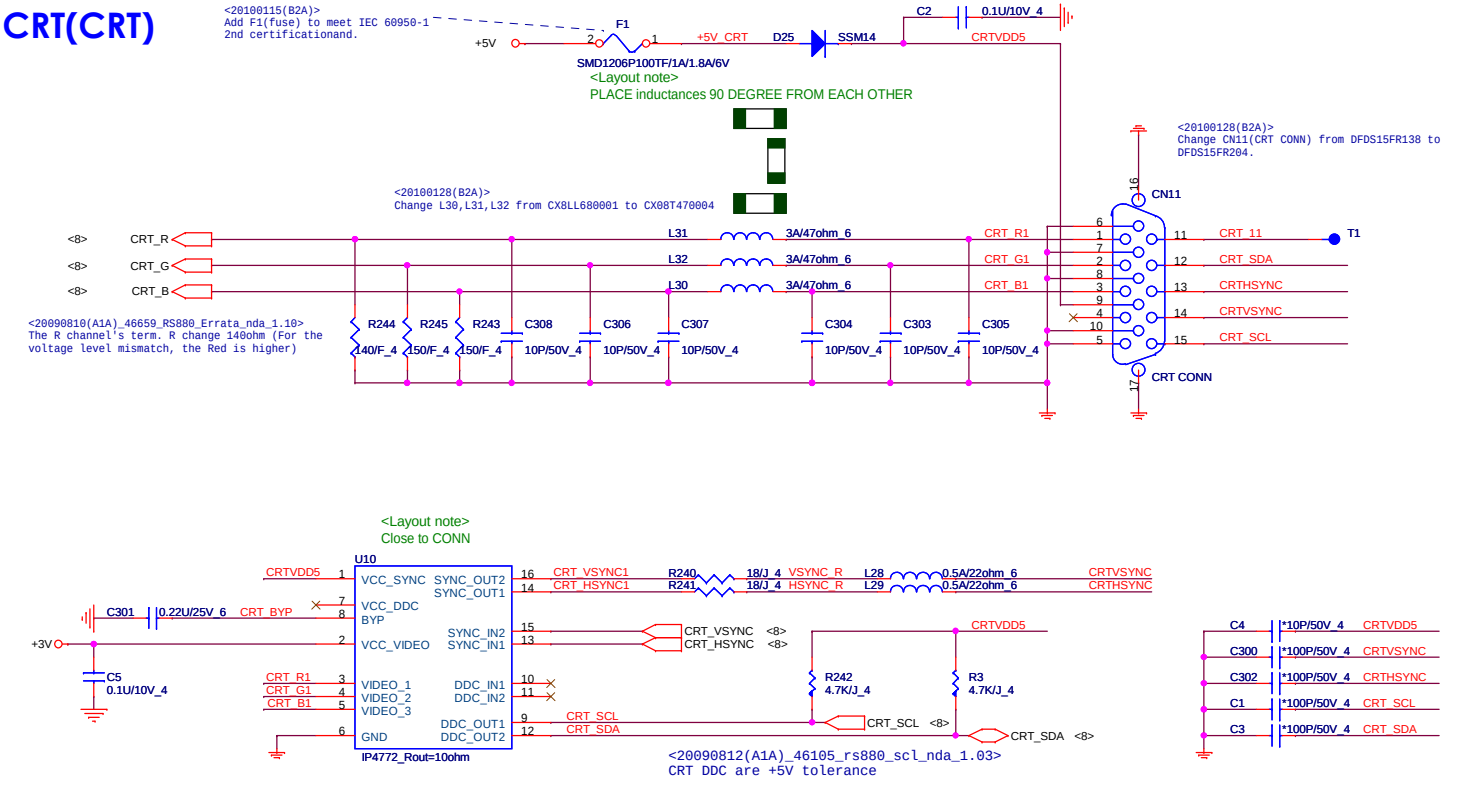
CAMERA POWER(CCD)

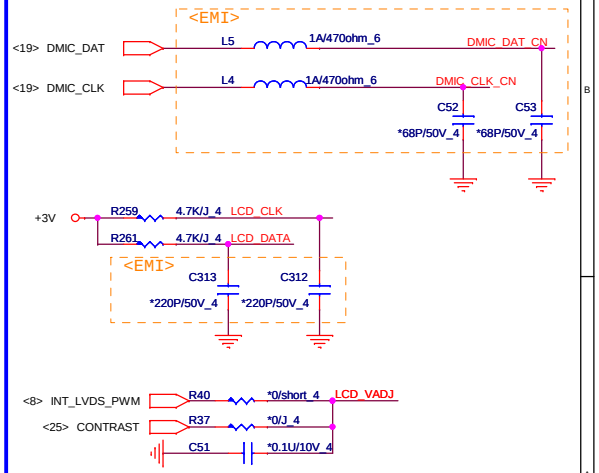


LCD MODULE(LDS)



CRT(CRT)





Quanta Computer Inc.

PROJECT : ZH9

Size	Document Number	Rev
	CRT/LVDS	4A

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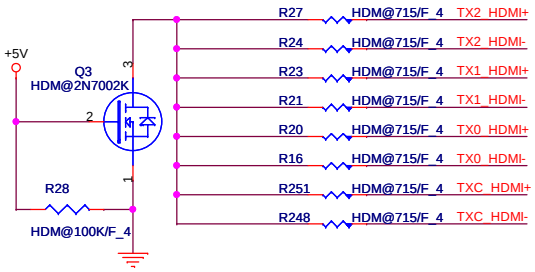
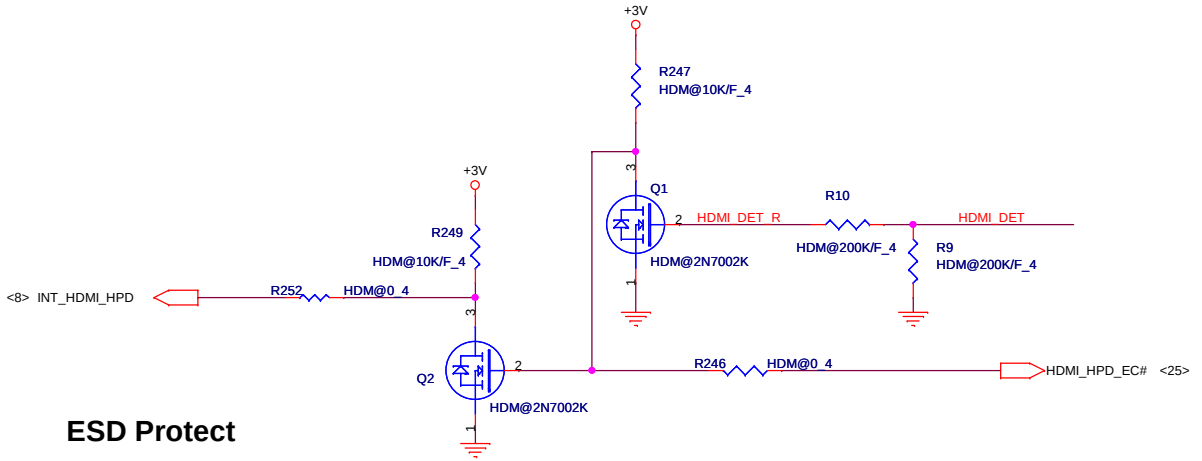
(HDM)

Close to HDMI Connector

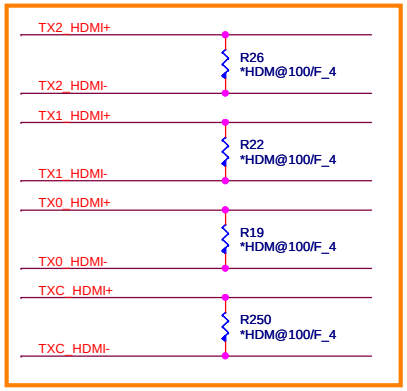


HDMI HPD SENSE



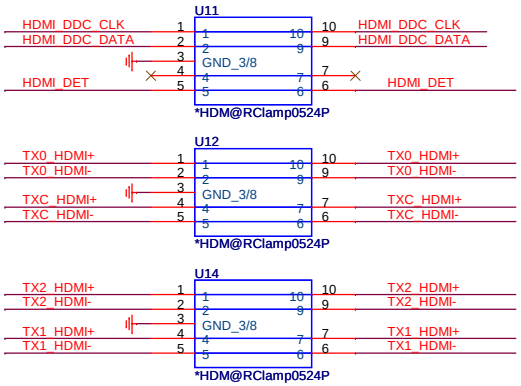
EMI reserve for HDMI(HDM)

Close connector

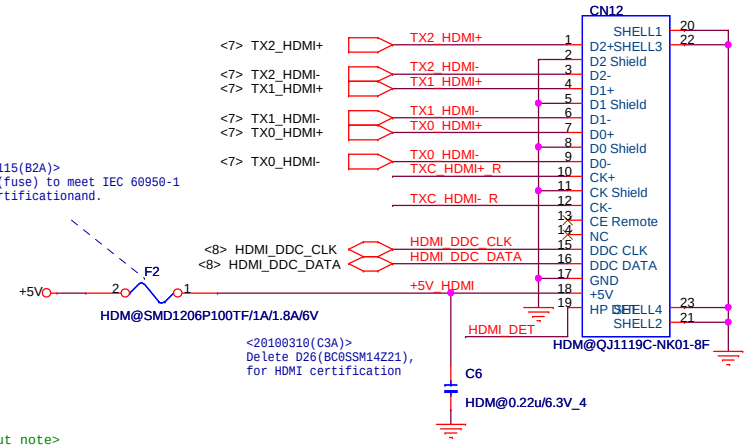


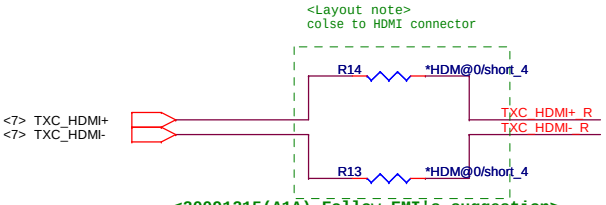
ESD Protect

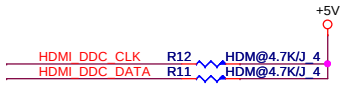
close to HDMI connector



HDMI PORT







<20091215(A1A)_Follow EMI's suggestion>
add a common mode chock in HDMI CLK to
prevent AMD issue

<20100324(RAMP)>
Delete L1 and change R13,R14 to shortpad.

Quanta Computer Inc.
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Size	Document Number	Rev
	HDMI	4A
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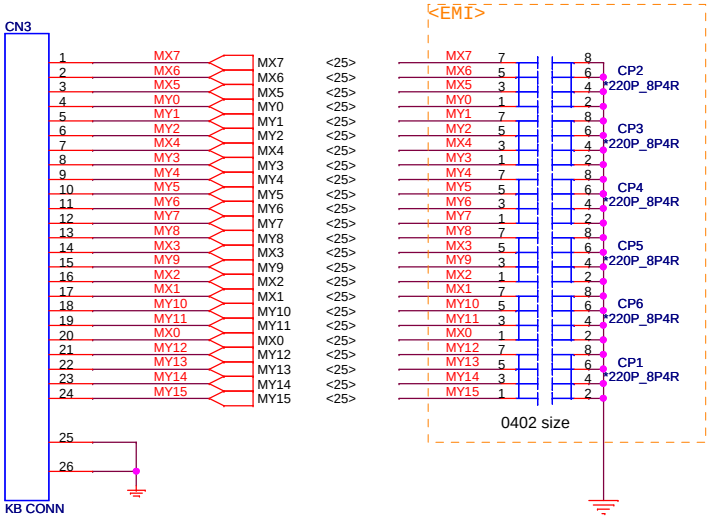
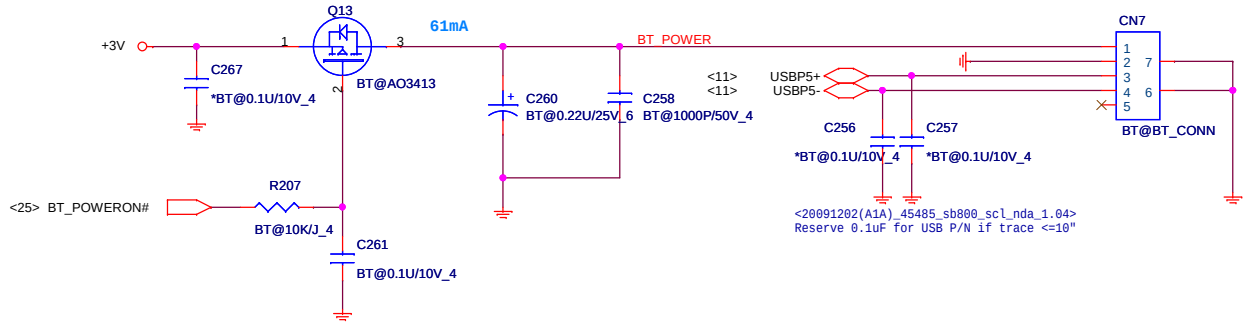
KEYBOARD(KBC)

<20100303(C3A)>
Change CP1~CP6 footprint from 8p4r-0402 to 8p4r-0402-smt, for SMT open issue.

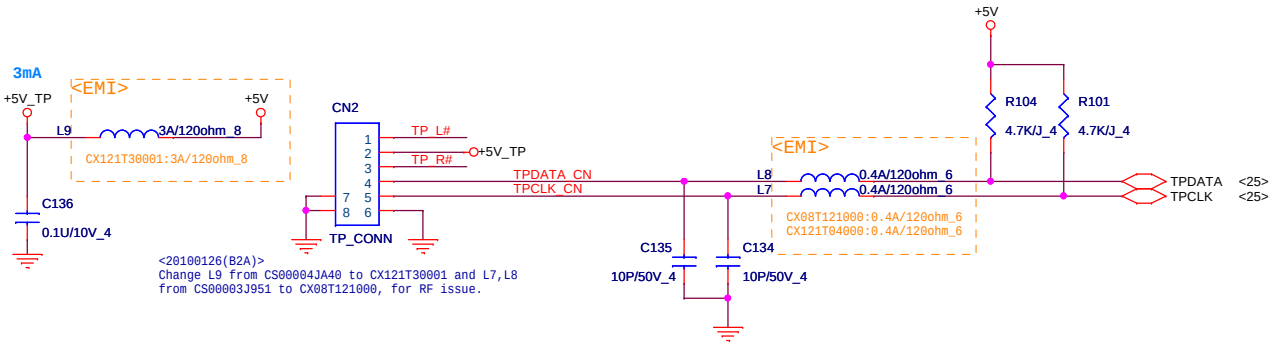


BLUETOOTH(BTM)

BT	PWR	LED
T77H056.00	+3V	
T60H928.33	+3V	



TOUCH PAD(TPD)



<20100126(B2A)>
Change SW2,SW3 from DHP00AC1G00 to DHP00533K00, for SMT issue.

Quanta Computer Inc.
PROJECT : ZH9

Size	Document Number	Rev
	KB/BT/TP/LED/Power Connector	4A
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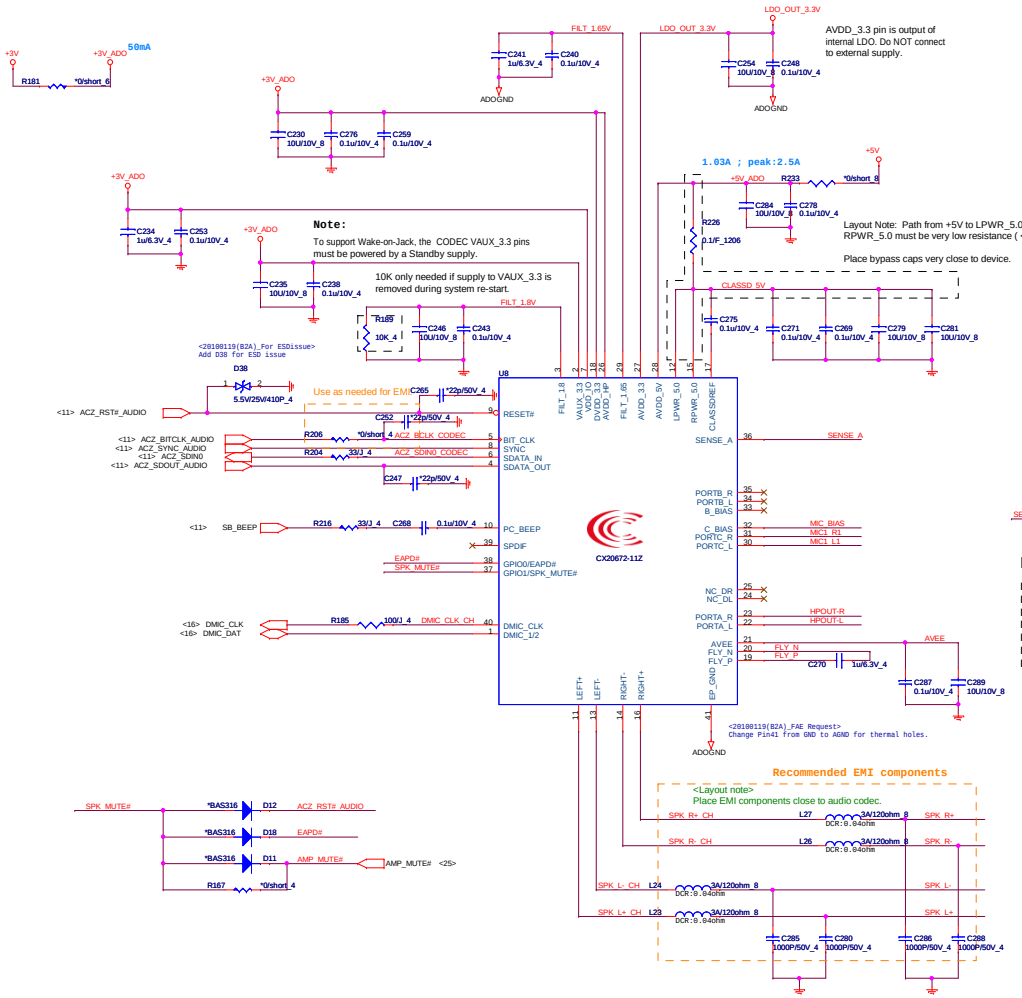
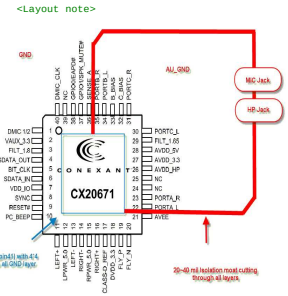
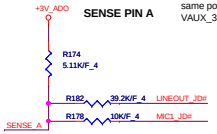
AUDIO CODEC



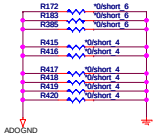


JACK DETECT RESISTORS

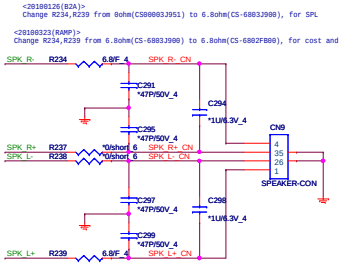


Port Configuration

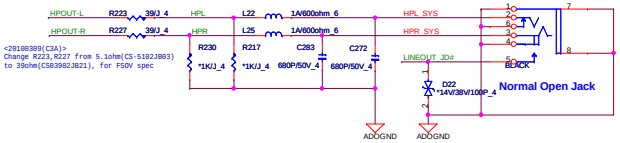
```
Port A:  Headphone jack (jack shared with S/PDIF)
Port B:  Internal analog mono mic (stereo option)/Line In
Port C:  Microphone jack
Port D:  LineOut jack(need cap) or Headphone jack(cap less)
Port G:  Internal stereo speakers
Port J:  Optional Internal stereo digital mic
Port H:  S/PDIF (jack shared with headphone)
```



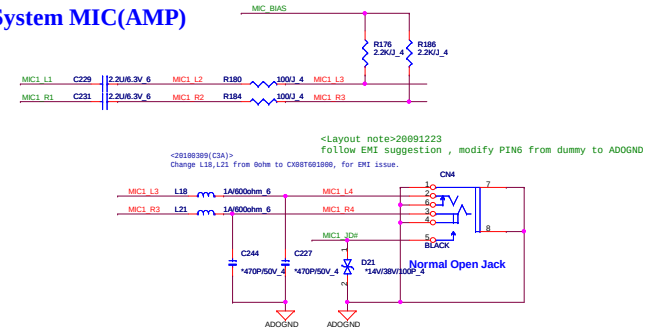
Speaker (AMP)



Earphone(AMP)



System MIC(AMP)



Quanta Computer Inc.			
PROJECT : ZH9			
Size	Document Number		Rev
	AUDIO CODEC CX20672		4A
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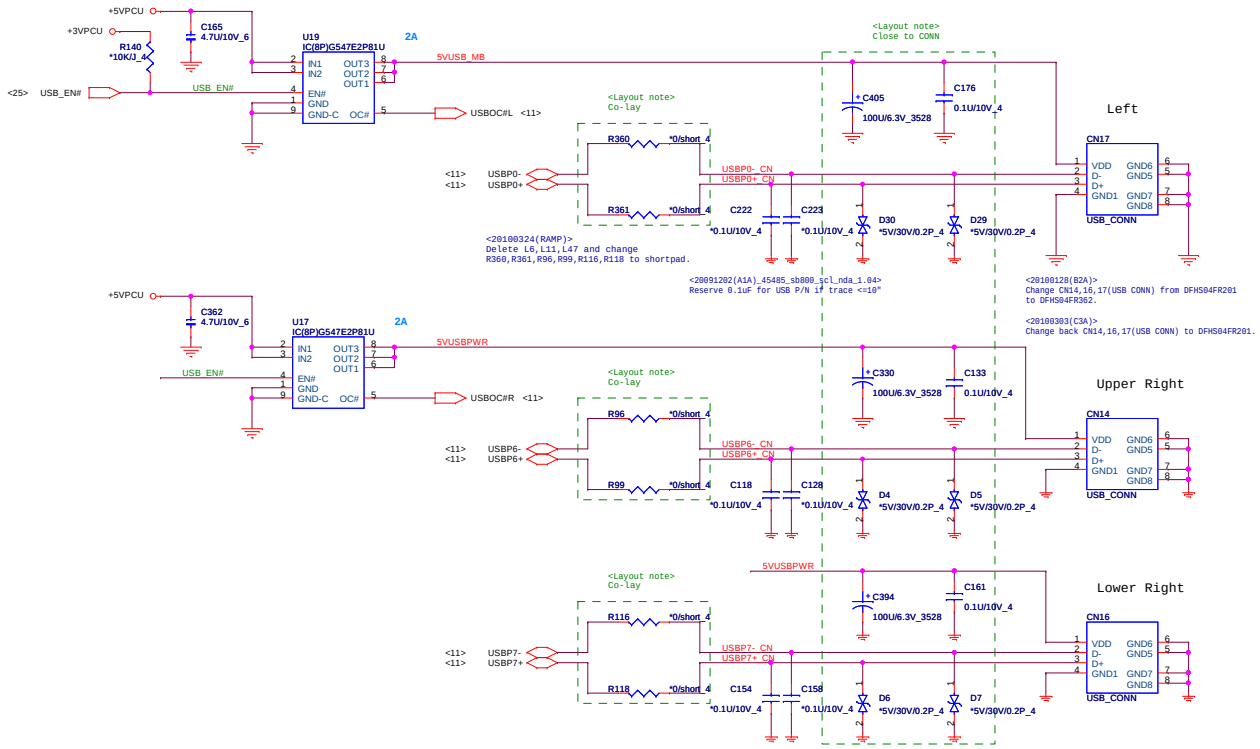
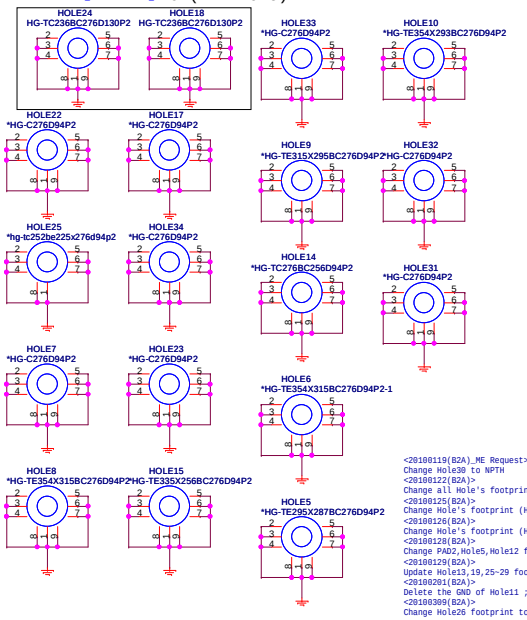
USB(USB)

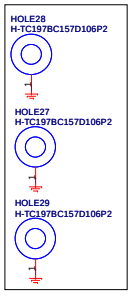


HOLE(OTH)

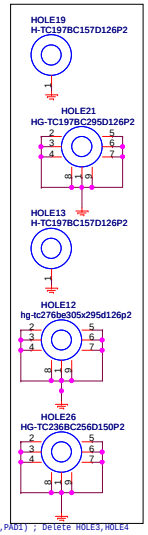
TOP(HDD Hole)

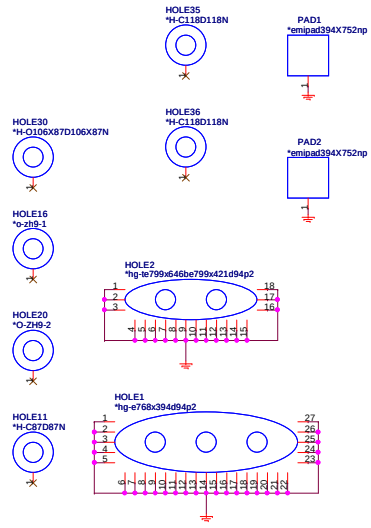


BOT (Mini-PCIe Hole)



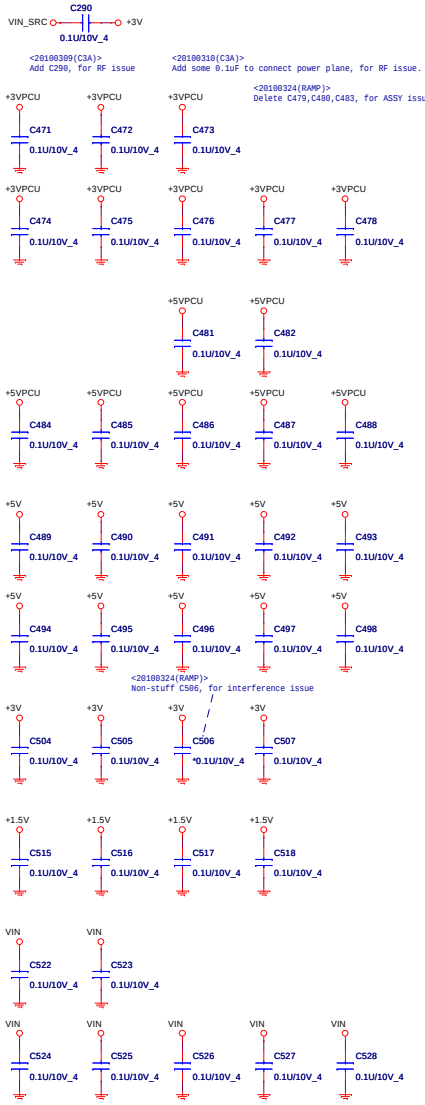
BOT(Thermal Hole)





<20100119(B2A)_ME Request>
Change Hole30 to NPTH
<20100122(B2A)>
Change all Hole's footprint for 凸鍋
<20100125(B2A)>
Change Hole's footprint (HOLE12,HOLE25,HOLE1,HOLE2,HOLE20,PAD1) ; Delete HOLE3,HOLE4
<20100126(B2A)>
Change Hole's footprint (HOLE12)
<20100128(B2A)>
Change PAD2,Hole5,Hole12 footprint ; add two holes (Hole35,Hole36)
<20100129(B2A)>
Update Hole13,19,25~29 footprint.
<20100201(B2A)>
Delete the GND of Hole11 ; add a nut(MBFJ6002010) on Hole26 on BOT side.
<20100309(B2A)>
Change Hole26 footprint to HG-TC236BC256D150P2

EMI(EMC)



Quanta Computer Inc.

PROJECT : ZH9

Size	Document Number	Rev
	USB on Board/LED/SW/HOLE	4A

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<BOM note>
If center tap power come from internal switch regulator
=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO
=>Stuff 52LDO@

<20100303(C3A)_FAE's suggestion>
Change L3 from CV-4710MN03 to CV-4710TZ01.

<Layout note>
Close to Pin40

L3 52SWR@4.7uH/1A DCR:0.15ohm LX
C46 52SWR@1000P/50V_4
C47 52SWR@0.1U/16V_4
C30 52SWR@10U/10V_8
VDDCT
VDDCT_REG R35 *52LDO@0/J_6
C37 0.1U/16V_4
C48 *52LDO@1U/10V_4

C67 *3P/50V_4
<10> CLK_25M_LAN XTLI_LAN
C43 33P/50V_4 XTLO_LAN
XTLI_LAN
Y1 25MHz-LAN
C44 33P/50V_4

<20100129(B2A)>
Non-stuff Y1,C43,C44 ; Stuff C67. Change the value of C43,C44 from 27pF to 33pF. (CLK for LAN from crystal change to internal CLK.)

<20100310(C3A)>
Stuff Y1,C43,C44 ; Non-Stuff C67. (14M_25M_48M_OSC is S0 plane, doesn't support WoL.)

76.1mA ; 30mil <Layout note> Close to Pin1

+3V_S5 +3V_LAN
R36 *0/short_6
C69 10U/10V_8
C45 1U/10V_4
C36 0.1U/16V_4
C28 1000P/50V_4

Power Sequence:
VDD33 to PERSTn >= 100ms

U1
AR8152
5X5mm
40-Pin QFN
AR8152-AL1A-RL

1 VDD33
2 PERSTn <10,23,24> PLTRST#
3 WAKEn <11,23> PCIE_WAKE#
4 VDDCT_REG
5 VDDCT
6 AVDDL_REG
7 XTLO XTLO_LAN
8 XTLI XTLI_LAN
9 AVDDH_REG
10 RBIAS R29 2.37K/F_4 RBIAS
11 TRXP0 TX0P
12 TRXN0 TX0N
13 NC
14 TRXP1 TX1P
15 TRXN1 TX1N
16 NC
17 NC
18 NC
19 NC
20 NC
21 NC

Int. PU in SB
20mil VDDCT C40 0.1U/16V_4
20mil AVDDL C41 1U/10V_4 C42 0.1U/16V_4
20mil AVDDH C33 1U/10V_4 C34 0.1U/16V_4

<Layout note>
Close to LAN Chip
1nF reserved for EMI
RN2 49.9/F_4P2R
RN1 49.9/F_4P2R
C21 0.1U/16V_4 C18 *1000P/50V_4
C14 0.1U/16V_4 C15 *1000P/50V_4

22 AVDDH
23 CLKREQn R413 *4.7K/J_4 R412 *0/short_4 CLKREQ_LAN# <11>
24 DVDDL
25 SMCLK SMBUS for debug only
26 SMDATA
27 TESTMODE
28 TEST_RST R15 4.7K/J_4 +3V_LAN
29 TX_N PCIE_RXN0_LAN C7 0.1u/10V_4 PCIE_RXN0 <7>
30 TX_P PCIE_RXP0_LAN C10 0.1u/10V_4 PCIE_RXP0 <7>
31 AVDDL
32 REFCLK_N CLK_PCIE_LANN <10>
33 REFCLK_P CLK_PCIE_LANP <10>
34 AVDDL
35 RX_P PCIE_TXP0 <7>
36 RX_N PCIE_TXN0 <7>
37 DVDDL_REG
38 LED0 LAN_ACTLED
39 LED1 LAN_LINKLED#
40 LX 40mil
41 GND

AVDDH C9 0.1U/16V_4
PU in CLK Gen.
<20100303(C3A)> Reserve R413,R414, for e-fuse.
DVDDL C8 0.1U/16V_4
R414 *1K/J_4
AVDDL C11 0.1U/16V_4
C13 0.1U/16V_4
DVDDL 20mil
C19 0.1U/16V_4
C16 1U/10V_4

AR8152-A : w/o 802.3az
AR8152-B : w/ 802.3az

ATHEROS AR8152

+3V_S5	1	VDD33	AVDDL_REG	6	+1.1V regulator output (For all the analog 1.1V supply pins)
+1.1V analog power	31/34	AVDDL	AVDDH_REG	9	+2.7V regulator output (Connected to pin 22)
+1.1V digital power	24	DVDDL	DVDDL_REG	37	+1.1V regulator output (For all the digital 1.1V supply pins)
+2.7V analog power	22	AVDDH	VDDCT_REG	4	+1.8V regulator output (For VDDCT when LDO mode)
+1.7V analog power	5	VDDCT	LX	40	+1.7V Switching regulator (For VDDCT when switching mode)

TRANSFORMER

VDDCT L2 *0/short_6 AVDD_CEN
CX8EG601000: 0.5A/600ohm_6
C22 1U/6.3V_4
C24 0.1U/16V_4
C26 *1000P/50V_4
C23 0.1U/16V_4
C25 *1000P/50V_4
InF reserved for EMI

U13
NS0014 LF_Bothhand

TX1N	8 TD-	TX- 9	X-TX1N
TX1P	7 TD+	TX+ 10	X-TX1P
	6 CT	CT 11	TERM0
	5 NC	NC 12	
	4 NC	NC 13	
	3 CT	CT 14	TERM1
TX0N	2 RD-	RX- 15	X-TX0N
TX0P	1 RD+	RX+ 16	X-TX0P

R18 75/F_8 R17 75/F_8
C12 1000P/3KV_1808 TERM9

R25 5.1K/J_8
C17 *0.1u/50V_8 LAN_ACTLED
Active LED Pin:
Non-overclocking=>active high
R30 *52LDO@5.1K/J_8
C54 *0.1u/50V_8 LAN_LINKLED#
LINK LED Pin:
SWR mode=>active low
LDO mode=>active high

<20100125(B2A)>
Connect pin4,5,7,8 of CN10 to net TERM9, for EMI and Safety issue

RJ45

CN10
LAN_ACTLED R8 510/J_6
TERM9
X-TX1N
TERM9
X-TX1P
X-TX0N
X-TX0P
R7 *52LDO@0/J_8
LAN_LINKLED# R6 52SWR@510/J_6
R5 *52LDO@510/J_6
+3V_S5 R4 *52SWR@0/short_8

12	Y-	Y+	10
8	NC4/3-	NC/3+	7
6	RX-/1-	NC2/2-	5
4	NC1/2+	RX+/1+	3
2	TX-/0-	TX+/0+	1
14	GND	GND	13
11	G-	G+	9

RJ45-CONN

<20100125(B2A)>
Change CN10 from DFTJ12FR069(SUY) to DFTJ12FR066(FOX), for SMT issue.

Quanta Computer Inc.
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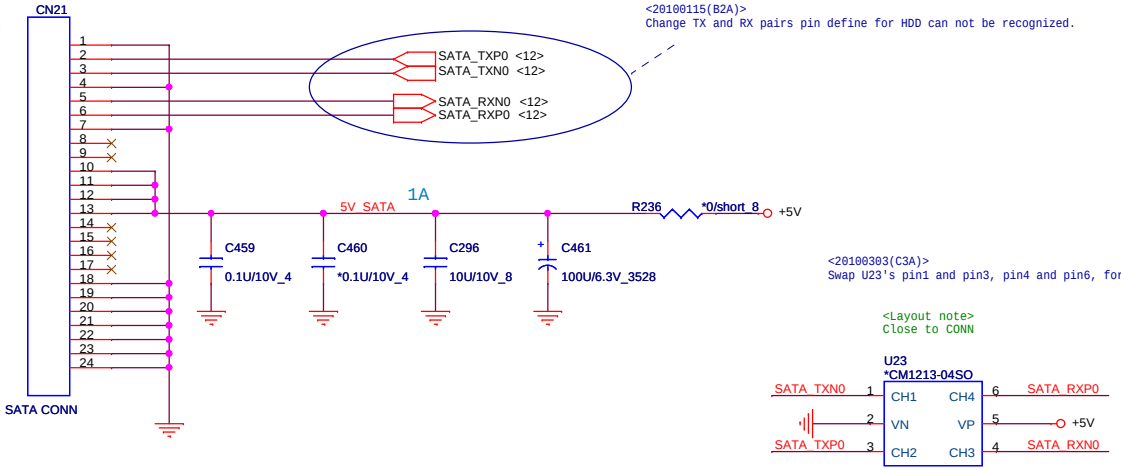
2.5" SATA HDD(HDD)



<20100115(B2A)>
Change TX and RX pairs pin define for HDD can not be recognized.

<20100303(C3A)>
Swap U23's pin1 and pin3, pin4 and pin6, for layout issue.

<Layout note>
Close to CONN

LED/SW(UIF)

<20091214(A1A)_Confirm with Acer Johnson_Yeh>
The JV01_NL and SJV01_NL had 4 LEDs --> Power / Battery / HDD / Communication

<20100203(B2A)>
Change R401 from CS13302JB21 to CS12702JB14
Change R402 from CS13302JB21 to CS14702JB28
Change R403 from CS13302JB21 to CS11202JB21
Change R404,R406 from CS13302JB21 to CS15602JB19
Change R405,R407 from CS13302JB21 to CS13602JB13
For LED's light issue.

<20100326(RAMP)>
Change R401 from CS12702JB14 to CS13302JB21
Change R404,R406 from CS15602JB19 to CS14702JB28
Change R403 from CS11202JB21 to CS12702JB14
Change R405,R407 from CS13602JB13 to CS12702JB14
For LED's light issue.

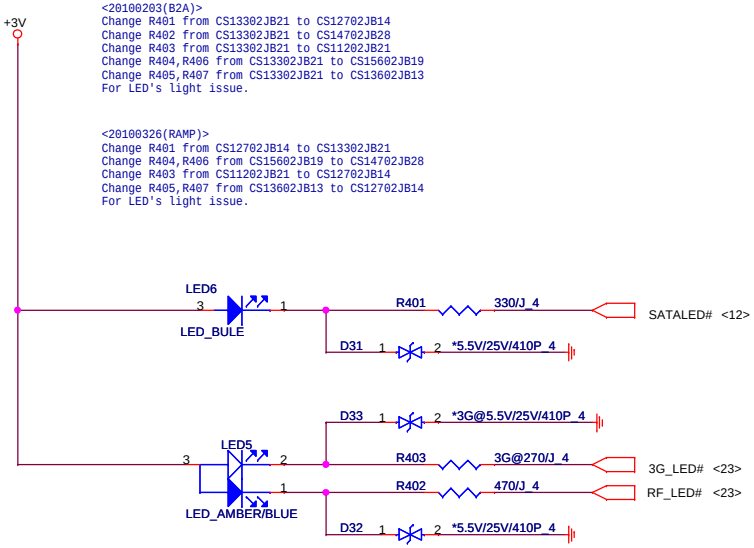
CAPS LED

NUM LED

HDD LED

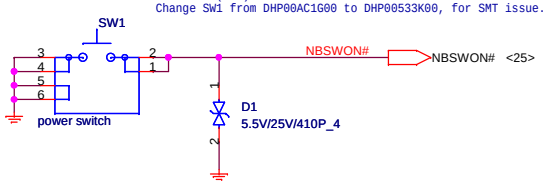
3G LED

WLAN LED

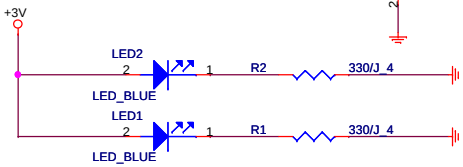


BT LED

<20100125(B2A)>
Change SW1 from DHP00AC1G00 to DHP00533K00, for SMT issue.

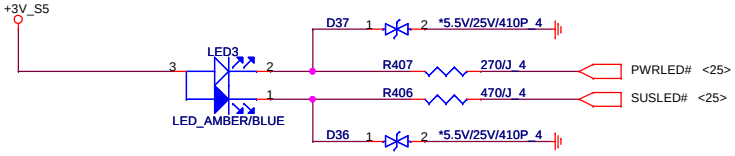


PWR indicator



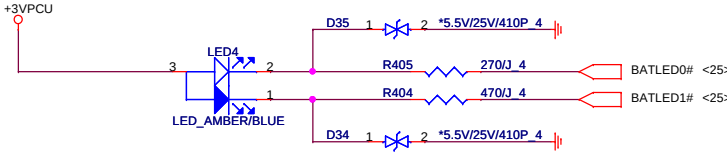
PWR LED

SUS LED



FULL LED

CHG LED



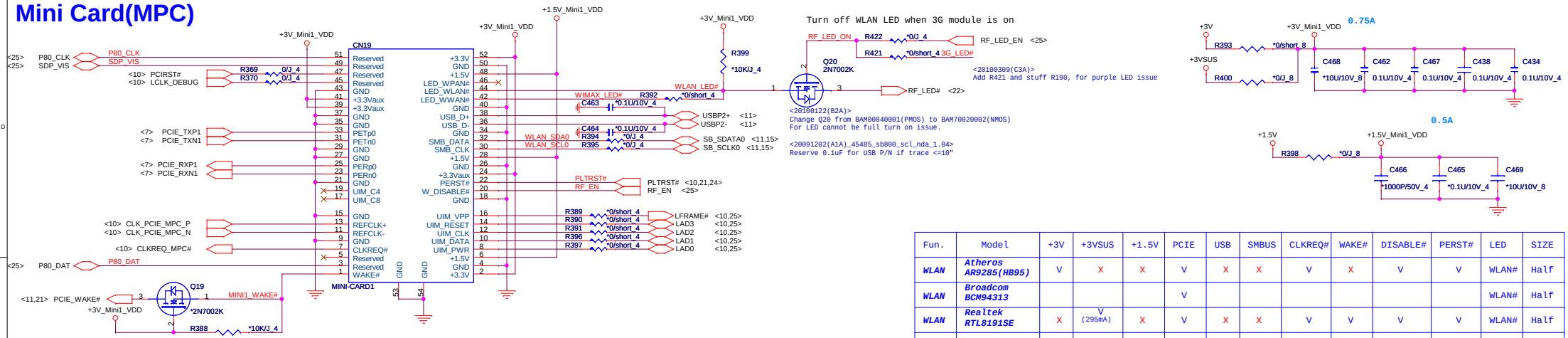
<LED spec>
BLUE :
Vf = 2.7~3.2V ; If = 5mA
BLUE/ORANGE :
BH→Vf = 2.7~3.7V ; If = 20mA max=25mA
S2→Vf = 1.7~2.4V ; If = 20mA max=25mA

ID(Left-->Right)
Power LED/BATT LED/HDD LED/WiFi LED

Quanta Computer Inc.
PROJECT : ZH9

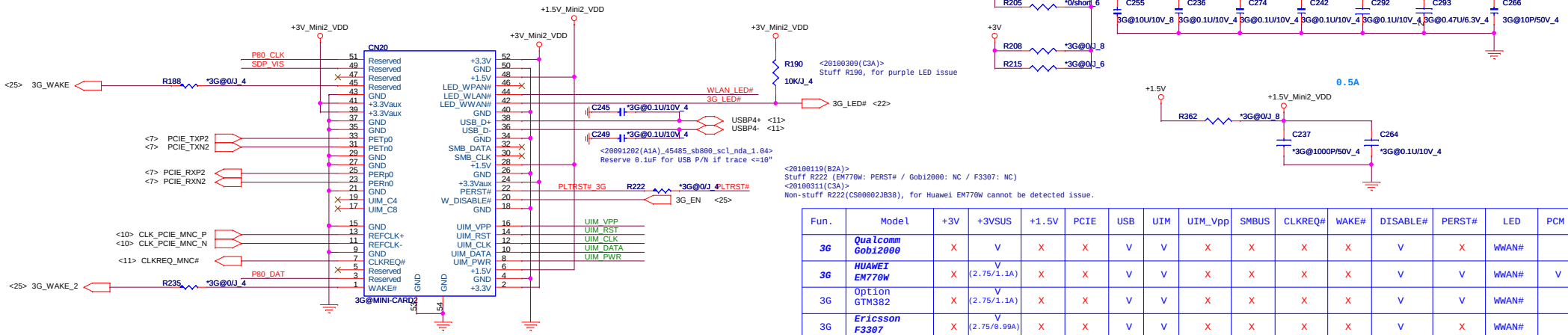
Size	Document Number	Rev
	SATA HDD/LED/SW	4A
Date: Sunday, March 28, 2010	Sheet 22 of 40	

Mini Card(MPC)



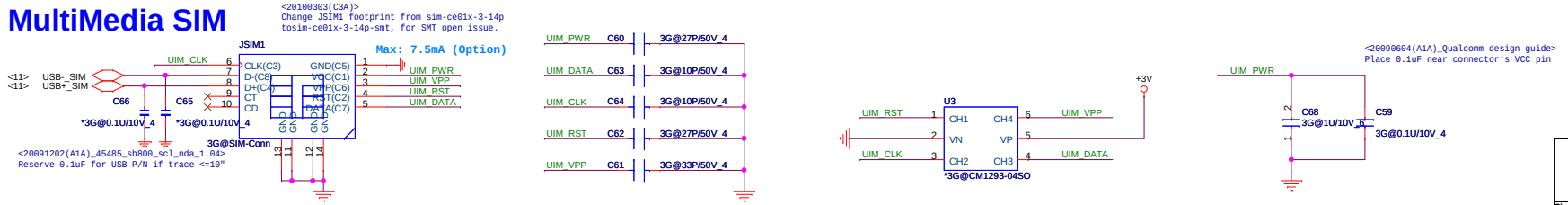
Fun.	Model	+3V	+3VSUS	+1.5V	PCIE	USB	SMBUS	CLKREQ#	WAKE#	DISABLE#	PERST#	LED	SIZE
WLAN	Atheros AR9285(HB95)	V	X	X	V	X	X	V	X	V	V	WLAN#	Half
WLAN	Broadcom BCM94313				V							WLAN#	Half
WLAN	Realtek RTL8191SE	X	V (295mA)	X	V	X	X	V	V	V	V	WLAN#	Half

Mini Card 2(MNC)



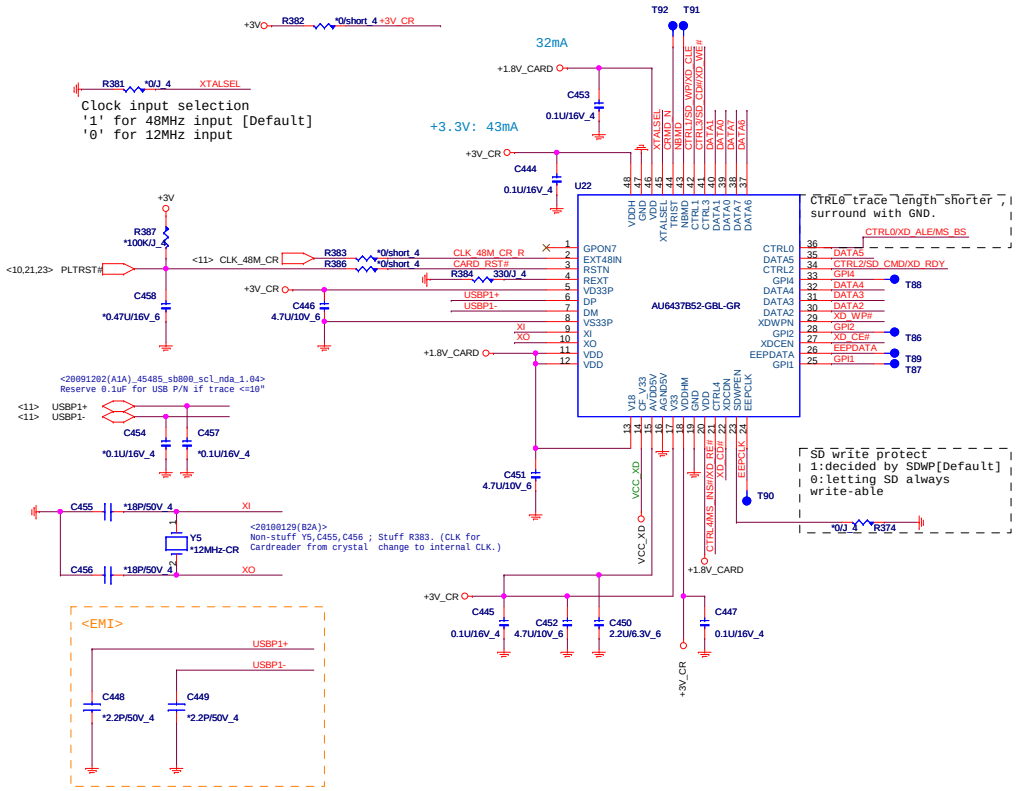
Fun.	Model	+3V	+3VSUS	+1.5V	PCIE	USB	UIM	UIM_Vpp	SMBUS	CLKREQ#	WAKE#	DISABLE#	PERST#	LED	PCM	SIZE
3G	Qualcomm Gobi2000	X	V	X	X	V	V	X	X	X	X	V	X	WWAN#		Full
3G	HUAWEI EM770W	X	V (2.75/1.1A)	X	X	V	V	X	X	X	X	V	V	WWAN#	V	Full
3G	Option GTM382	X	V (2.75/1.1A)	X	X	V	V	X	X	X	X	V	V	WWAN#		Full
3G	Ericsson F3307	X	V (2.75/0.99A)	X	X	V	V	X	X	X	X	V	X	WWAN#		Full
Wimax	Intel 5150(512...)	X	V (643mA)	X	V	V	X	X	X	V	V	V	V	WLAN# WWAN#		Full

MultiMedia SIM

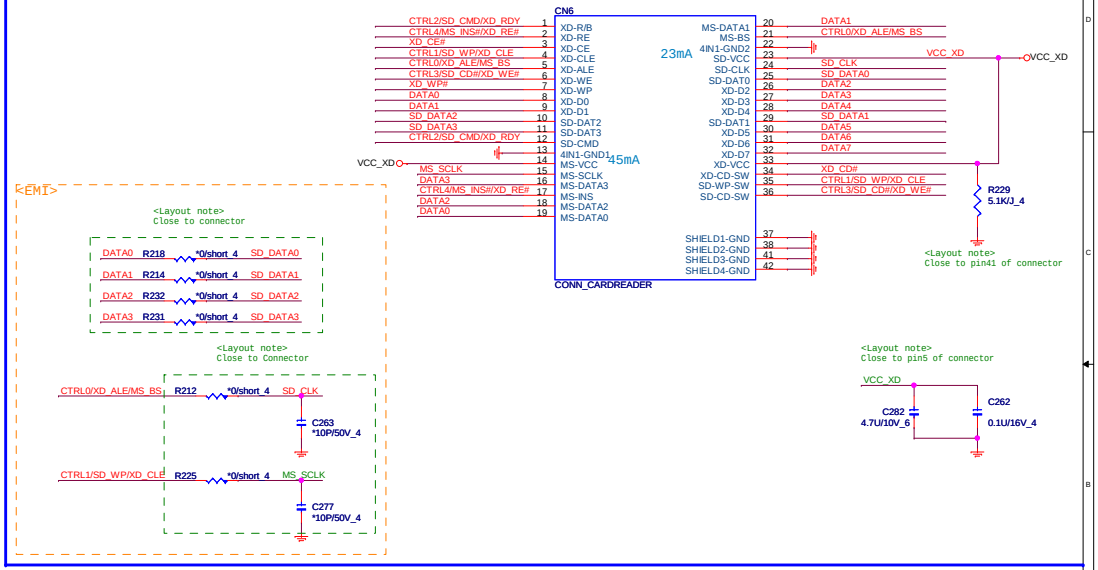


Quanta Computer Inc.	
PROJECT : ZH9	
Size	Document Number: Mini-Card/WL/3G/SIM — Rev: 4A
Date: Sunday, March 28, 2010	Sheet 23 of 40

AU6437B52-GBL-GR (MMC)



4 IN 1 CARD READER (MMC)



Quanta Computer Inc.			
PROJECT : ZH9			
Size	Document Number		Rev
	AU6437 (Card Reader)		4A
Date: Sunday, March 28, 2010	Sheet 24	of	40

EC(KBC)

<Layout note>
Place every 0.1uF
close to every
power pin

U6

NPCE781L(A0DX)

I/O ADDRESS SETTING

TEST Mode	TEST#	XORTR#	TRIST#
no test mode selected (normal operation)	1	X	X
XOR-tree test mode	0	0	1
ICT mode	0	1	0
Reserved exclusively for Nuvoton use	0	00 or 11	

SHBM=0: Enable shared memory with host BIOS

SM BUS PU

1ST: Battery
2ND: CPU Thermal Sensor / DTS
3RD: VGA Thermal Sensor

SPI FLASH

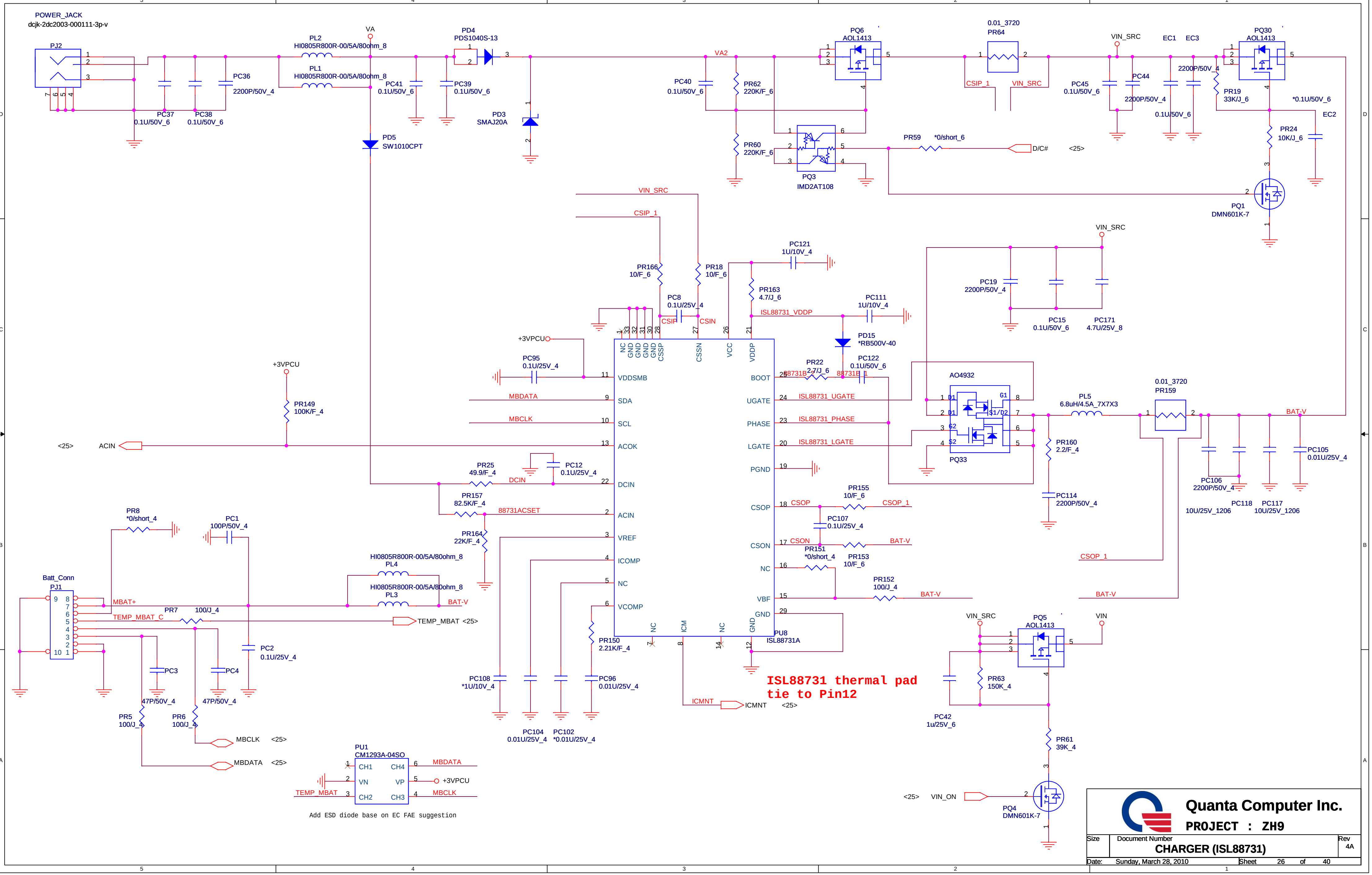
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

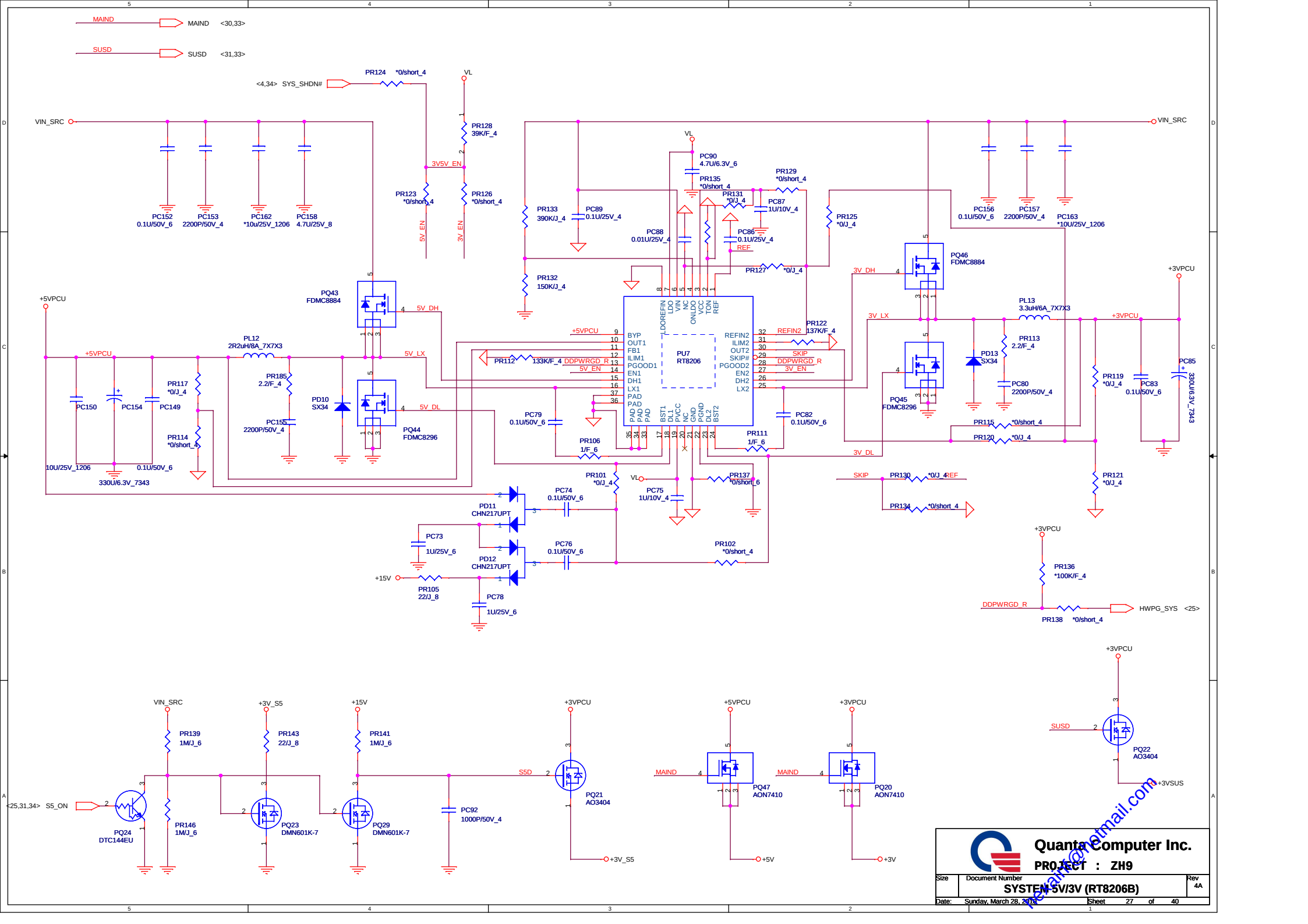
HWPG

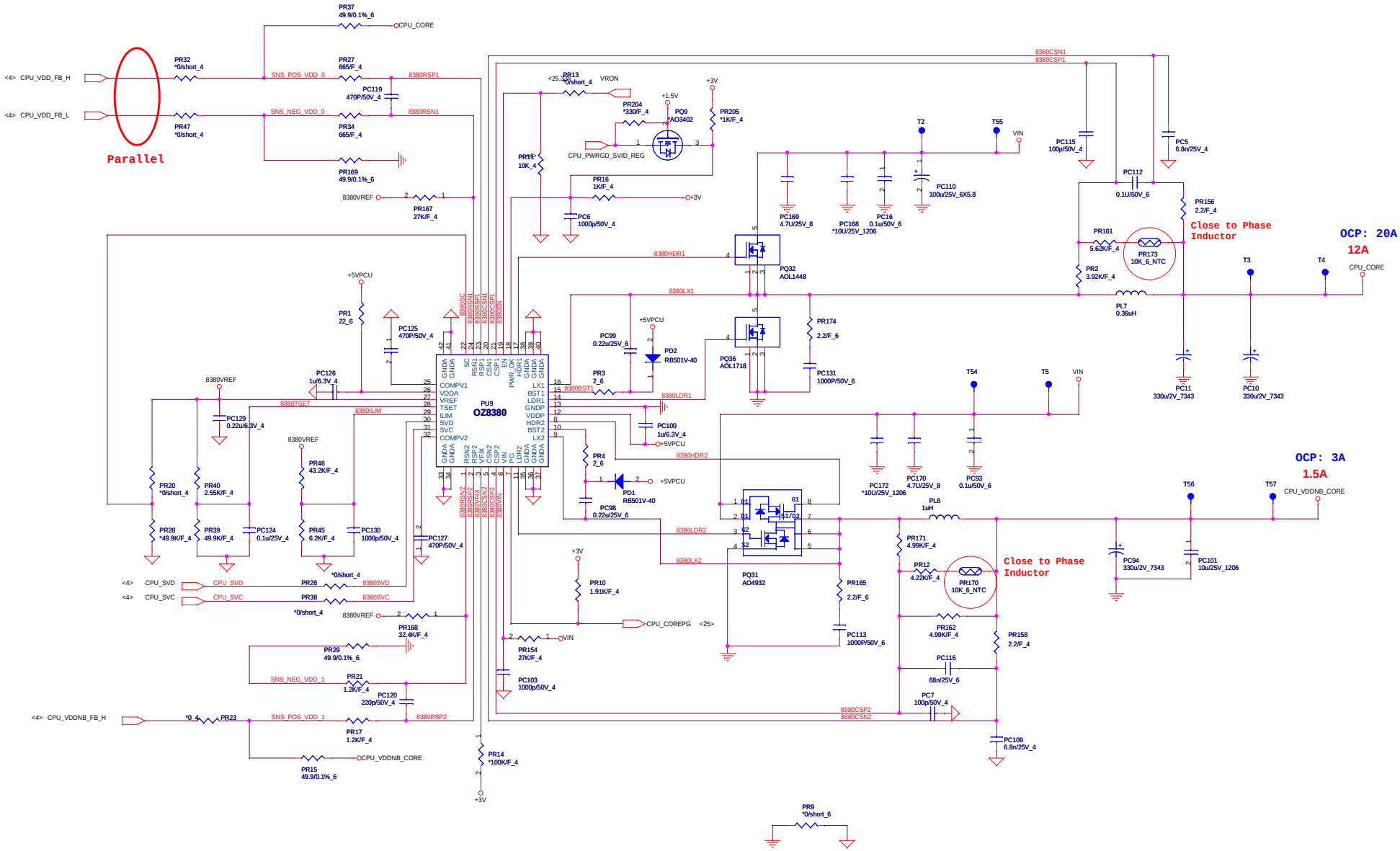
INTERNAL KEYBOARD STRIP SET

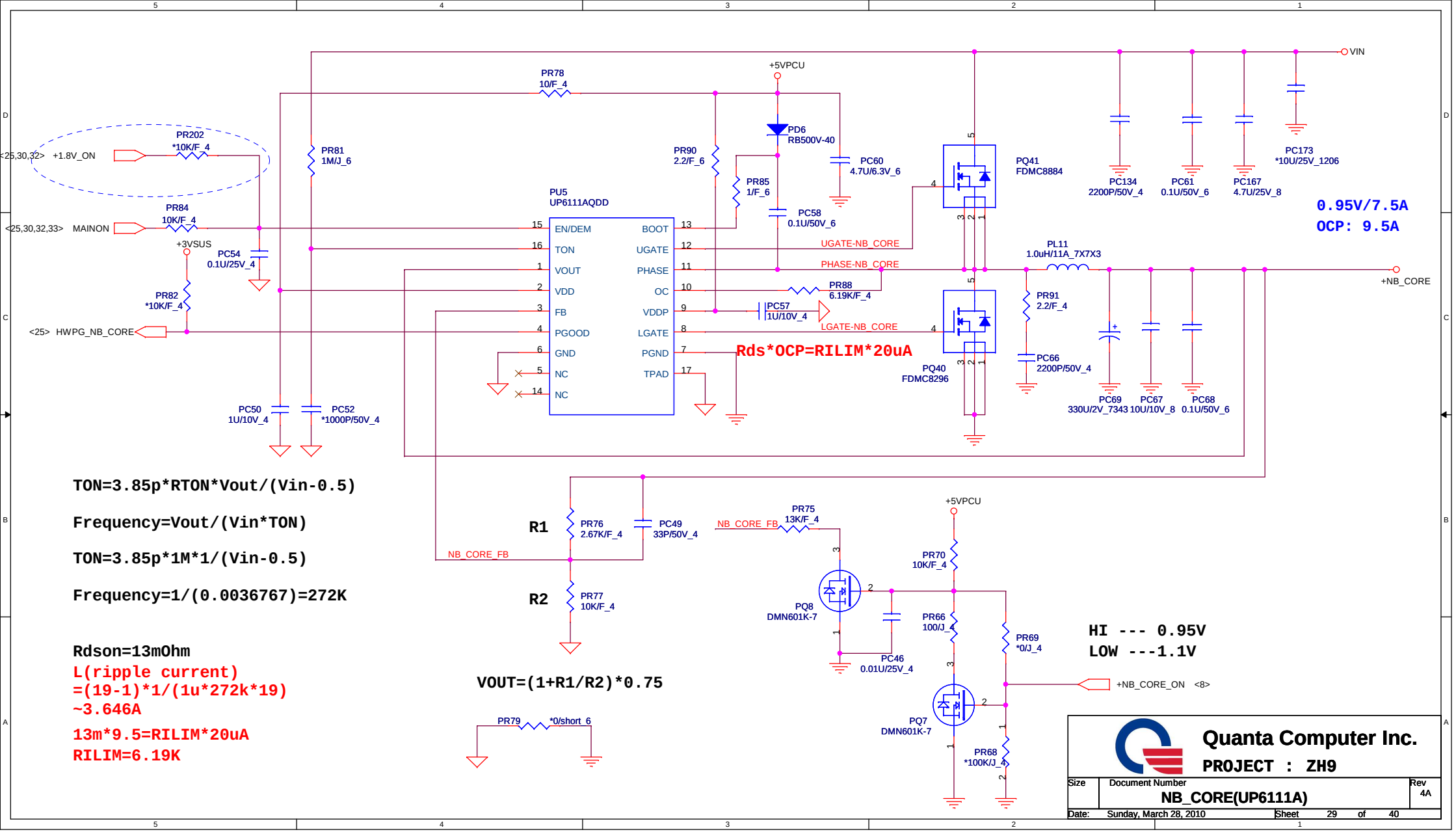
Plam Rest
Thermal Sersor

Quanta Computer Inc.	
PROJECT : ZH9	
Size	Document Number: NPCE781L & FLASH — Rev: 4A
Date: Sunday, March 28, 2010	Sheet 25 of 40

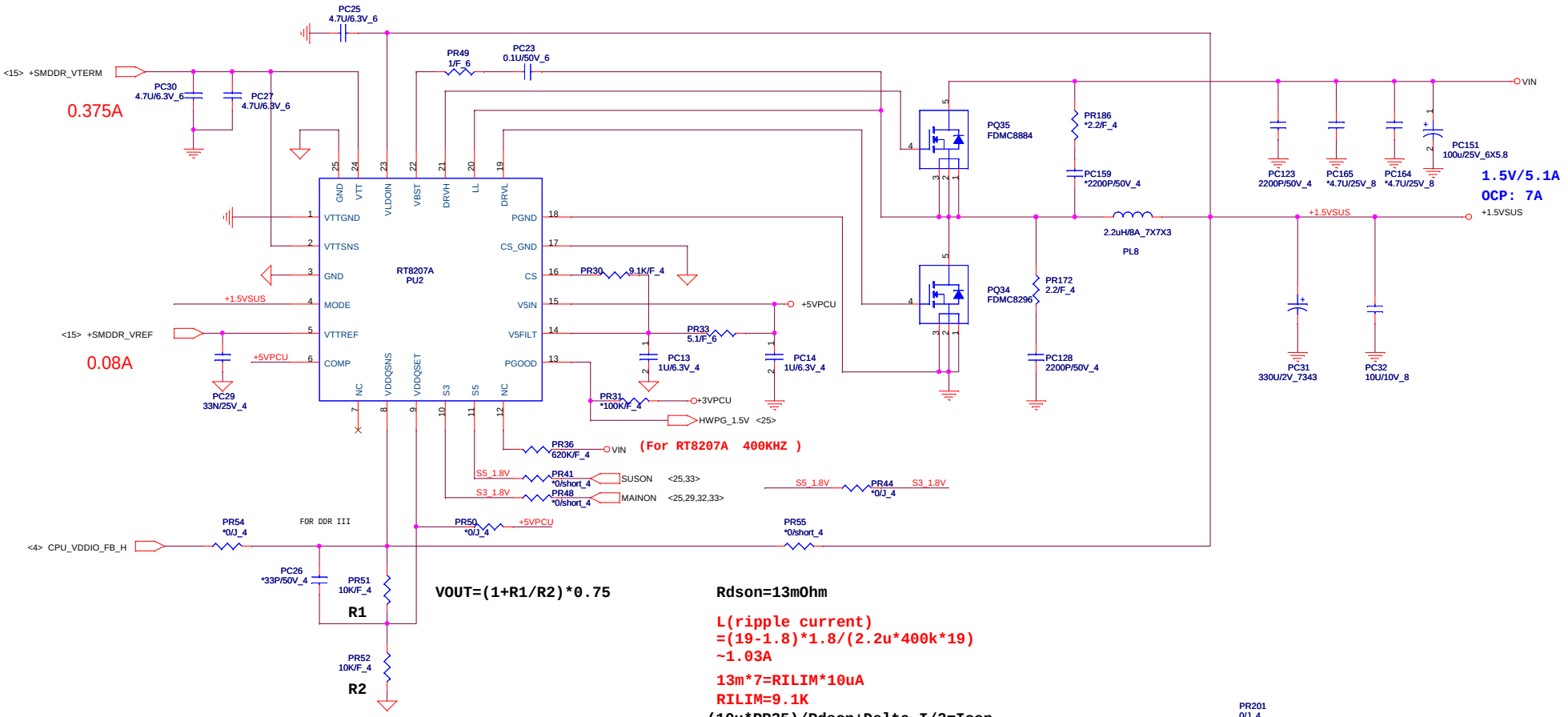

POWER_JACK
dcjk-2dc2003-000111-3p-v
PJ2
PL2
HI0805R800R-00/5A/80ohm_8
PL1
HI0805R800R-00/5A/80ohm_8
VA
PD4
PDS1040S-13
PD3
SMAJ20A
PD5
SW1010CPT
PC36
2200P/50V_4
PC37
0.1U/50V_6
PC38
0.1U/50V_6
PC41
0.1U/50V_6
PC39
0.1U/50V_6
VA2
PC40
0.1U/50V_6
PR62
220K/F_6
PR60
220K/F_6
PQ6
AOL1413
PQ3
IMD2AT108
0.01_3720
PR64
CSIP_1
VIN_SRC
PR59
*0/short_6
D/C#
<25>
PC45
0.1U/50V_6
PC44
2200P/50V_4
EC1
EC3
0.1U/50V_6
2200P/50V_4
PR19
33K/J_6
PQ30
AOL1413
*0.1U/50V_6
EC2
PR24
10K/J_6
PQ1
DMN601K-7
PR166
10/F_6
PR18
10/F_6
PC8
0.1U/25V_4
CSIP
CSIN
PC121
1U/10V_4
PR163
4.7/J_6
ISL88731_VDDP
PC111
1U/10V_4
PD15
*RB500V-40
PC19
2200P/50V_4
PC15
0.1U/50V_6
PC171
4.7U/25V_8
+3VPCU
PC95
0.1U/25V_4
PR149
100K/F_4
ACIN
MBDATA
MBCLK
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
NC GND GND GND GND CSSP CSSN VCC VDDP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
NC ICM NC GND
PU8
ISL88731A
PR22
2.7/J_6
PC122
0.1U/50V_6
88731B
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
AO4932
PQ33
PL5
6.8uH/4.5A_7X7X3
0.01_3720
PR159
BAT-V
PR160
2.2/F_4
PC114
2200P/50V_4
PC106
2200P/50V_4
PC118
10U/25V_1206
PC117
10U/25V_1206
PC105
0.01U/25V_4
PC12
0.1U/25V_4
PR25
49.9/F_4
PR157
82.5K/F_4
88731ACSET
PR164
22K/F_4
PR155
10/F_6
CSOP
CSOP_1
PC107
0.1U/25V_4
CSON
PR151
*0/short_4
PR153
10/F_6
PR152
100/J_4
PR8
*0/short_4
PC1
100P/50V_4
Batt_Conn
PJ1
MBAT+
TEMP_MBAT_C
PR7
100/J_4
HI0805R800R-00/5A/80ohm_8
PL4
HI0805R800R-00/5A/80ohm_8
PL3
TEMP_MBAT
PC2
0.1U/25V_4
PC3
PC4
47P/50V_4
47P/50V_4
PR5
100/J_4
PR6
100/J_4
MBCLK
MBDATA
PC108
*1U/10V_4
PC104
0.01U/25V_4
PC102
*0.01U/25V_4
PR150
2.21K/F_4
PC96
0.01U/25V_4
ICMNT
ISL88731 thermal pad
tie to Pin12
PQ5
AOL1413
VIN
PR63
150K_4
PC42
1u/25V_6
PR61
39K_4
VIN_ON
PQ4
DMN601K-7
PU1
CM1293A-04SO
CH1 CH4 VN VP CH2 CH3
TEMP_MBAT
+3VPCU
Add ESD diode base on EC FAE suggestion
Quanta Computer Inc.
PROJECT : ZH9
Size
Document Number
CHARGER (ISL88731)
Rev
4A
Date: Sunday, March 28, 2010
Sheet 26 of 40


MAIND
MAIND <30,33>
SUSD
SUSD <31,33>
<4,34> SYS_SHDN#
PR124 *0/short_4
VL
VIN_SRC
PR128 39K/F_4
PR123 *0/short_4
PR126 *0/short_4
3V5V_EN
5V_EN
3V_EN
PC152 0.1U/50V_6
PC153 2200P/50V_4
PC162 *10u/25V_1206
PC158 4.7U/25V_8
PR133 390K/J_4
PC89 0.1U/25V_4
PR132 150K/J_4
PC90 4.7U/6.3V_6
PR135 *0/short_4
PR131 *0/J_4
PR129 *0/short_4
PC87 1U/10V_4
PC88 0.01U/25V_4
PC86 0.1U/25V_4
REF
PR127 *0/J_4
PR125 *0/J_4
PC156 0.1U/50V_6
PC157 2200P/50V_4
PC163 *10U/25V_1206
PU7 RT8206
LDOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
BST1
DL1
PVCC
NC
GND
PGND
DL2
BST2
PR122 137K/F_4
PR112 133K/F_4
DDPWRGD_R
SKIP
3V_EN
PC79 0.1U/50V_6
PC82 0.1U/50V_6
PR106 1/F_6
PR111 1/F_6
PR101 *0/J_4
PR137 *0/short_6
PC74 0.1U/50V_6
PC75 1U/10V_4
PD11 CHN217UPT
PD12 CHN217UPT
PC73 1U/25V_6
PC76 0.1U/50V_6
PR102 *0/short_4
PR105 22/J_8
PC78 1U/25V_6
+15V
+5VPCU
+3VPCU
PQ43 FDMC8884
PQ44 FDMC8296
PQ46 FDMC8884
PQ45 FDMC8296
5V_DH
5V_LX
5V_DL
3V_DH
3V_LX
3V_DL
PL12 2R2uH/8A_7X7X3
PL13 3.3uH/6A_7X7X3
PR117 *0/J_4
PR114 *0/short_4
PR185 2.2/F_4
PC155 2200P/50V_4
PD10 SX34
PD13 SX34
PR113 2.2/F_4
PC80 2200P/50V_4
PR119 *0/J_4
PC83 0.1U/50V_6
PC85 330U/6.3V_7343
PR115 *0/short_4
PR120 *0/J_4
PR121 *0/J_4
PR130 *0/J_4 REF
PR134 *0/short_4
PC150
PC154
PC149
10U/25V_1206
0.1U/50V_6
330U/6.3V_7343
PR136 *100K/F_4
PR138 *0/short_4
HWPG_SYS <25>
<25,31,34> S5_ON
PR139 1M/J_6
PR143 22/J_8
PR141 1M/J_6
PR146 1M/J_6
PQ24 DTC144EU
PQ23 DMN601K-7
PQ29 DMN601K-7
PC92 1000P/50V_4
S5D
PQ21 AO3404
+3V_S5
MAIND
PQ47 AON7410
PQ20 AON7410
+5V
+3V
SUSD
PQ22 AO3404
+3VSUS
Quanta Computer Inc.
PROJECT : ZH9
Size
Document Number
SYSTEM 5V/3V (RT8206B)
Rev 4A
Date: Sunday, March 28, 2010
Sheet 27 of 40


Parallel
PU9
OZ8380
Close to Phase Inductor
OCP: 20A
12A
Close to Phase Inductor
OCP: 3A
1.5A
Quanta Computer Inc.
PROJECT : ZH9
AMD CPU Core (OZ8380)
Size
Document Number
Rev
4A
Date: Sunday, March 28, 2010
Sheet 28 of 40



[PWM]

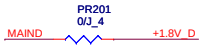


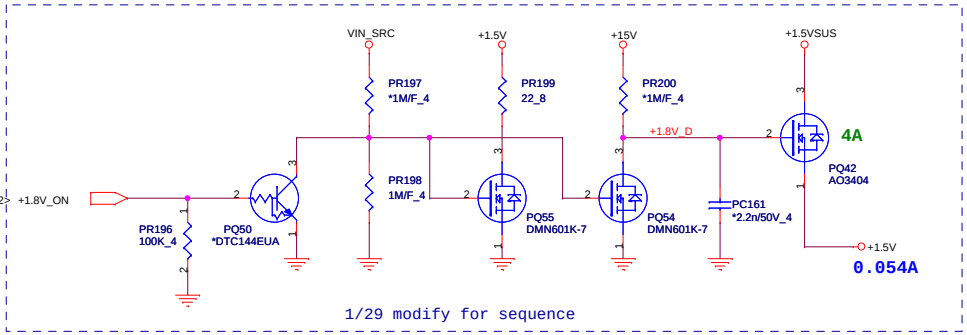
VOUT=(1+R1/R2)*0.75

Rdson=13mOhm

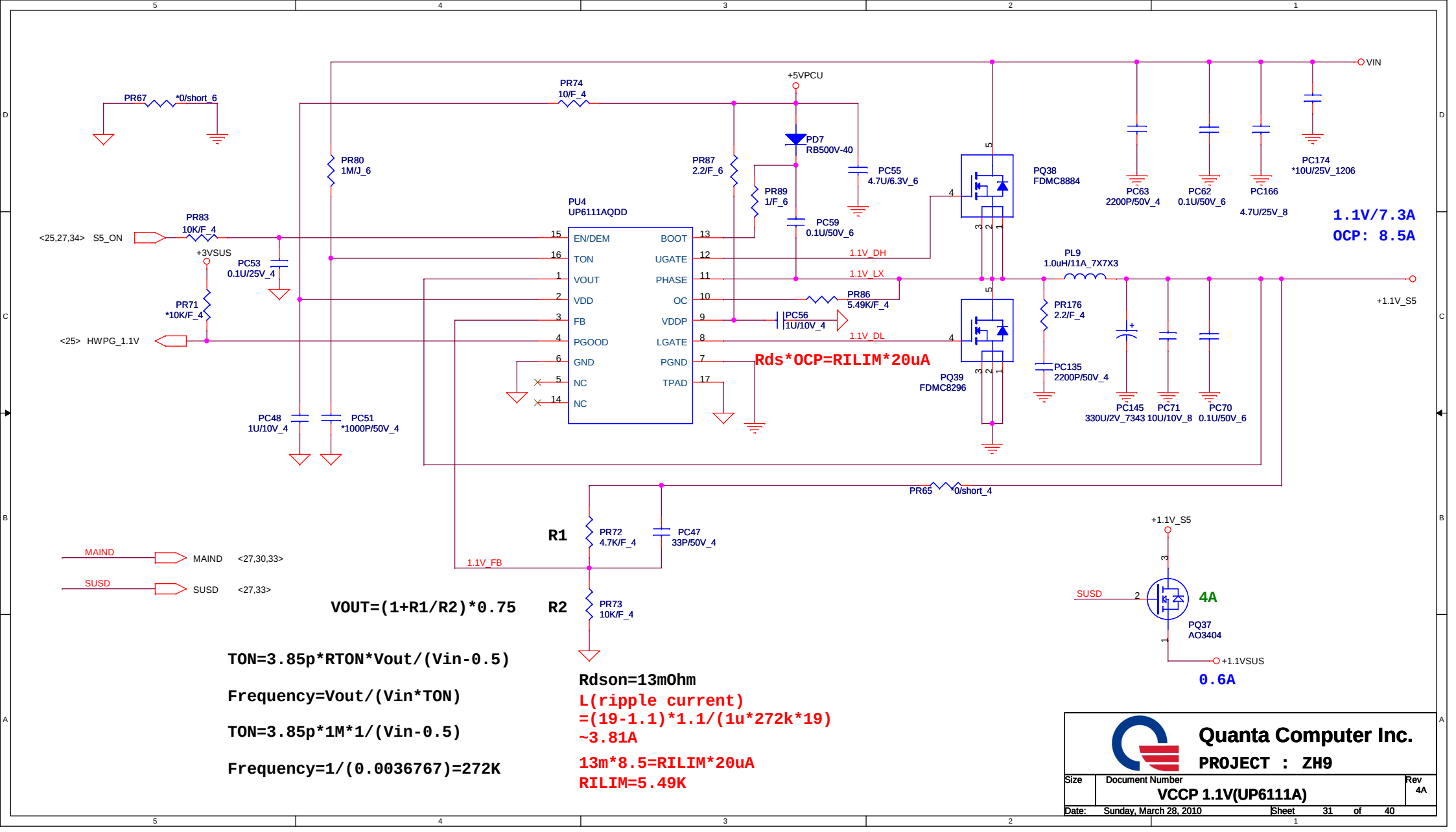
L(ripple current)
=(19-1.8)*1.8/(2.2u*400k*19)
~1.03A

13m*7=RILIM*10uA
RILIM=9.1K
(10u*PR35)/Rdson+Delta_I/2=Iocp

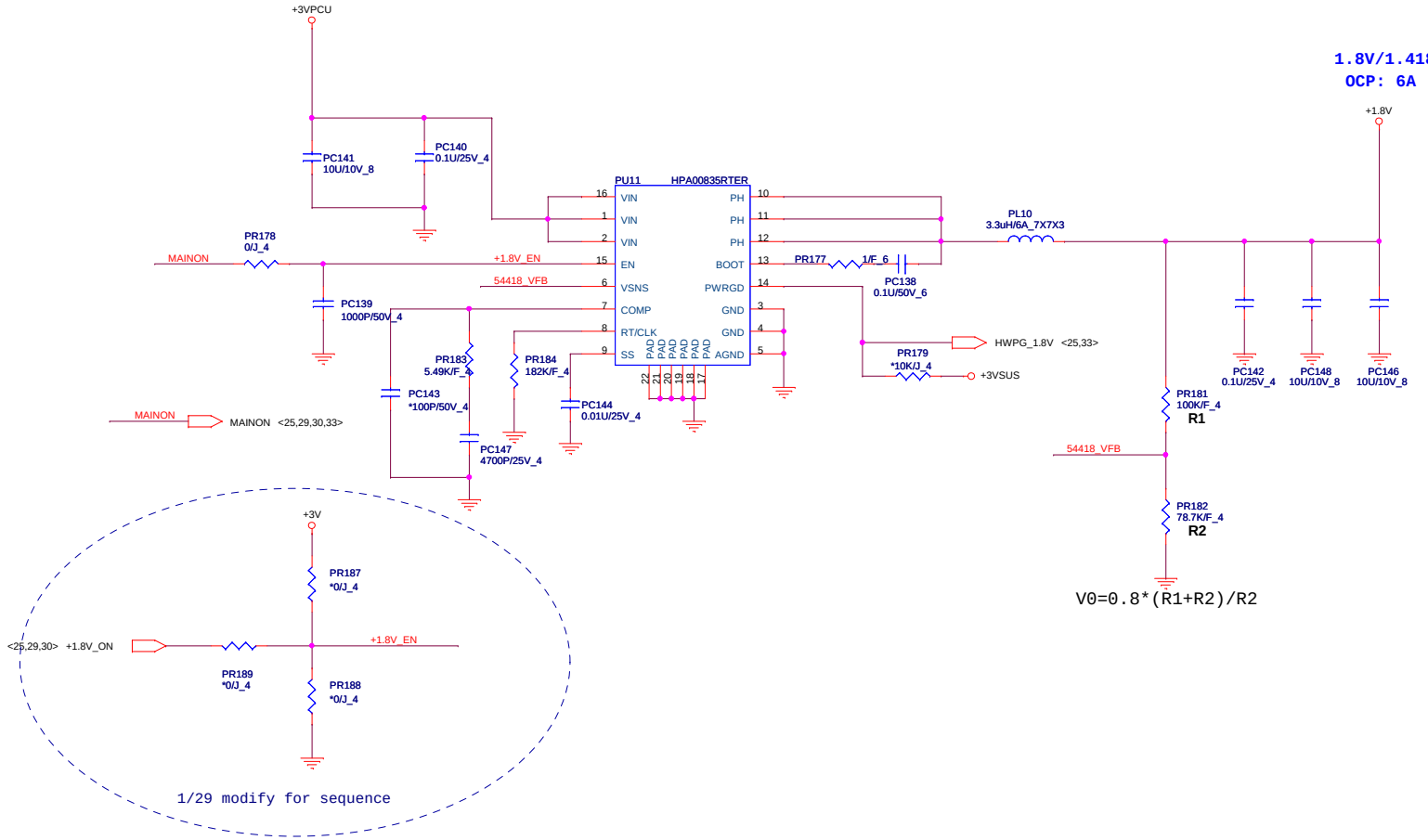




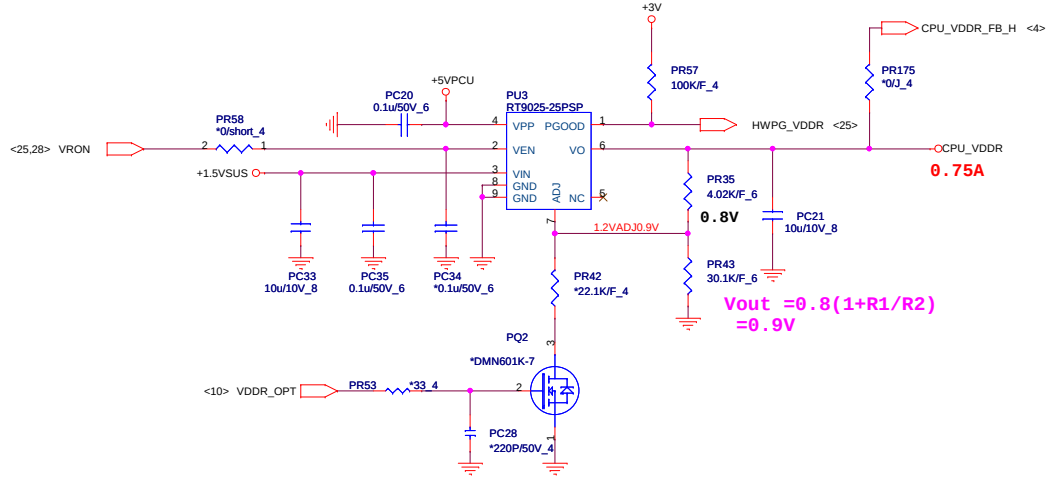
Quanta Computer Inc.		
PROJECT : ZH9		
Size	Document Number: DDR 1.5V(RT8207A)	Rev: 4A
Date: Sunday, March 28, 2010	Sheet 30 of 40	

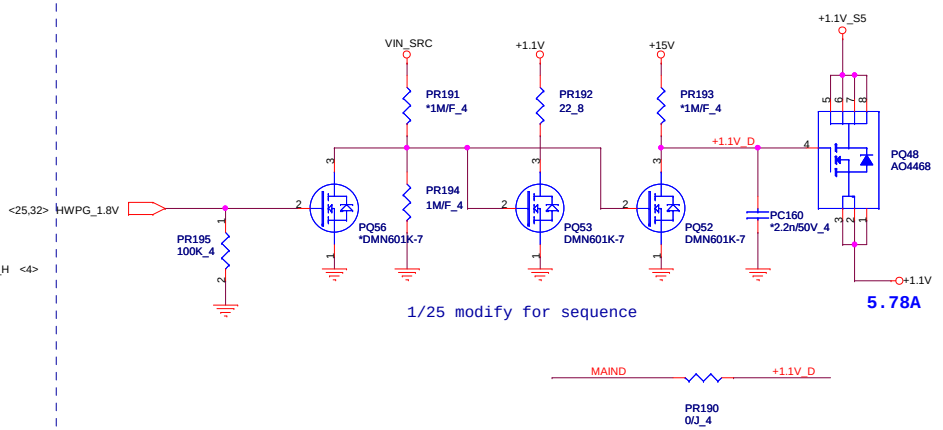


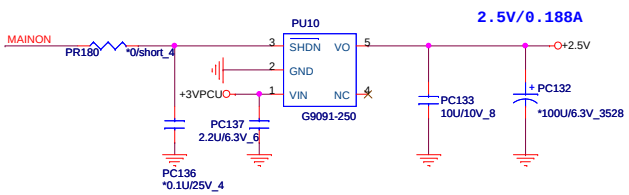
Quanta Computer Inc.		
PROJECT : ZH9		
Size	Document Number: VCCP 1.1V(UP6111A)	Rev: 4A
Date: Sunday, March 28, 2010	Sheet 31 of 40	

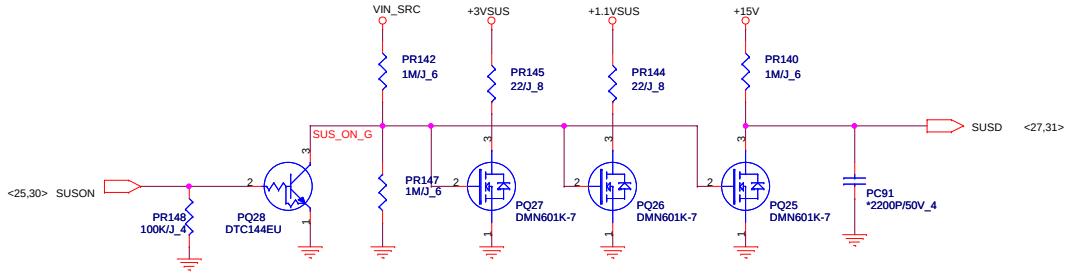


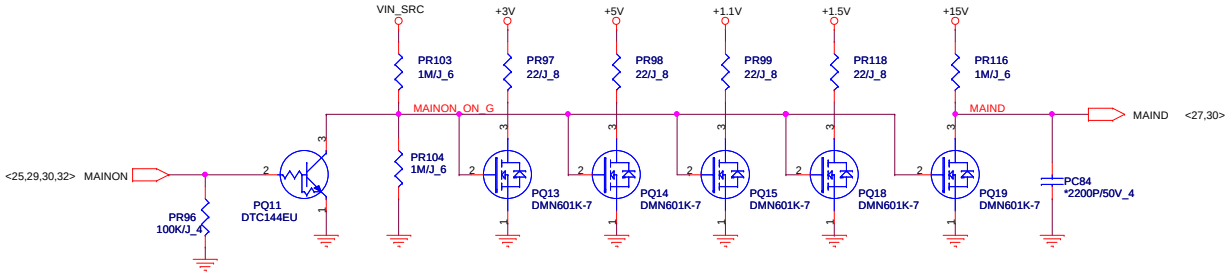
Quanta Computer Inc.		
PROJECT : ZH9		
Size	Document Number: +1.8V(TPS54418)	Rev: 4A
Date: Sunday, March 28, 2010	Sheet 32 of 40	







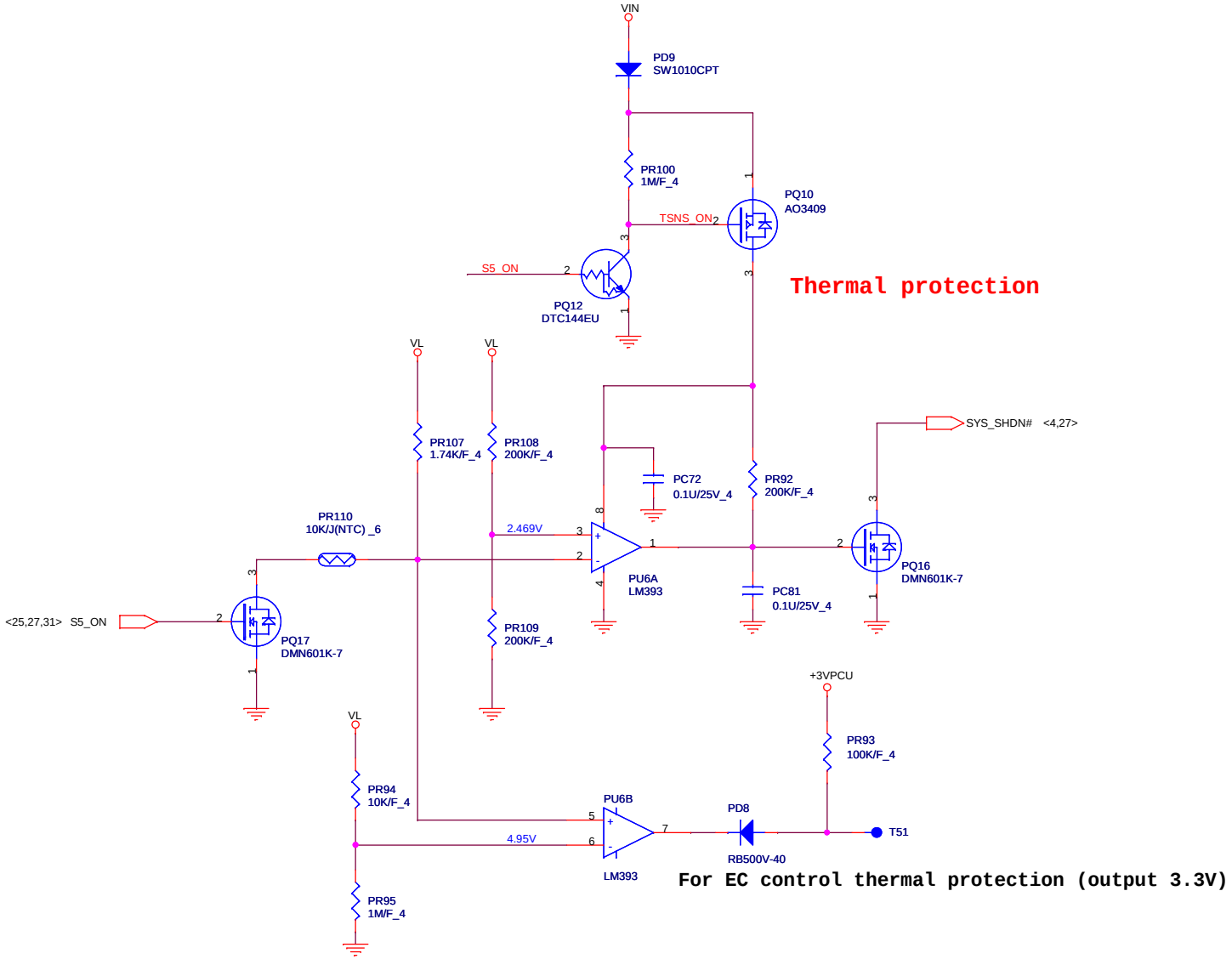




Quanta Computer Inc.

PROJECT : ZH9

Size	Document Number	Rev
	Discharge (2.5V/1.2V/VDDR)	4A
Date: Sunday, March 28, 2010	Sheet 33 of 40	

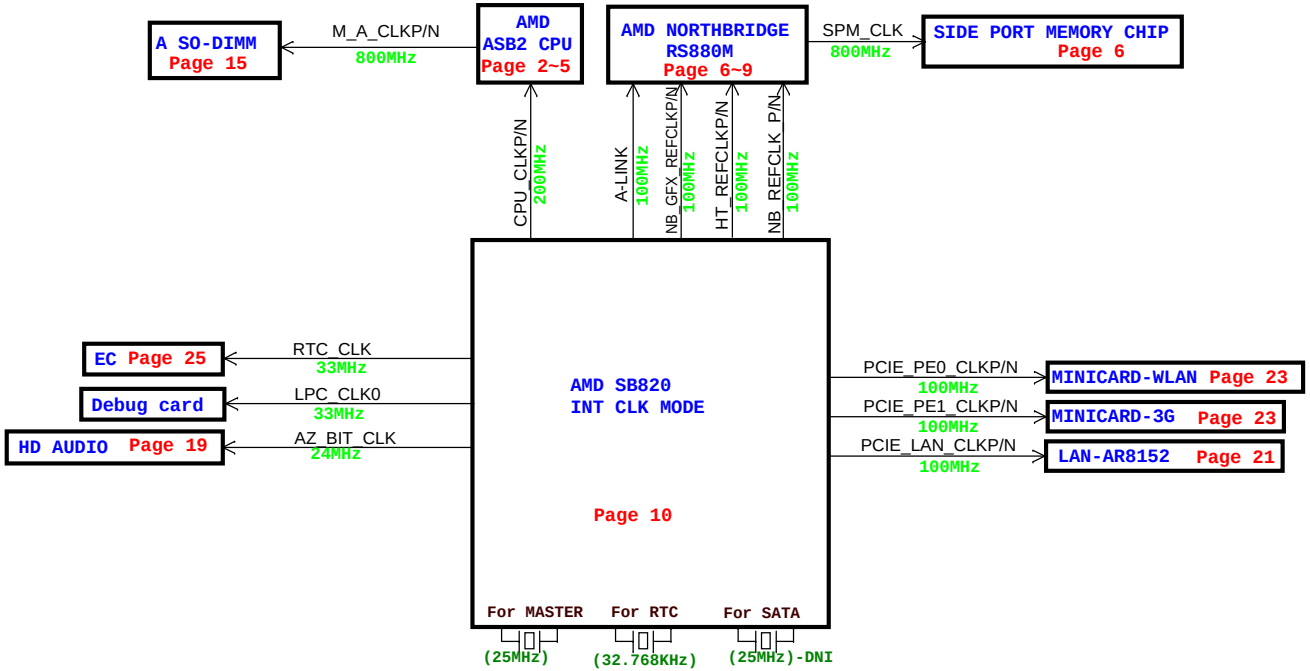


Quanta Computer Inc.

PROJECT : ZH9

Size	Document Number	Rev
	Thermal protect	4A
Date: Sunday, March 28, 2010	Sheet 34 of 40	

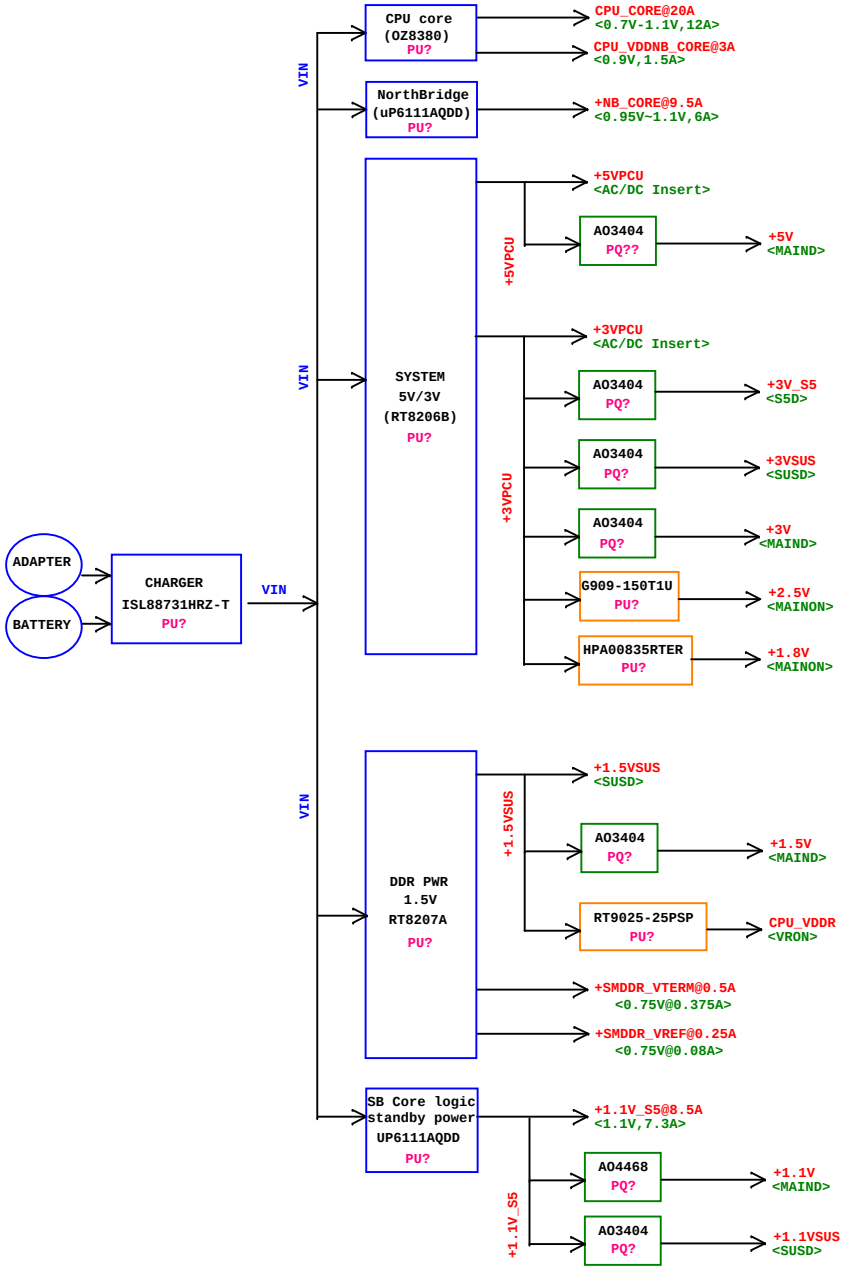
INTERNAL CLOCK MODE



Quanta Computer Inc.

PROJECT : ZH9

Size	Document Number	Rev
	Clock Distribution Diagram	4A
Date: Sunday, March 28, 2010	Sheet 35 of 40	



POWER	Distribution
VIN	LCD Backlight, CPU_CORE,NB_CORE, +5VPCU, +3VPCU, +1.5VSUS, +1.1V_S5
CPU_CORE	CPU
CPU_VDDNB_CORE	power supply for on-die NorthBridge
NB_CORE	NorthBridge power supply
+5VPCU	USB Connecter
+5V	CRT,Touch Pad ,Audio codec,SATA
+1.8V	NB & SB power supply
+3VPCU	RTC, Hall Sensor, System LED, EC, BIOS, Acer ID EEPROM, +3V_S5, +3VSUS, +3V
+3V_S5	SouthBridge,LAN , LAN EEPROM , RJ45 LED
+3VSUS	3G
+3V	CLK_GEN, CPU, NB,SB, LCD power switch,CCD, DMIC, BT, System LED, Codec, WLAN/Wimax, Card reader, EC
+2.5V	CPU,Discharge
+1.5VSUS	CPU,DDR,Discharge
+1.5V	CPU,DDR,NB
+SMDDR_VTERM	DDR
+SMDDR_VREF	CPU, DDR
+1.1V_S5	NorthBridge,Discharge
+1.1VSUS	Southbridge
+1.1V	CLK_GEN,CPU,NB,SB
CPU_VDDR	CPU

BOM Structure	
Fun.	Description
SPM@	w/ Sideport RAM
3G@	w/ 3G module
BT@	w/ BT module
HDM@	w/ HDMI
BOM@	BOM Control

BOM@		
Function		Description
CPU	CPU V105	U16: AJ00105VT00
	CPU K125	U16: AJ0K125VT02
	CPU K325	U16: AJ0K325VT02
	CPU K625	U16: AJ0K625VT03
w/ Sideport	w/ Sideport	L45,L46: Stuff(CX8PG221003) R142: Non-stuff C214: Stuff(CH4102K1B03) C416: Stuff(CH5102K9B06) Check U7,R295,R296,R283,R284
	w/ SAM Sideport	U7: AKD5LGGT506 ; R295,R284: Stuff ; R296,R283: Non-stuff
	w/ Hynix Sideport	U7: AKD5LZGTW04 ; R295,R283: Stuff ; R296,R284: Non-stuff
	w/ ATI Sideport	U7: AKD5LGGT700 ; R296,R284: Stuff ; R295,R283: Non-stuff
w/o Sideport	w/o Sideport	L45,L46: CS00003J951(0ohm) R142: Stuff(CS23002JB13) C214,C416: CS00002JB38(0ohm) U7,R295,R296,R283,R284: Non-stuff

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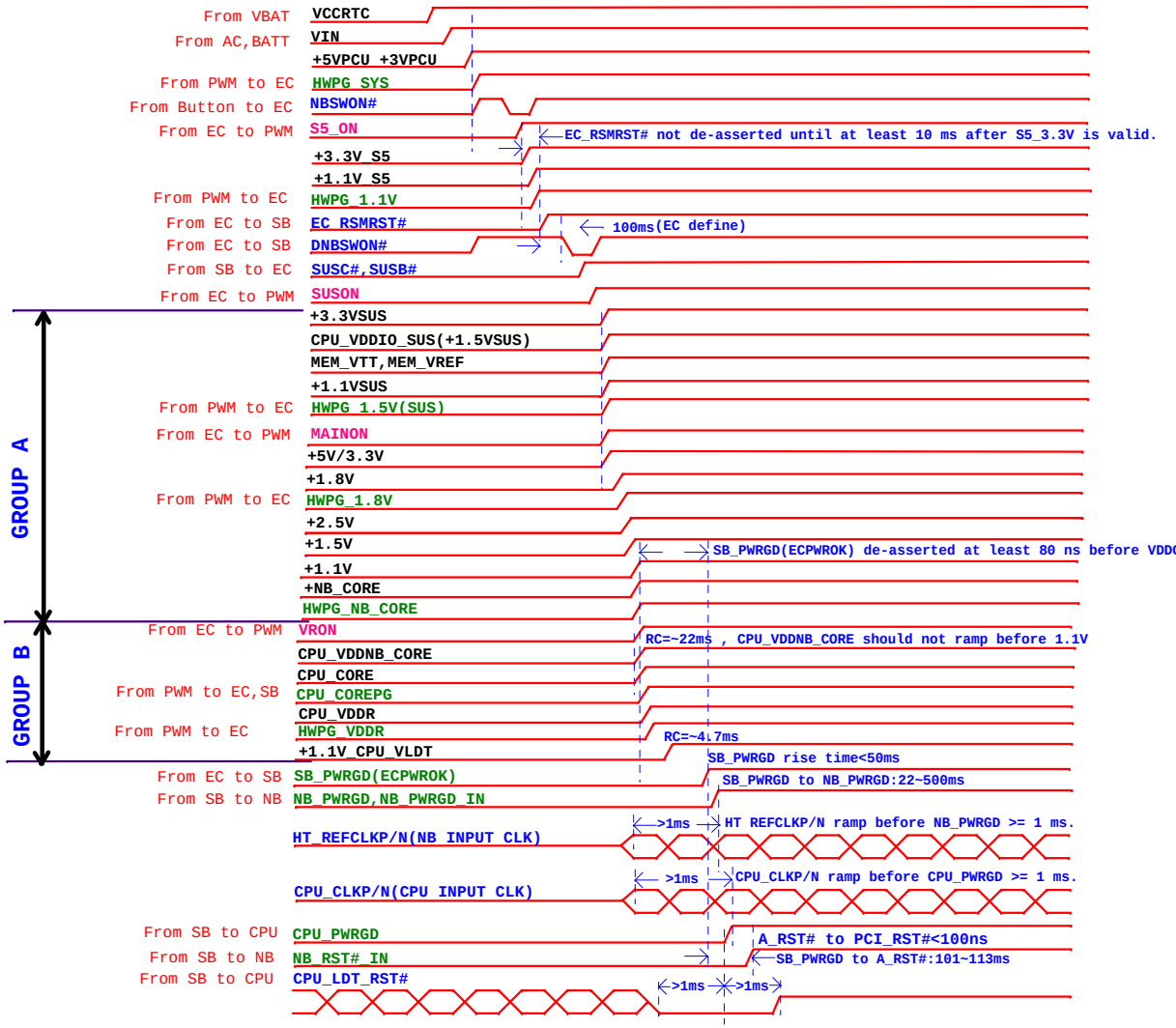
Nile Power On Sequence



Power on sequence required:

SB820:
1. EC_RSMRST# ramp up time (10% to 90%) <= 50 ms
2. SB_PWRGD(ECPWROK) rise time <= 50 ms
3. SB_PWRGD(ECPWROK) fail time <= 1 ms
4. SB_PWRGD(ECPWROK) de-asserted at least 1 ns before EC_RSMRST# is asserted when entering G3 state.
5. VBAT will be valid at least 5 seconds before S5_3.3V and S5_1.1V are ramped up to allow start time for internal RTC.
6. 50us<=all power rails rise time except +3.3V_S5<=40ms
7. 100us<=+3.3V_S5 rise time<=40ms
8. +1.8V_S0 rails cannot ramp before the +3.3V_S0 rails.
9. +1.1V_S0 rails cannot ramp before the +1.8V_S0 rails.
10. +1.1V_S0 rails cannot ramp before the +3.3V_S0 rails.
11. +1.1V_S5 rails cannot ramp before the +3.3V_S5 rails.
12. +3V_S5 ramp down time > 300 µs.

RS880:
1. +1.1V valid before NB_PWRGD HIGH >= 1 ms
2. +1.8V_NB_IOPLLVDD18c(+1.8V) cannot ramp before the 3.3-V rails
3. +1.5V_SPM_VDDQ(+1.5V)cannot ramp before the 3.3-V rails
4. +1.8V_NB_VDDLTP18(+1.8V)cannot ramp before the 3.3-V rails
5. +1.8V_NB_PLLVDD18(1.8V)cannot ramp before the 3.3-V rails
6. 3.3-V rails cannot exceed the 1.8/1.5-V Sideport or 1.8-V Display and PLL rails by > 2.1 V.
7. IOPLLVDD/PLLVDD(+1.1V) cannot ramp up before the 1.8/1.5-V Sideport or 1.8-V Display and PLL rails.
8. VDDC(+NB_CORE) rail cannot ramp before the 1.1-V PLL rails.

Notice:
1. CPU_LDT_RST# msut be asserted a minimum of 1ms prior to the assertion of CPU_PWRGD
2. CPU_CLKP/N must be within specification a minimum of 1ms prior to the assertion of CPU_PWRGD
3. CPU_PWRGD remains deasserted at least 1ms after both CPU_CLKP/N and all voltages to the processor are within specification for operation
4. all NB power rails(1.8V/1.2V/1.1V) valid before NB_PWRGD at least 1ms
5. stable input clocks from CLKGEN(HT_REFCLKP/N) to NB before NB_PWRGD at least 1ms

SB SMBUS Table

	CLK GEN	RAM	Mini Card (WLAN)
(SB_DA0)/(SB_CL0) (+3V)	V	V	V
Power Plane	+3V	+3V	+3V
MOS CKT (Level shift)	X	X	X*

*Reserve: There is not SMBUS function in AVL

EC SMBUS Table

	Battery	CPU thermal Sensor
EC775 SDA1 / SCL1 (+3VPCU)	V	
EC775 SDA2 / SCL2 (+3V)		V
EC775 SDA3 / SCL3 ()		
Power Plane	+3VPCU	+3V
MOS CKT (Level shift)	X	X

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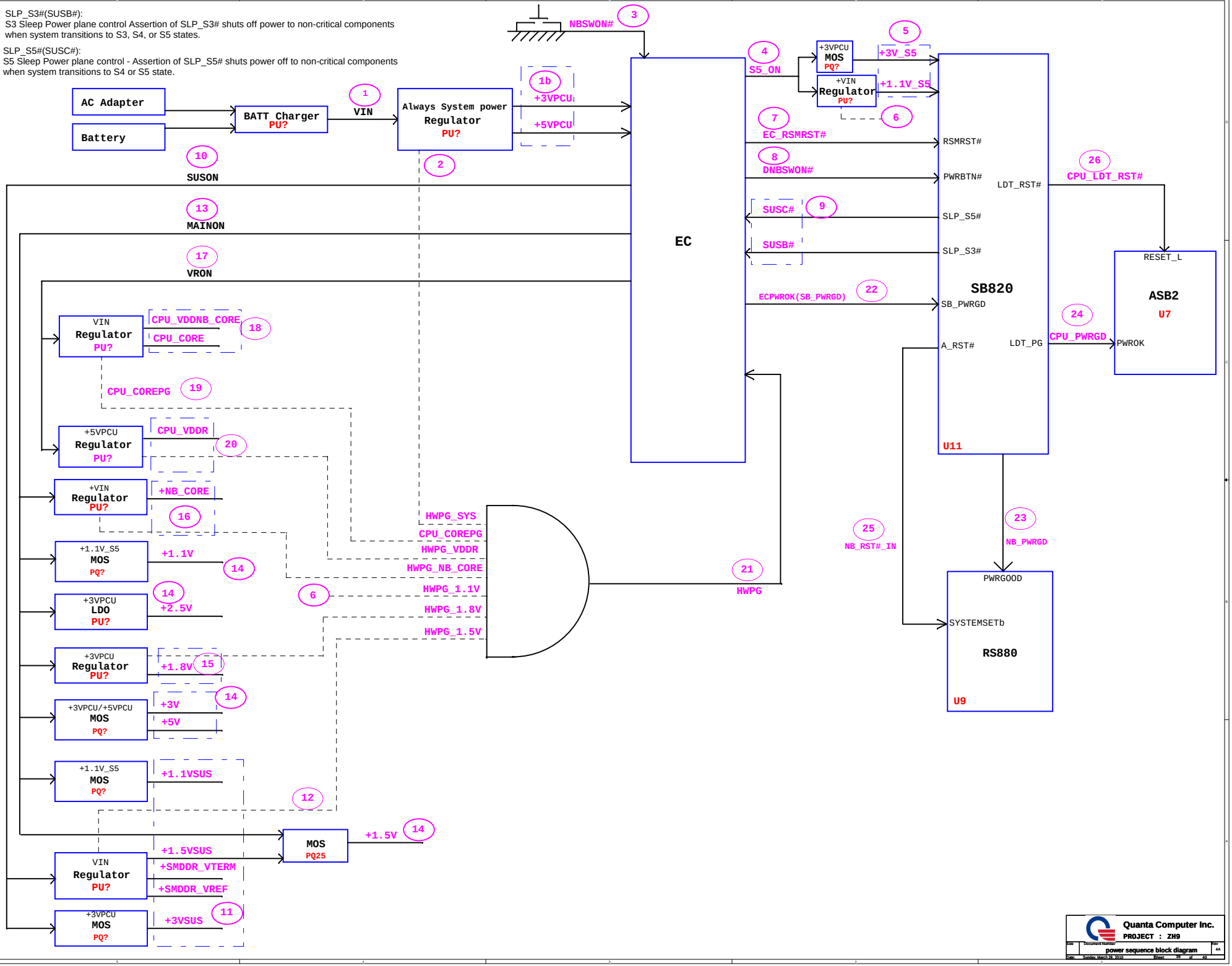
SLP_S3#(SUSB#):
S3 Sleep Power plane control Assertion of SLP_S3# shuts off power to non-critical components when system transitions to S3, S4, or S5 states.

SLP_S5#(SUSC#):
S5 Sleep Power plane control - Assertion of SLP_S5# shuts power off to non-critical components when system transitions to S4 or S5 state.



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