

# Compal Confidential

## PAV70 DDR3 Schematics Document

### Intel Pineview Processor with Tigerpoint + DDRIII

2010-06-25

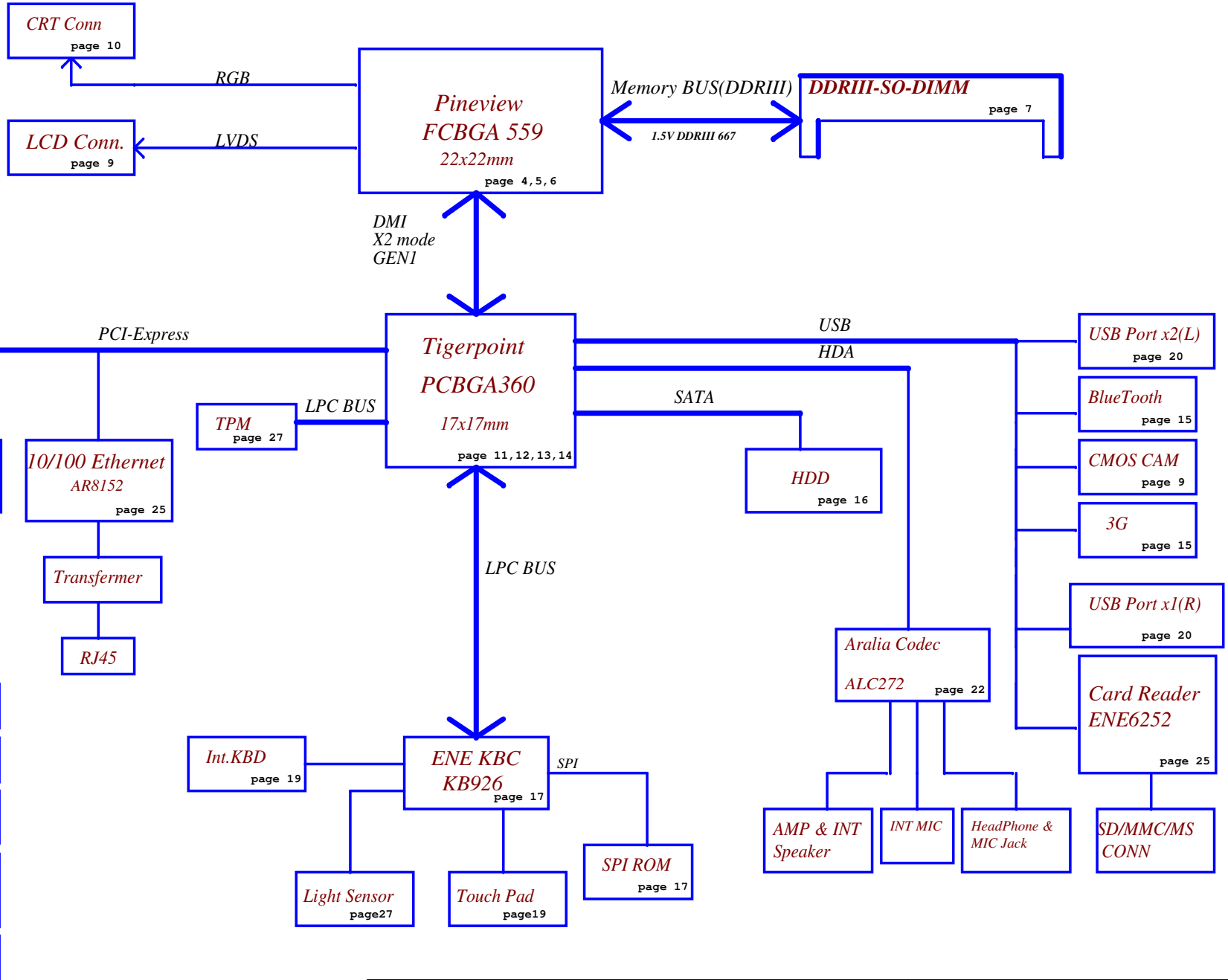
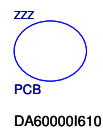
REV: 1.0

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Model Name : PAV50  
File Name : LA-6421P

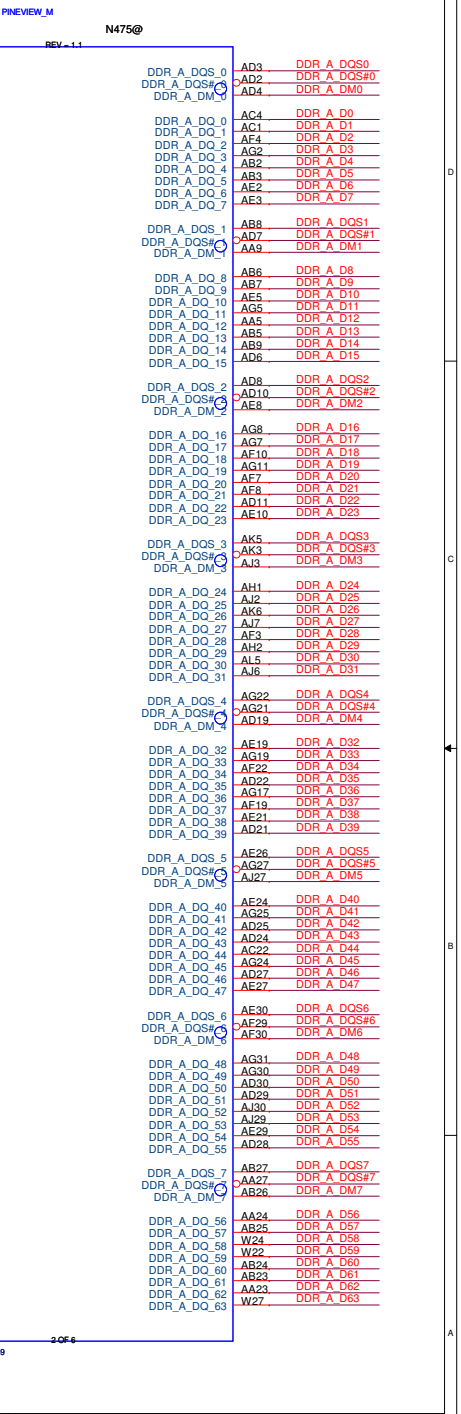
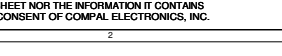
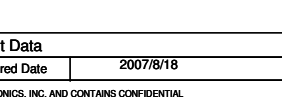
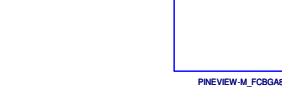
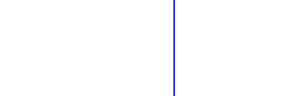
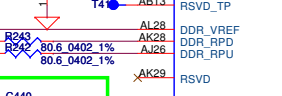
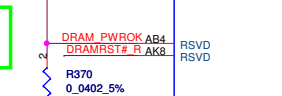
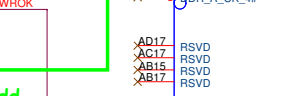
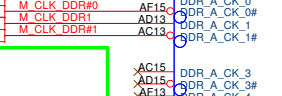
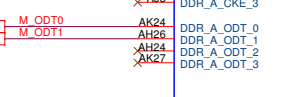
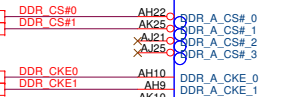
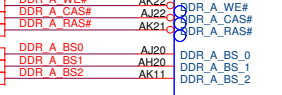
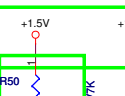
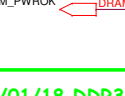
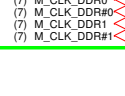
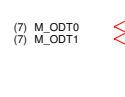
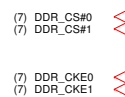
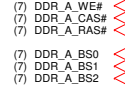
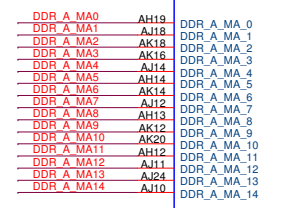
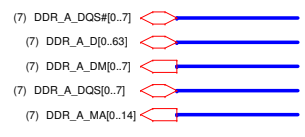
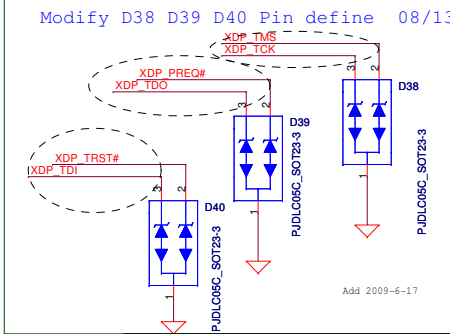
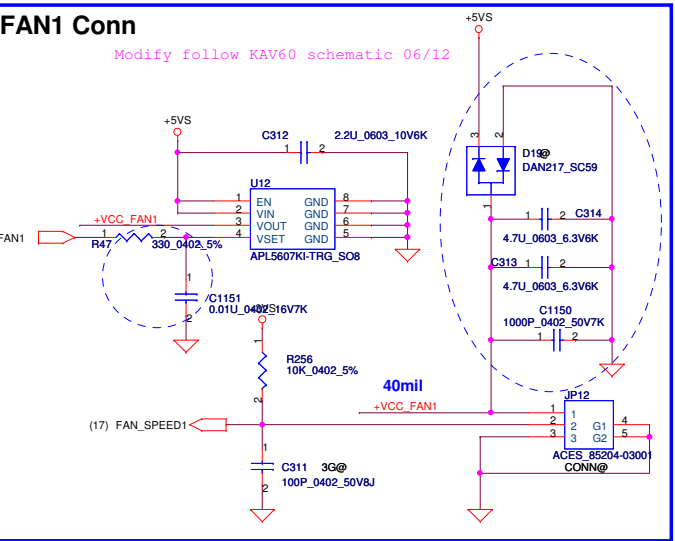
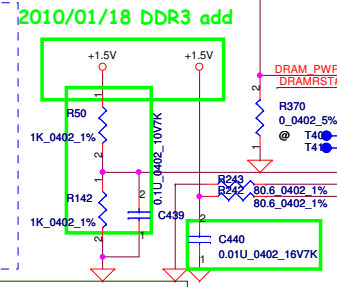
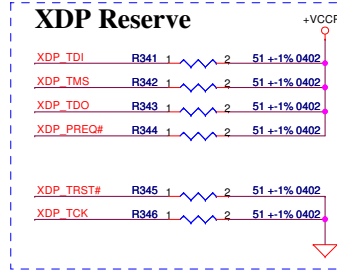
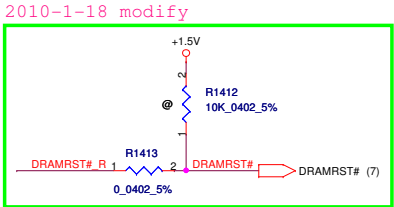
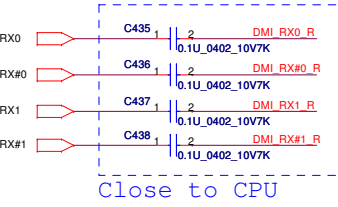
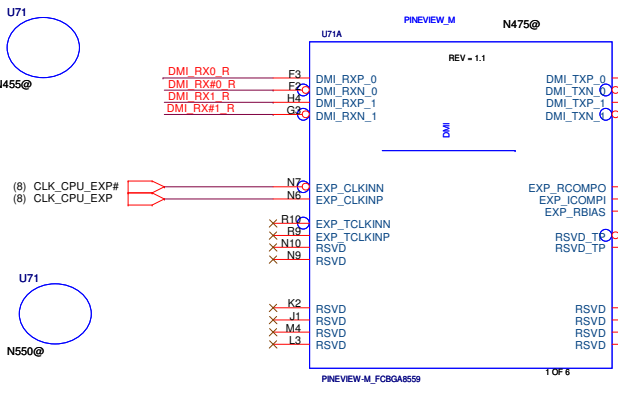
Clock Generator  
CK505  
page 8



- Power ON/OFF** page 18
- DC IN** page 30
- BATT IN** page 31
- CHARGER** page 32
- DC/DC Interface** page 29
- 3VALW/5VALW** page 33
- 1.5VP/VCCP** page 34
- 0.89VP/1.8VP 0.75VS** page 35
- CPU\_CORE** page 36

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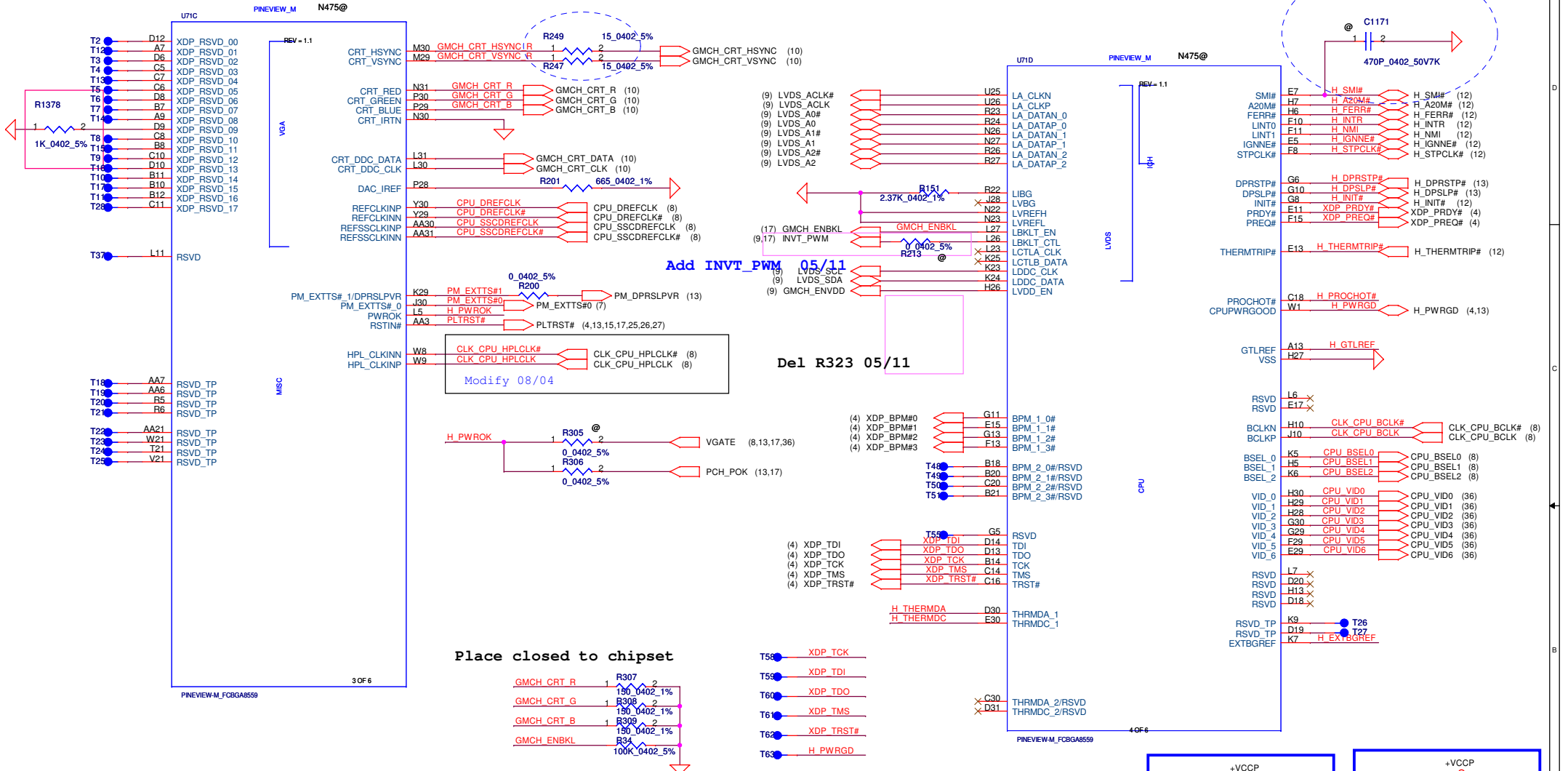


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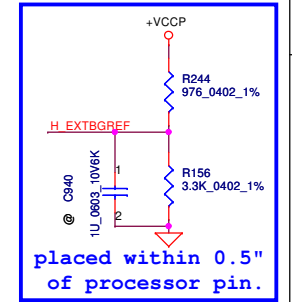
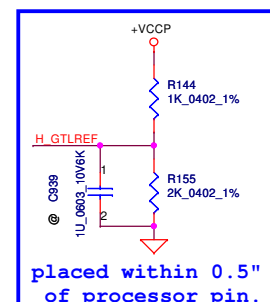
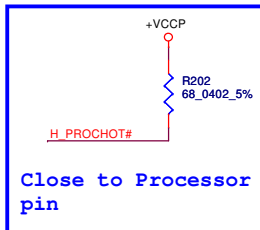
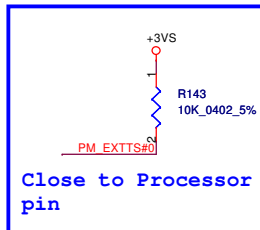
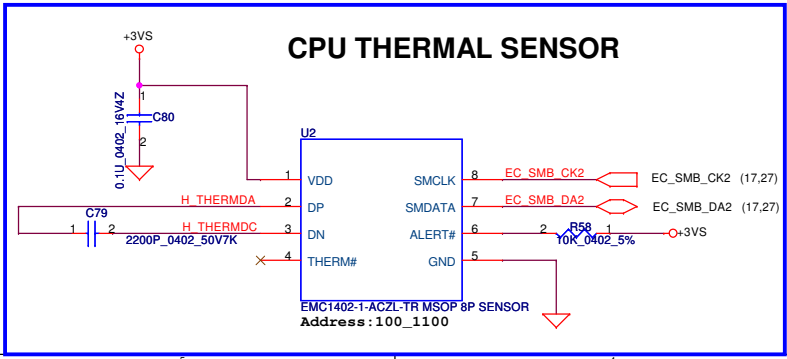
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Pineview(1/3)		
Title	Size	Rev
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Date: Monday, June 26, 2010	Sheet	4 of 39

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Add 470PF on H\_SMI# for known issda 07/08



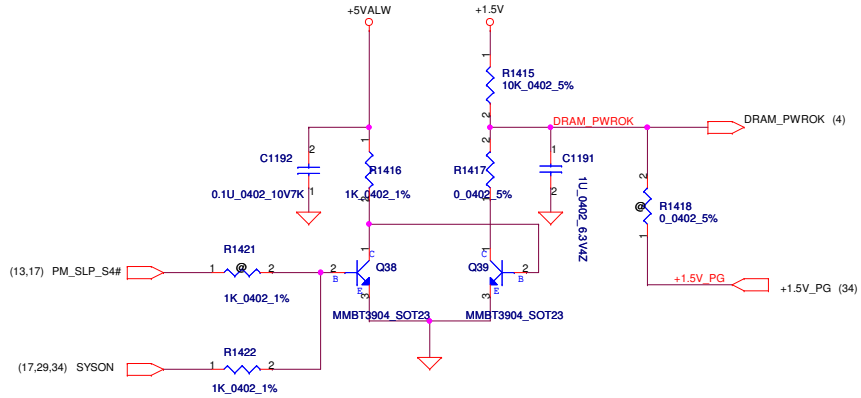
H\_THERMDA, H\_THERMDC routing together.  
Trace width / Spacing = 10 / 10 mil



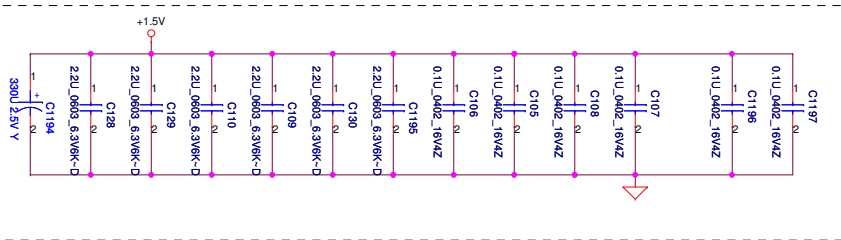
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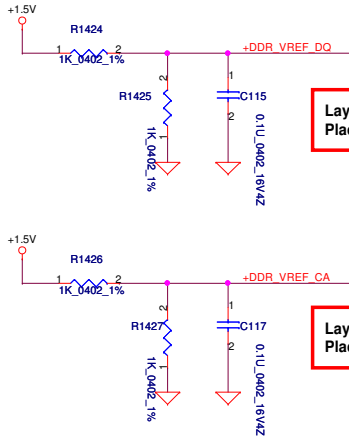
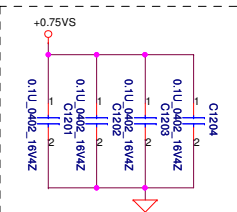
# 2010/01/18 DDR3 modify



**Layout Note:**  
Place near JDIMM1



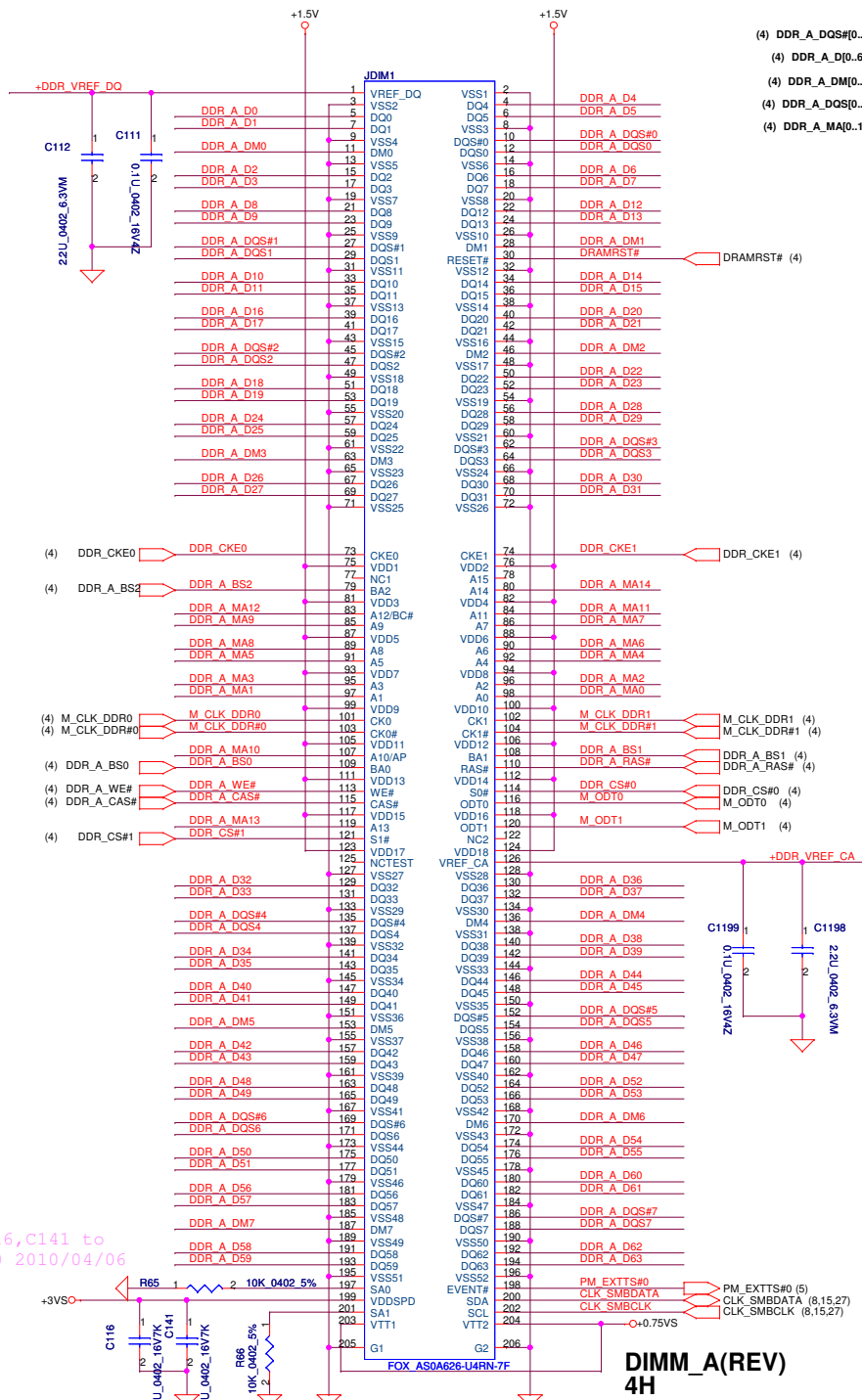
**Layout Note:**  
Place near JDIMM1.203 & JDIMM1.204



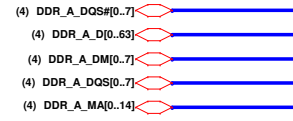
**Layout Note:**  
Place near JDIMM1.1

Change C116, C141 to SE076104K80 2010/04/06

**Layout Note:**  
Place near JDIMM1.126



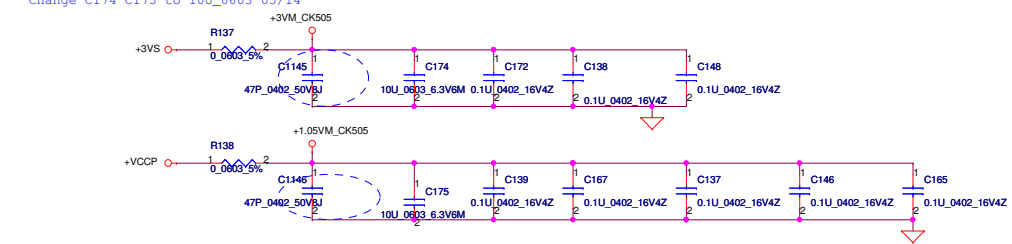
**DIMM\_A(REV) 4H**



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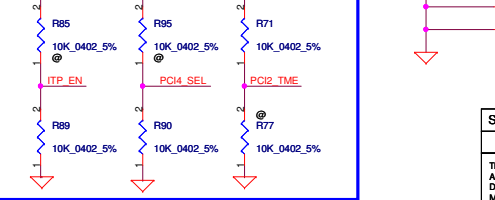
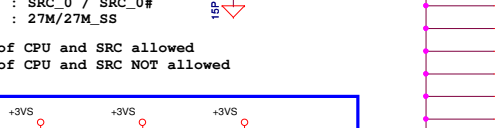
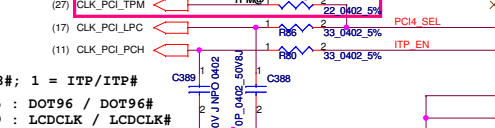
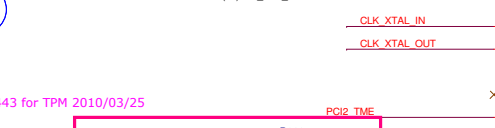
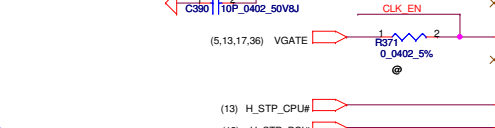
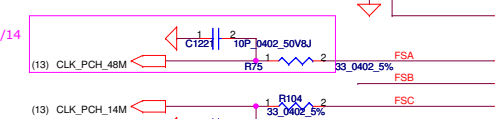
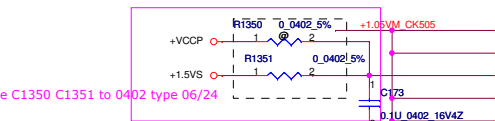
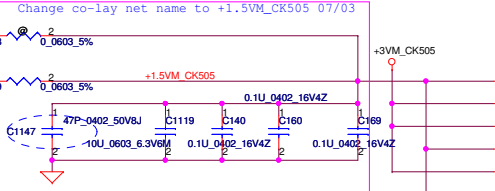
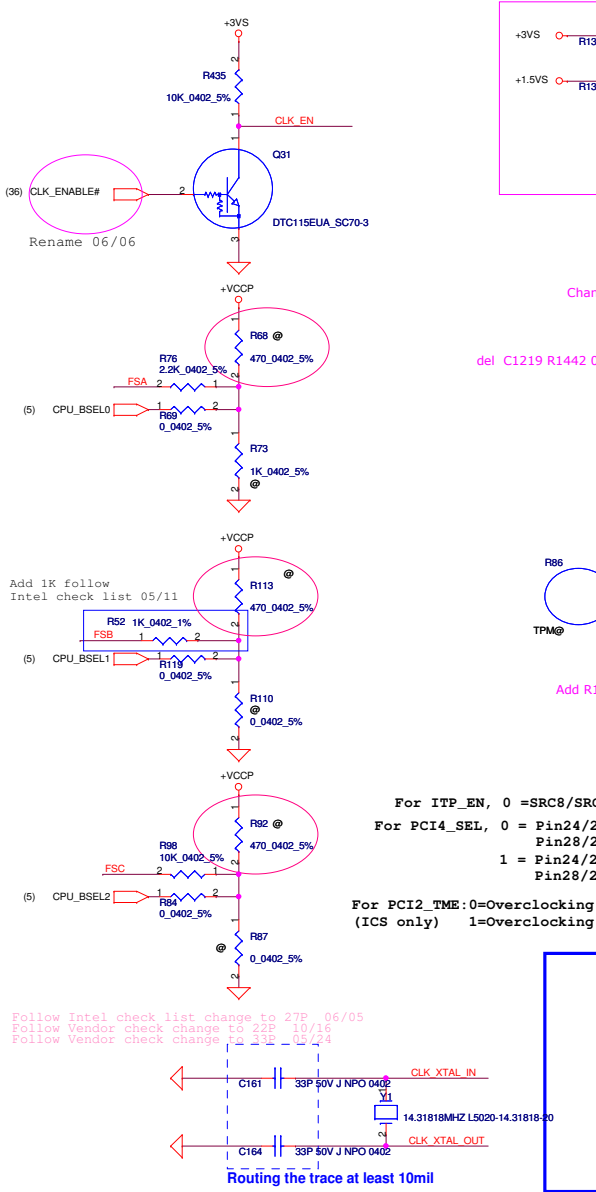
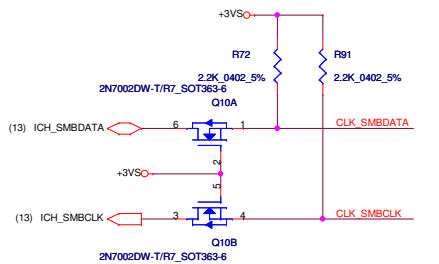
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0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								



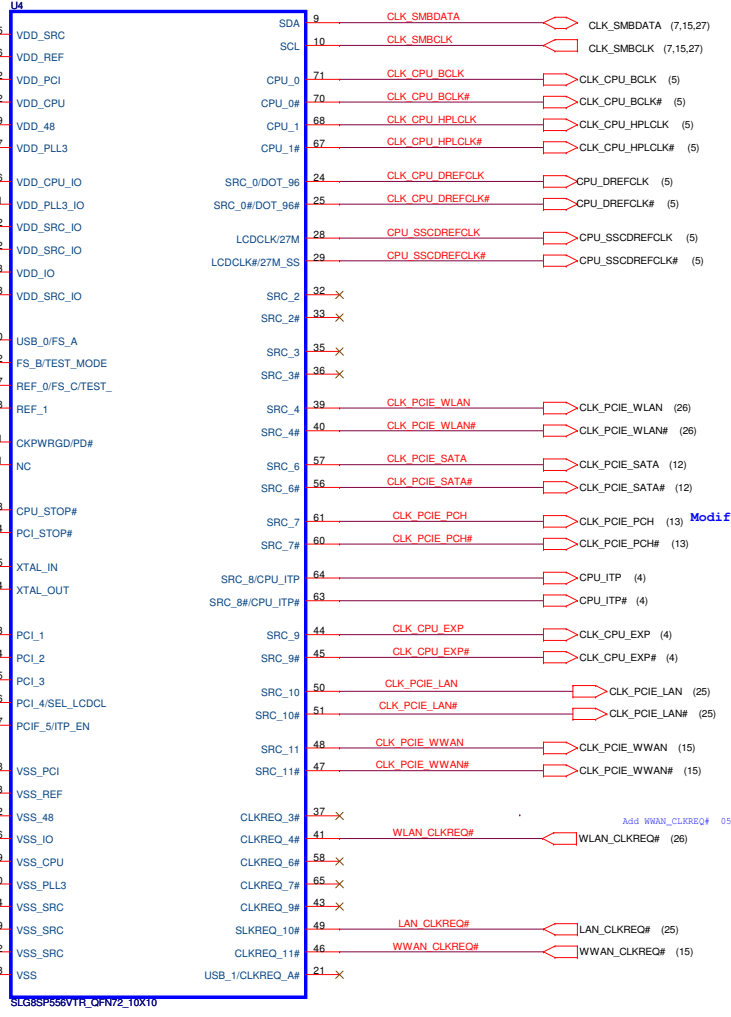
Add C1145 C1146 C1147 for EMI 06/12

IDT: SA00003H610

Change Q10 to SB00000DH00 2010/04/06



Realtek: SA00003H730



### SRC PORT LIST

PORT	DEVICE
SRC1	CPU_SSCDREFCLK
SRC2	
SRC3	
SRC4	PCIE_WLAN
SRC6	PCIE_SATA
SRC7	PCIE_PCH
SRC8	CPU_ITP
SRC9	CLK_CPU_EXP
SRC10	PCIE_LAN
SRC11	PCIE_WWAN

Modify CLK SRC Port list 05/12



### REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	PCIE_WLAN
REQ_6#	
REQ_7#	
REQ_9#	
REQ_10#	PCIE_WWAN
REQ_11#	
REQ_A#	

Follow Intel check list change to 27P\_06/05  
 Follow Vendor check change to 22P\_10/16  
 Follow Vendor check change to 33P\_05/24

Routing the trace at least 10mil

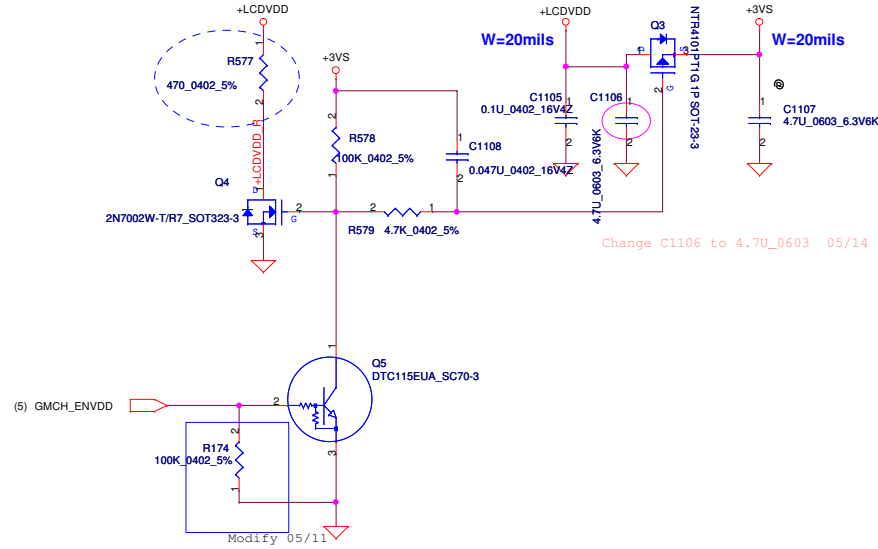
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Compal Electronics, Inc.			
Clock Generator CK505			
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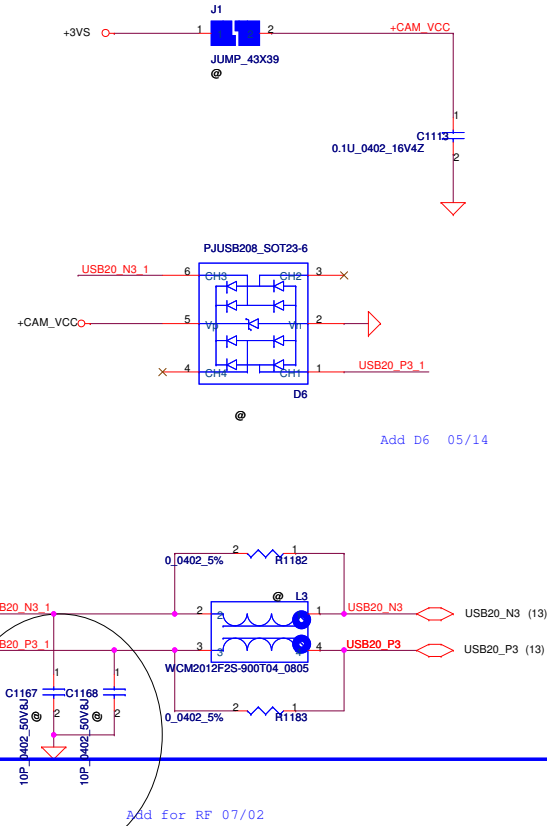
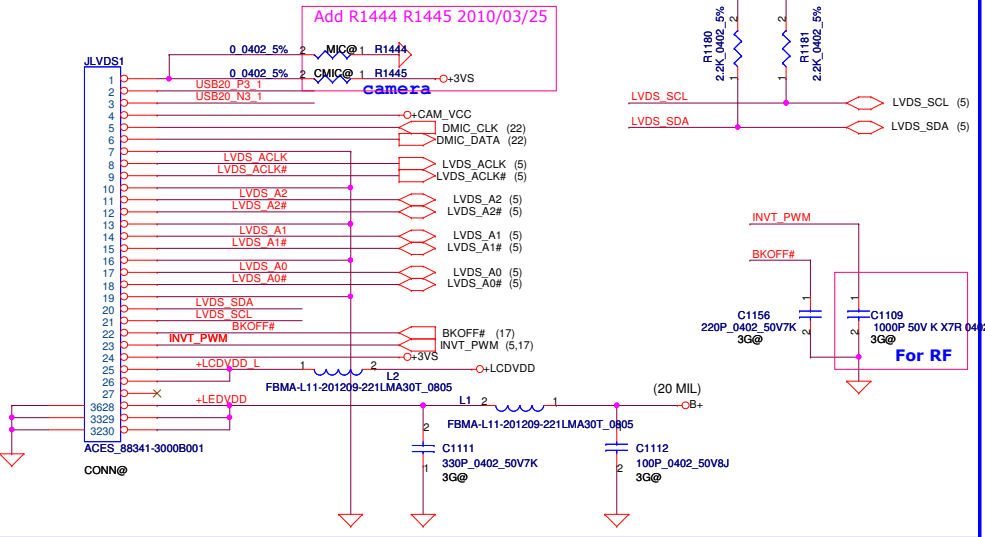
### LCD POWER CIRCUIT

Change R577 to 0402 SIZE 06/16

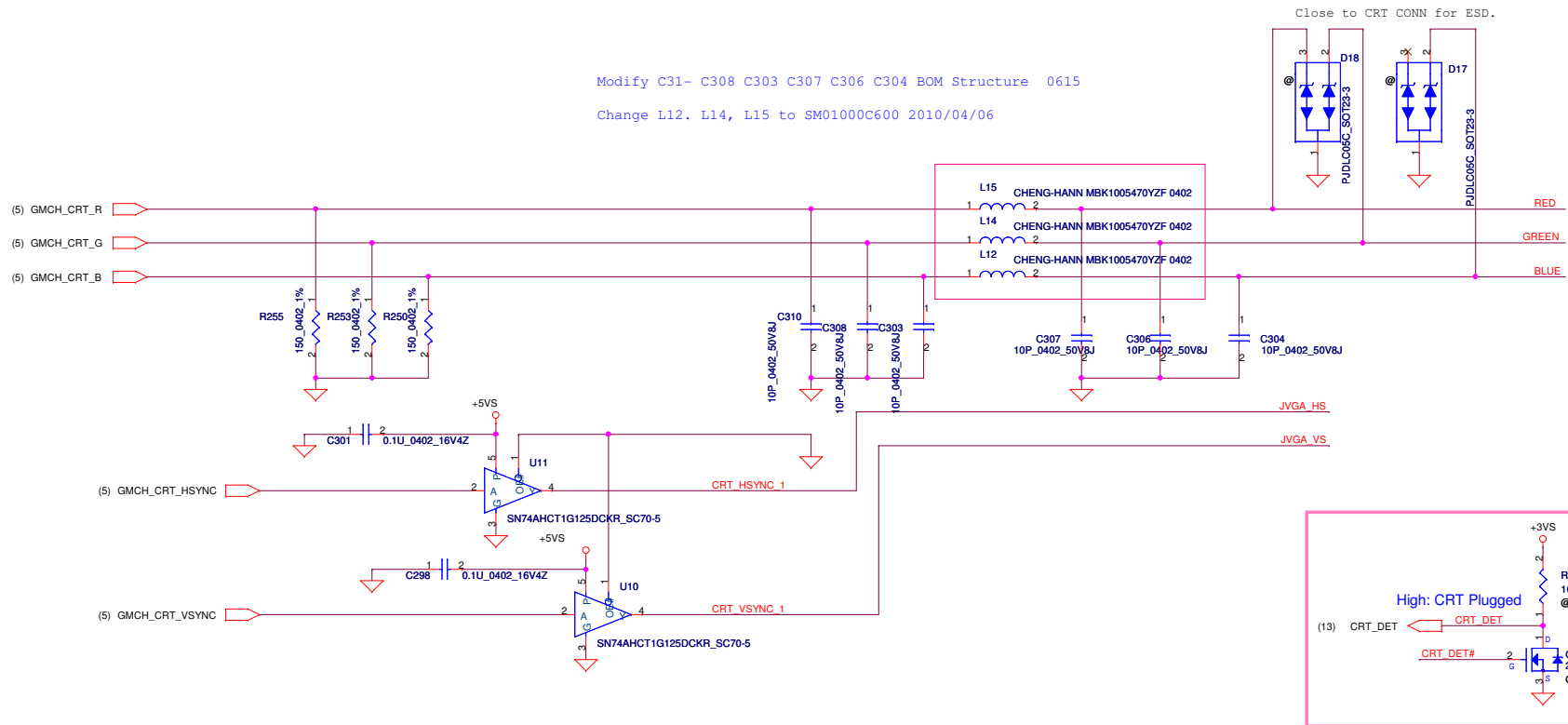


### CMOS & LCD/PANEL BD. Conn.

Modify JLVDS1 08/04

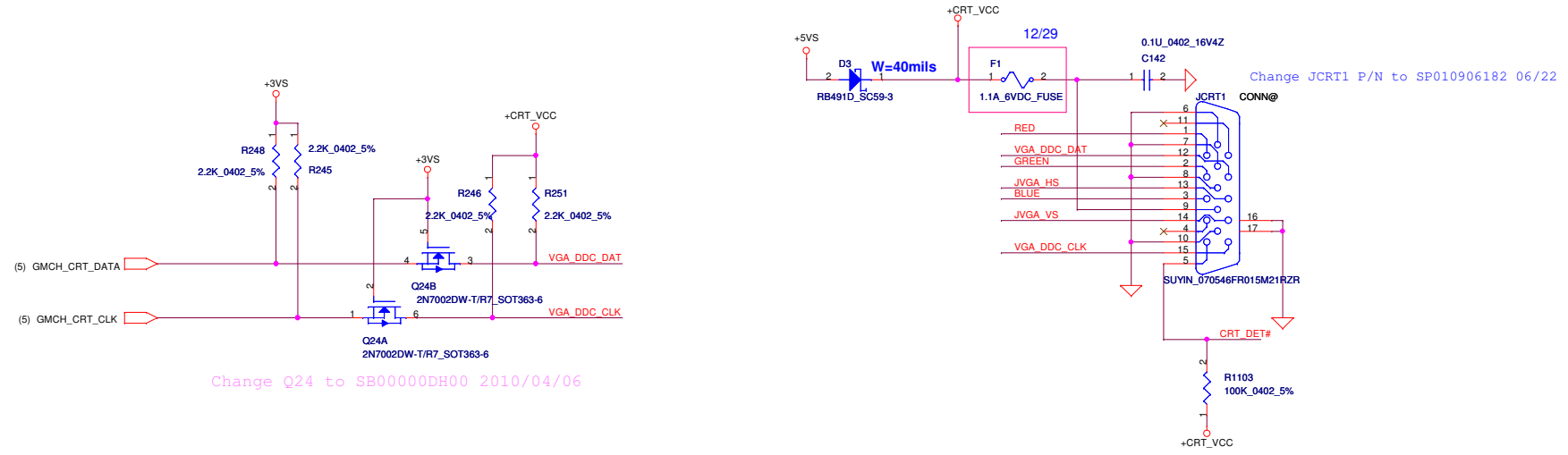


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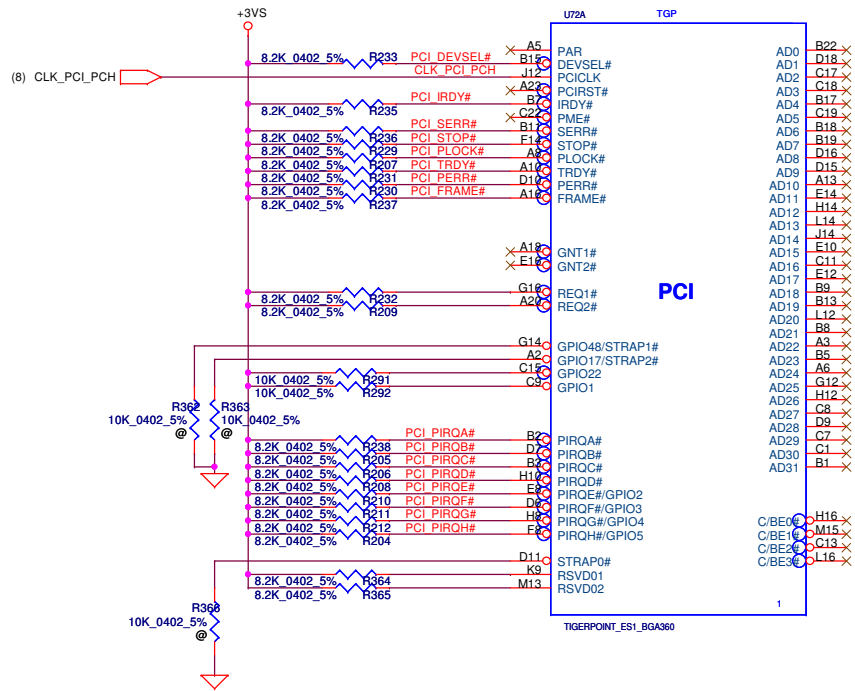
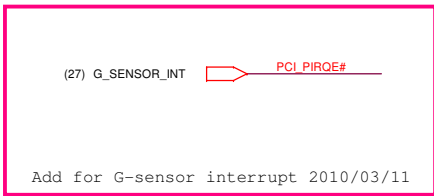
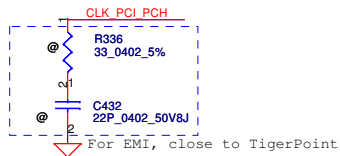


Modify C31- C308 C303 C307 C306 C304 BOM Structure 0615  
 Change L12, L14, L15 to SM01000C600 2010/04/06

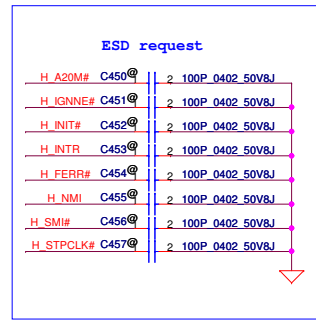
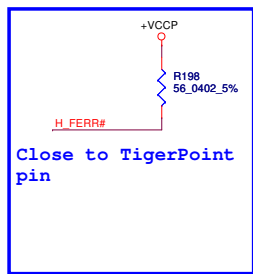
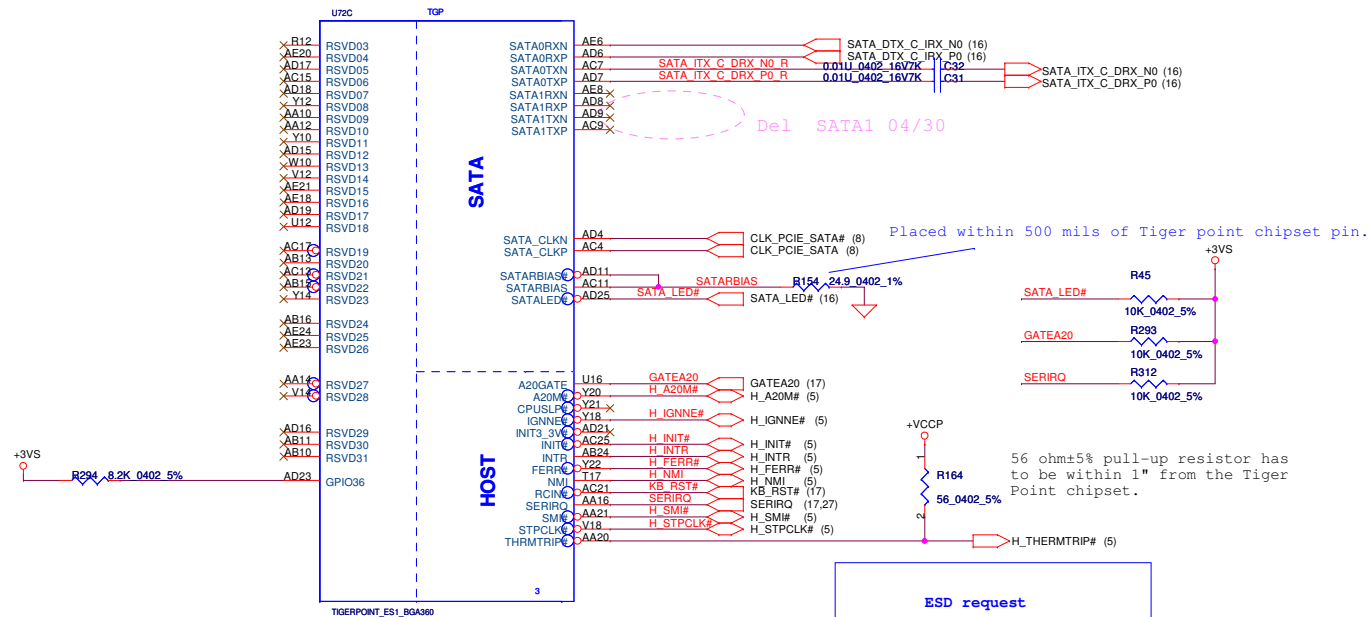
### CRT PORT



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				LA-6421P	
				Date:	Tuesday, June 22, 2010
				Sheet	10 of 39



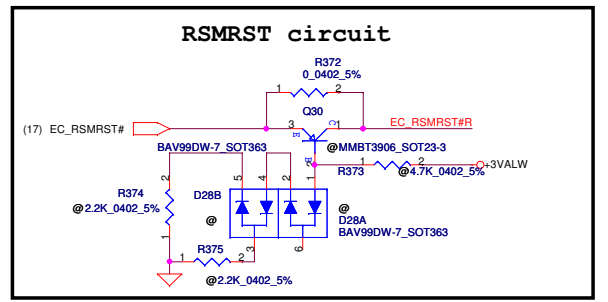
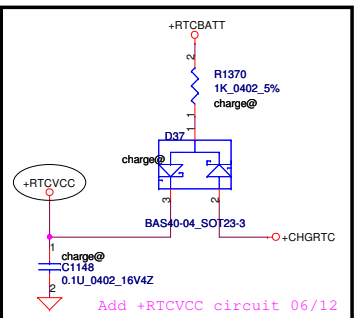
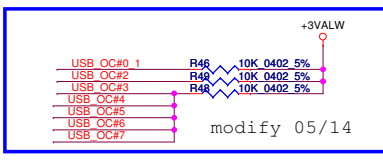
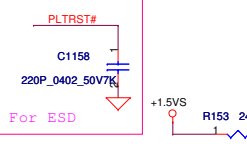
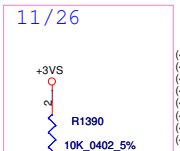
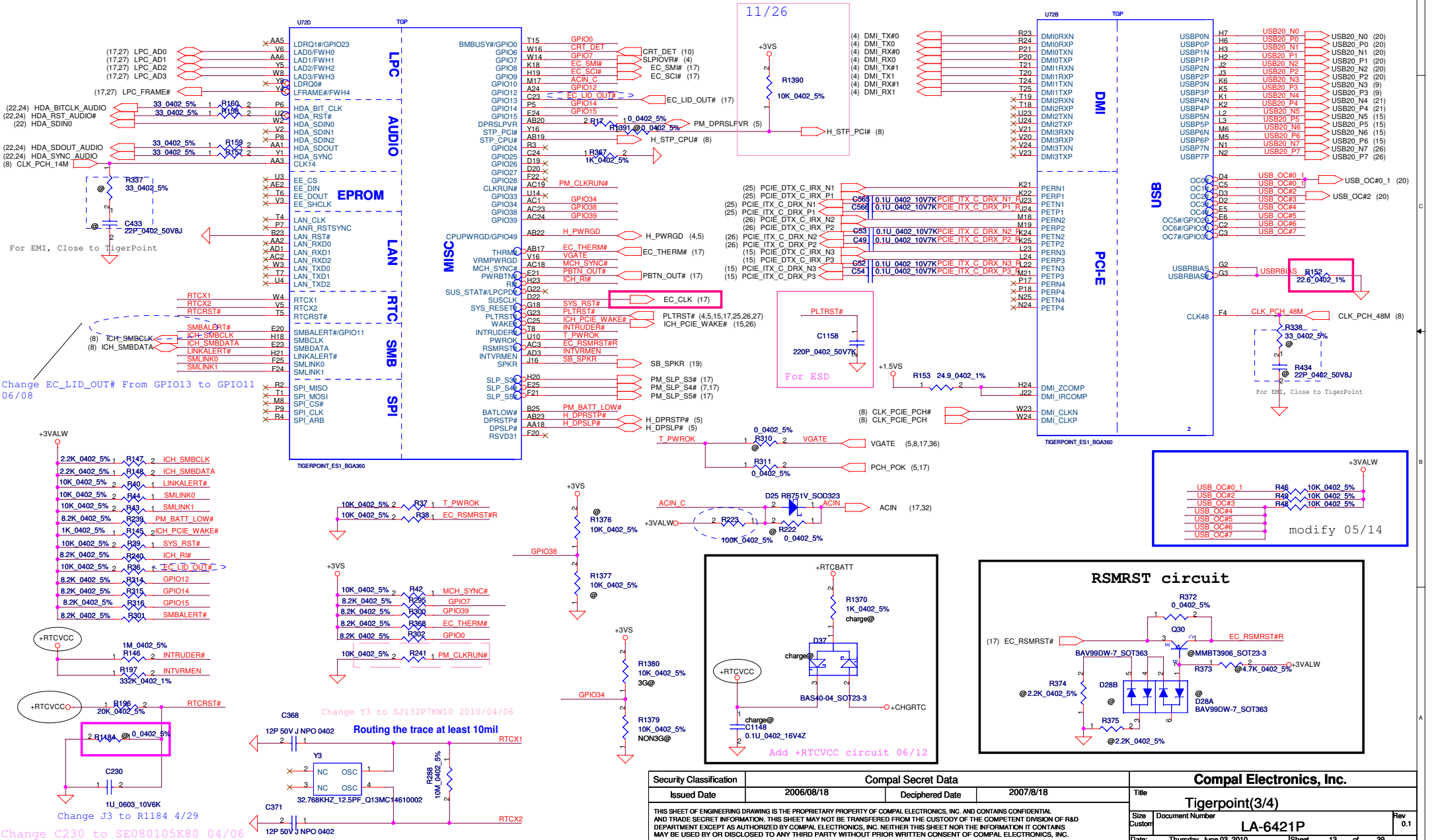
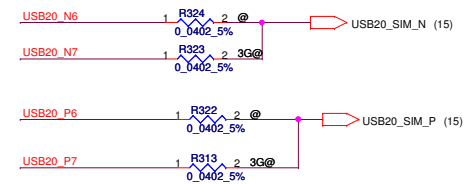
STRAP2# GPIO17	STRAP1# GPIO48	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC



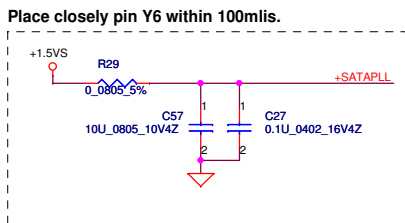
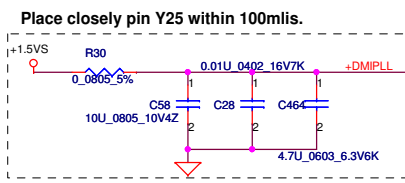
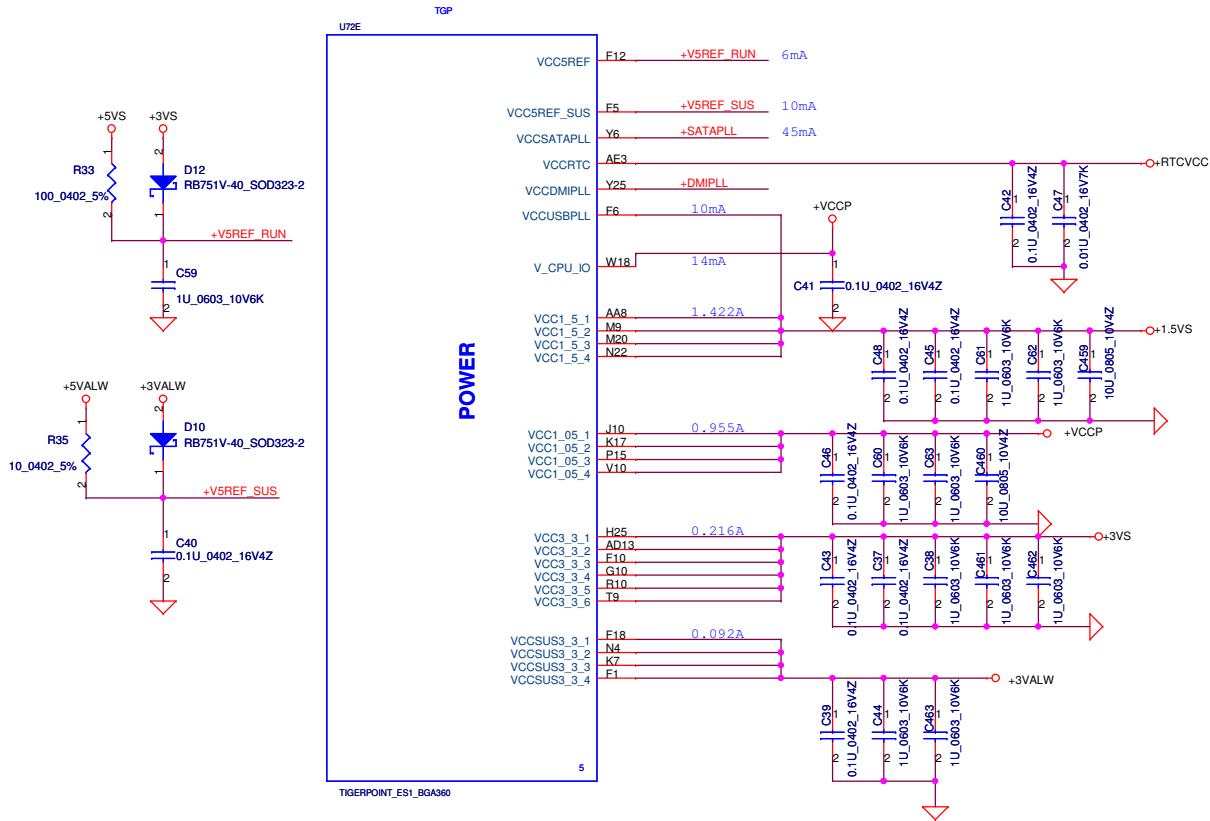
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title Tigerpoint(2/4)	
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Date: Thursday, June 03, 2010				Rev 0.1	Sheet 12 of 39

1	LAN
2	WLAN
3	WWAN
4	

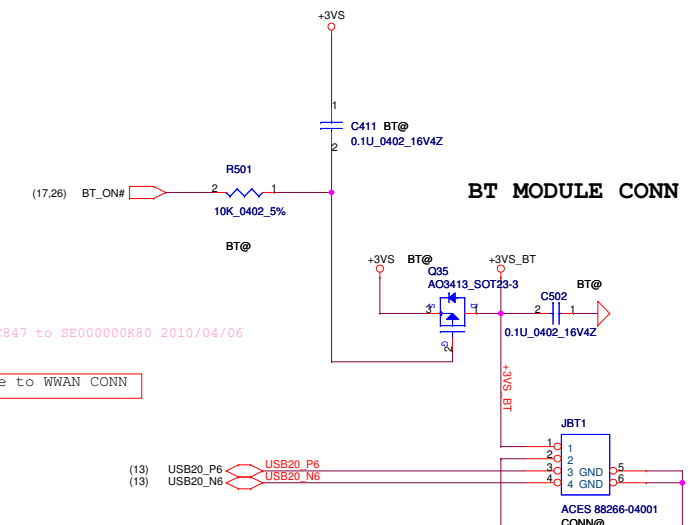
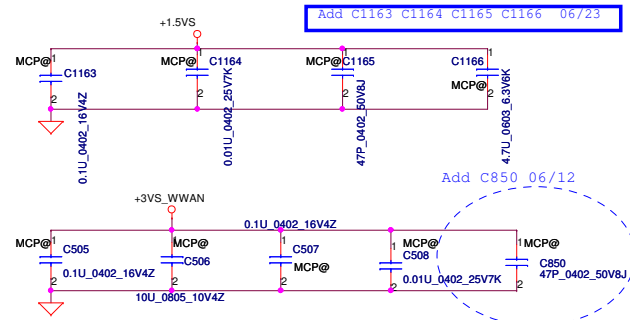
0	USB Left1
1	USB Left2
2	USB Right2
3	CMOS
4	CardReader
5	WWAN
6	BT
7	WIMAX



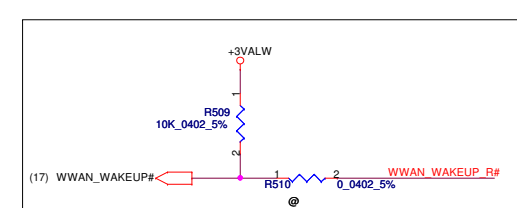
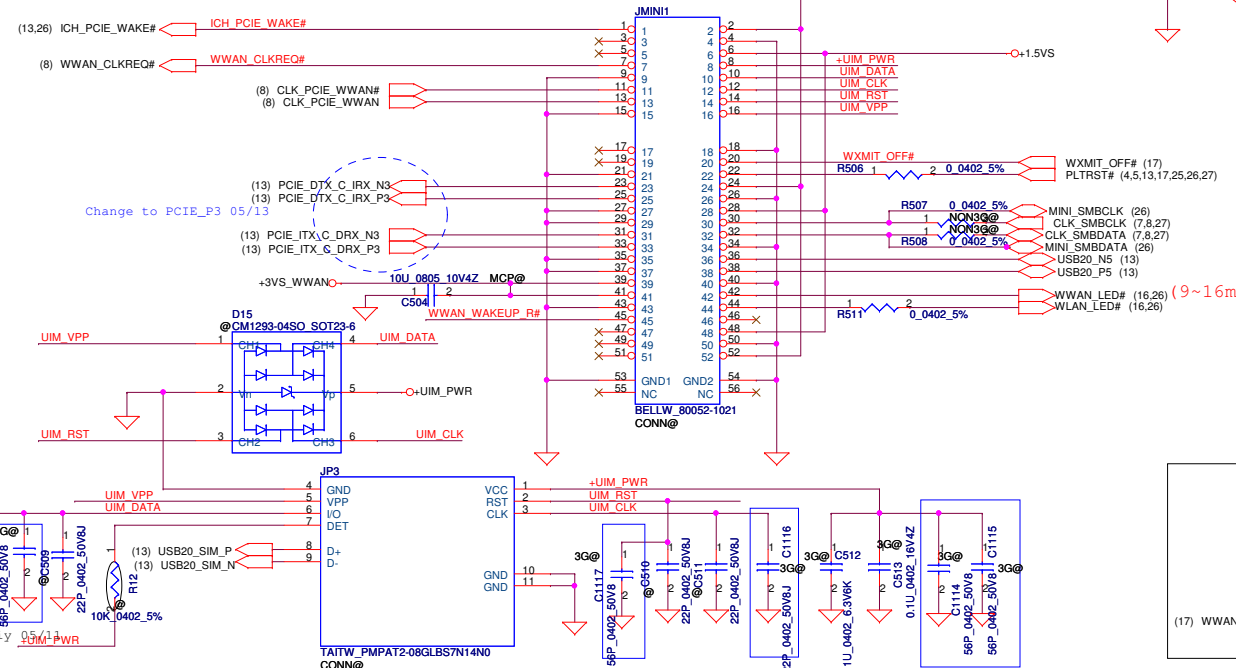
Security Classification	Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Compal Electronics, Inc.
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Size	Document Number	Rev		0.1	
Custom	LA-6421P				
Date:	Thursday, March 25, 2010	Sheet	14	of	39



Change JMINI1 to FOX\_AS0B246-S50U-7F\_52P-T 06/29



Reserve for SIM card does not meet rise time and pull-up is needed.

Add C1115 C1114 C1116 C1117 C1118 05/11  
Change C512 to 1U\_0402 05/14

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/05	Deciphered Date	2007/8/18	
Title Mini-Card/BT CONN				
Size	Document Number	Rev	0.1	
Date:	Monday, June 28, 2010	Sheet	15	of 39

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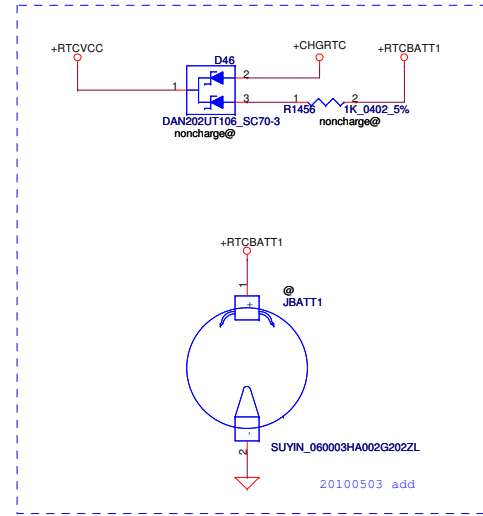
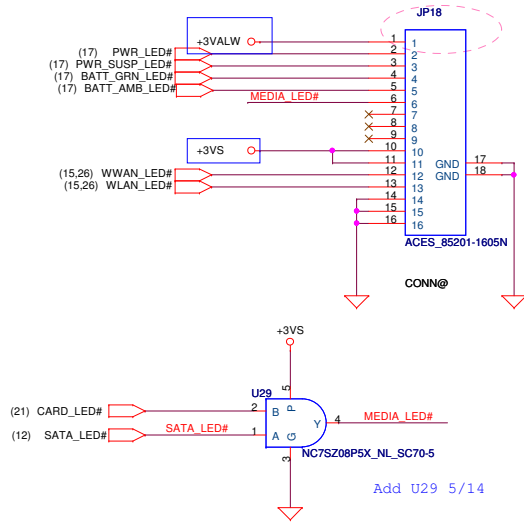


**ADD LED PCB CONN 06/12**

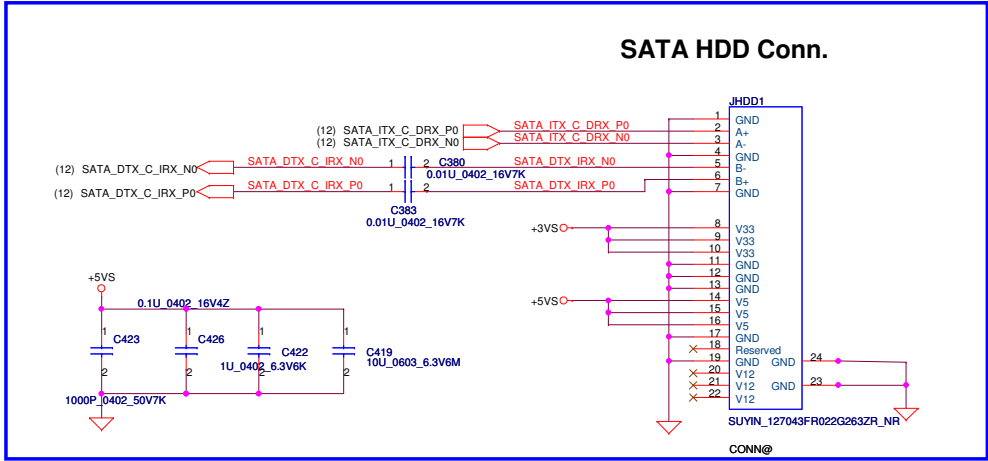
Change JP18 to NEW P/N 06/23

09/03 Change +5VALW , +5VS to +3VALW +3VS

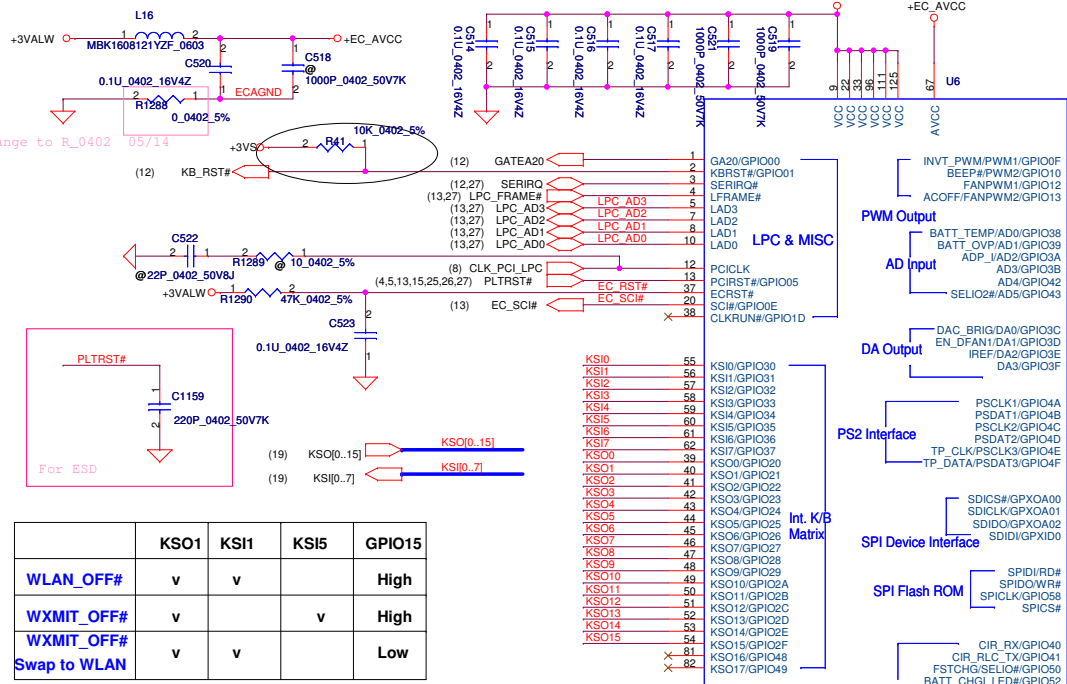
**LED PCB CONN**



**SATA HDD Conn.**



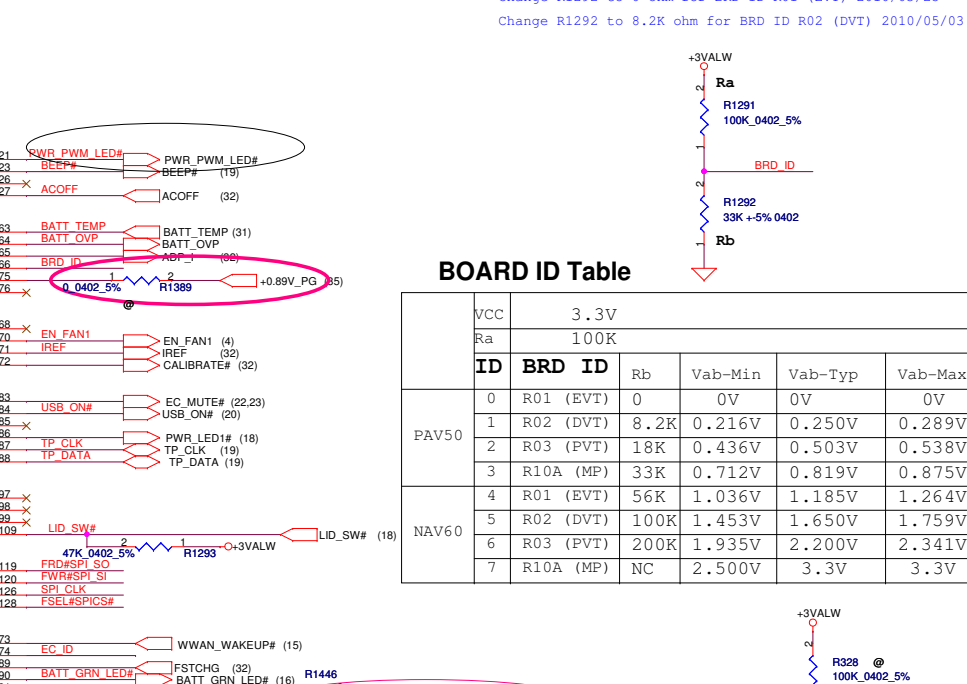
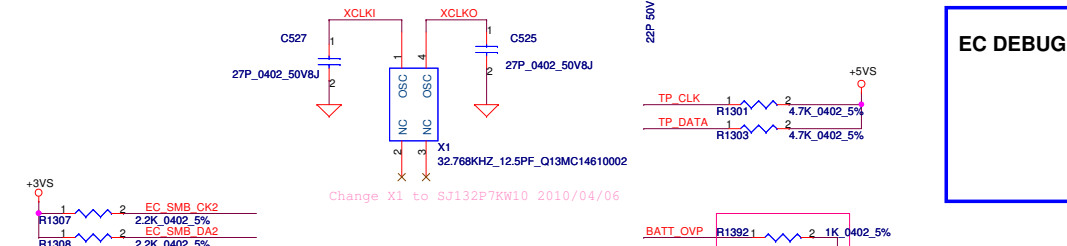
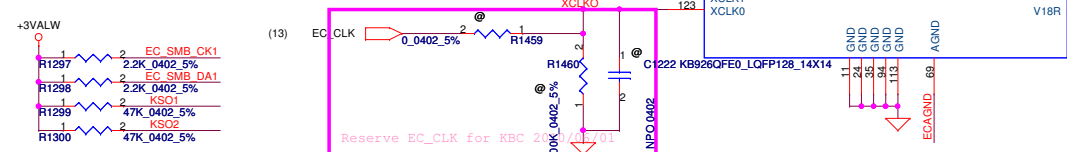
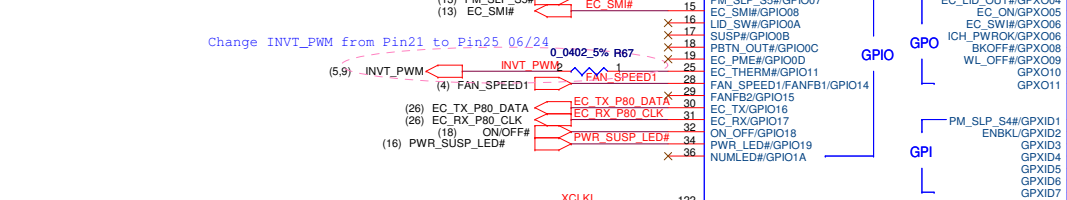
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title
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	KSO1	KSI1	KSI5	GPIO15
WLAN_OFF#	v	v		High
WXMIT_OFF#	v		v	High
WXMIT_OFF# Swap to WLAN	v	v		Low

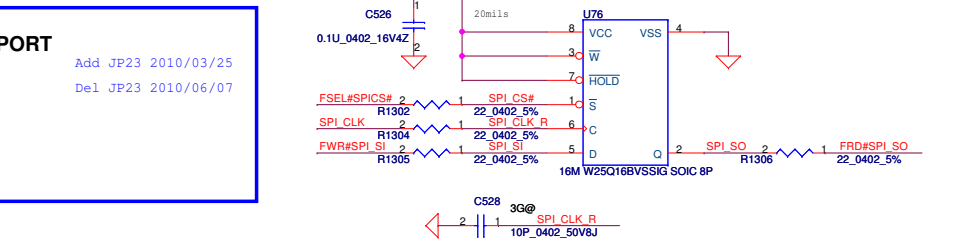
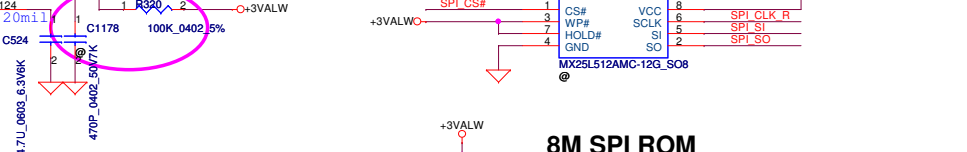
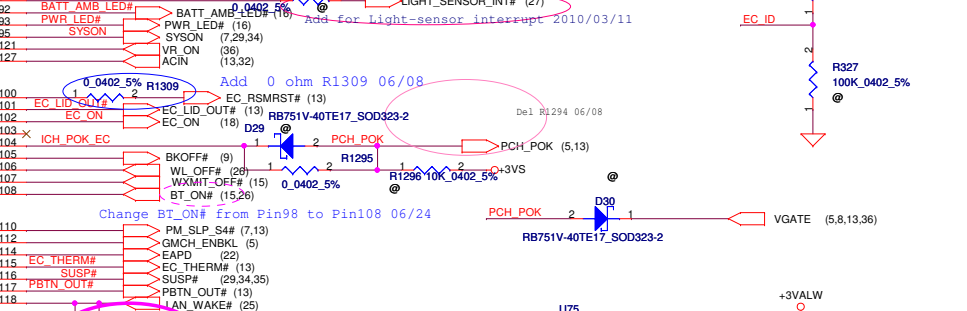
  

	KSO1
KSI1	WL_BTN#
KSI5	3G_BTN#



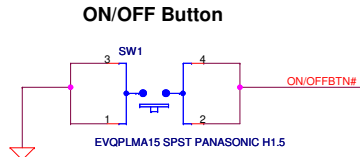
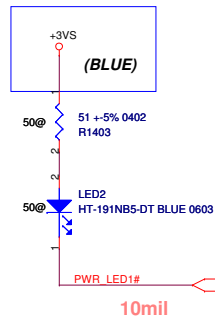
### BOARD ID Table

	VCC	3.3V				
	Ra	100K				
ID	BRD ID	Rb	Vab-Min	Vab-Typ	Vab-Max	
PAV50	0	R01 (EVT)	0	0V	0V	0V
	1	R02 (DVT)	8.2K	0.216V	0.250V	0.289V
	2	R03 (PVT)	1.8K	0.436V	0.503V	0.538V
	3	R10A (MP)	33K	0.712V	0.819V	0.875V
NAV60	4	R01 (EVT)	56K	1.036V	1.185V	1.264V
	5	R02 (DVT)	100K	1.453V	1.650V	1.759V
	6	R03 (PVT)	200K	1.935V	2.200V	2.341V
	7	R10A (MP)	NC	2.500V	3.3V	3.3V

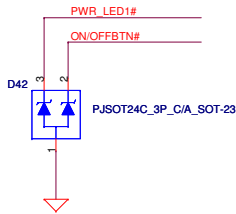
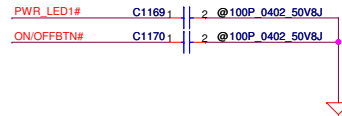


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Customer	Document Number		LA-6421P	Rev
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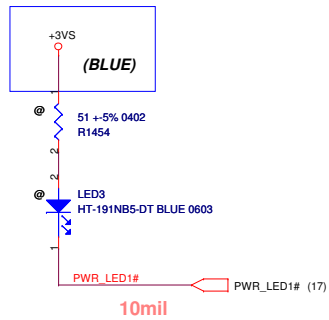
Add For NAV50 07/06  
09/03 Change +5VS to +3VS



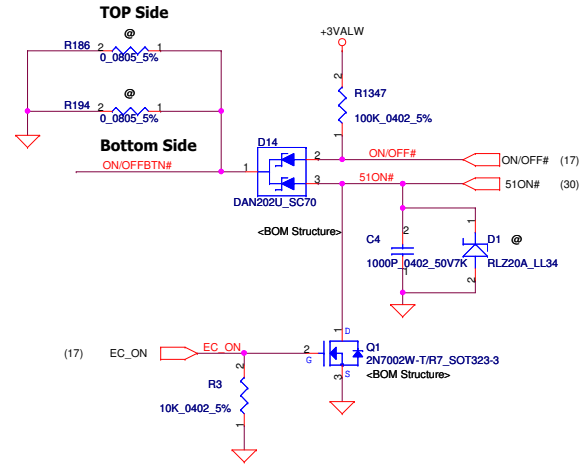
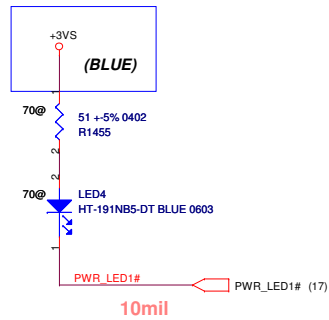
**FOR EMI**



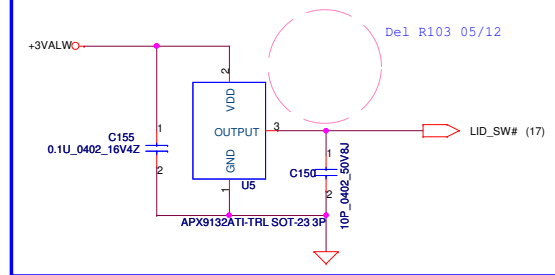
Add For PAV70 2010/04/09



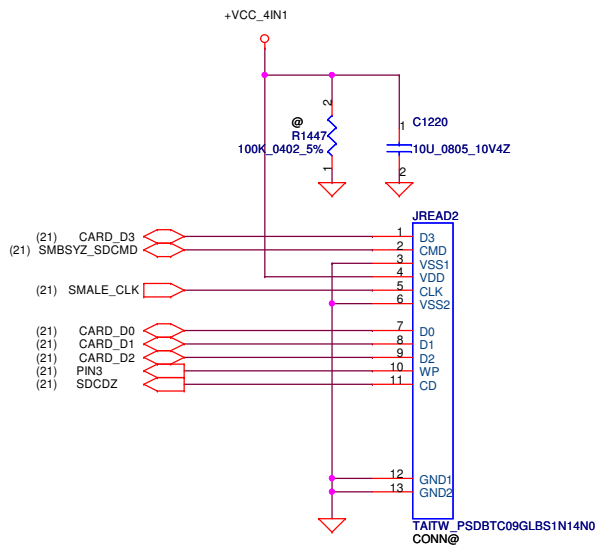
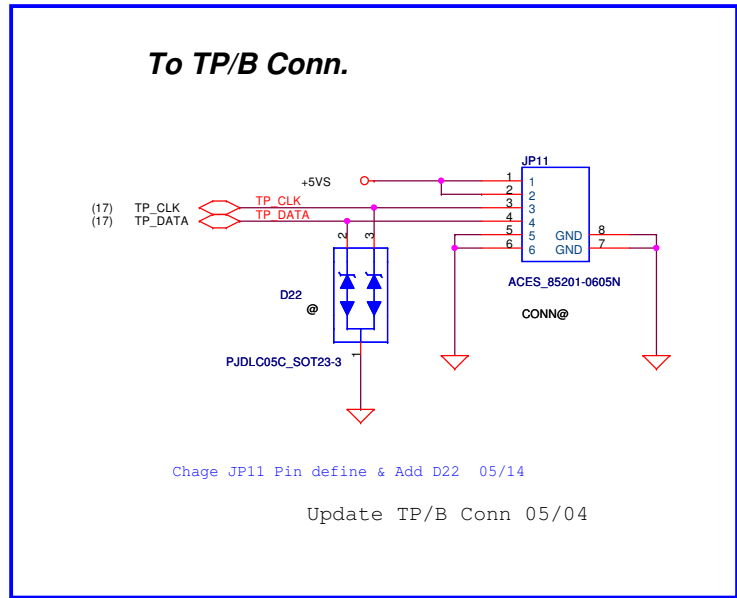
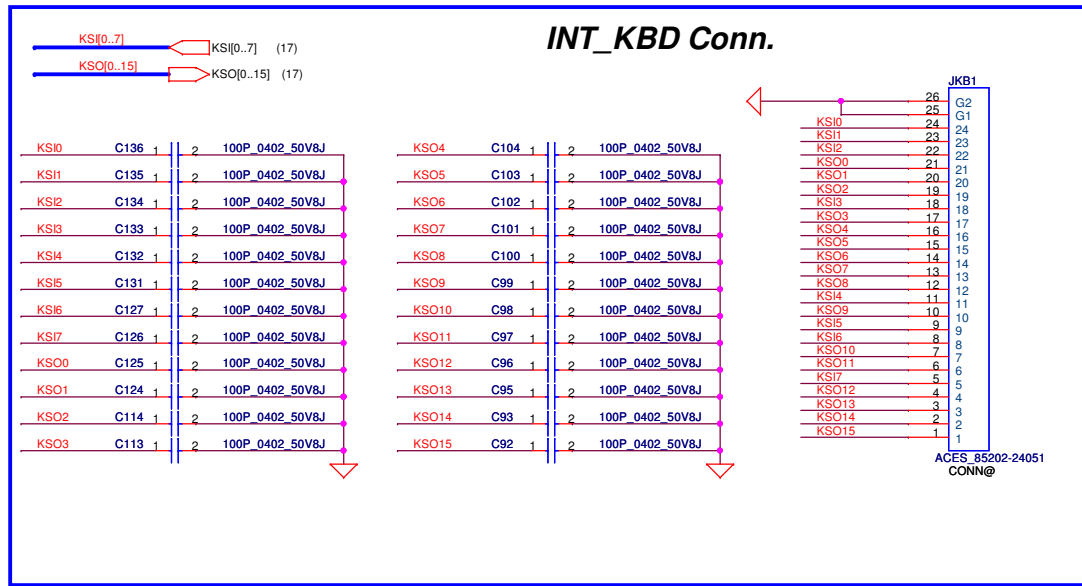
Add For PAV70 2010/04/09



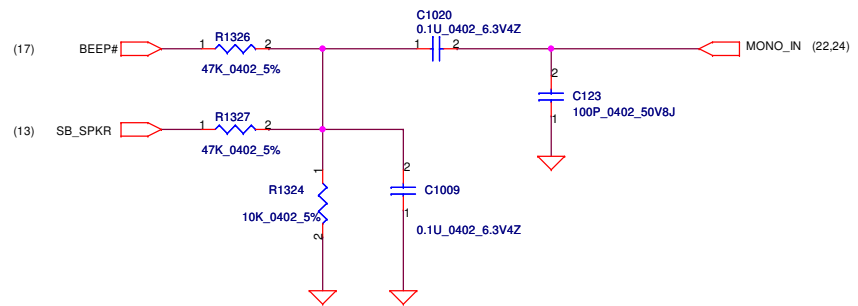
**LID Switch**



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Size	Document Number		Rev	
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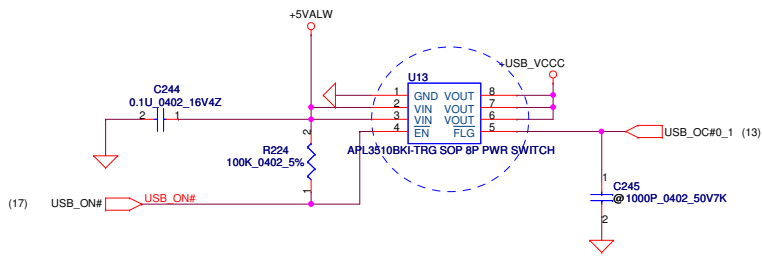


6/26 Add circuit



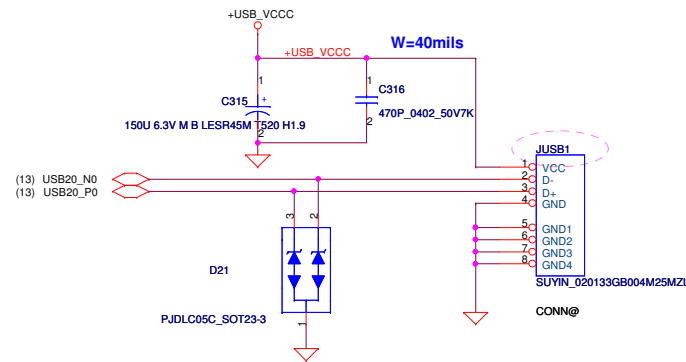
Modify MONO\_IN schematic, move some parts to I/O Board, Add the MONO\_IN\_R on M/B 06/25

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				KB Conn/TP/CR Conn	
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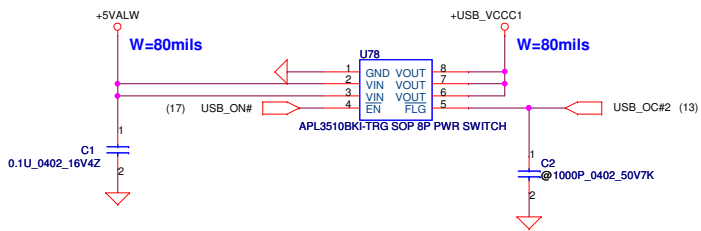
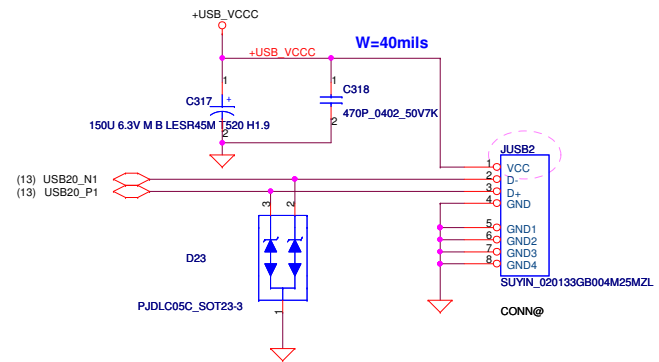


Change JUSB1 JUSB2 to NEW P/N SP010906181 06/23

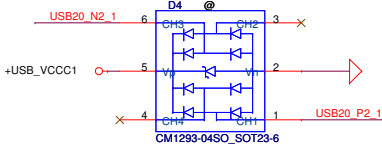
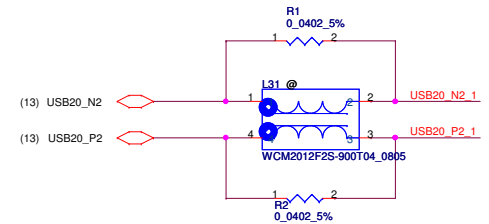
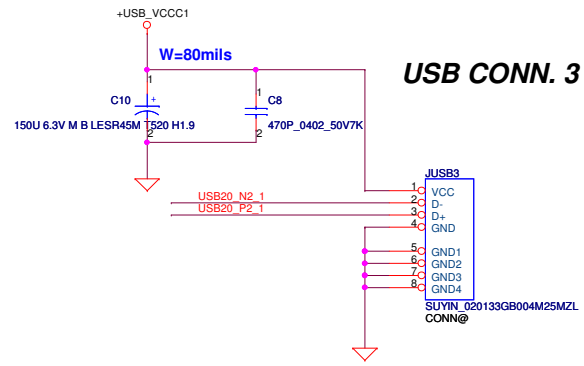
### USB CONN.1



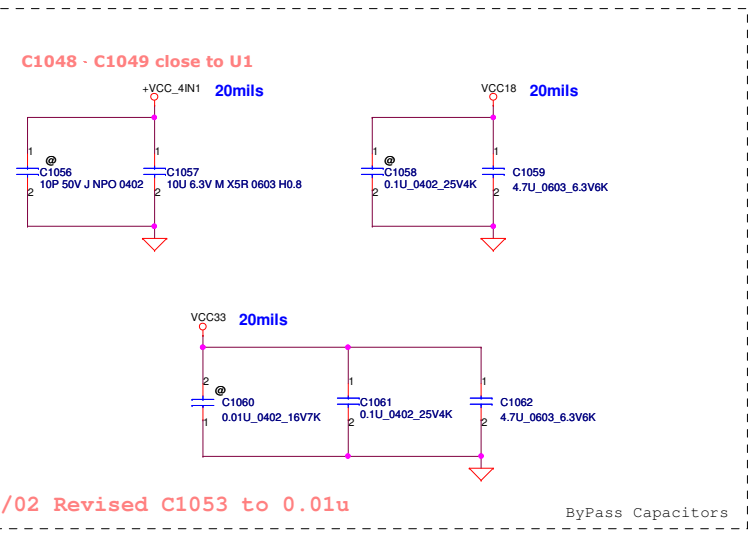
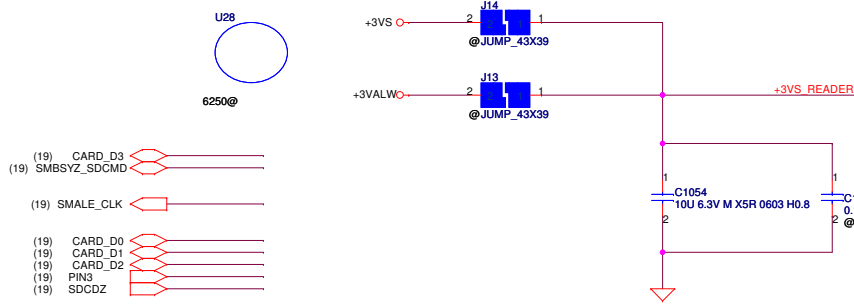
### USB CONN.2



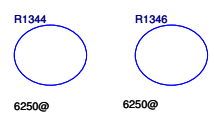
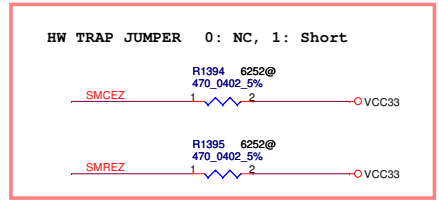
### USB CONN. 3



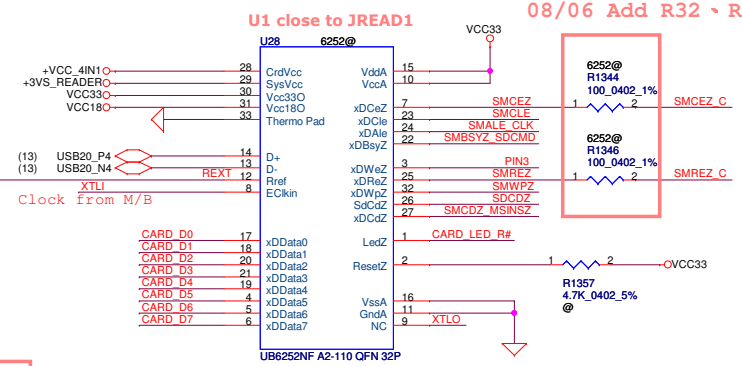
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title		
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Size B	Document Number		Rev		0.1	
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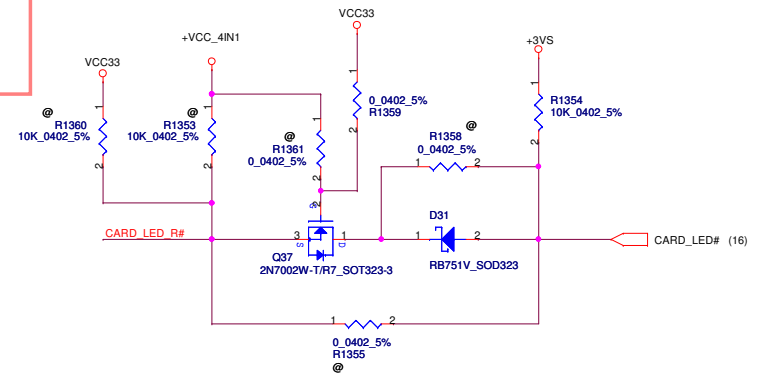
08/06 Add R1347, R1348



08/06 Add R32, R33

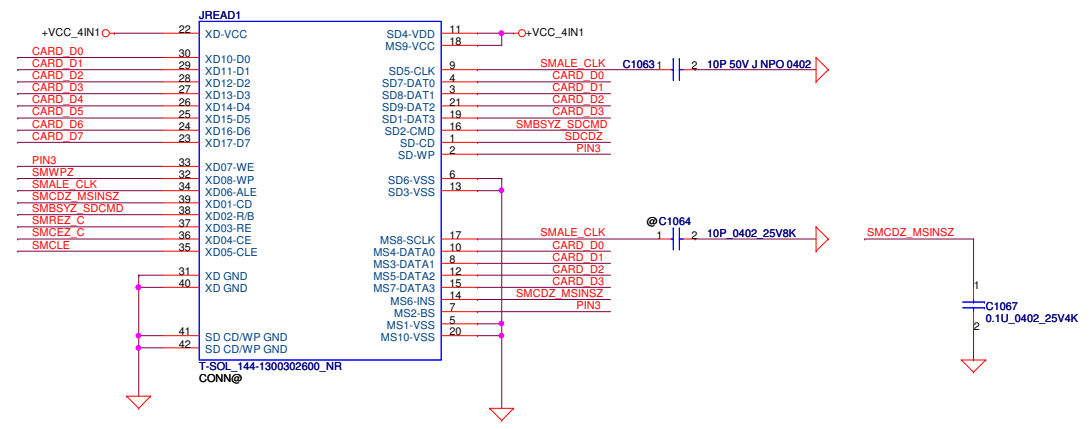


If use external crystal (Y4), U1 will change UB6252

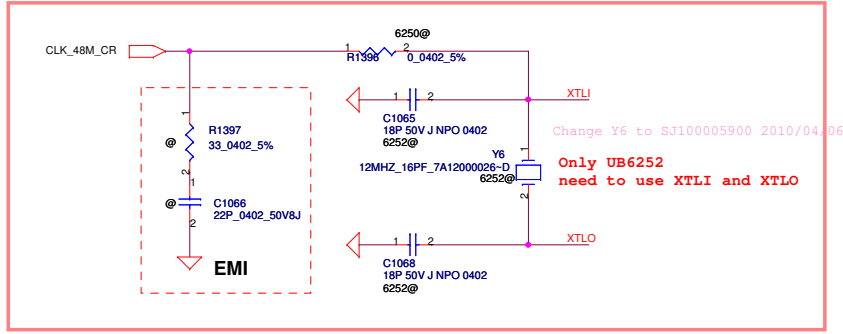


07/02 Update JREADER1

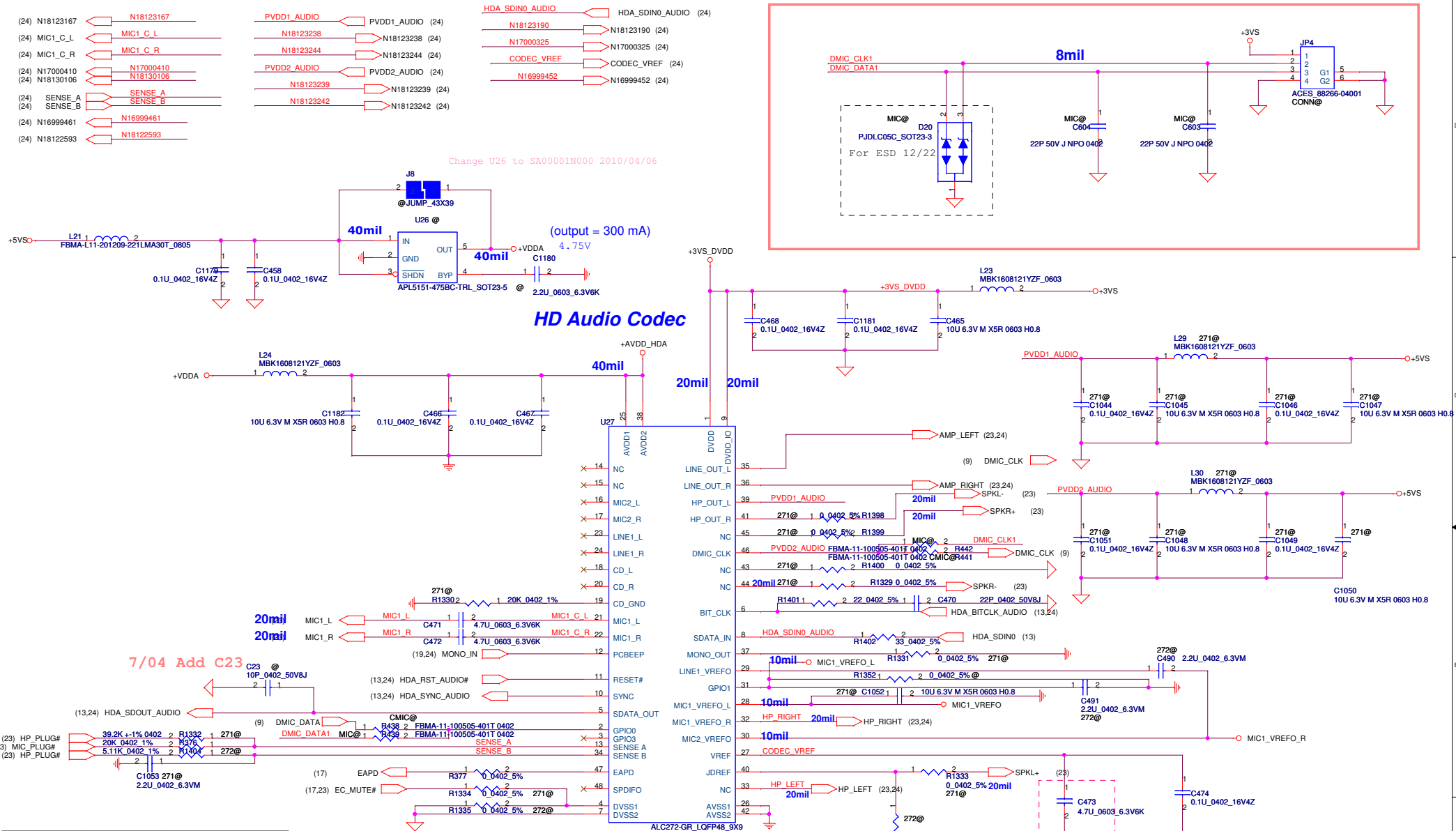
Card Reader Connector



4/30 Add CLK\_SD\_48M

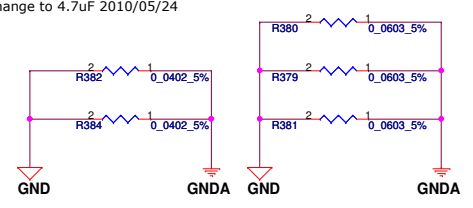


Security Classification	Compal Secret Data		Title	
Issued Date	2009/01/22	Deciphered Date	2009/11/20	Card reader
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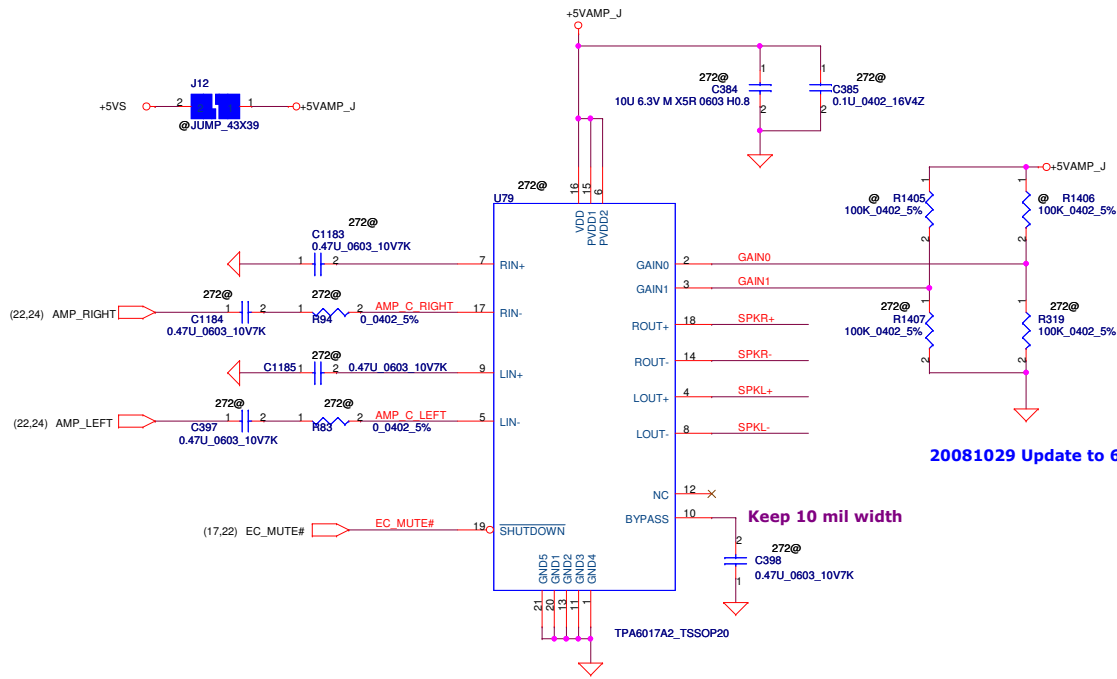


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Change to SA0002CI20 ALC272-VA2-GR

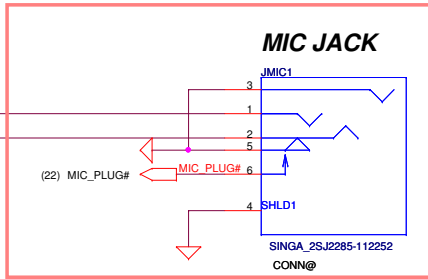
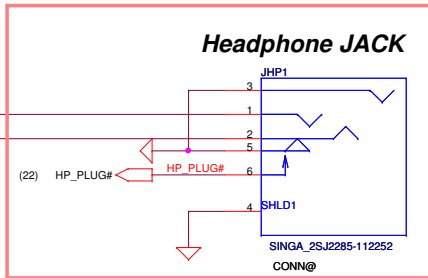
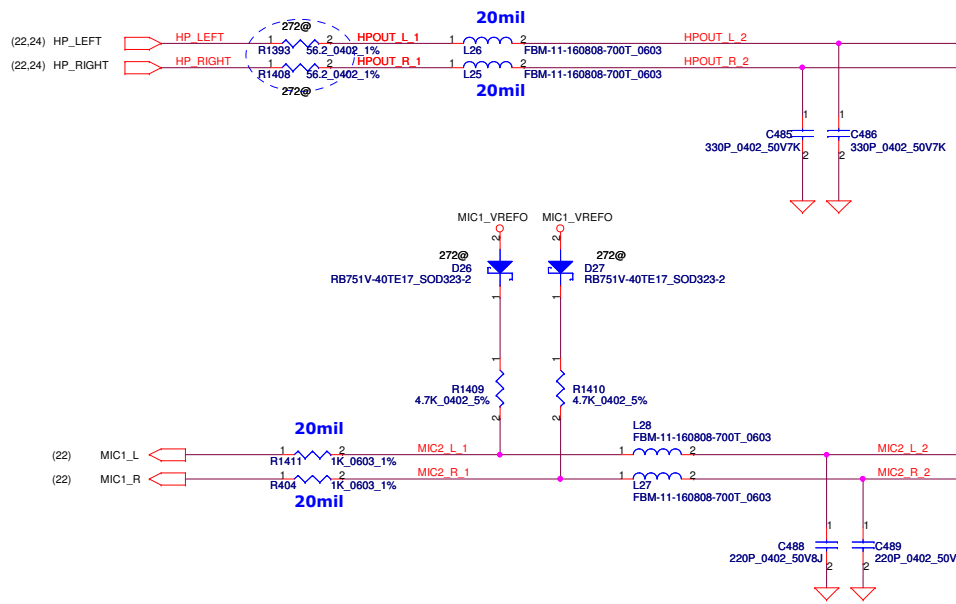
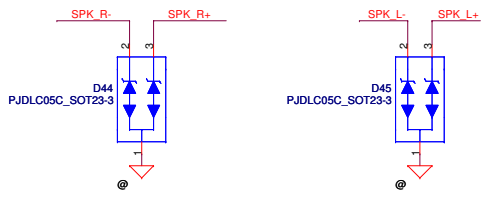
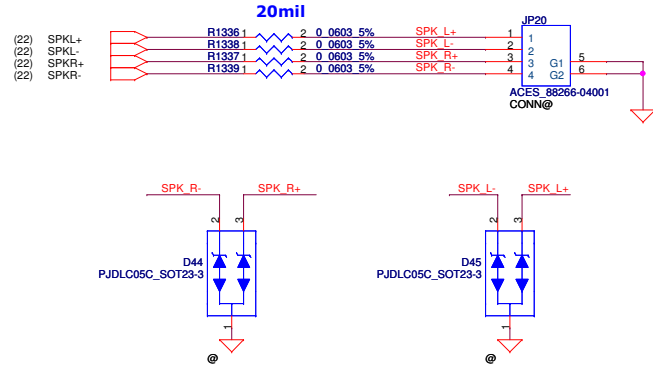






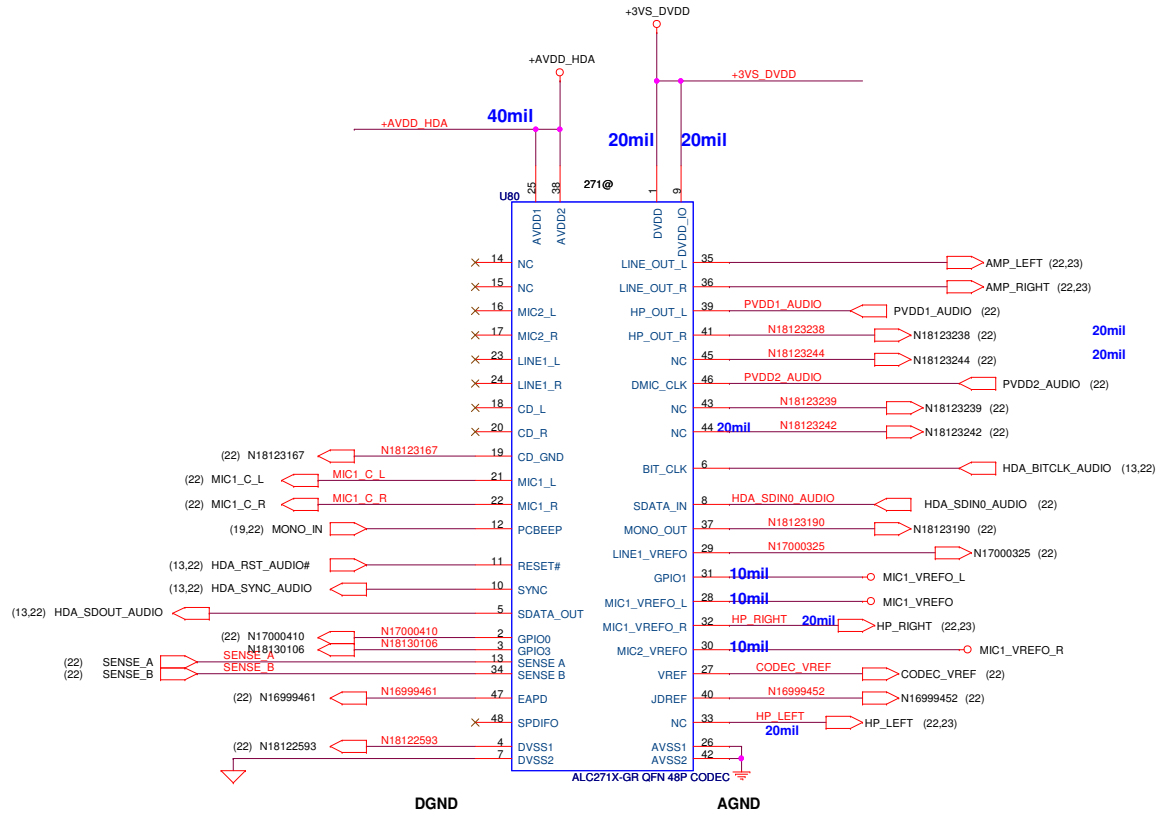
20081029 Update to 6dB

### Int. Speaker Conn.



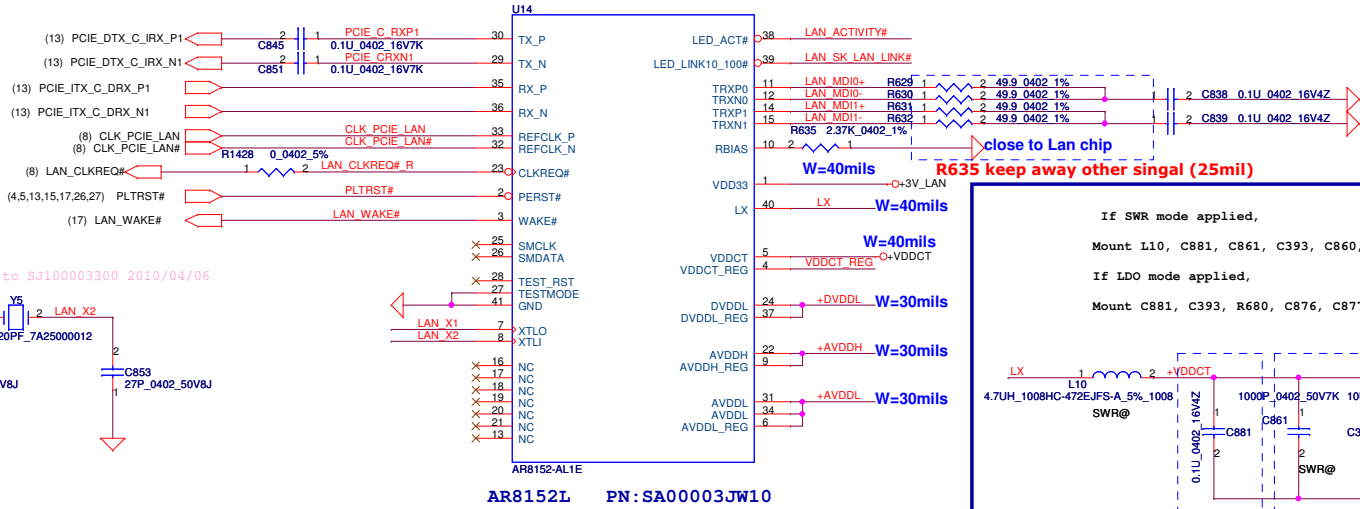
<b>Compal Electronics, Inc.</b>		
Title	<Title> <b>Amplifier &amp; Audio Jack</b>	
Size	Document Number	Rev
Customer	LA-6222P	0.1
Date:	Tuesday, June 22, 2010	Sheet 23 of 39

## HD Audio Codec

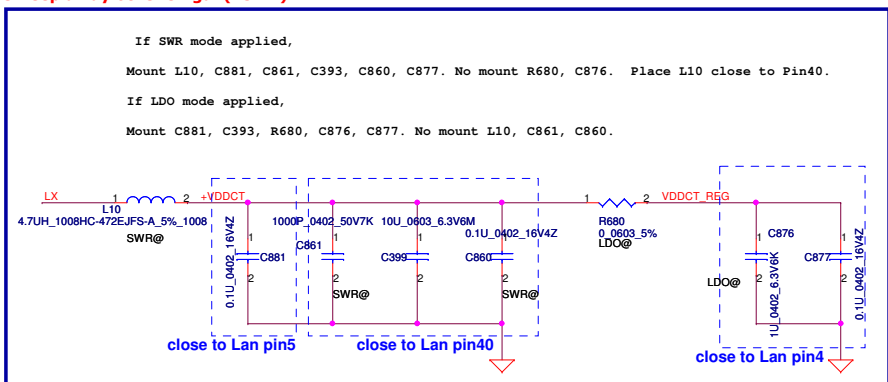
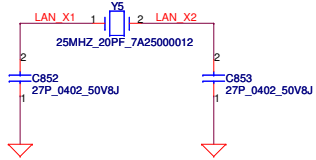


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

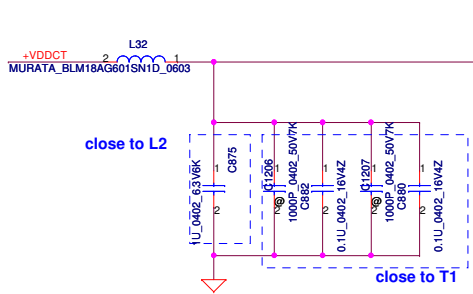
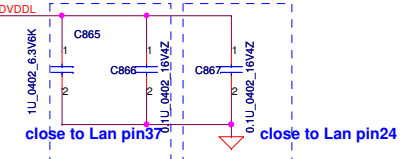
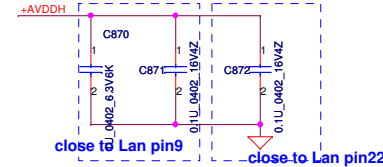
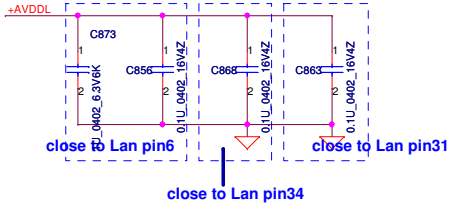
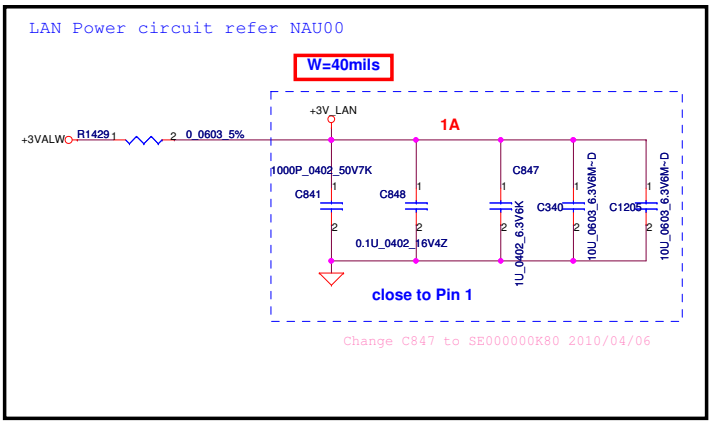
Change LAN chip to AR8152-L for NAV70/80 DDR3 2010/01/22



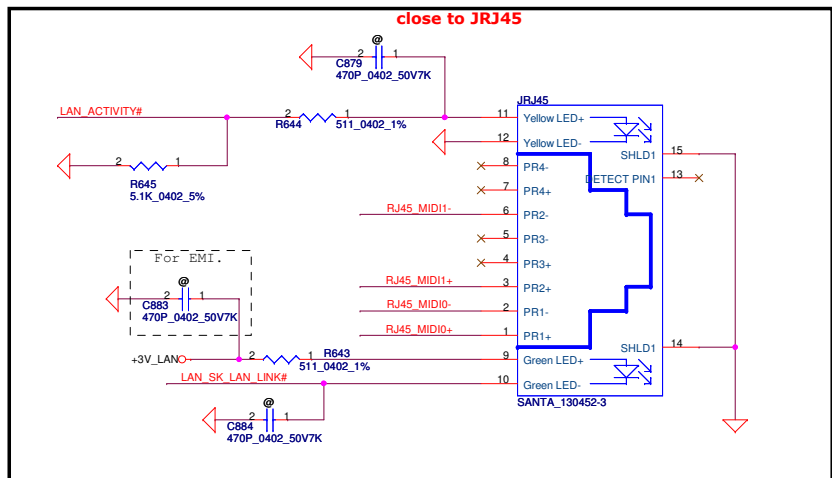
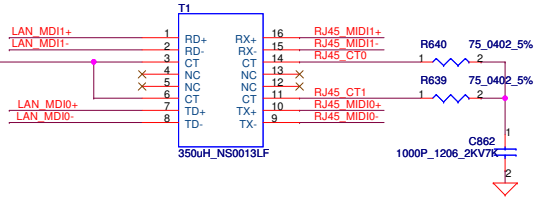
Change Y5 to SJ100003300 2010/04/06



Change C865, C870, C873, C876 to SE000000K80 2010/04/06

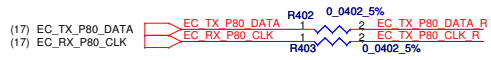


Change C875 to SE000000K80 2010/04/06

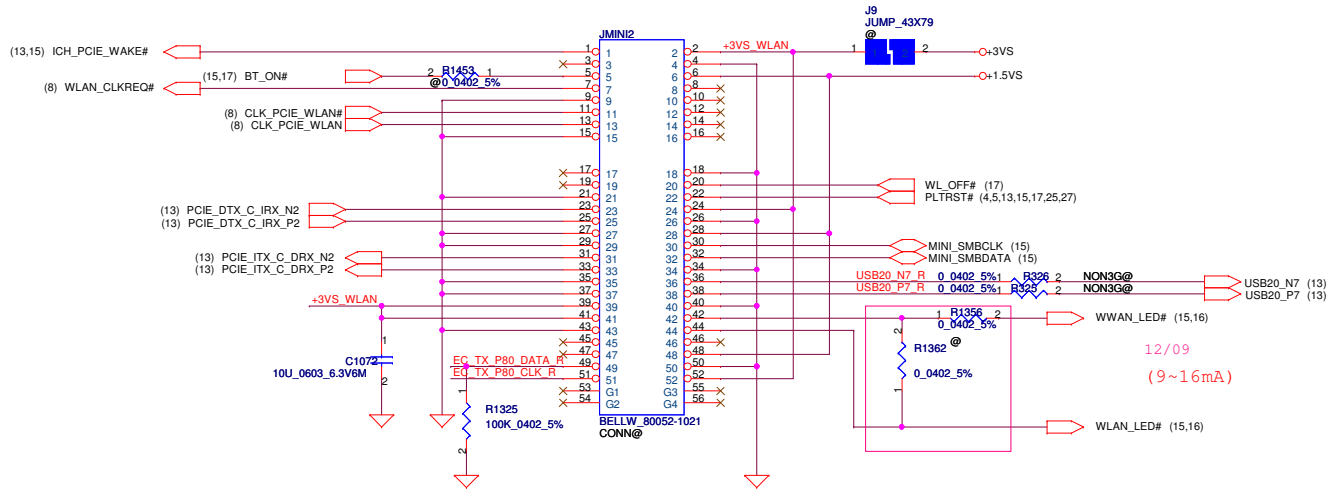
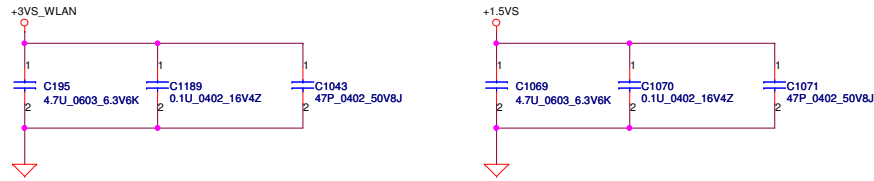


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Size	Document Number	Rev		
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Date:	Thursday, June 03, 2010	Sheet	25	of 39

# Mini-Express Card for WWAN



# Mini-Express Card for WLAN



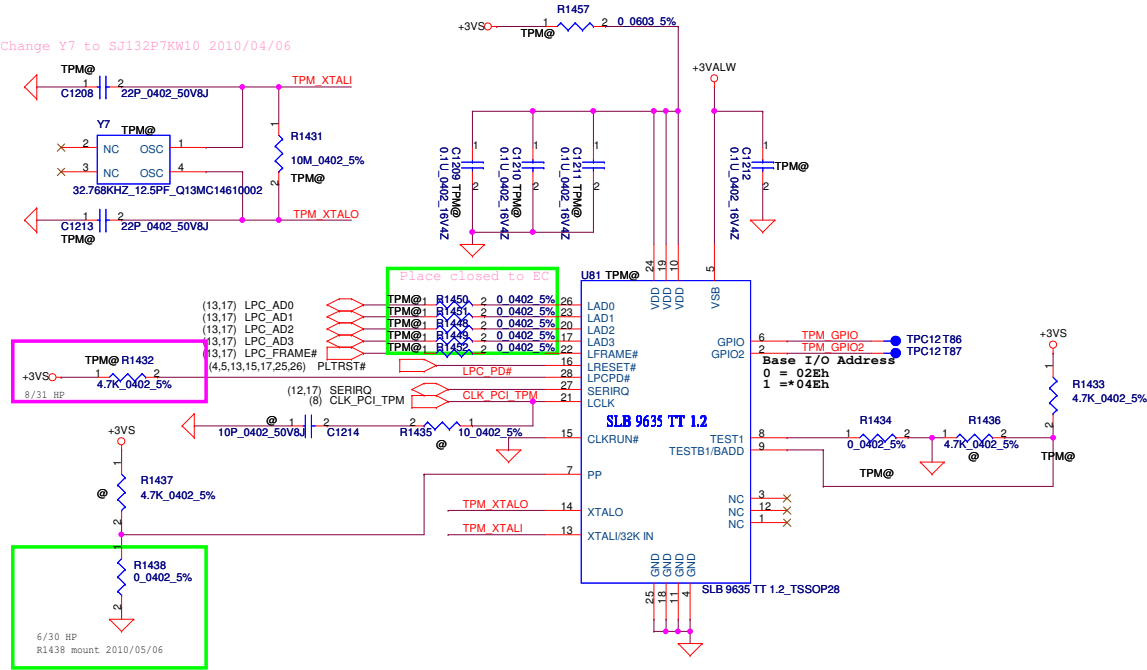
5/12 Update WLAN connector(the same as KAV60)  
 6/1 Revised 37、39、41、42、43 to NC  
 6/12 Update connector to DC040006S00  
 6/26 Update JMINI1 footprint  
 7/01 update pin 23,25,31,33

12/09  
 (9~16mA)

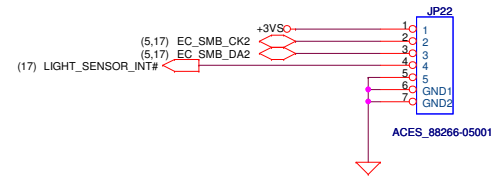
<b>Compal Electronics, Inc.</b>		
Title	<Title> WLAN	
Size	Document Number	Rev
Customer	LA-6222P	0.1
Date:	Monday, June 07, 2010	Sheet 26 of 39

# TPM1.2 on board

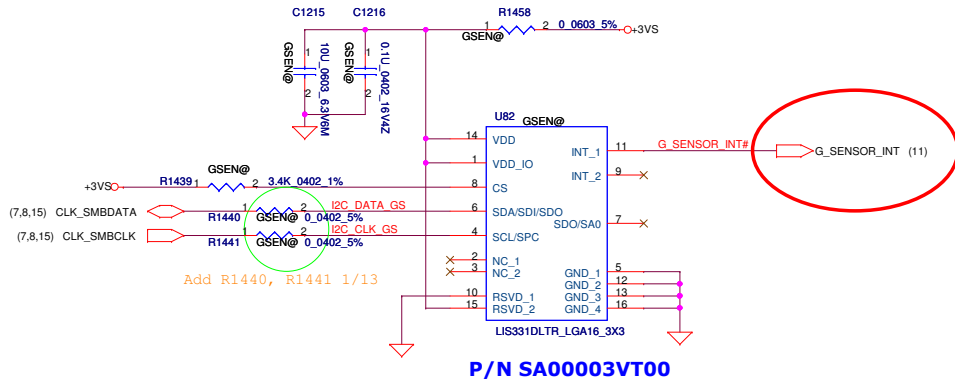
Change Y7 to SJ132P7KW10 2010/04/06



# ALS (Ambient Light Sensor)

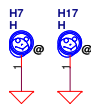
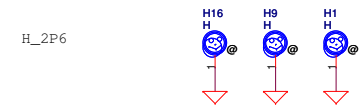
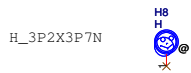


# ST LIS33DE(G-Sensor)

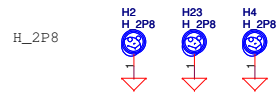
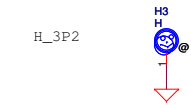
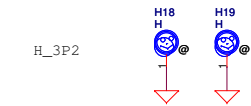


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Size	Document Number	Rev	Date			
	LA-6421P	0.1	Thursday, June 03, 2010   Sheet 27 of 39			

Modify Hole location by (ME Drawing 06/12) 0615



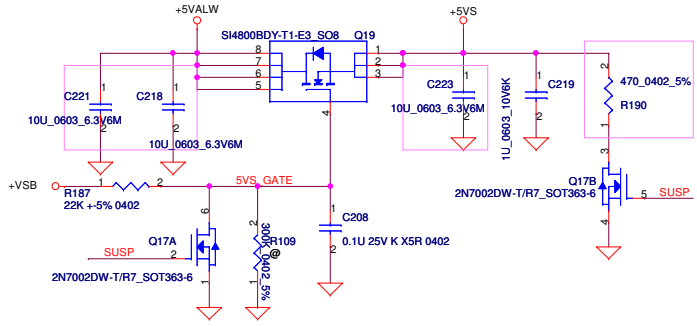
09/03 Del H12



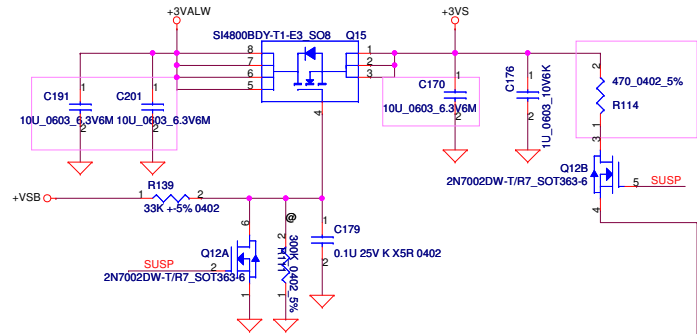
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title Screw		
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Change R51 R57 R70 R63 R317 R114 R190 to 0402 SIZE 04/30  
 Change C221 C218 C223 C 191 C201 C170 C392 C393 C394 to 0603 SIZE 04/30

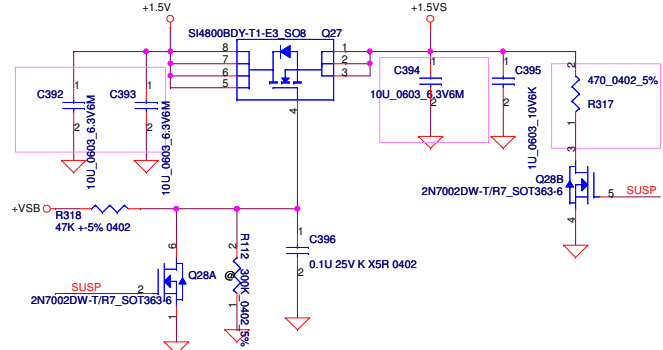
**+5VALW TO +5VS**



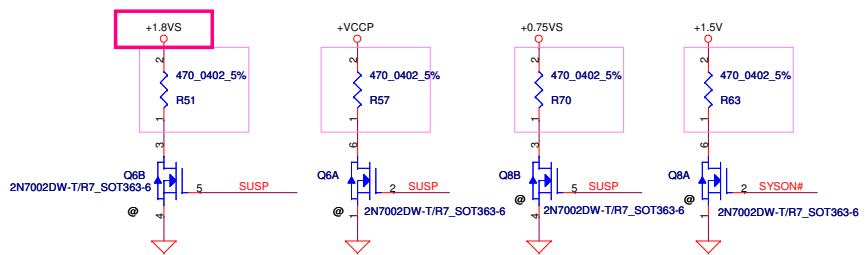
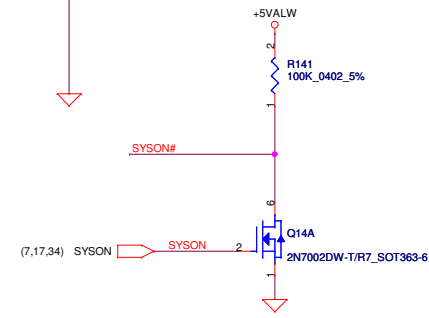
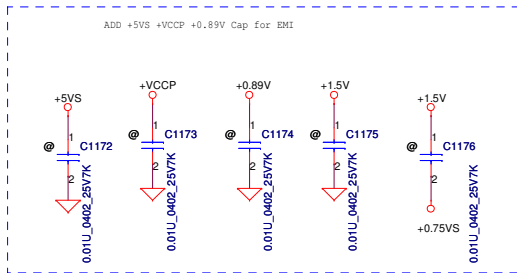
**+3VALW TO +3VS**



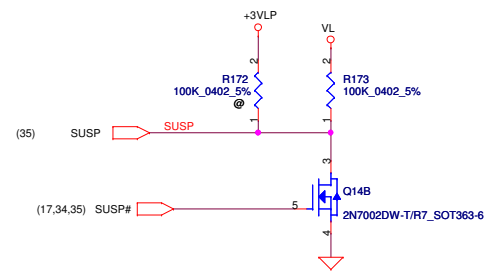
**+1.5V to +1.5VS**



Change Q12,Q14,Q17,Q28 to SB00000DH00 2010/04/06  
 Change C176,C219,C395 to SE080105K80 2010/04/06

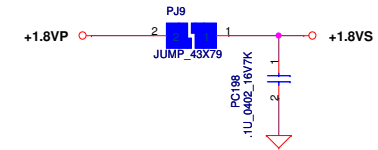
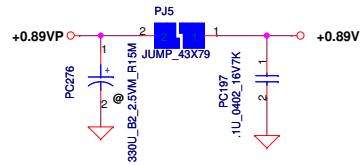
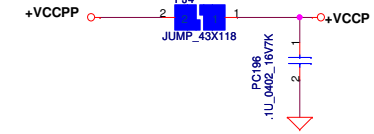
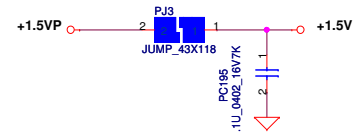
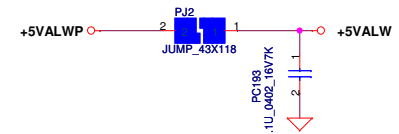
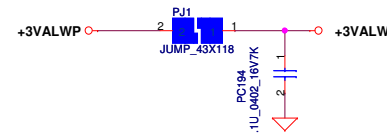
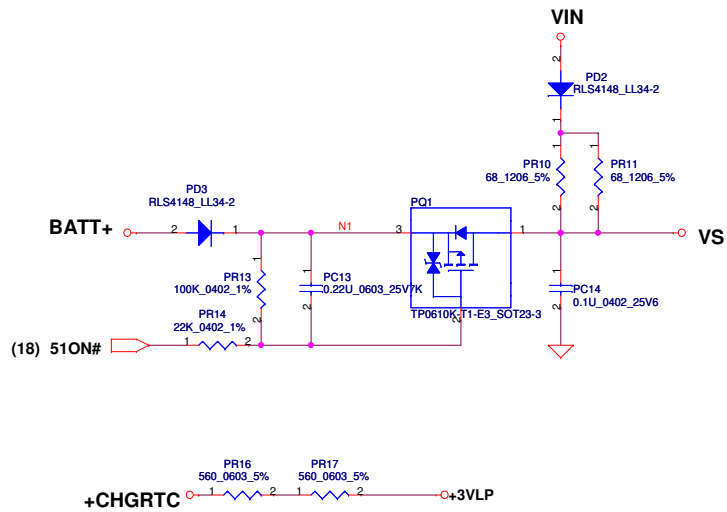
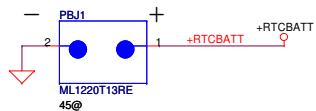
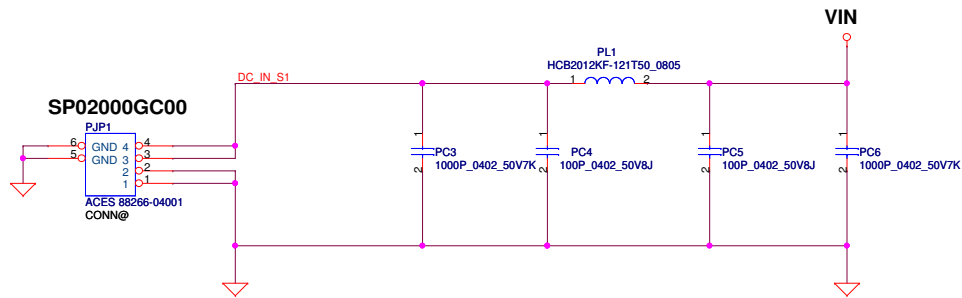


Change Q6,Q8 to SB00000DH00 2010/04/06



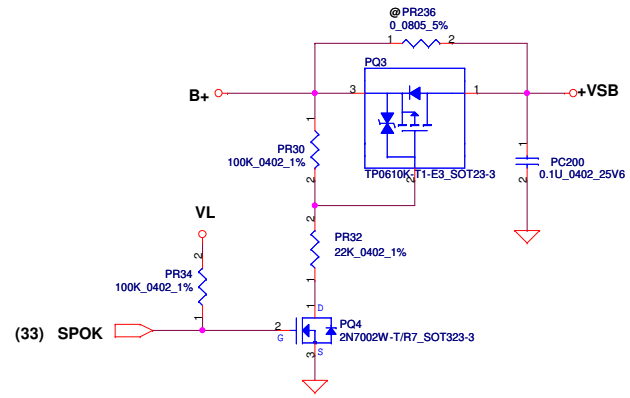
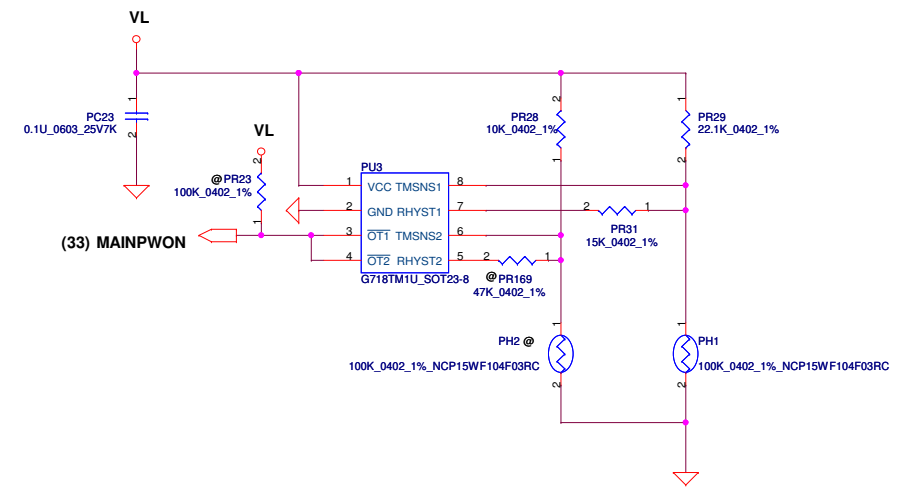
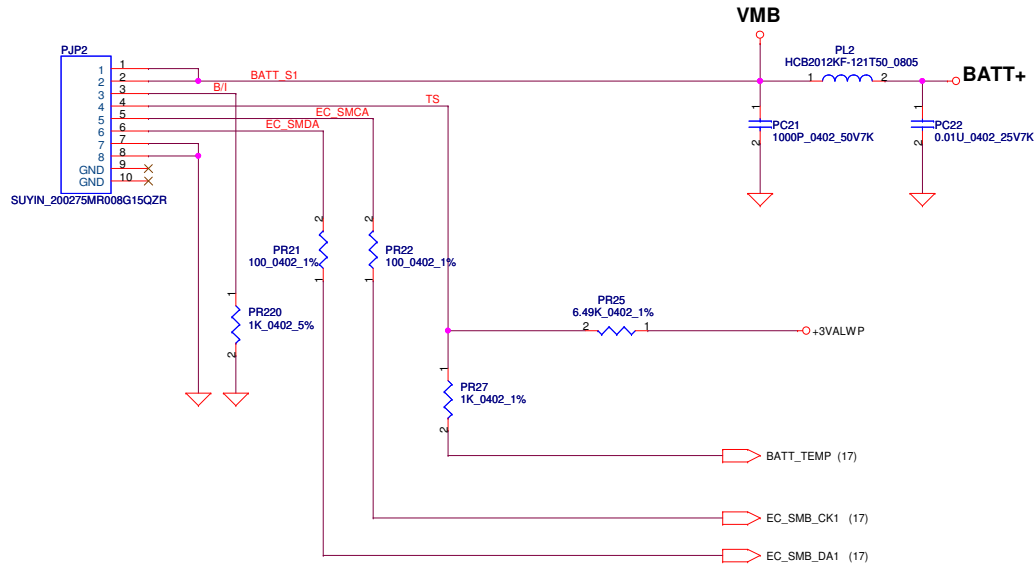
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				DC INTERFACE		
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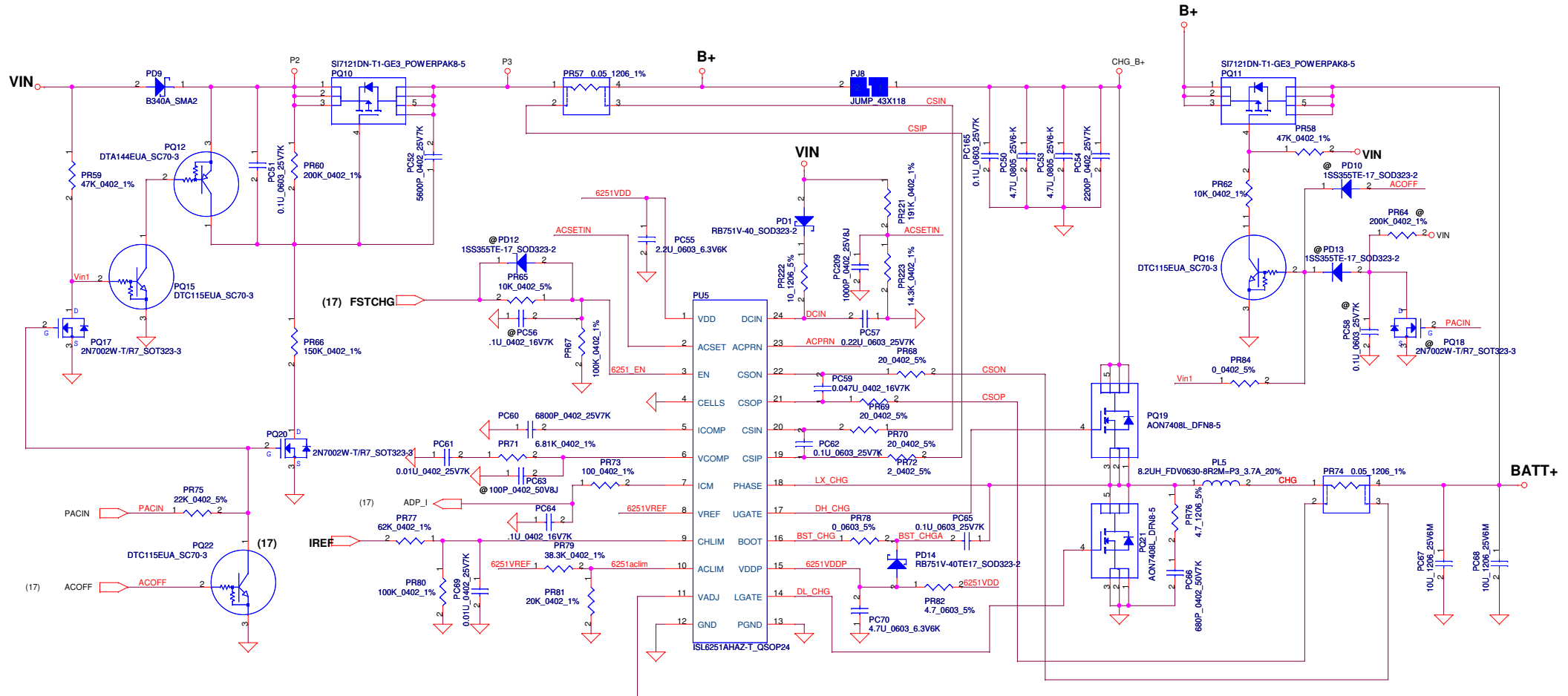


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PH1 under CPU botten side :  
 CPU thermal protection at 92 degree C  
 Recovery at 72 degree C



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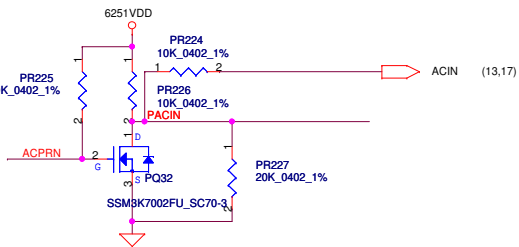
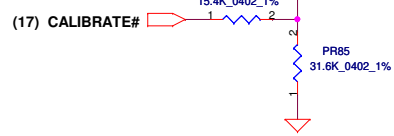
$I_{ada} = 0 \sim 1.58A (30W)$      $CP = 85\% \cdot I_{ada}$  ;  $CP = 1.343A$

CP mode  
 $V_{aclim} = 2.39 \cdot (20K / (20K + 38.3K)) = 0.8199V$   
 $I_{input} = (1 / 0.05) \cdot ((0.05 \cdot V_{aclim}) / 2.39 + 0.05)$   
 where  $V_{aclim} = 0.8199V$ ,  $I_{input} = 1.343A$

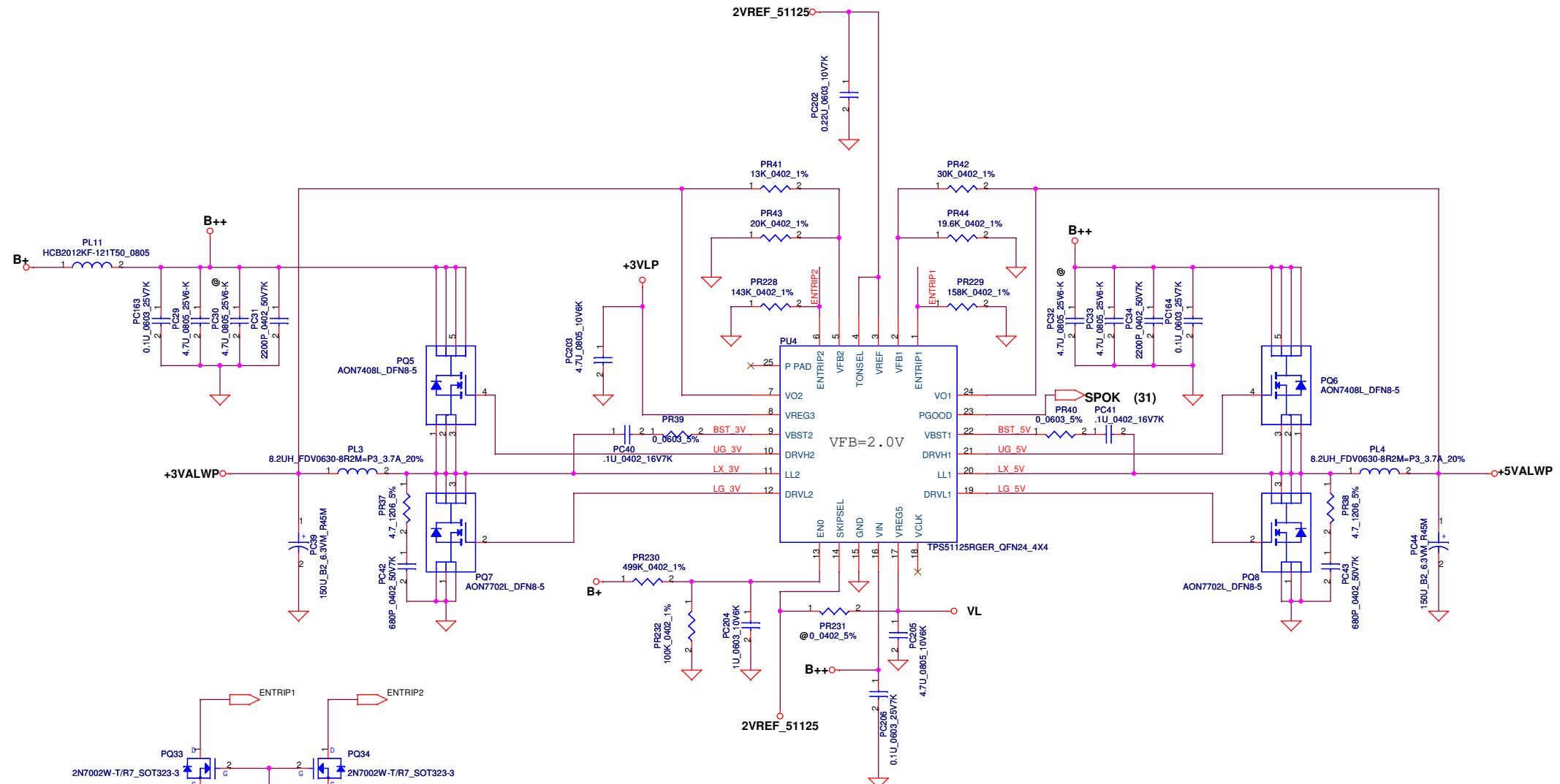
$CC = 0.3 \sim 1.76A$   
 $I_{REF} = 1.62 \cdot I_{charge}$   
 $I_{REF} = 0.486V \sim 2.85V$   
 $3.24V \implies 2A$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

$V_{ADJ} \rightarrow V_{REF} \rightarrow 4.41V$   
 $V_{ADJ} \rightarrow \text{Ground} \rightarrow 3.59V$   
 $V_{cell} = (0.175 \cdot V_{ADJ} + 3.99)$

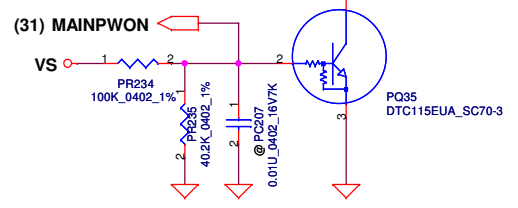


$V_{th, rise (typical)} = ((191K / 14.3K) + 1) \cdot 1.26$   
 $= 18.89V$   
 $V_{th, fall (typical)} = ((191K / 14.3K) + 1) \cdot 1.26 - 3.4\mu A \cdot 191K$   
 $= 17.43V$

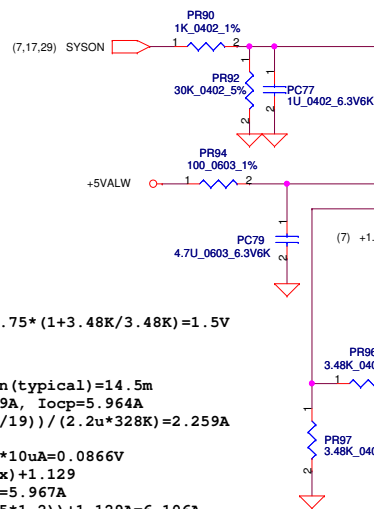


**+3.3VALWP** Ipeak=5.731A Imax=4.012A  
 Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)  
 $V_{trip} = (10E-06 * 130K) / 9 - 24mV = 134.9mV$   
 $I_{limit} = 134.9mV / 17.9m \sim 134.9mV / 14.5m \times 1.2$   
 $= 7.536A \sim 7.752A$   
 $I_{ocp} = I_{limit} + \Delta I / 2$   
 $= 8.081A \sim 8.297A$   
 $\Delta I = 1.090A$  (Freq=305KHz)

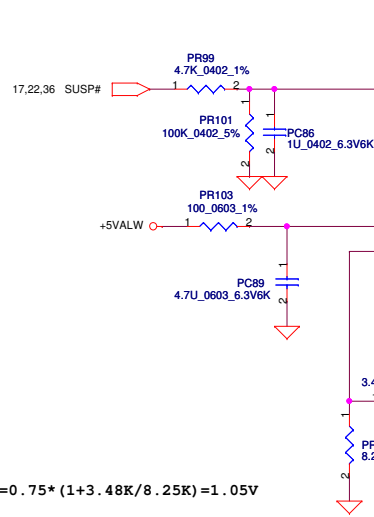
**+5VALWP** Ipeak=7.0A Imax=4.9A  
 Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)  
 $V_{trip} = (10E-06 * 147K) / 9 - 24mV = 151mV$   
 $I_{limit} = 151mV / 17.9m \sim 151mV / 14.5m \times 1.2$   
 $= 8.467A \sim 8.710A$   
 $I_{ocp} = I_{limit} + \Delta I / 2$   
 $= 9.384A \sim 9.627A$   
 $\Delta I = 1.834A$  (Freq=245KHz)



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Size	Document Number			Rev	0.1
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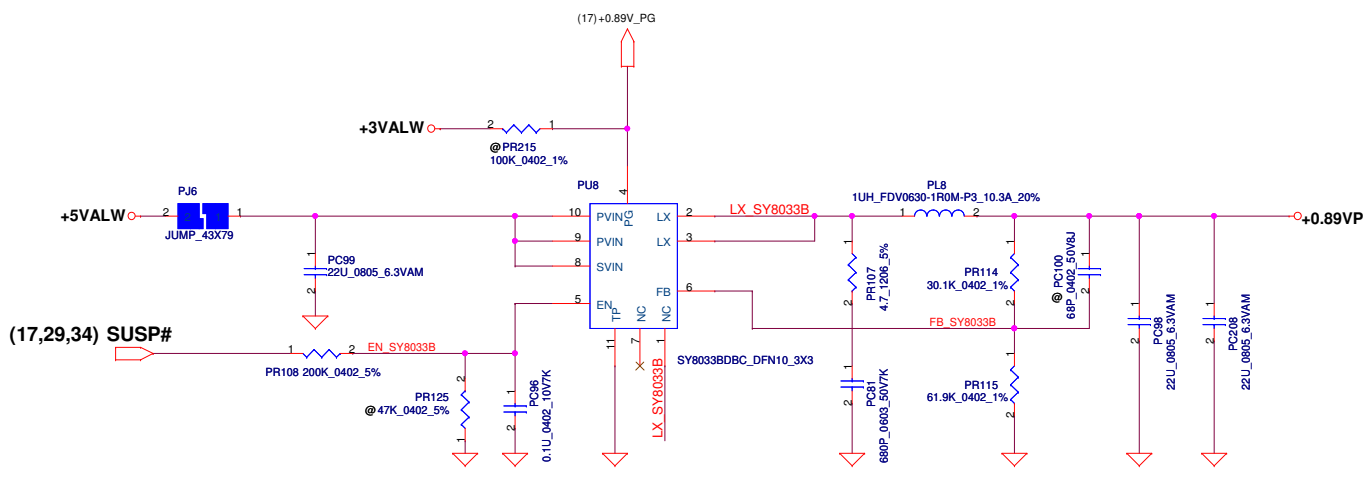
$\langle V_o=1.5V \rangle$   $V_{FB}=0.75V$   
 $V_o=V_{FB} \cdot (1+PR96/PR97)=0.75 \cdot (1+3.48K/3.48K)=1.5V$   
 $F_{sw}=328KHz$   
 $C_{out} ESR=15m\ \Omega$   
 $R_{dson(max)}=17.9m$   $R_{dson(typical)}=14.5m$   
 $I_{peak}=4.97A$ ,  $I_{max}=3.479A$ ,  $I_{ocp}=5.964A$   
 $\Delta I = ((19-1.8) \cdot (1.8/19)) / (2.2u \cdot 328K) = 2.259A$   
 $\Rightarrow 1/2 \Delta I = 1.129A$   
 $V_{trip}=R_{trip} \cdot 10uA = 8.66K \cdot 10uA = 0.0866V$   
 $I_{ocpmin}=V_{trip} / (R_{dsonmax}) + 1.129$   
 $= 0.0866 / (0.0179) + 1.129 = 5.967A$   
 $I_{ocpmax} = (0.0866 / (0.0145 \cdot 1.2)) + 1.129A = 6.106A$   
 $I_{ocp} = 5.967A - 6.106A$



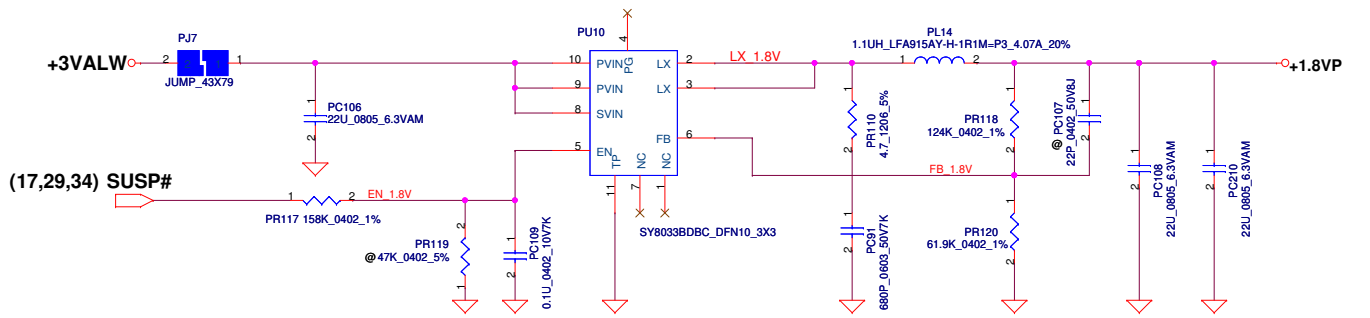
$\langle V_o=1.05V \rangle$   $V_{FB}=0.75V$   
 $V_o=V_{FB} \cdot (1+PR105/PR106)=0.75 \cdot (1+3.48K/8.25K)=1.05V$   
 $F_{sw}=280KHz$   
 $C_{out} ESR=15m\ \Omega$   $R_{dson(max)}=17.9m$   $R_{dson(typical)}=14.5m$   
 $I_{peak}=3.124A$ ,  $I_{max}=2.187A$ ,  $I_{ocp}=3.749A$   
 $\Delta I = ((19-1.05) \cdot (1.05/19)) / (1.5u \cdot 280K) = 3.549A$   
 $\Rightarrow 1/2 \Delta I = 1.774A$   
 $V_{trip}=R_{trip} \cdot 10uA = 14K \cdot 10uA = 0.14V$   
 $I_{ocpmin}=V_{trip} / (R_{dsonmax}) + 1.774$   
 $= 0.14 / (0.0179) + 1.774 = 9.596A$   
 $I_{ocpmax} = (0.14 / (0.0145 \cdot 1.2)) + 1.774A = 9.820A$   
 $I_{ocp} = 9.596A - 9.820A$

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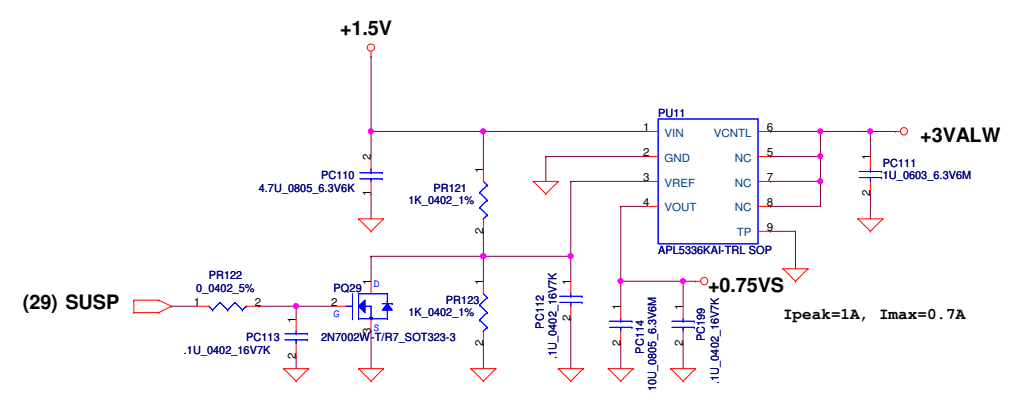
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Title			
1.5VP / +VCCPP			
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<Vo=0.89V> VFB=0.6V  
 $Vo = VFB * (1 + PR114 / PR115) = 0.6 * (1 + 30.1K / 61.9K) = 0.89V$   
 Ipeak=2.64A, Imax=1.848A

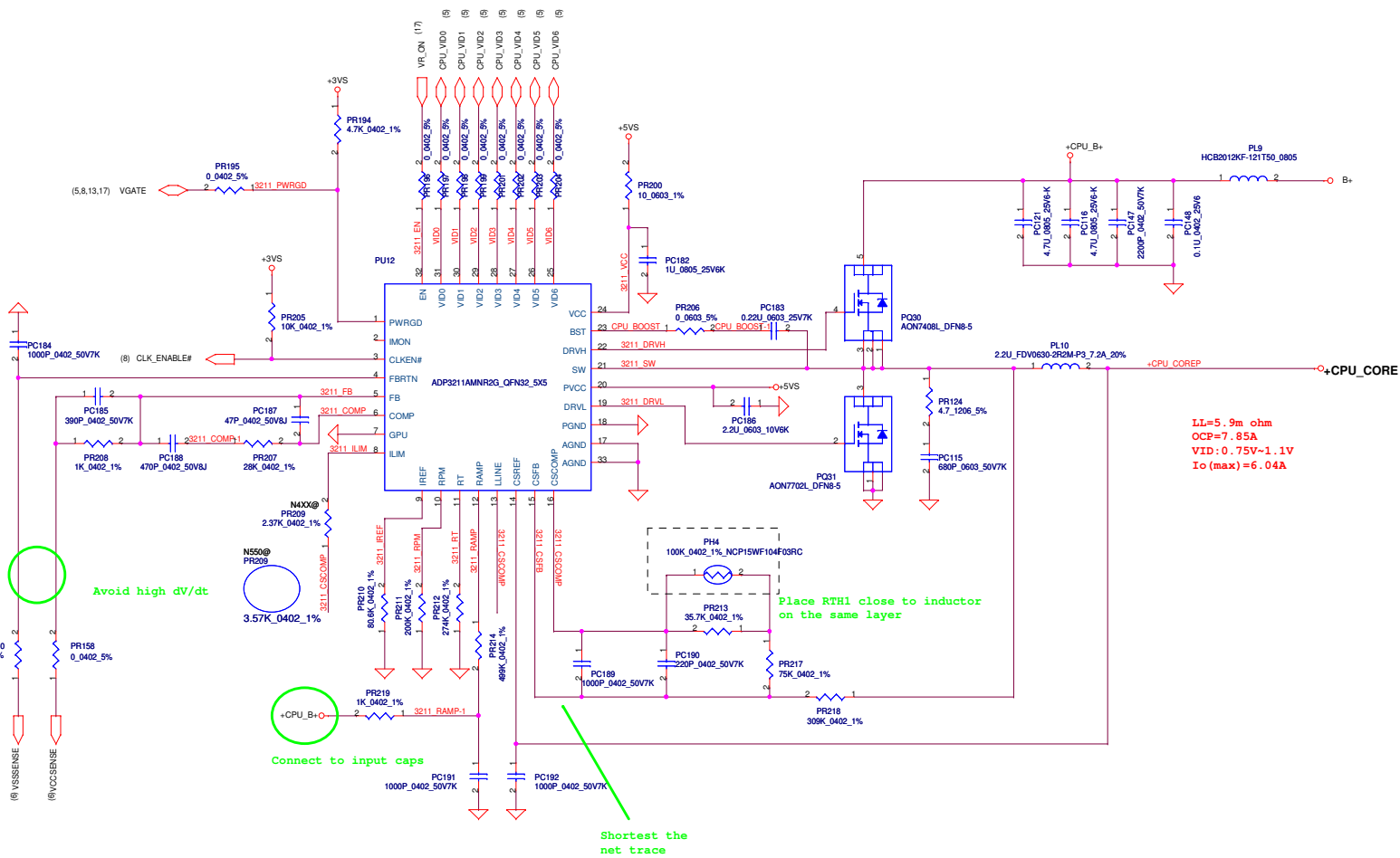


<Vo=1.8V> VFB=0.6V  
 $Vo = VFB * (1 + PR118 / PR120) = 0.6 * (1 + 124K / 61.9K) = 1.8V$   
 Ipeak=0.318A, Imax=0.223A



Ipeak=1A, Imax=0.7A

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LL=5.9m ohm  
 OCP=7.85A  
 VID: 0.75V~1.1V  
 Io(max)=6.04A

Place RTH close to inductor on the same layer

Connect to input caps

Shortest the net trace

Avoid high dV/dt

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change power solution	For design change	0.1	34	Change PU7 from SA000031D00(S IC RT8209BGQW WQFN 14P PWM) to SA00003RU00(S IC SY8033BDBC DFN 10P SINGLE BUCK)	2010.5.03	DVT
2	Change PU8 SY8033B Pin1 net	For design change	0.1	34	Change PU8 SY8033B Pin1 connect Pin2 & Pin3	2010.5.03	DVT
3	Change PC100	For design change	0.1	34	Change PC100 to SE071680J80 (S CER CAP 68P 50V J NPO 0402)	2010.5.03	DVT
4	Change PR105	For design change	0.1	32	Change PR105 from SD034100200(S RES 1/16W 10K +-1% 0402) to SD034100280 (S RES 1/16W 10K +-1% 0402 )	2010.5.13	DVT
5	Change PC30 & PC32 to non-pop	For cost down plan	0.1	33		2010.6.2	PVT
6	Change PL3,PL4,PL5,PL6,PL7,PL8, PL10,PL14	For TMP choke shortage issue	0.1		Change PL3,PL4,PL5 from SH00000JI00 to SH00000BS00 Change PL6,PL10 from SH00000FD10 to SH000000700 Change PL7,PL8 from SH00000J300 to SH000007N00 Change PL14 from SH00000IS00 to SH00000HY00	2010.6.2	PVT
7	Change power solution	For design change	0.1	34	Change PU7 from SA00003RU00(S IC SY8033BDBC DFN 10P SINGLE BUCK) to SA000031D00(S IC RT8209BGQW WQFN 14P PWM)	2010.6.8	PVT
8	Change PD10.PD13.PC58.PR64. PQ18 to non-pop Change PR84 to pop	For cost down plan	0.1	33		2010.6.10	PVT
9	Modify CPU CORE OCP for N550	Design change for N550 CPU	0.1	32	Add PR209 = SD034357180 (3.57K_0402_1%) @N550 PR209 = SD034357180 (2.37K_0402_1%) @N4XX series	2010.6.10	PVT
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				PIR (PWR)	
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
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<2010/03/25>  
. P06 - Add C1217, C1218 for +0.89V  
. P08 - Add R1442, R1443  
. P09 - Add R1444, R1445 for DMIC  
. P10 - L12, L14, L15 change to SM010000200  
. P23 - Add JP24 for cardreader connector

<2010/06/28>  
. P04 - Change C239 BOM structure to 3G@  
. P17 - Change C528, C530, C531 BOM structure to 3G@

<2010/03/26>  
. P27 - Add R1448, R1449, R1450,R1451,R1452  
JP22 change to SP02000H500

<2010/04/06>  
. P10 - Change L12. L14, L15 to SM01000C600  
. P26 - Add R1453  
. P21 - Change Y6 to SJ100005900  
. P25 - Change Y5 to SJ100003300  
Change C847,C865,C870,C873,C875,C876 SE000000K80  
. P13 - Change X1,Y3,Y7 to SJ132P7KW10  
. P22 - Change U26 to SA00001N000  
. P29 - Change Q6,Q8,Q10,Q12,Q14,Q17,Q24,Q28 to SB000000DH00  
Change C176,C219,C230,C395 to SE080105K80  
. P07 - Change C116,C141 to SE076104K80

<2010/04/14>  
. P06 - Del C1218 2010/04/14  
. P08 - Del C1219, R1442 change Y1 to SJ100009H00  
. P27 - Add TPM@ GSEN@ for PAV70

<2010/05/03>  
. P04 - R354, R347, R348 nu-mount  
. P13 - Change R152 to SD034226A80(22.6ohm\_0402)  
. P13 - Change R241 to SD028100280(10Kohm\_0402)  
. P13 - R1376, R1377 nu-mount  
. P16 - Add JBATT1 CONN.  
. P17 - Change U76 to SA00001V400  
. P17 - Change R1292 to SD028820180

<2010/05/04>  
. P16 - Change JBATT1 NET to +RTCBATT1  
. P27 - Add J15, J16

<2010/05/06>  
. P10 - Change L12, L14 and L15 footprint  
. P27 - Del J15, J16 ; Add R1457, R1458  
. P27 - U81.15 connect to GND

<2010/05/24>  
. P04 - Change U71 to SA00003WBA0(N475@) and SA00003WAB0(N455@)  
. P08 - Change C161, C164 to SE071330J80(33P 50V J NPO 0402)  
. P08 - Change C388 to SE071100J80(10P 50V J NPO 0402)  
. P22 - Change C473 to SE107475K80(4.7U 6.3V K X5R 0603)

<2010/06/01>  
. P13 - Add NET: EC\_CLK  
. P17 - Add R1459, R1460 for Reserve EC\_CLK  
. P17 - Change U6.36 NET to PWR\_LED1#  
. P18 - Change NET from PWR\_LED# to PWR\_LED1#

<2010/06/07>  
. P06 - Change C239 footprint to 0805 size  
. P17 - Del JP23  
. P26 - Change R1325 to 100k-ohm

<2010/06/25>  
. P04 - Change C311 BOM configure to un-mount  
. P09 - Change C1109, C1111, C1112, C1156 BOM configure to 3G@  
. P15 - Change C1163~C1166, C504~C508, C850 BOM configure to MCP@  
. P17 - Change C528, C530, C531 BOM configure to un-mount  
. P10 - Change D17, D18 BOM configure to un-mount  
. P22 - Change D22 BOM configure to un-mount  
. P23 - Change D44, D45 BOM configure to un-mount

Title			
<Title>			
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