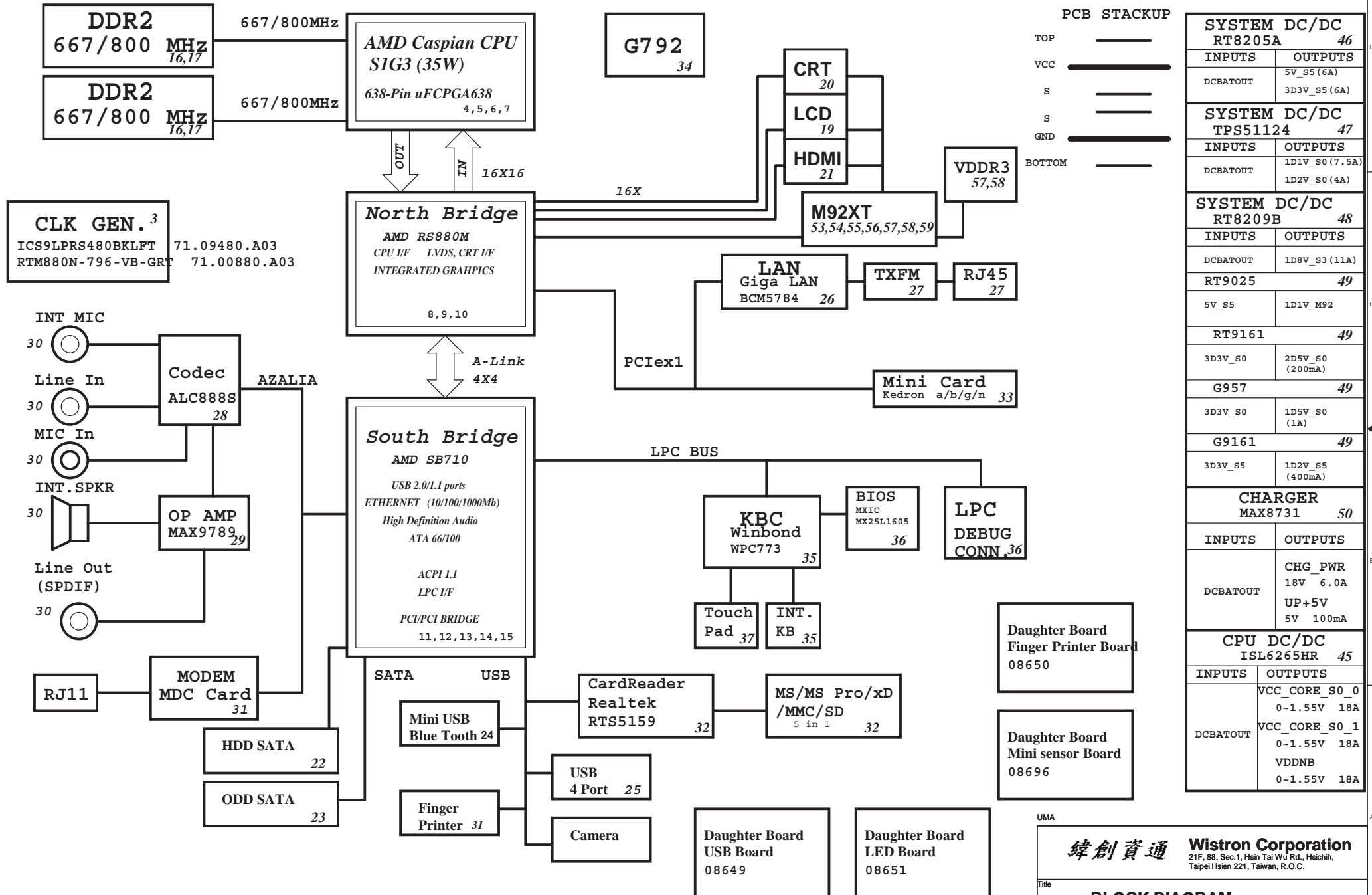


JV71-TR Block Diagram

Project code: 91.4FP01.001

PCB P/N : 48.4FP02.0SB

REVISION : 09243-SB



PCB STACKUP

TOP	_____
VCC	_____
S	_____
S	_____
GND	_____
BOTTOM	_____

SYSTEM DC/DC RT8205A 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (6A)
	3D3V_S5 (6A)
SYSTEM DC/DC TPS51124 47	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0 (7.5A)
	1D2V_S0 (4A)
SYSTEM DC/DC RT8209B 48	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 (11A)
	RT9025 49
5V_S5	1D1V_M92
	RT9161 49
3D3V_S0	2D5V_S0 (200mA)
	G957 49
3D3V_S0	1D5V_S0 (1A)
	G9161 49
3D3V_S5	1D2V_S5 (400mA)
CHARGER MAX8731 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A
	UP+5V 5V 100mA
CPU DC/DC ISL6265HR 45	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A
	VCC_CORE_S0_1 0~1.55V 18A
	VDDNB 0~1.55V 18A

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Title: **BLOCK DIAGRAM**

Size: A3 Document Number: **JV71-TR** Rev: **SB**

Date: Monday, July 06, 2009 Sheet 1 of 61

5

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USB/PCIE Routing	
Title USB/PCIE Routing	Rev SA
Size A3	Document Number JV71-TR
Date: Monday, July 06, 2009	Sheet 2 of 61

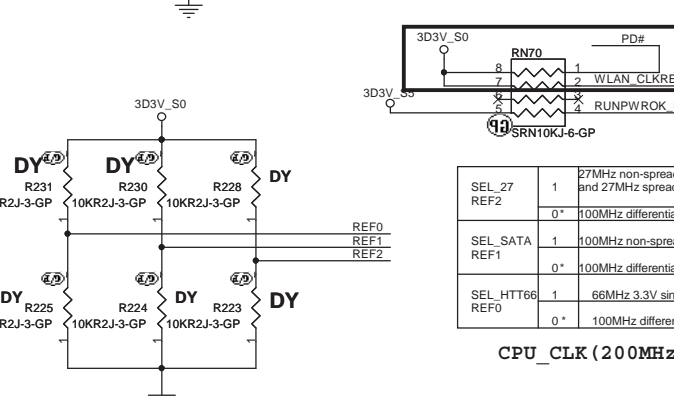
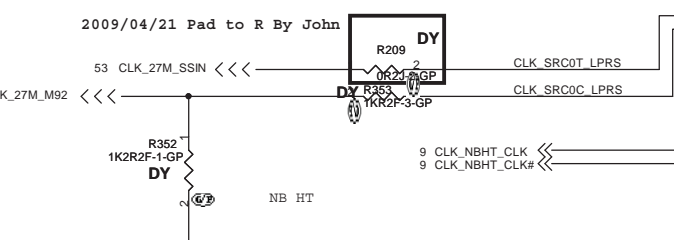
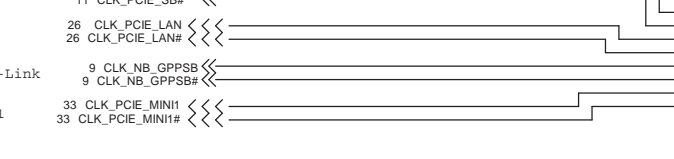
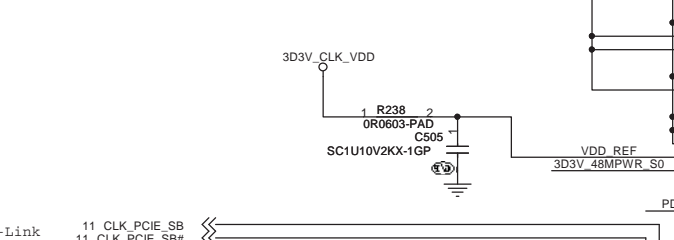
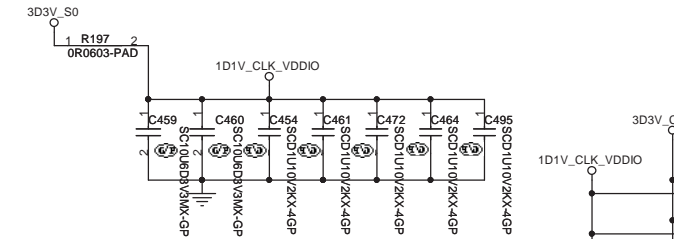
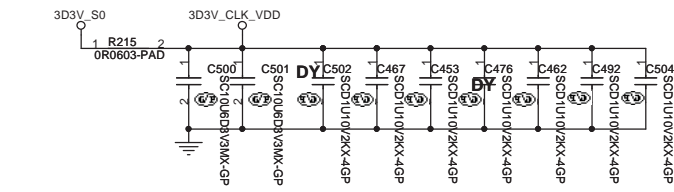
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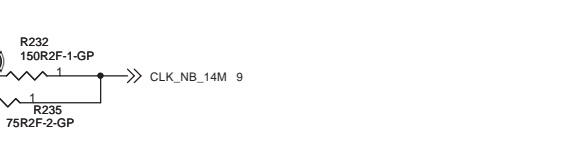
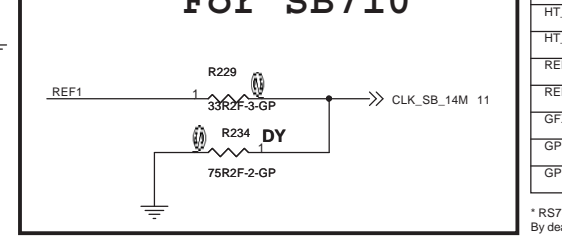
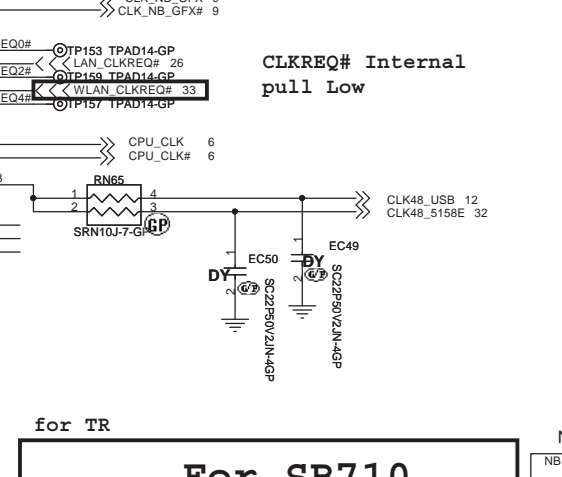
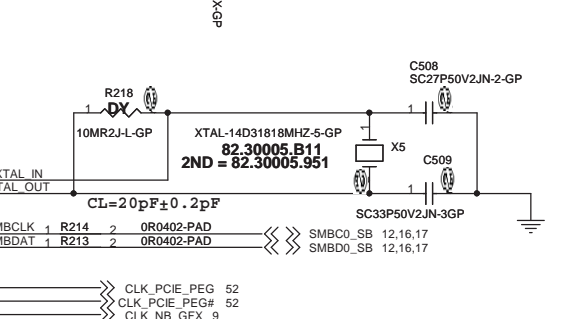
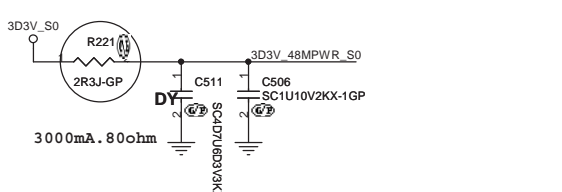


SEL_27	REF2	1	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
SEL_SATA	REF1	0*	100MHz differential spreading SRC clock
SEL_SATA	REF0	1	100MHz non-spreading differential SATA clock
SEL_HTT66	REF0	0*	100MHz differential spreading SRC clock
SEL_HTT66	REF0	1	66MHz 3.3V single ended HTT clock
SEL_HTT66	REF0	0*	100MHz differential HTT clock

CPU_CLK (200MHz)

OSC 14M NB
RS780M 1.1V 158R/90.9R

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Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIe reference clocks. By default, chip will configured as input mode, BIOS can program it to output mode.

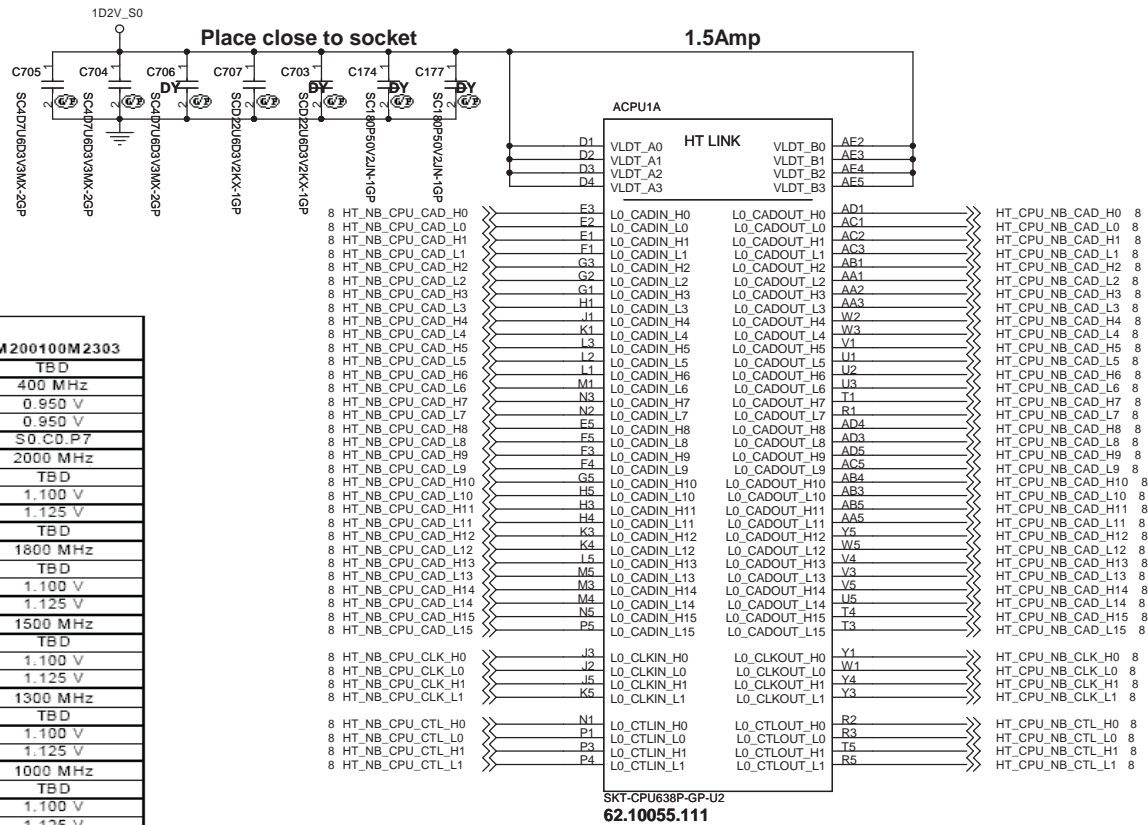
UMA

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Title: **CLKGEN ICS9LPRS480**

Size: **A3** Document Number: **JV71-TR** Rev: **SB**

Date: **Monday, July 06, 2009** Sheet **3** of **61**



State	Specification	Notes	ZM200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1500 MHz
S0.C0.P2	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1300 MHz
	TDP	3	TBD
S0.C0.P3	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
S0.C0.P4	VID_VDD Max	2	1.125 V
	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
S0.C0.P6	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
S0.C0.P7	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

SKT-BGA638H176

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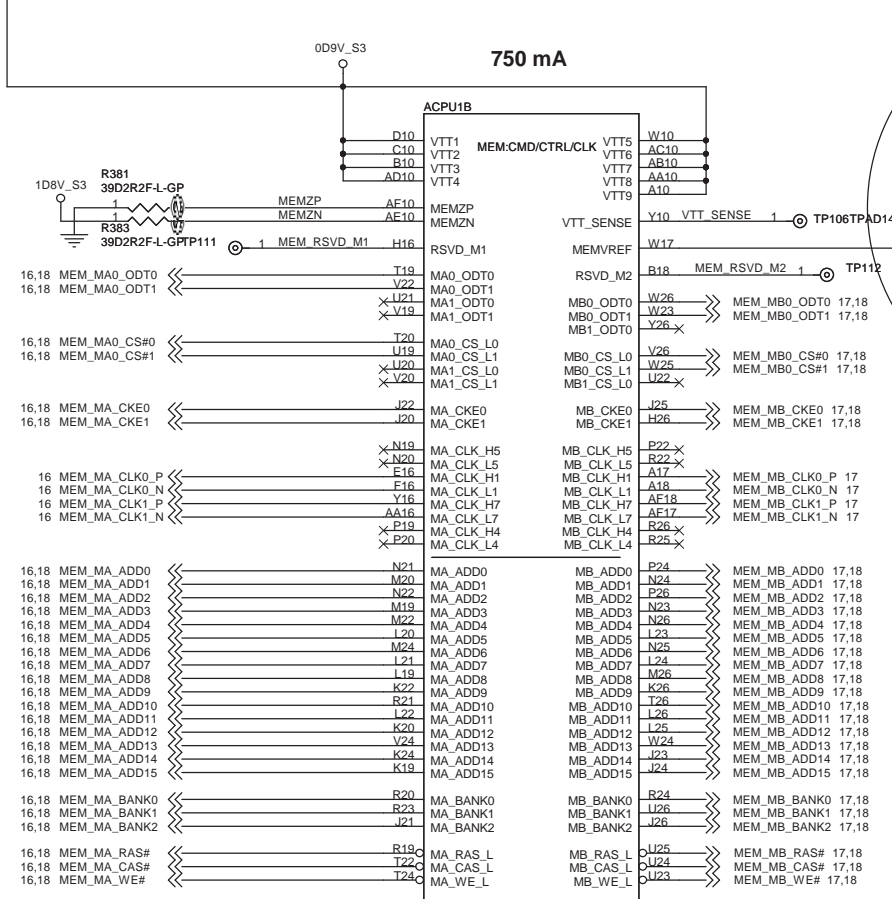
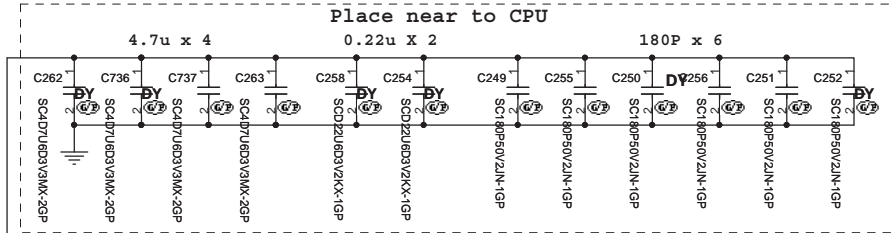
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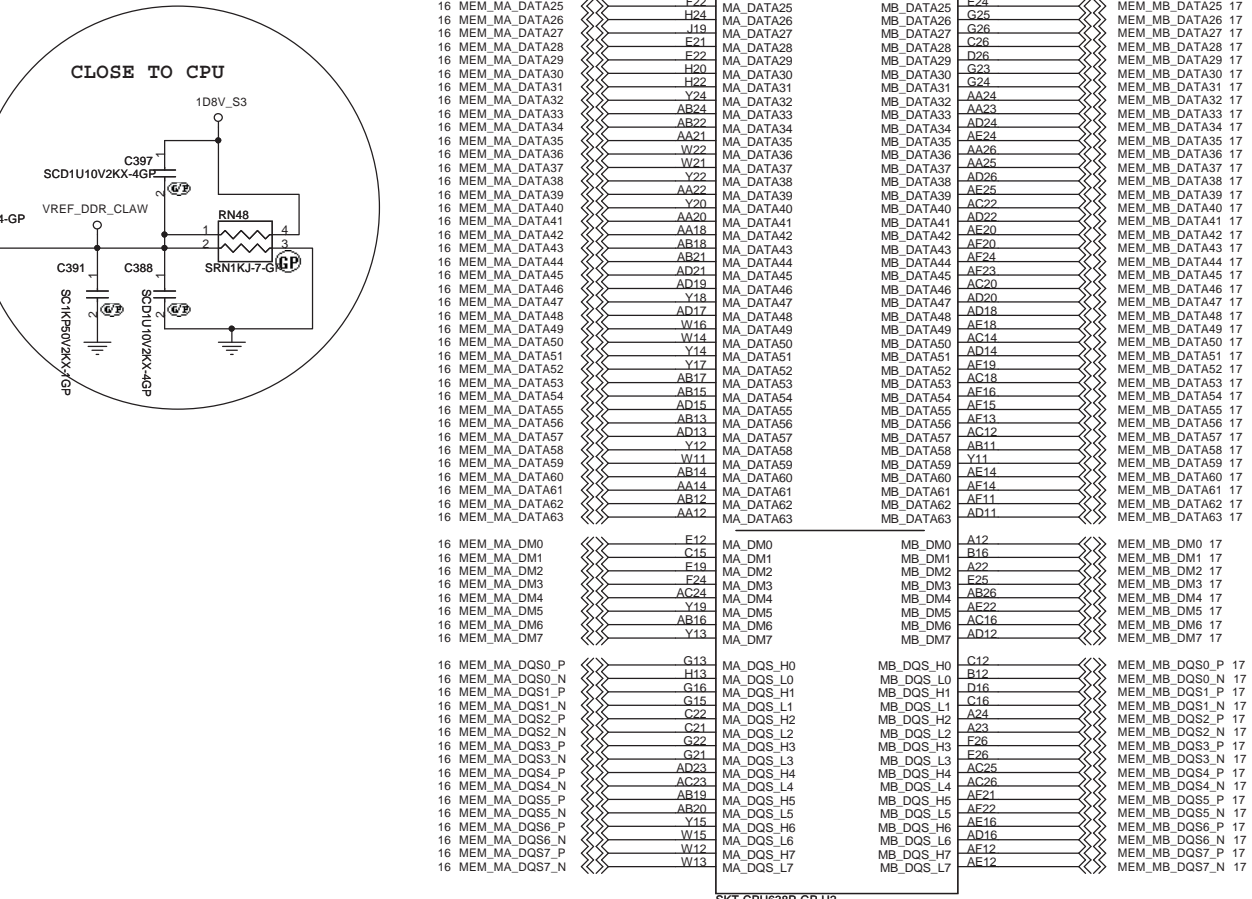
Title: **CPU HT LINK I/F (1/4)**

Size: **A3** Document Number: **JV71-TR** Rev: **SA**

Date: Monday, July 06, 2009 Sheet 4 of 61



SKT-CPU638P-GP-U2
62.10055.111



SKT-CPU638P-GP-U2
62.10055.111

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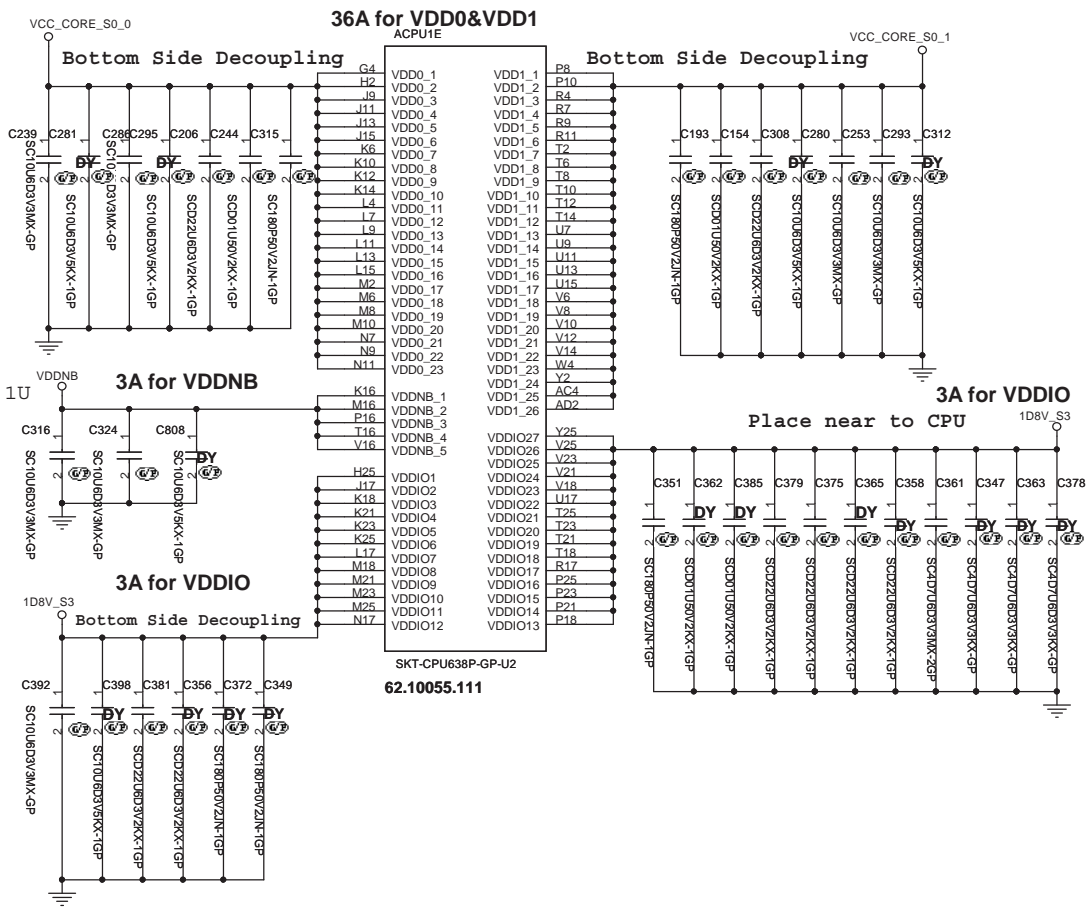
Title: CPU DDR (2/4)

Size: A3 Document Number: JV71-TR Rev: SA

Date: Monday, July 06, 2009 Sheet 5 of 61

ACPU1F		
AA4	VSS1	VSS66
AA11	VSS2	VSS67
AA13	VSS3	VSS68
AA15	VSS4	VSS69
AA17	VSS5	VSS70
AA19	VSS6	VSS71
AB2	VSS7	VSS72
AB7	VSS8	VSS73
AB9	VSS9	VSS74
AB23	VSS10	VSS75
AB25	VSS11	VSS76
AC11	VSS12	VSS77
AC13	VSS13	VSS78
AC15	VSS14	VSS79
AC17	VSS15	VSS80
AC19	VSS16	VSS81
AC21	VSS17	VSS82
AD6	VSS18	VSS83
AD8	VSS19	VSS84
AD25	VSS20	VSS85
AE11	VSS21	VSS86
AE13	VSS22	VSS87
AE15	VSS23	VSS88
AE17	VSS24	VSS89
AE19	VSS25	VSS90
AE21	VSS26	VSS91
AE23	VSS27	VSS92
B4	VSS28	VSS93
B6	VSS29	VSS94
B8	VSS30	VSS95
B9	VSS31	VSS96
B11	VSS32	VSS97
B12	VSS33	VSS98
B15	VSS34	VSS99
B17	VSS35	VSS100
B19	VSS36	VSS101
B21	VSS37	VSS102
B23	VSS38	VSS103
B25	VSS39	VSS104
D6	VSS40	VSS105
D9	VSS41	VSS106
D11	VSS42	VSS107
D13	VSS43	VSS108
D15	VSS44	VSS109
D17	VSS45	VSS110
D19	VSS46	VSS111
D21	VSS47	VSS112
D23	VSS48	VSS113
D25	VSS49	VSS114
F4	VSS50	VSS115
F2	VSS51	VSS116
F11	VSS52	VSS117
F13	VSS53	VSS118
F15	VSS54	VSS119
F17	VSS55	VSS120
F19	VSS56	VSS121
F21	VSS57	VSS122
F23	VSS58	VSS123
F25	VSS59	VSS124
H7	VSS60	VSS125
H9	VSS61	VSS126
H21	VSS62	VSS127
H23	VSS63	VSS128
J4	VSS64	VSS129
	VSS65	VSS129

SKT-CPU638P-GP-U2
62.10055.111



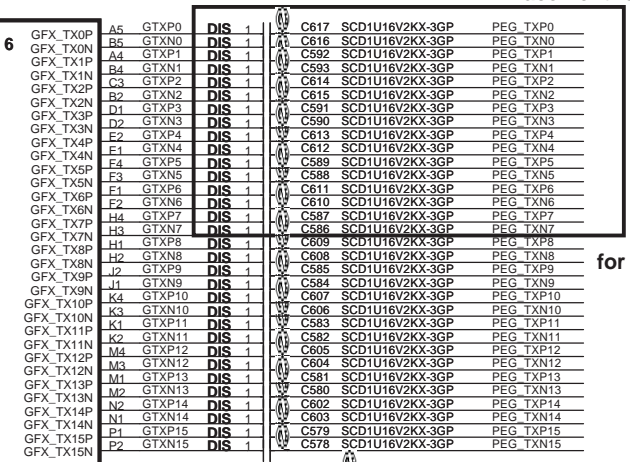
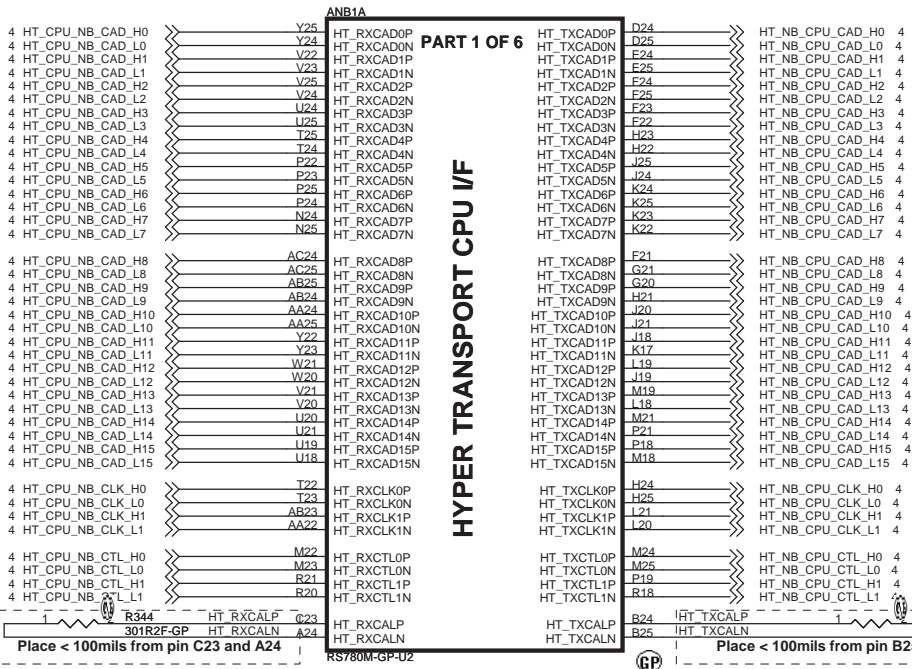
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Title: **CPU_Power_(4/4)**

Size: A3	Document Number: JV71-TR	Rev: SA
Date: Monday, July 06, 2009	Sheet 7 of 61	



Place < 100mils from pin B25 and B24

RS780M Display Port Support (muxed on GFX)

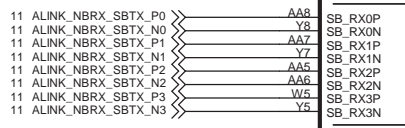
DP0	GFX_TX0, TX1, TX2, TX3, AUX0, HPD0
DP1	GFX_TX4, TX5, TX6, TX7, AUX1, HPD1

GTXP0	LIMA	C30	1	SCD1U16V2KX-3GP	HDMI DATA2+
GTXN0	LIMA	C29	1	SCD1U16V2KX-3GP	HDMI DATA2-
GTXP1	LIMA	C27	1	SCD1U16V2KX-3GP	HDMI DATA1+
GTXN1	LIMA	C26	1	SCD1U16V2KX-3GP	HDMI DATA1-
GTXP2	LIMA	C25	1	SCD1U16V2KX-3GP	HDMI DATA0+
GTXN2	LIMA	C22	1	SCD1U16V2KX-3GP	HDMI DATA0-
GTXP3	LIMA	C21	1	SCD1U16V2KX-3GP	HDMI_CLK+
GTXN3	LIMA	C19	1	SCD1U16V2KX-3GP	HDMI_CLK-

LAN 26
 MINICARD1 33

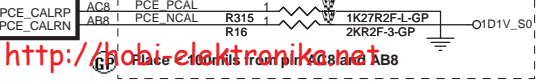
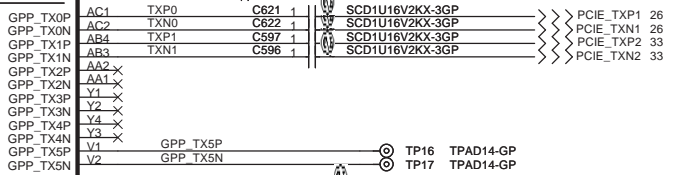
TPAD14-GP TP21
 TPAD14-GP TP20

A-LINK



PCIE I/F GPP

PCIE I/F SB

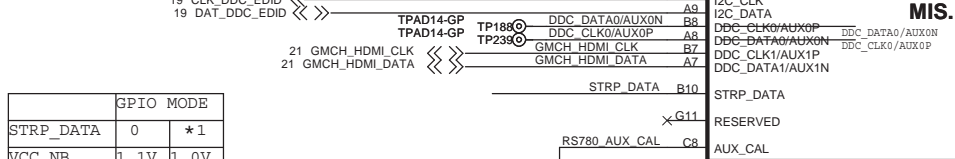
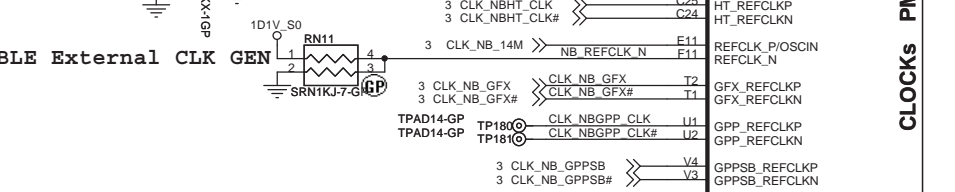
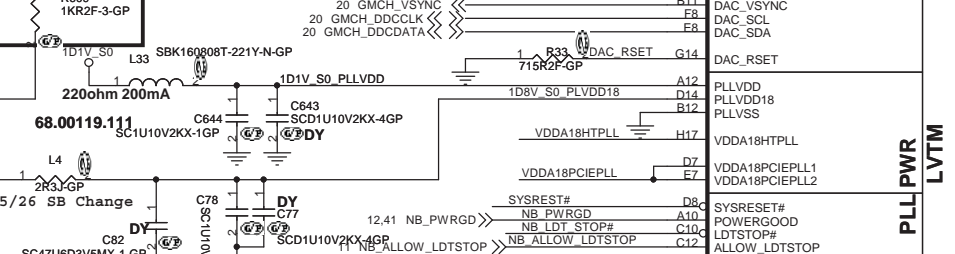
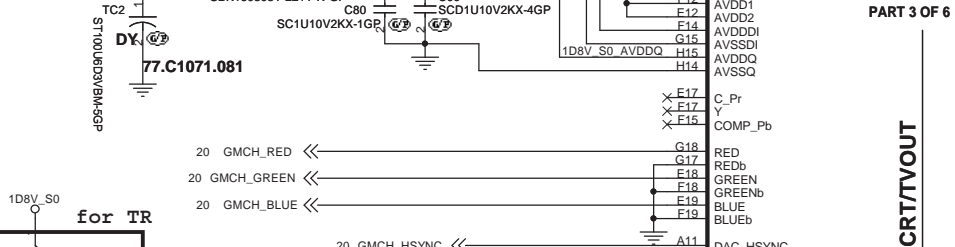
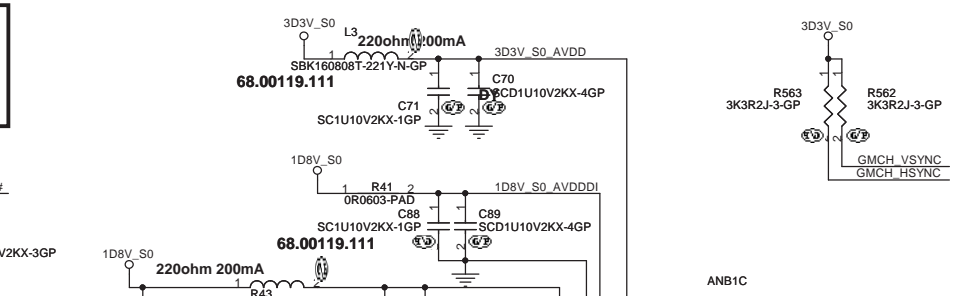
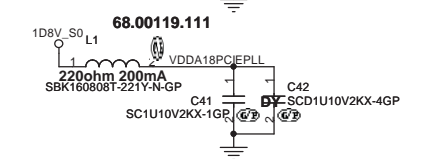
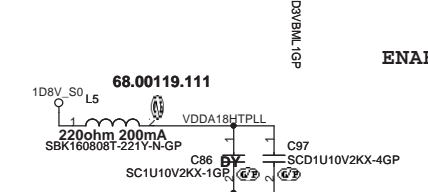
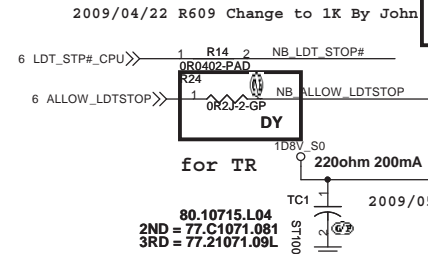
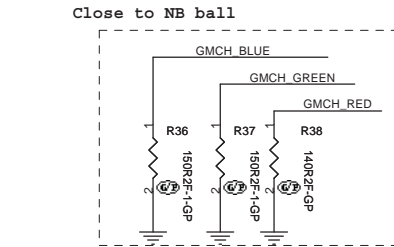
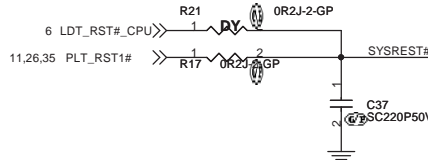


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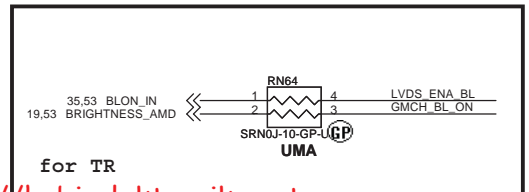
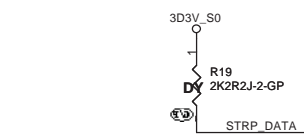
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Title		ATI-RS880M_HT LINK&PCIe(1/3)	
Size	Document Number	Rev	
A3	JV71-TR	SA	
Date:	Monday, July 06, 2009	Sheet	8 of 61

Reserve for DY
EMI
0408



GPIO MODE		
STRP_DATA	0	* 1
VCC_NB	1.1V	1.0V

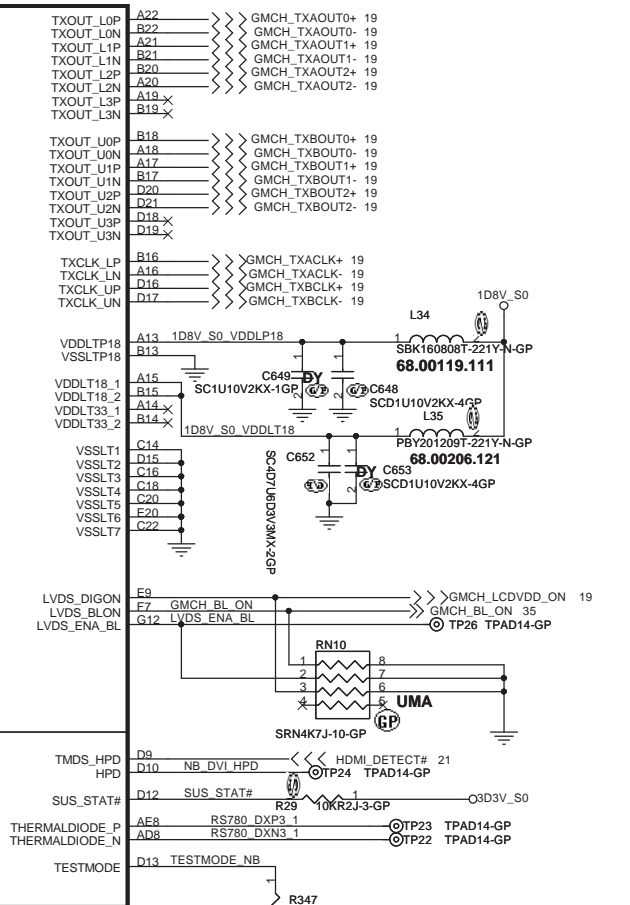


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STRAP_DEBUG_BUS_GPIO_ENABLEB
Enables the Test Debug Bus using GPIO. (PIN: RS780M--> VSYNC#)
* 1 :Disable 0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)
* 1 :Disable 0 : Enable

SUS_STAT#
Selects loading of STRAPS from EEPROM
* 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected



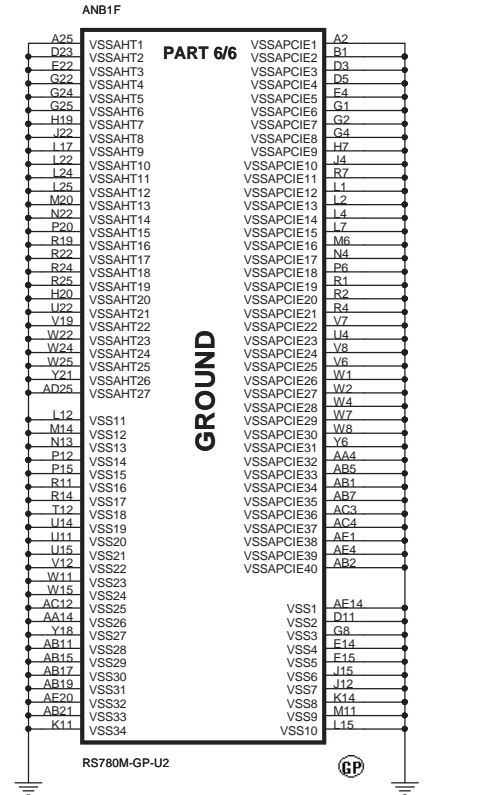
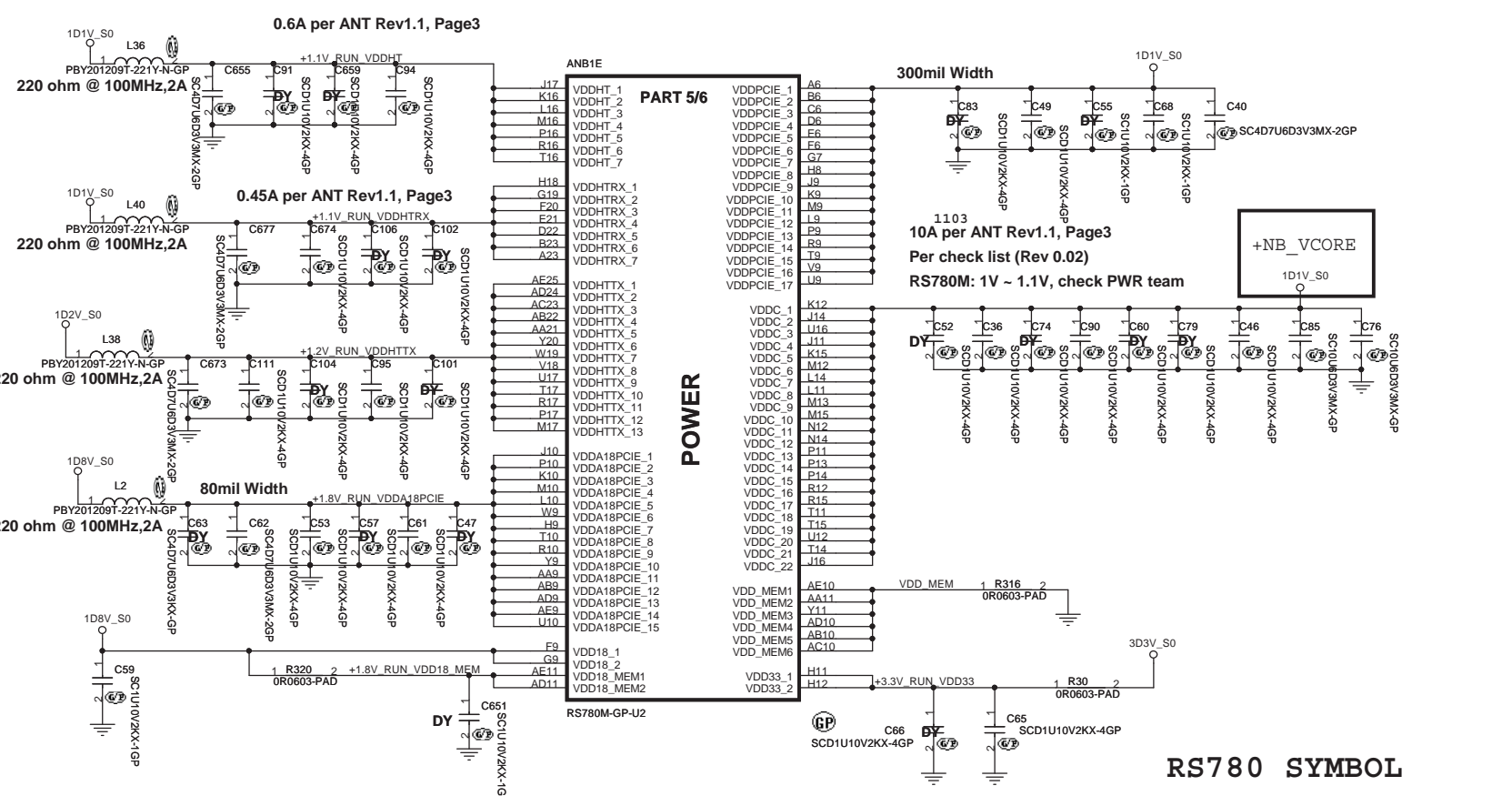
RS780 SYMBOL

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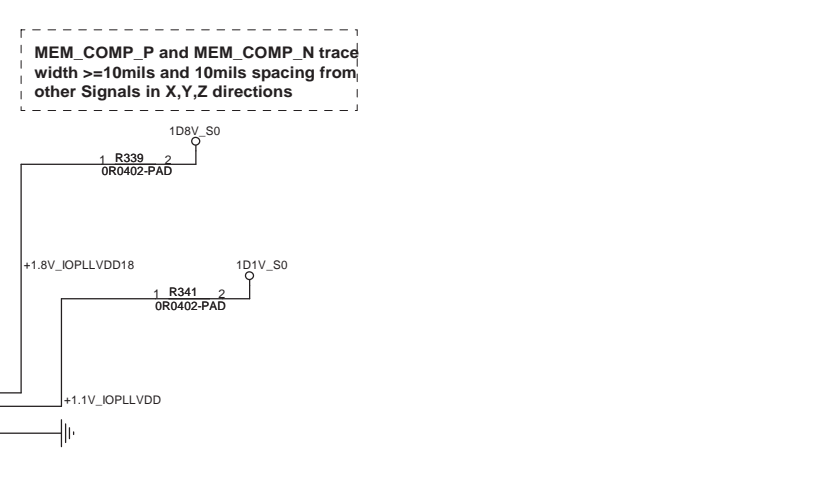
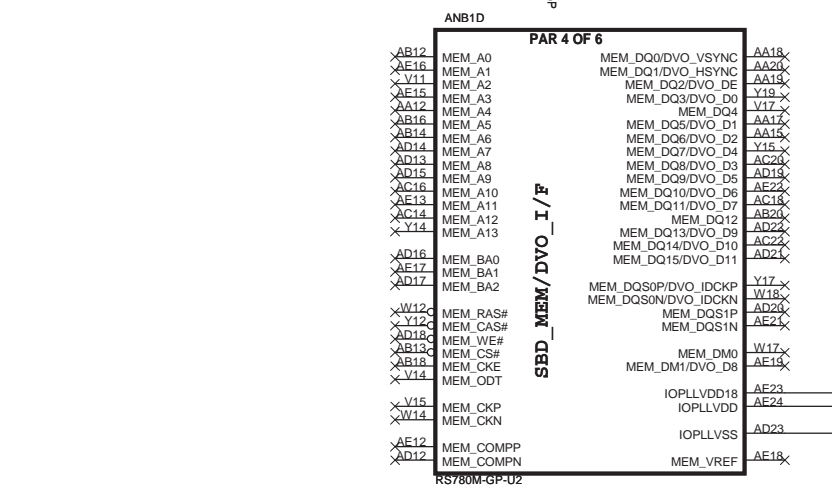
Title: **ATI-RS880M LVDS&CRT (2/3)**

Size A3 Document Number **JV71-TR** Rev SA

Date: Monday, July 06, 2009 Sheet 9 of 61



RS780 SYMBOL



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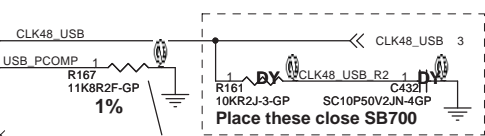
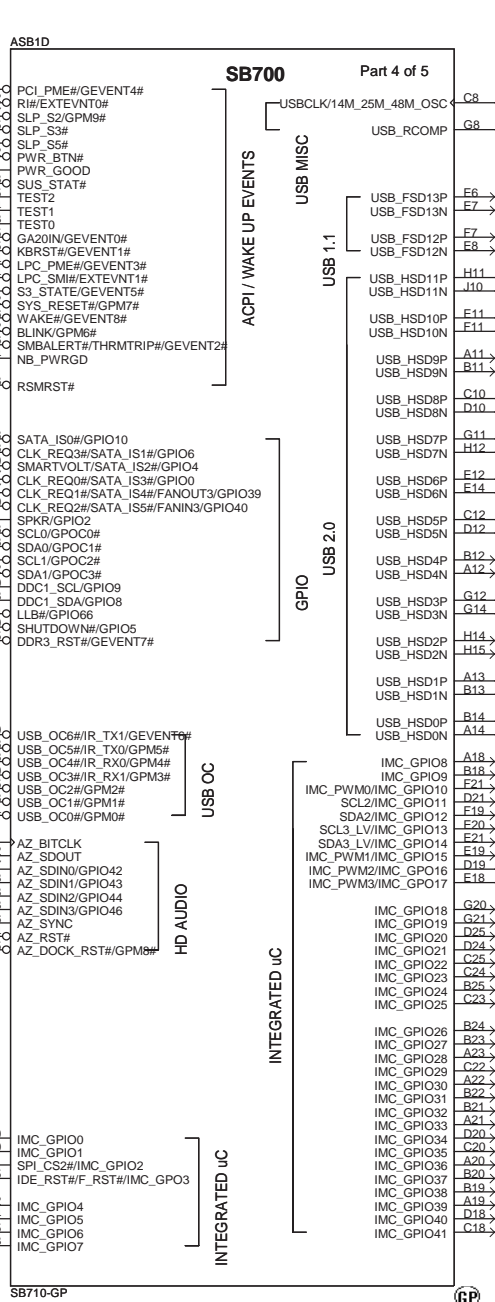
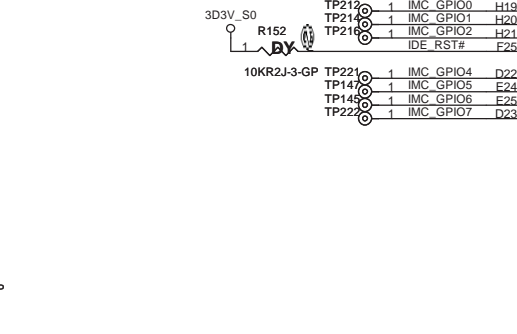
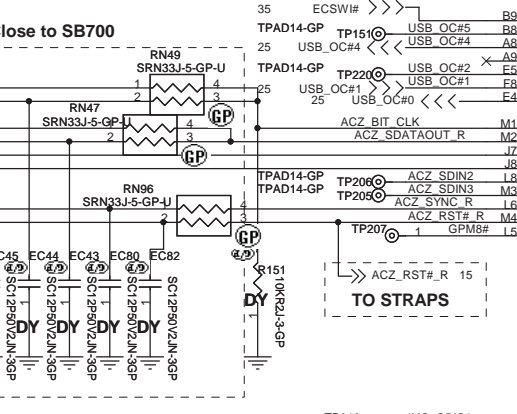
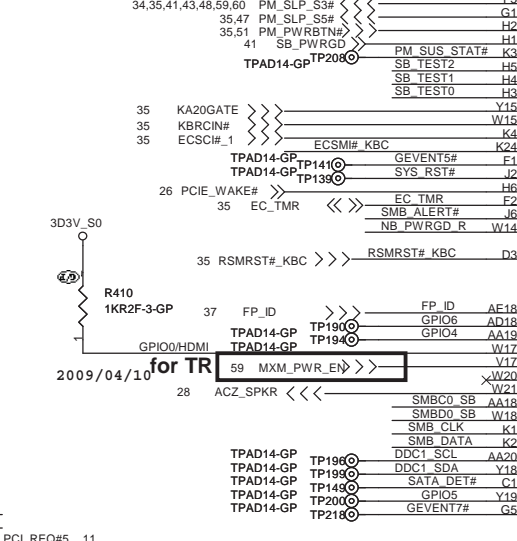
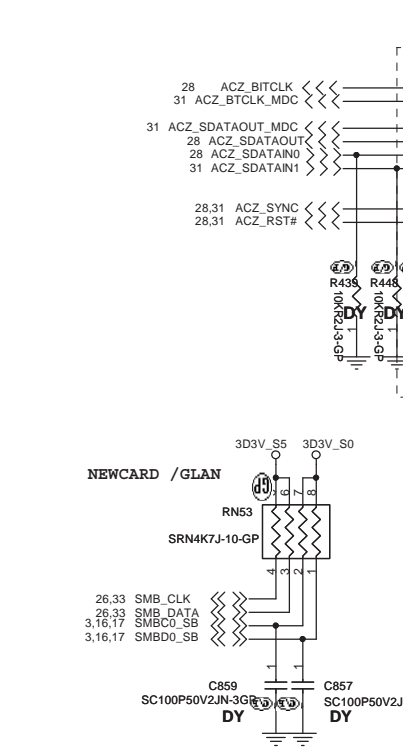
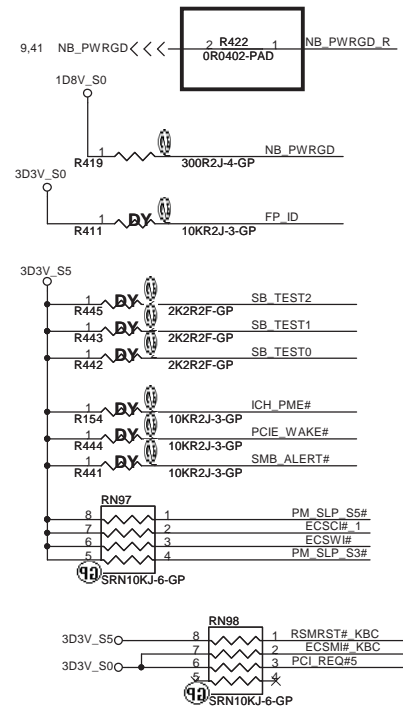
緯創資通 Wistron Corporation
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Title: **Ati-RS880M Side Port&PWR&GND(3/3)**

Size: A3 Document Number: **JV71-TR** Rev: SA

Date: Monday, July 06, 2009 Sheet 10 of 61

Reserve for DY
EMI
0408



Place R near pin14. Route it with 10mils
Trace width and 25mils spacing to any
signals in X, Y, Z directions.

USB	
Pair	Device
11	CardReader
10	WEBCAM
9	NC
8	USB2
7	USBCN1
6	USB1
5	Bluetooth
4	NC
3	Fringier print
2	NC
1	MINIC1
0	USB3

OCP1#
OCP0#

Strap Pin / define to use LPC or SPI ROM

UMA

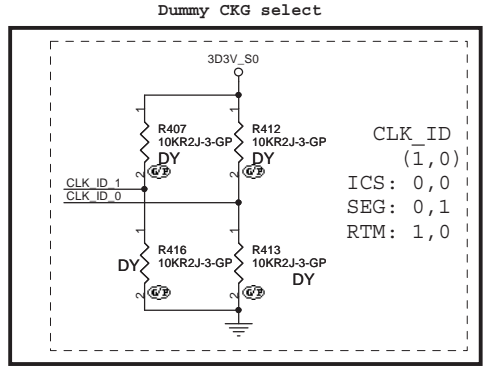
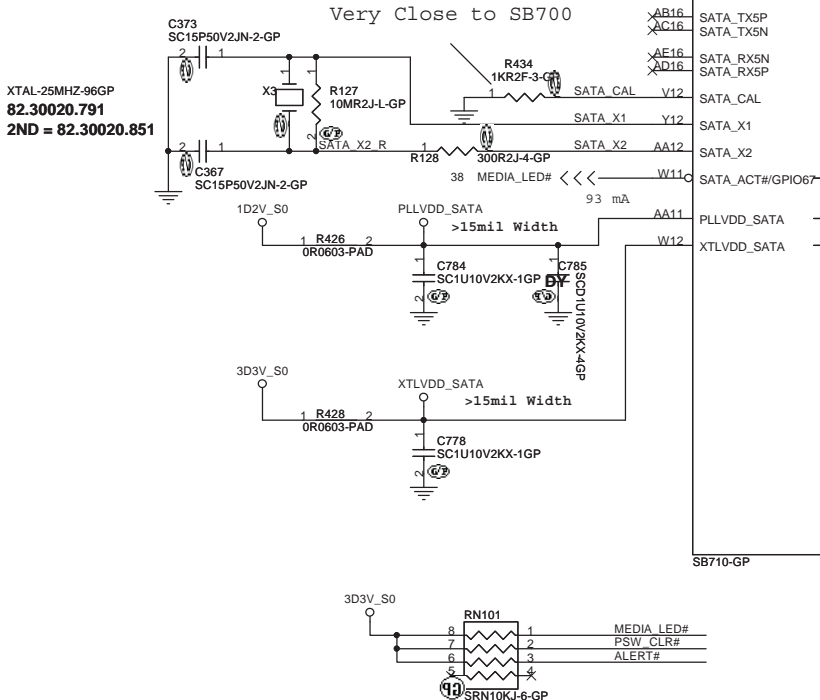
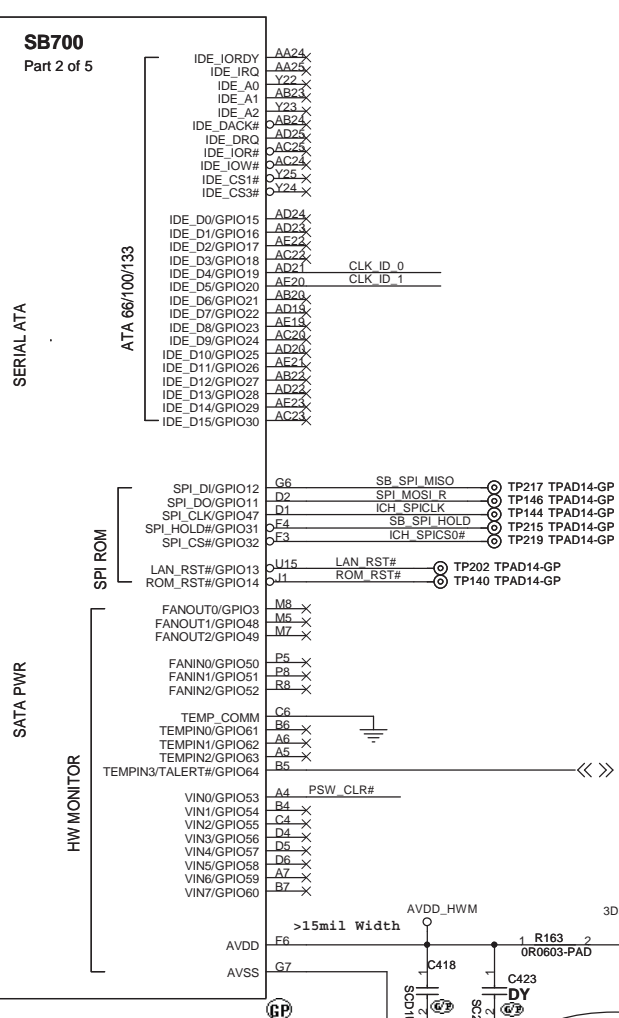
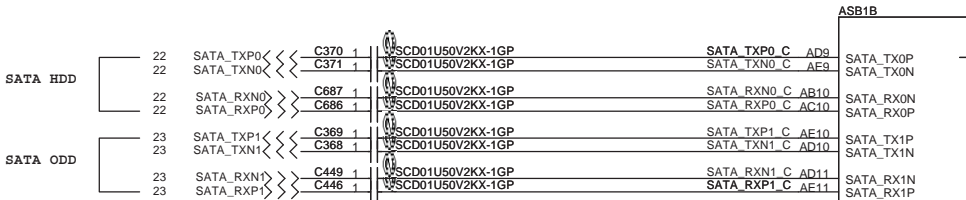
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-SB710 USB&GPIO (2/5)**

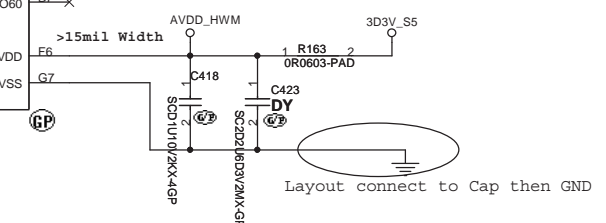
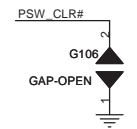
Size A3 Document Number **JV71-TR** Rev SA

Date: Monday, July 06, 2009 Sheet 12 of 61

PLACE SATA AC DECOUPLING CAPS CLOSE TO SB700



2009/04/09 ALL DY



<http://hobi-elektronika.net>

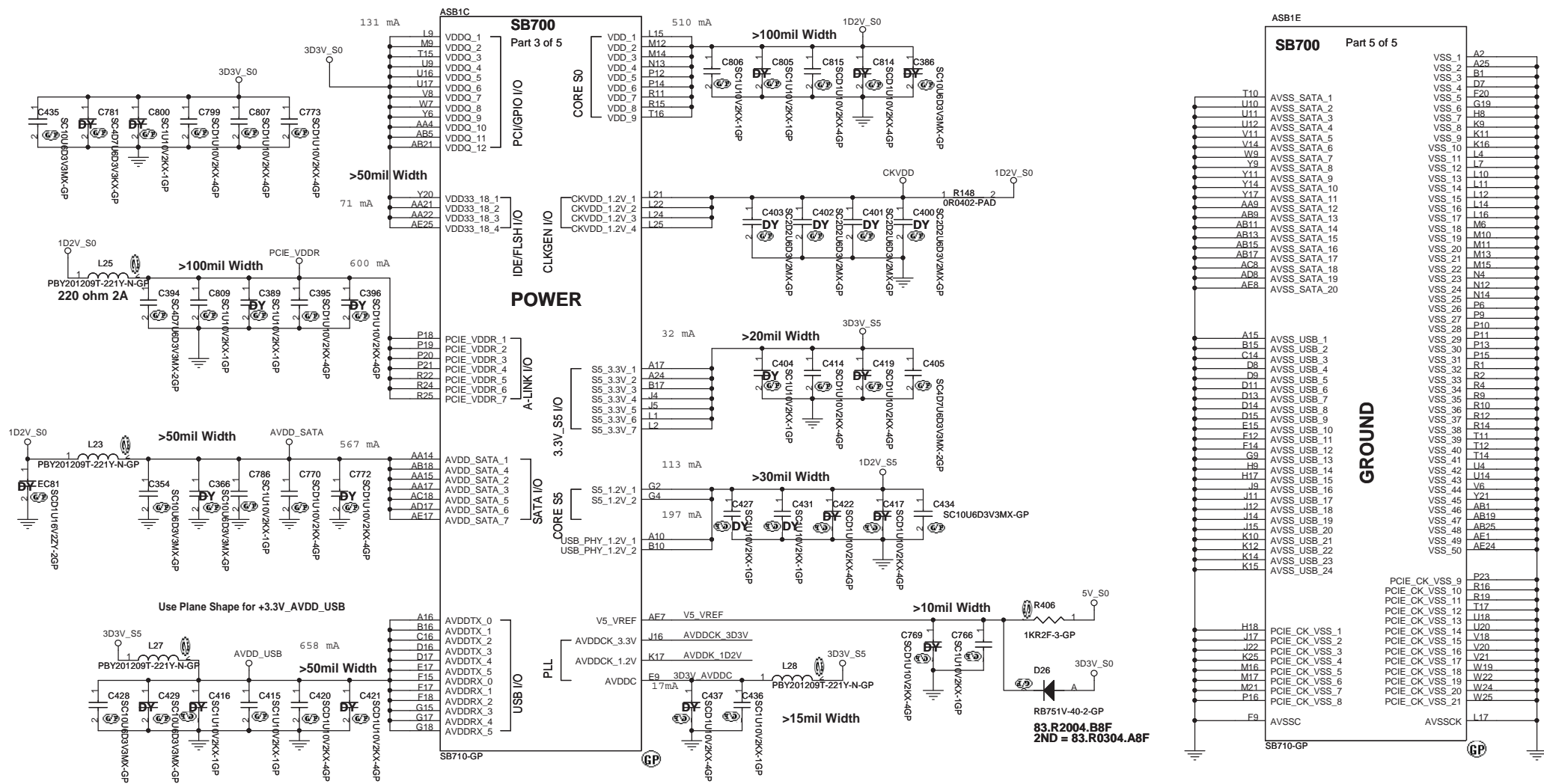
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATi-SB710 SATA-IDE (3/5)**

Size: A3 Document Number: **JV71-TR** Rev: SB

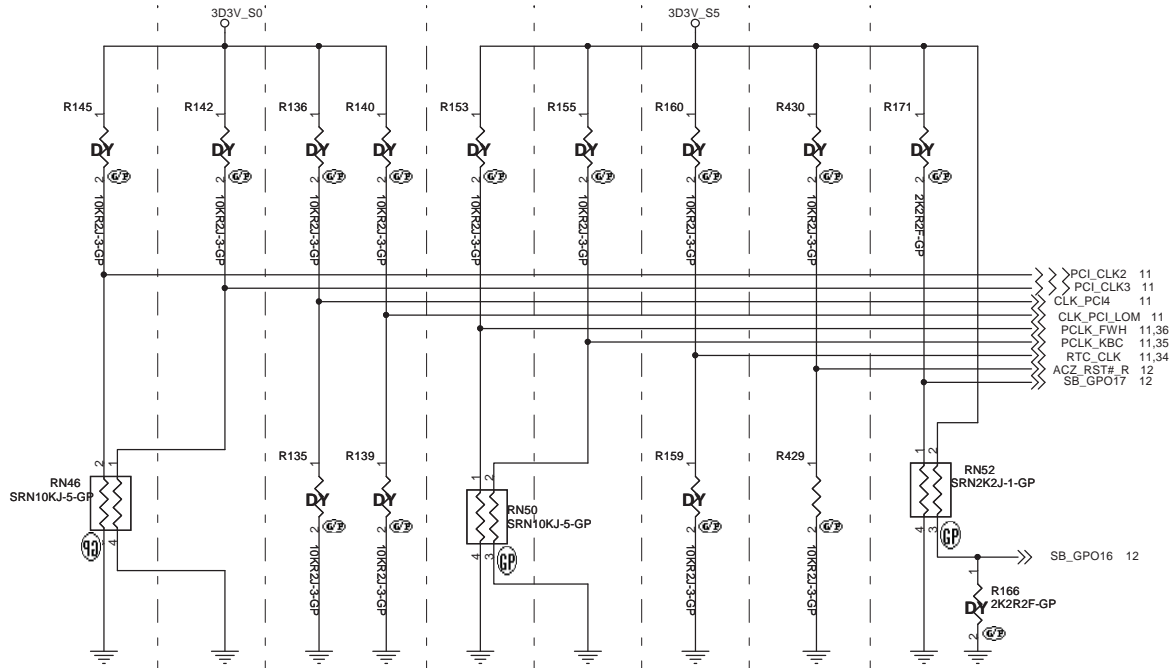
Date: Monday, July 06, 2009 Sheet 13 of 61



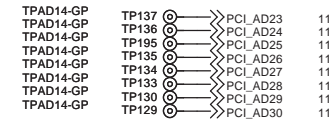
<http://hobi-elektronika.net>

緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ATi-SB710 POWER&GND (4/5)	
Size: A3	Document Number: JV71-TR
Date: Monday, July 06, 2009	Rev: SB
Sheet: 14	of: 61

REQUIRED STRAPS REQUIRED SYSTEM STRAPS



DEBUG STRAPS



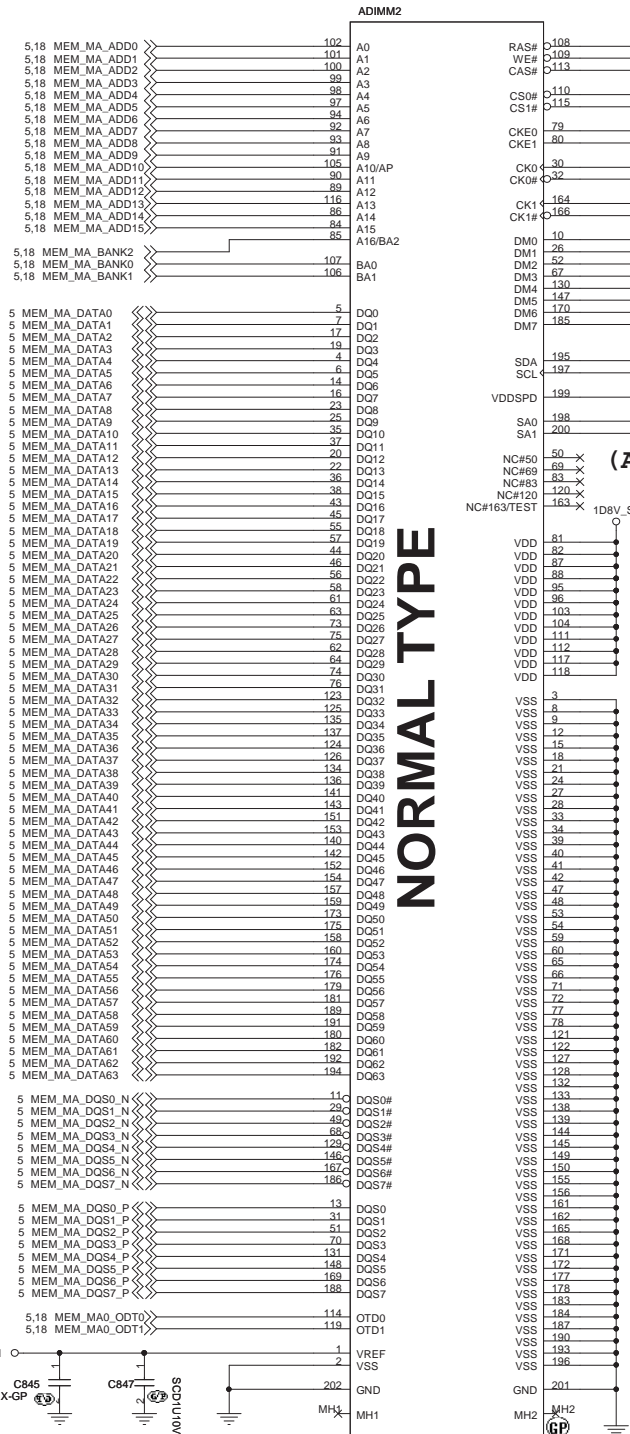
	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17, SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM DEFAULT L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

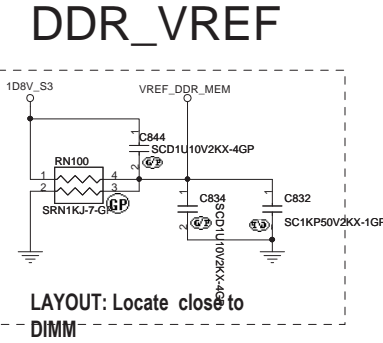
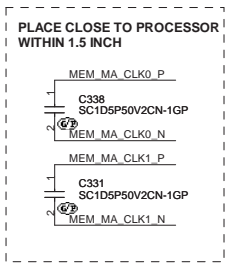
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

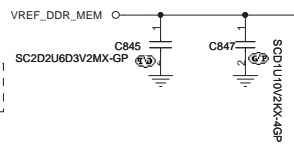
UMA



NORMAL TYPE



Place C2.2uF and 0.1uF < 500mils from DDR connector



SKT-SODIMM20020U4GP
 62.10017.661
 2ND = 62.10017.A41
 3RD = 62.10017.G81

LOW 5.2 mm

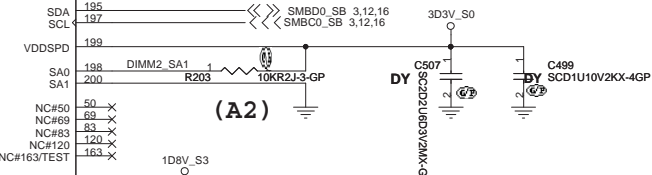
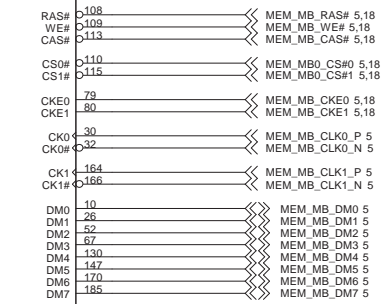
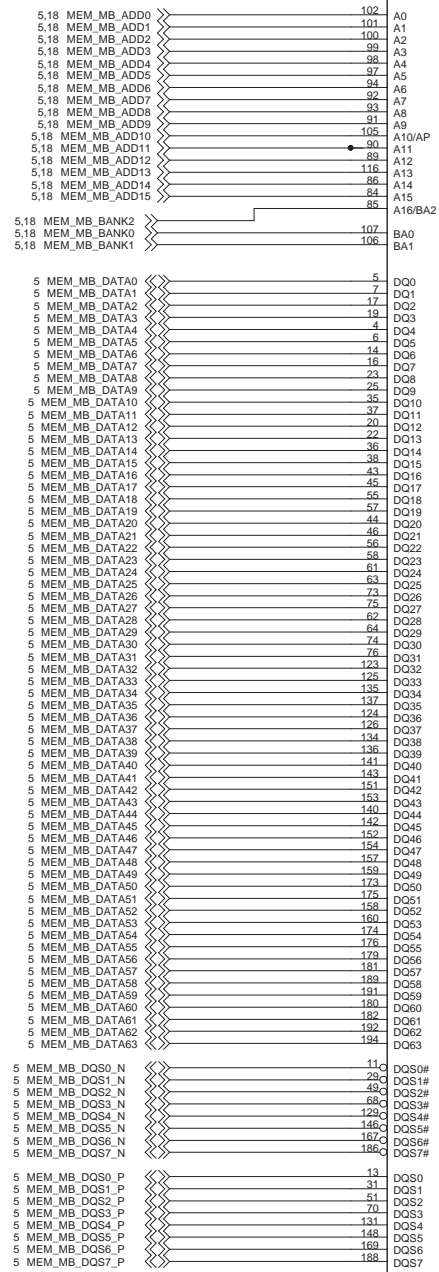
UMA

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

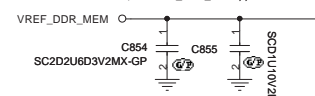
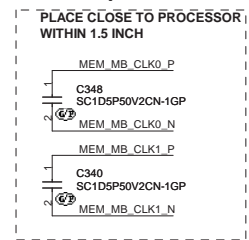
Title: **DDR SO-DIMM SKT_1**

Size: Custom Document Number: **JV71-TR** Rev: **SB**

Date: Monday, July 06, 2009 Sheet: 16 of 61



NORMAL TYPE



Place C2.2uF and 0.1uF < 500mils from DDR connector

SKT-SODIMM200-37GP
62-10017.E21
2ND = 62-10017.A51
3RD = 62-10017.G7

HI 9.2mm
<http://hobi-elektronika.net>

UMA

緯創資通 Wistron Corporation
2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

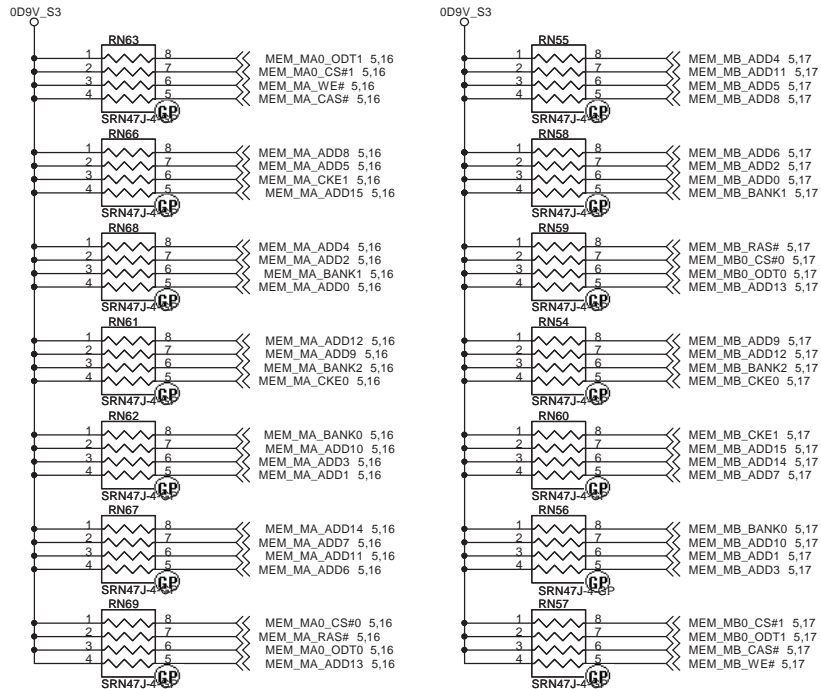
Title: **DDR SO-DIMM SKT 2**

Size: Custom Document Number: **JV71-TR** Rev: **SB**

Date: Monday, July 06, 2009 Sheet 17 of 61

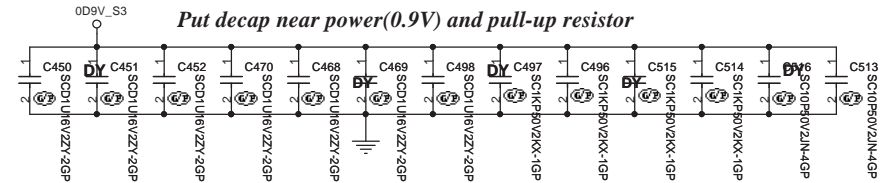
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

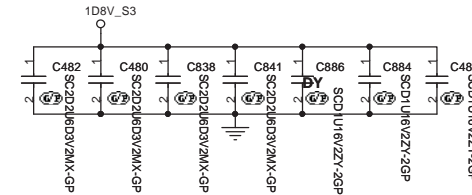


Do not share the Term resistor between the DDR address and Control Signals.

Decoupling Capacitor

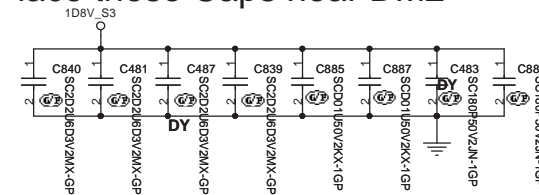


Place these Caps near DM1



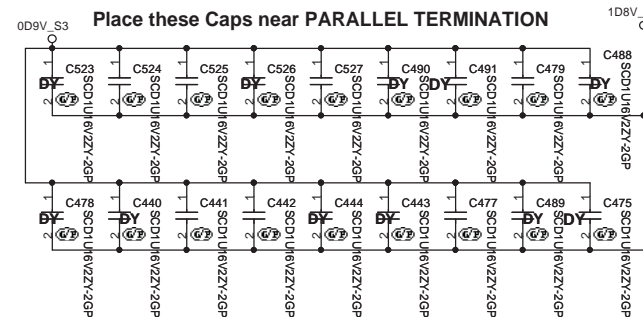
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



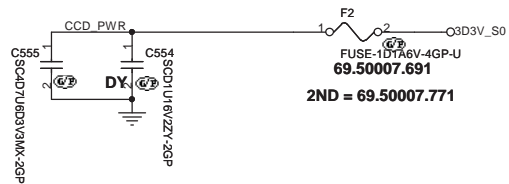
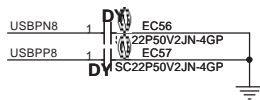
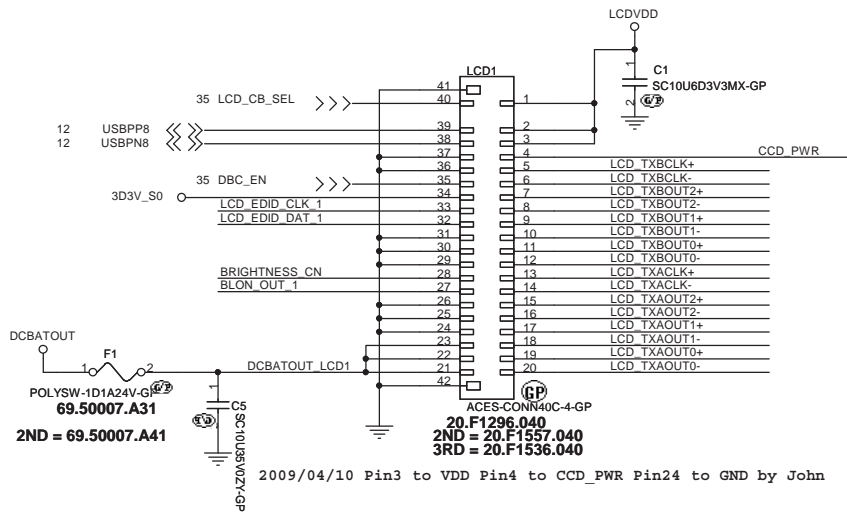
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION

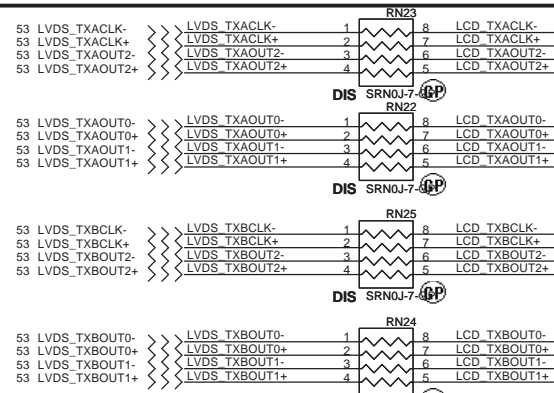
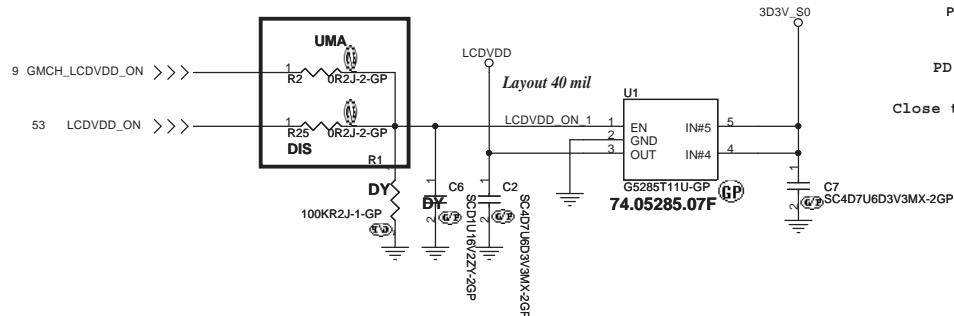


LCD/INVERTER/CCD CONN

for TR

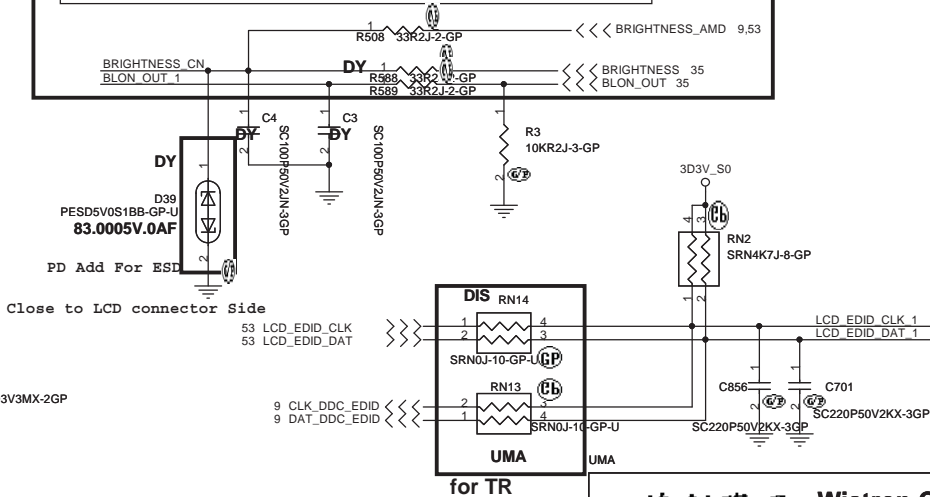
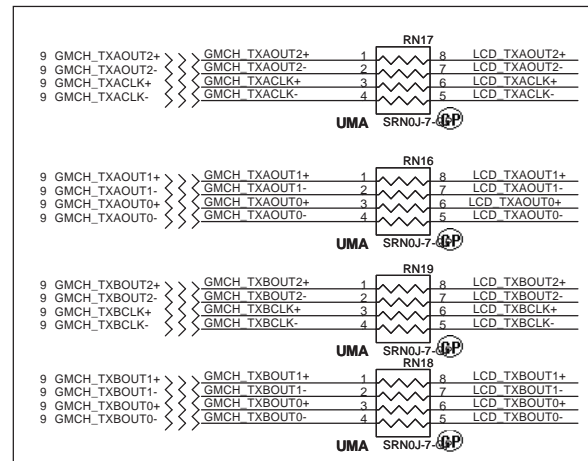


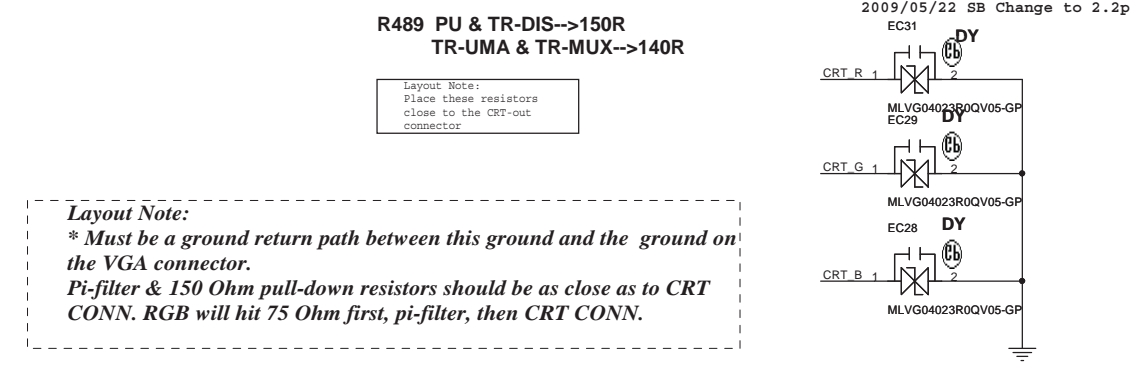
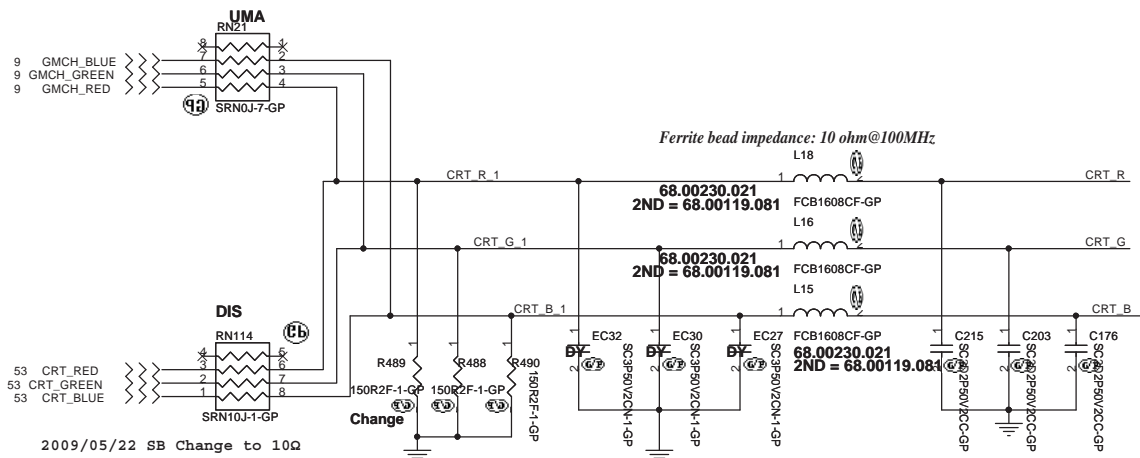
for TR



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

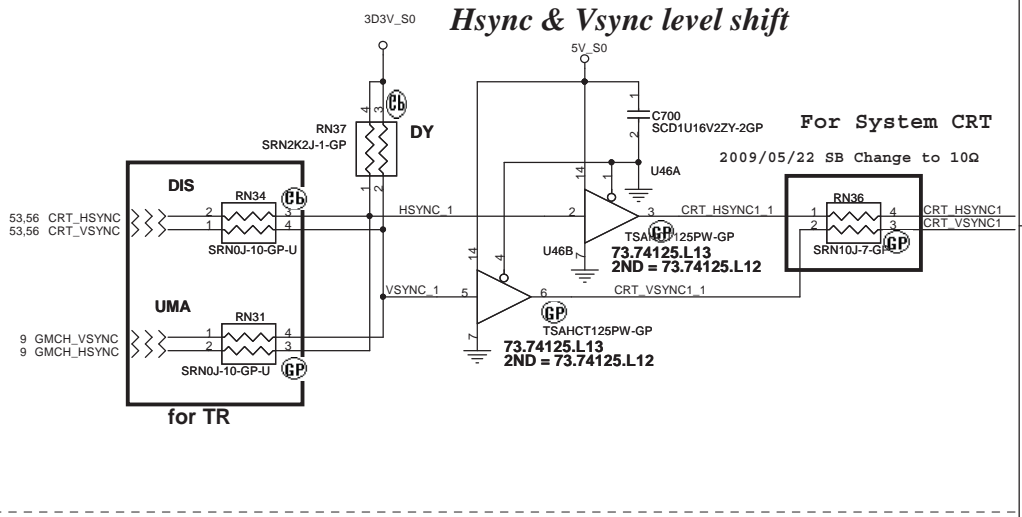
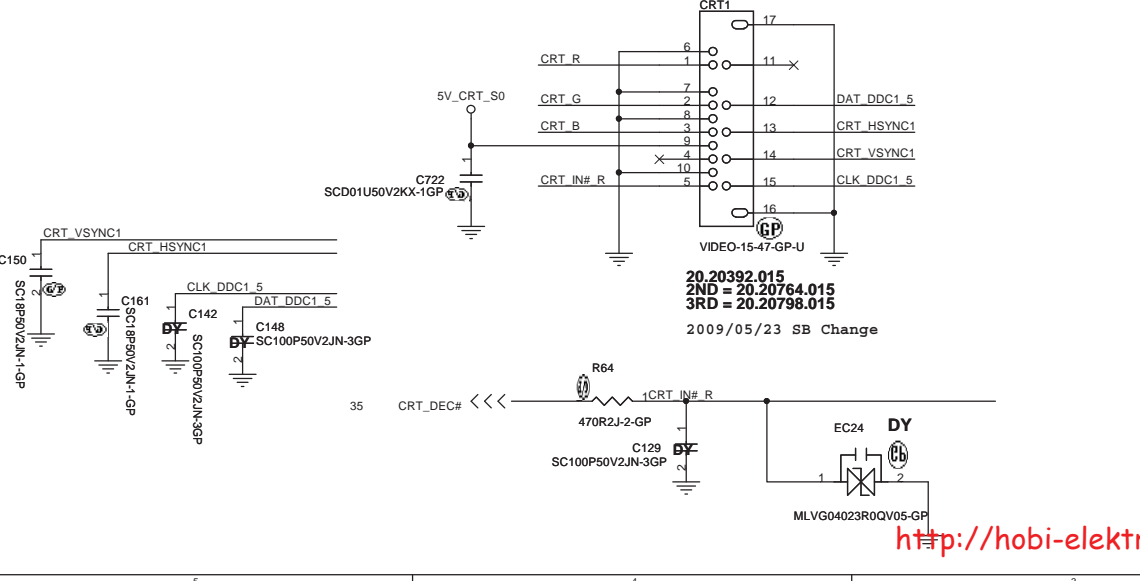
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



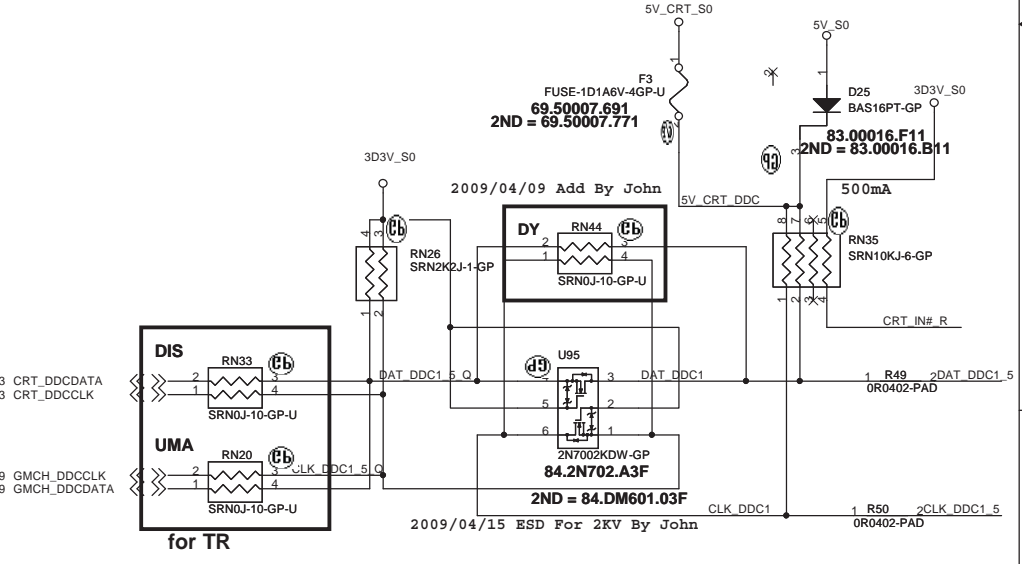


Layout Note:
Place these resistors close to the CRT-out connector

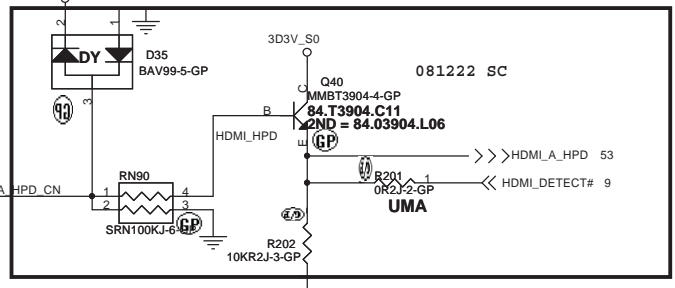
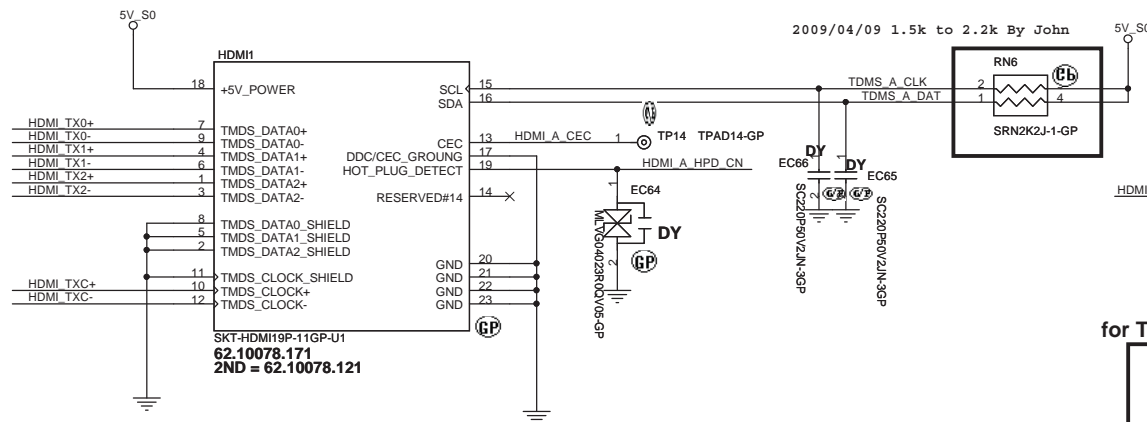
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



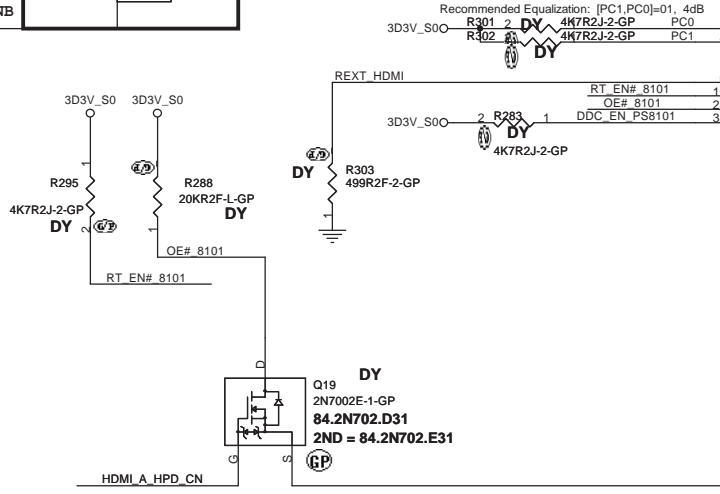
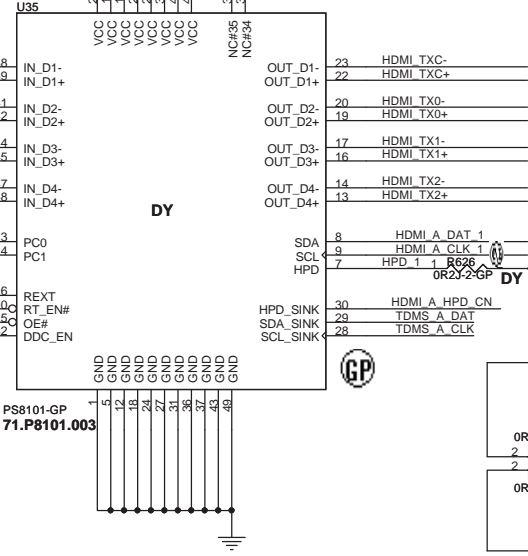
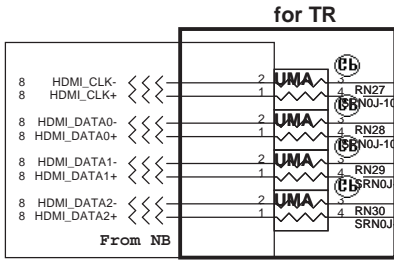
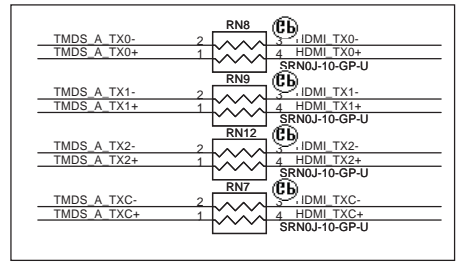
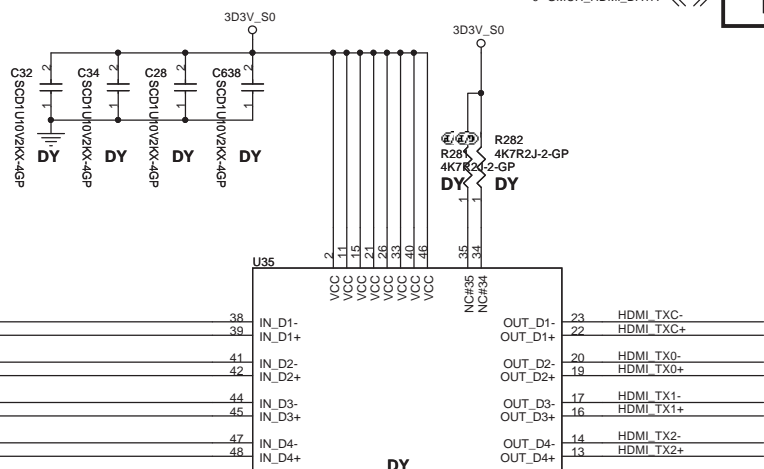
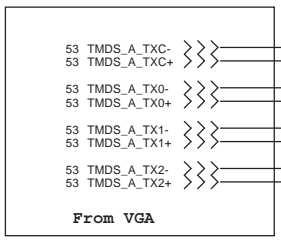
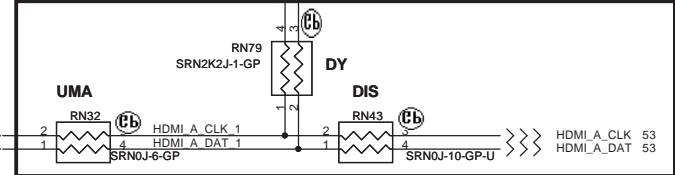
DDC_CLK & DATA level shift



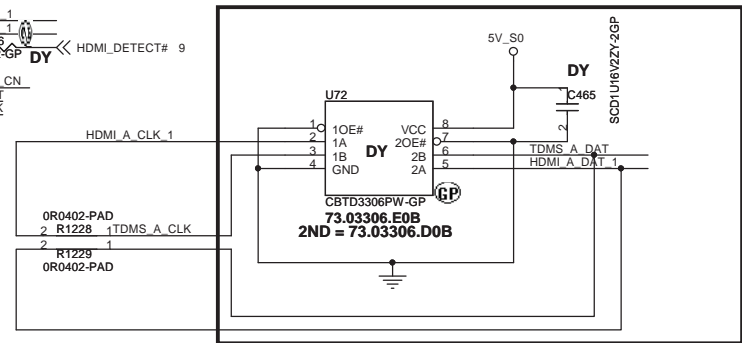
緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
CRT Connector	
JV71-TR	
Title	Rev
Size	SB
Date: Monday, July 06, 2009	Sheet 20 of 61



for TR



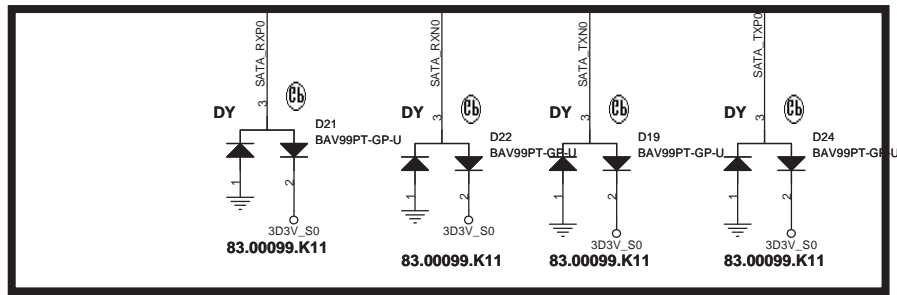
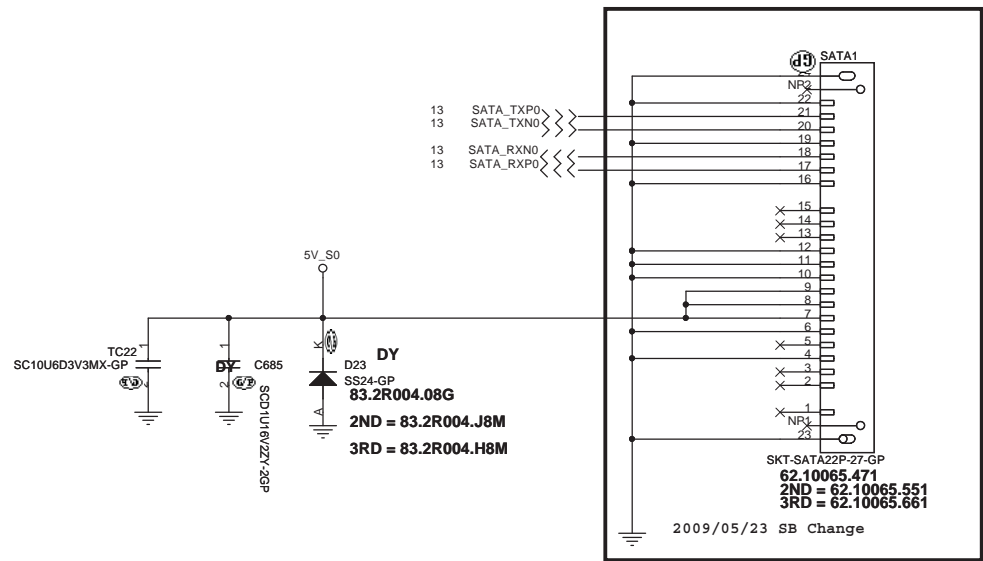
2009/04/14 Follow JM70 By John



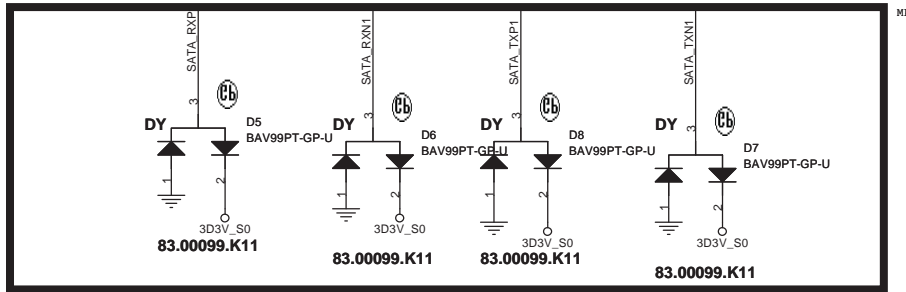
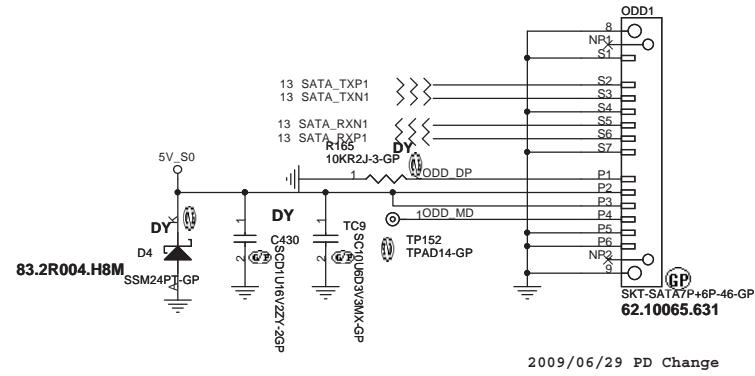
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			HDMI Connector		
Size	Document Number	JV71-TR		Rev	SB
Date: Monday, July 06, 2009	Sheet	21	of	61	

SATA Connector



SATA ODD Connector



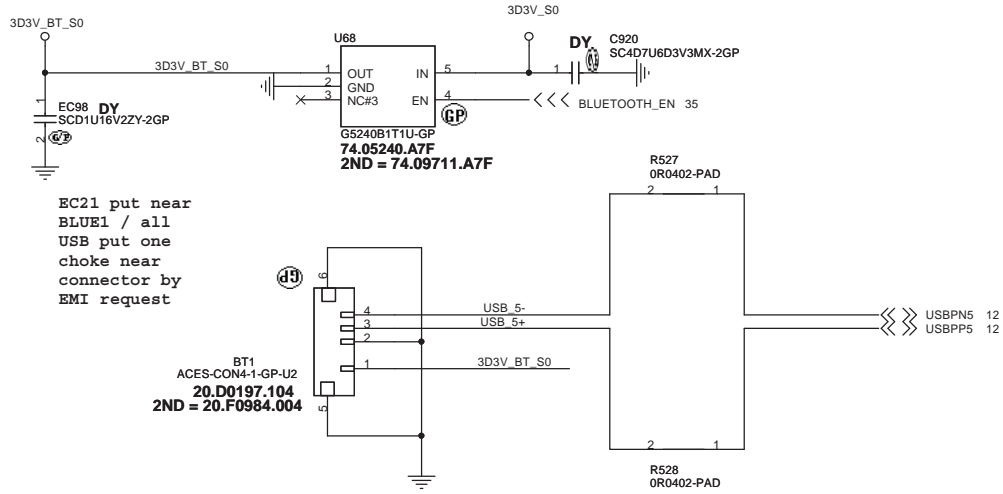
<http://hobi-elektronika.net>

UMA

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title ODD			
Size	Document Number	Rev	
	JV71-TR	SB	
Date:	Monday, July 06, 2009	Sheet	23 of 61

BLUETOOTH MODULE

1.5A / High Active Voltage 2V

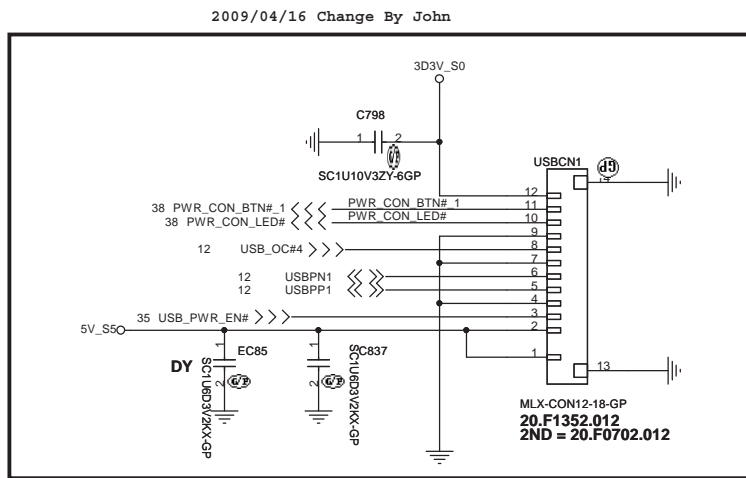
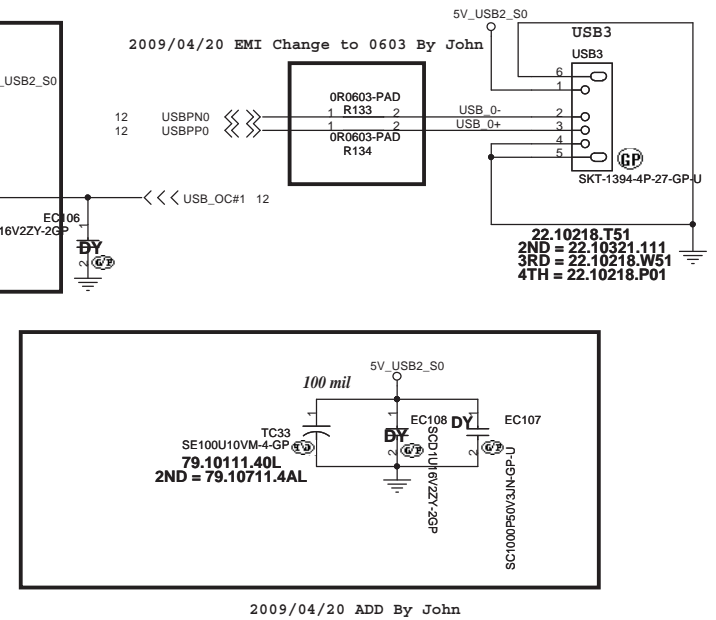
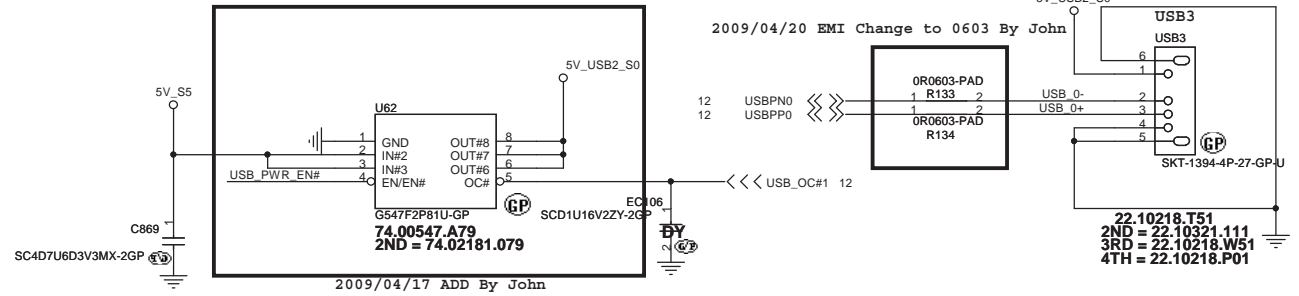
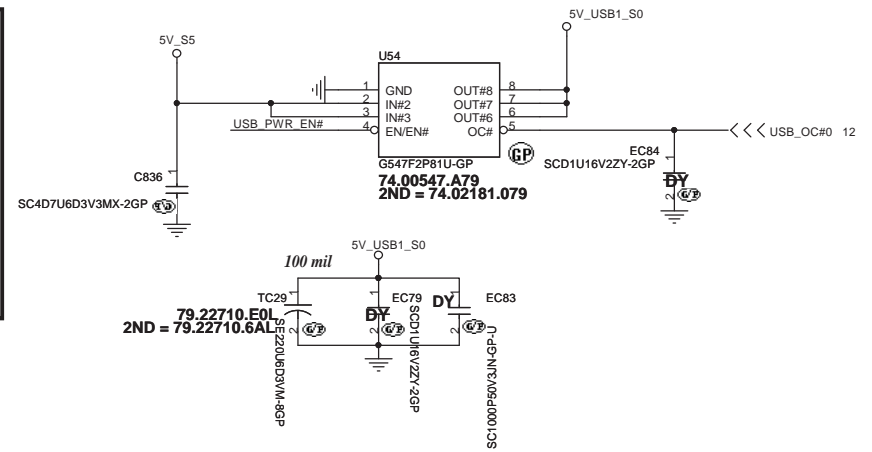
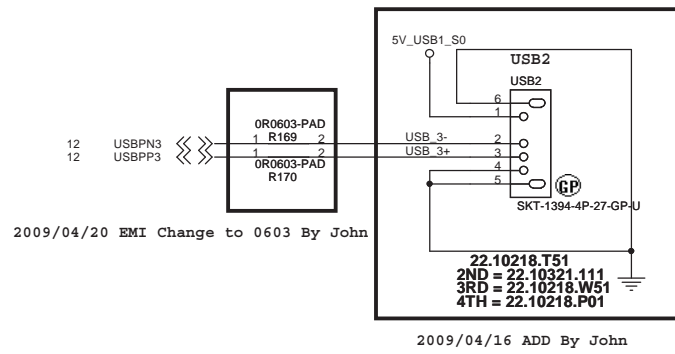
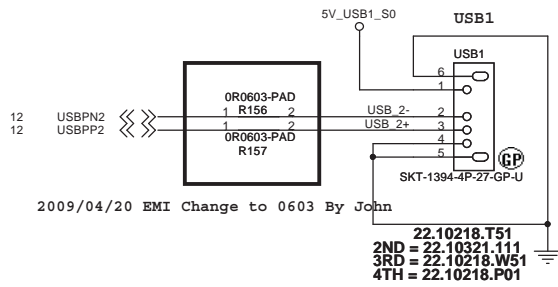


EC21 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request

<http://hobi-elektronika.net>

UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
BLUETOOTH			
Title		Rev	
Size		SA	
Document Number		JV71-TR	
Date: Monday, July 06, 2009		Sheet 24 of 61	



- USB_OC#4 1 173 AFTE14P-GP
- USBPN1 1 174 AFTE14P-GP
- USBPPP1 1 176 AFTE14P-GP
- USB_PWR_EN# 1 178 AFTE14P-GP
- 5V_S5 1 179 AFTE14P-GP

<http://hobi-elektronika.net>

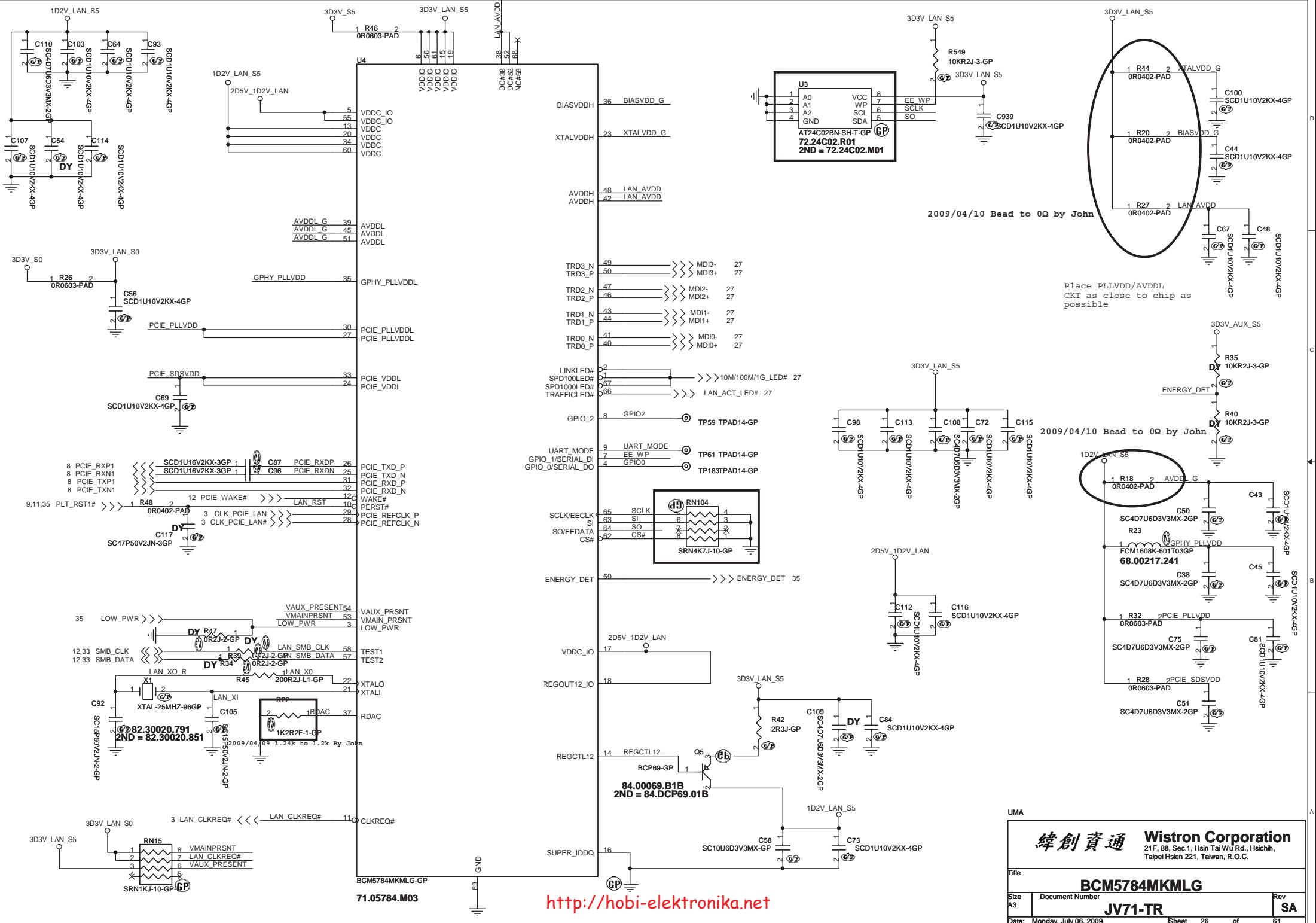
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB**

Size	Document Number	Rev
	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 25 of 61



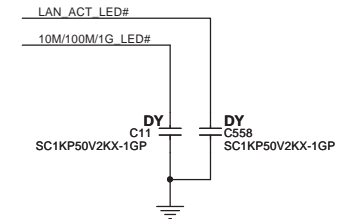
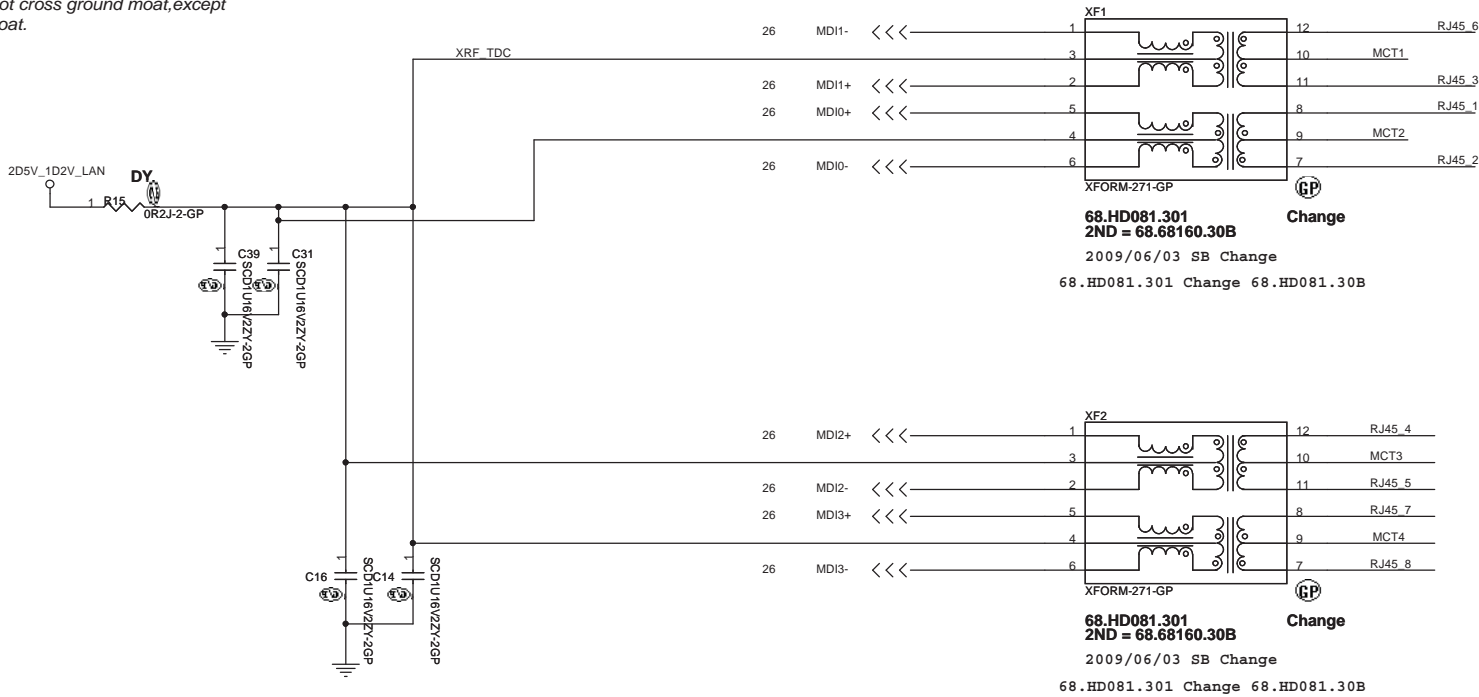
<http://hobi-elektronika.net>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.	
Title: BCM5784M KMLG	
Size: A3	Document Number: JV71-TR
Date: Monday, July 06, 2009	Sheet 26 of 61

LAN Connector

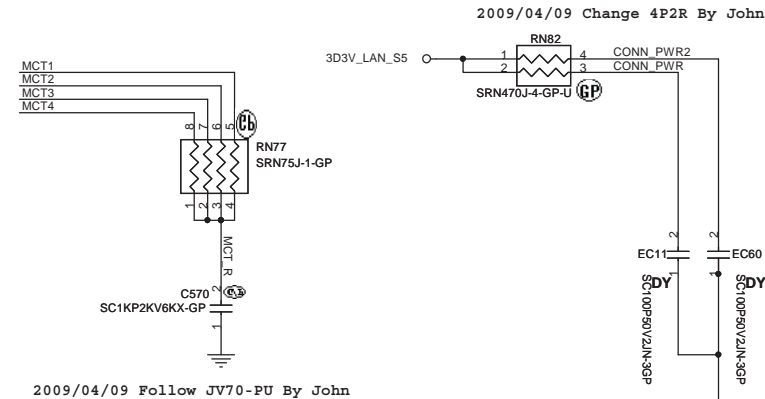
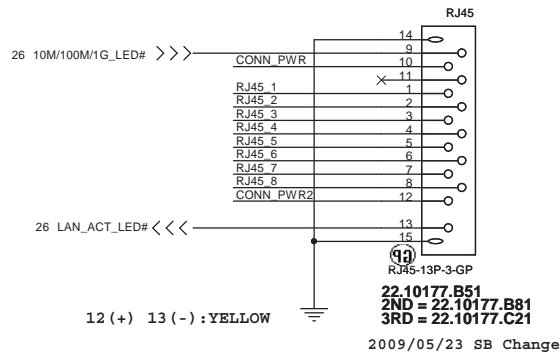
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

GIGA Lan Transformer

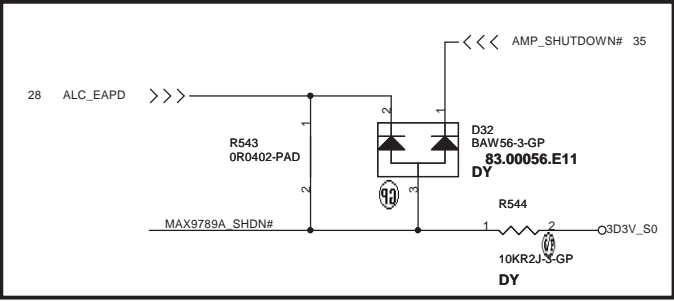
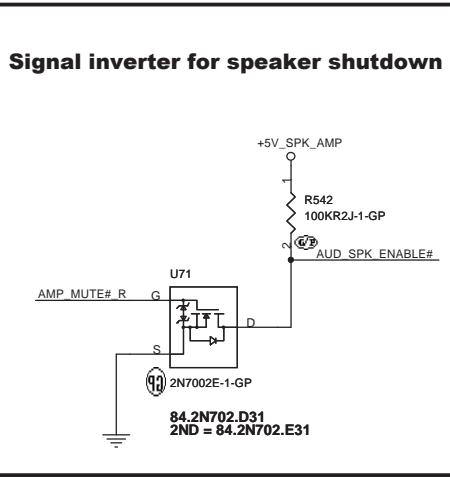
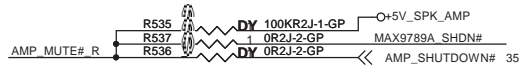
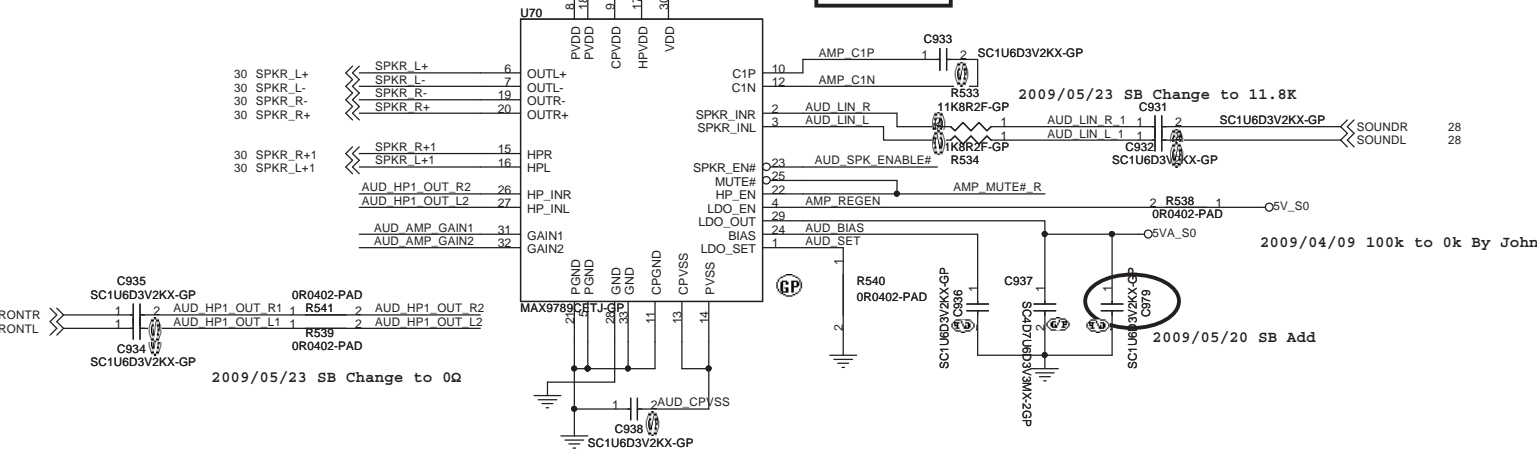
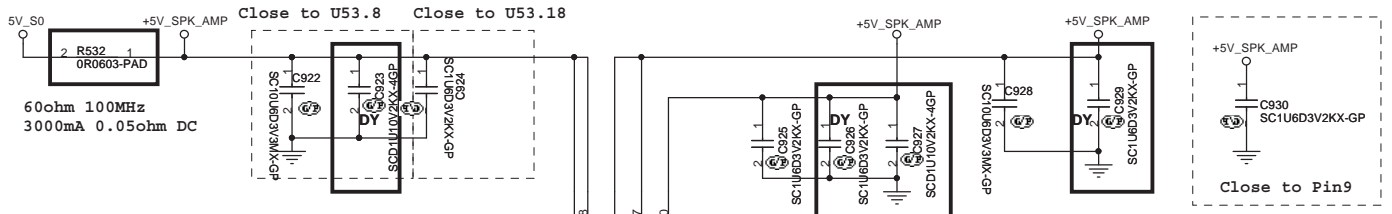


10 (+) 9 (-) : : GREEN
 10 (+) 11 (-) : ORANGE

LAN Connector



DOC_TIP,DOC_RING,TIP,RING:
 W/S : 10/100 @ Surface layers
 10/20 @ Inner layers



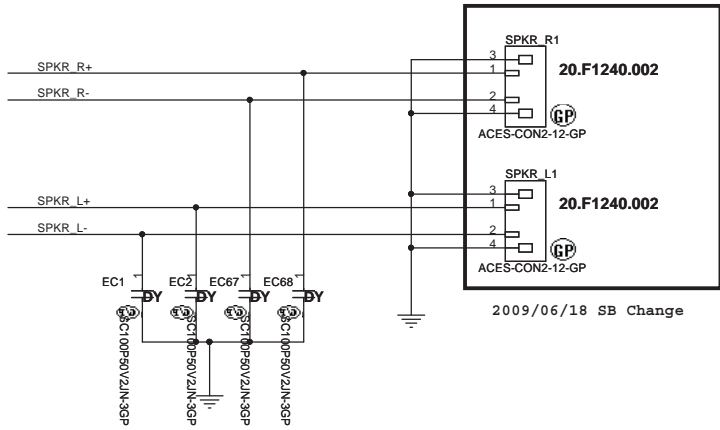
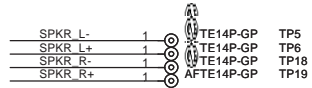
GAIN SETTING

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

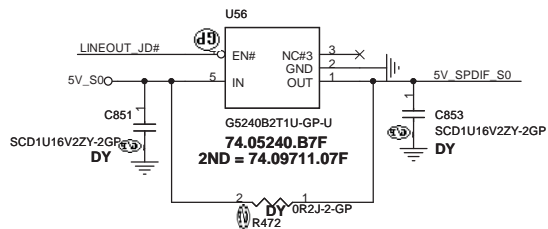
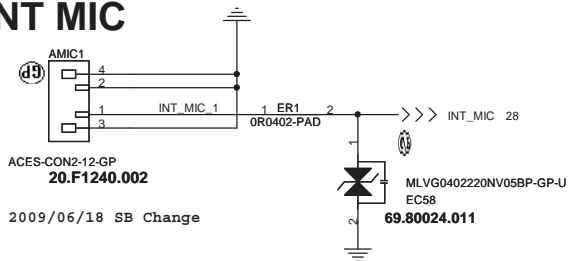
<http://hobi-elektronika.net>

Internal Speaker

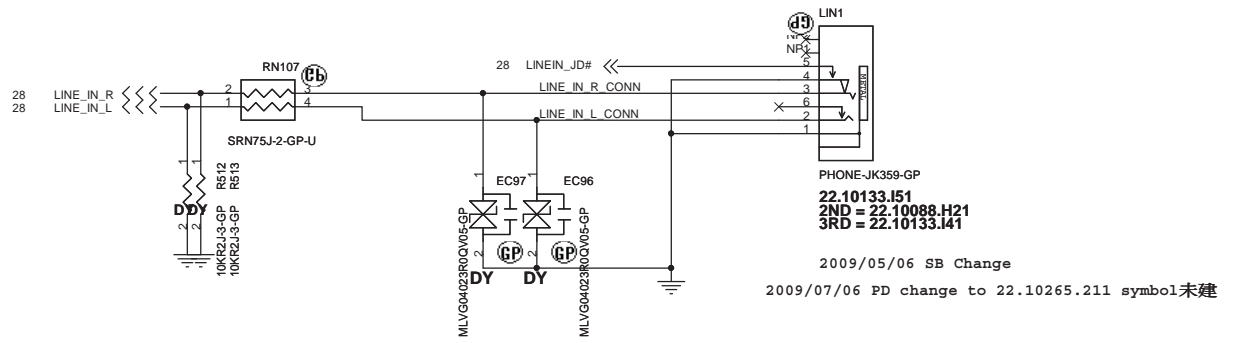
29 SPKR_L- <<< SPKR_L-
 29 SPKR_L+ <<< SPKR_L+
 29 SPKR_R- <<< SPKR_R-
 29 SPKR_R+ <<< SPKR_R+



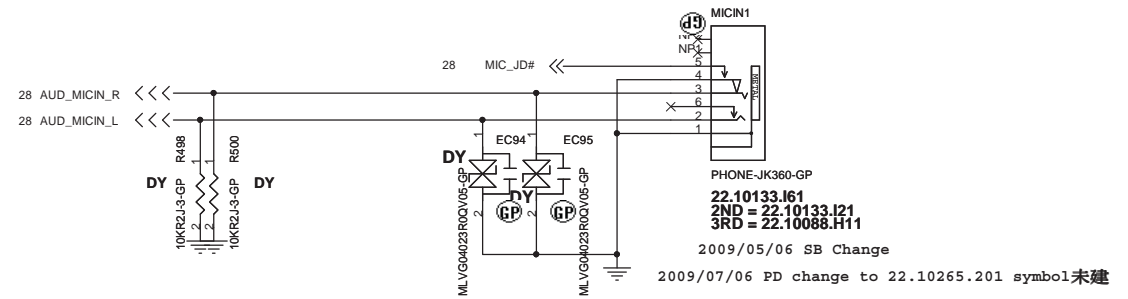
INT MIC



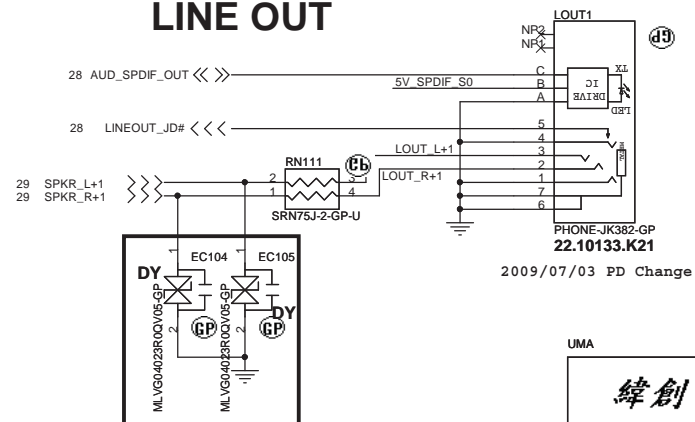
LINE IN



MIC IN

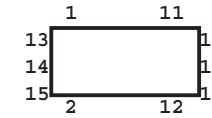
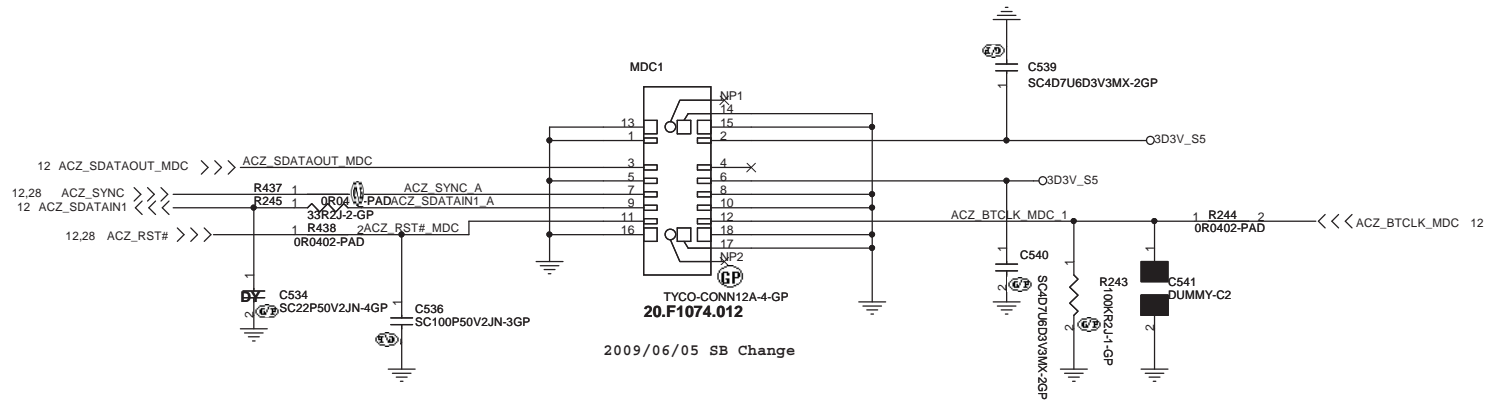


LINE OUT



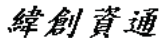
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
AUDIO JACK	
JV71-TR	
Title: _____ Size: _____ Date: Monday, July 06, 2009	Document Number: _____ Sheet: 30 of 61
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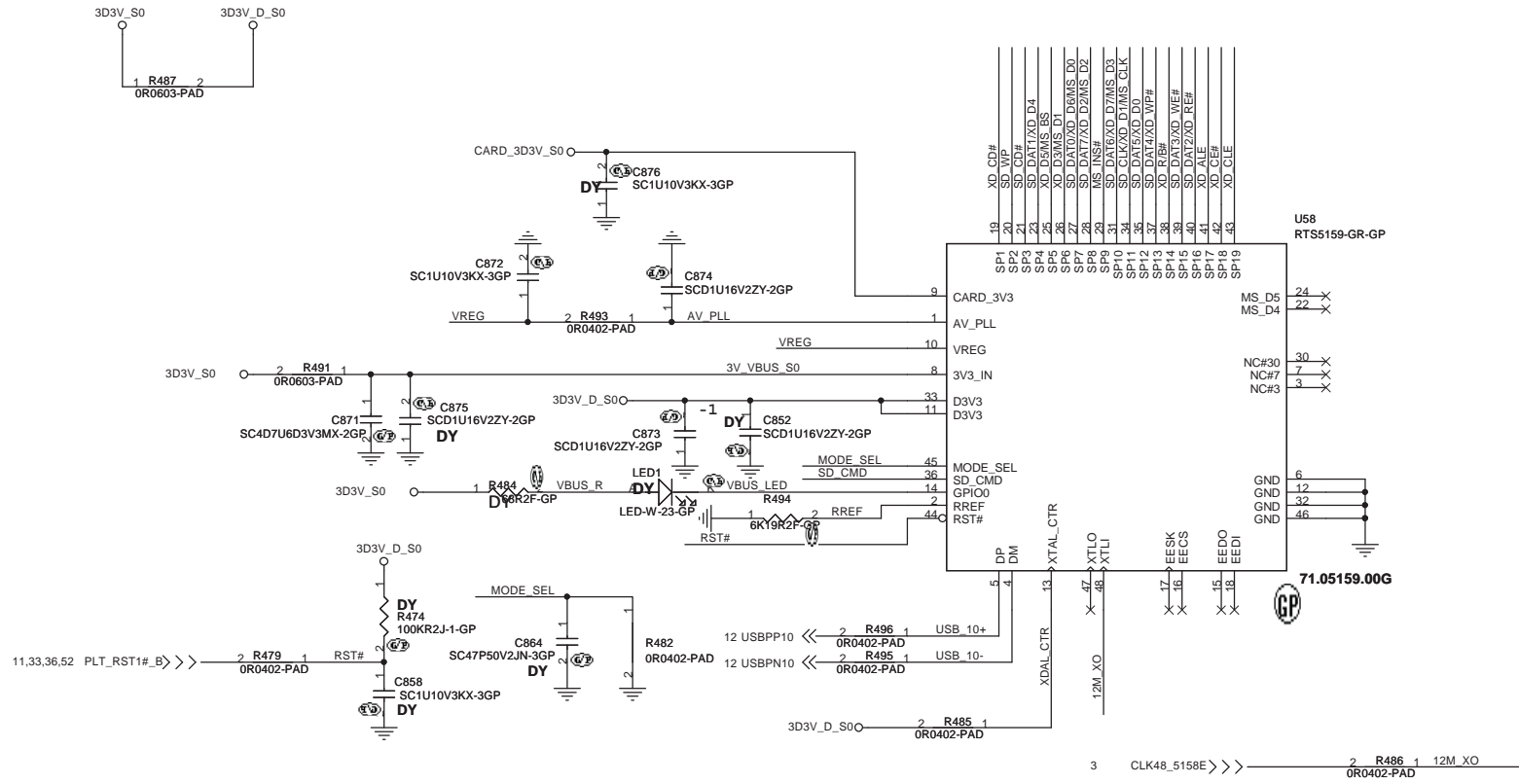
MDC 1.5 CONN



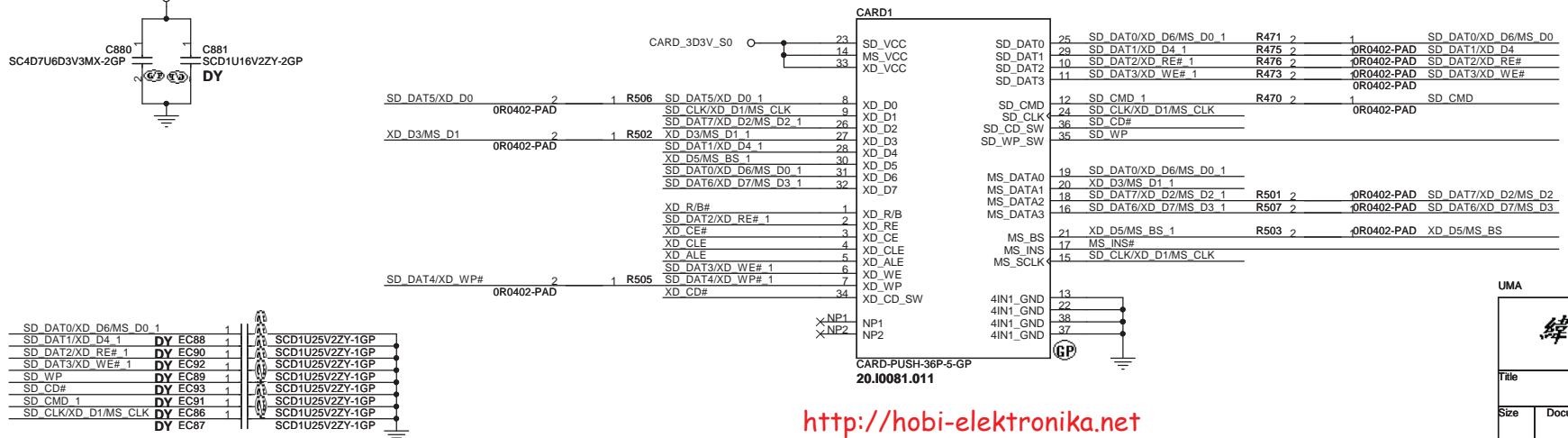
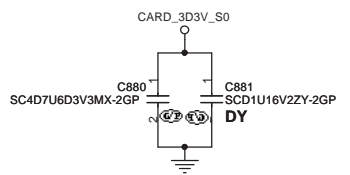
<http://hobi-elektronika.net>

UMA

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MDC	
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5 IN 1 CARD-READER (SD/MMC/MS/MS PRO/XD)



<http://hobi-elektronika.net>

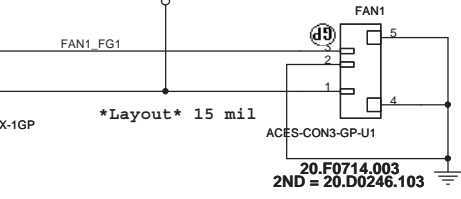
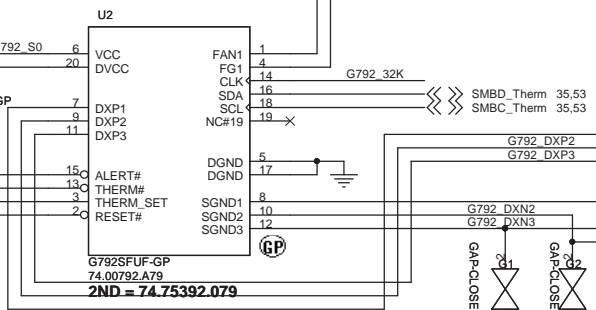
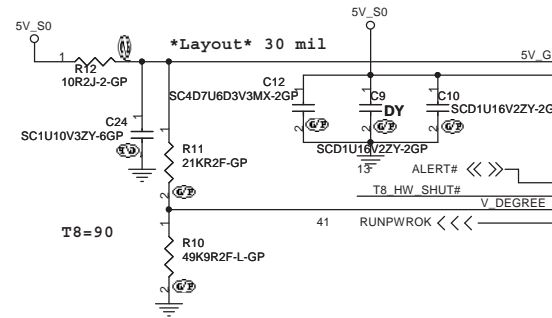
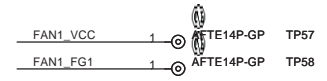
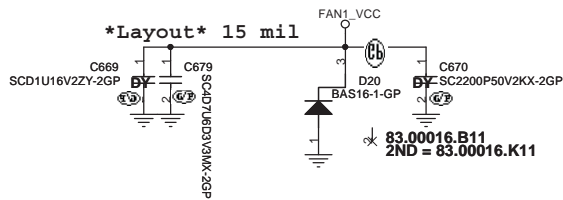
UMA

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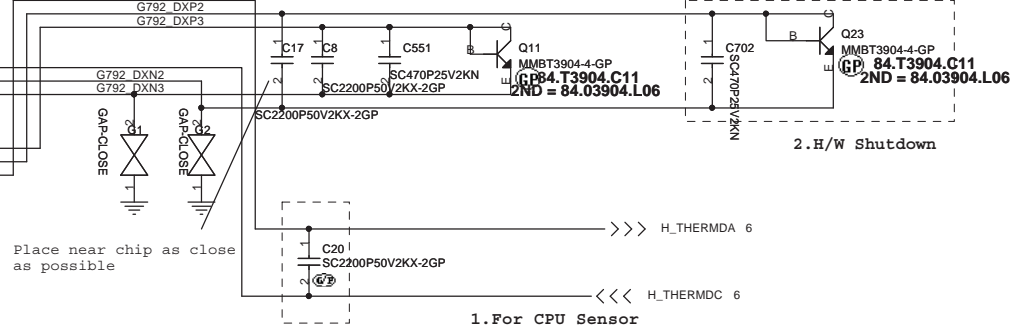
Title: **CARDREADER- RTS5159**

Size: Document Number: **JV71-TR** Rev: **SB**

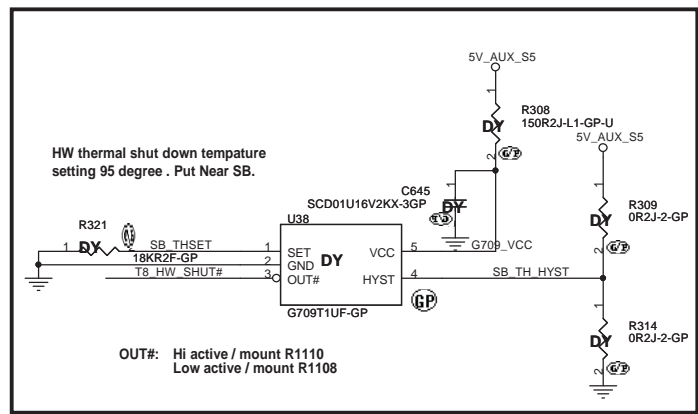
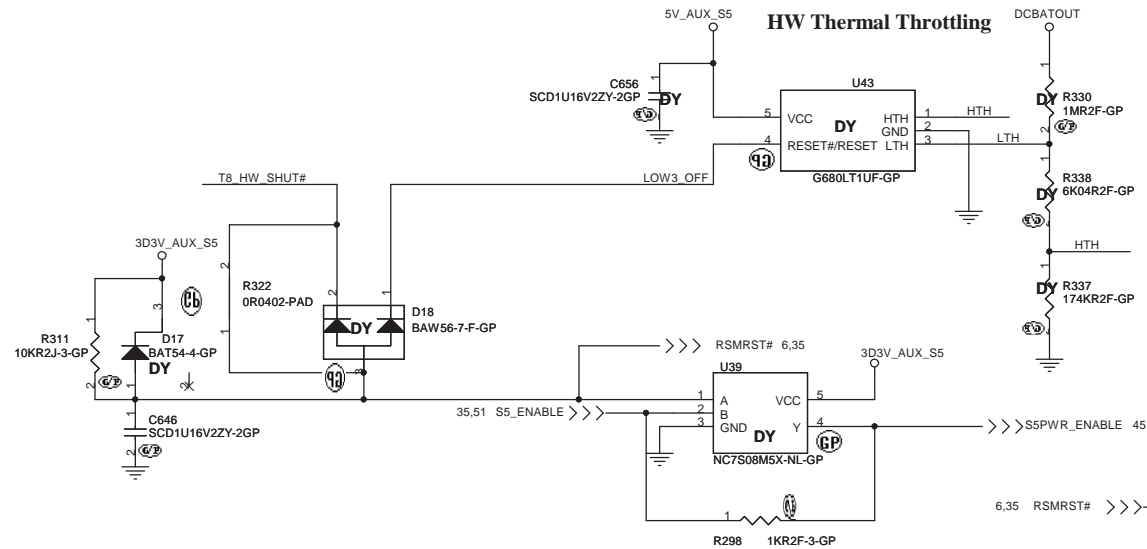
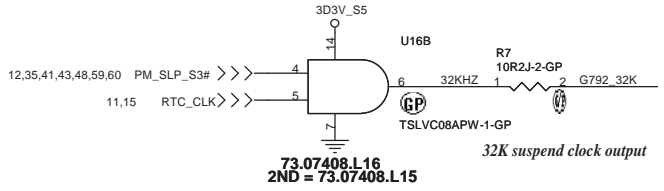
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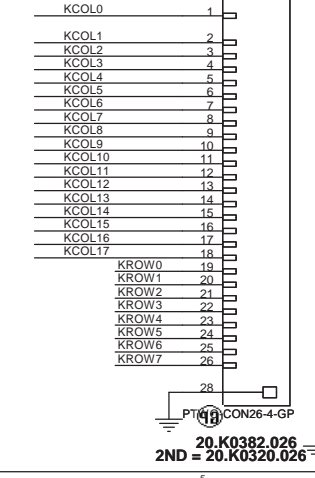
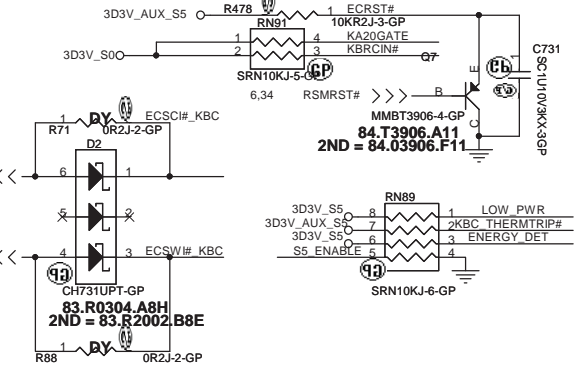
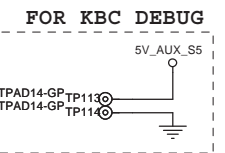
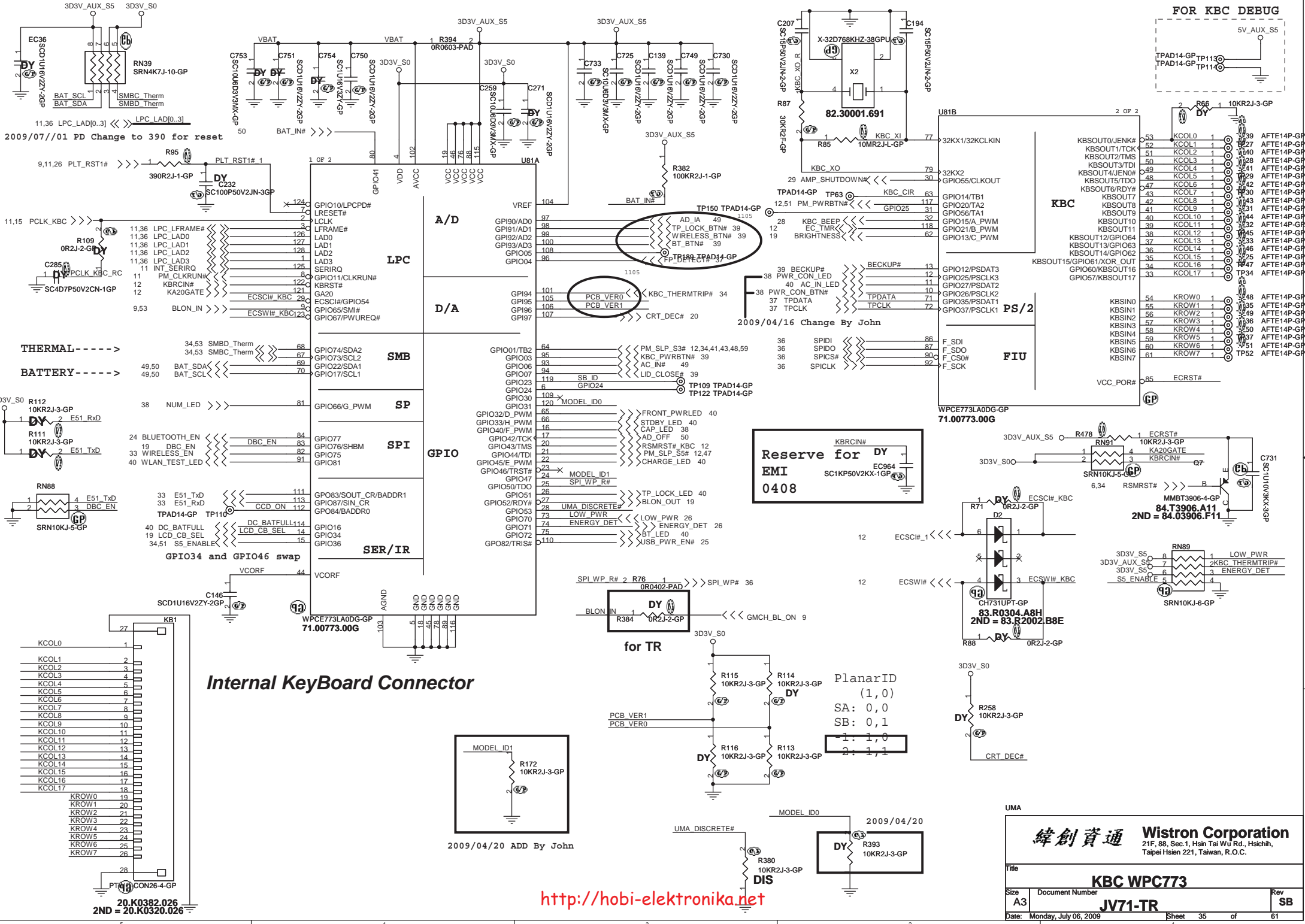
3.System Sensor, Put Flamrest.



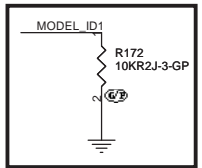
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree



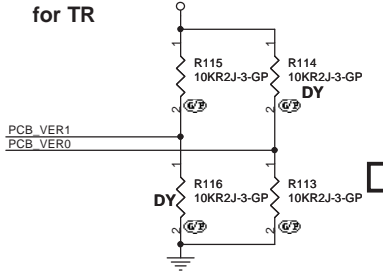
<http://hobi-elektronika.net>
83.R2003.E81
2ND = 83.BAT54.081



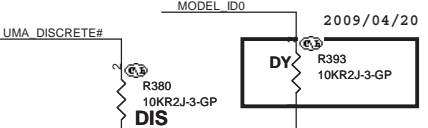
Internal KeyBoard Connector



2009/04/20 ADD By John



PlanarID
(1,0)
SA: 0,0
SB: 0,1
1.1,0
2.1,1,1



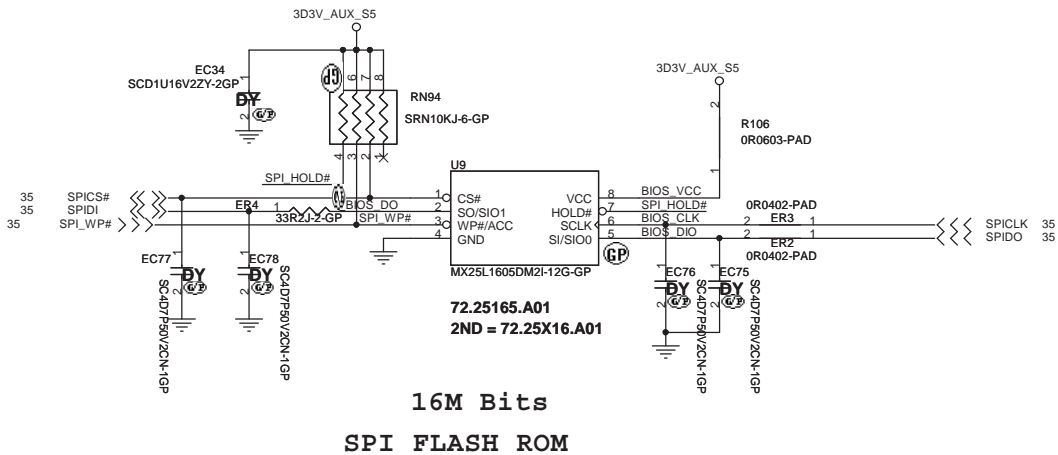
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KBC WPC773

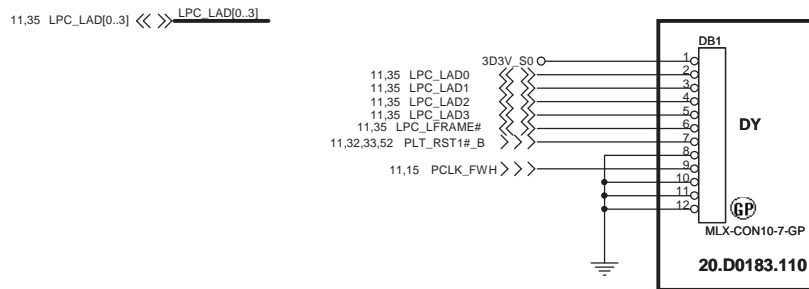
File: **JV71-TR**

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GOLDEN FINGER FOR DEBUG BOARD

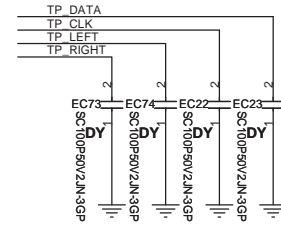
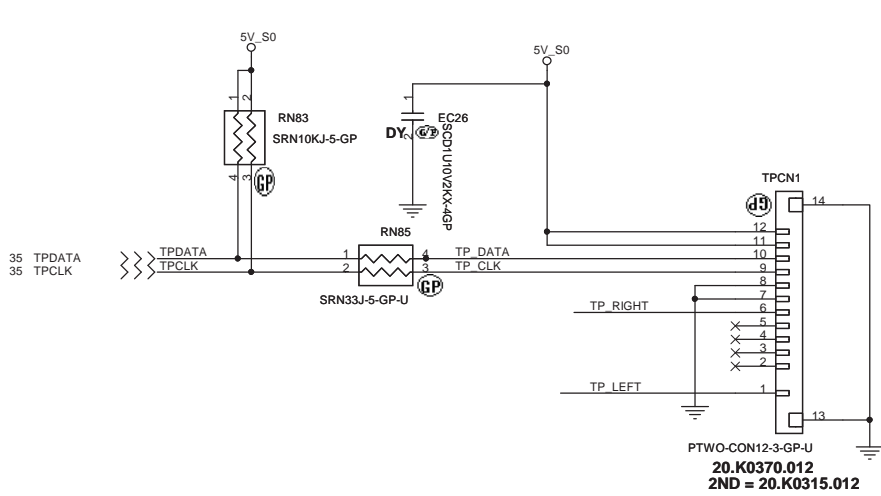


<http://hobi-elektronika.net>

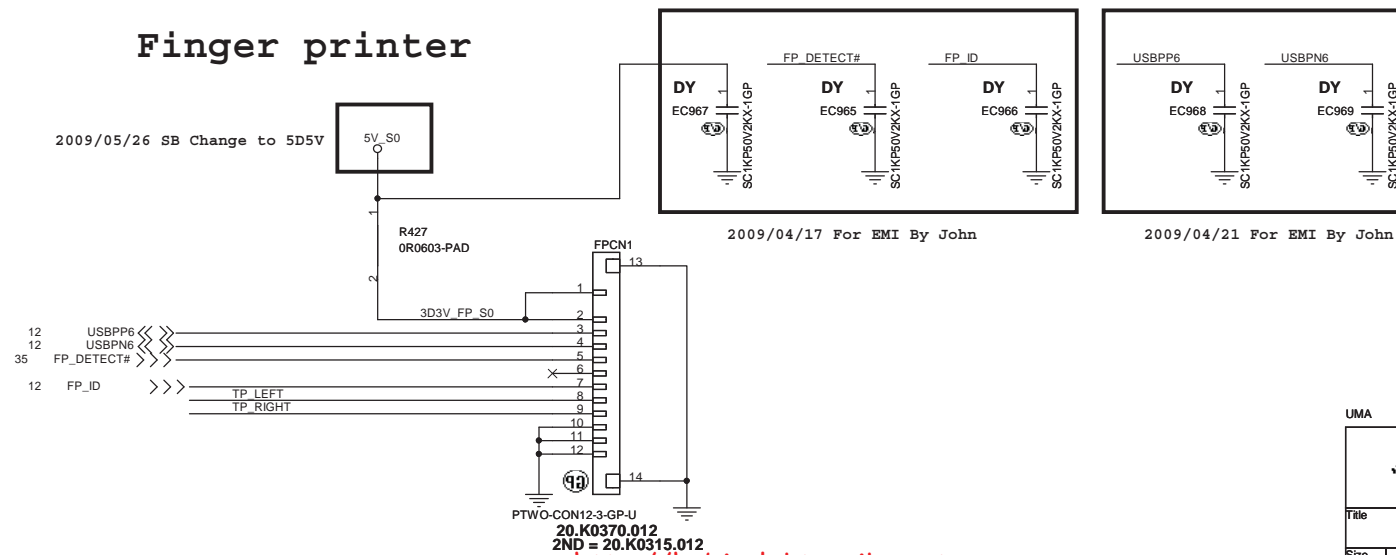
UMA

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Title		
BIOS		
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TOUCH PAD



Finger printer



<http://hobi-elektronika.net>

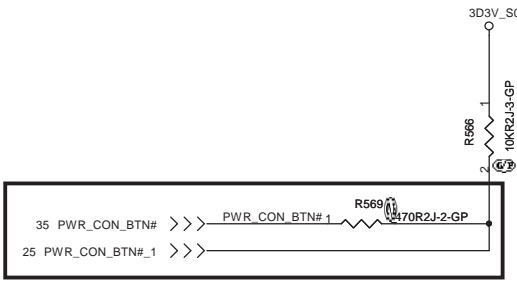
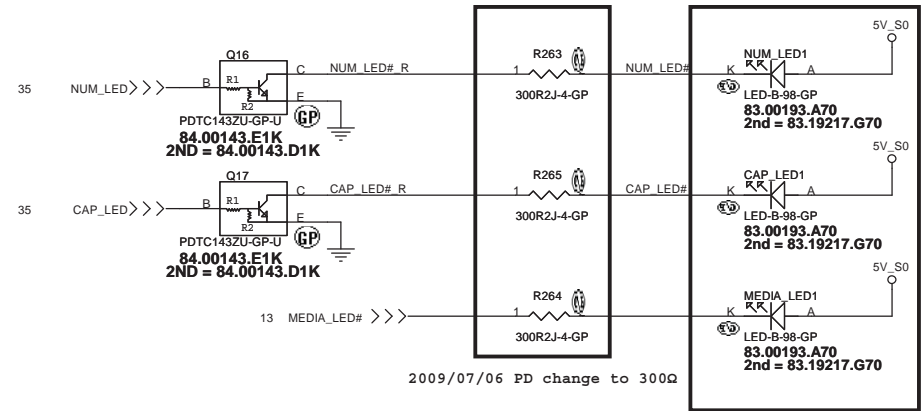
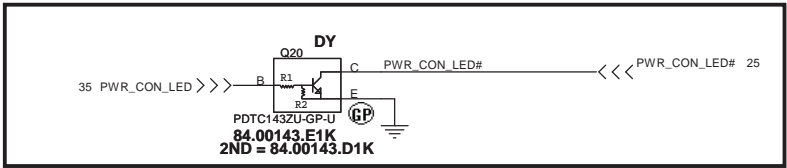
UMA

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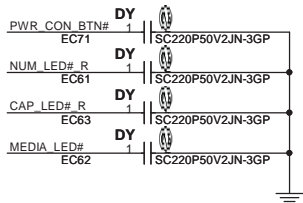
Title: **Touch PAD/Finger printer**

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2009/04/16 Change By John



2009/04/16 Change By John

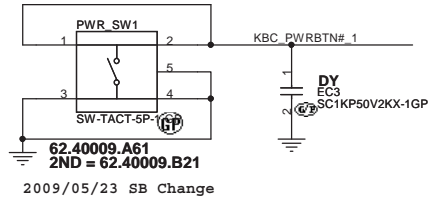


<http://hobi-elektronika.net>

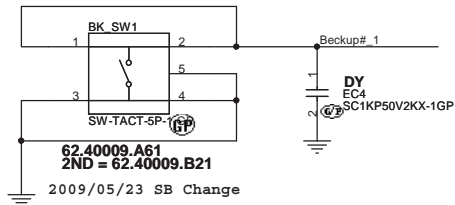
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Title LAUNCH BOARD		
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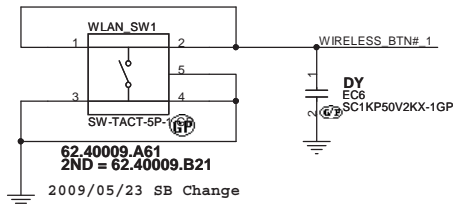
Power Button



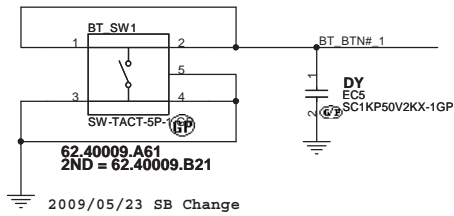
Beckup Button



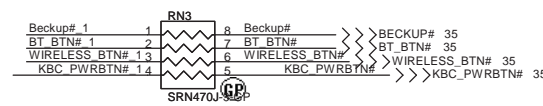
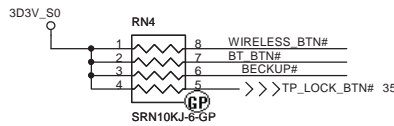
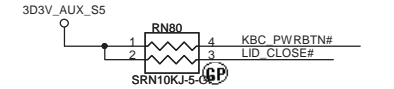
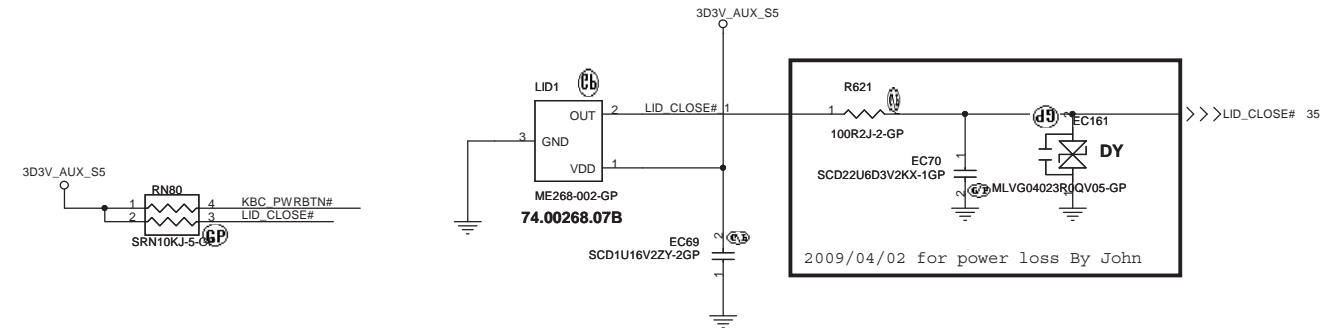
WIRELESS Button



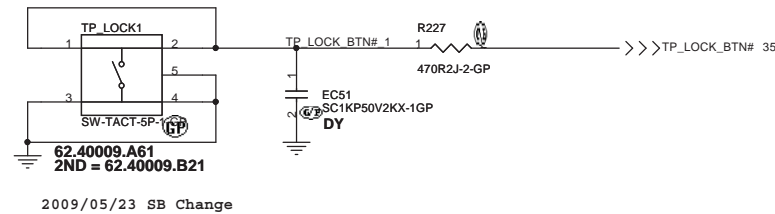
BT/3G Button

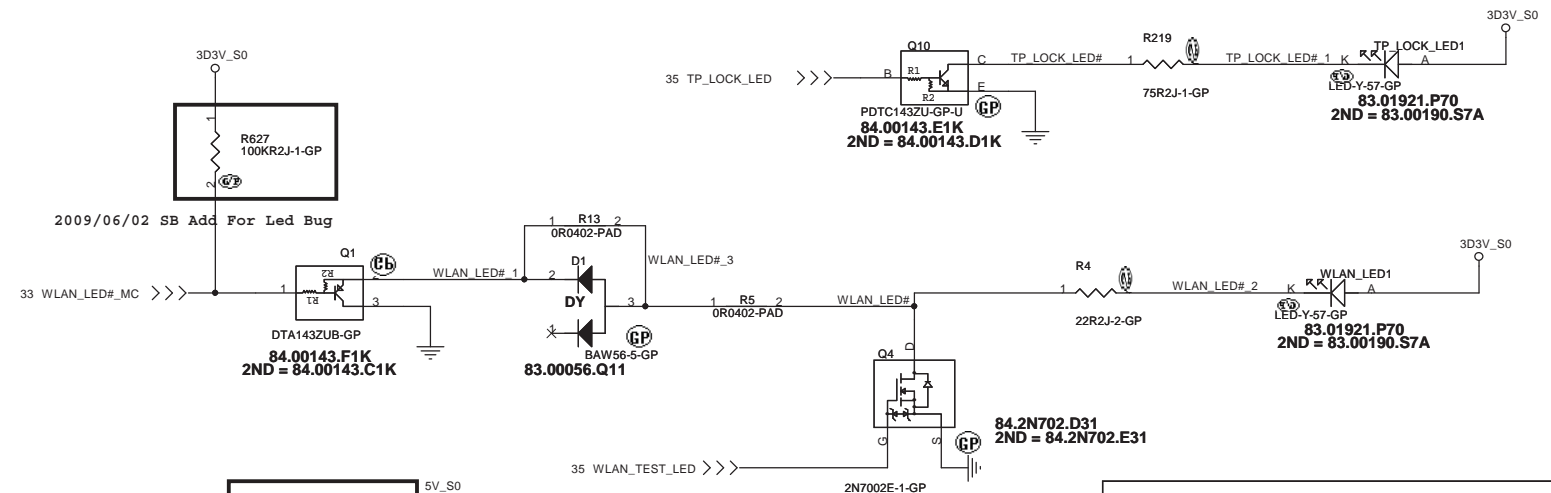
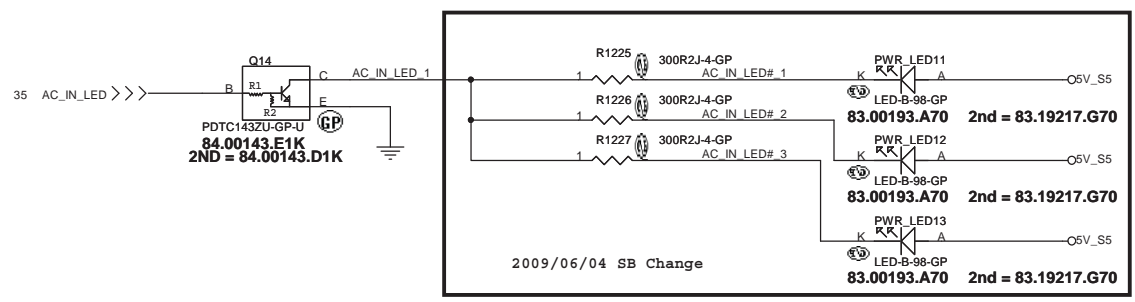
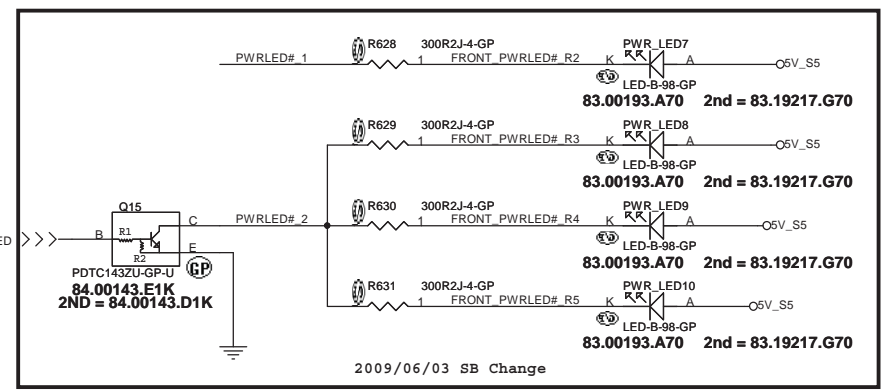
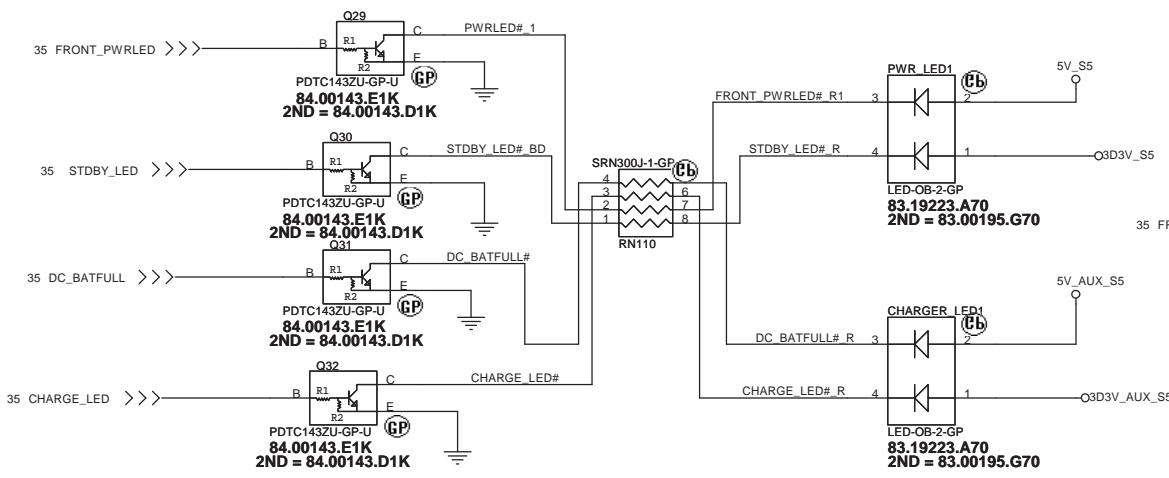


Cover Up Switch



T/P lock Button





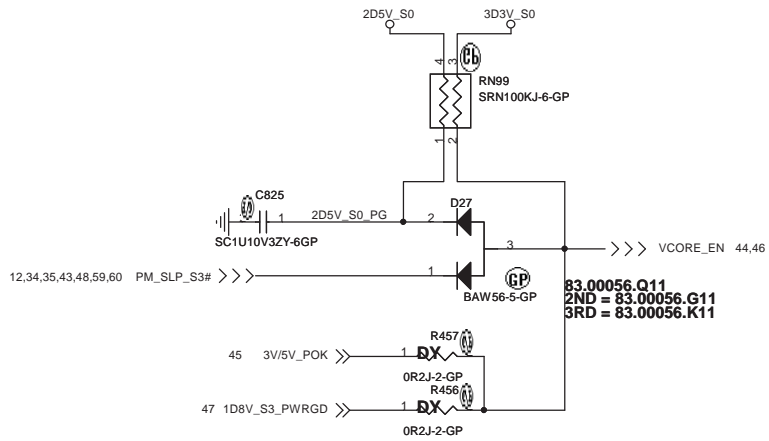
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Title: **LED**

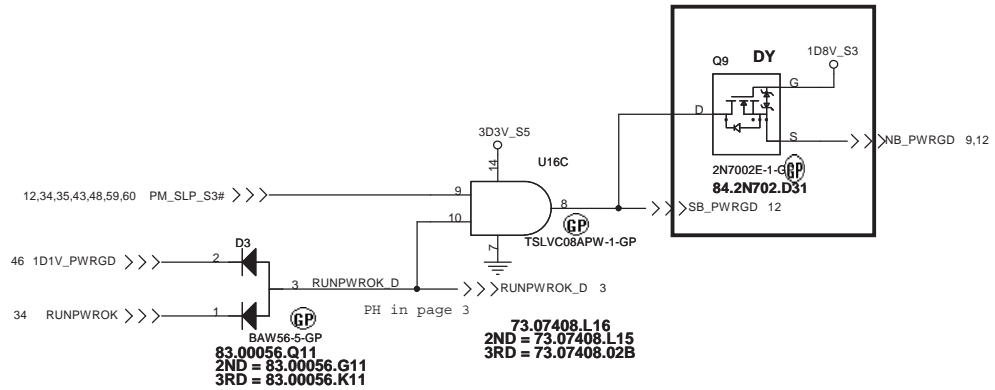
Size: A3 Document Number: **JV71-TR** Rev: **SB**

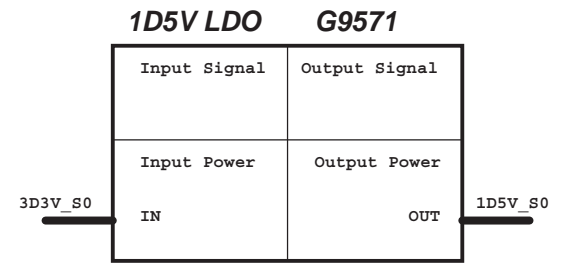
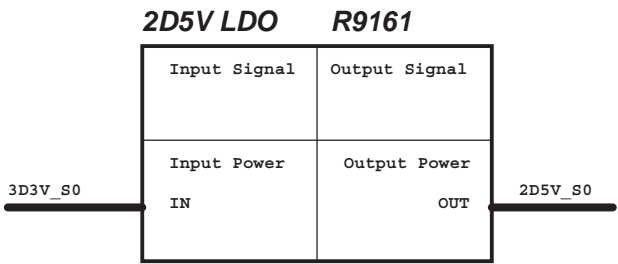
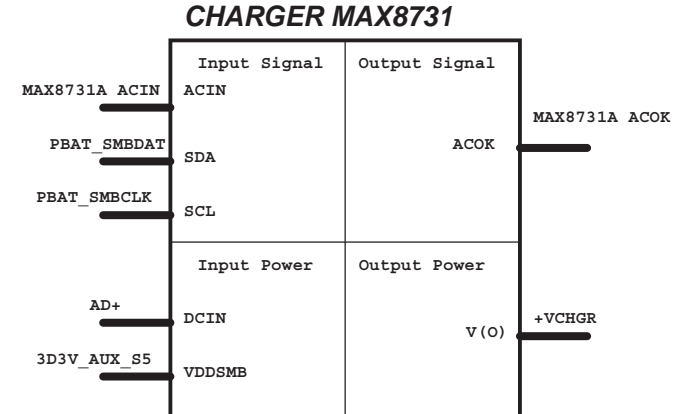
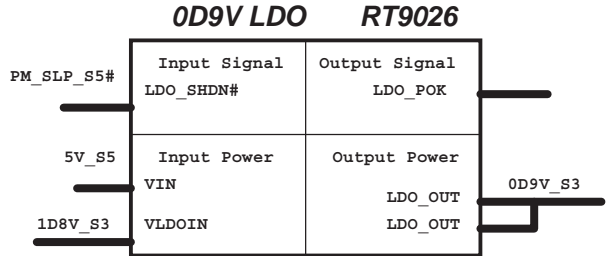
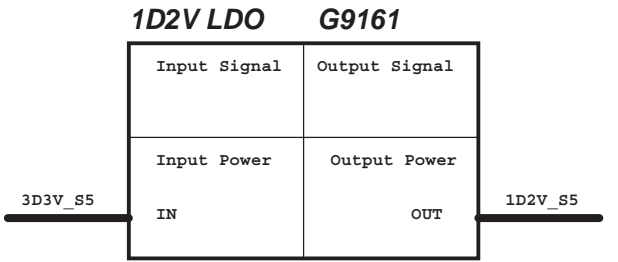
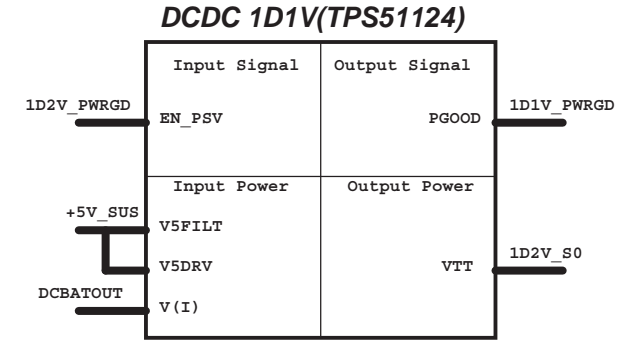
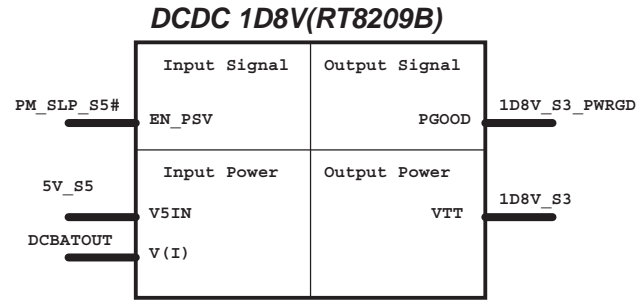
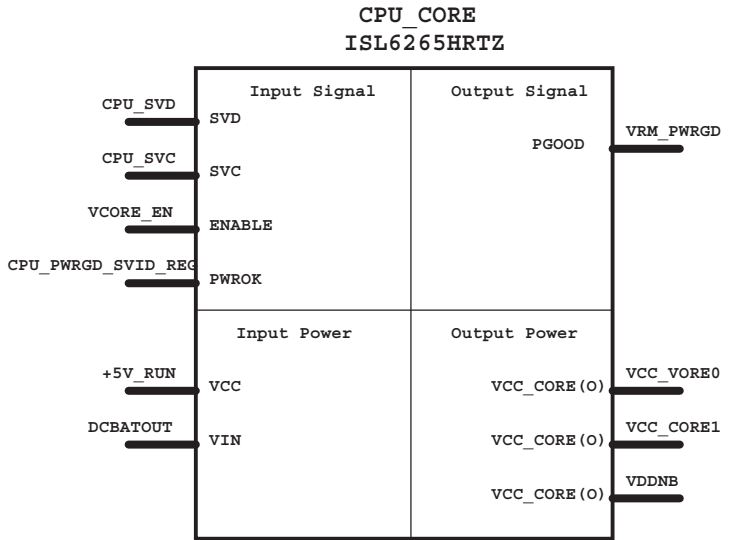
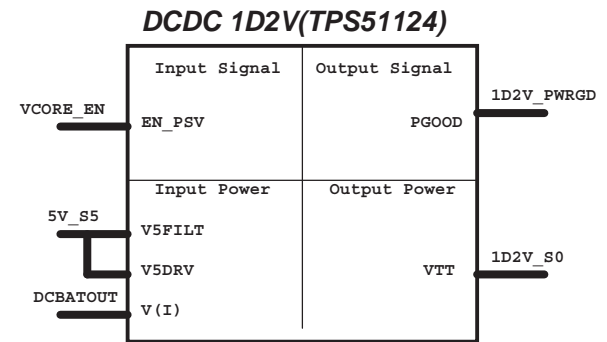
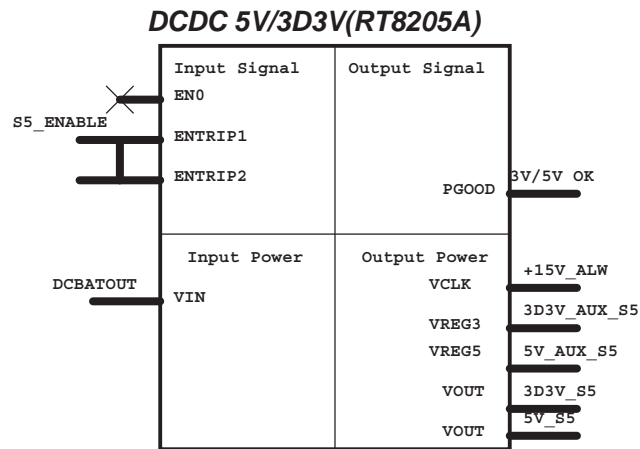
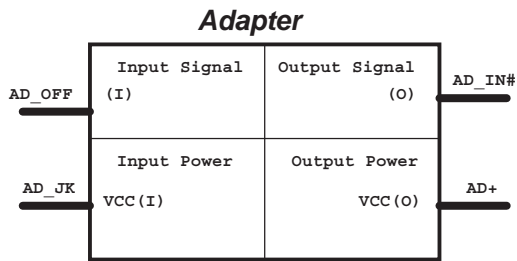
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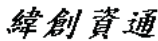
P/H @ 1D8V_S3 PAGE



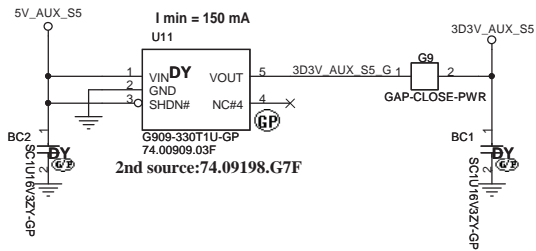


<http://hobi-elektronika.net>

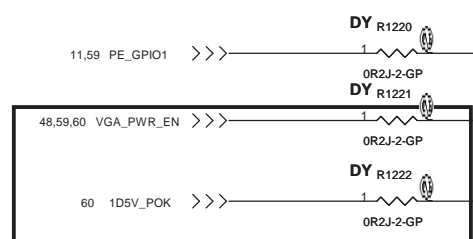
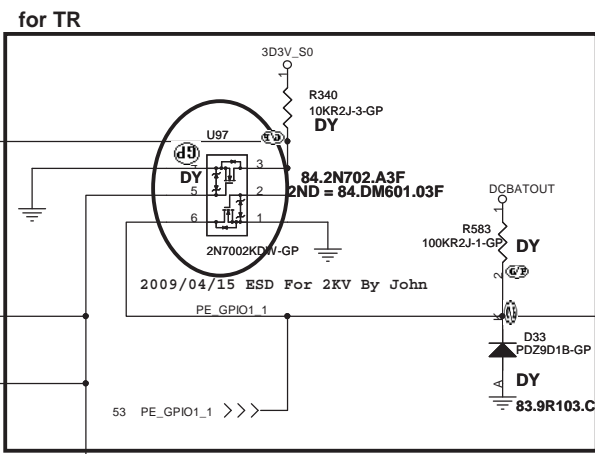
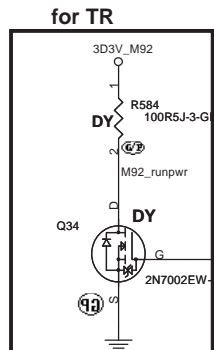
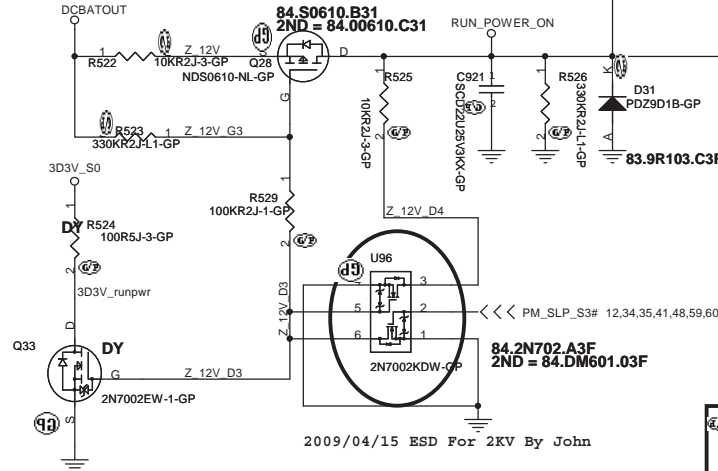
UMA

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Title Power Block Diagram	
Size A3	Document Number JV71-TR
Date: Monday, July 06, 2009	Rev SA
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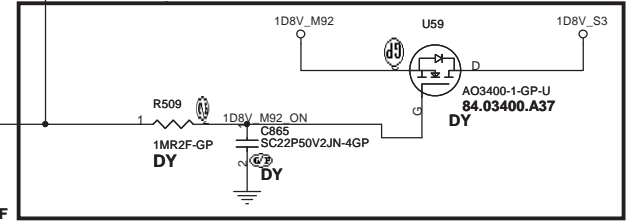
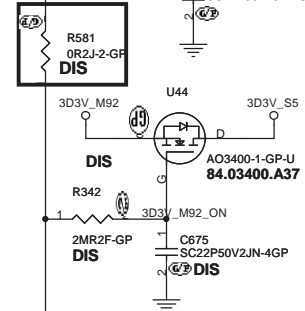
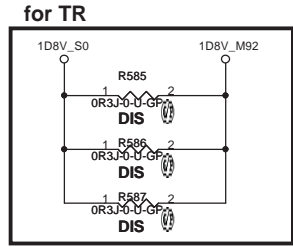
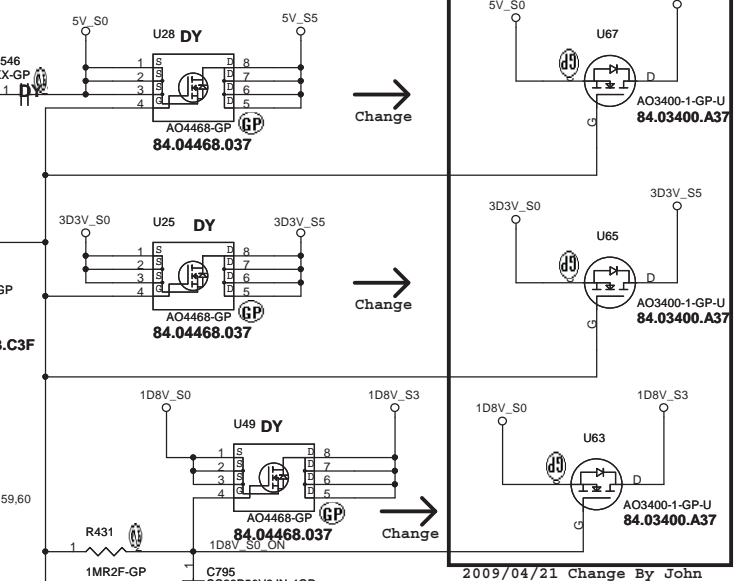
Aux Power 3D3V_AUX_S5



Run Power



2009/04/21 ADD By John



R509, R342--10MΩ
 C865--22pF
 C795--1000pF
 For VGA sequence issue

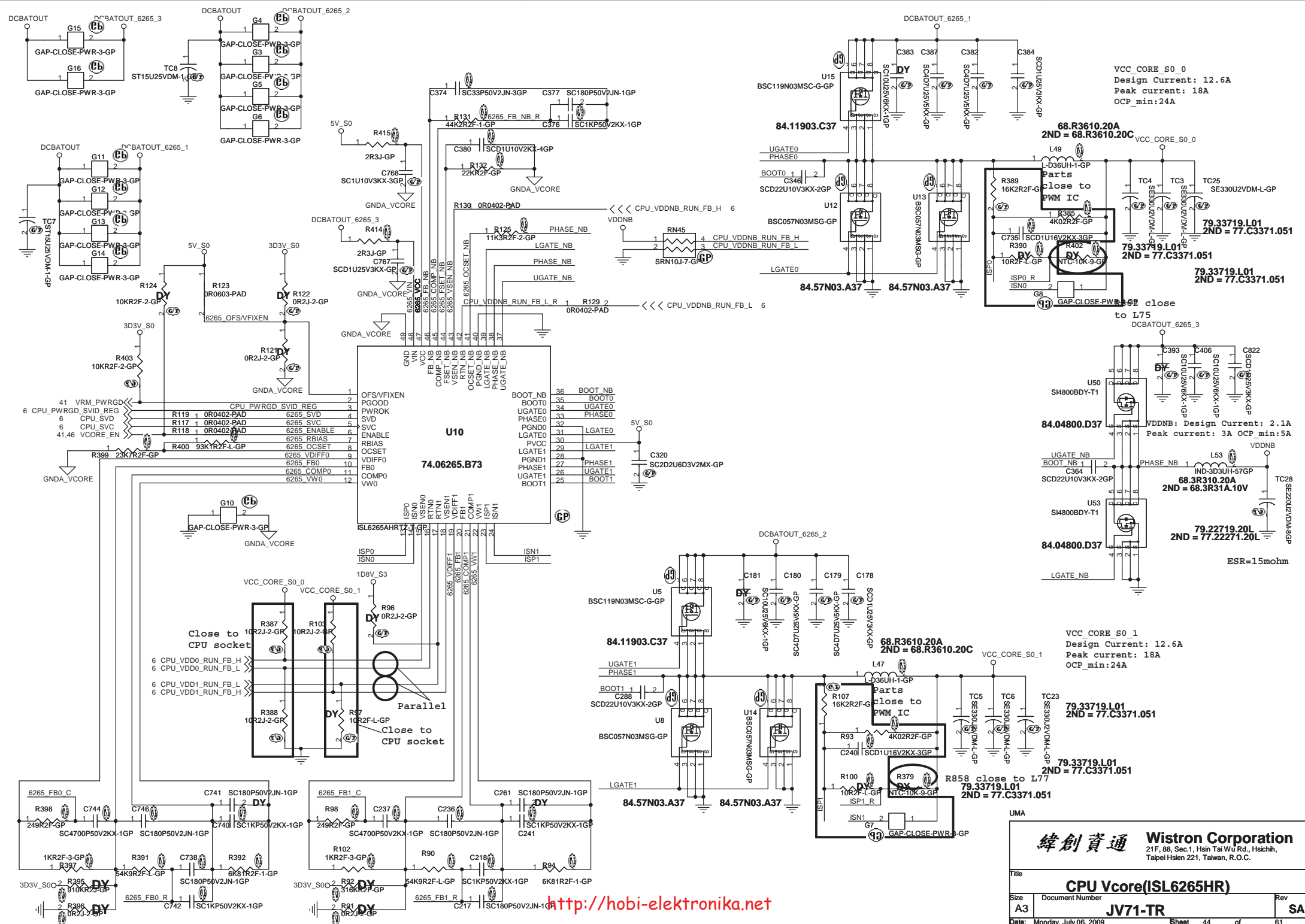
UMA

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Title: **RUN AND AUX POWER**

Size: A3 Document Number: **JV71-TR** Rev: SA

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VCC_CORE_S0_0
 Design Current: 12.6A
 Peak current: 18A
 OCP_min:24A

VDDNB: Design Current: 2.1A
 Peak current: 3A OCP_min:5A

VCC_CORE_S0_1
 Design Current: 12.6A
 Peak current: 18A
 OCP_min:24A

79.33719.L01
 2ND = 77.C3371.051

79.33719.L01
 2ND = 77.C3371.051

79.33719.L01
 2ND = 77.C3371.051

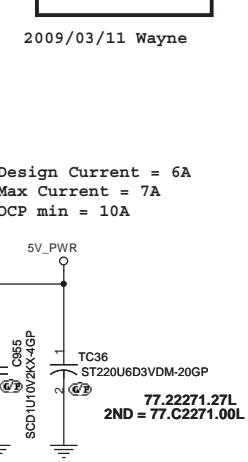
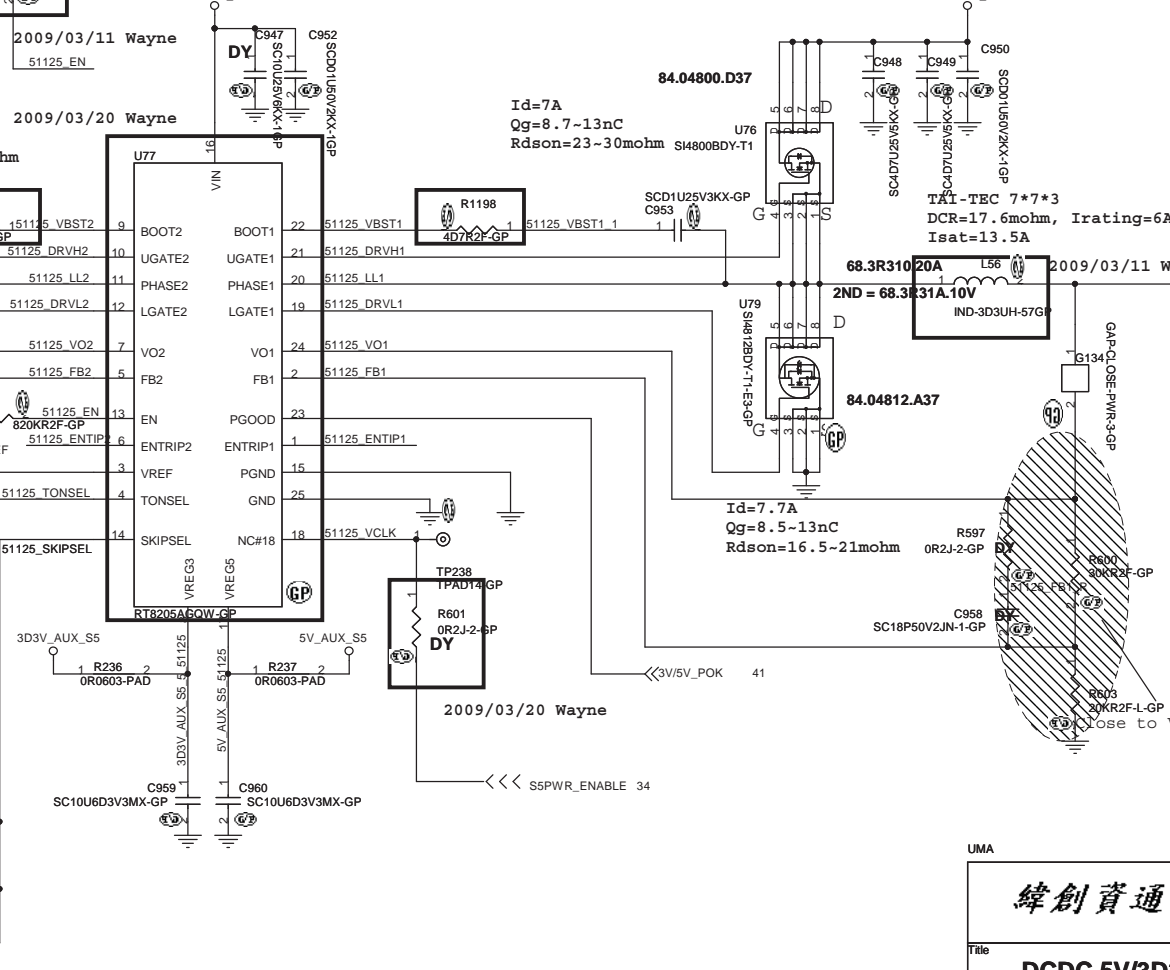
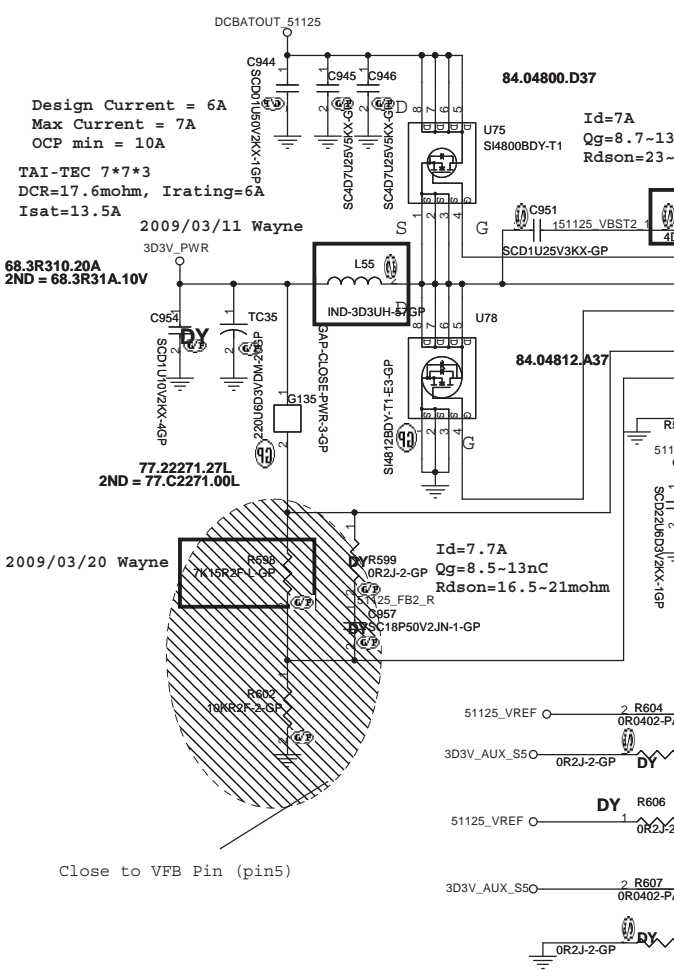
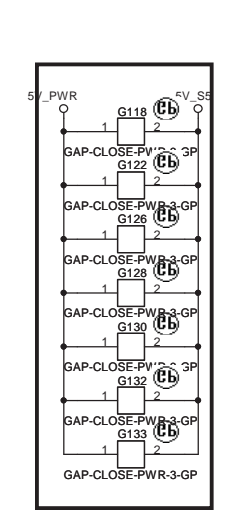
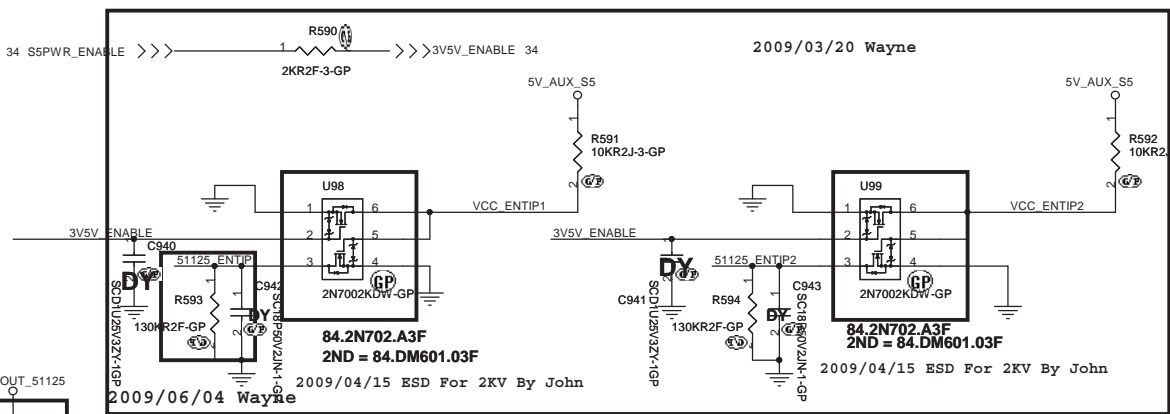
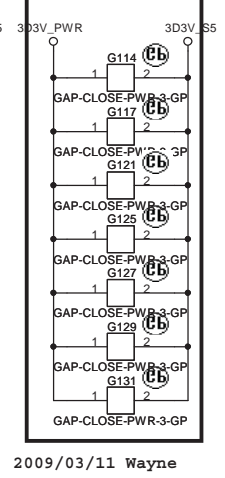
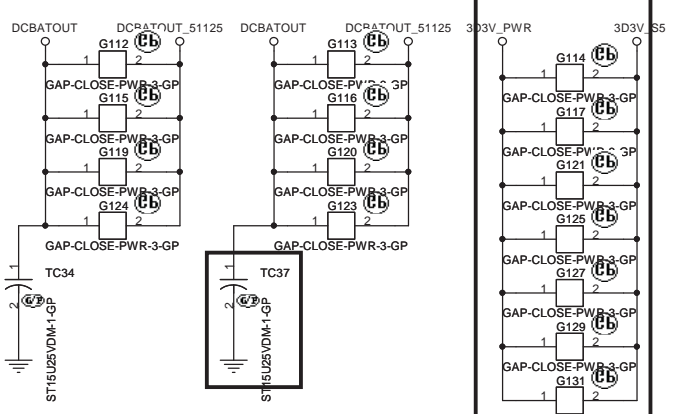
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU Vcore(ISL6265HR)**

Size: A3 Document Number: **JV71-TR** Rev: SA

Date: Monday, July 06, 2009 Sheet 44 of 61

<http://hobi-elektronika.net>



<http://hobi-elektronika.net>

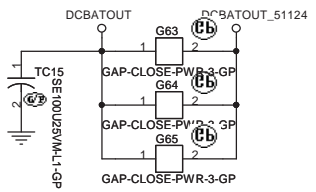
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

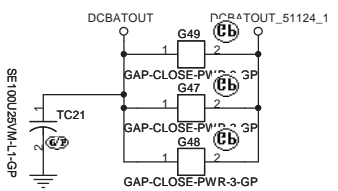
Title: DCDC 5V/3D3V (RT8205A)

Size A3 Document Number JV71-TR Rev SA

Date: Monday, July 06, 2009 Sheet 45 of 61



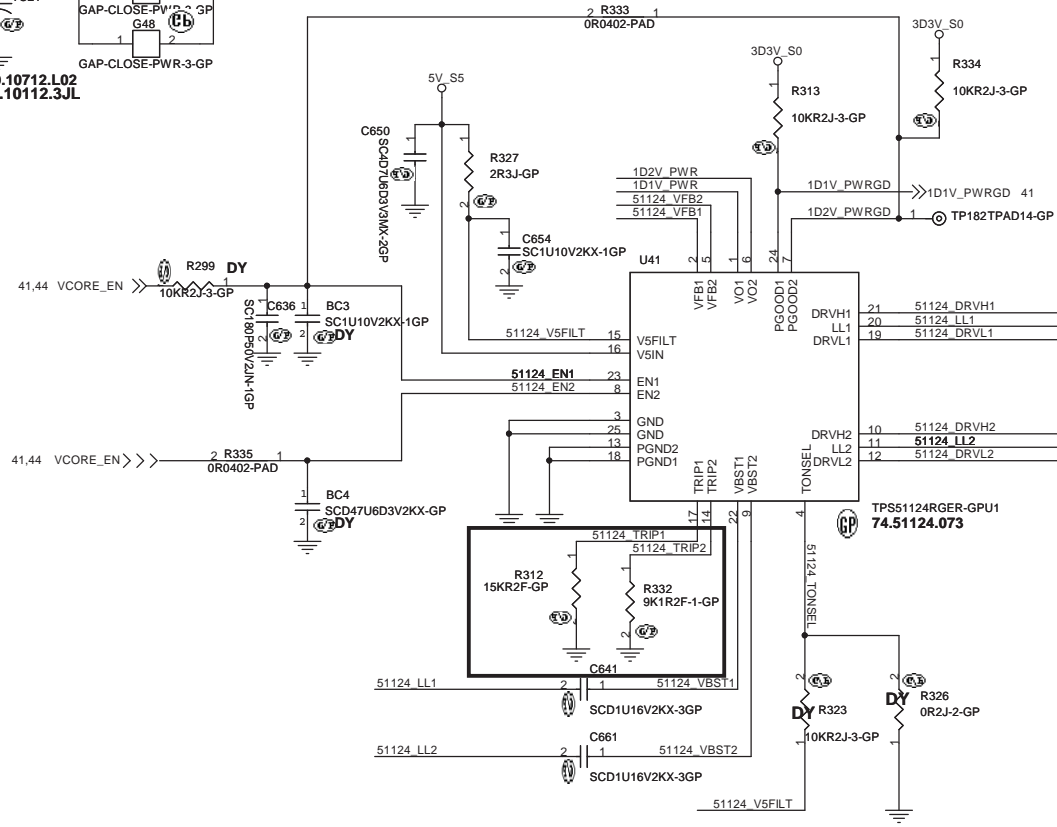
79.10712.L02
2ND = 79.10112.3JL



79.10712.L02
2ND = 79.10112.3JL

$$V_{trip} (mV) = R_{trip} (Kohm) * 10 (uA)$$

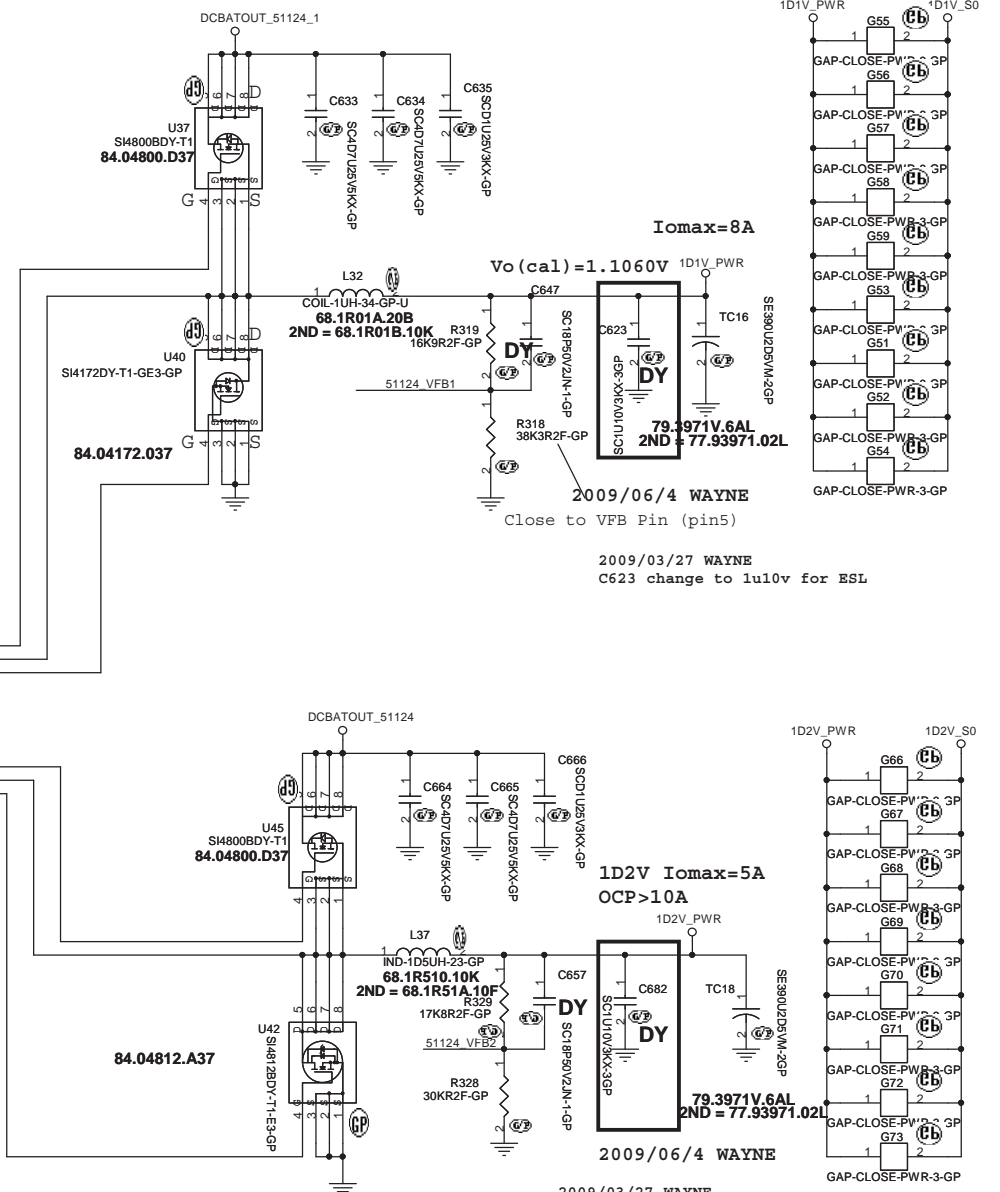
$$I_{ocp} = (V_{trip} / R_{dson}) + ((1 / (2 * L * f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in})$$



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1 + R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1 + R2) / R2$ --> Skip Mode

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$I_{omax} = 8A$

$V_o (cal) = 1.1060V$

2009/06/4 WAYNE
Close to VFB Pin (pin5)

2009/03/27 WAYNE
C623 change to 1u10v for ESL

$I_{omax} = 5A$
 $OCP > 10A$

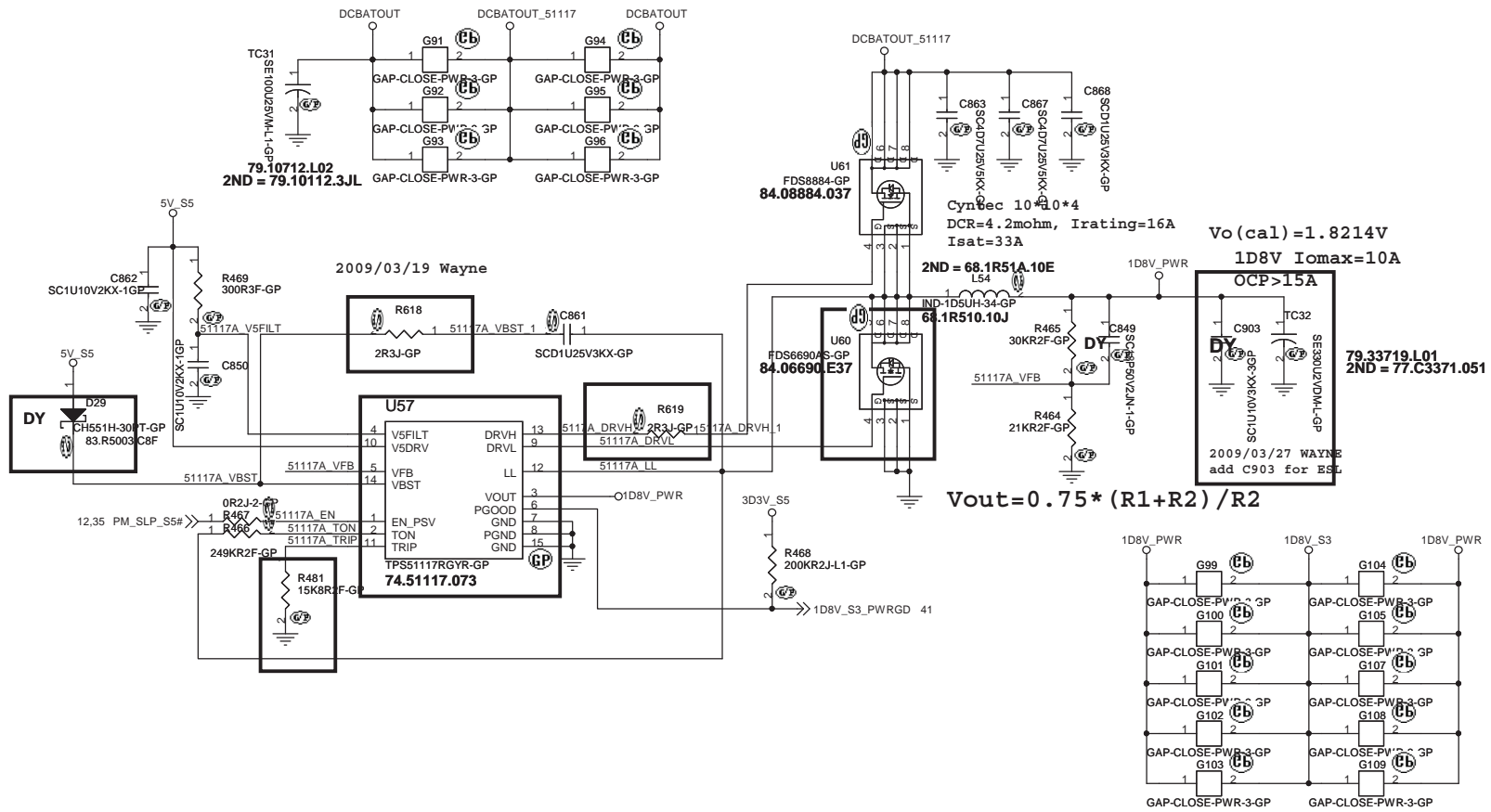
2009/06/4 WAYNE
2009/03/27 WAYNE
C682 change to 1u10v for ESL

UMA

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51124 1D1V 1D2V**

Size: A3	Document Number: JV71-TR	Rev: SA
Date: Monday, July 06, 2009	Sheet: 46 of 61	



79.10712.L02
2ND = 79.10112.3JL

84.08884.037

CynSec 10#10*4
DCR=4.2mohm, Irating=16A
Isat=33A

Vo(cal)=1.8214V
1D8V Iomax=10A
OCP>15A

79.33719.L01
2ND = 77.C3371.051

$V_{out} = 0.75 * (R1 + R2) / R2$

DDR_0.9V

Iomax=1.5A
OCP>3A

74.09026.079
2ND = 74.02997.A79

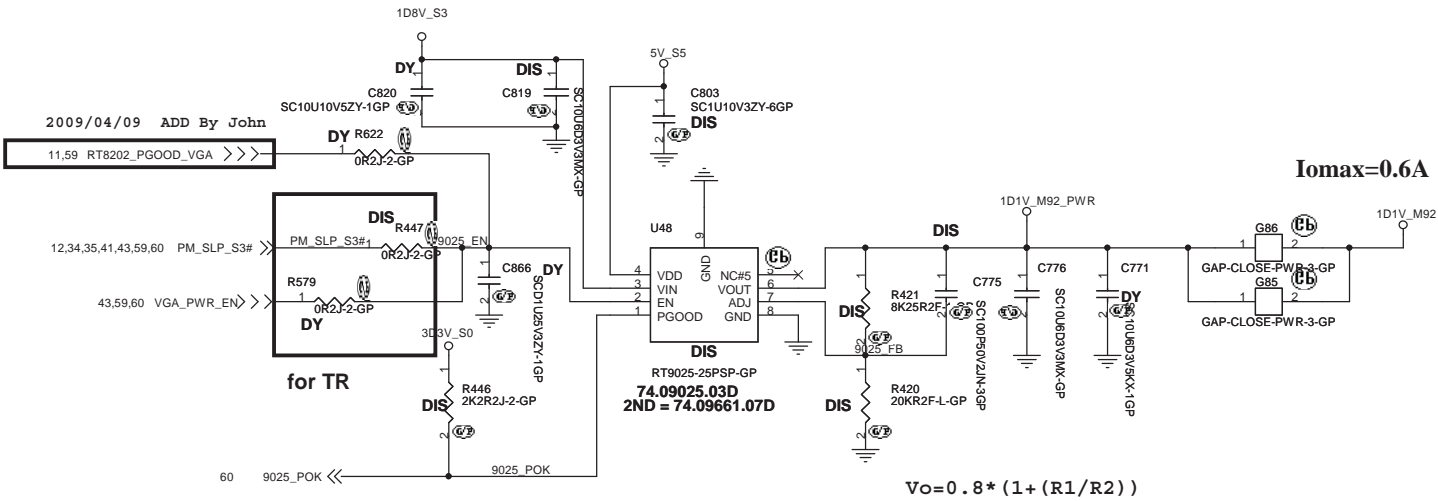
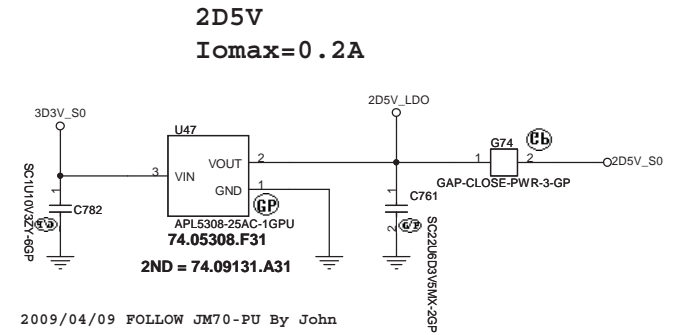
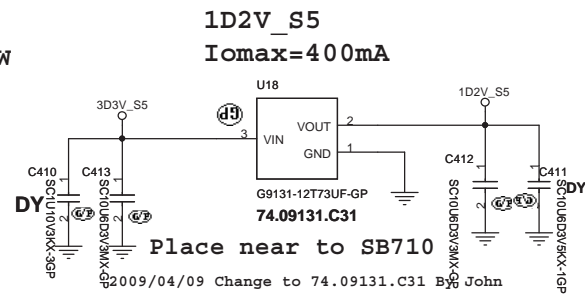
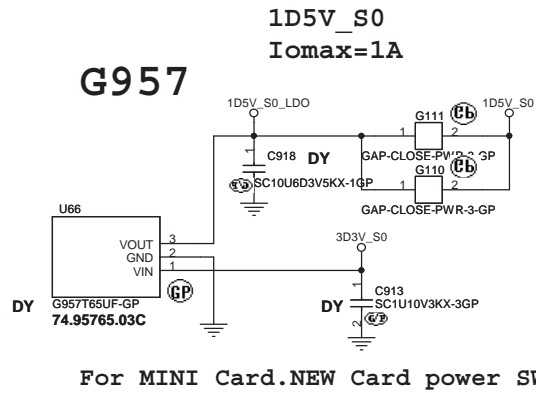
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCDC 1D8V APW7141/LDO 0D9V**

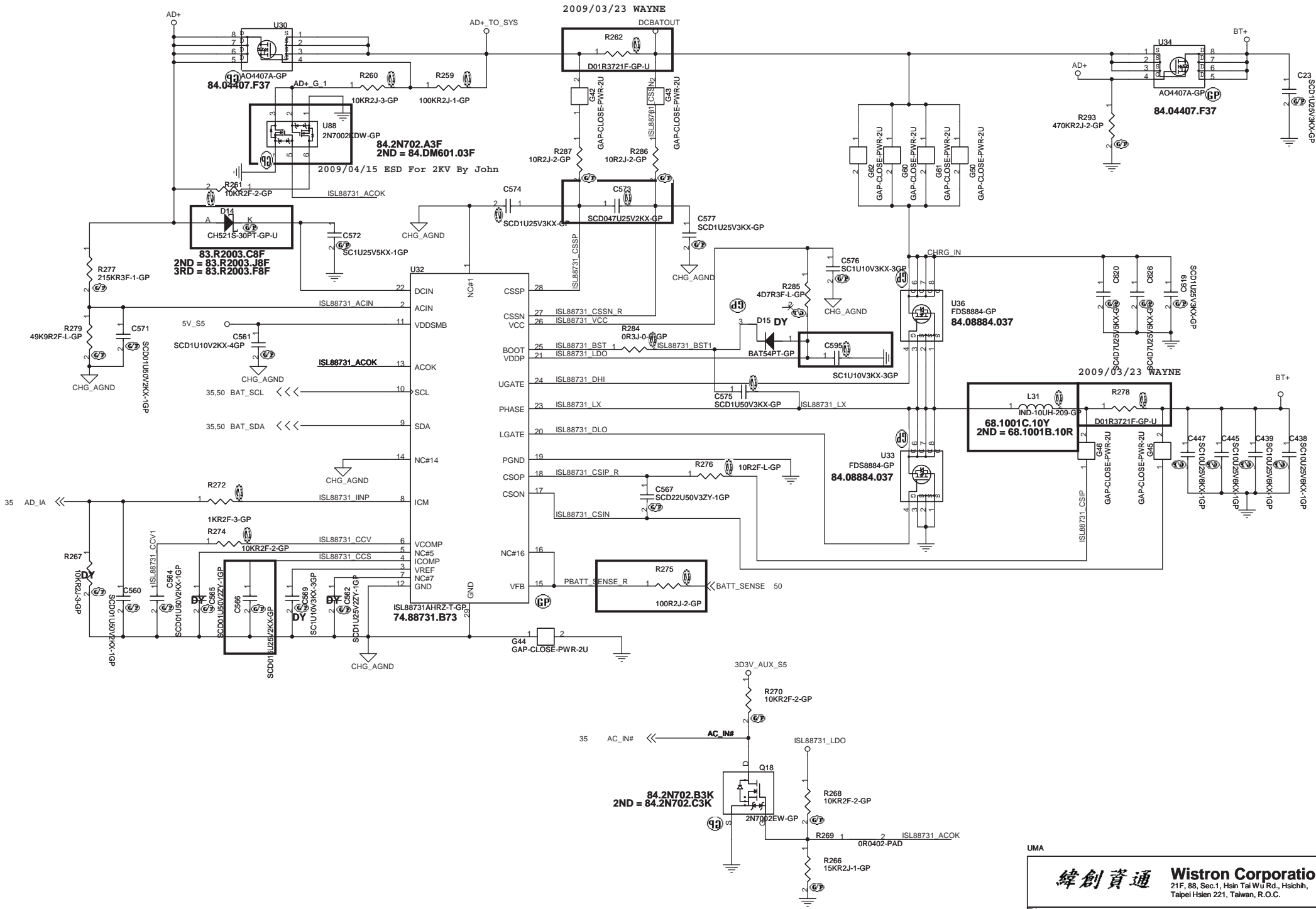
Size: A3 Document Number: **JV71-TR** Rev: SA

Date: Monday, July 06, 2009 Sheet: 47 of 61



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UMA	
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LDO 2D5V/1D5V/1D2V S5/1D1V M92
Size	Document Number
A3	JV71-TR
Date	Rev
Monday, July 06, 2009	SA
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48	61



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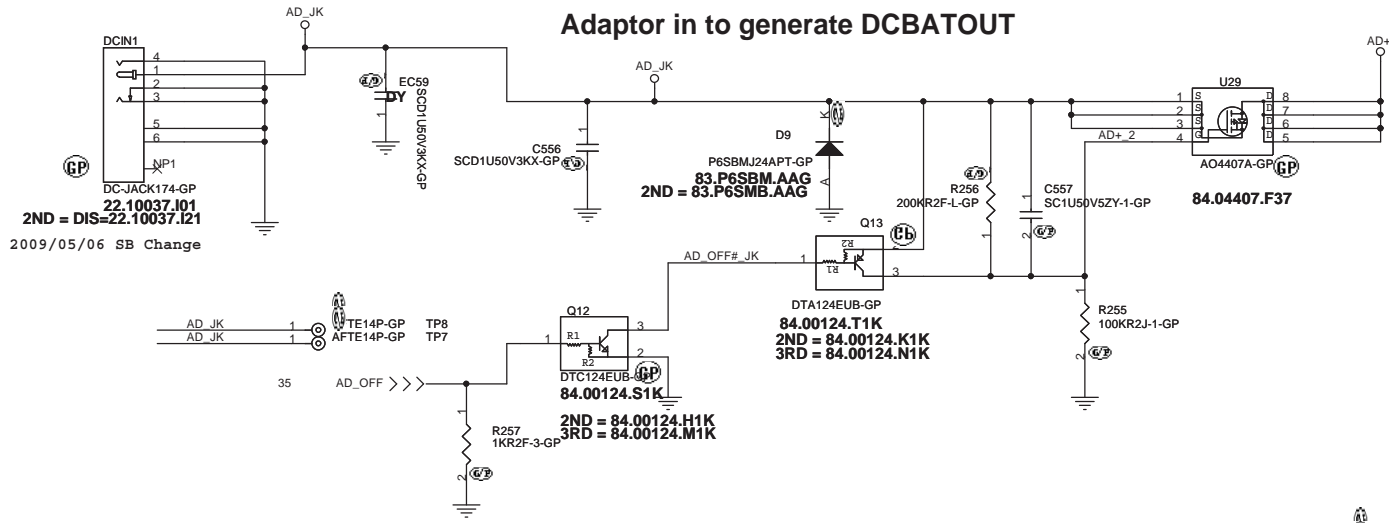
UMA

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

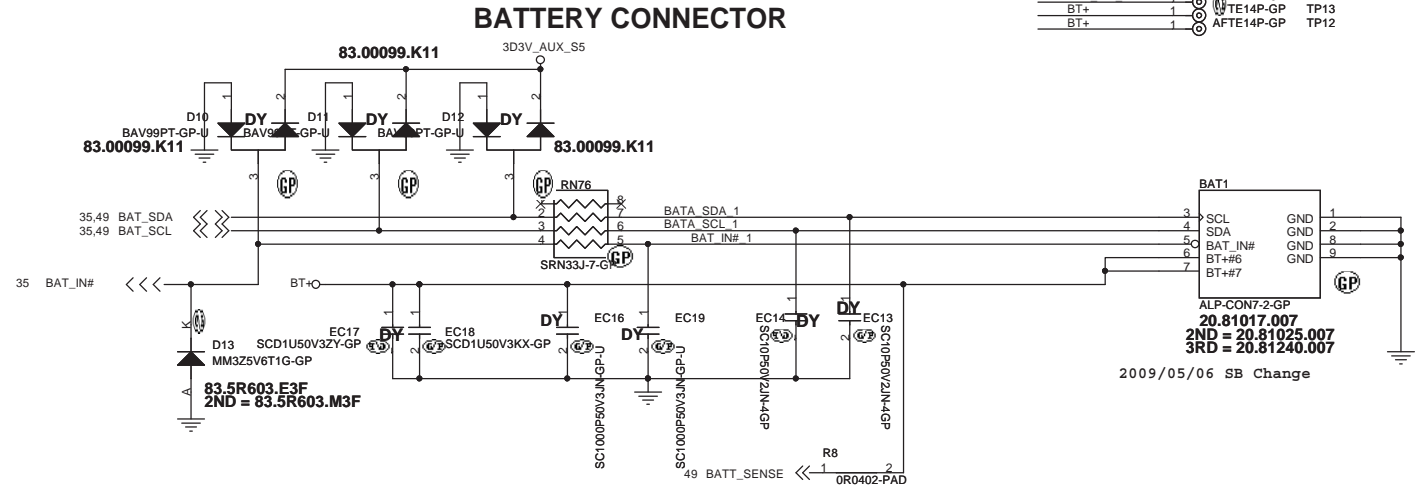
Title: **ISL88731A Charger**

Size A3 Document Number: **JV71-TR** Rev SA

Date: Monday, July 06, 2009 Sheet 49 of 61



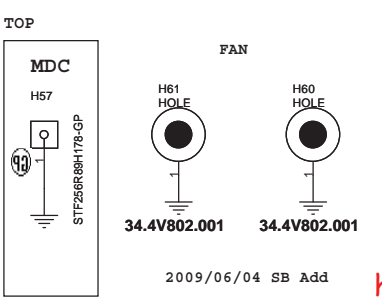
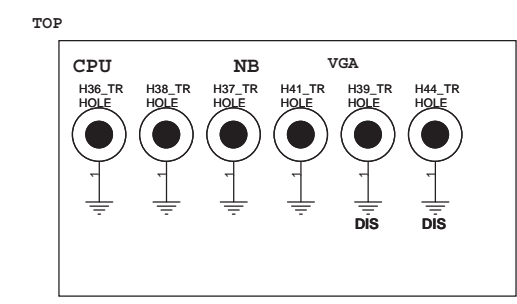
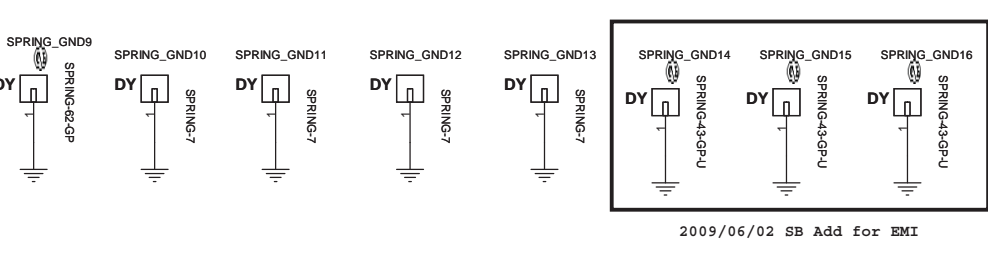
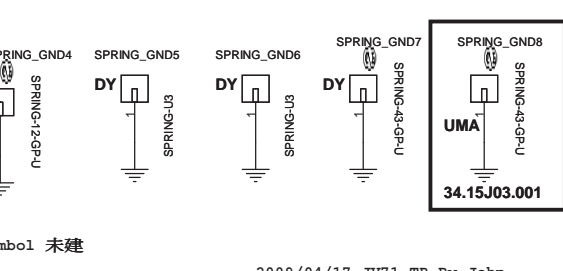
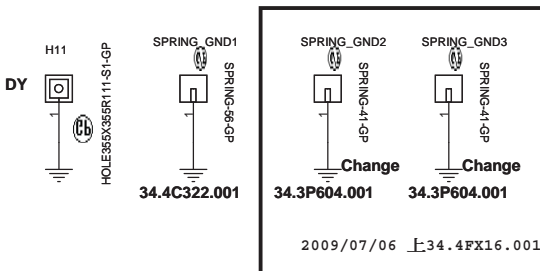
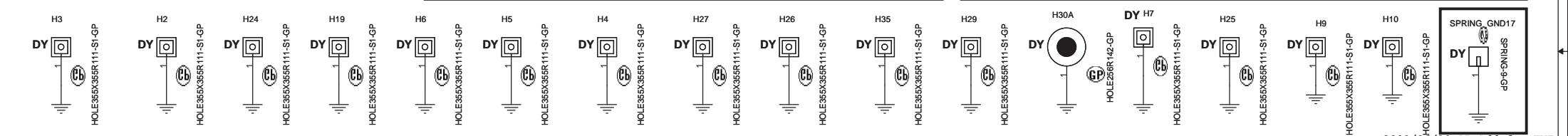
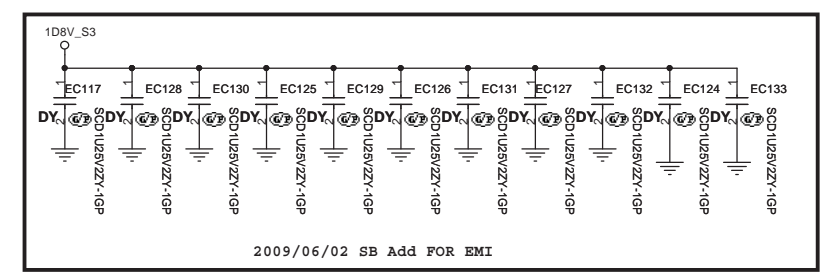
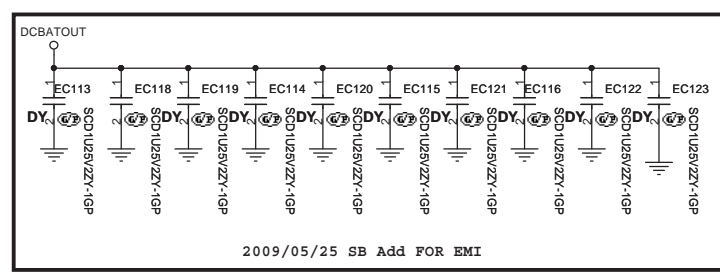
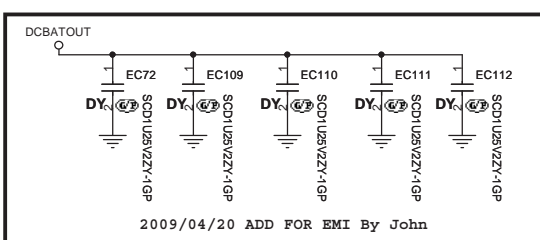
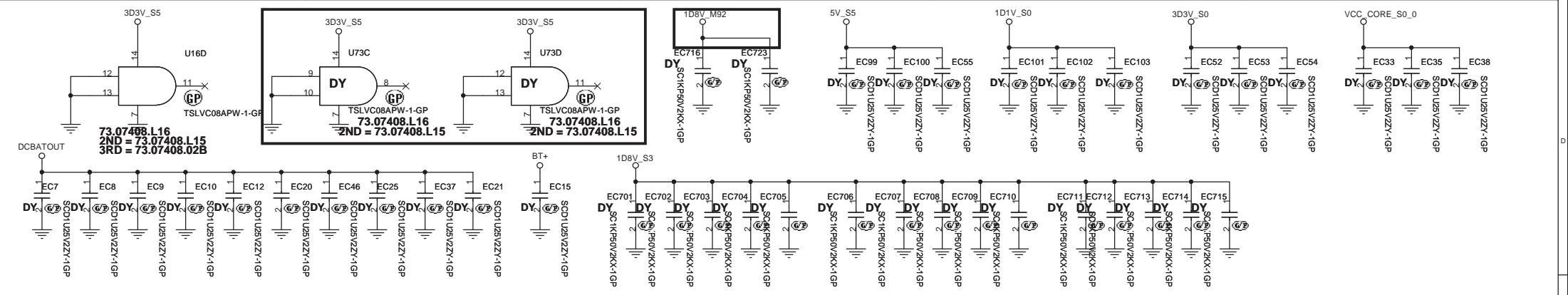
BATA_SDA_1	1	TE14P-GP	TP9
BATA_SCL_1	1	TE14P-GP	TP10
BAT_IN#_1	1	TE14P-GP	TP11
BT+	1	TE14P-GP	TP13
BT+	1	AFTE14P-GP	TP12



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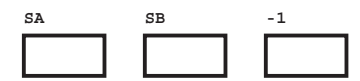
UMA	
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title AD/BATT CONN	
Size	Document Number
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SB



Check test point

3D3V_S0	TP233	TPAD14-GP
3D3V_AUX_S5	TP232	TPAD14-GP
3D3V_S5	TP231	TPAD14-GP
5V_S5	TP230	TPAD14-GP
12,35 PM_PWRBTN#	TP229	TPAD14-GP
6,11 CPU_PWRGD	TP228	TPAD14-GP
34,35 SS_ENABLE	TP227	TPAD14-GP
6,11 CPU_LDT_RST#	TP226	TPAD14-GP



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Test Point放在Dimm Door打開可量測處

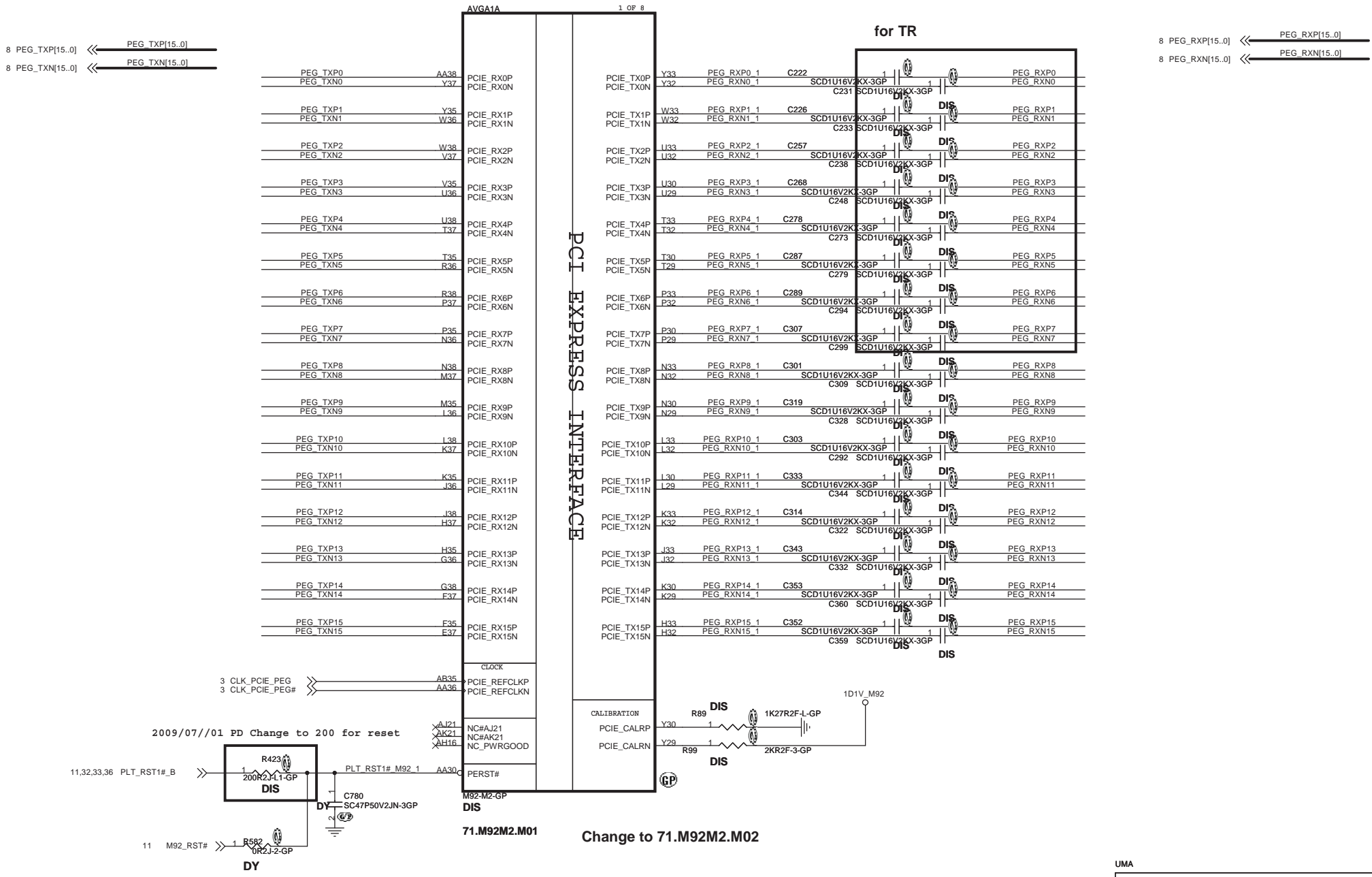
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **EMI/Spring/Boss**

Size: Document Number **JV71-TR** Rev **SB**

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2009/07//01 PD Change to 200 for reset

Change to 71.M92M2.M02

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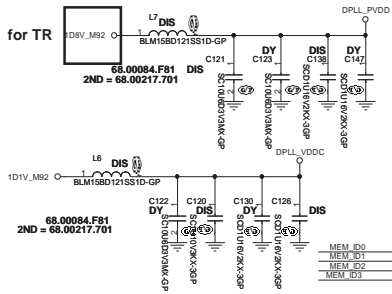
UMA

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **M92 PCIE**

Size A3 Document Number **JV71-TR** Rev **SB**

Date: Monday, July 06, 2009 Sheet 52 of 61

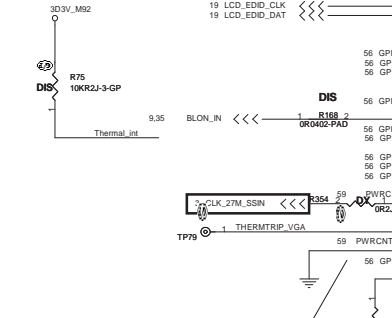


DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request

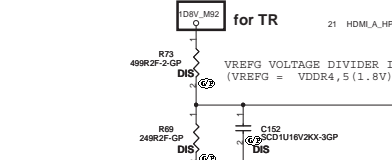
DVPDATA [3:0]

0100 512MB Hynix-H5PS1G63EPR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G16C2F-20 (500MHz)

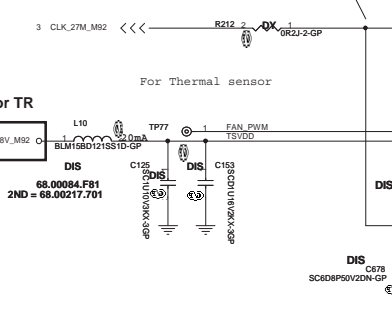
It's strap for GDDR3-136ball
Need to Clarify



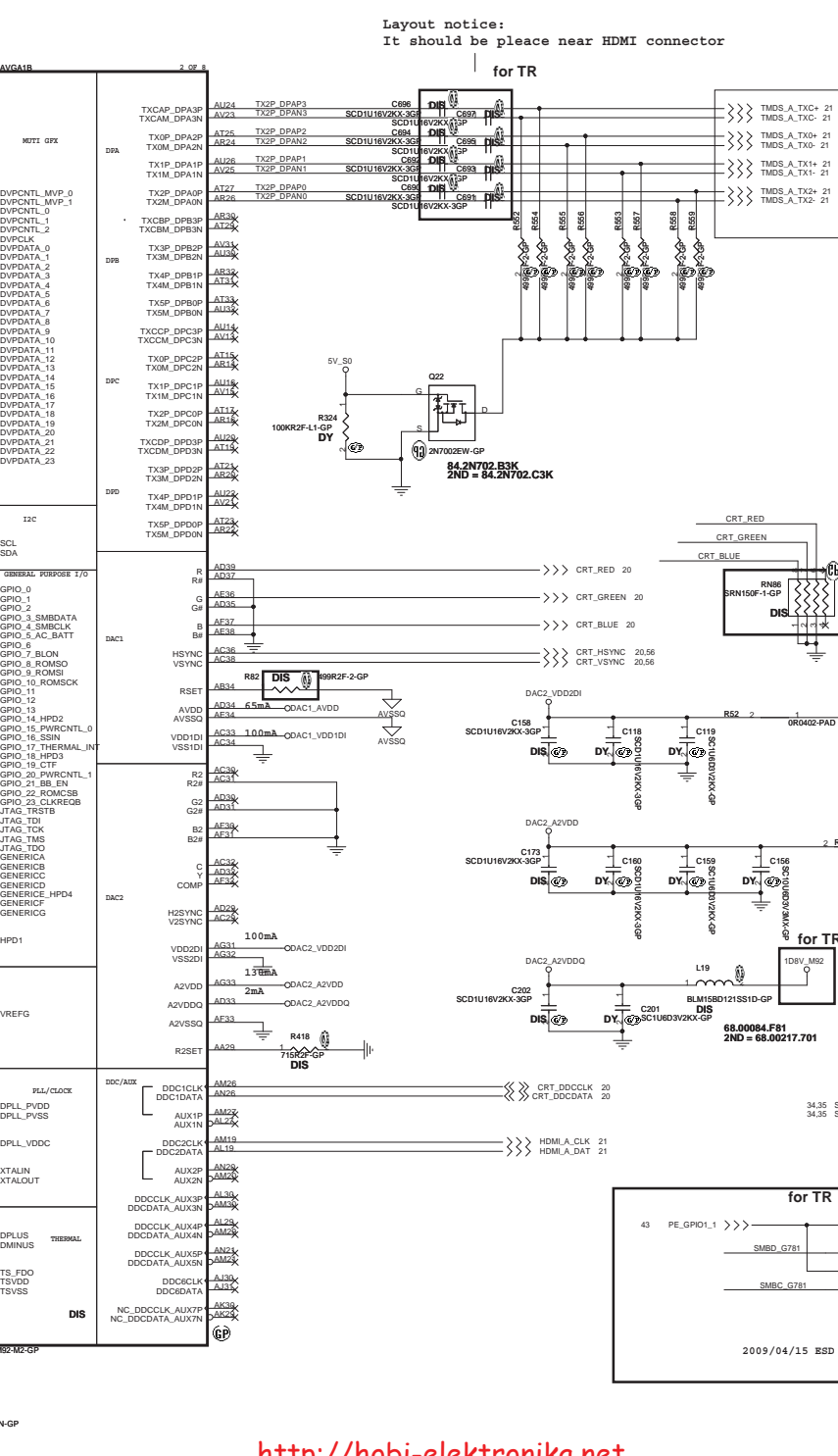
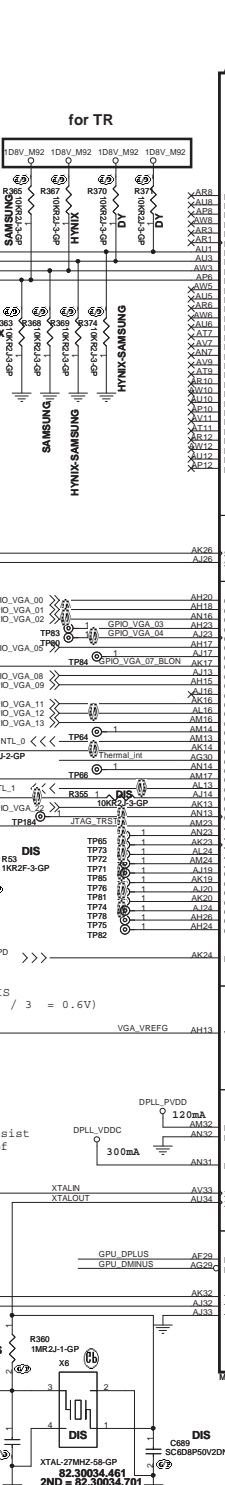
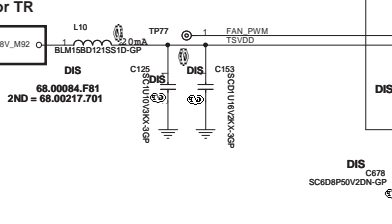
Back Bias (body bias) which minimizes power consumption in battery modes.
PD = Disable
PU = Enable



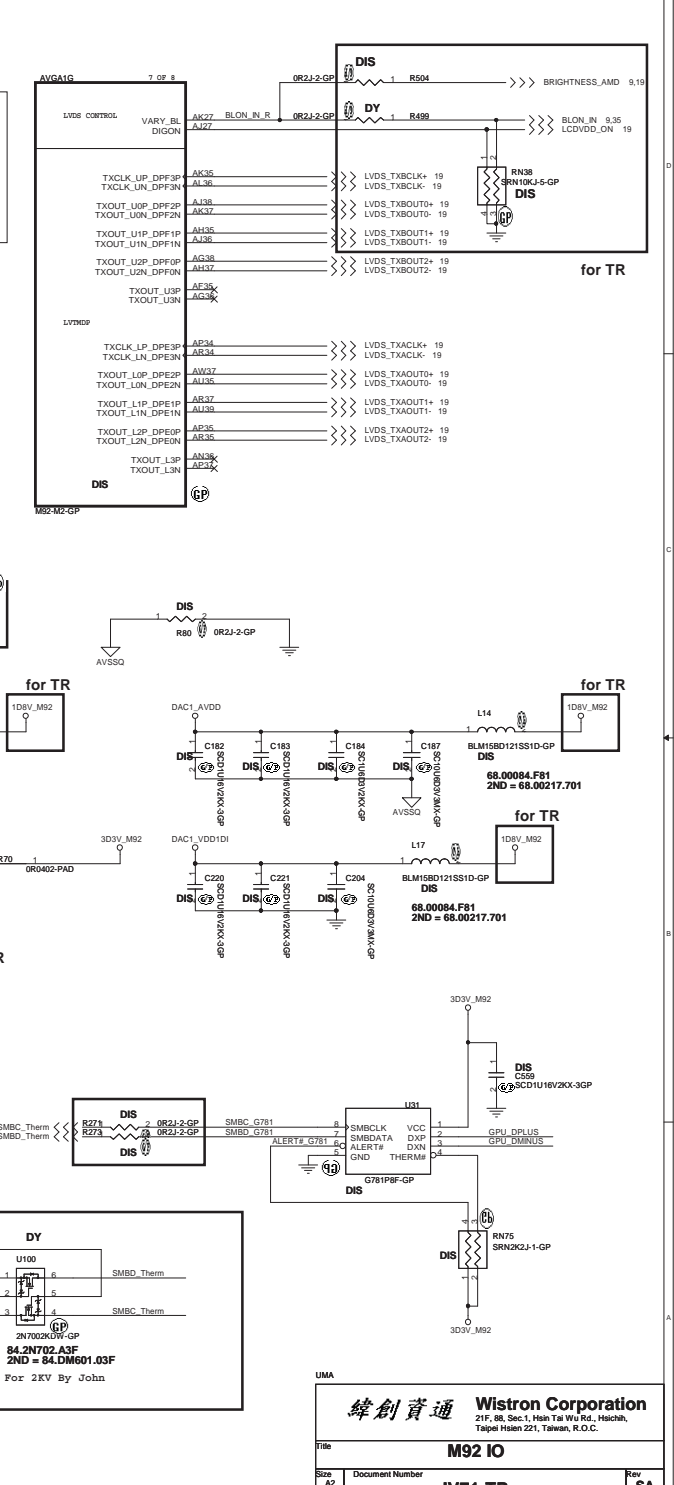
Depending on OSC used select voltage divider resist values R25 R70 to ensure XTALIN voltage level of 1.8V



For Thermal sensor

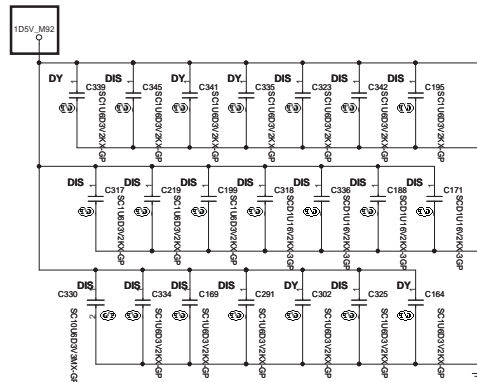


Layout notice:
It should be placed near HDMI connector

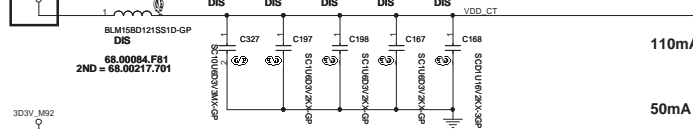


<http://hobi-elektronika.net>

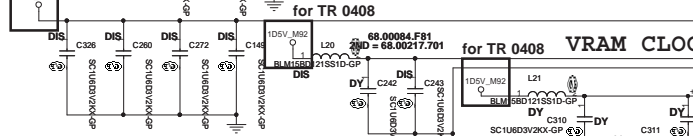
for TR 0408 VDDR1+VDDRHX 1.50 V (DDR3 700 MHz) 0.93 A (RMS) / 1.2 A (peak)



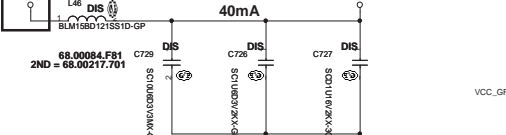
for TR 108V_M92



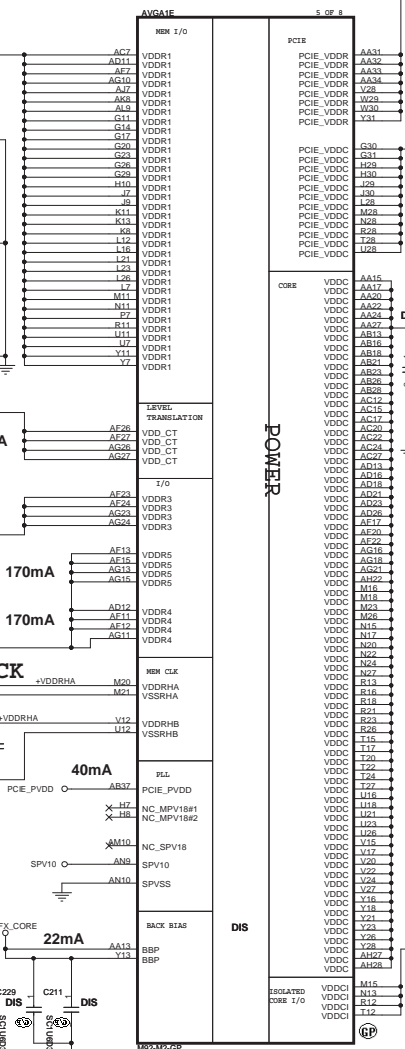
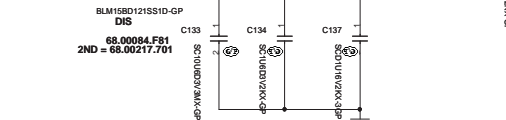
for TR 108V_M92



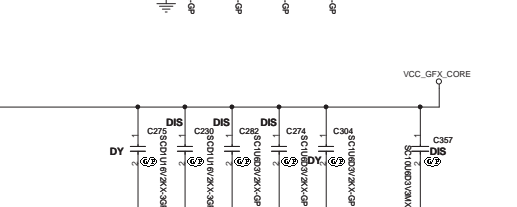
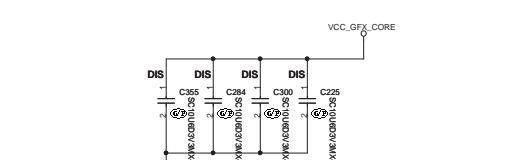
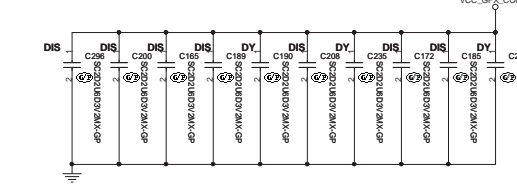
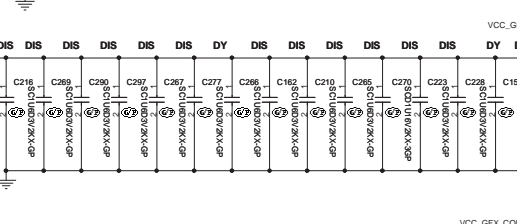
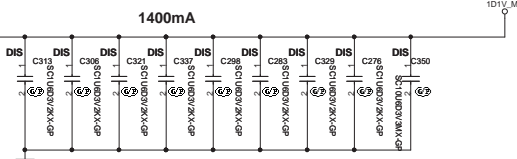
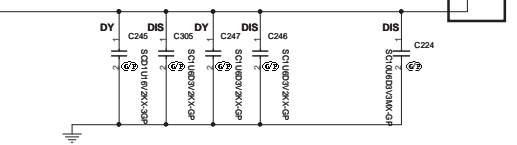
for TR 108V_M92

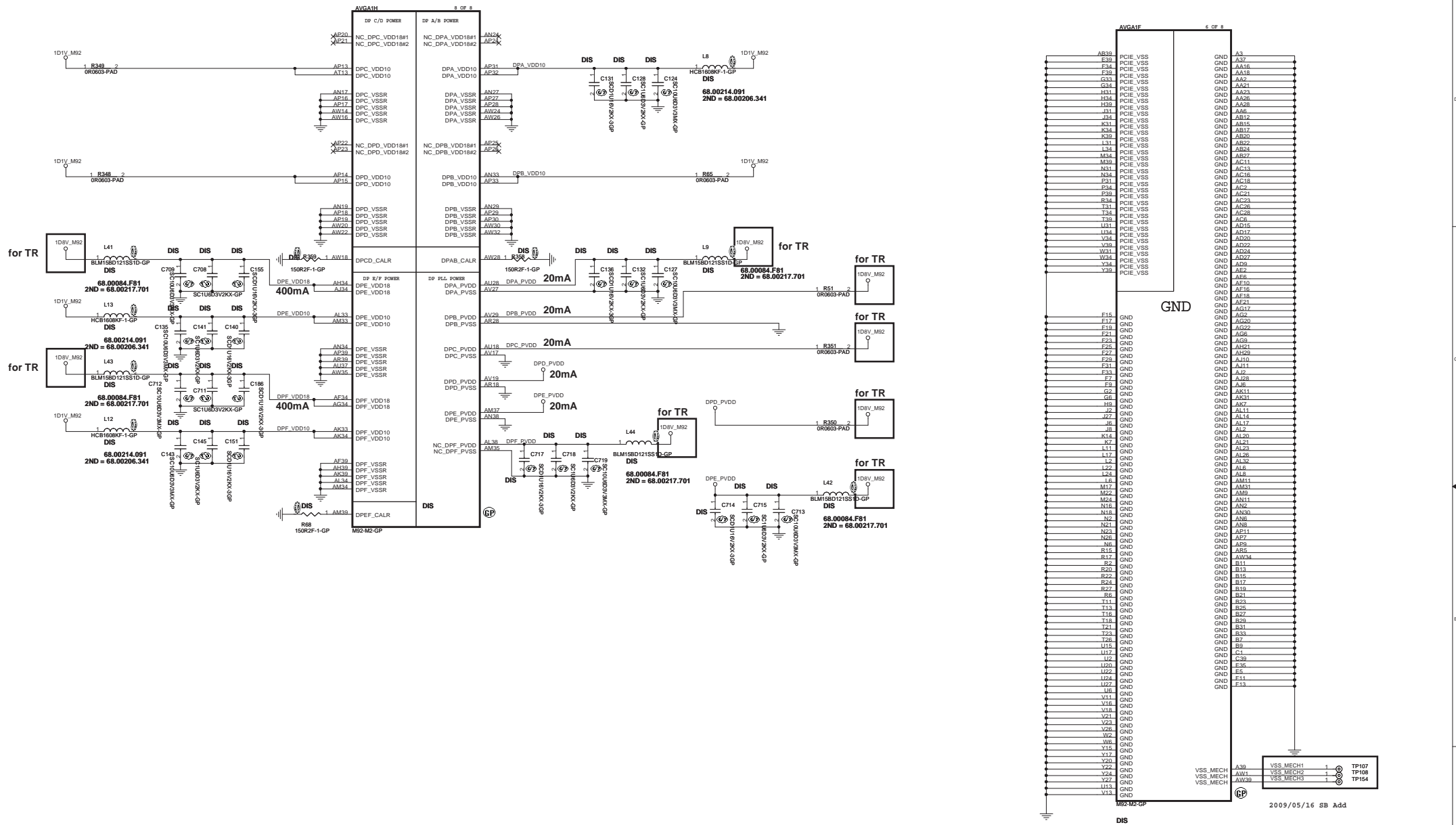


for TR 108V_M92



for TR 108V_M92





VSS_MECH	AW3	VSS_MECH1	1	TP107
VSS_MECH	AW1	VSS_MECH2	1	TP108
VSS_MECH	AW33	VSS_MECH3	1	TP154

2009/05/16 SB Add

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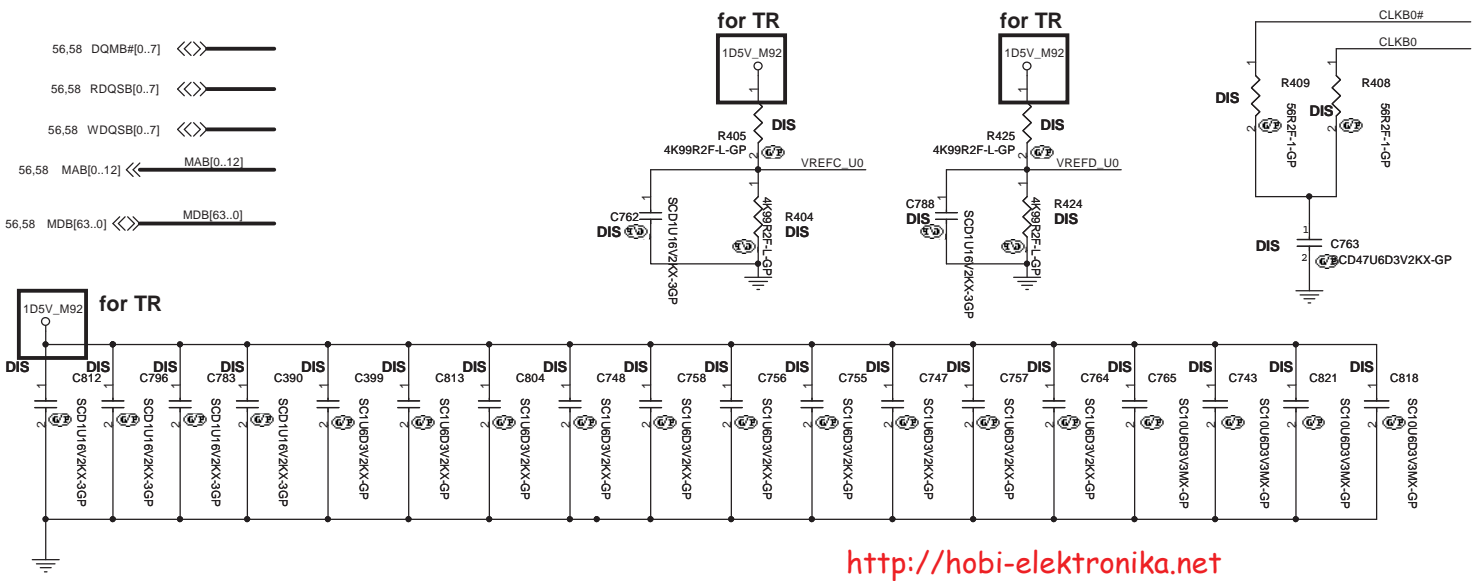
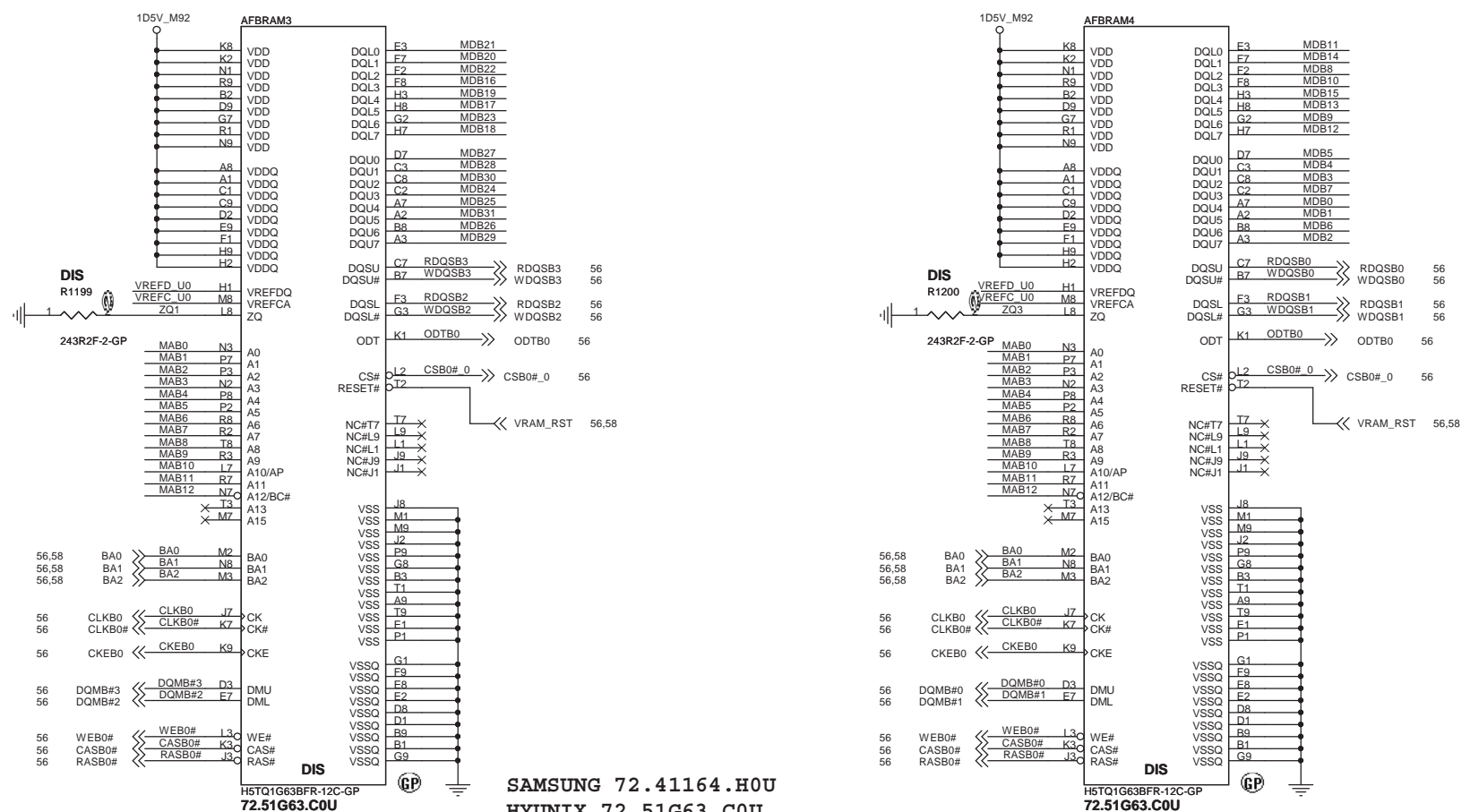
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

File: **DP POWER_GND**

Size: A2 Document Number: **JV71-TR** Rev: SA

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DDR3



<http://hobi-elektronika.net>

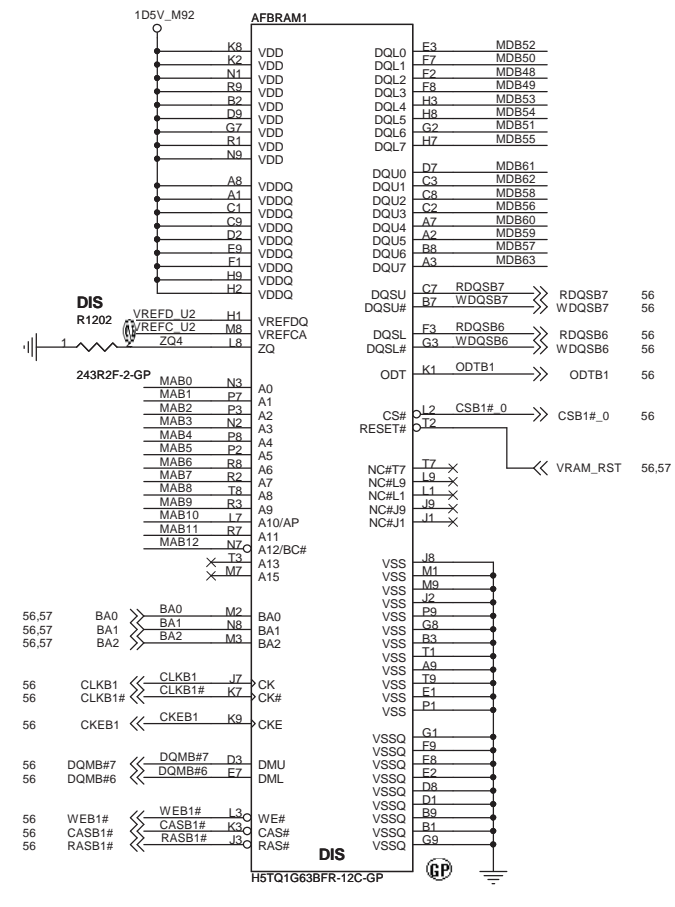
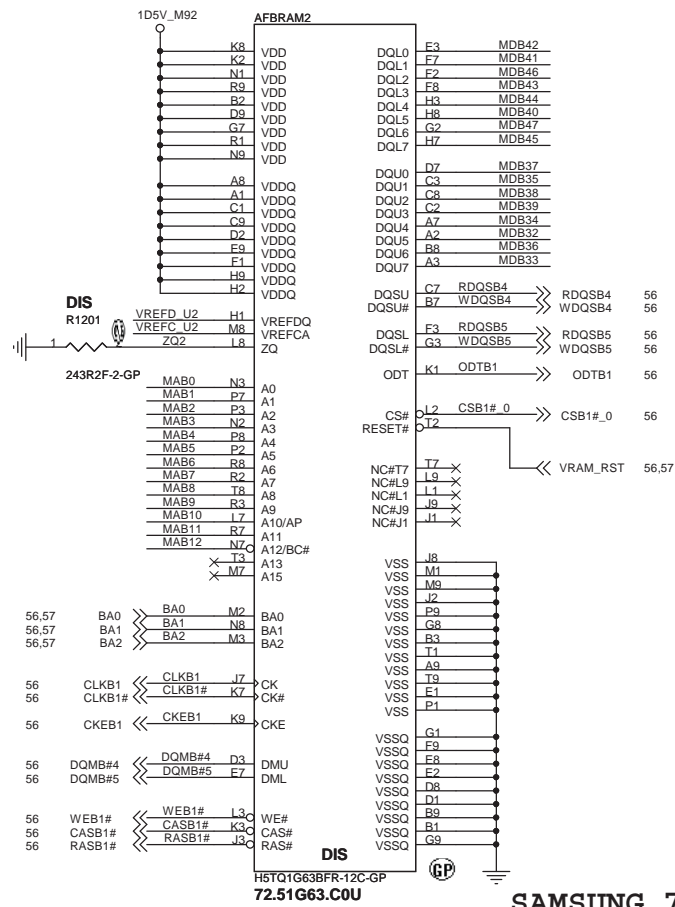
UMA

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

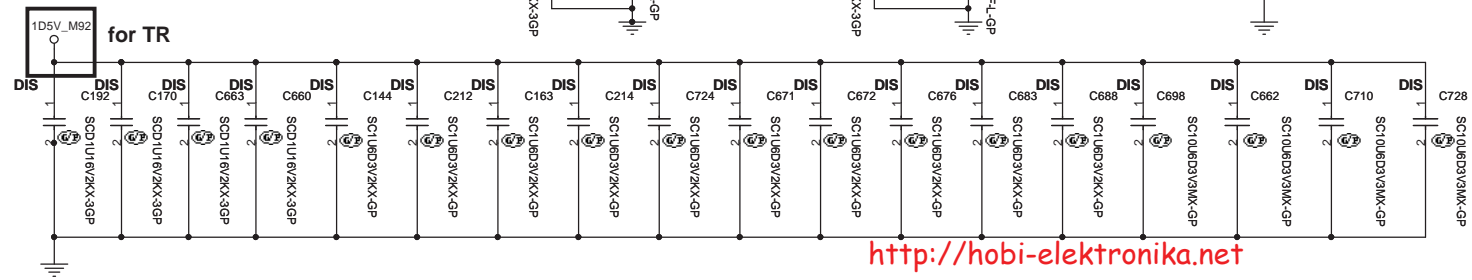
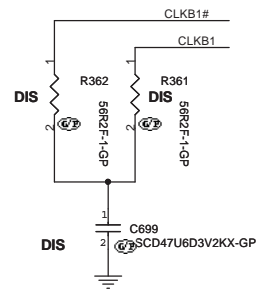
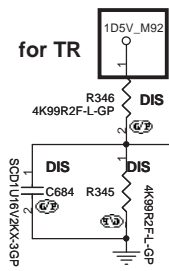
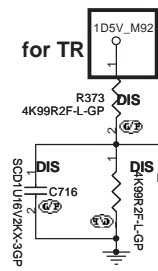
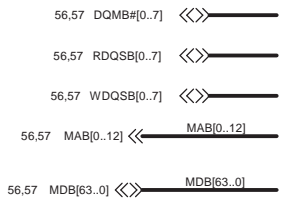
File: DDR3 B0

Size A3 Document Number **JV71-TR** Rev **SB**

Date: Monday, July 06, 2009 Sheet 57 of 61



SAMSUNG 72.41164.H0U
HYUNIX 72.51G63.C0U



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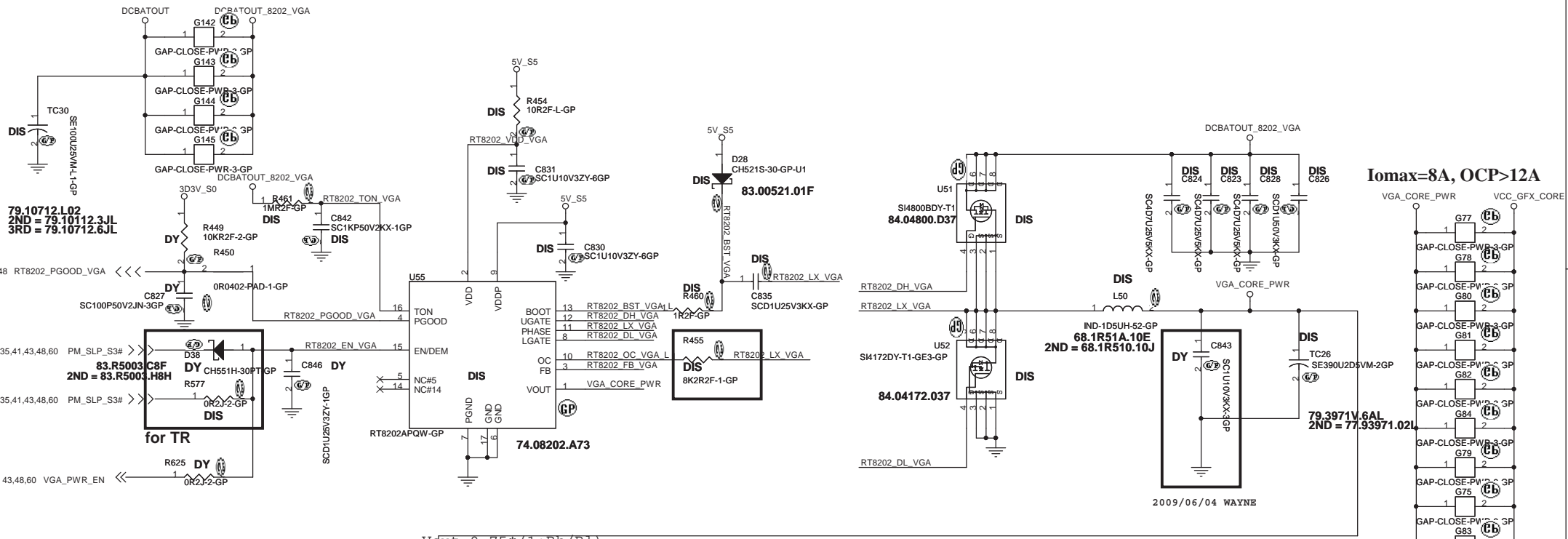
UMA

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **M92 DDR3 B1**

Size A3 Document Number **JV71-TR** Rev **SB**

Date: Monday, July 06, 2009 Sheet 58 of 61

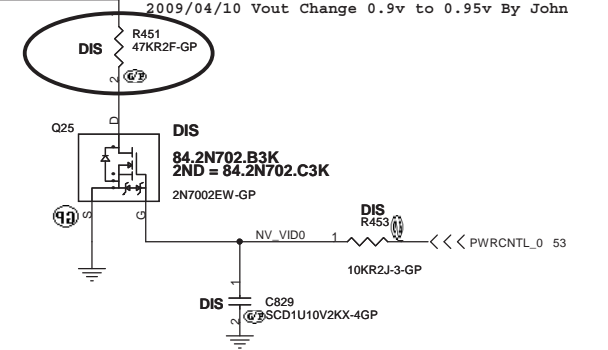
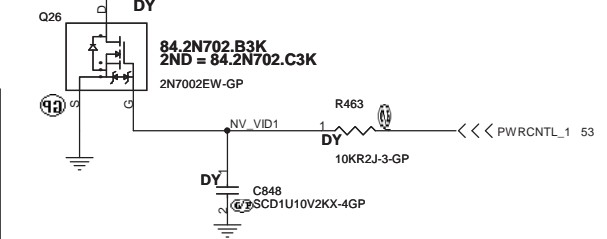
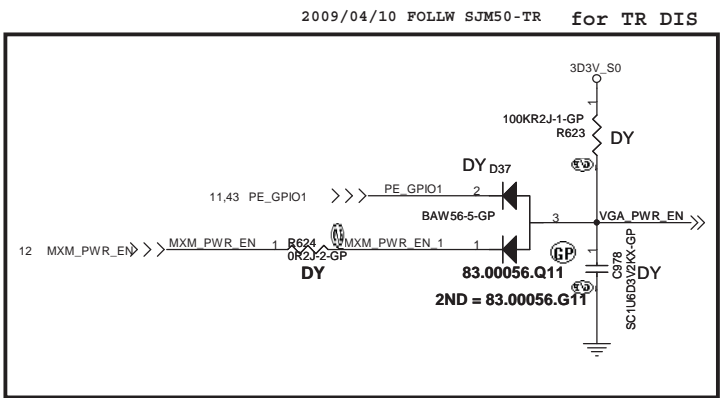


11,48 RT8202_PG0OD_VGA <<<
 12,34,35,41,43,48,60 PM_SLP_S3# >>>
 12,34,35,41,43,48,60 PM_SLP_S3# >>>
 43,48,60 VGA_PWR_EN <<<

for TR
 83.R5003.C8F
 2ND = 83.R5003.H8H
 83.R5003.H8H
 2ND = 83.00056.G11

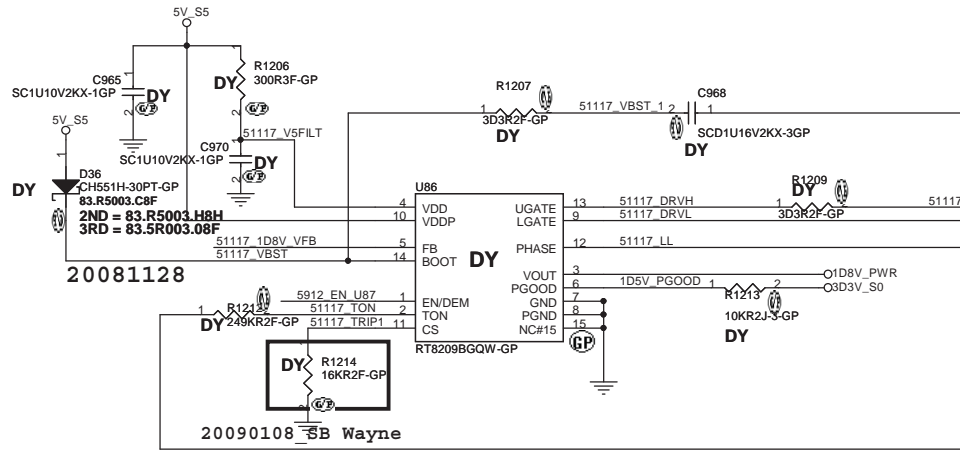
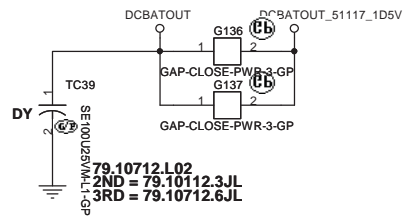
$V_{out} = 0.75 * (1 + R_h/R_l)$
 2009/04/10 Vout Change 0.9v to 0.95v By John

2009/04/10 Vout Change 0.9v to 0.95v By John

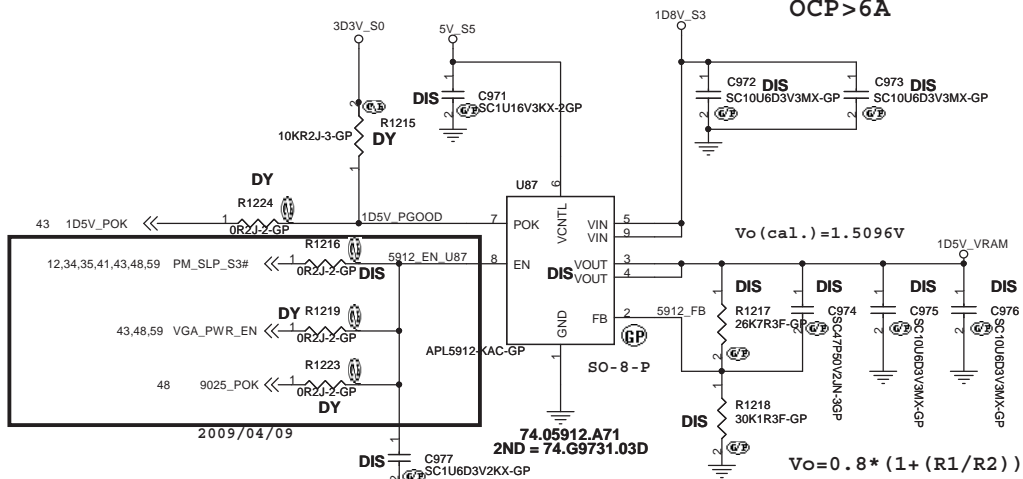


<http://hobi-elektronika.net>

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緯創資通 Wistron Corporation		
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
RT8202A VGA CORE		
Size A3	Document Number	Rev SA
JV71-TR		
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