

Compal Confidential

KAW60 Schematics Document

AMD AM2 / RS690MC / SB600

2008 / 08 / 08

Rev:1.0

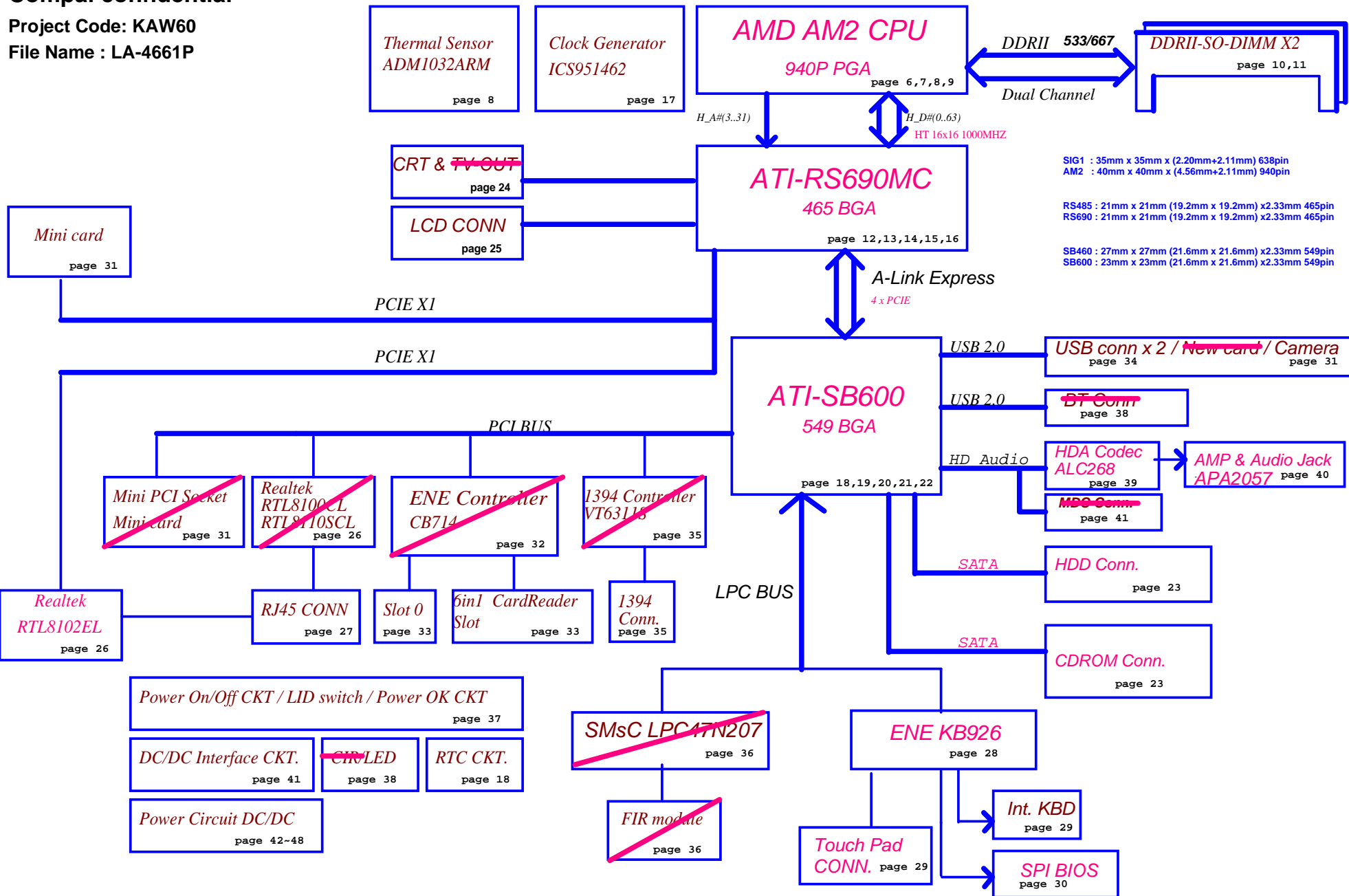
FOR Pre-MP

Security Classification	Compal Secret Data			Title		
Issued Date	2005/05/09	Deciphered Date	2006/03/08	Cover Sheet		
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				Date	Friday, August 08, 2008	Sheet 1 of 50

Compal confidential

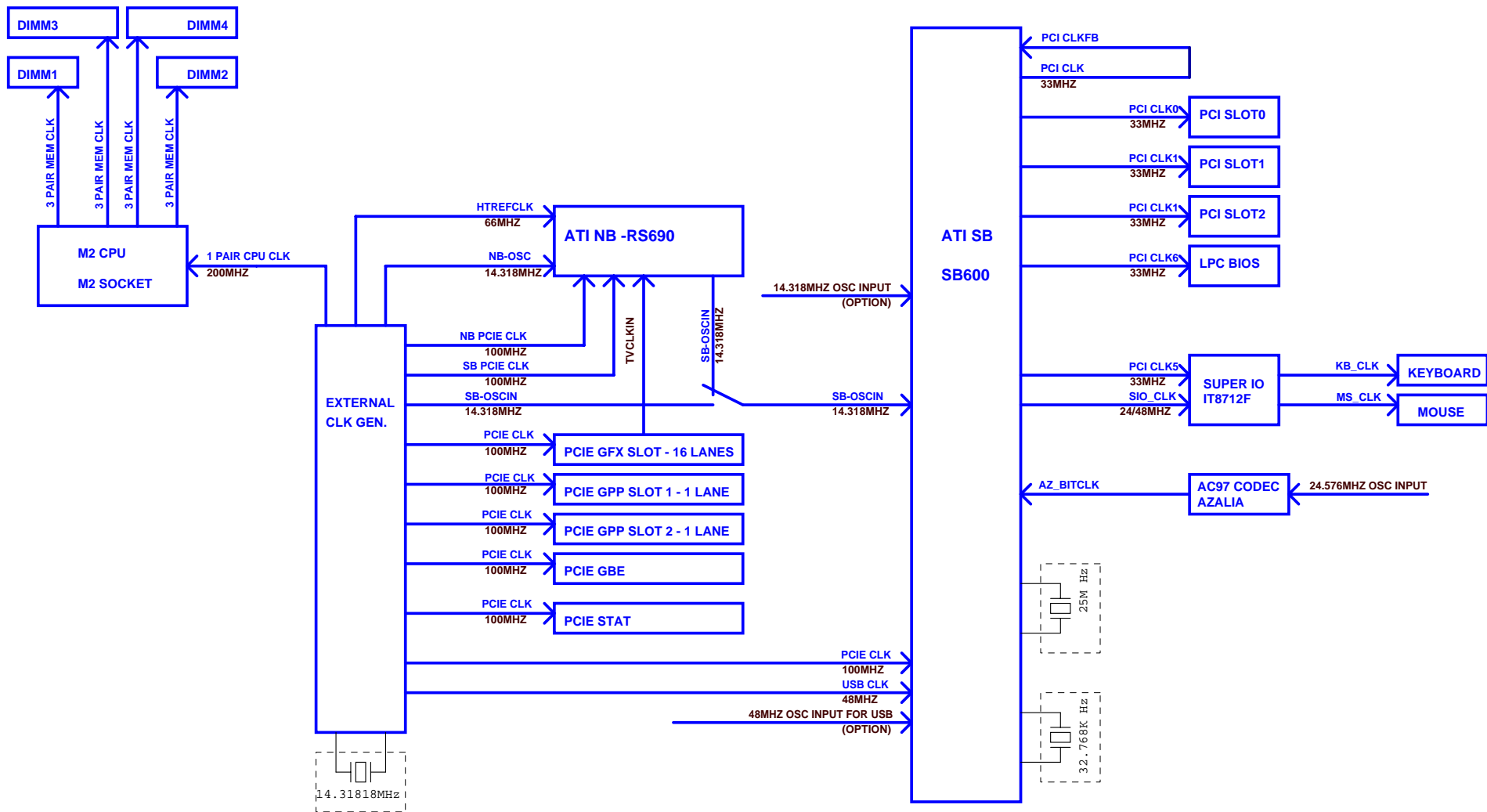
Project Code: KAW60

File Name : LA-4661P

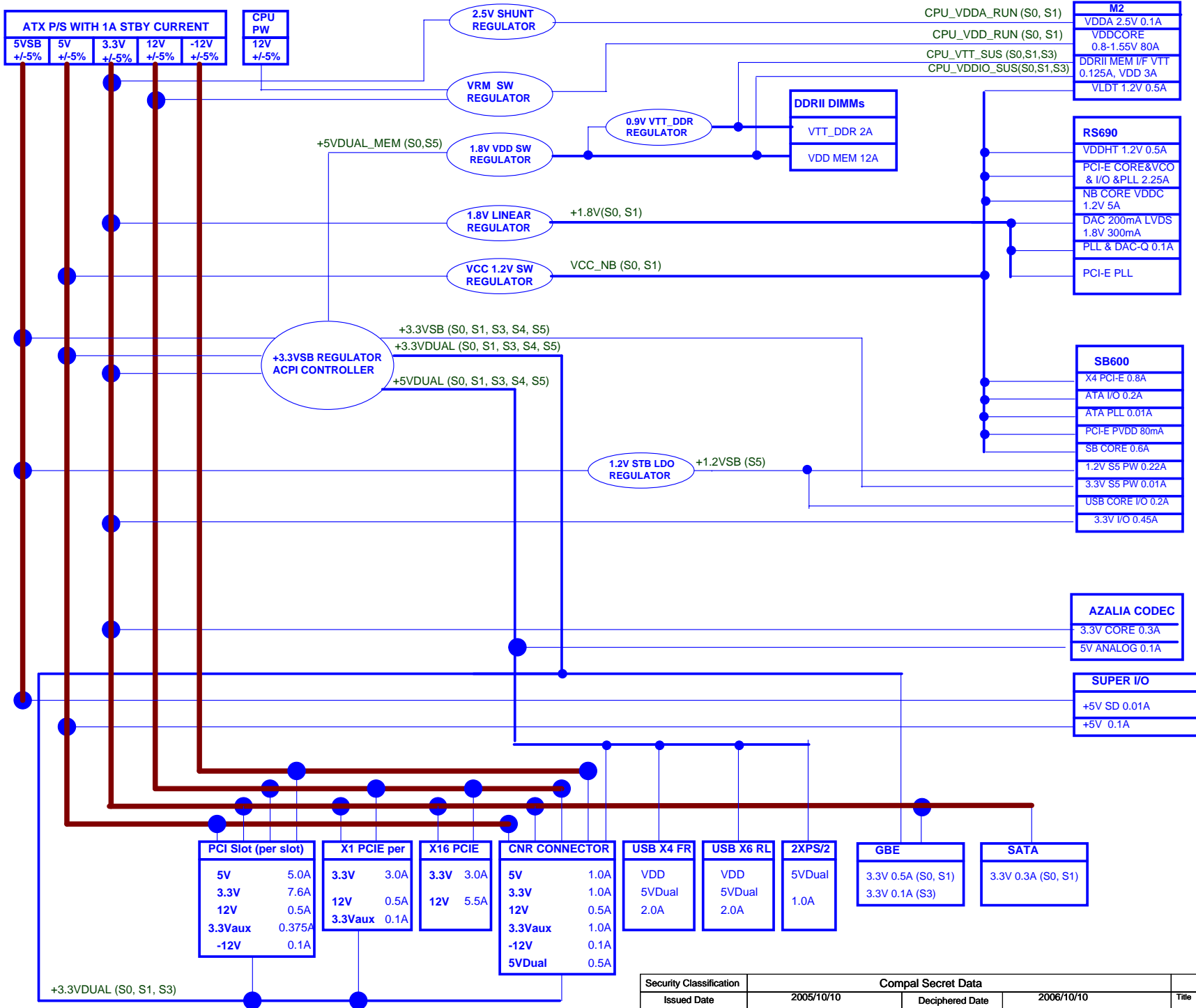


SIG1 : 35mm x 35mm x (2.20mm+2.11mm) 638pin
 AM2 : 40mm x 40mm x (4.56mm+2.11mm) 940pin
 RS485 : 21mm x 21mm (19.2mm x 19.2mm) x2.33mm 465pin
 RS690 : 21mm x 21mm (19.2mm x 19.2mm) x2.33mm 465pin
 SB460 : 27mm x 27mm (21.6mm x 21.6mm) x2.33mm 549pin
 SB600 : 23mm x 23mm (21.6mm x 21.6mm) x2.33mm 549pin

Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/08	Deciphered Date	2006/03/08	BLOCK DIAGRAM	
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				Rev	2.0



M2	
VDDA 2.5V	0.1A
VDDCORE	0.8-1.55V 80A
DDRII MEM I/F VTT	0.125A, VDD 3A
VLDI	1.2V 0.5A

RS690	
VDDHT	1.2V 0.5A
PCI-E CORE&VCO & I/O &PLL	2.25A
NB CORE VDDC	1.2V 5A
DAC	200mA LVDS 1.8V 300mA
PLL & DAC-Q	0.1A
PCI-E PLL	

SB600	
X4 PCI-E	0.8A
ATA I/O	0.2A
ATA PLL	0.01A
PCI-E PVDD	80mA
SB CORE	0.6A
1.2V S5 PW	0.22A
3.3V S5 PW	0.01A
USB CORE I/O	0.2A
3.3V I/O	0.45A

AZALIA CODEC	
3.3V CORE	0.3A
5V ANALOG	0.1A

SUPER I/O	
+5V SD	0.01A
+5V	0.1A

PCI Slot (per slot)	
5V	5.0A
3.3V	7.6A
12V	0.5A
3.3Vaux	0.375A
-12V	0.1A

X1 PCIE per	
3.3V	3.0A
12V	0.5A
3.3Vaux	0.1A

X16 PCIE	
3.3V	3.0A
12V	5.5A

CNR CONNECTOR	
5V	1.0A
3.3V	1.0A
12V	0.5A
3.3Vaux	1.0A
-12V	0.1A
5VDual	0.5A

USB X4 FR	
VDD	2.0A
5VDual	

USB X6 RL	
VDD	2.0A
5VDual	

2XPS/2	
5VDual	1.0A

GBE	
3.3V	0.5A (S0, S1)
3.3V	0.1A (S3)

SATA	
3.3V	0.3A (S0, S1)

Security Classification		Compal Secret Data		Title		
Issued Date	2005/10/10	Deciphered Date	2006/10/10	POWER DELIVERY CHART		
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				Custort	KAW60 LA-4661P	2.0
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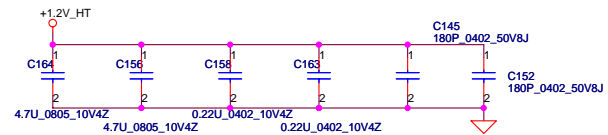
PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

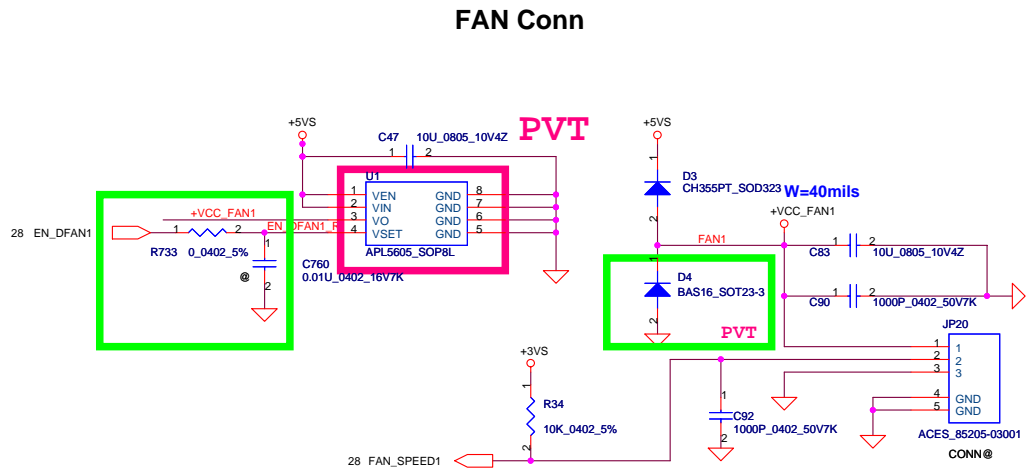


Trace length limit (Don't care)

CONN@
SOC127MM48X51-948! 6090022000; JCPU1
TEMP SYMBOL

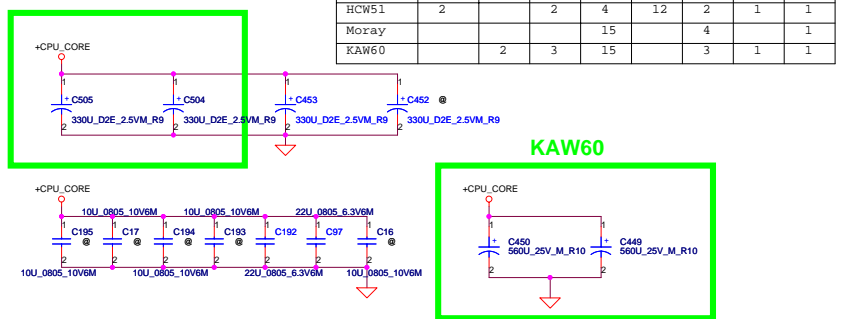
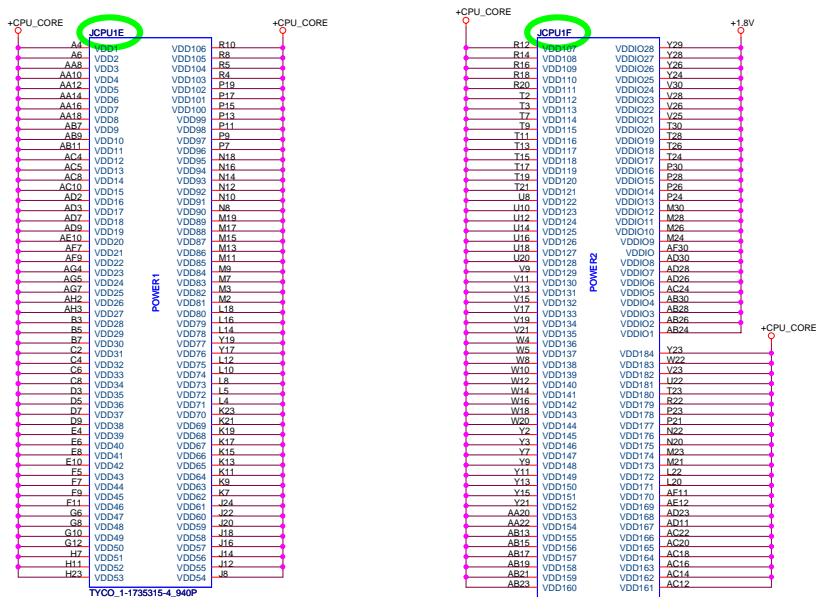


LAYOUT: Place bypass cap on topside of board
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDTO POWER PINS

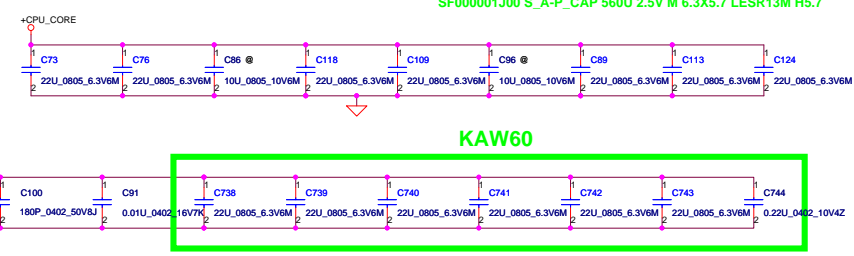


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Issued Date	2005/10/11	Deciphered Date	2006/10/11	AMD CPU HT I/F		
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	CPU_CORE	820u	560u	330u	22u	10u	.22u	.01u	180p
HWC51	2				4	12	2	1	1
Moray				15		4			1
KAW60		2	3	15		3	1	1	

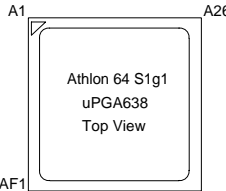
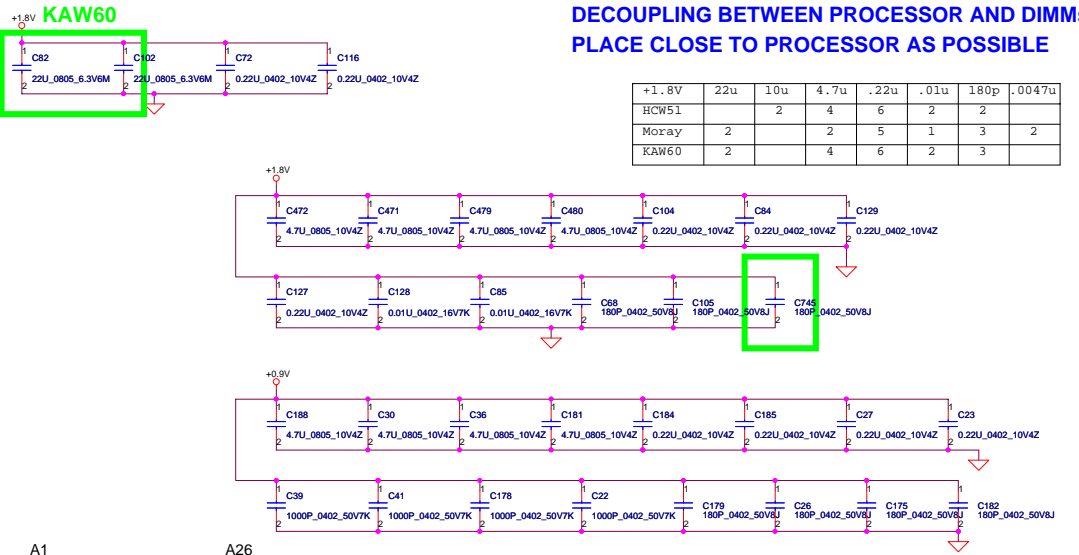


CPU SOCKET AM2 DECOUPLING



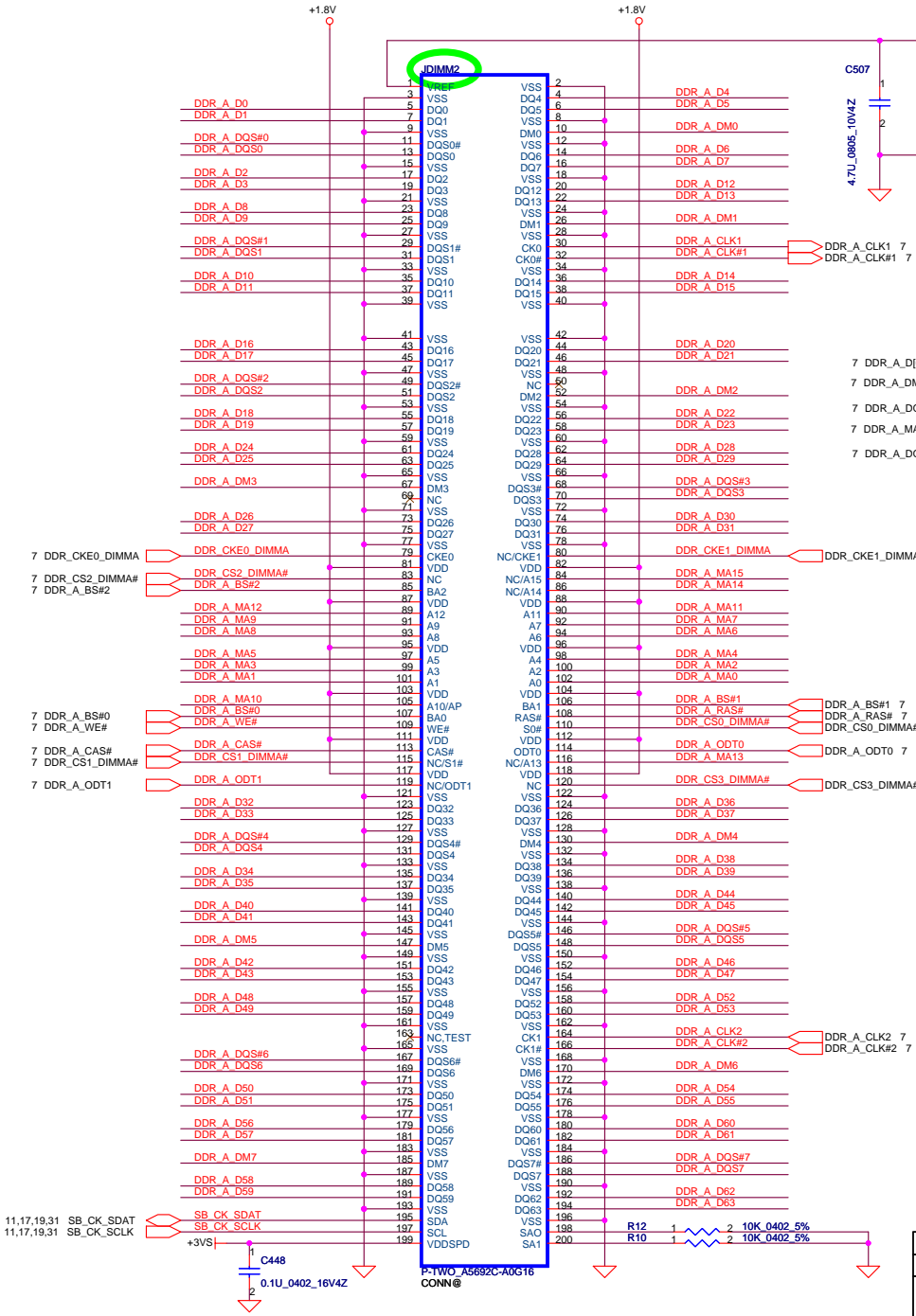
DECOUPLING BETWEEN PROCESSOR AND DIMMS PLACE CLOSE TO PROCESSOR AS POSSIBLE

	+1.8V	22u	10u	4.7u	.22u	.01u	180p	.0047u
HWC51			2	4	6	2	2	
Moray	2		2	5	1	3	2	
KAW60	2		4	6	2	3		

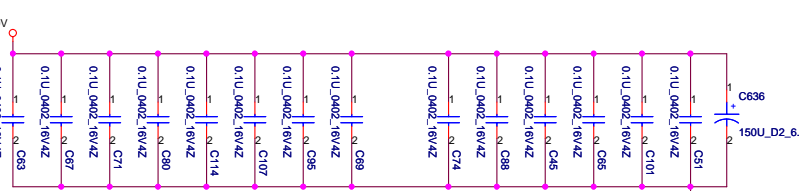
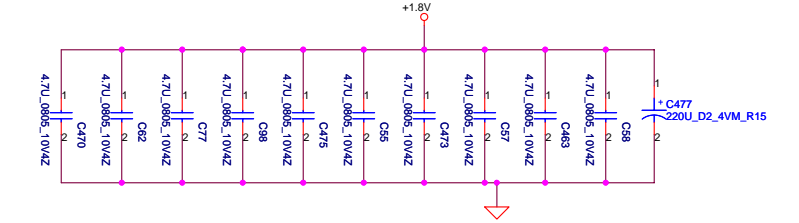
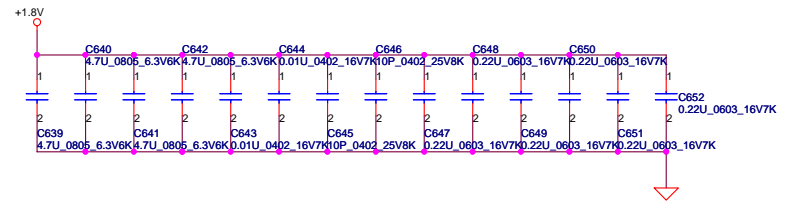


PROCESSOR POWER AND GROUND

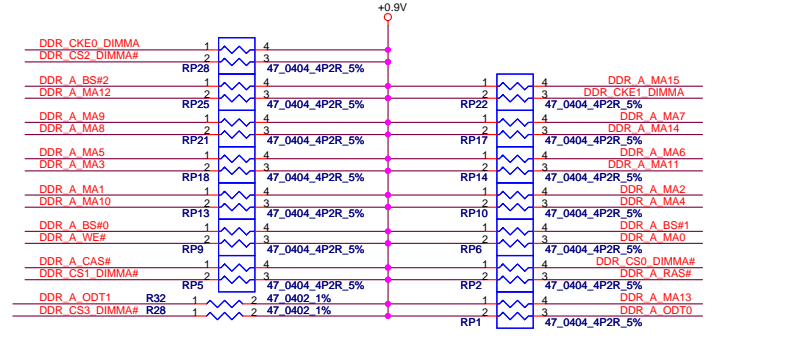
	+0.9V	4.7u	.22u	.0047u	1000p	180p
HWC51	4	4			4	4
Moray	2	4	4	4	4	4
KAW60	4	4			4	4



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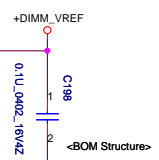
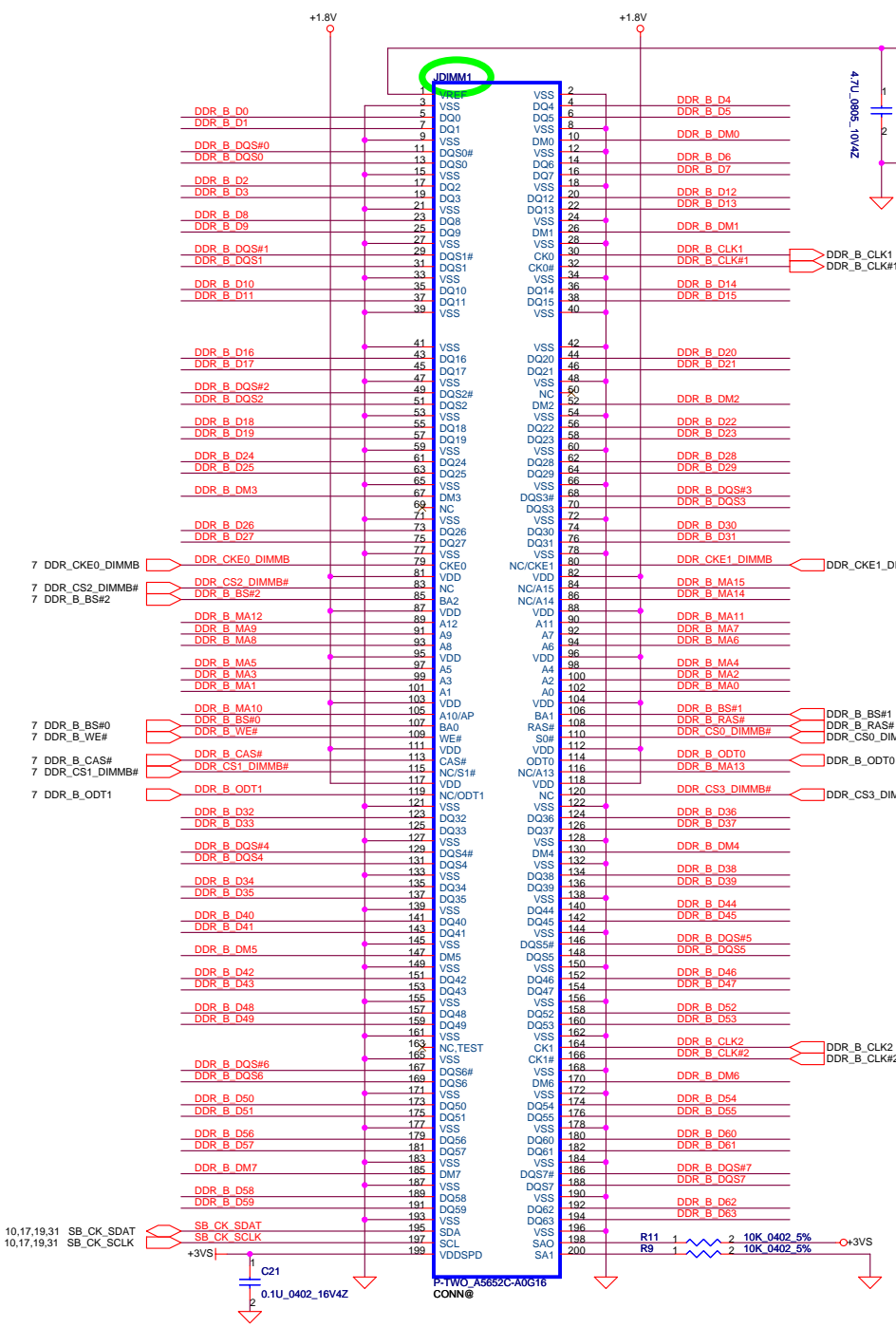


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

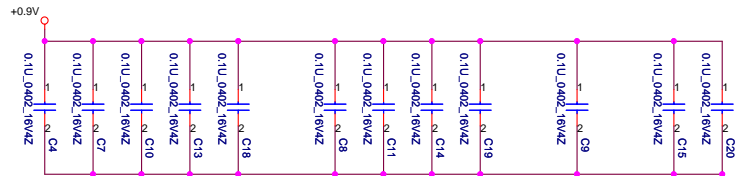
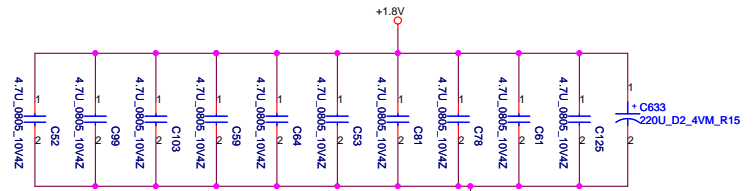


Layout Note:
Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V

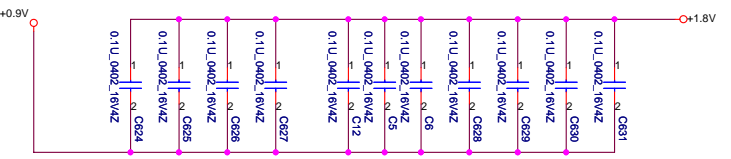
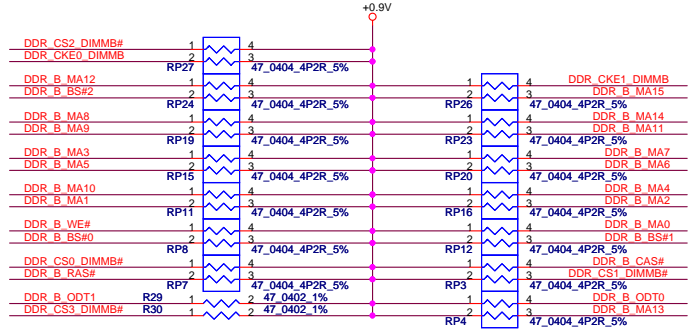
Title		
DDR2 SO-DIMM I		
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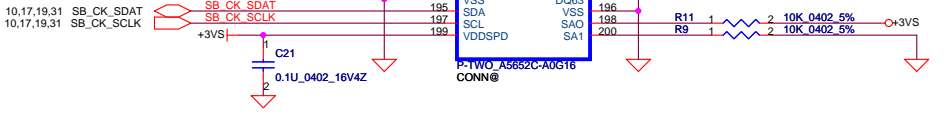
- 7 DDR_B_D0[.63] DDR B D0(.63)
- 7 DDR_B_DM[0..7] DDR B DM(0..7)
- 7 DDR_B_DQS[0..7] DDR B DQS(0..7)
- 7 DDR_B_MA[0..15] DDR B MA(0..15)
- 7 DDR_B_DQS#[0..7] DDR B DQS#[0..7]



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



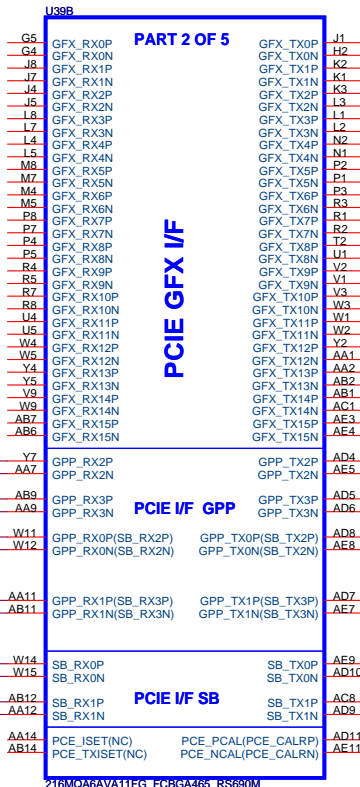
Layout Note:
Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V



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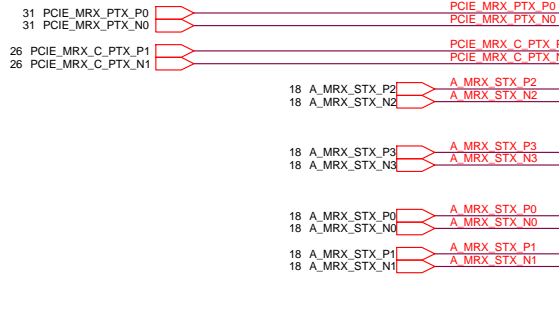


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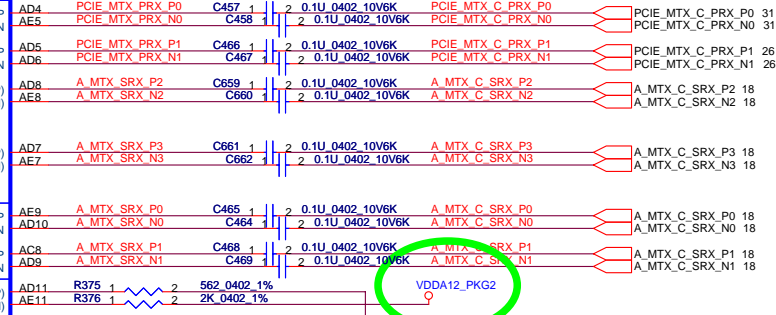
WLAN

LAN



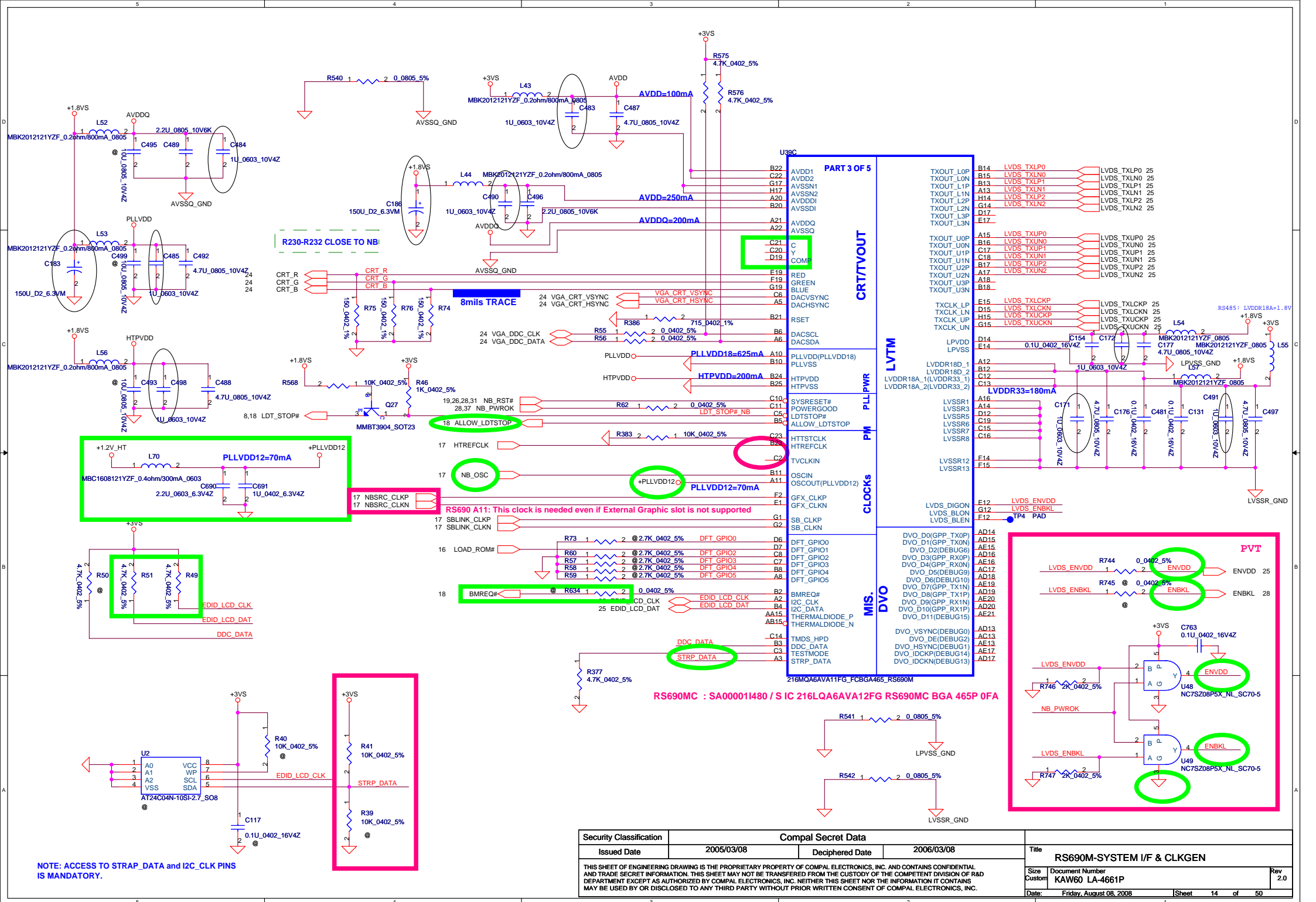
WLAN

LAN



RS690MC : SA00001I480 / S IC 216LQA6A12FG RS690MC BGA 465P OFA

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NOTE: ACCESS TO STRAP_DATA and I2C_CLK PINS IS MANDATORY.

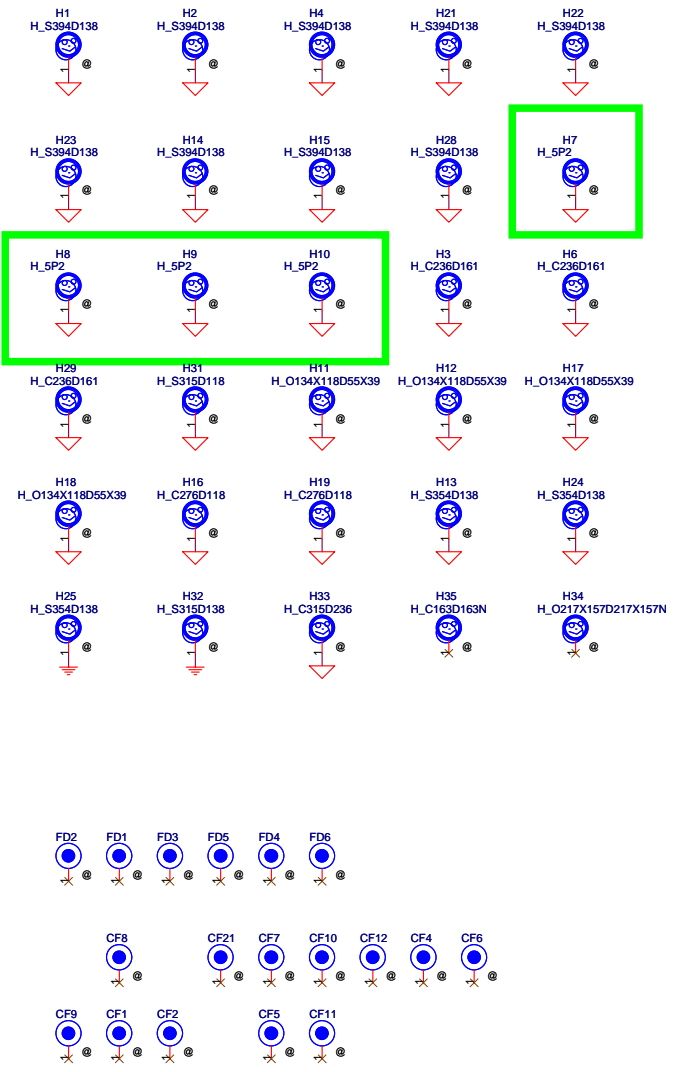
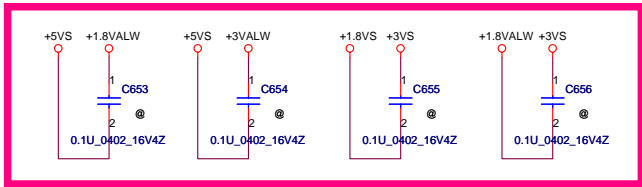
RS690MC : SA000011480 / I C 216LQA6VA12FG RS690MC BGA 465P 0FA

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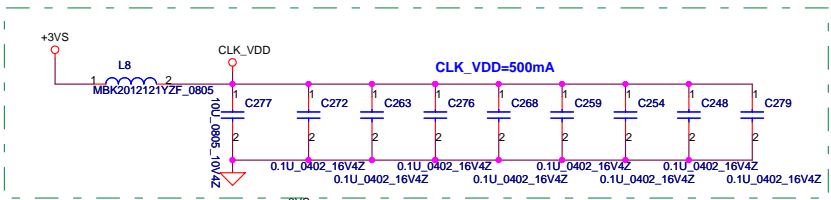


LOAD_ROM#: LOAD ROM STRAP ENABLE

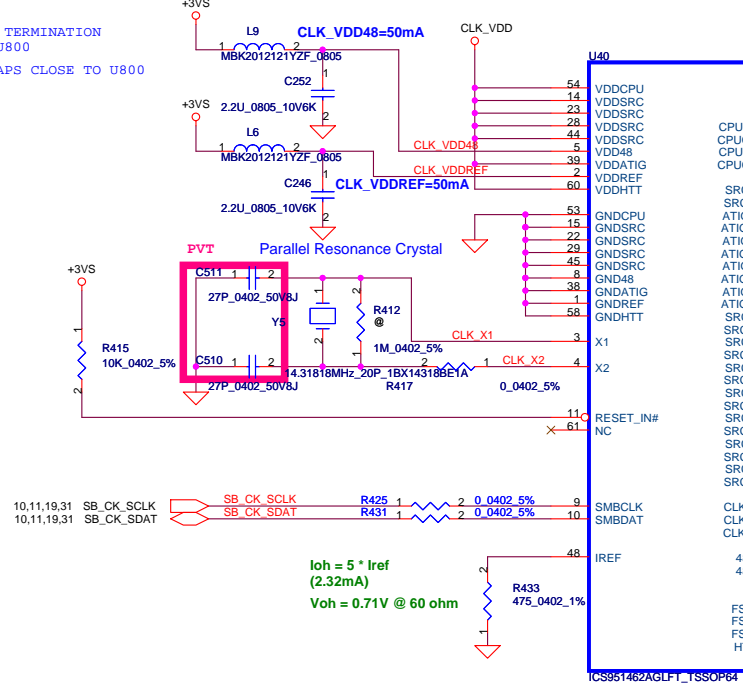
High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE



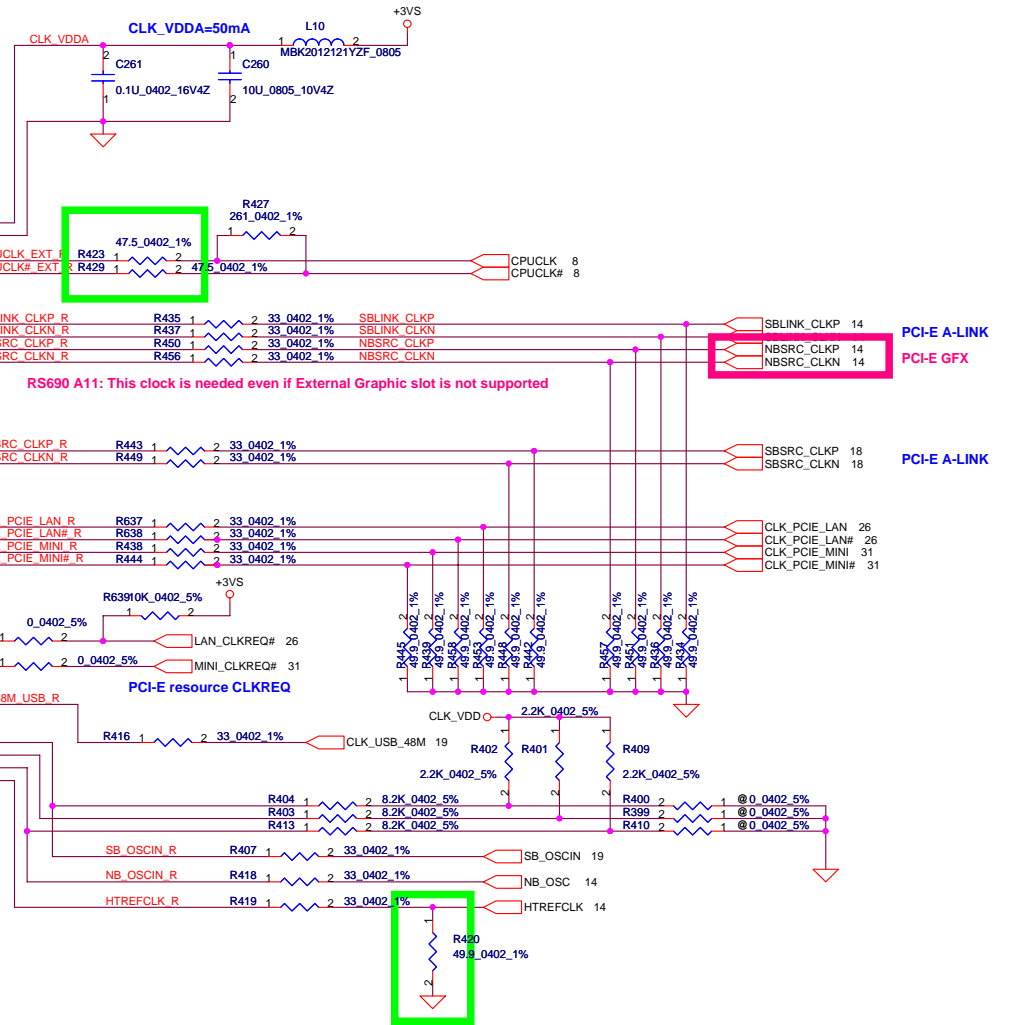
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/08	Deciphered Date	2006/03/08	RS690MC-STRAPS & SCREW	
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- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

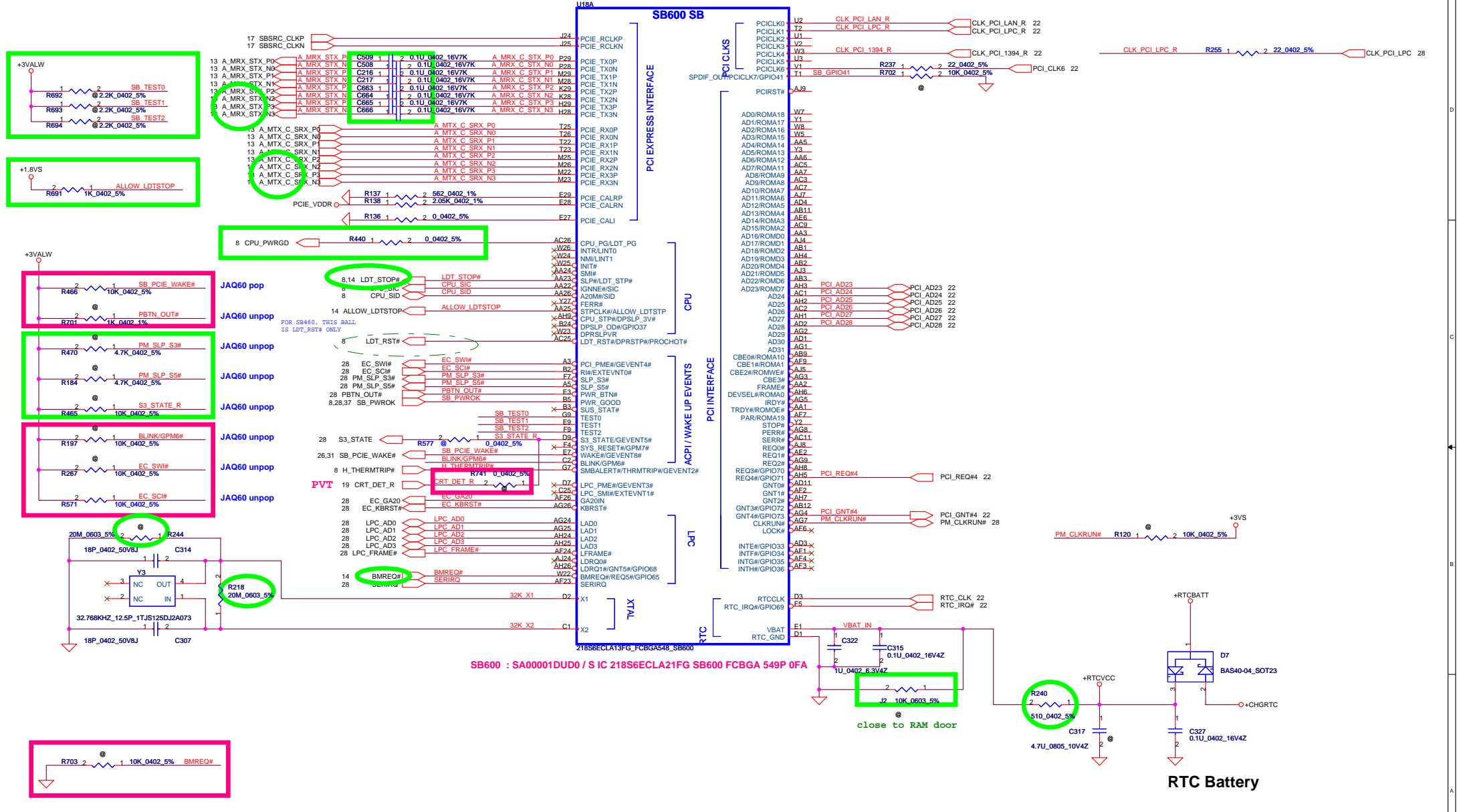


$I_{oh} = 5 * I_{ref}$
 (2.32mA)
 $V_{oh} = 0.71V @ 60 \text{ ohm}$



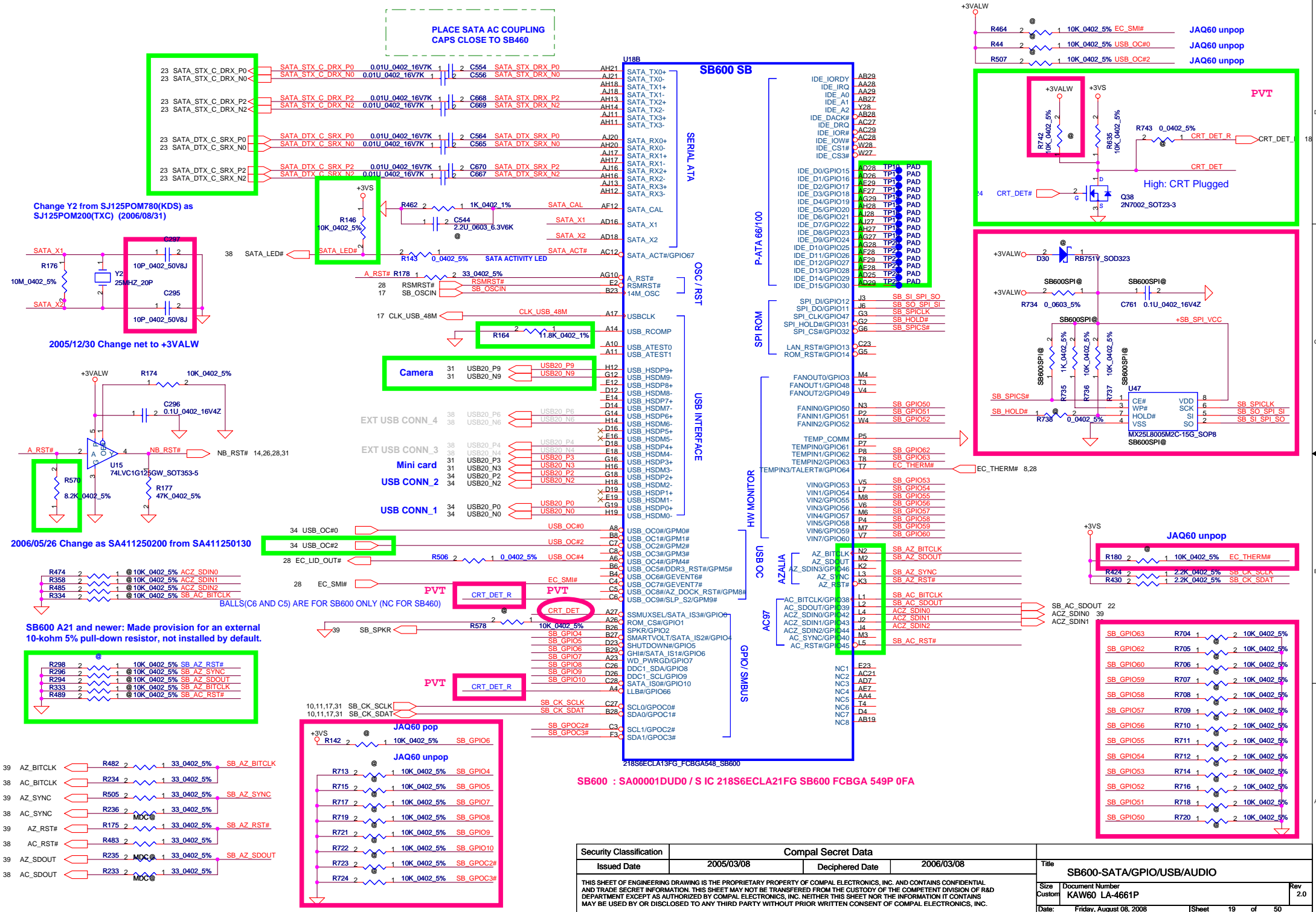
EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation



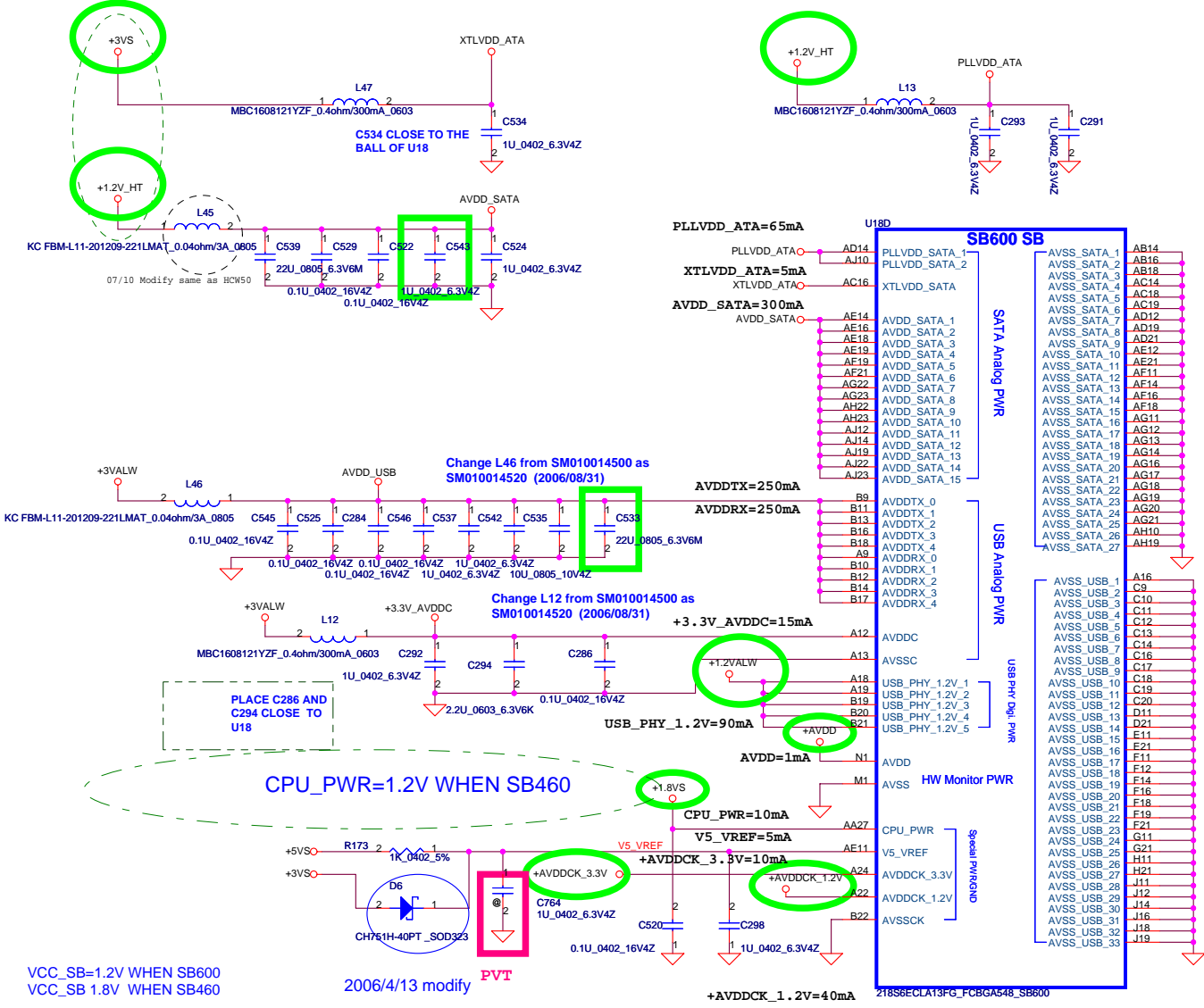
SB600 : SA00001DUD0 / S IC 21856ECLA21FG SB600 FCBGA 549P 0FA

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SB600-SATA/GPIO/USB/AUDIO			Rev 2.0
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SB600 : SA00001DUD0 / S IC 218S6ECLA21FG SB600 FCBGA 549P 0FA



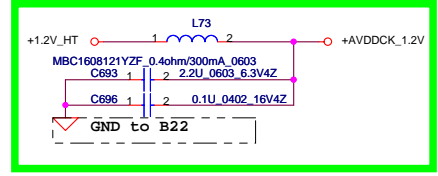
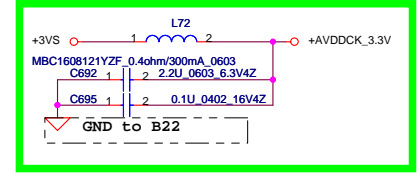
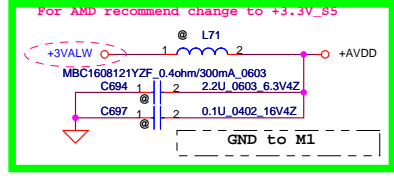
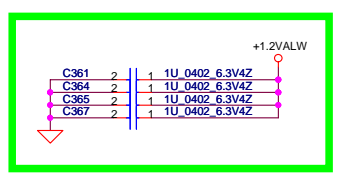
VCC_SB=1.2V WHEN SB600
VCC_SB 1.8V WHEN SB460

CPU_PWR=1.2V WHEN SB460

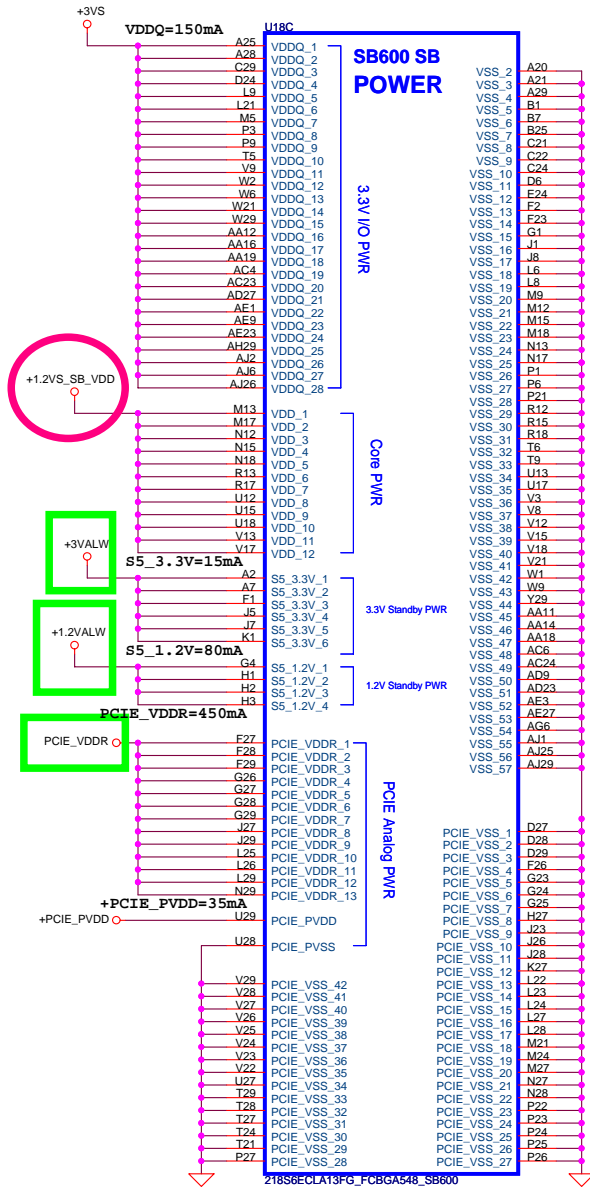
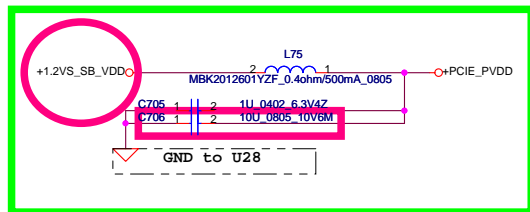
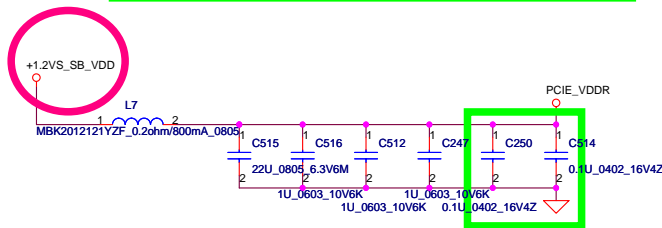
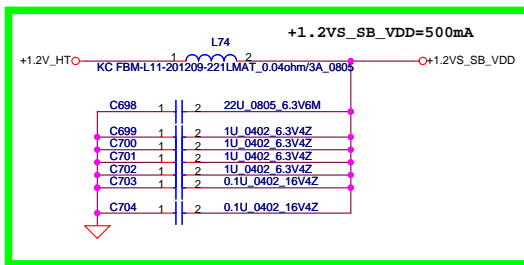
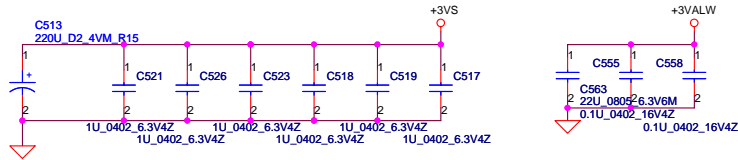
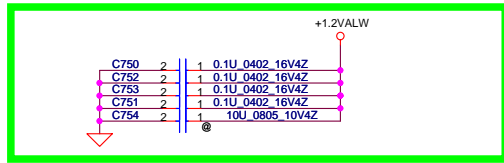
SB600 : SA00001DUD0 / S IC 218S6ECLA21FG SB600 FCBGA 549P 0FA

PLACE SATA_CAL RES & CAP VERY CLOSE TO BALL OF U18

NOTE:
R462 IS 1K 1% FOR 25MHZ
XTAL, 4.99K 1% FOR 100MHZ
INTERNAL CLOCK



Security Classification	Compal Secret Data			Title	SB600-PWR & GND I	
Issued Date	2005/03/08	Deciphered Date	2006/03/08	Size	Document Number	Rev
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				Date:	Thursday, July 24, 2008	Sheet

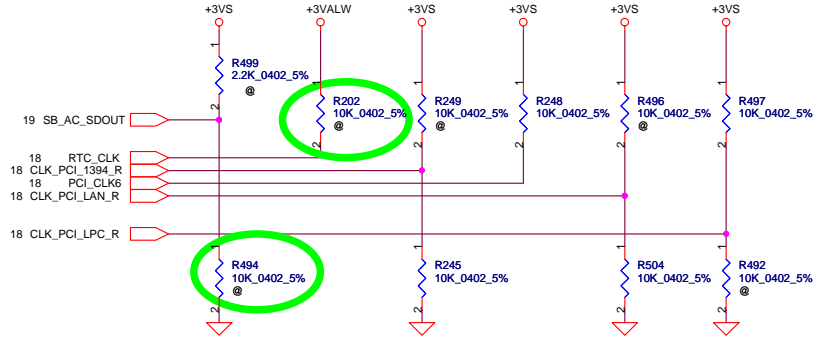


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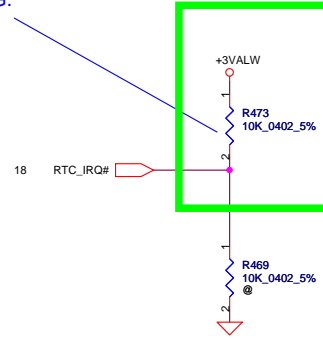
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Issued Date	2005/03/08	Deciphered Date	2006/03/08	SB600-PWR & GND II	
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Size	Document Number	Rev			
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Date:	Thursday, July 24, 2008	Sheet	21	of	50

REQUIRED STRAPS

SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT, 15K PU FOR RTC_CLK, EXTERNAL PU/PD IS NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE REQUIRED



NOTE: R473 PU RESISTOR FOR RTC_IRQ# IS REQUIRED FOR SB600 TO KEEP THE INPUT FROM FLOATING.



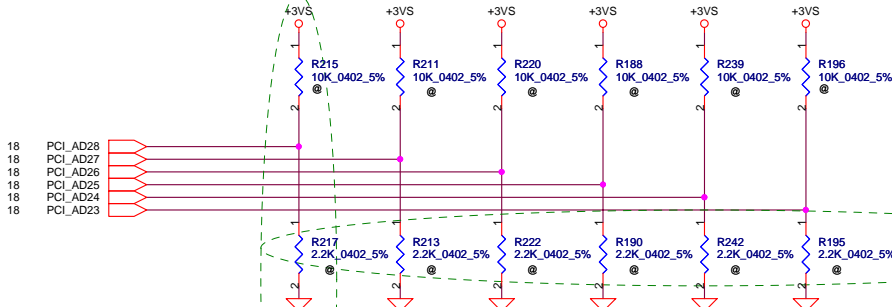
SB460 ONLY

	ACPWON	SPDIF_OUT	PCI_MINI_R	PCI_PCM_R	PCI_SIO_R	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

		SB600				SB460	
		AC_SDOUT	RTC_CLK	PCI_1394_R	PCI_CLK6	PCI_LAN_R	PCI_LPC_R
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM L, H = LPC II ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]		

DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

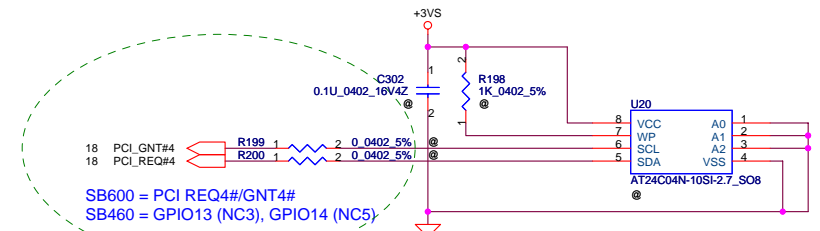
SB600 ONLY

NOTE: FOR SB460, PCI_AD23 IS RESERVED

SB460 ONLY

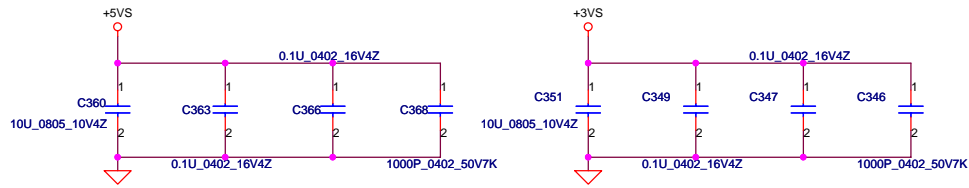
SB600 ONLY

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

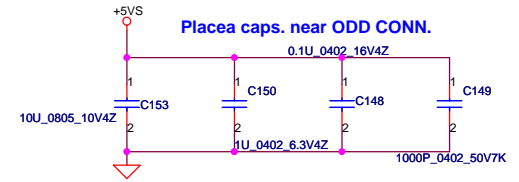


SB PCIE EEPROM STRAPS

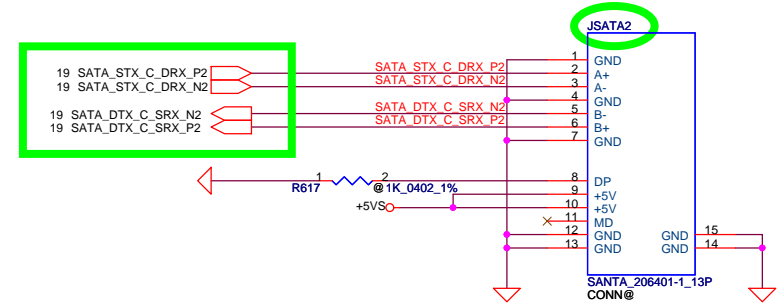
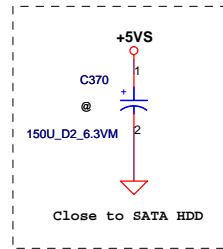
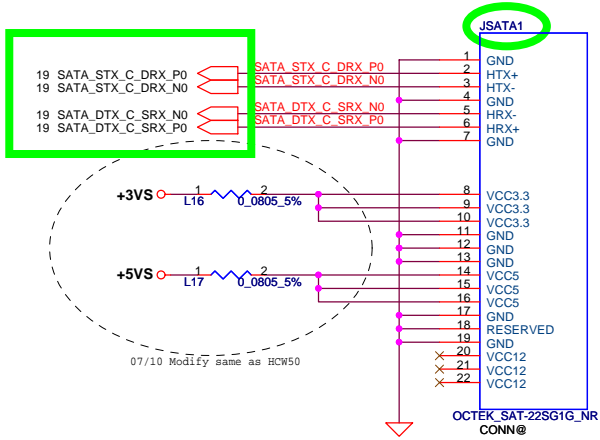
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/08	Deciphered Date	2006/03/08	SB600-STRAPS	
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Date: Friday, August 08, 2008				Sheet 22	of 50



SATA HDD CONN

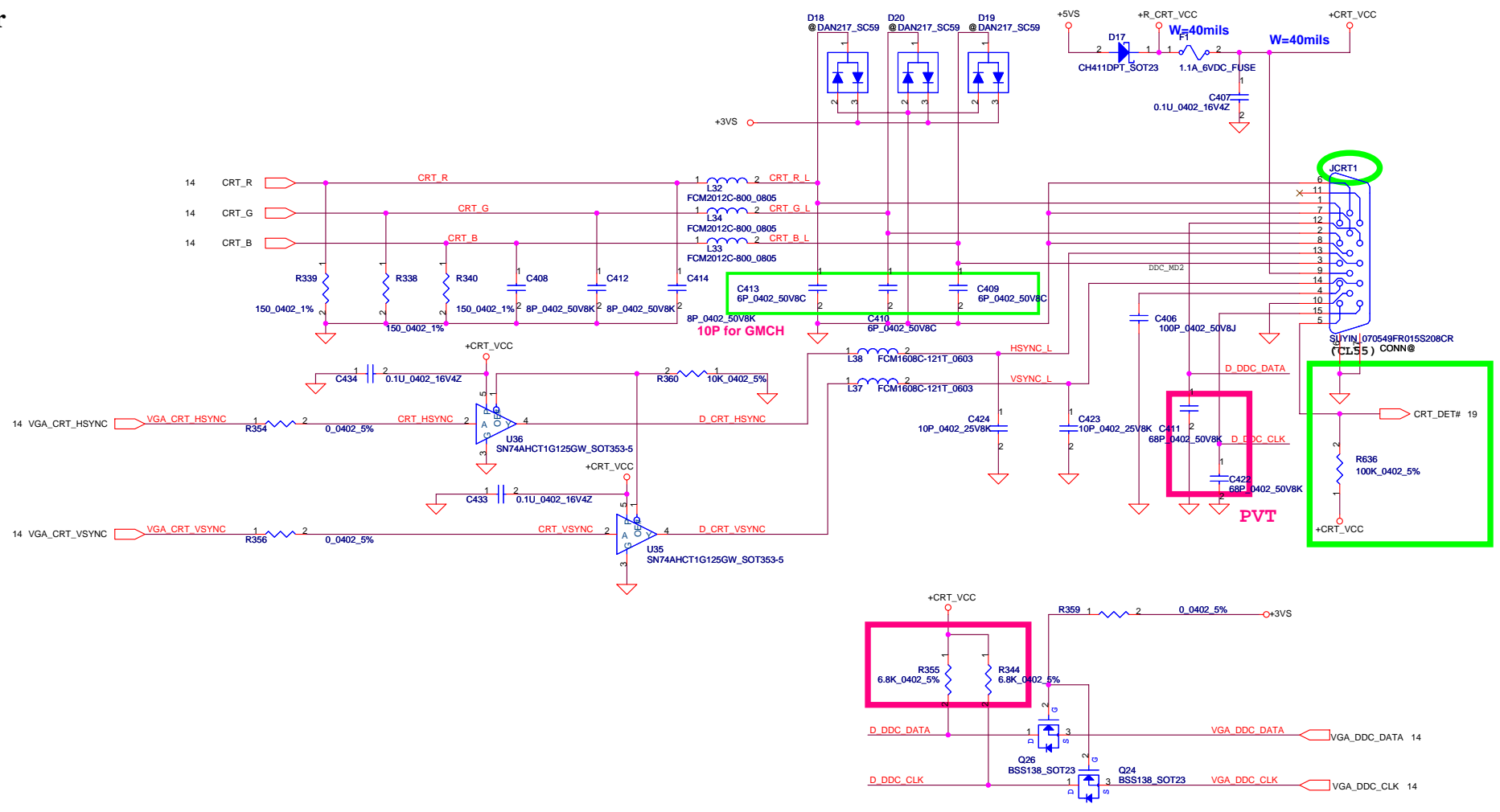


SATA ODD CONN



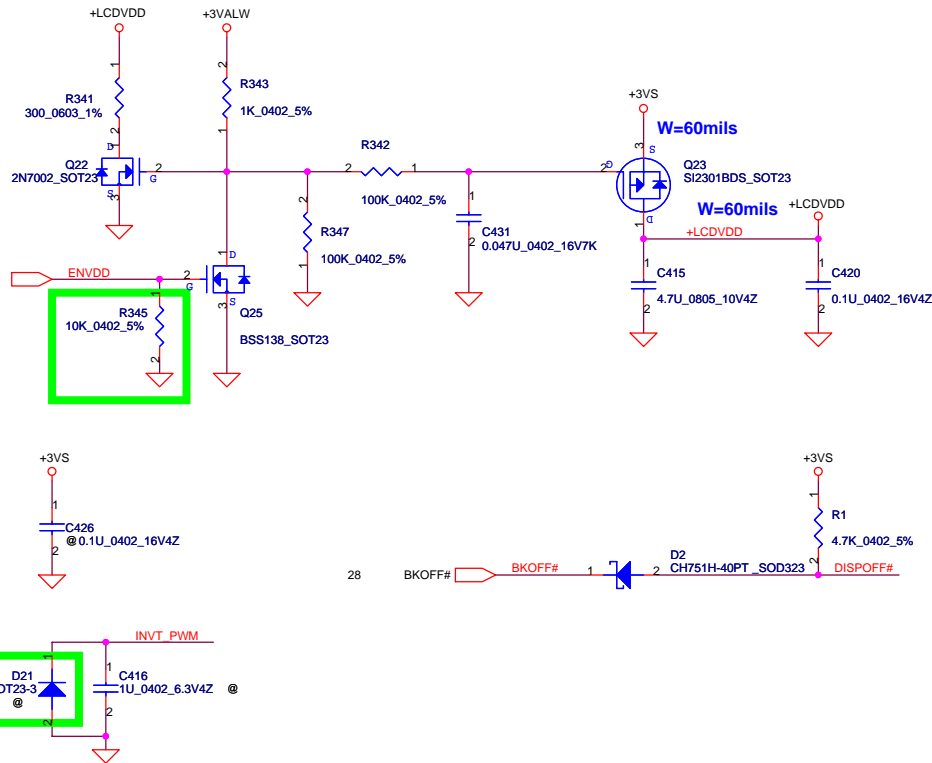
Security Classification	Compal Secret Data			Title	
Issued Date	2005/03/08	Deciphered Date	2006/03/08	HDD/CDROM	
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CRT Connector

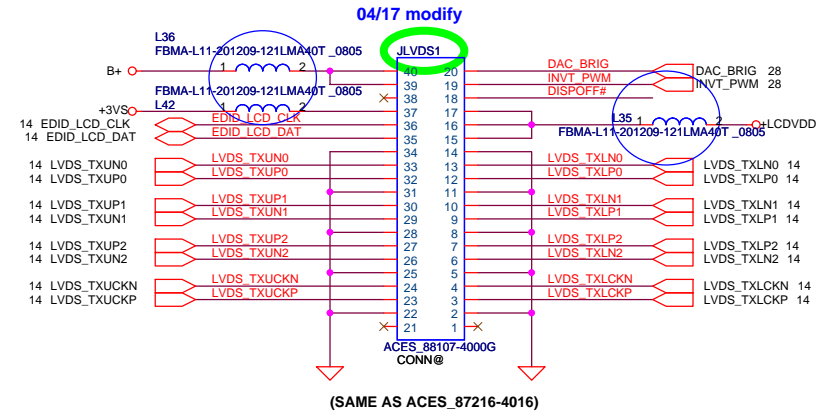


Security Classification	Compal Secret Data			Title	CRT Conn.
Issued Date	2005/03/08	Deciphered Date	2006/03/08	Size Custom	Document Number KAW60 LA-4661P
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				Sheet	24 of 50
				Rev	2.0

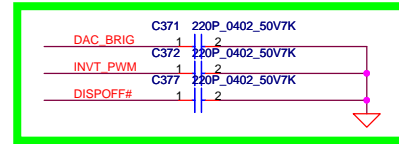
LCD POWER CIRCUIT



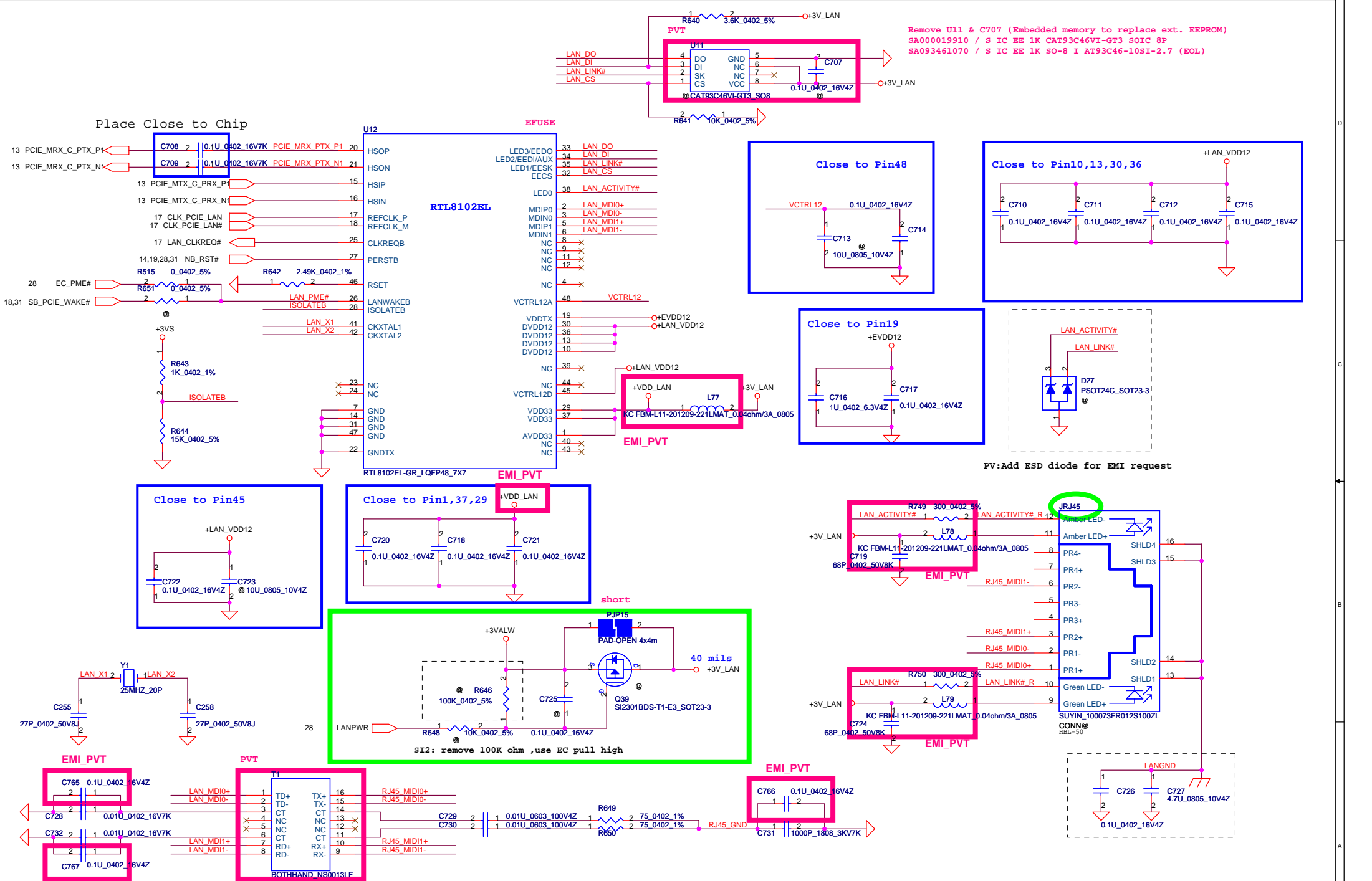
LCD/PANEL CONN.



EMI



Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/08	Deciphered Date	2006/03/08	LCD Conn.	
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Size	Custom	Document Number	KAW60 LA-4661P		Rev
Date:	Friday, August 08, 2008	Sheet	25	of	50



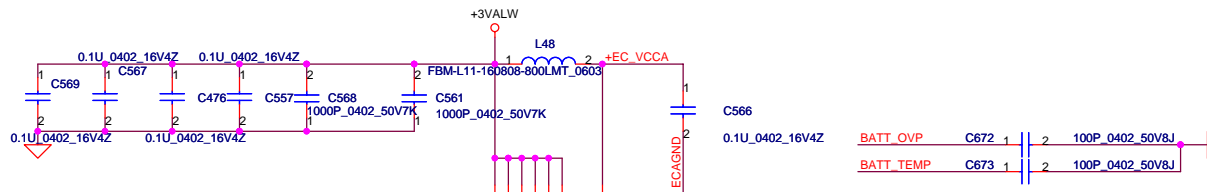
SP050003N00 S X'FORM_N8681680 LAN (MHPC , Not for ABO)
 SP050001210 S X'FORM_N80013LF LAN (BOTHHAND)
 SP050001310 S X'FORM_LF-H80P-1 COUPLING (lankom)
 SP050004L00 S X'FORM_HD-024A 10/100 PC CARD LAN (TAIMAG)

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Title LAN RTL8102EL & RJ45			
Size B	Document Number KAW60 LA-4661P	Rev 2.0	
Date Friday, August 08, 2008	Sheet 26	of 50	

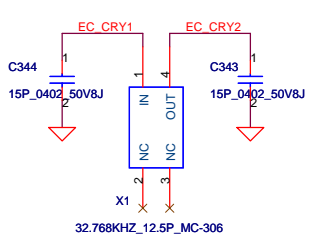
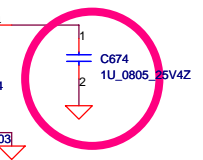
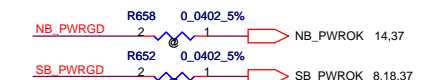
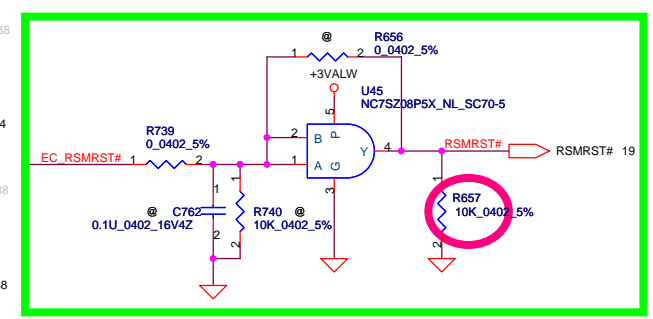
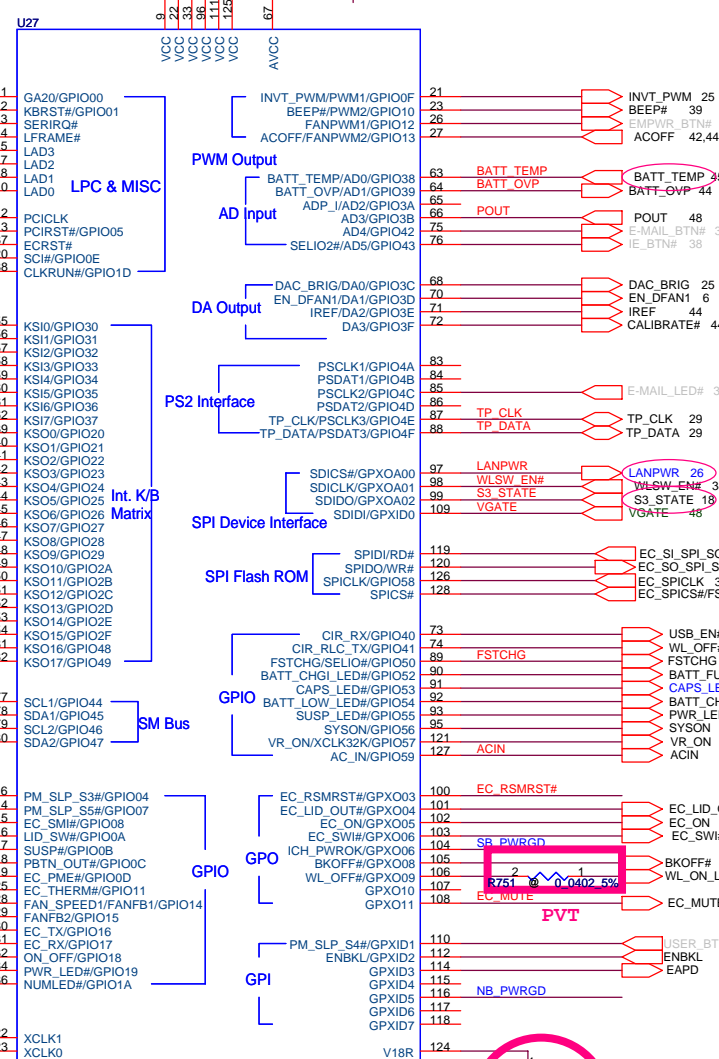
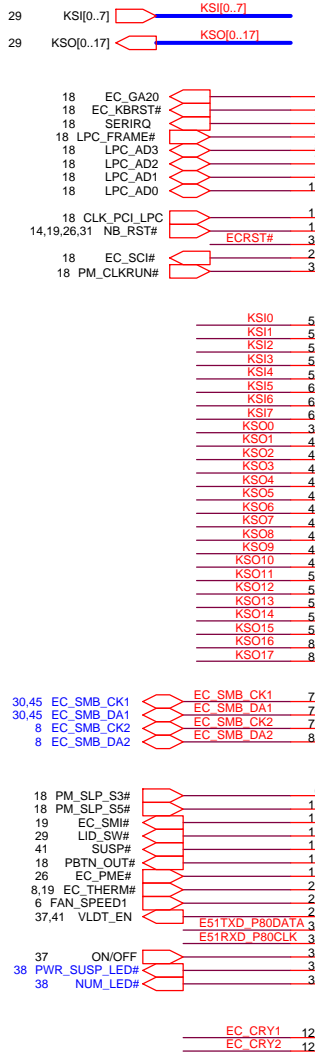
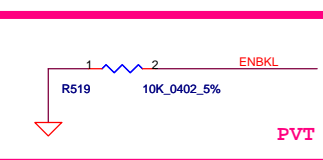
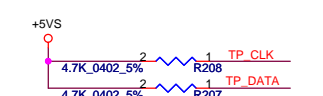
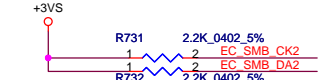
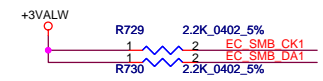
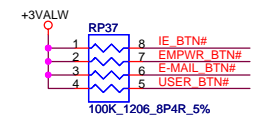
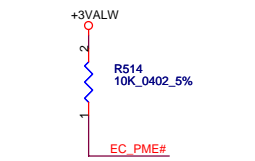
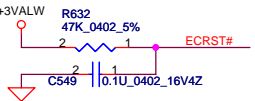
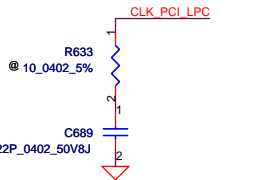
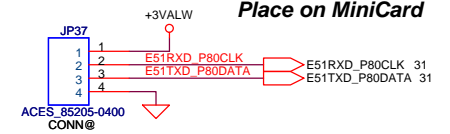


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				B	KAW60 LA-4661P	Rev	2.0
				Date	Tuesday, June 17, 2008	Sheet	27 of 50



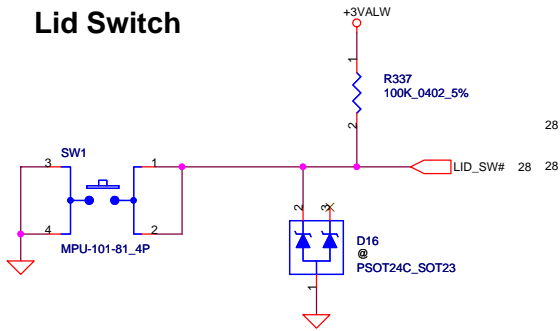
For EC Tools

Place on MiniCard

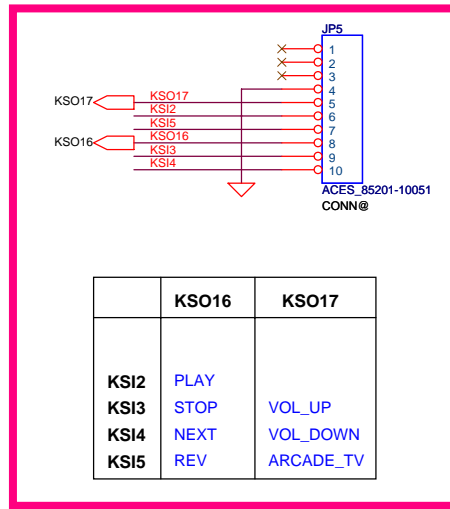


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Issued Date	2007/5/18	Deciphered Date	2008/5/18	Size	ENE-KB926
				Document Number	KAW60 LA-4661P
				Rev	0.2
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				Sheet	28 of 50

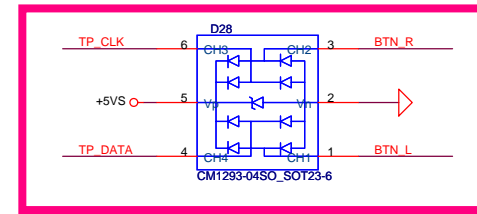
Lid Switch



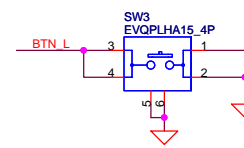
W/O media board (LS2921P)



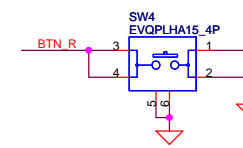
PVT



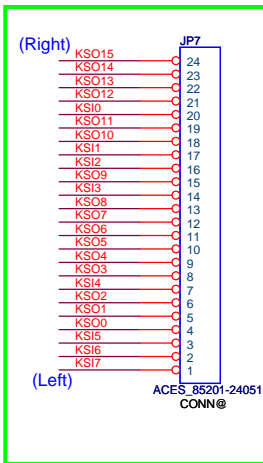
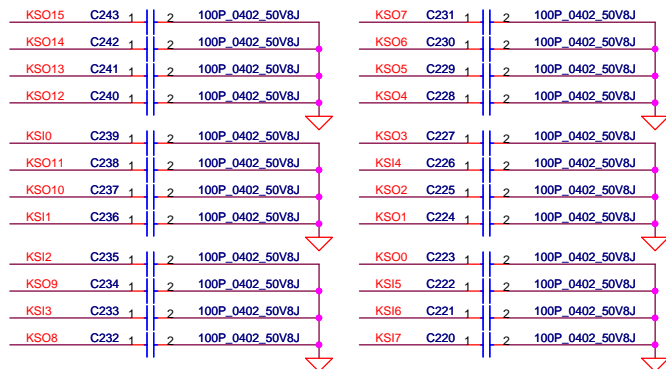
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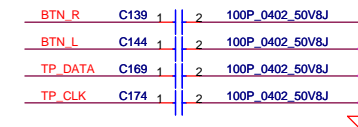
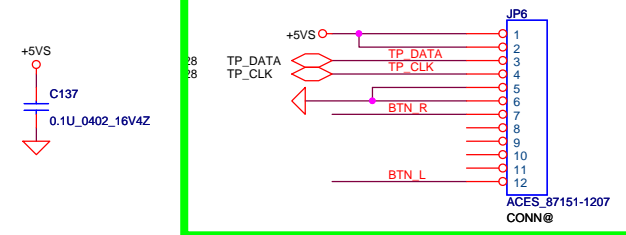
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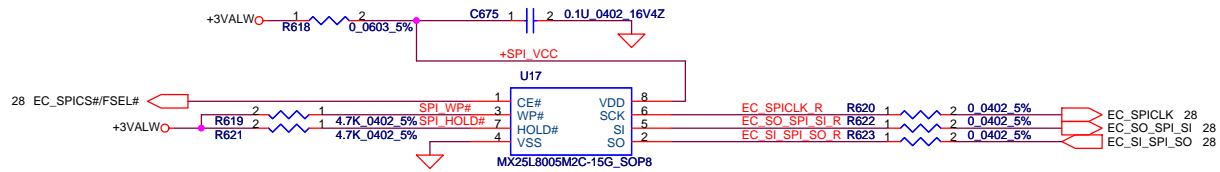
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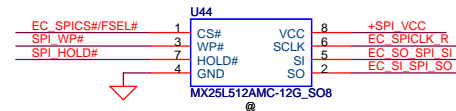
To TP/B Conn.



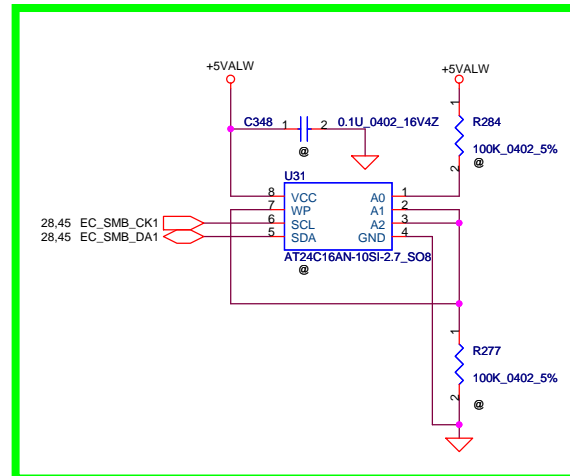
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Size Custom	29	of 50	Rev 2.0



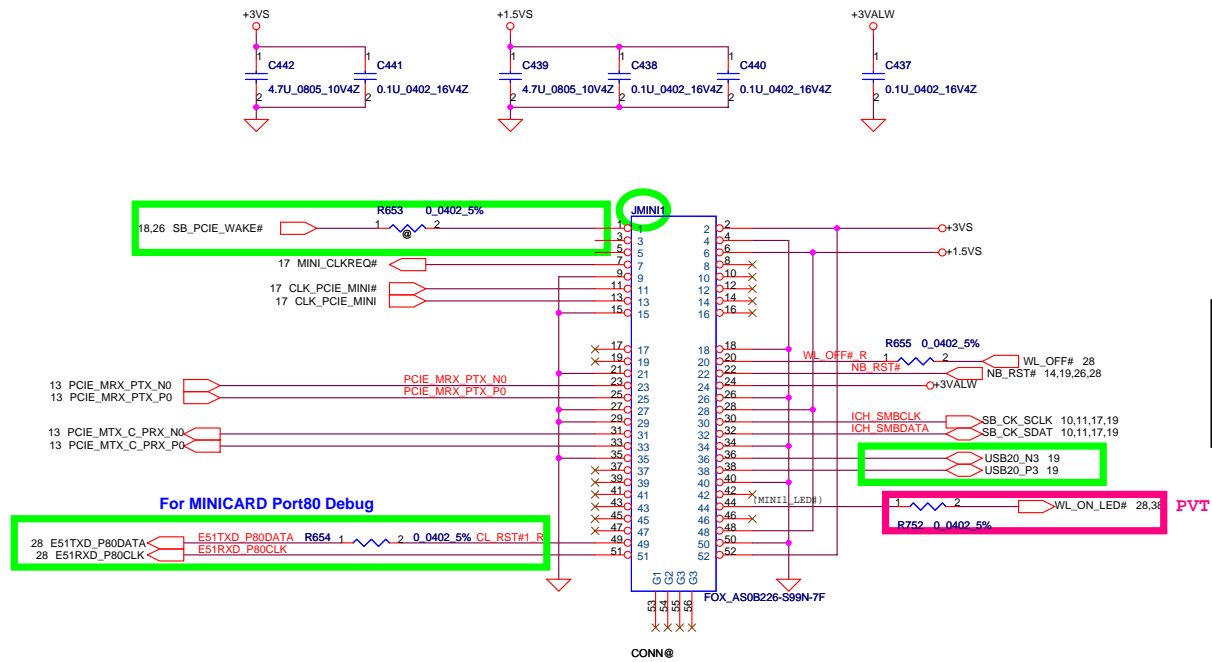
SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P
 ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz



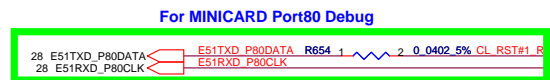
Reserved for BIOS simulator.
 Footprint S08
 SPI ROM Footprint 150mil



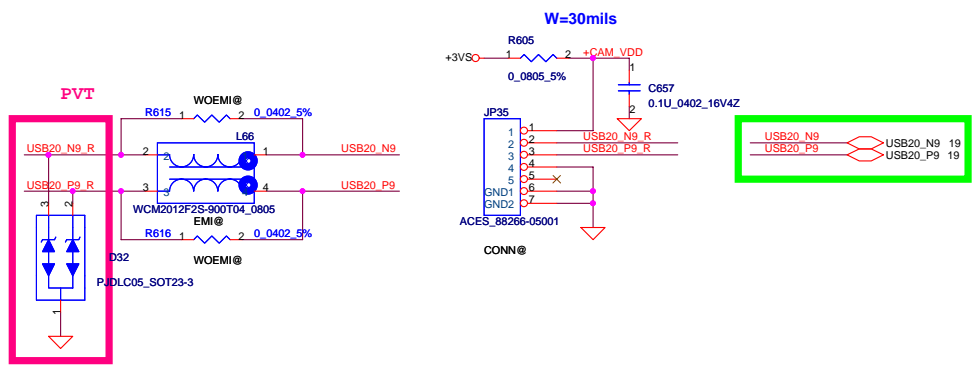
Security Classification	Compal Secret Data		Title	
Issued Date	2005/03/08	Deciphered Date	2006/03/08	BIOS
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				Document Number
				KAW60 LA-4661P
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Date: Friday, August 08, 2008		Sheet 30 of 50		



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	Normal
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



Camera



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		2006/06/20

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Compal Electronics, Inc.		
Title		
MINI Card & Camera		
Size B	Document Number	Rev
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				B	KAW60 LA-4661P
				Date:	Rev
				Tuesday, June 17, 2008	2.0
				Sheet	33 of 50

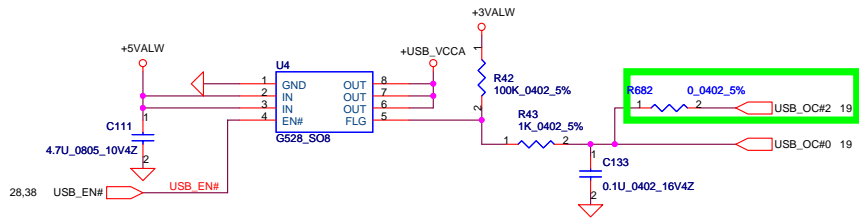
A

B

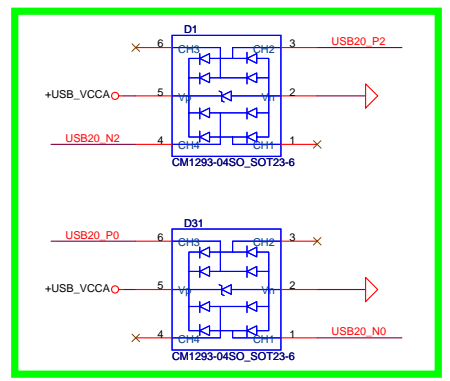
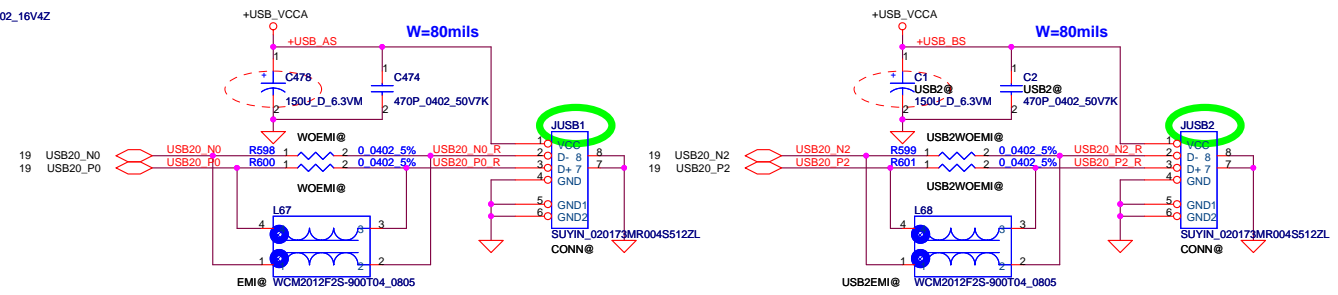
C

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USB CONN. 1 & 2



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				Date: Tuesday, June 17, 2008	Rev 2.0
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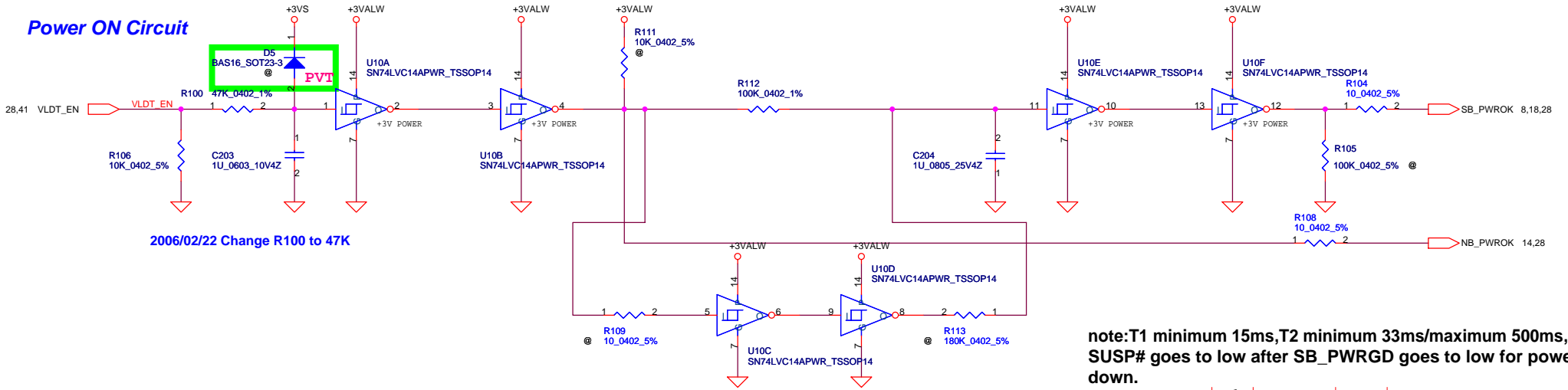
C

D

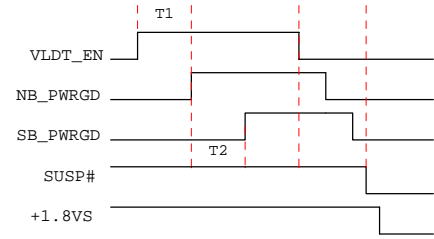
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Date: Tuesday, June 17, 2008				Sheet	36	of 50

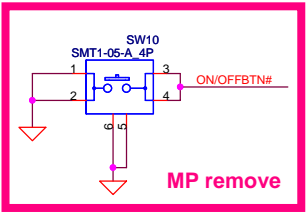
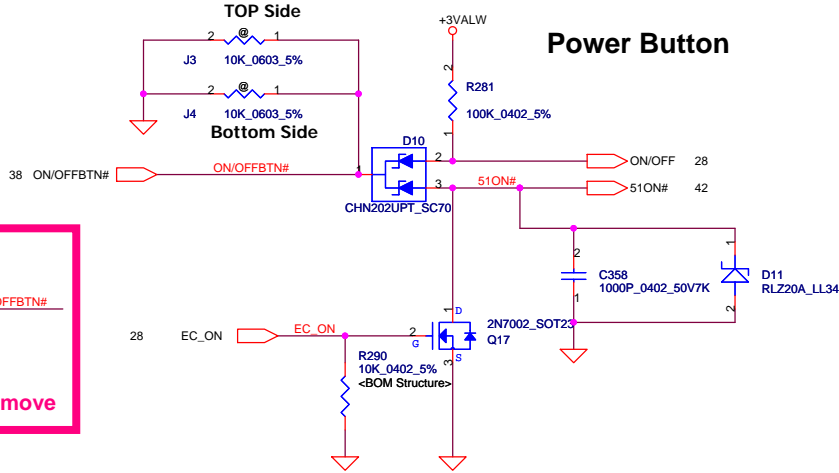
Power ON Circuit



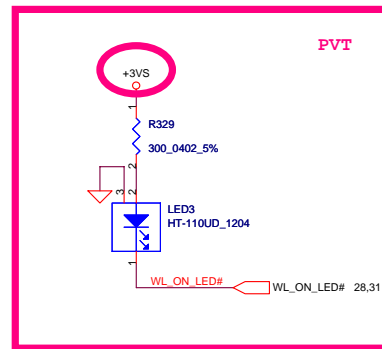
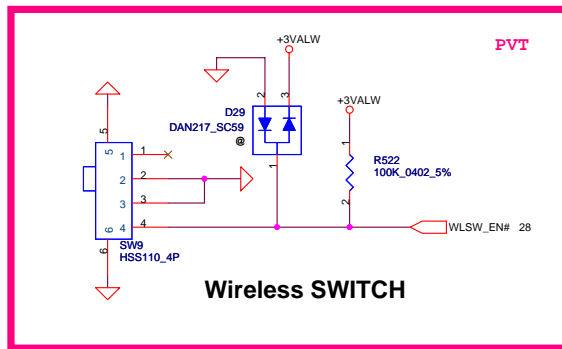
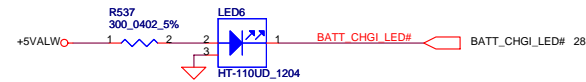
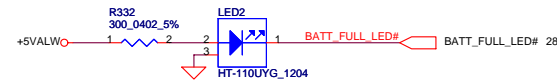
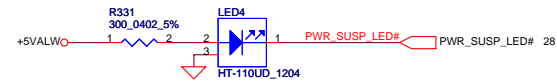
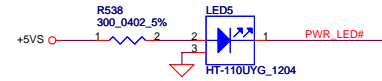
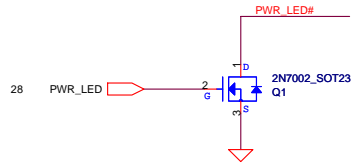
note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.



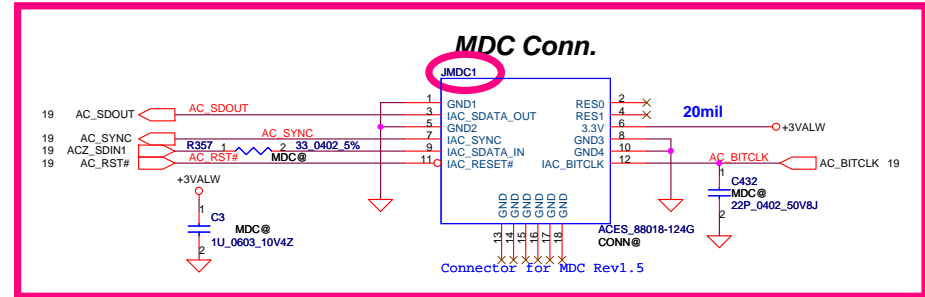
Power Button



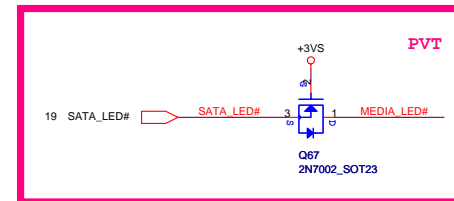
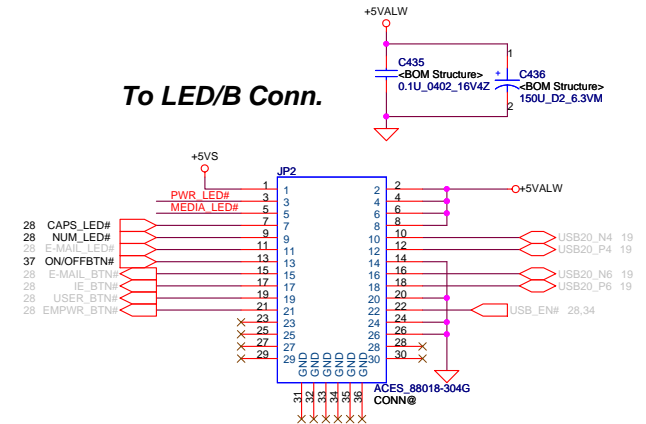
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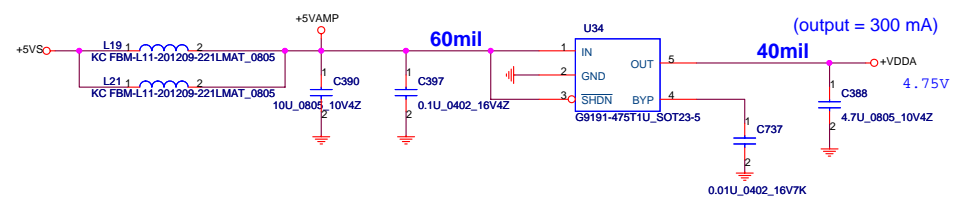
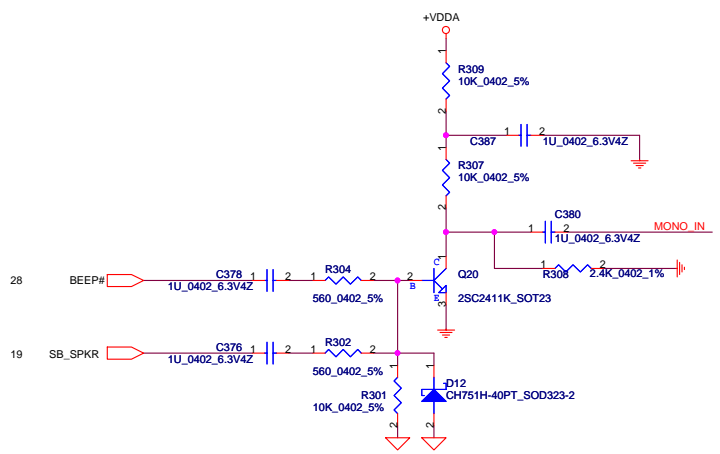
W/O Modem



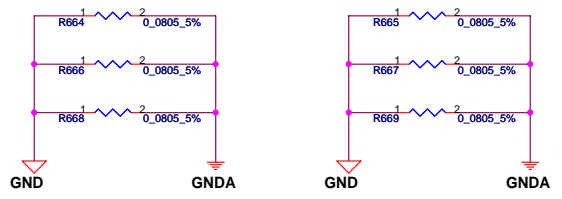
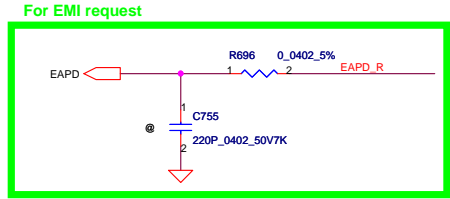
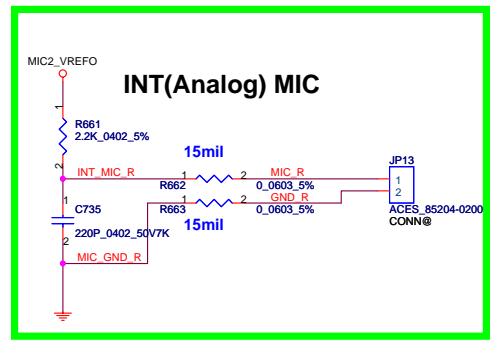
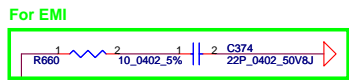
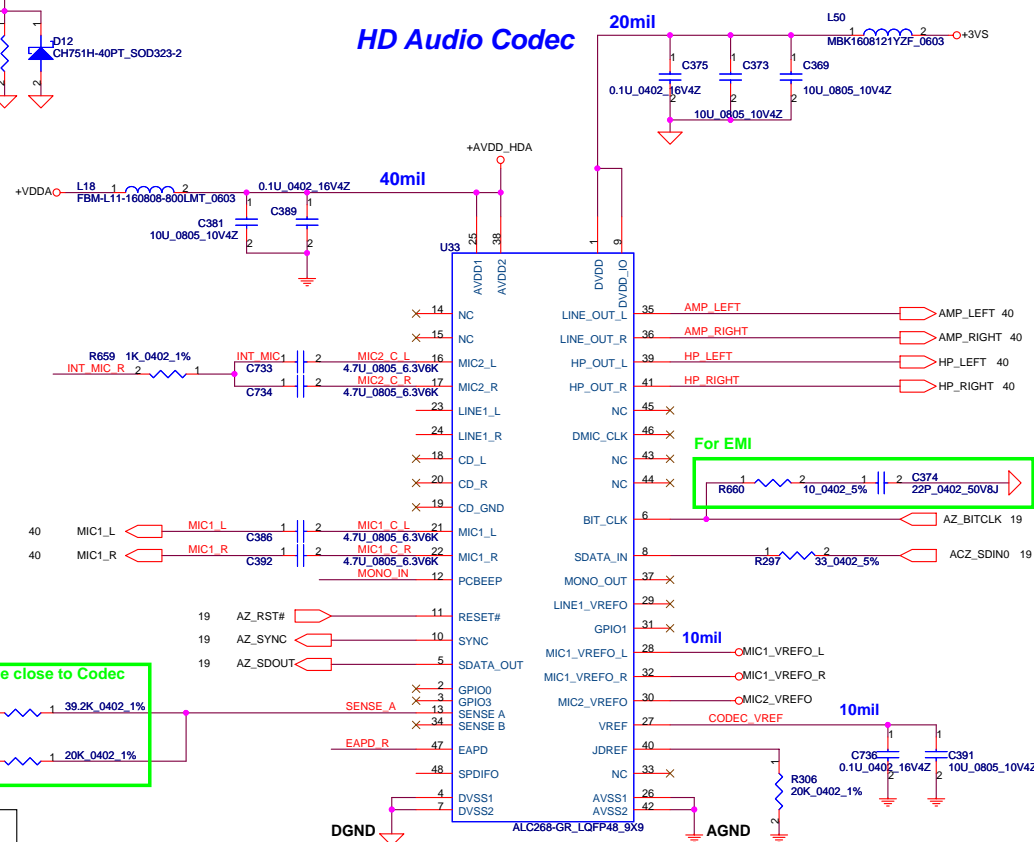
To LED/B Conn.



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				Rev 2.0 Sheet 38 of 50

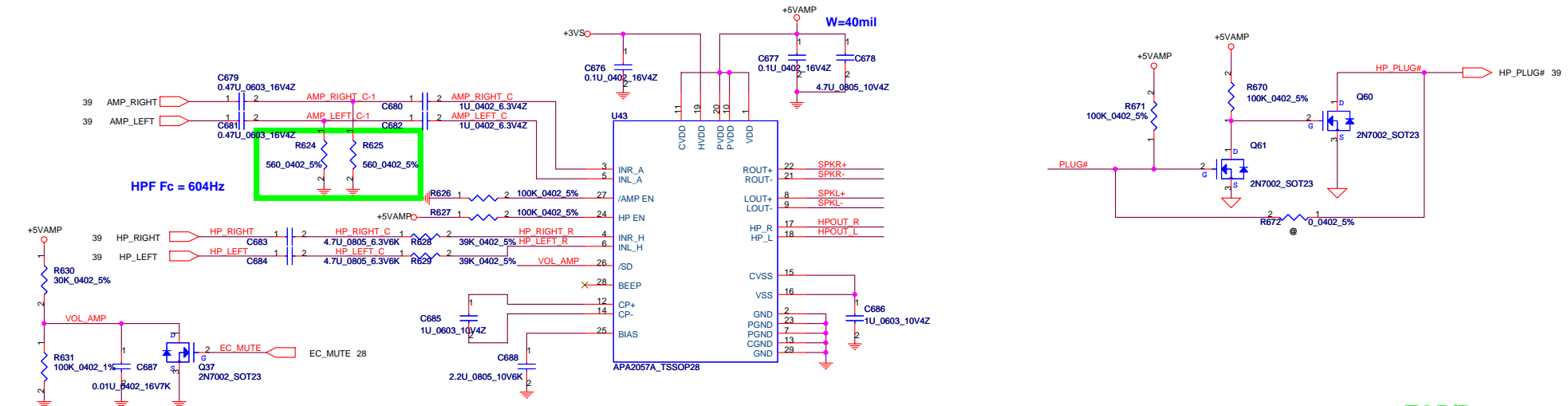


HD Audio Codec

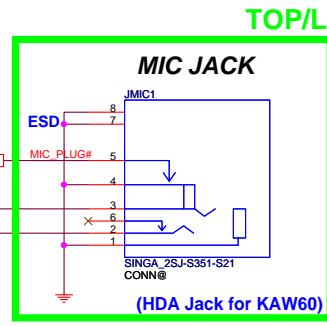
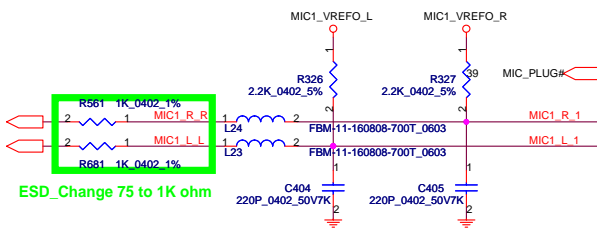
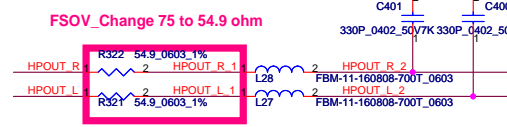
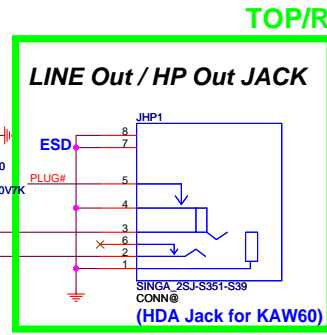
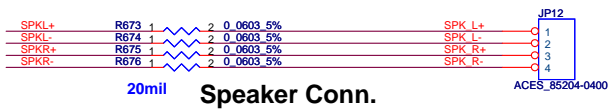


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

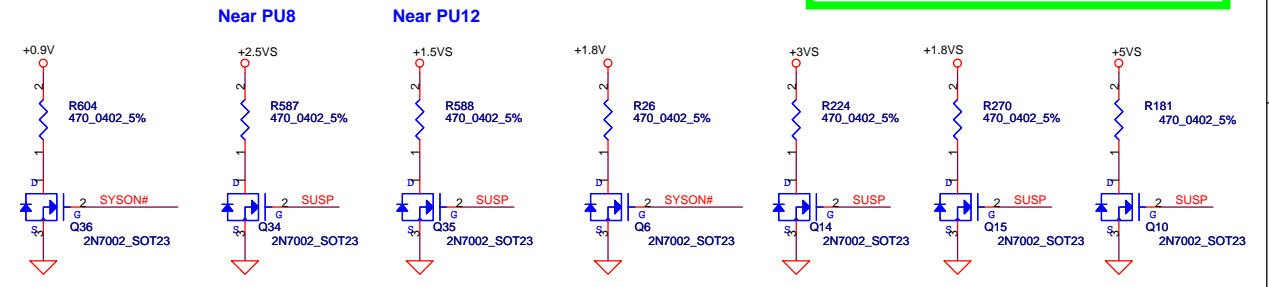
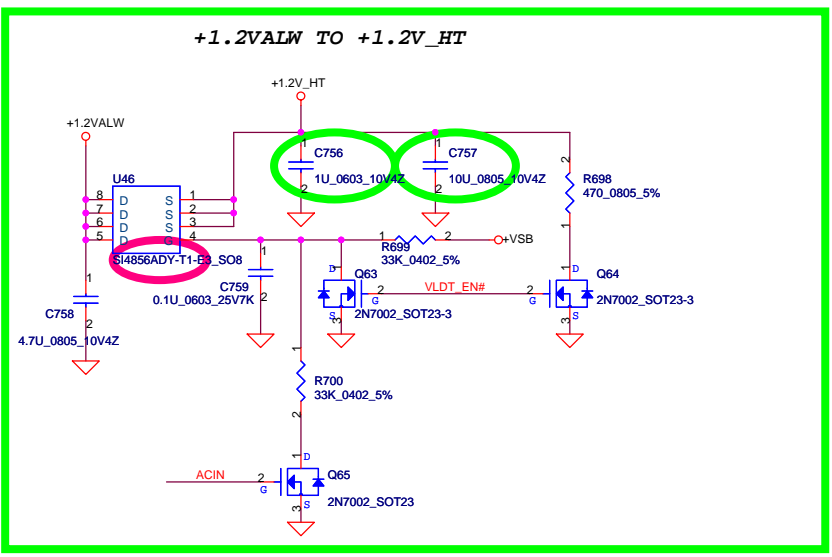
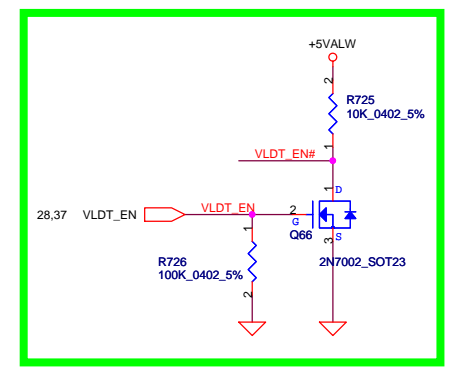
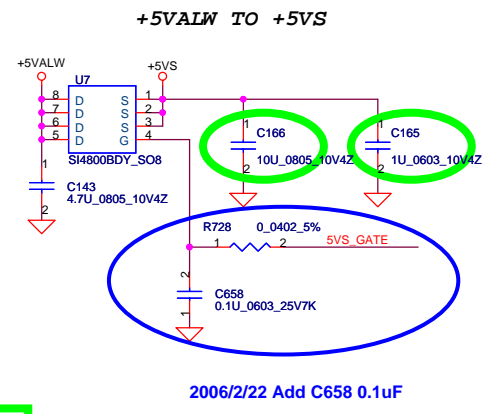
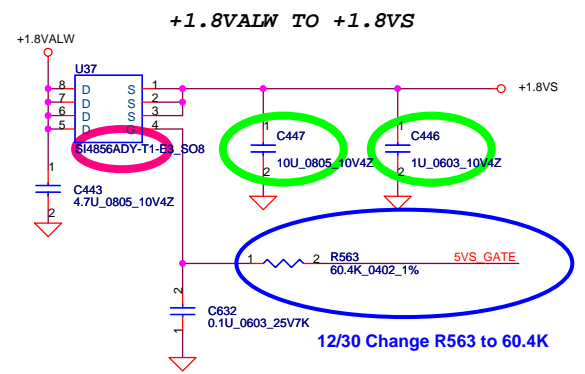
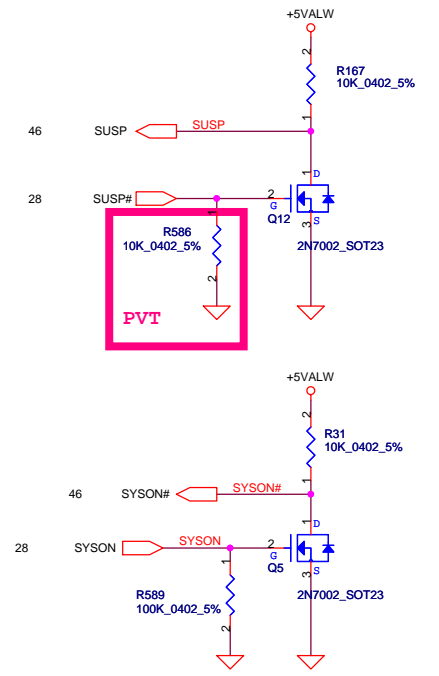
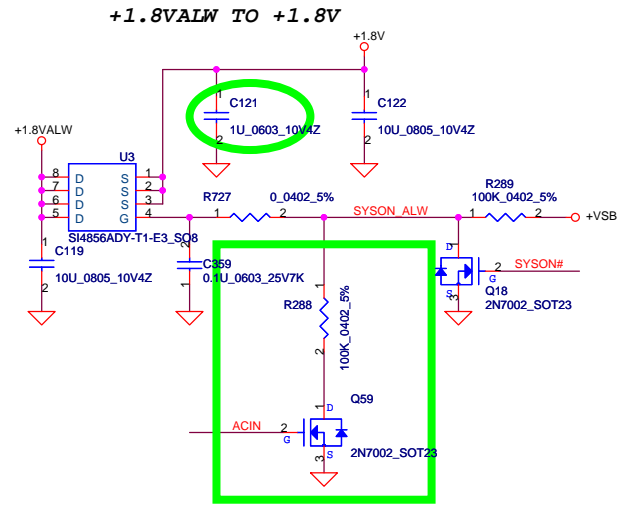
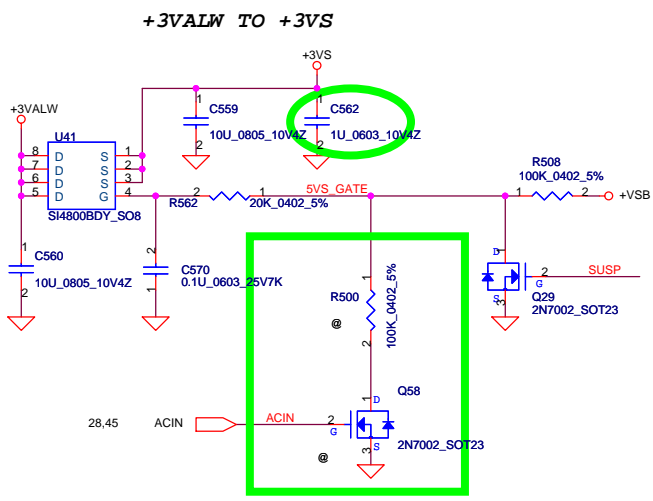
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Size B	Document Number	Date		Rev
	KAW60 LA-4661P	Friday, August 08, 2008		0.1
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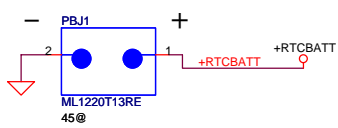
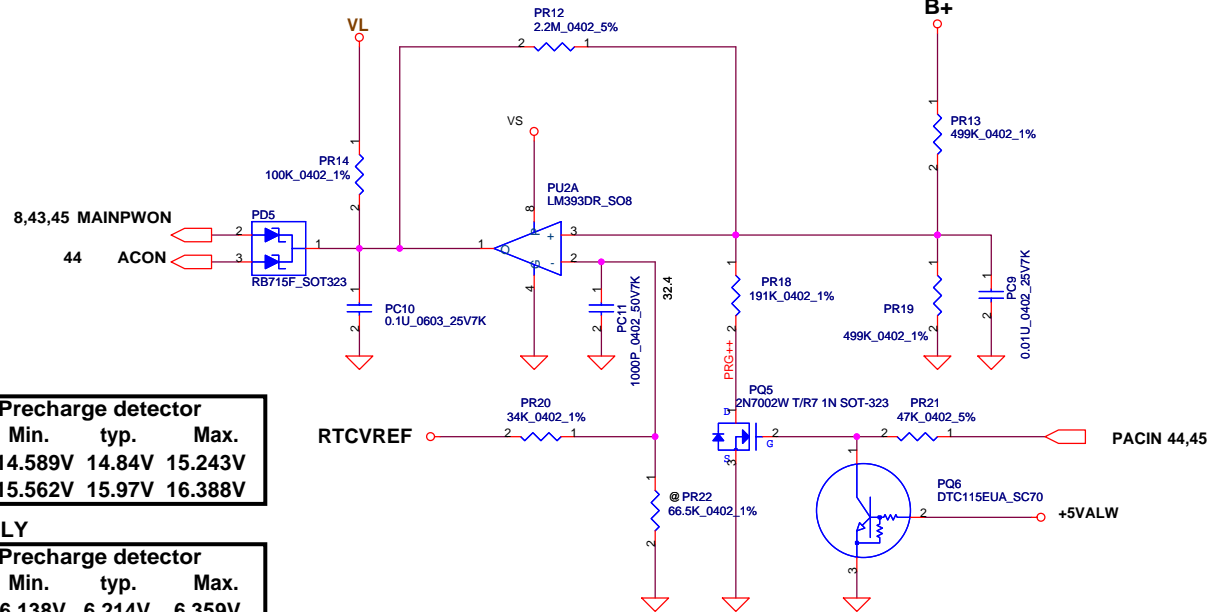
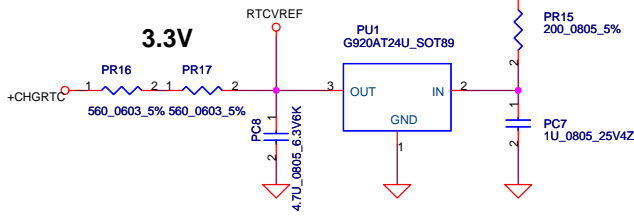
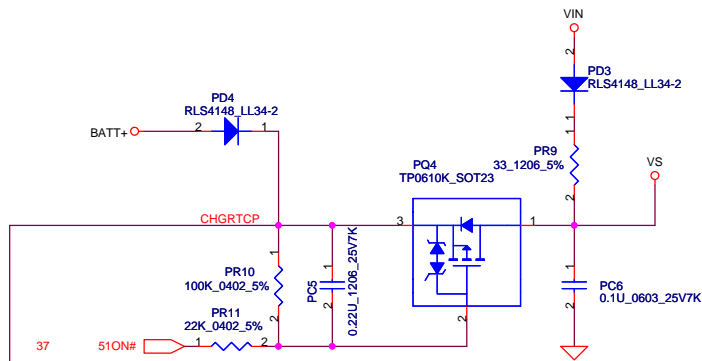
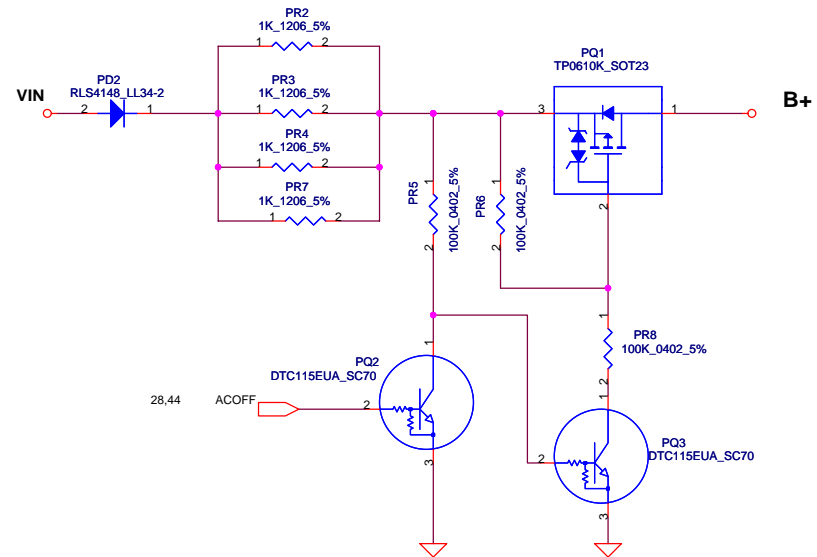
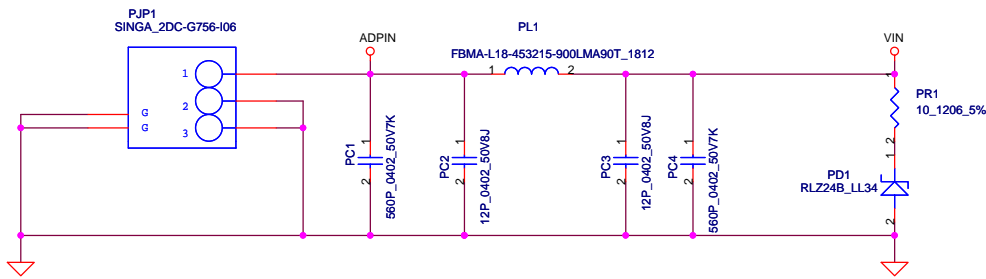
Gain= 14dB



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Size B	Document Number	Date:		Rev	0.1
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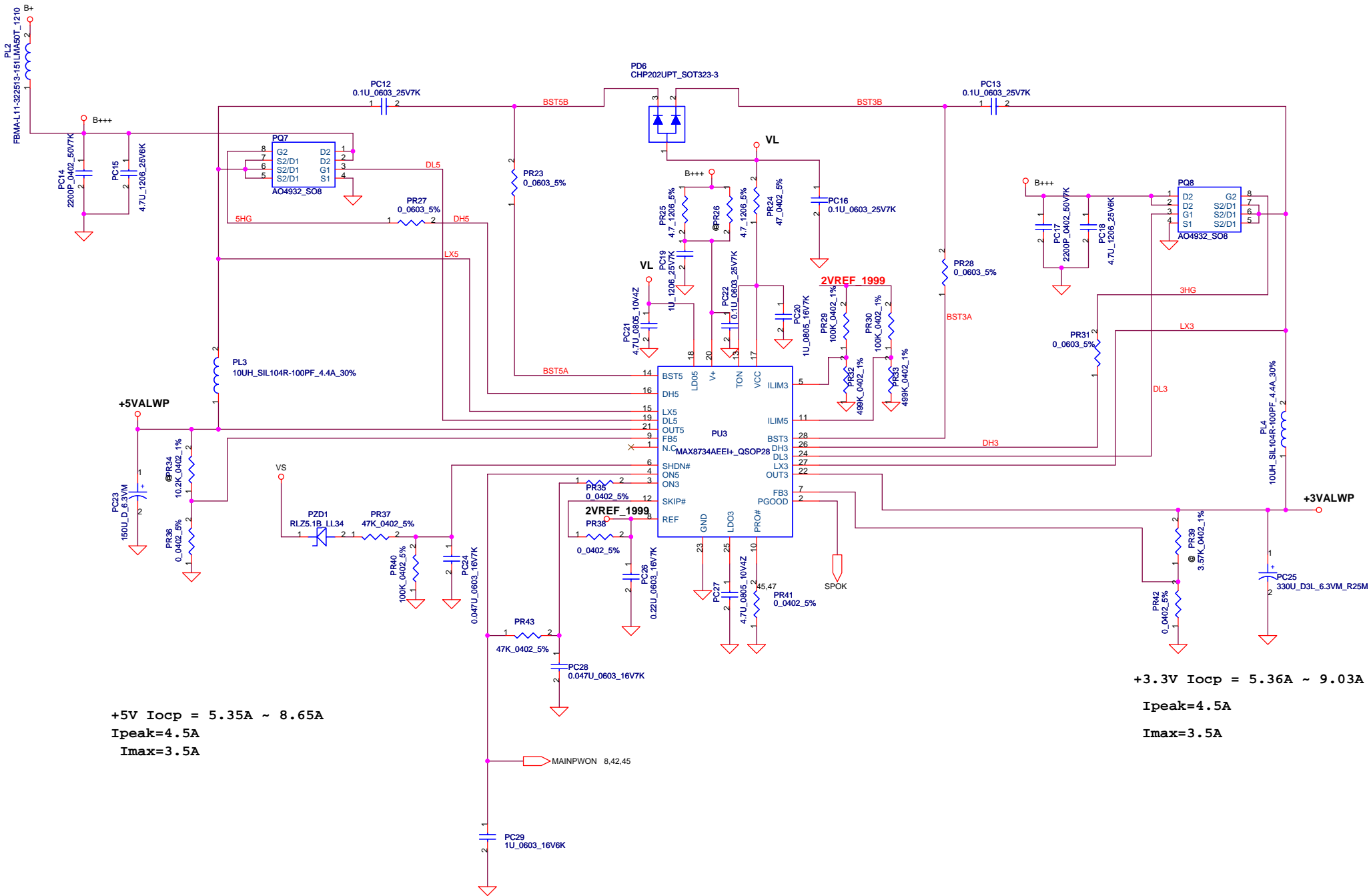
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/08	Deciphered Date	2006/03/08	DC INTERFACE	
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ACIN			
Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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				Date:	Friday, August 08, 2008
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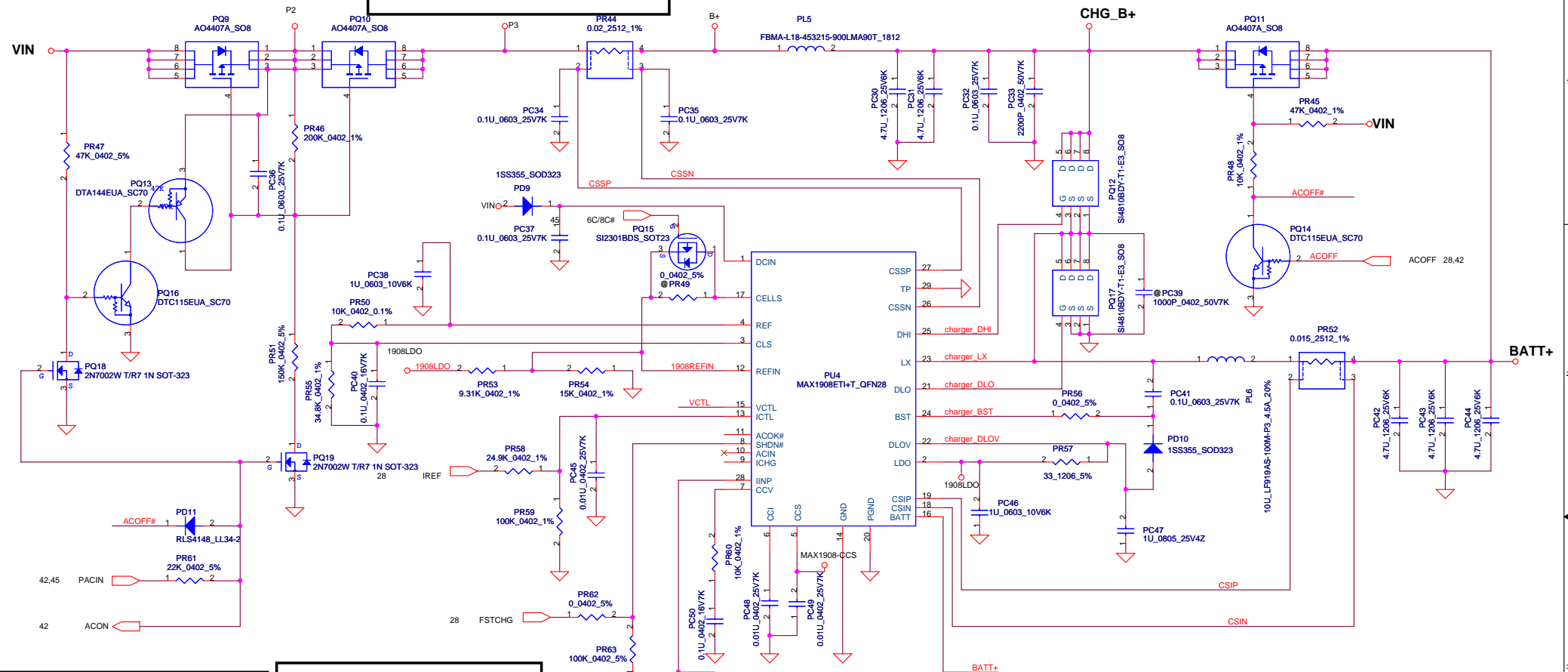
+5V Iocp = 5.35A ~ 8.65A
Ipeak=4.5A
Imax=3.5A

+3.3V Iocp = 5.36A ~ 9.03A
Ipeak=4.5A
Imax=3.5A

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Iadp=0~2.912A(65W)

CP Point:
 85% CP Point, 3.42A*0.85=2.907A-2.912A
 Iinput=(34.8K/44.8K)*(75/20)=2.912A



Charger ADJ	Calibrate#	PR170	PR173
4.0V	L	@	@
4.1V	L	665K	221K
4.2V	H	@	@

$V_{refin} = V_{1908LDO} * (15K / (9.31K + 15K)) = 5.4V * (15K / (9.31K + 15K)) = 3.331V$
 $V_{vctl} = 3.331 * (221K / (221K + 665K)) = 0.83087V$
 $V_{batt} = CELLS * (4 + (0.4 * (V_{vctl} / V_{refin}))) = 3 * (4 + (0.4 * (0.83087 / 3.331))) = 12.29v$

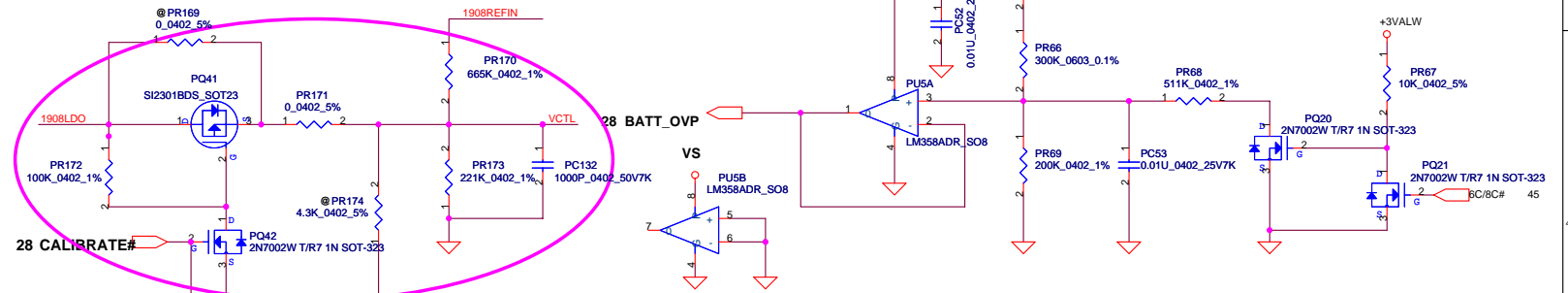
IREF=0.832*Icharge
 IREF=0.73~3.3V

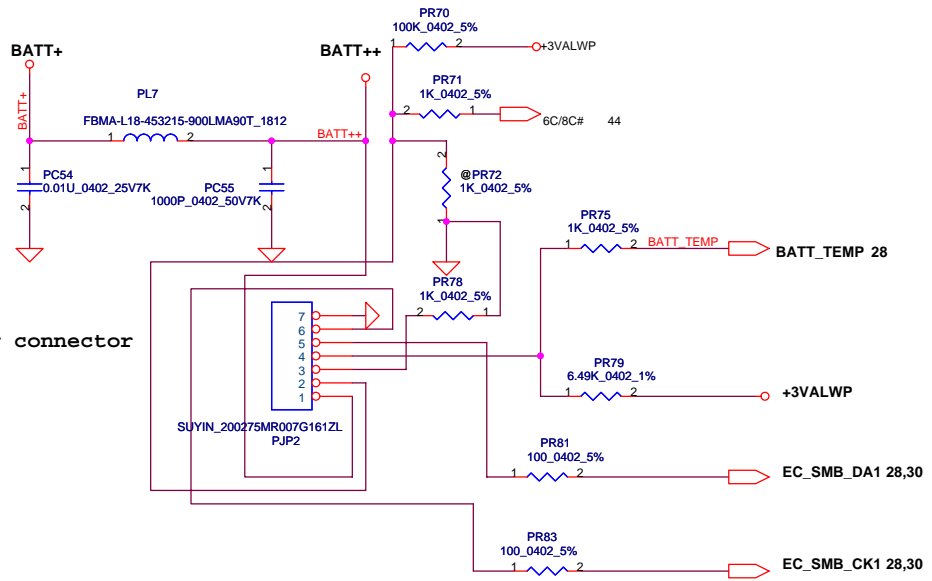
2P3S:4400mAH
 0.8C=3.52A

OVP-Voltage:
 LI-3SBattery Pack=13.5V---BATT-OVP=2.0061V
 Battery-OVP=0.1486*BATT+

Vbatt=CELLS*(4V+(0.4*(Vvctl/Vrefin)))

Charge voltage
 3S CC-CV MODE : 12.6V



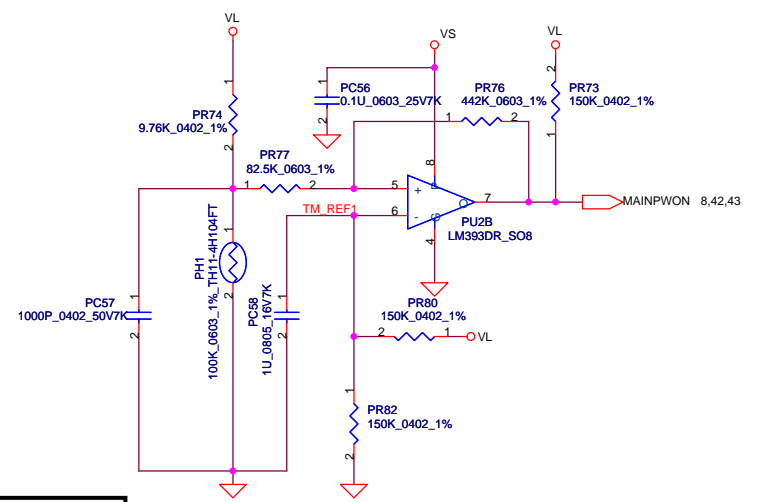


PJP2 battery connector

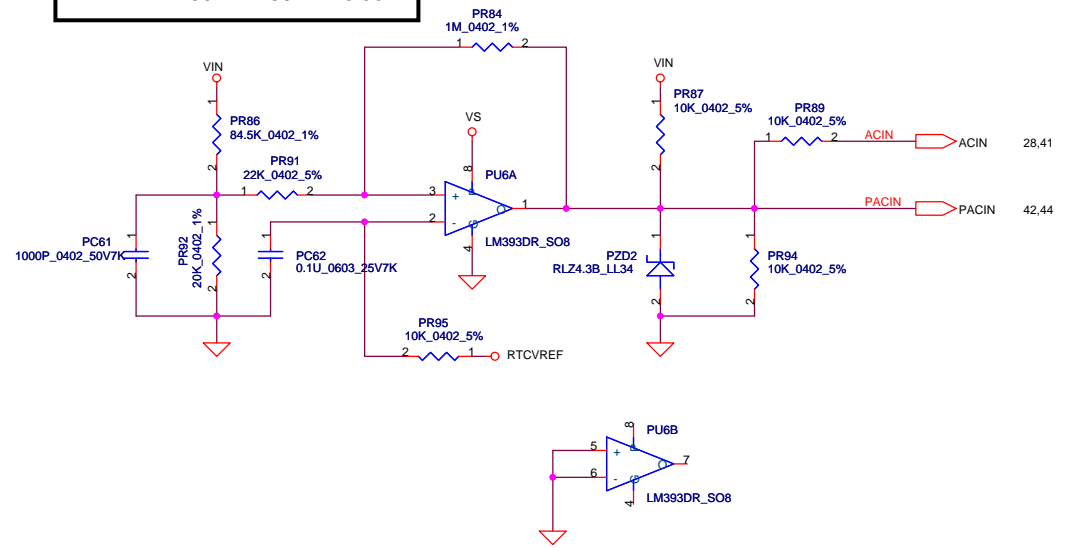
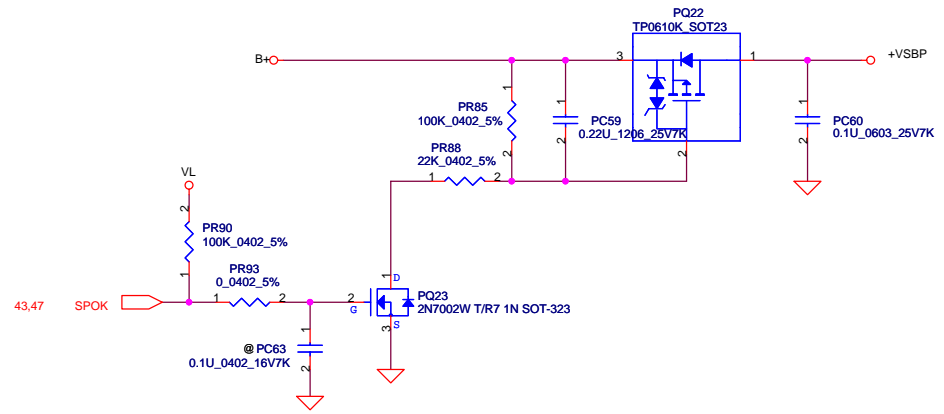
- SMART Battery:
- 1.GND
 - 2.SMC
 - 3.SMD
 - 4.TS
 - 5.B/I
 - 6.ID
 - 7.BATT+

KAW60 is used JAL90 battery connector footprint, but pin definition is reverse compare with KAW60 original battery connector, so schematic must be change to satisfy with JAL90 connector.

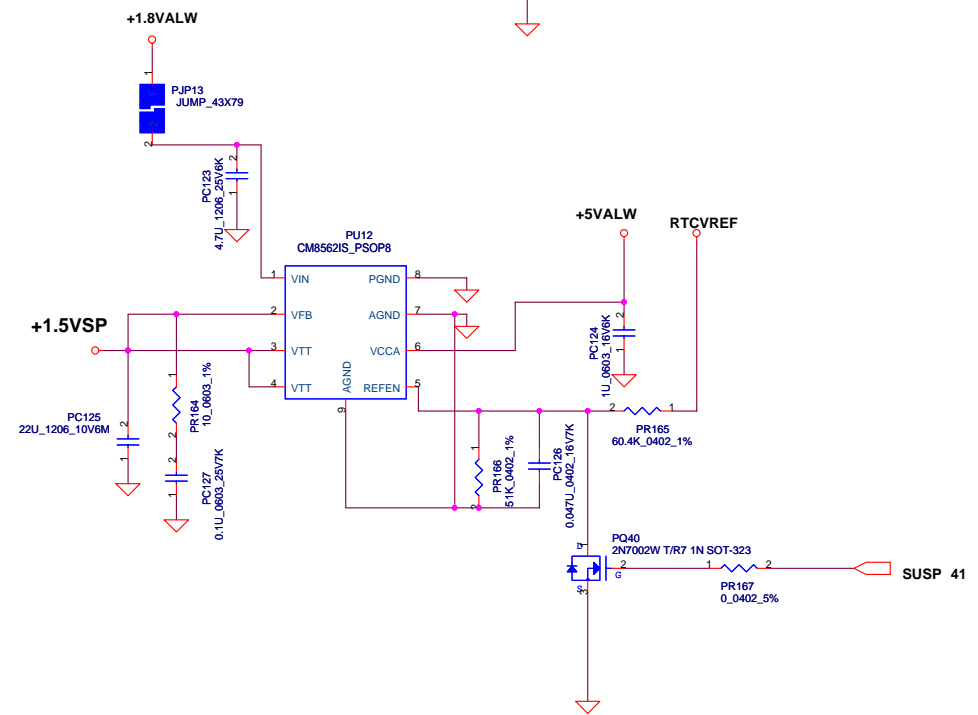
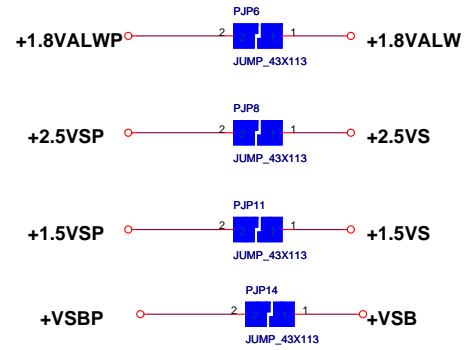
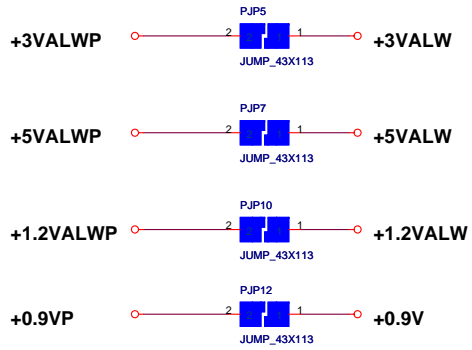
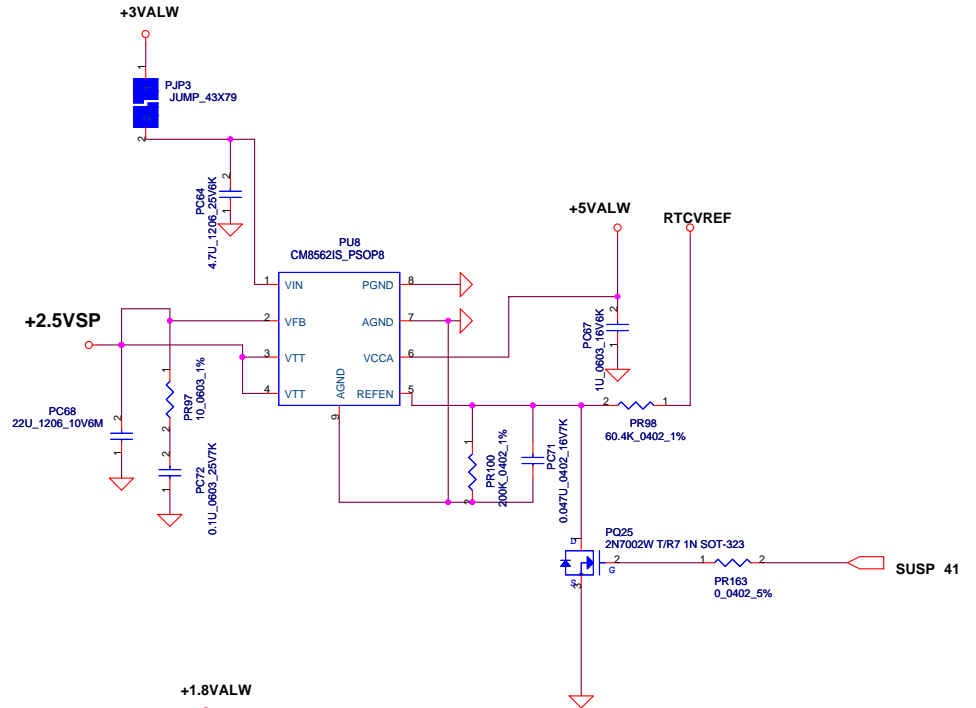
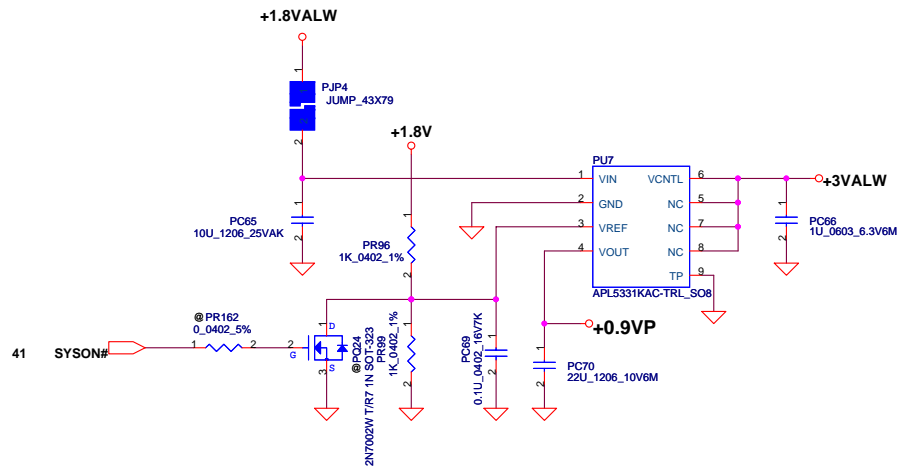
PH1 under CPU botten side :
 CPU thermal protection at 90 degree C
 Recovery at 70 degree C



Vin Detector		
Min.	typ.	Max.
H-->L 16.976V	17.257V	17.728V
L-->H 17.430V	17.901V	18.384V



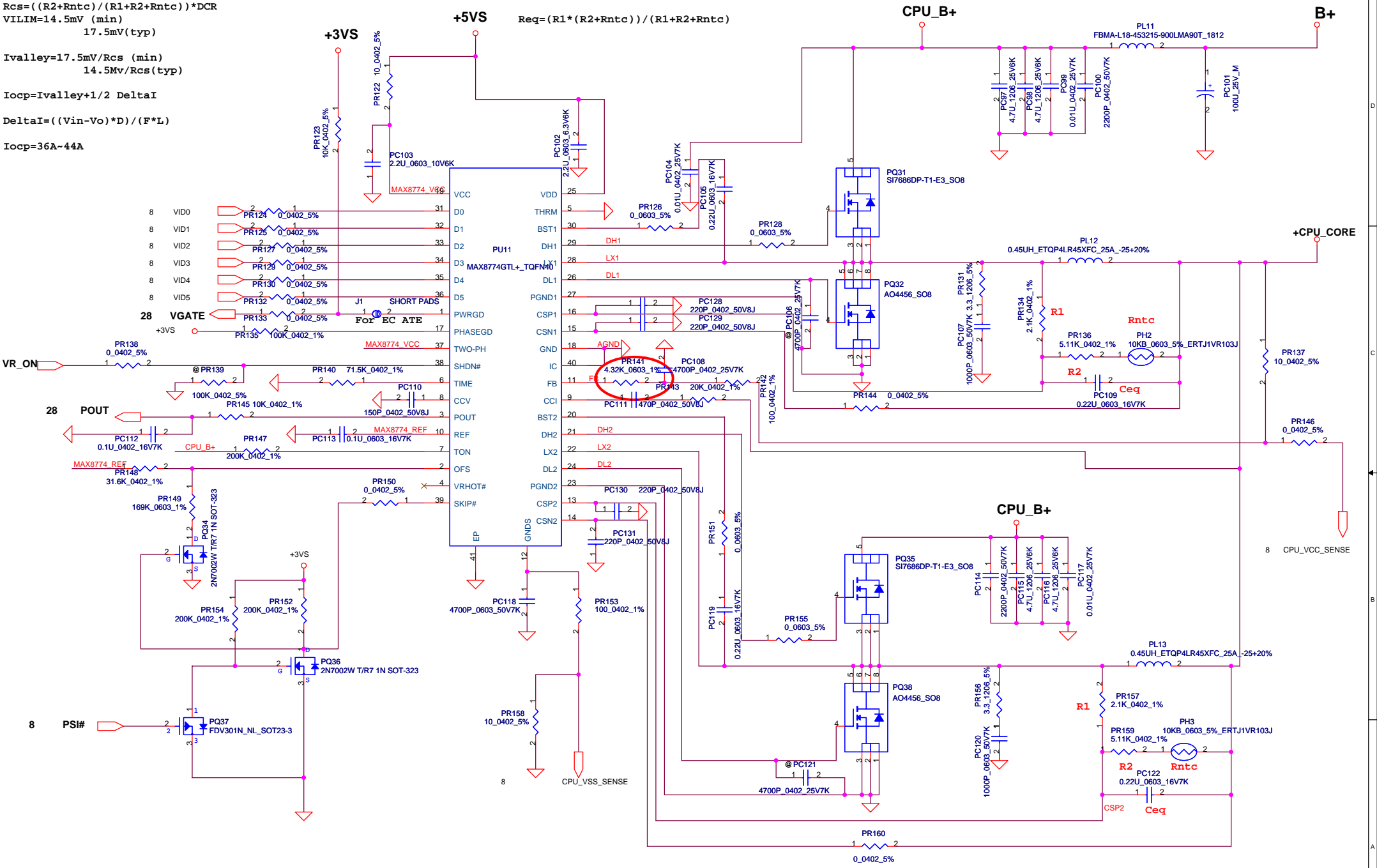
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OCP Setting:
 $Rcs = ((R2 + Rntc) / (R1 + R2 + Rntc)) * DCR$
 $VILIM = 14.5mV$ (min)
 $17.5mV$ (typ)
 $Ivalley = 17.5mV / Rcs$ (min)
 $14.5mV / Rcs$ (typ)
 $Iocp = Ivalley + 1/2 \Delta I$
 $\Delta I = ((Vin - Vo) * D) / (F * L)$
 $Iocp = 36A \sim 44A$

$Rcs * Ceq = L / Req$ must be satisfy!
 $Req = (R1 * (R2 + Rntc)) / (R1 + R2 + Rntc)$



<-BOM Structure>

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Size	Document Number	KAW60		Rev	0.1
Custom	Date:	Friday, August 08, 2008	Sheet	48	of 50

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	material issue.	Change to currently design	0.1	44	Change PQ9, PQ10, PQ11 from SB944070000(S TR AO4407 1P SO8 W/D) to SB00000DL00(S TR S TR AO4407A 1P SO8)	08,07/22	to PVT
2	material issue.	Change to currently design	0.1	48	Change PQ31 and PQ35 from SB578400080(S TR SI7840-T1-E3 1N SO8) to SB000008L80(S TR SI7686DP-T1-E3 1N POWERPAK SO8)	08,07/22	to PVT
3	material issue.	AO4916 will be EOL, change to AO4932	0.1	43	Change PQ7 and PQ8 from SB000002W80(S TR AO4916 2N SO8) to SB00000BG00(S TR AO4932 2N SO8)	08,07/22	to PVT
4	BOM error	BOM error	0.1	48	Change PR141 from SD014200180(S RES 1/10W 2K 0603 1%) to SD014432180(S RES 1/10W 4.32K 0603 1%)	08,07/22	to PVT
5	material issue.	SI4810 will be EOL, change to SI4894.	0.1	47	Change PQ12, PQ17, PQ29, PQ30 from SB548100020(S TR SI4810BDY-T1-E3 1N SO8) to SB00000D300(S TR SI4894BDY-T1-E3 1N SO8)	08,07/22	to PVT
6	Add VGATE pull high resistor.	Add VGATE pull high resistor.	0.1	48	Add PR123 SD028100280(S RES 1/16W 10K 0402 5%)	08,07/22	to PVT
7							
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PHASE	PAGE	MODIFICATION LIST	PURPOSE
PVT/MP	P.19 & 24	Update CRT_DET & CRT_DET# net name	NA
	P.18 & 19	Change CRT_DET from GPIO61 to GPIO0 & reserved R741 , R742 , R743	For ACER AP test CRT detect feature
	P.20	Remove L71 , C694 & C697	For +3Vs (1.5V) , +5Vs (0.388V) , +1.8Vs (0.154V) on S5 leakage issue
	P.28	Change R519 from 100K to 10K	For RS690MC ENBKL had unexpected 3.3V pulse before normal display & white screen flash symptom appear
	P.14	Reserved U48 , U49 , R744 , R745 , R746 , R747 , C763	For RS690MC ENBKL , ENVDD if had unexpected 3.3V pulse before normal display
	P.28 & 31	Modify WL_ON_LED# from KB926 to JMINI1 control	WL LED activity behavior controlled by wireless mini card itself
	P.38	Update SW9 Footprint & P/N	NA
	P.41	Change R586 from 100K to 10K	For Susp# had 3V level glitch when G3 to S5 (Plug AC in) & caused +5Vs /+3Vs had leakage immediately
	P.6	Change D4 as SC1BAS16000(S DIO BAS16PT SOT-23)	Sourcer recommend
	P.26	Change U11 as SA000019910(S IC EE 1K CAT93C46VI-GT3 SOIC 8P)	SA093461070 (S IC EE 1K SO-8 I AT93C46-10SI-2.7) EOL
	P.50	Change T1 as SP050001210 / S X'FORM_ NS0013LF LAN (BOTHHAND)	MHPC X'form part not for ABO , Sourcer recommend
	P.18	Delete R695,R179,R484 for SB_TEST pin	AMD reference schematic
	P.20	Reserved C764 (1u_0402)	AMD reference schematic & design guide
	P.38	Modify WL_LED power rail as +3Vs	NA
	P.28 & 38	Modify LED control of SATA drive from EC to SB (Add Q67)	EC(media_led#/pin86 , reference sata_led# from SB) control behavior abnormal
	P.17	Change C510 , C511 of 14.318MHz as 27P from 22P	NA
	P.37 & 25	Change D5 , D21 as SC1BAS16000	NA
	P.26	Add L77 , C765 , C766 , C767 & change R645 / R647 as L78 / L79 , reserved C719 , C724	EMI request
	P.31 & 34	Stuff L66 , L67 , L68 & remove R615 , R616 , R598 , R599 , R600 , R601	EMI request
	P.29	Stuff D28	ESD request
	P.6	Update net EN_DFAN1_R	NA
	P.6	Update JCPU1 PCB footprint as SOC127MM48X51-948	NA
	P.26	Add R749 , R750 (300ohm_0402)	For LAN external EEPROM program issue
	P.31	Add D32 (SCA00000A00)	ESD request
	P.28 & 31	Reserved R751 & R752	Reserved WL_LED controlled by EC (Navarrow project)
	P.24	Change C411 & C412 PN from SE081680k80 to SE071680J80	AP Code
	P.6	Change U1 as SA00001Z900 (S IC APL5605KI-TRL SOP 8P)	(SA009930010) S IC G993P1UF SOP 8P FAN LDO EOL
	P.15	Change C330 as 0402 package	NA

ZZZ



PCB 06B LA-4661P REV1 MB

LA4661MB Rev0 : DA600009Z00

LA4661MB with Sub/B Rev1 : DAZ06B00100

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