

Compal Confidential

HBL50 Schematics Document

**Intel Yonah Processor with 945GM/945PM + DDRII + ICH7M
(With nVIDIA NB7M-SE)**

2006-09-05

REV: 1.0

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File Name : LA-2922

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

G72MV	G72MV@
	G72MV64@
	G72MV128@
G72MZ	G72MZ@
G73	G73M128@

BTO Option Table

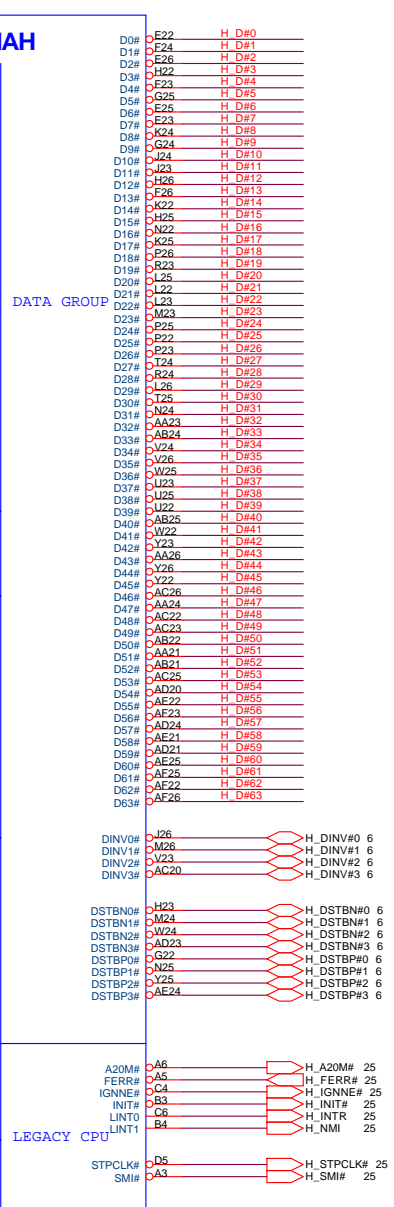
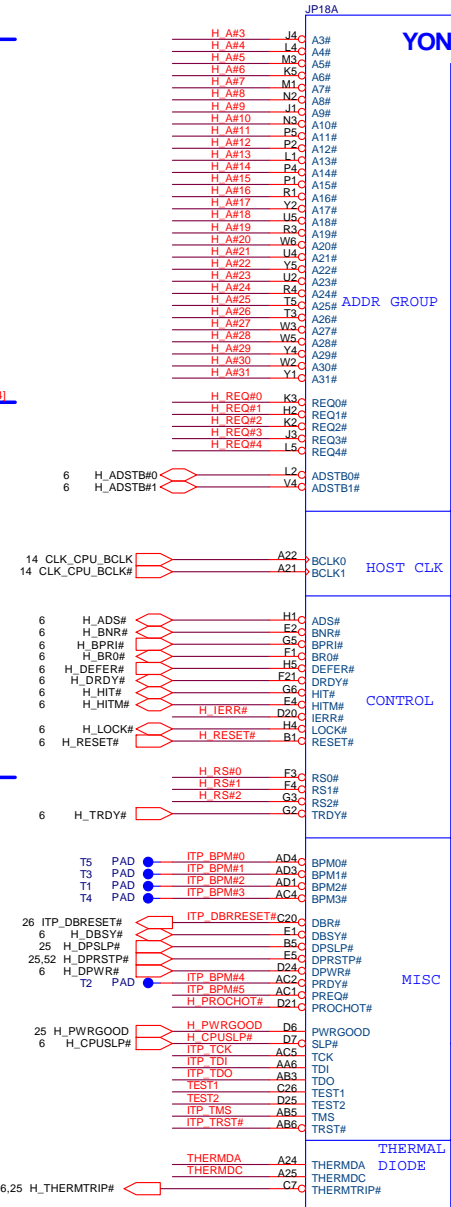
BTO Item	BOM Structure
VGA	PM@ + VGA@
UMA	GM@
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI CARD1	MINI1@
MINI CARD2	MINI2@
SATA-to-IDE	8040@
PATA	PATA@
GRAPEVINE	GRA@
G72MV Only	G72@
G73 Only	G73@
VRAM	X76@
VRAM 64M	64@
VRAM 128M	64@+128@
VRAM 256M	64@+128@+256@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
Sub-woofer	SUB@
5789&5787	8789@
4401&5789	0189@
VP1020	VP1020@
INTERNAL MIC	INTMIC@
1394	1394@
SATA HDD	SATA@
DVI	DVI@
CardReader	4IN1@
New Card	EXP@

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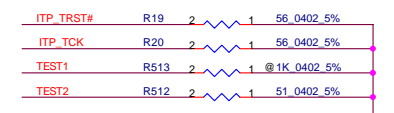
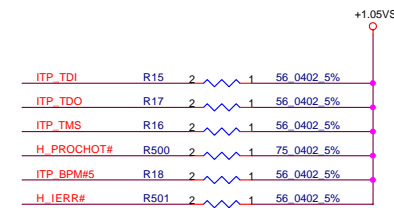
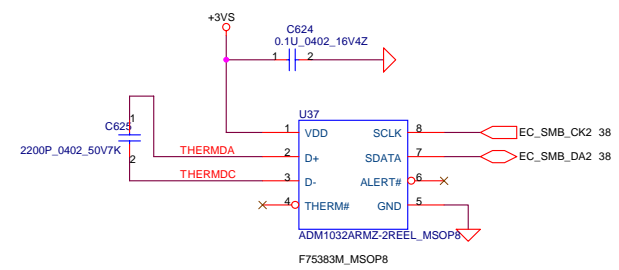
6 H_A#[3..31] H_A#[3..31]

6 H_REQ#[0..4] H_REQ#[0..4]

6 H_RS#[0..2] H_RS#[0..2]

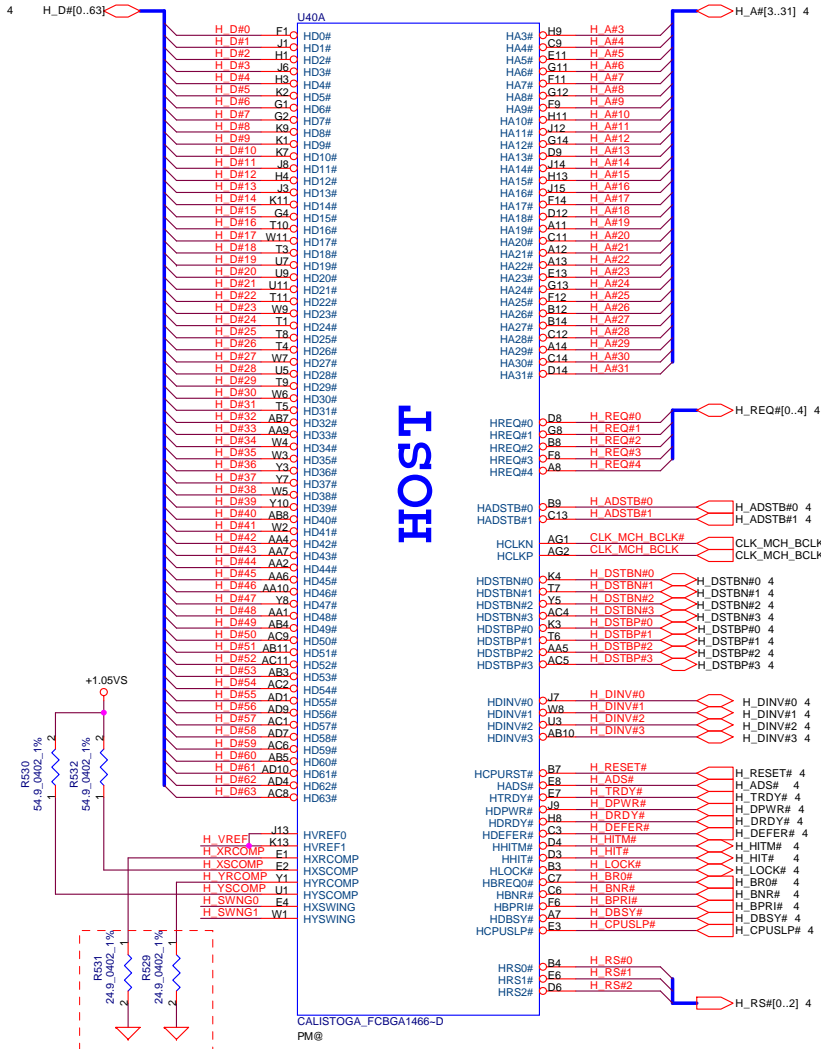


H_D#[0..63] H_D#[0..63] 6

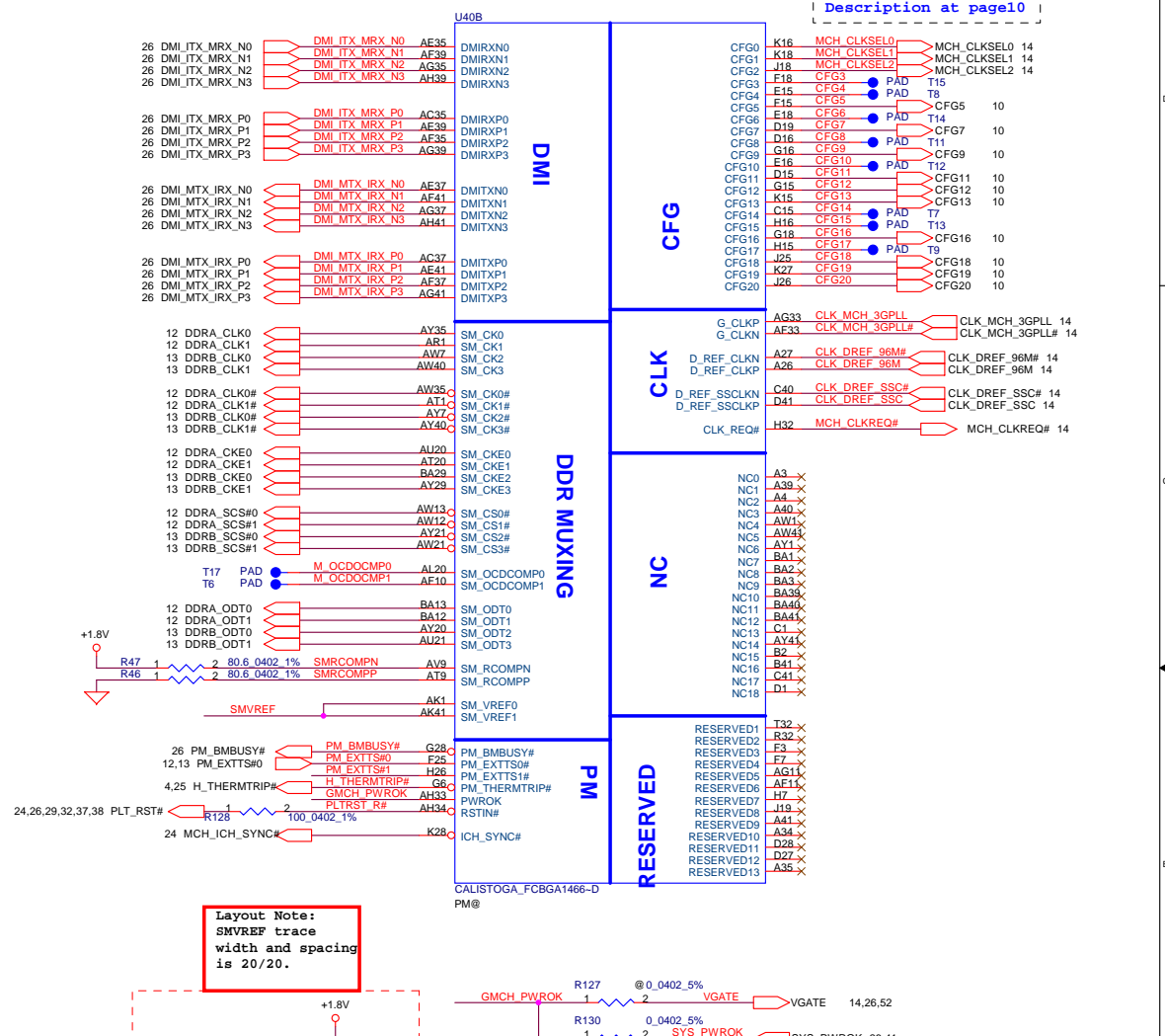
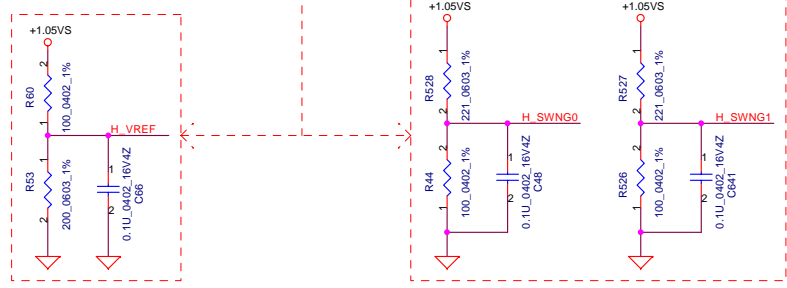


Layout Note:
THERMDA & THERMDC Trace / Space = 10 / 10 mil

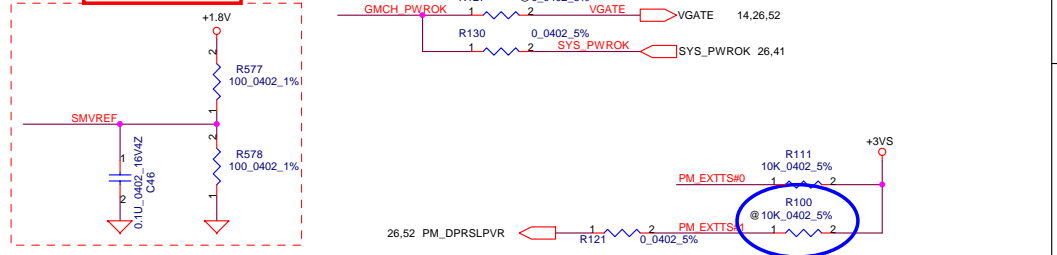
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Layout Note:
 H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 /
 H_SWNG1 trace width and spacing is 10/20.

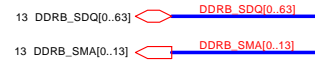
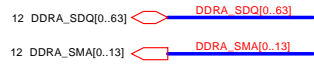


Layout Note:
 SMVREF trace
 width and spacing
 is 20/20.

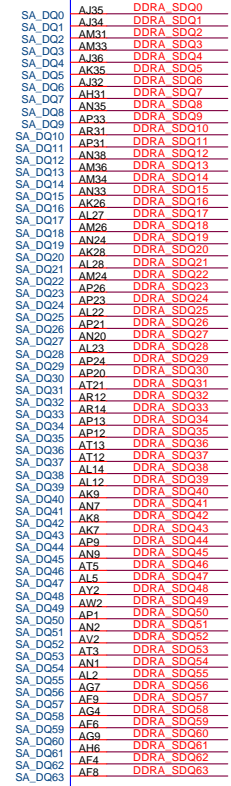


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DDR SYS MEMORY A



DDR SYS MEMORY B



check layout

check layout

CALISTOGA_FCBGA1466-D
 PM@

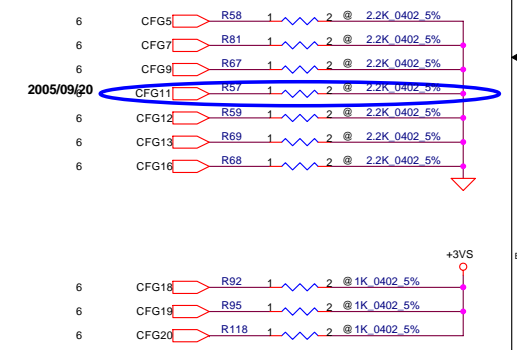
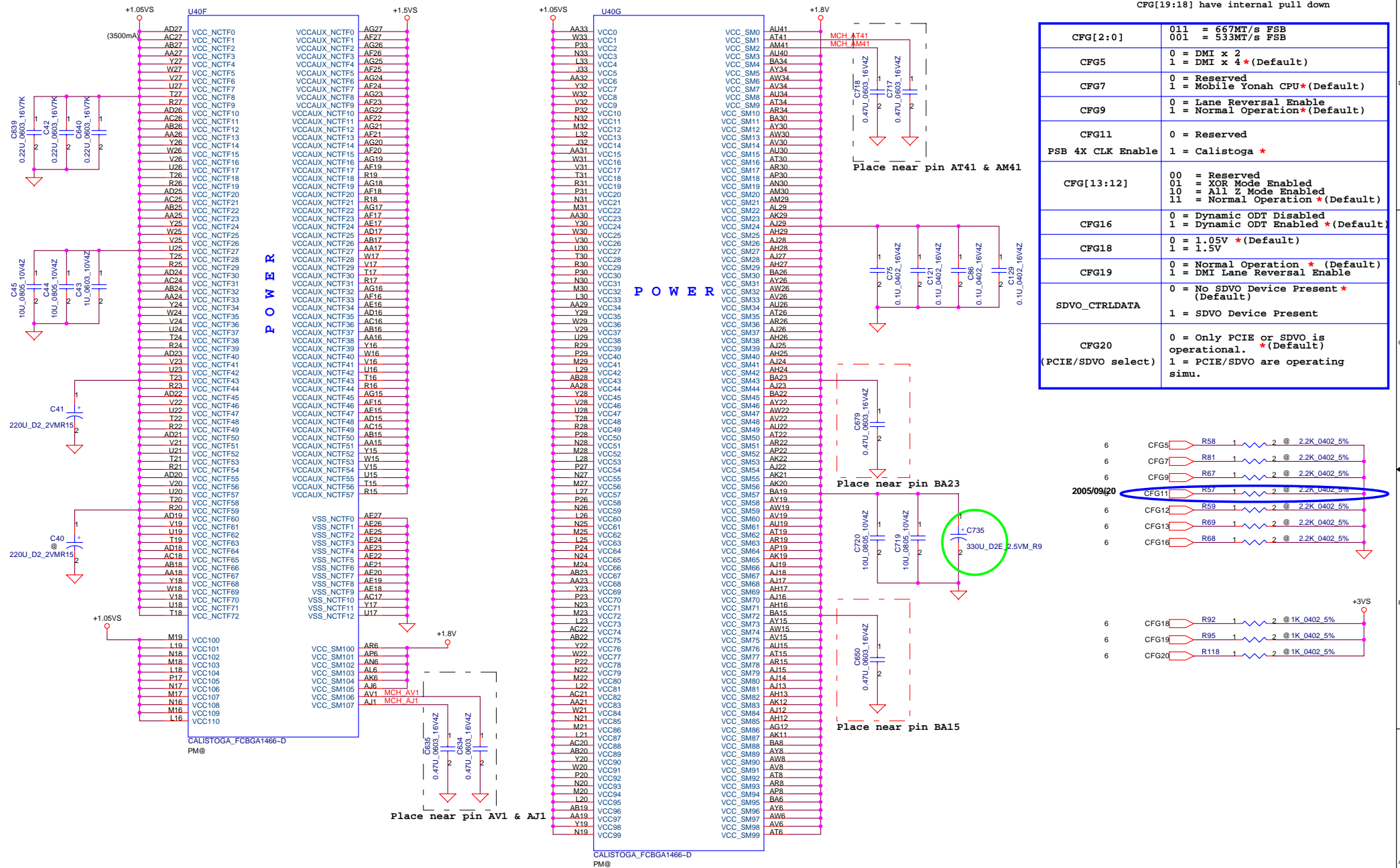
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 PM@

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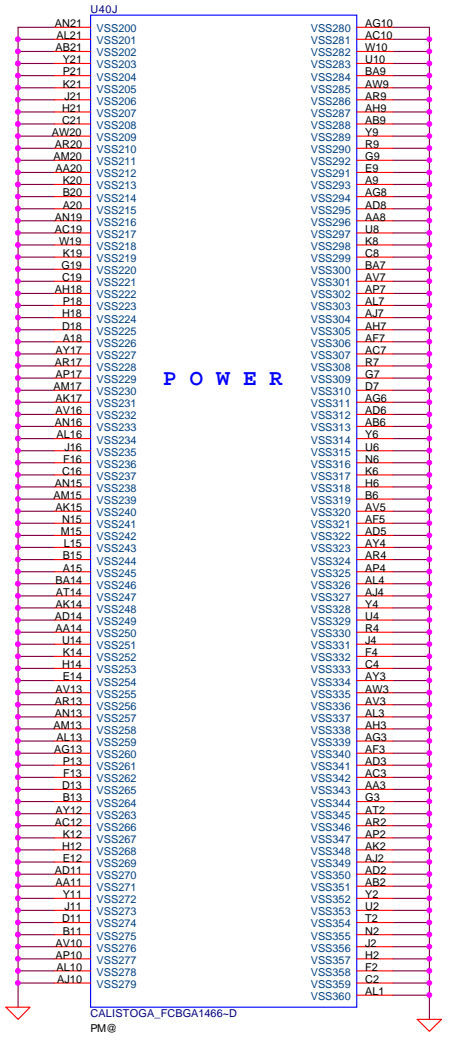
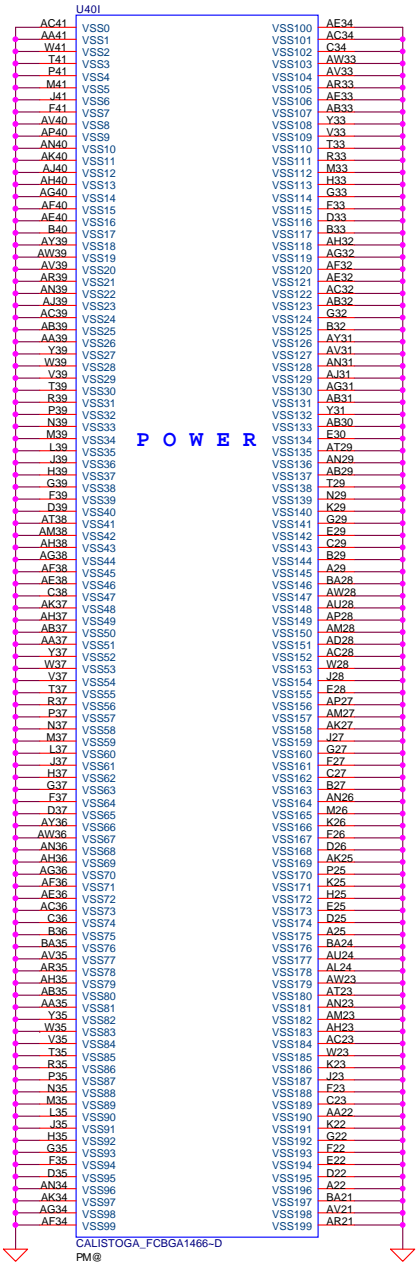
Strap Pin Table

CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation*(Default)
CFG11	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.

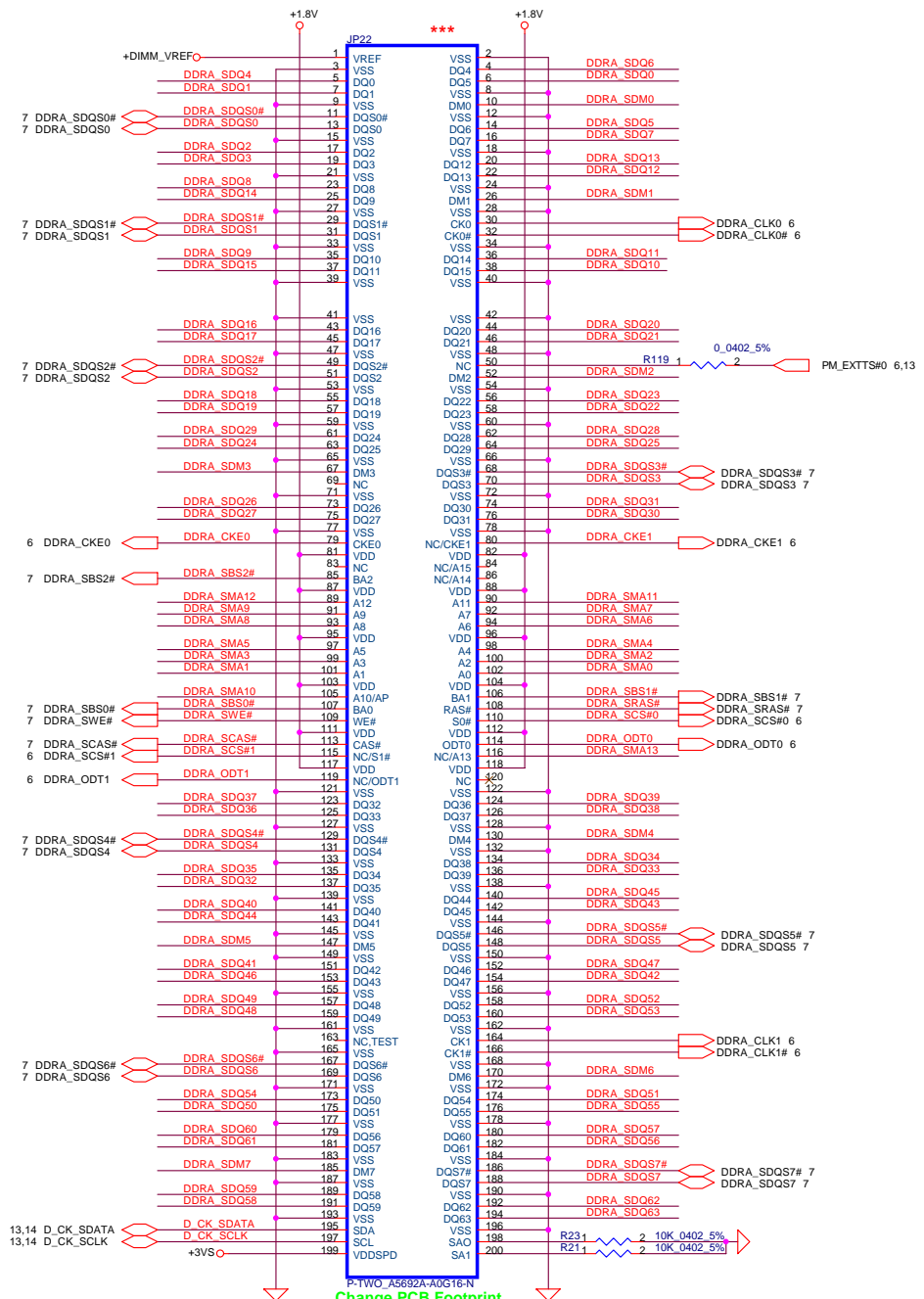


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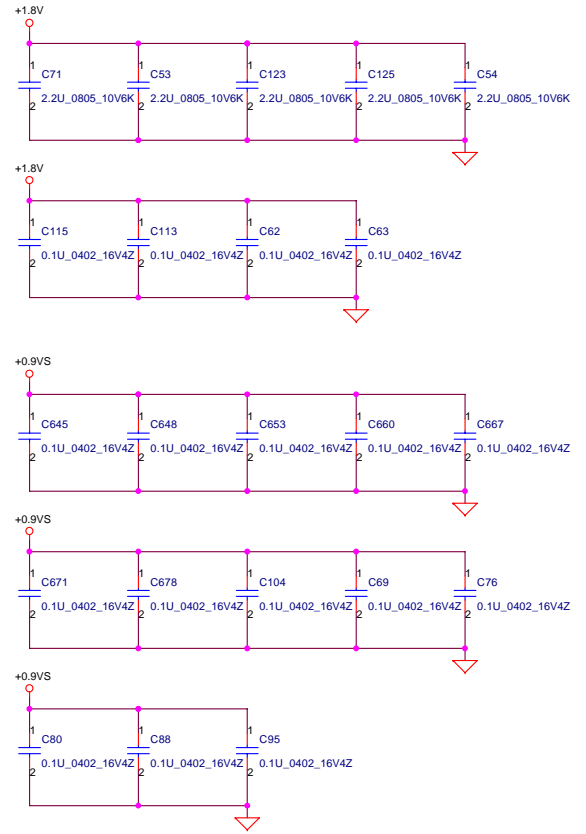
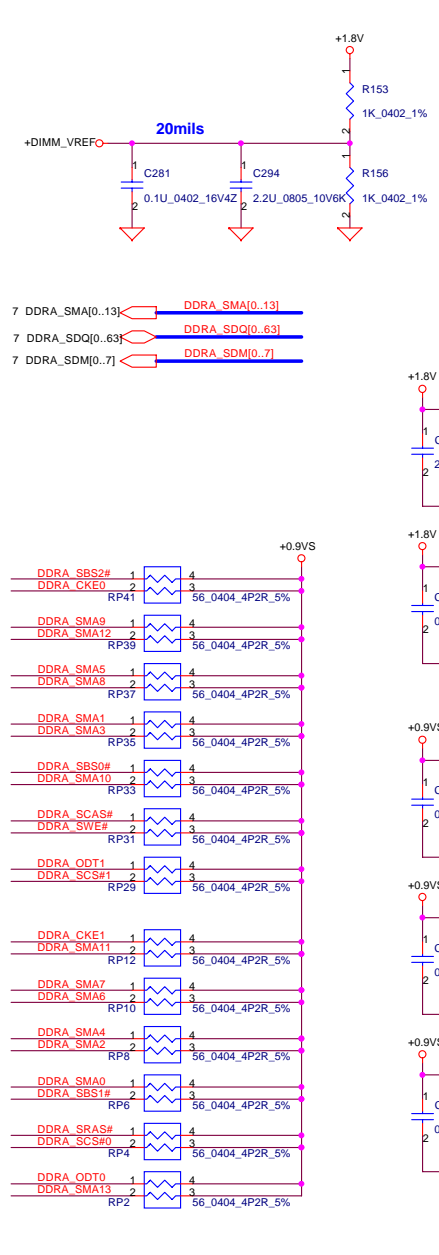


POWER

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DIMM0 STD H:9.2mm (BOT)



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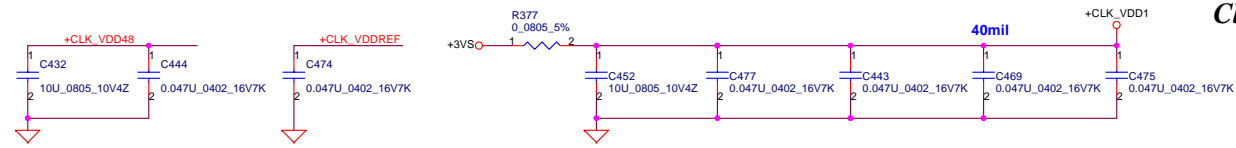
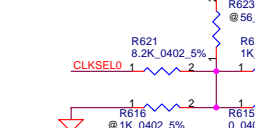
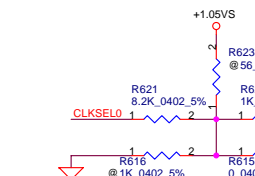
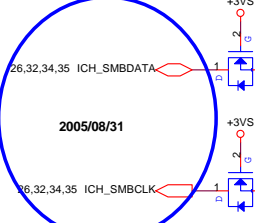
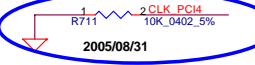
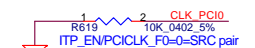
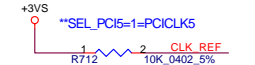
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPR325

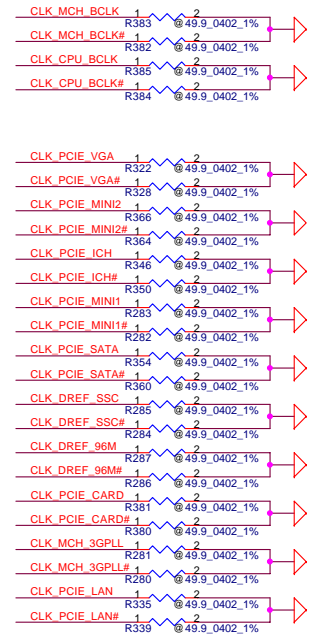
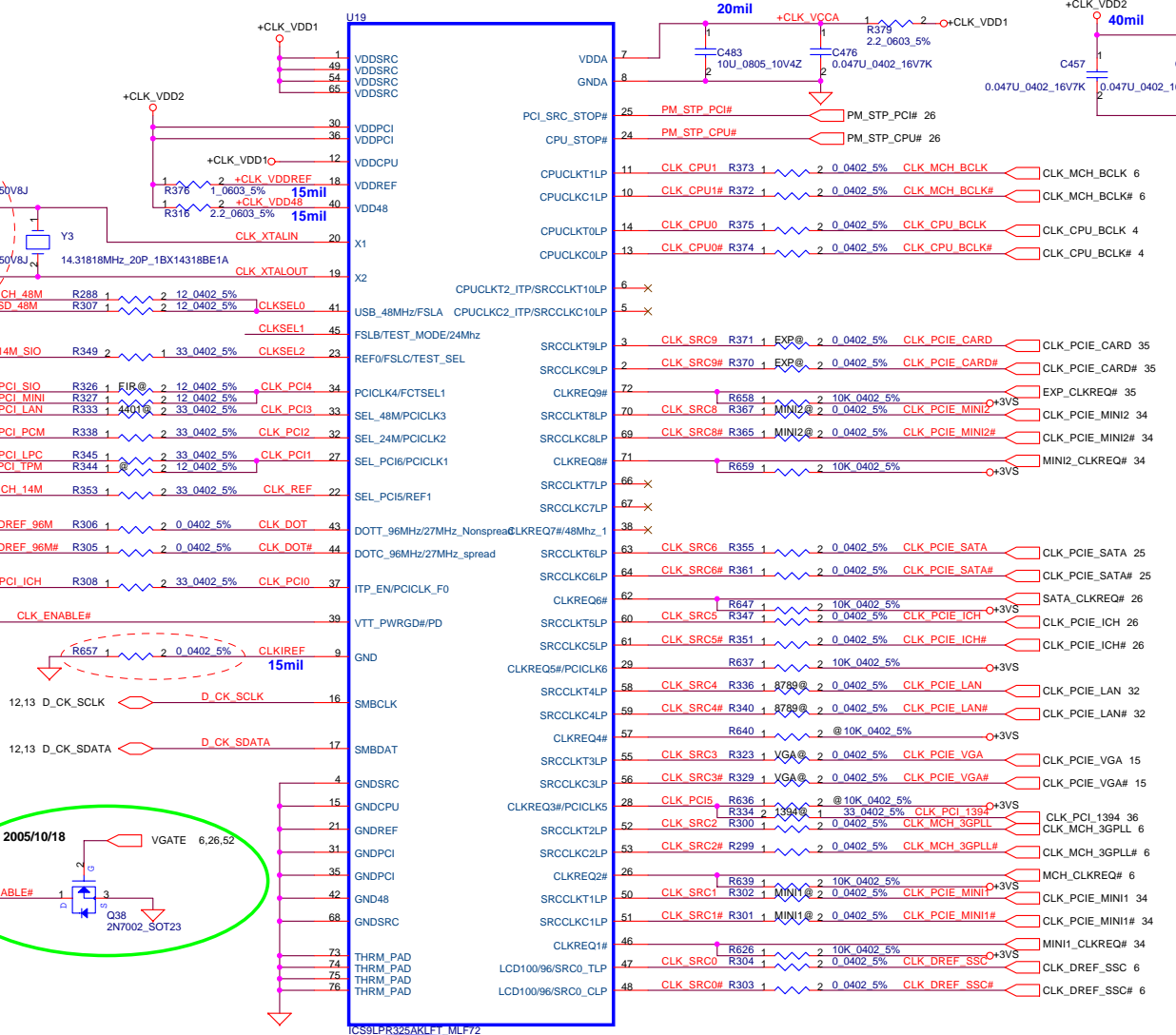
	0	1
**SEL_PCI5/REF1	CLKREQ3#	33.3MHz PCICLK5
**SEL_PCI6/PCICLK1	CLKREQ5#	33.3MHz PCICLK6
**SEL_24M/PCICLK2	TESTMODE	24MHz Output
**SEL_48M/PCICLK3	CLKREQ7#	48MHz_1 Output
ITP_EN/PCICLK_F0	SRC pair	CPU_ITP pair

**SEL_24M/PCICLK2=0=TESTMODE
**SEL_PCI6/PCICLK1=0=CLKREQ5#

**SEL_PCI5=1=PCICLK5
ITP_EN/PCICLK_F0=0=SRC pair



Clock Generator

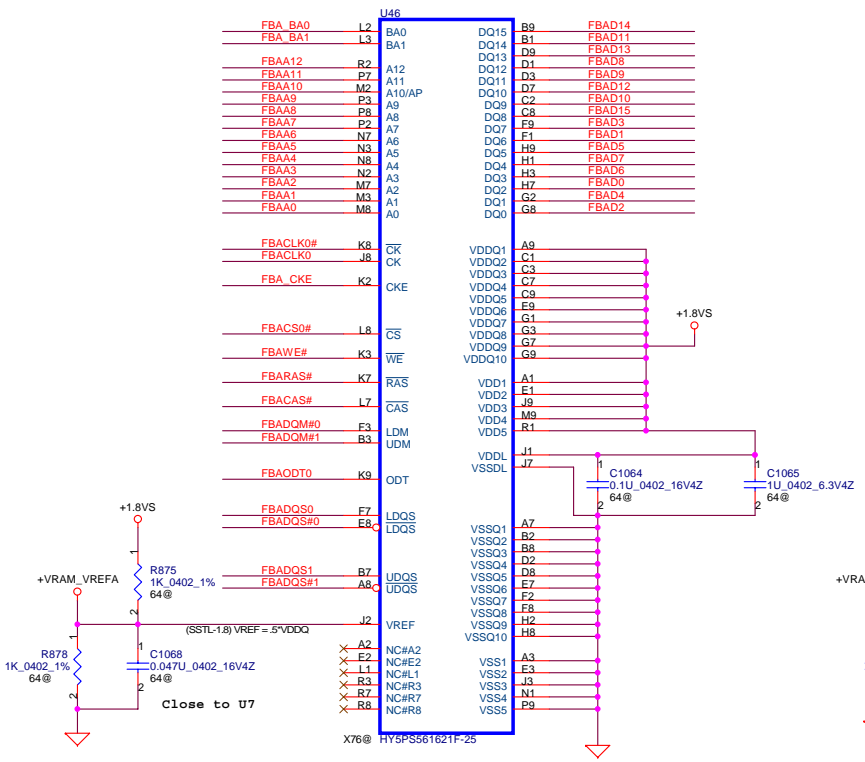


G73M: ICS9LPR325CKLFT_MLF72: SA00000RE20
* G72M: SLG8LP465VTR: SA00000T500

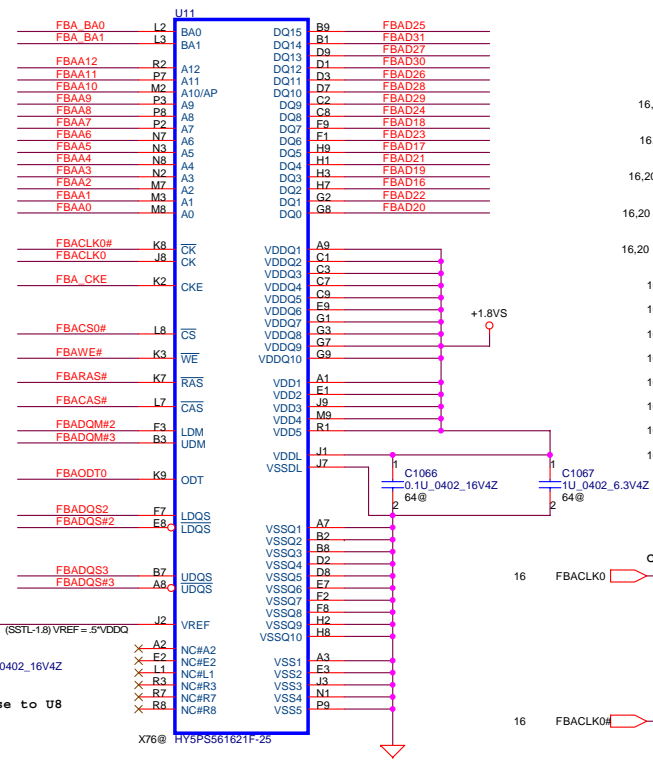
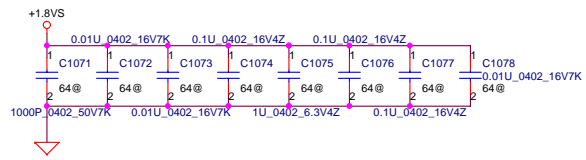
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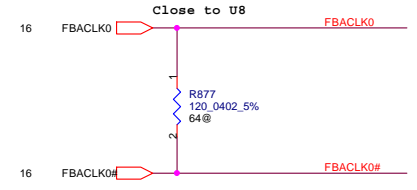
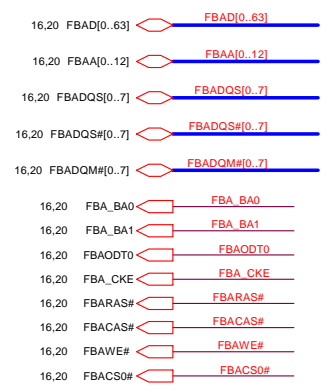
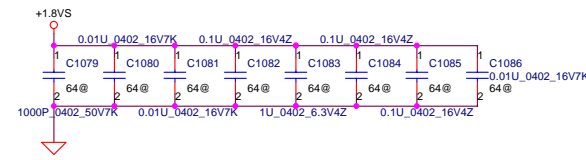
Compal Electronics, Inc.		
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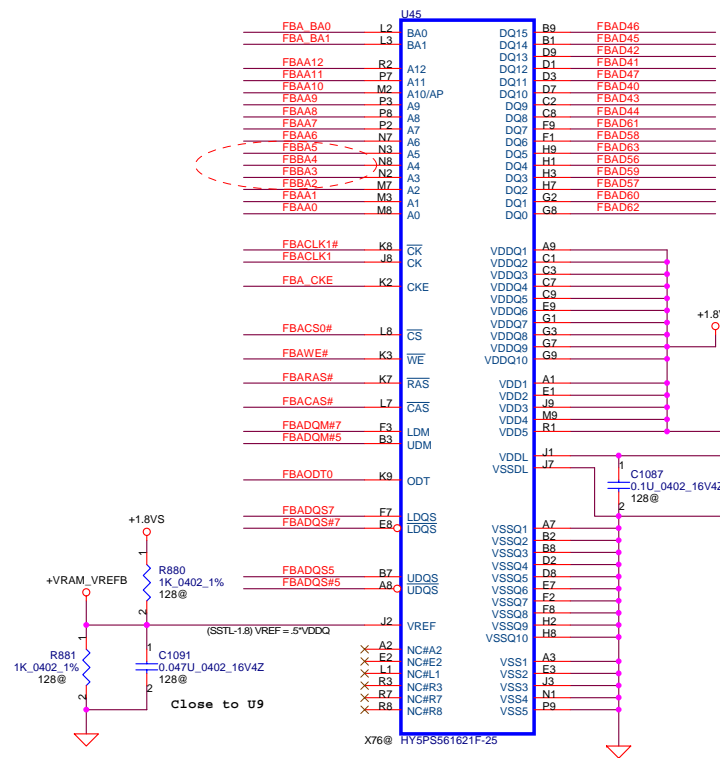
DDR2 BGA MEMORY



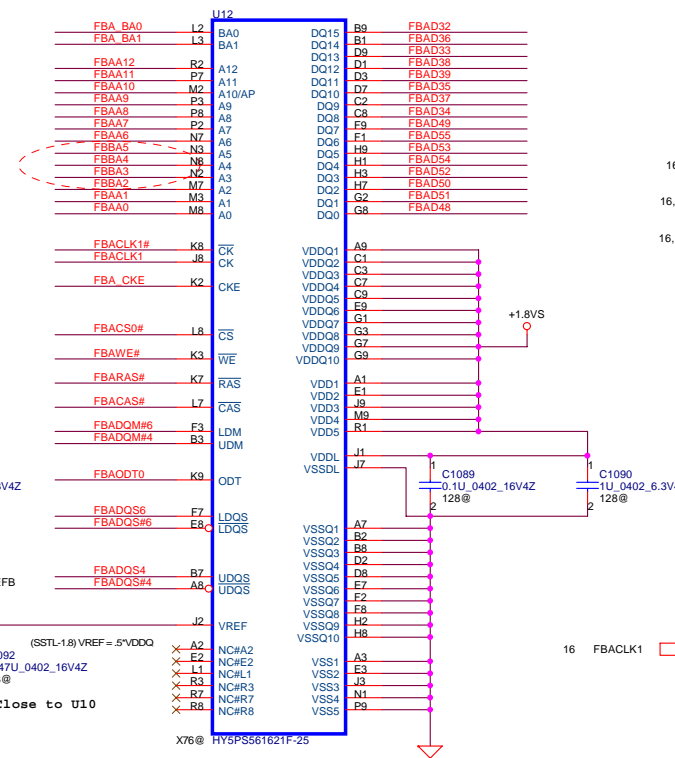
DDR2 BGA MEMORY



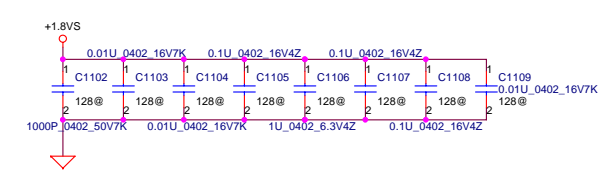
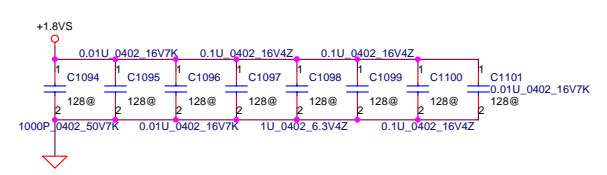
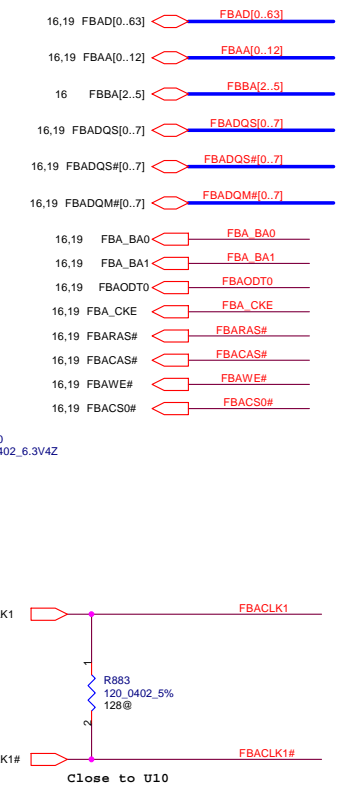
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DDR2 BGA MEMORY



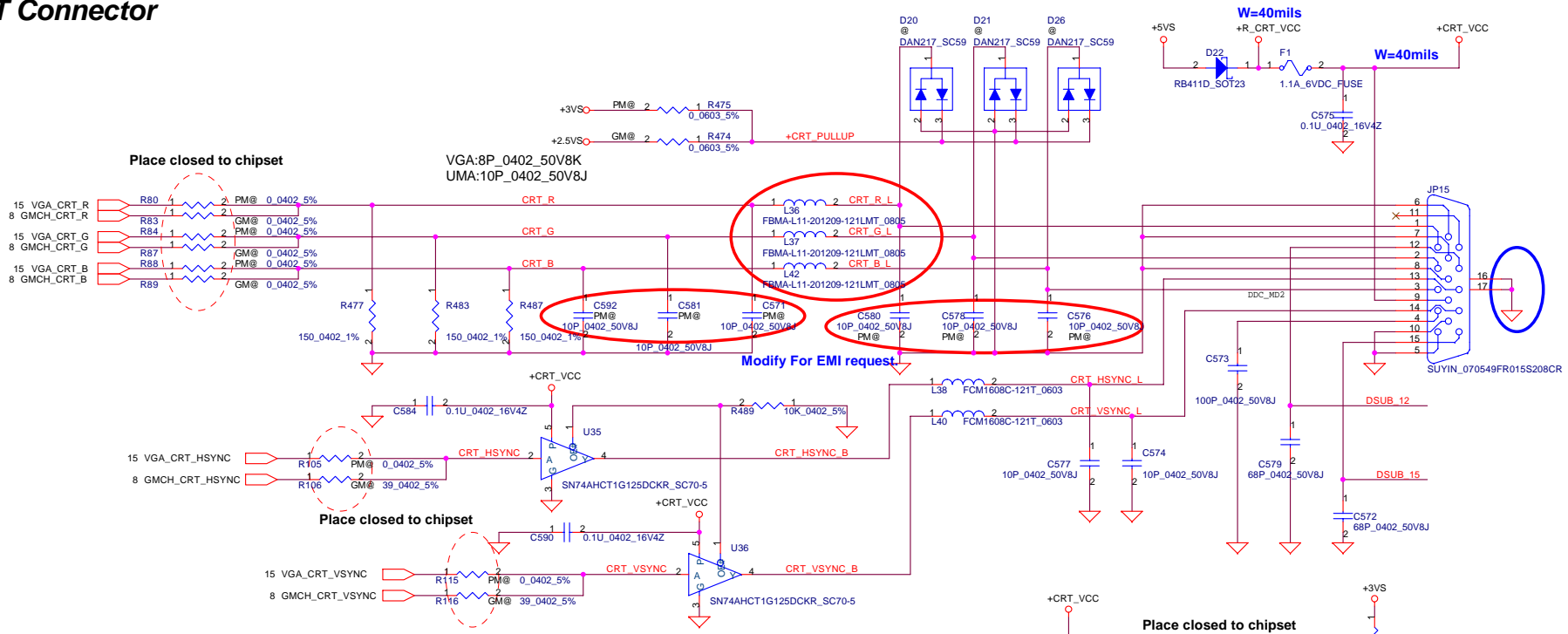
DDR2 BGA MEMORY



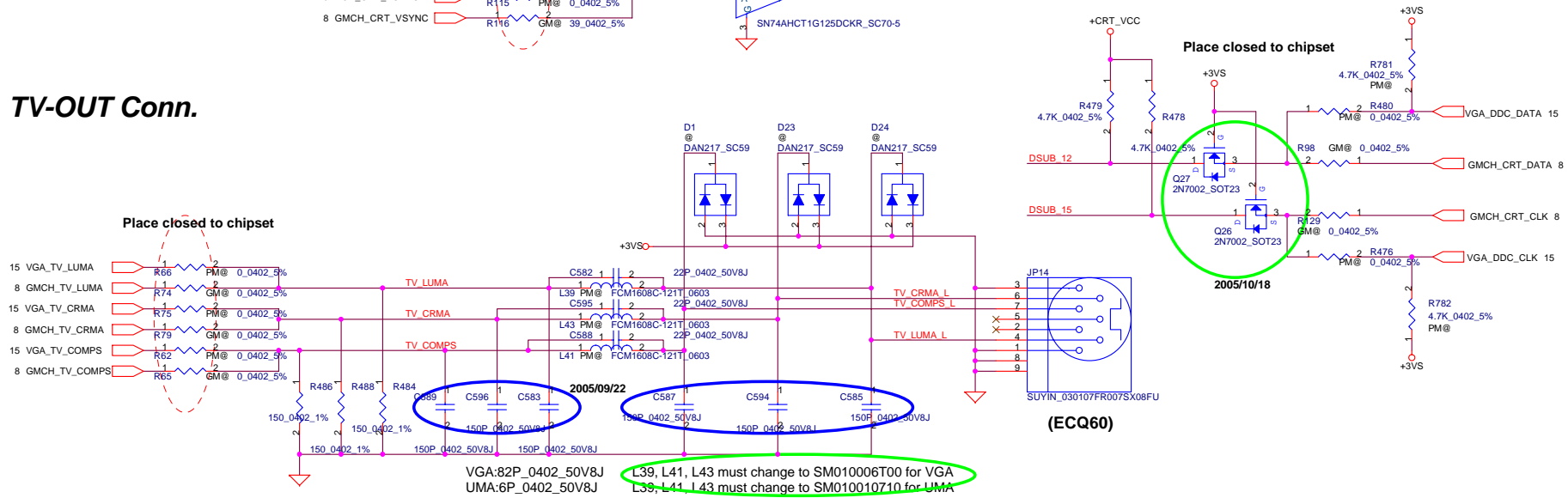
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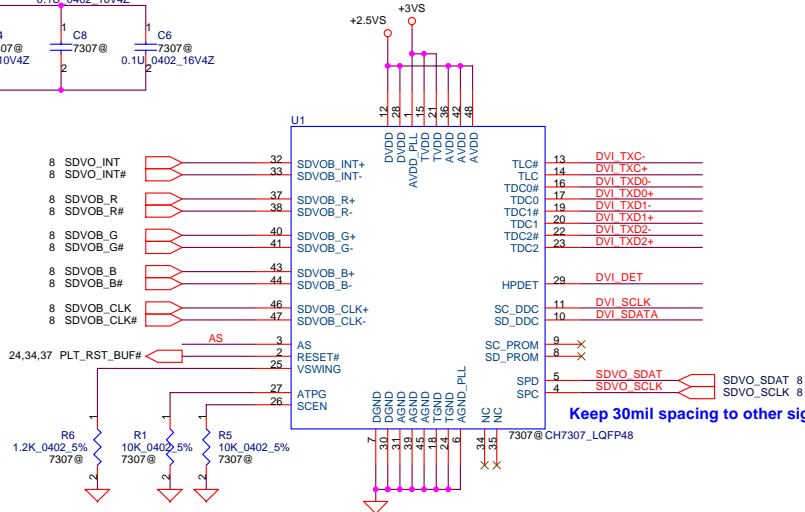
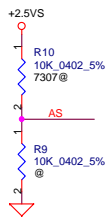
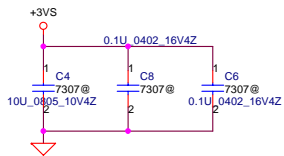
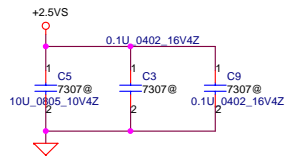
CRT Connector



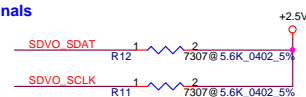
TV-OUT Conn.



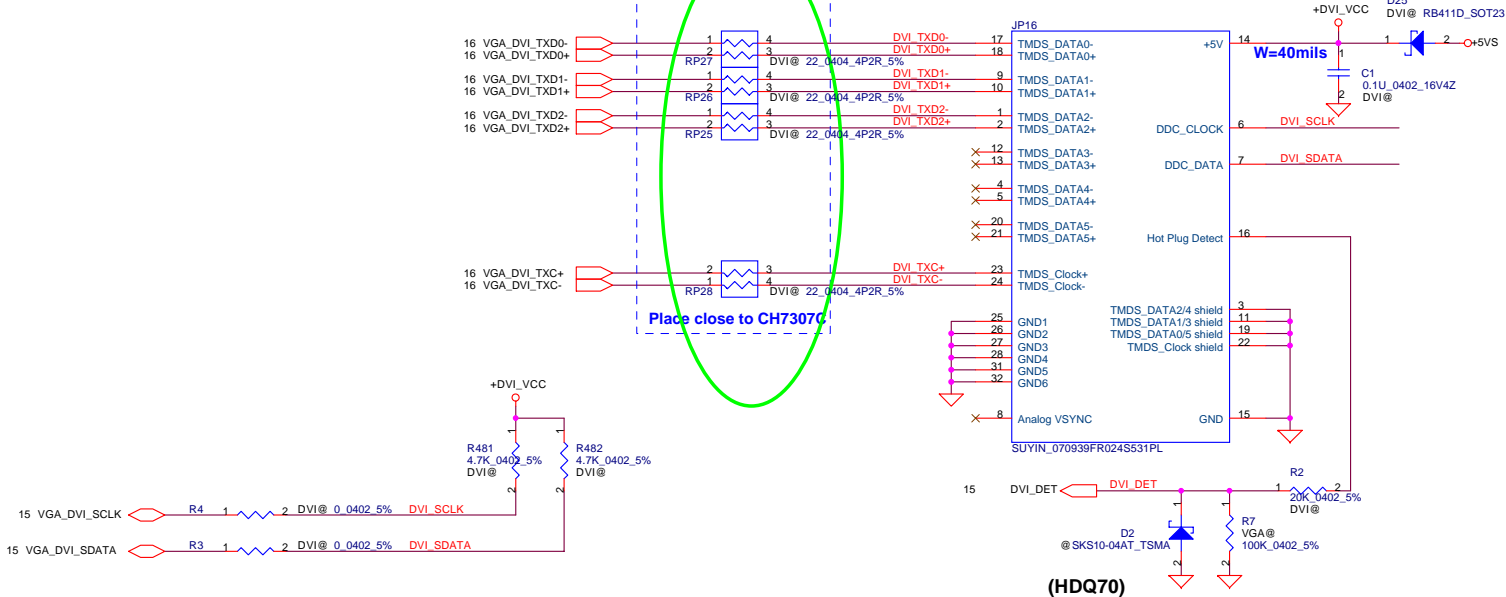
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BOM structure	DVI from SDVO	DVI from Discrete VGA
7307@	Stuff	No_Stuff
VGA@	No_Stuff	Stuff
@	No_Stuff	No_Stuff



DVI-D Connector

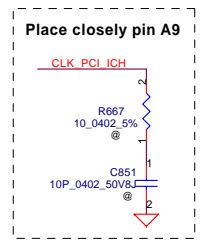
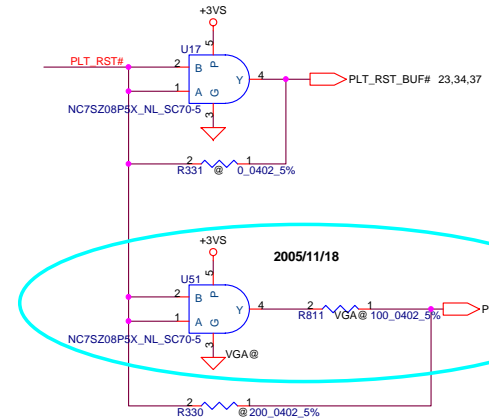
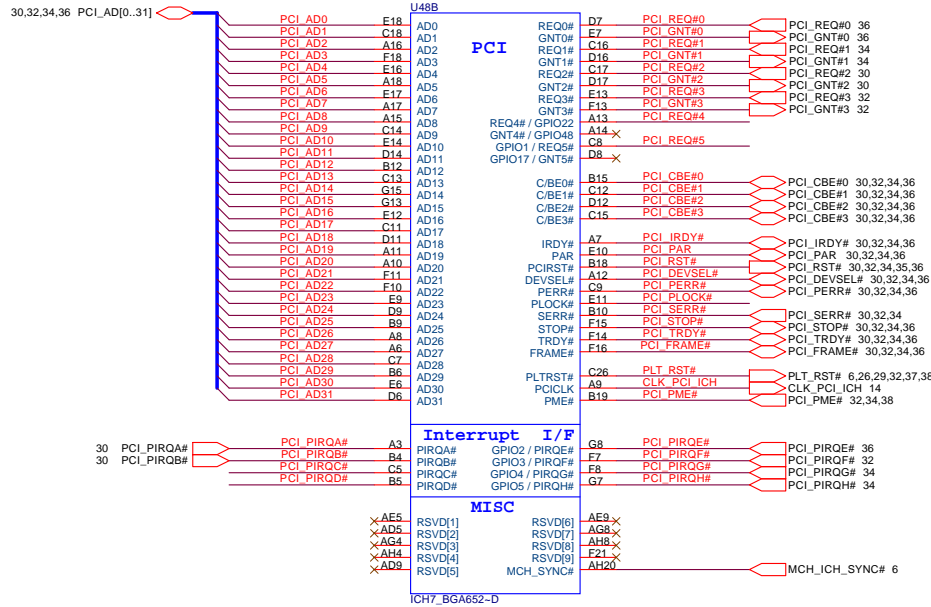
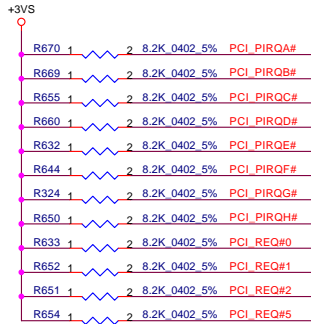
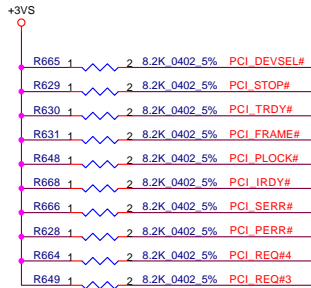


(HDQ70)

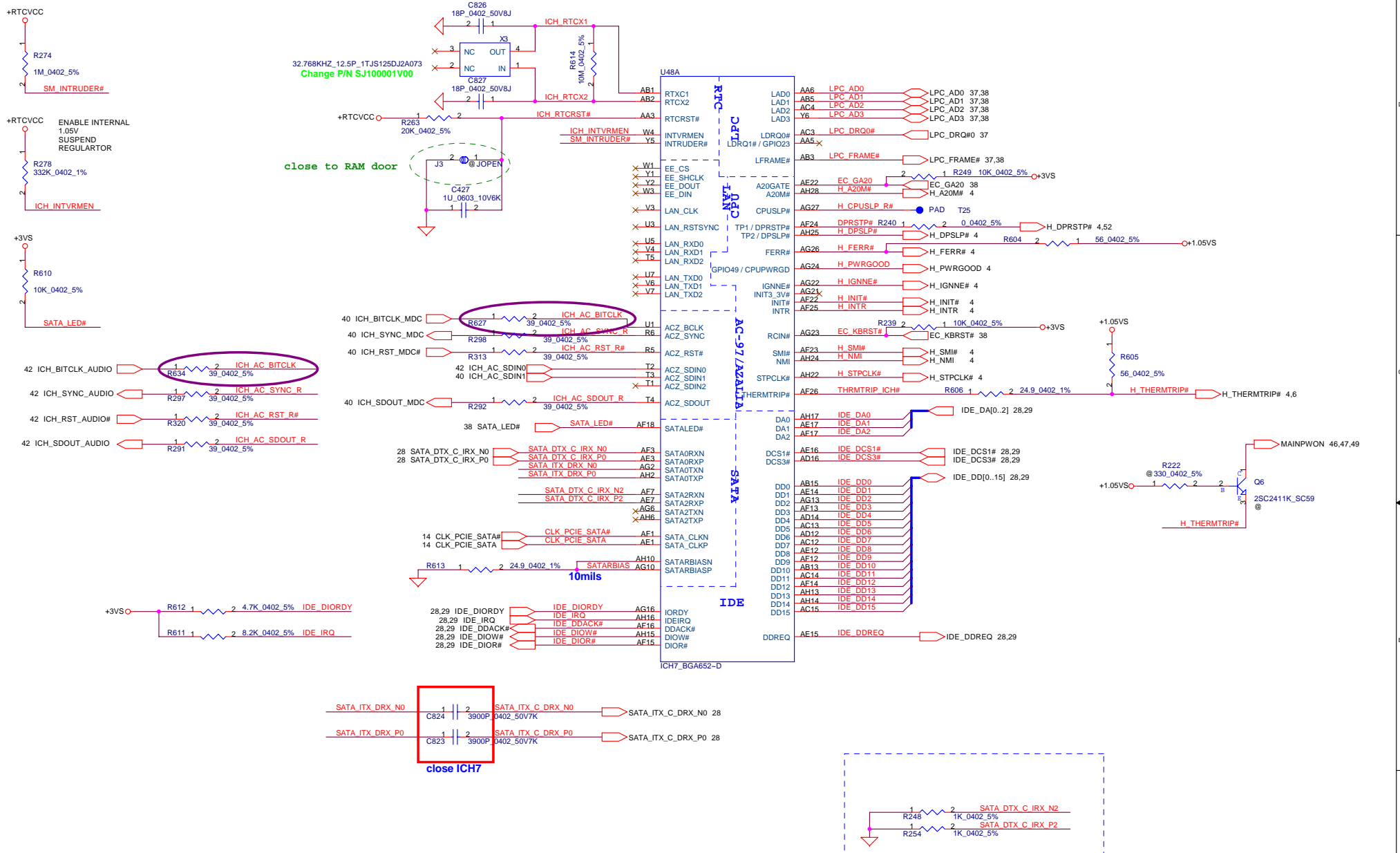
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ICH7M(SL8YB) [B-0]:SA00000V190 (ABO!)



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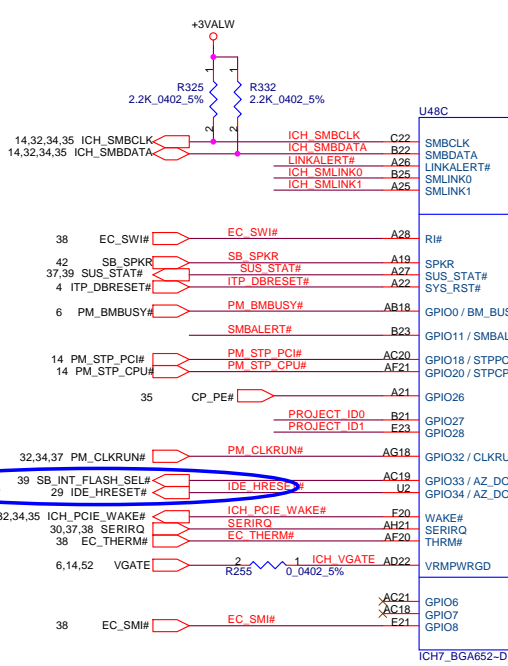
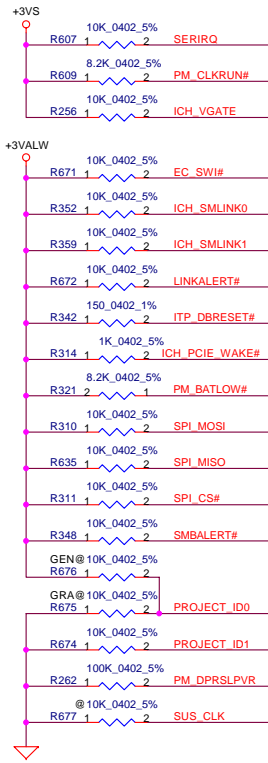
close to RAM door

close ICH7

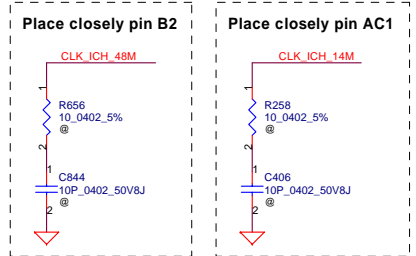
SATA_RXn/p need tie to ground when SATA port no used

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				Date: 日期四, 九月 14, 2006 Sheet 25 of 55	

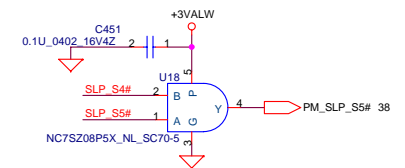
SCHEMATIC, M/B LA-2922P
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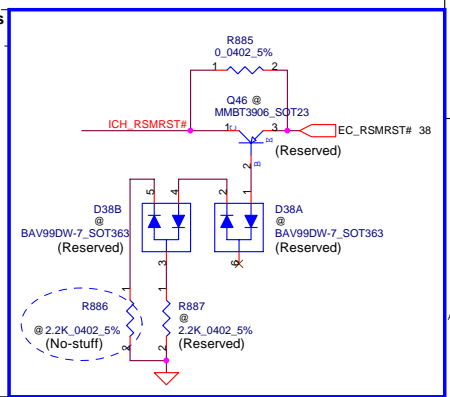
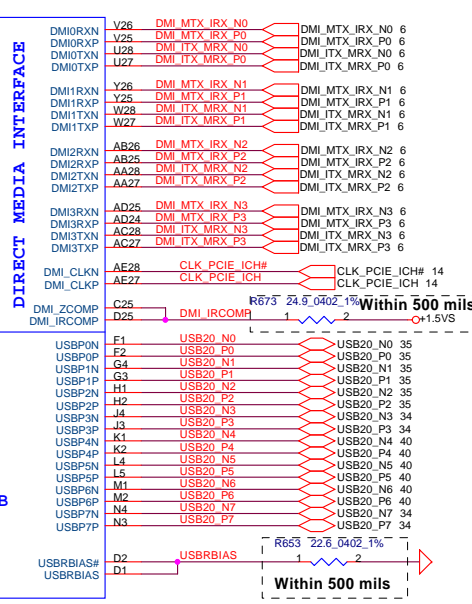
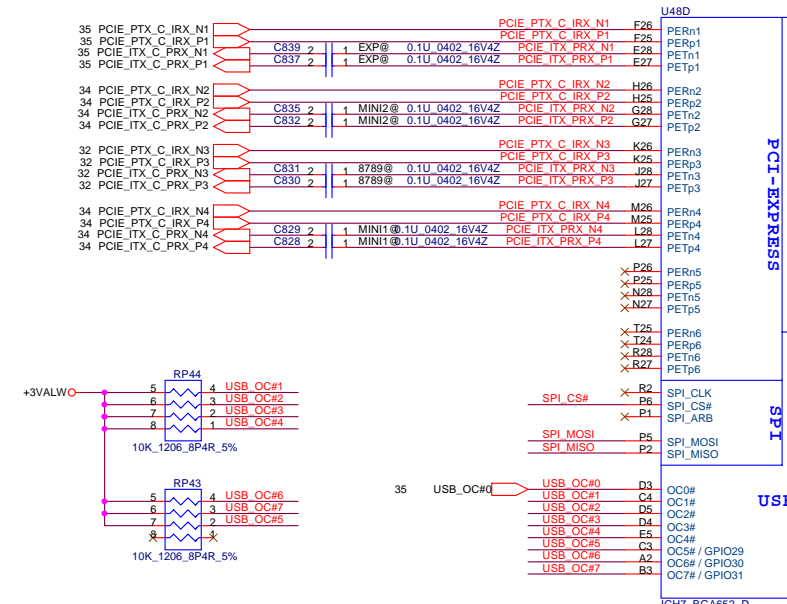
Need update symbol

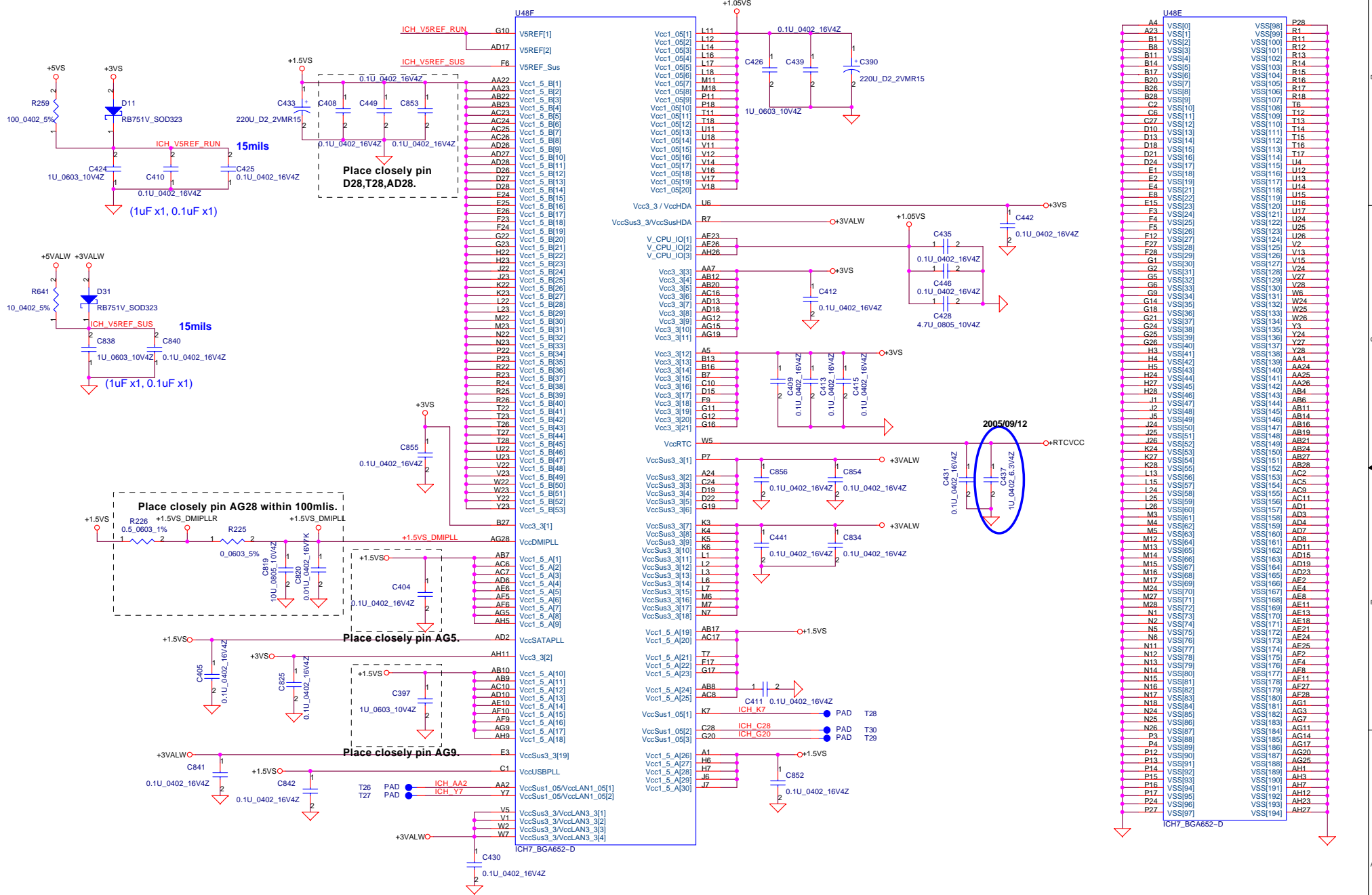


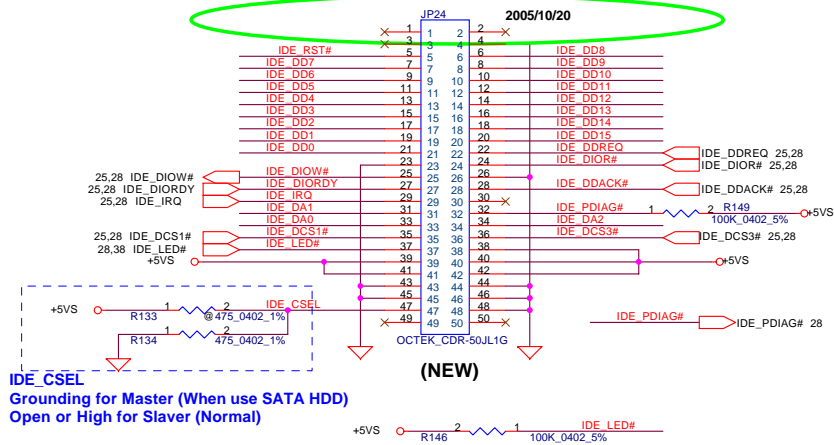
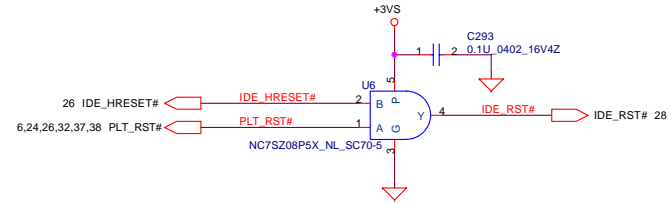
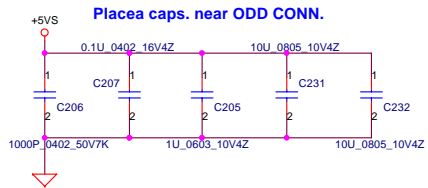
PM_DPRSPLVPR : Need to series a 500Ohm resistor to IMVP6



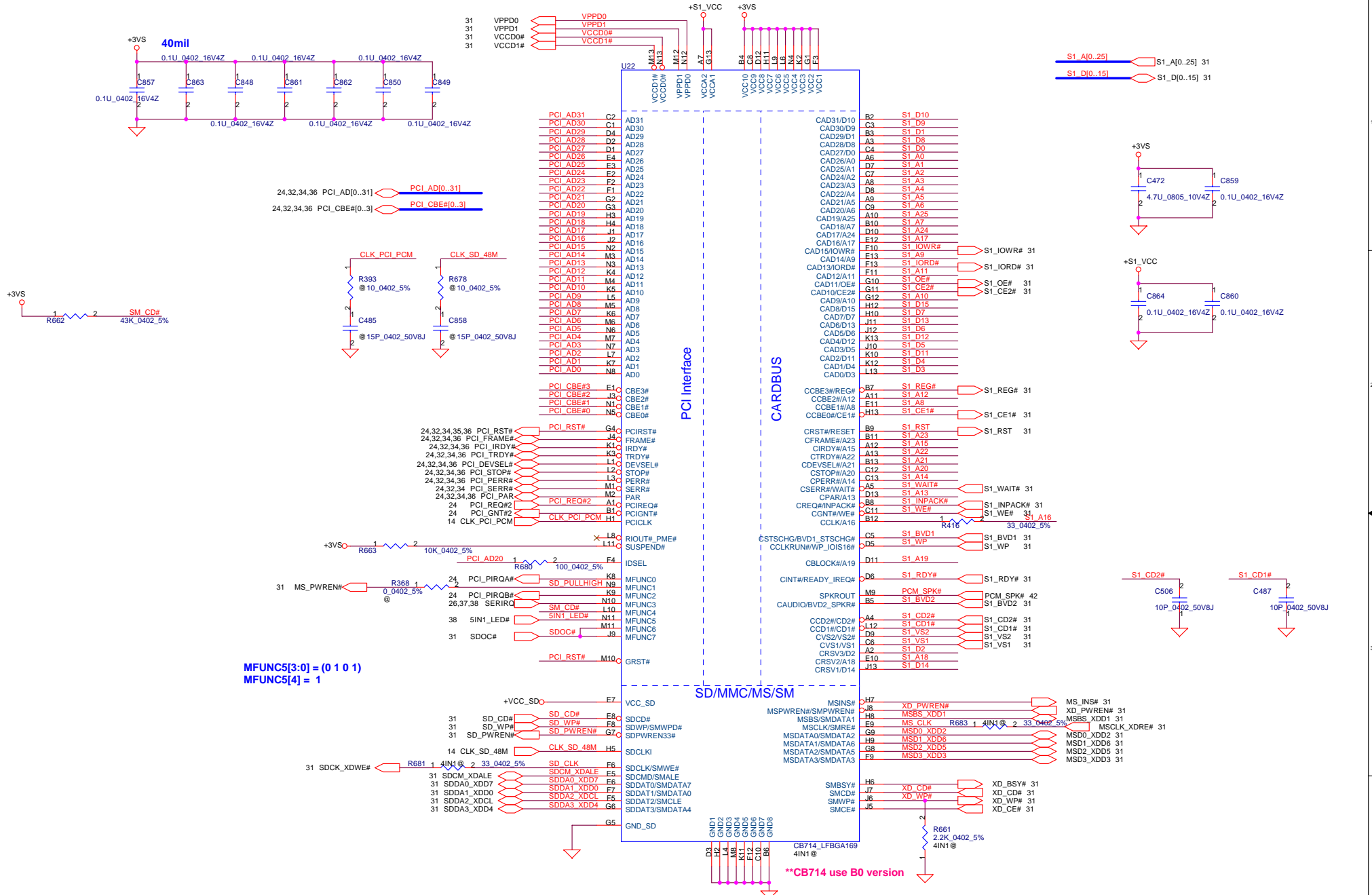
PROJECT_ID[0:1]	
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01	= Geneva







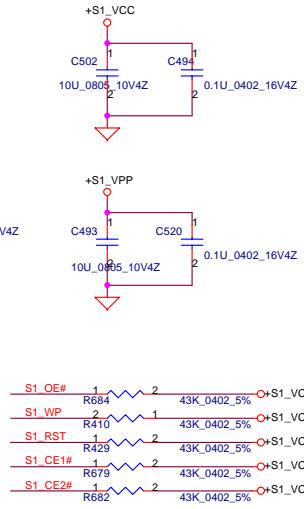
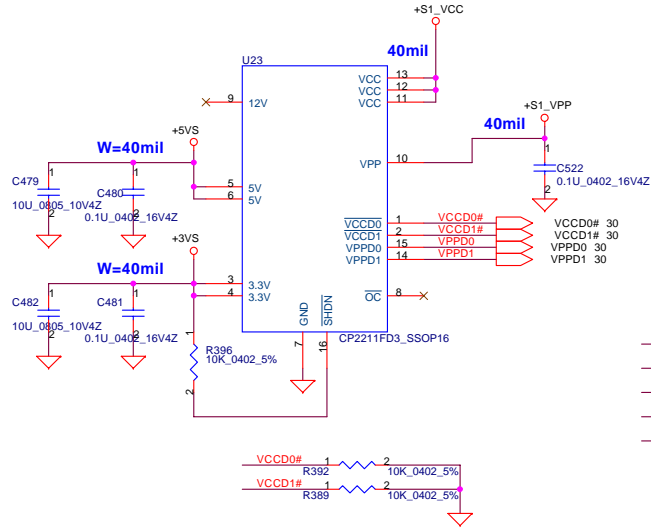
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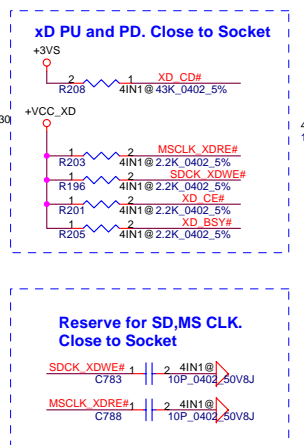
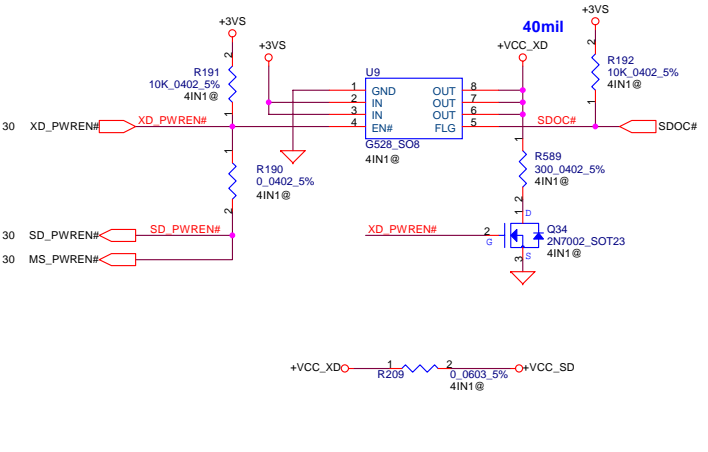
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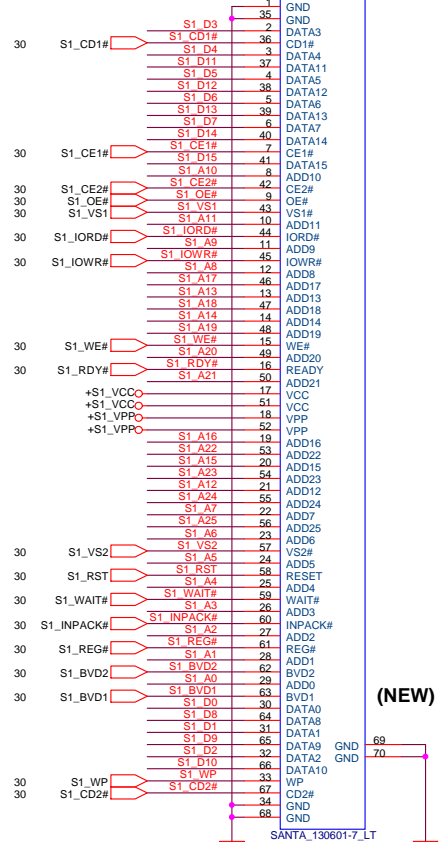
PCMCIA Power Control



SD/MS Power Control XD Power Control

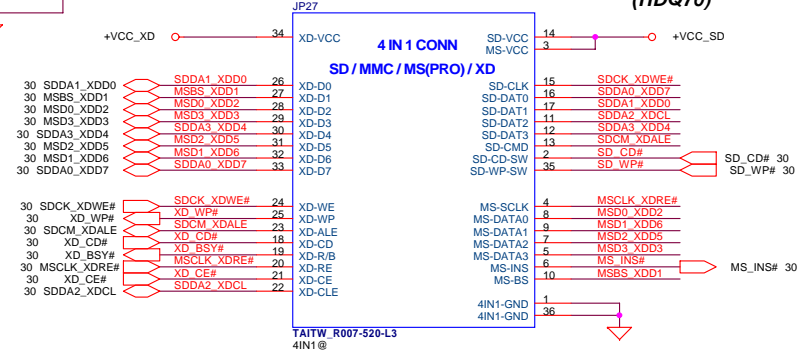


PCMCIA Socket

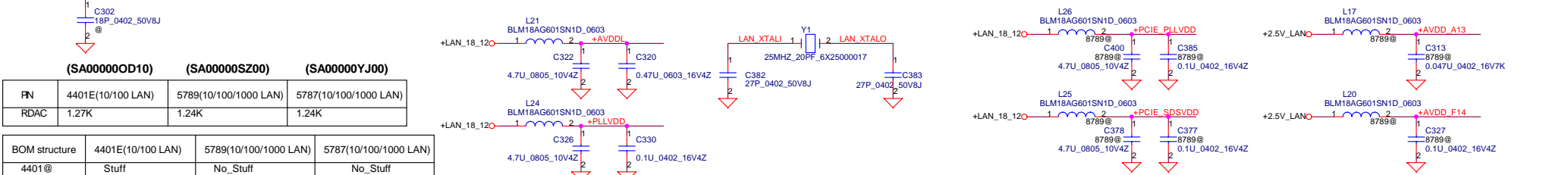
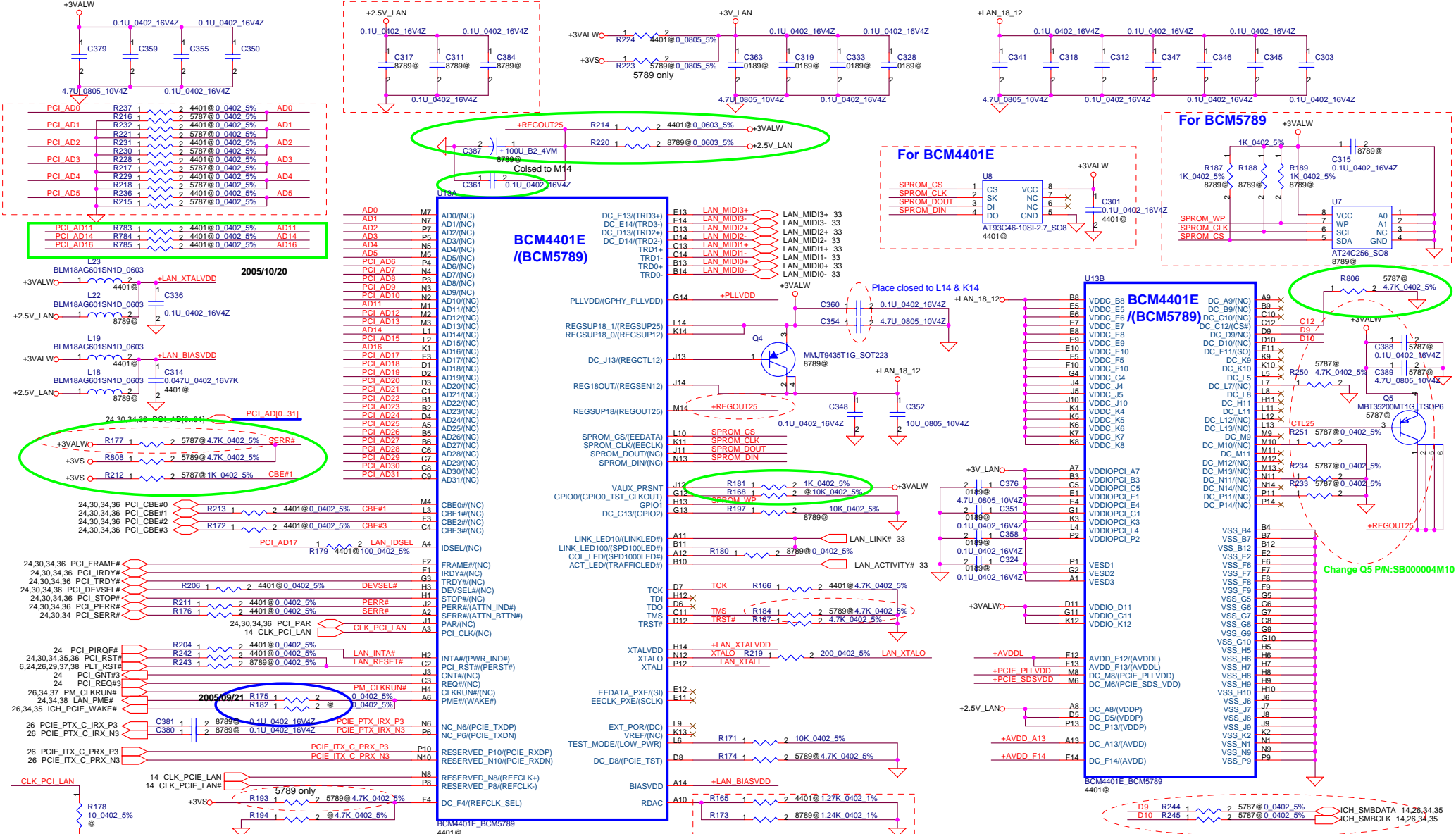


(NEW)

4 IN 1 Socket (HDQ70)



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	(SA00000D10)	(SA00000SZ00)	(SA00000YJ00)
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RDAC	1.27K	1.24K	1.24K

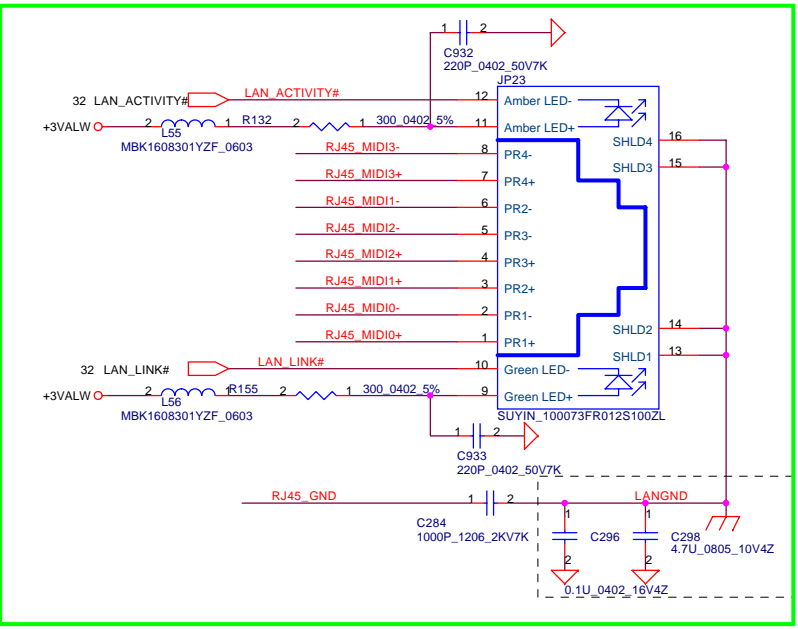
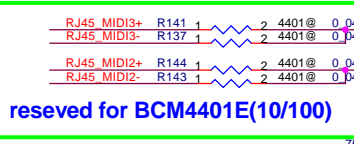
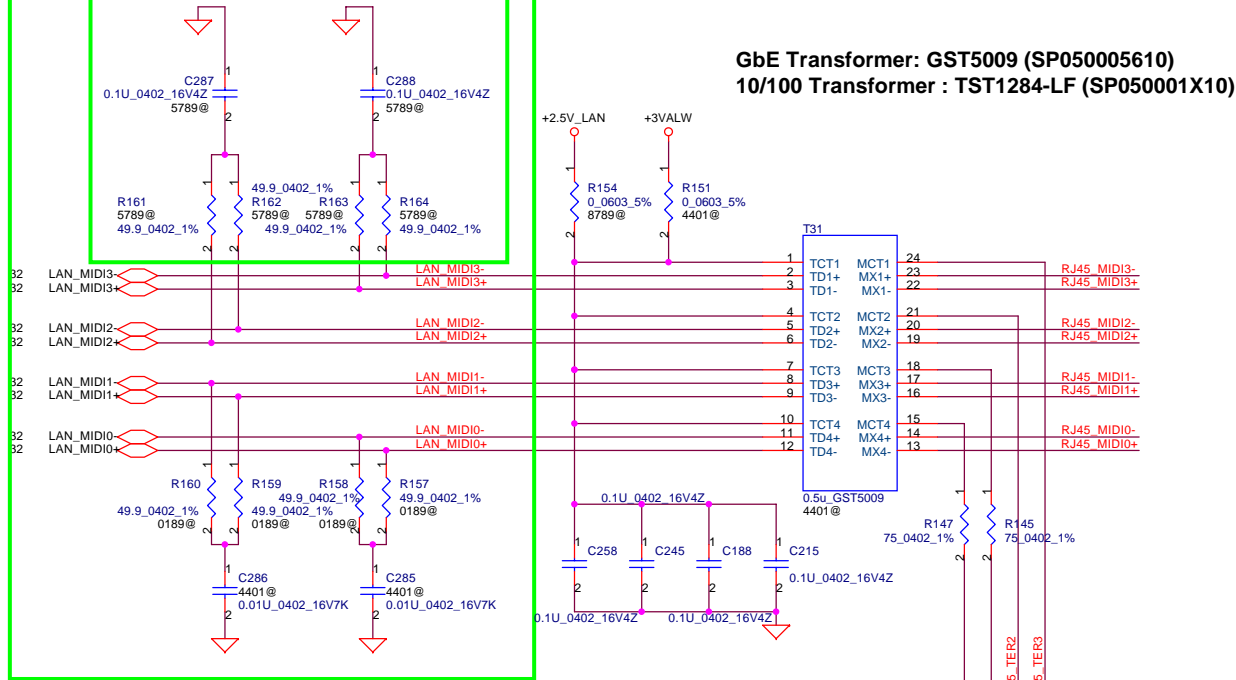
BOM structure	4401E(10/100 LAN)	5789(10/100/1000 LAN)	5787(10/100/1000 LAN)
4401@	Stuff	No_Stuff	No_Stuff
5789@	No_Stuff	Stuff	No_Stuff
5787@	No_Stuff	No_Stuff	Stuff
8789@	No_Stuff	Stuff	Stuff
@	No_Stuff	No_Stuff	No_Stuff

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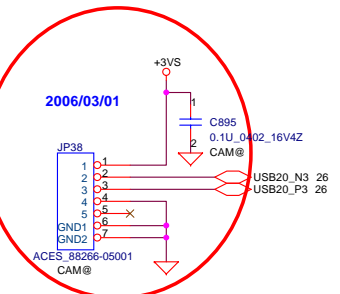
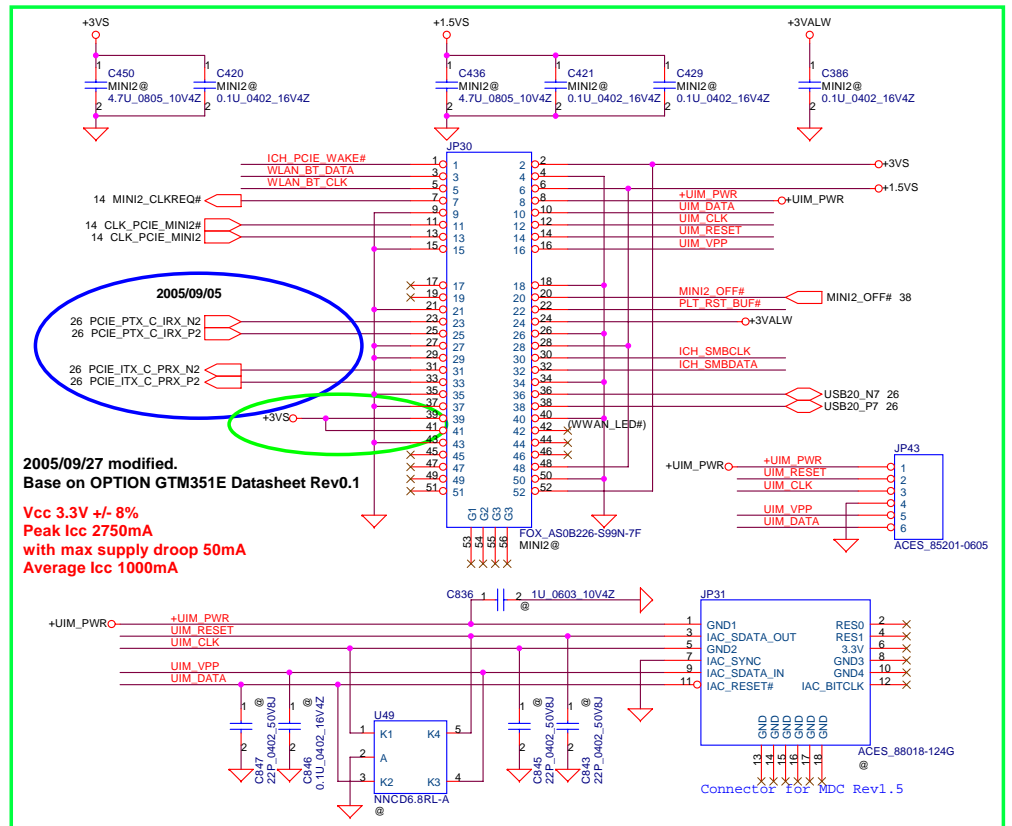
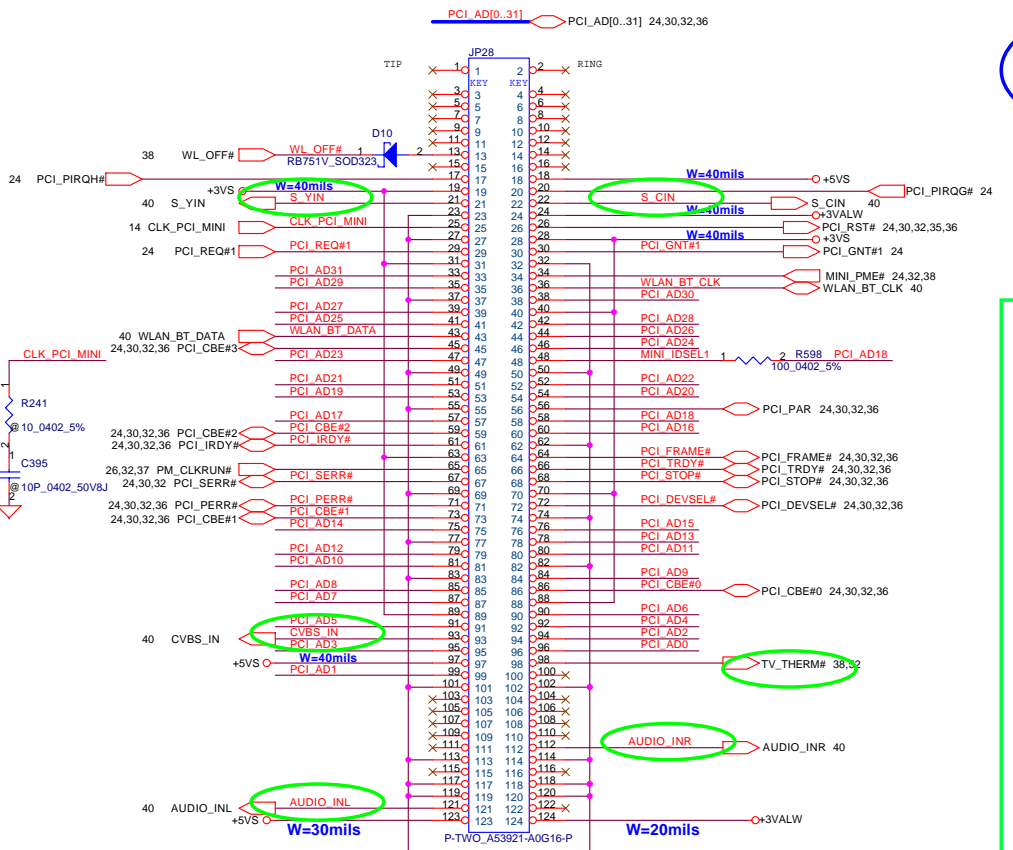
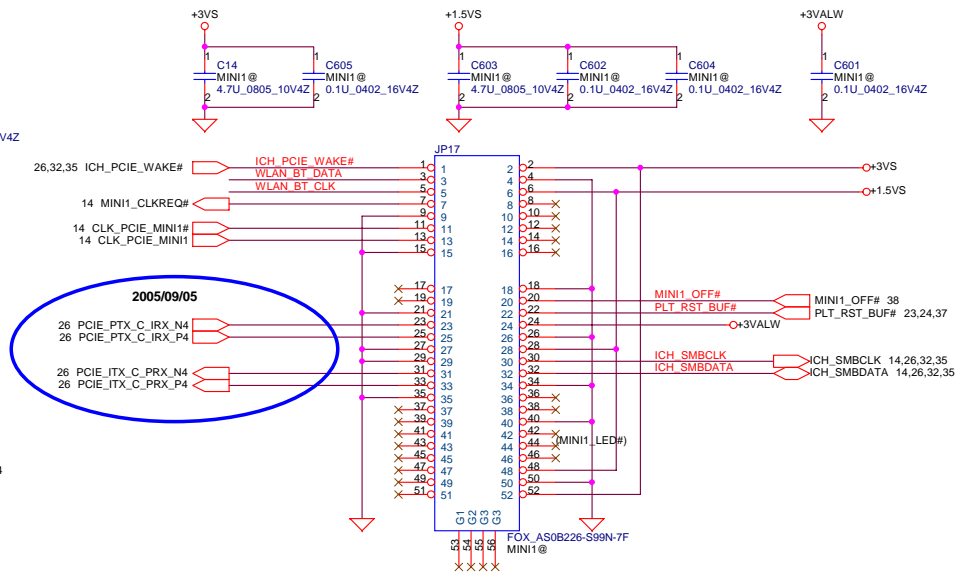
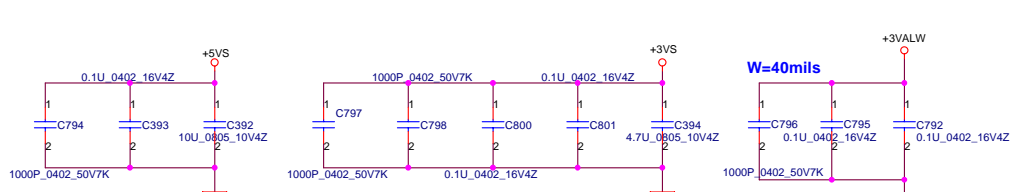
LAN BCM4401E/ BCM5789

Place these components colsed to LAN chip

unpop when use BCM4401E(10/100)



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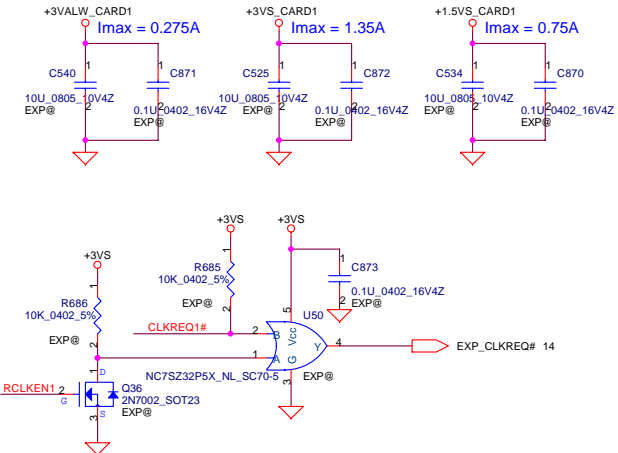
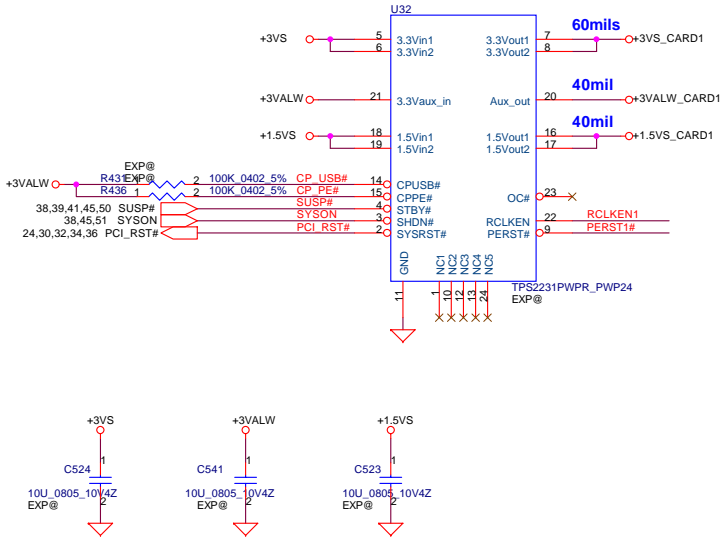


Mini Card Power Rating

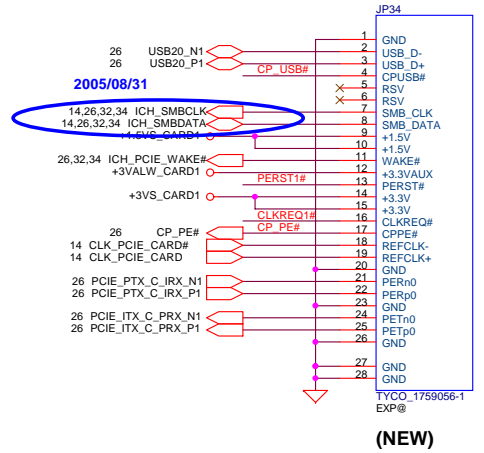
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

2005/09/27 modified.
 Base on OPTION GTM351E Datasheet Rev0.1
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

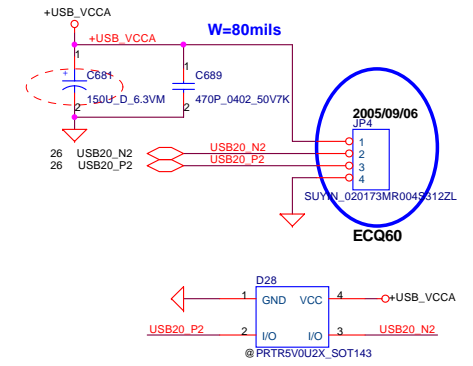
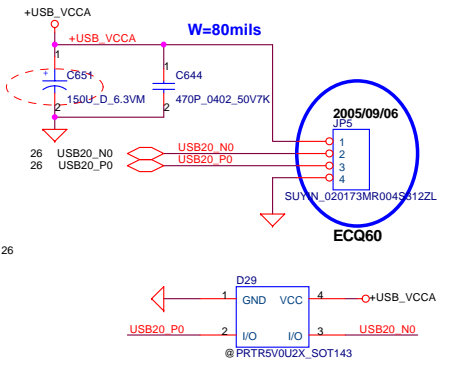
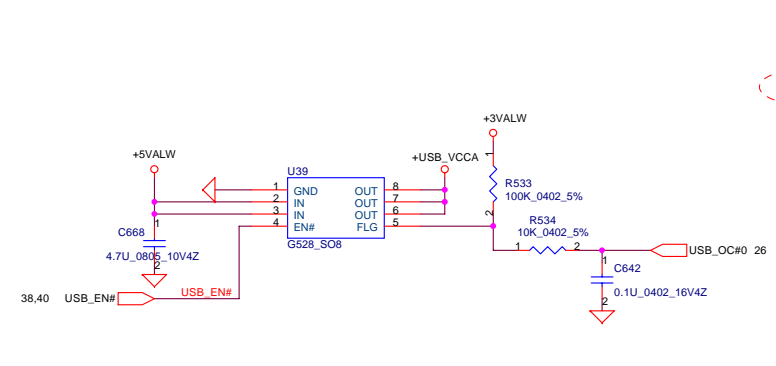
New Card Power Switch



New Card Socket (Left)

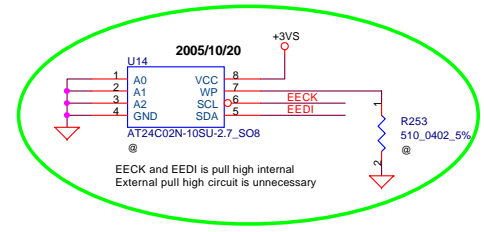
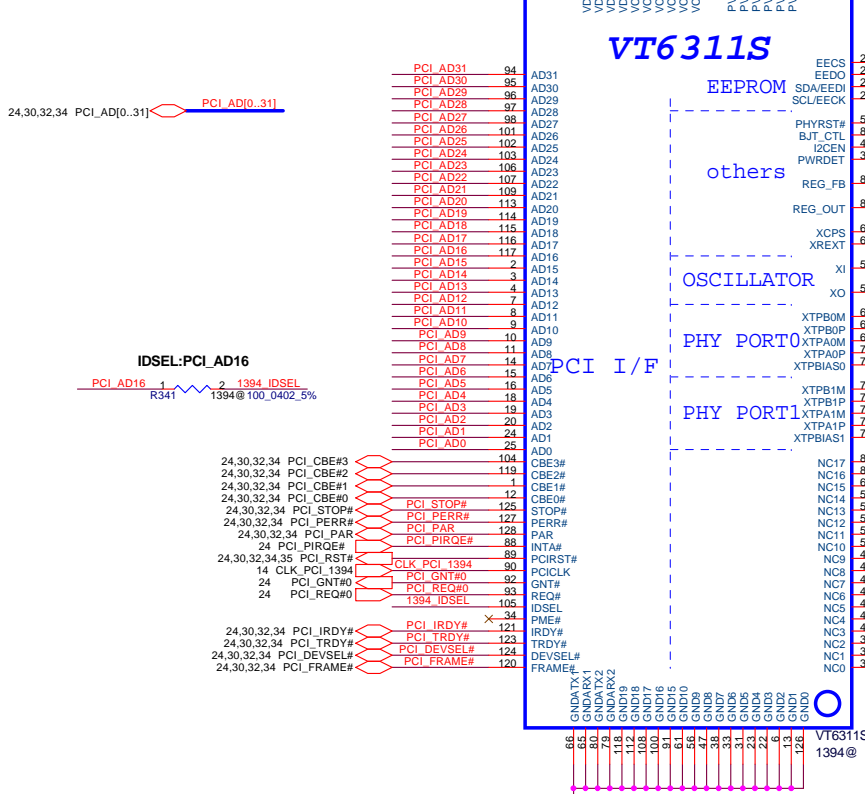
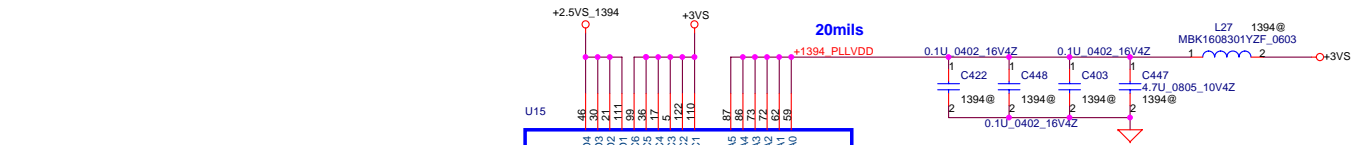
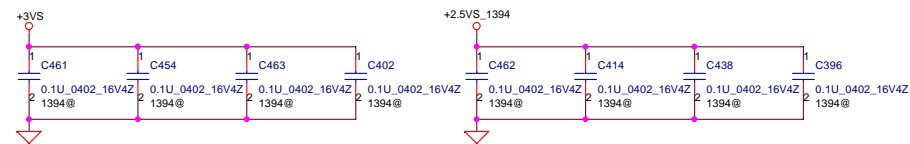


USB CONN. 1 & 2

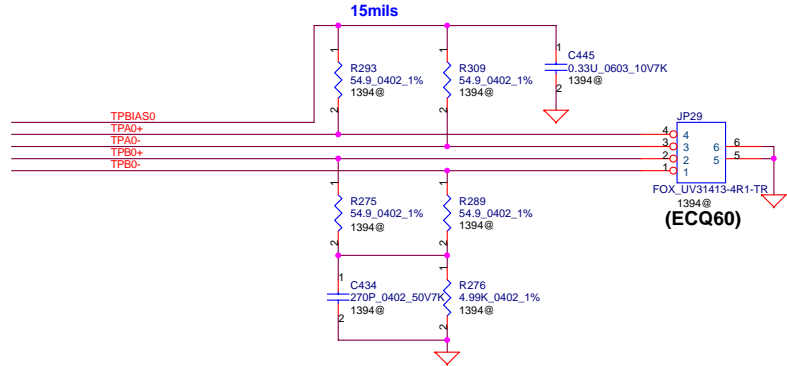
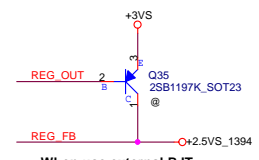


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Compal Electronics, Inc.		
Title SCHEMATIC, M/B LA-2922P		
Size B	Document Number 401454	Rev A
Date:	星期四, 九月 14, 2006	Sheet 35 of 55

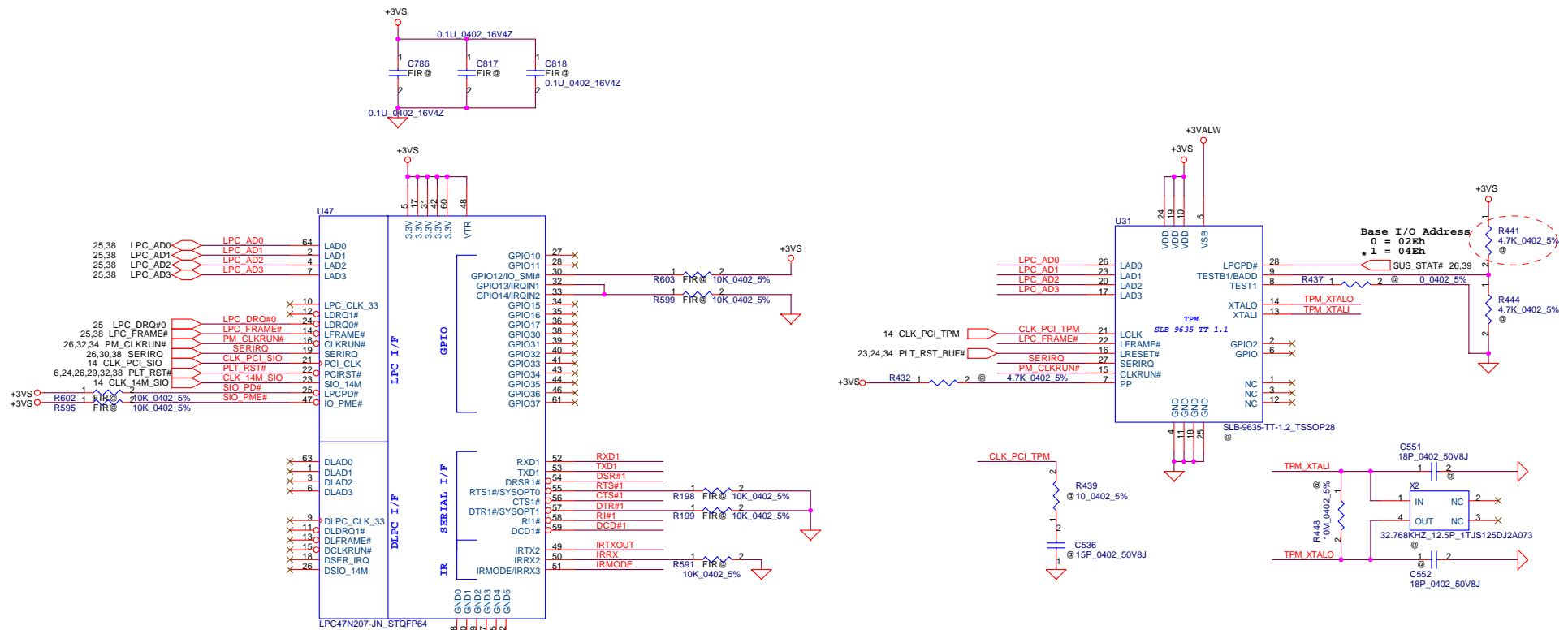


When use external EEPROM
Populate U14, R246, R253
Un-populate R261

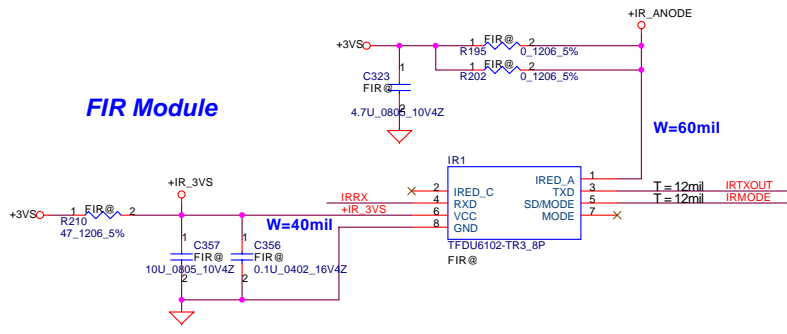


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SHEMATIC, M/B LA-2922P Sheet 36 of 55			Rev A	

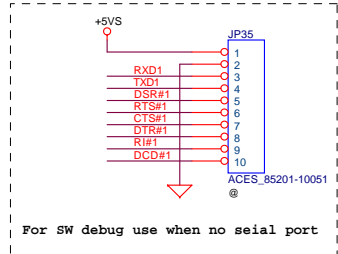
SUPER I/O SMsC LPC47N207



FIR Module

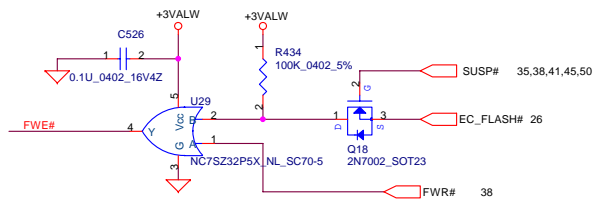


Place on the BOT side (near MINIPCI conn.)

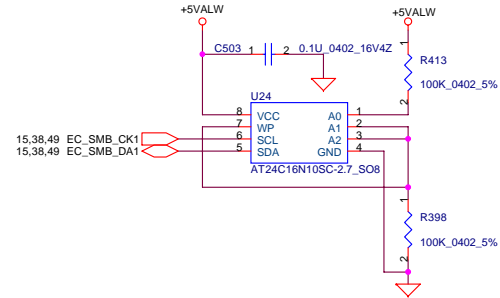


For SW debug use when no serial port

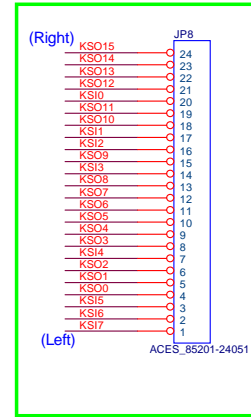
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Check PCB Footprint



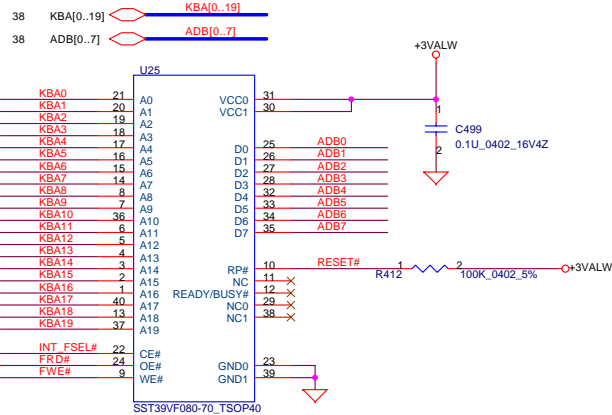
INT_KBD Conn.



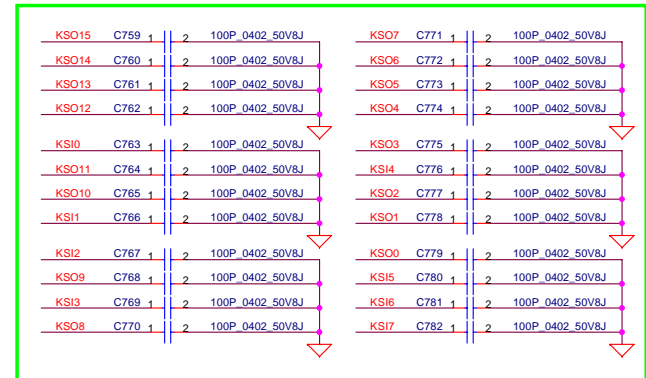
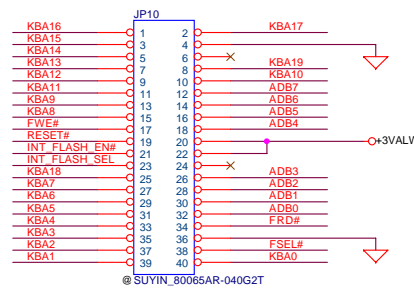
FOR DEBUG ONLY



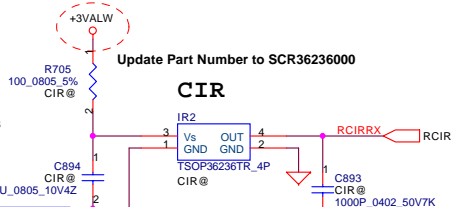
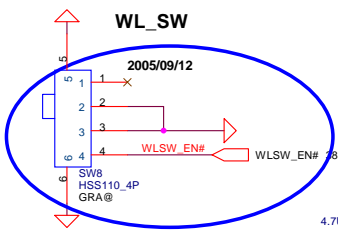
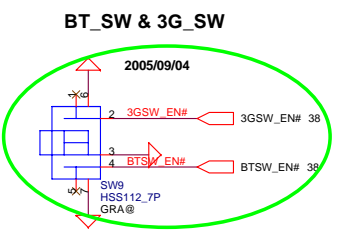
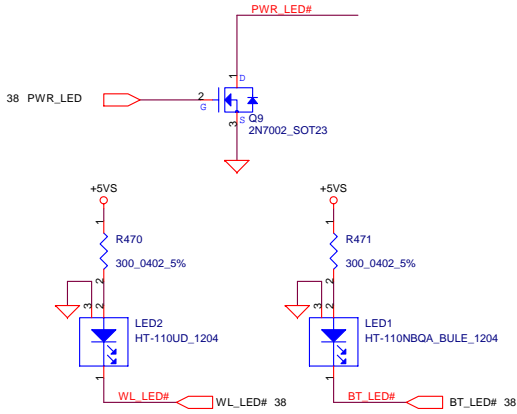
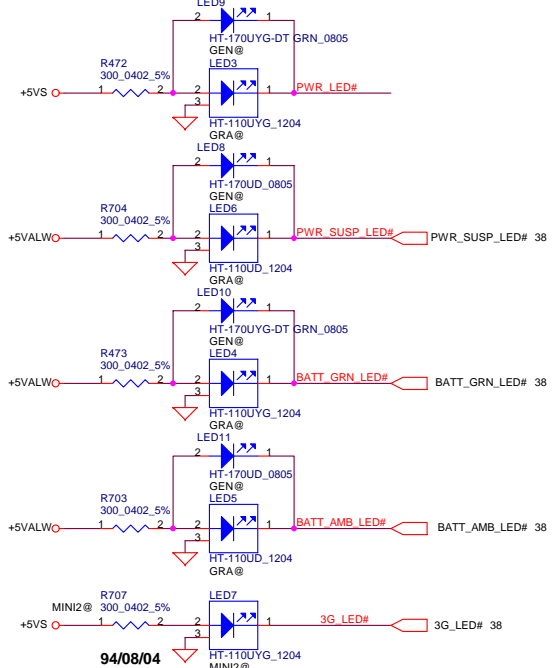
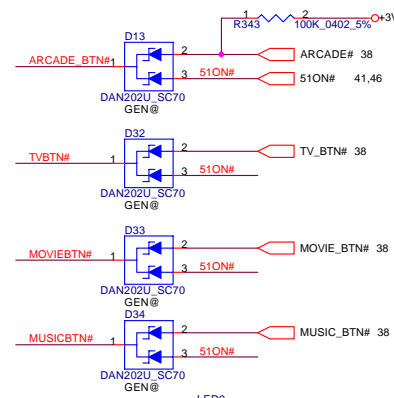
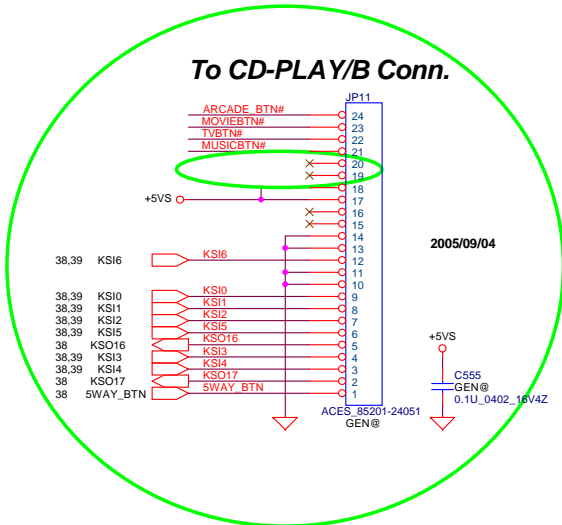
1MB Flash ROM



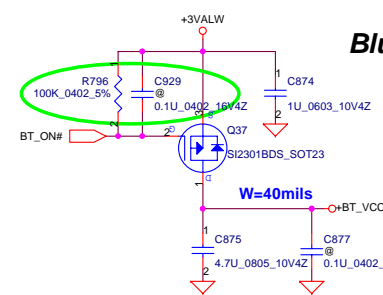
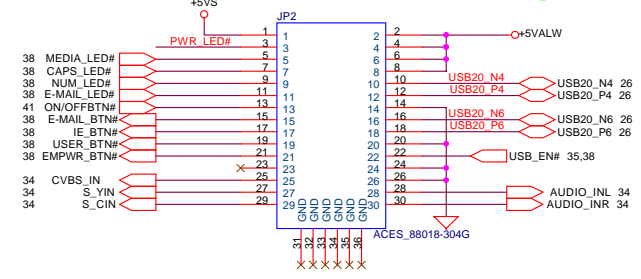
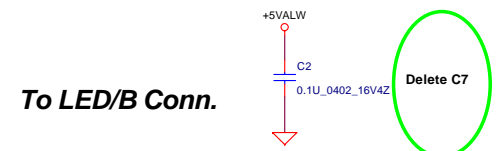
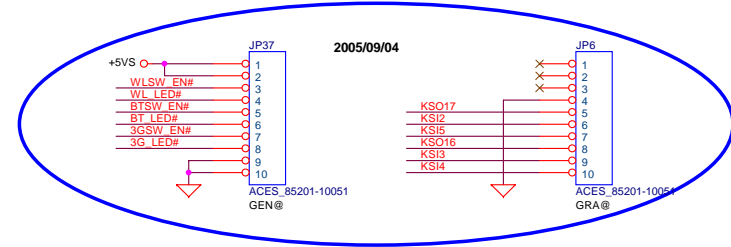
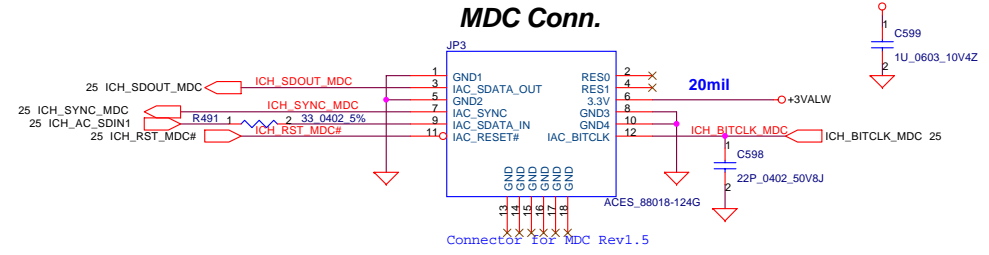
1MB ROM Socket



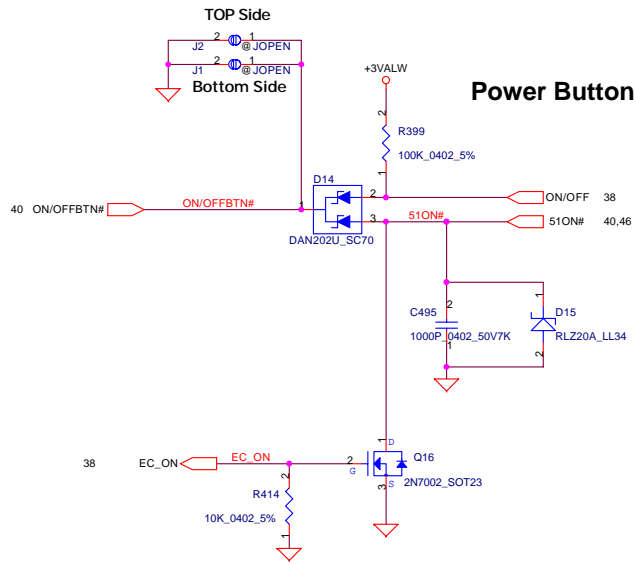
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Geneva		Grapevine	
KSO16	KSO17	KSO16	KSO17
KSIO VOL_UP	KSIO17 LEFT		
KSII RIGHT	KSII VOL_DOWN		
KSII PLAY	KSII ENTER	KSII PLAY	
KSII STOP		KSII STOP	VOL_UP
KSII NEXT		KSII NEXT	VOL_DOWN
KSII REV		KSII REV	ARCADE_TV
KSII6	KSII6 RECORD		

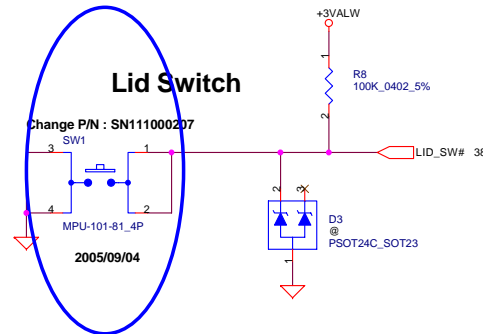
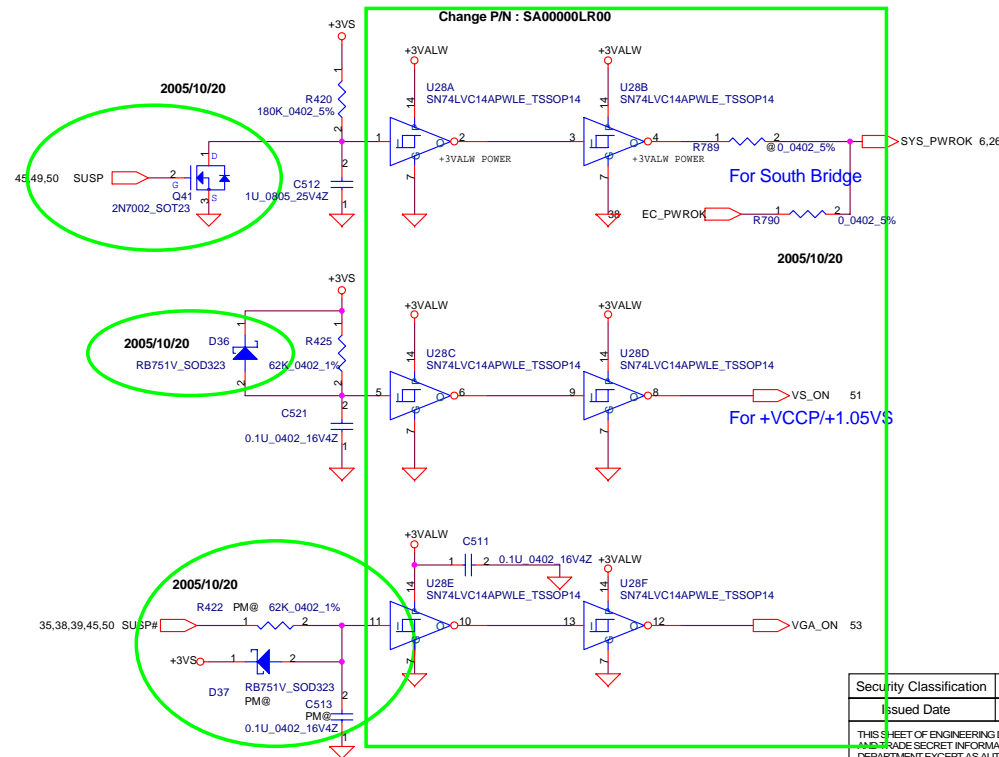


ON/OFF switch



Power Button

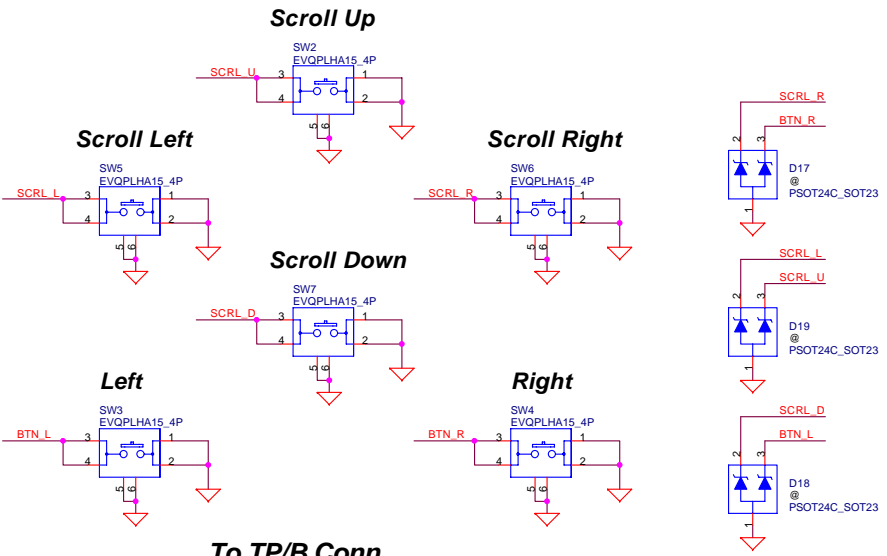
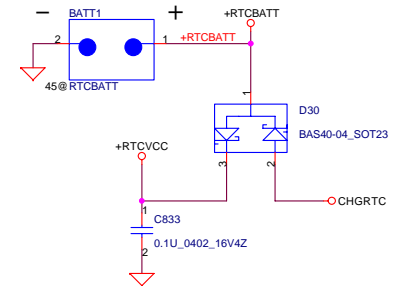
Power ON Circuit



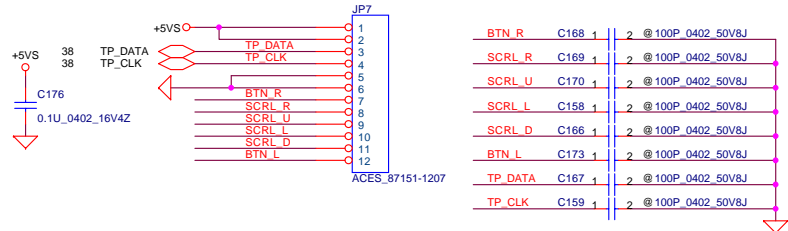
Lid Switch

Change BATT1 P/N : SP093PA0200 (Panasonic)
SP093MX0000 (MAXELL)

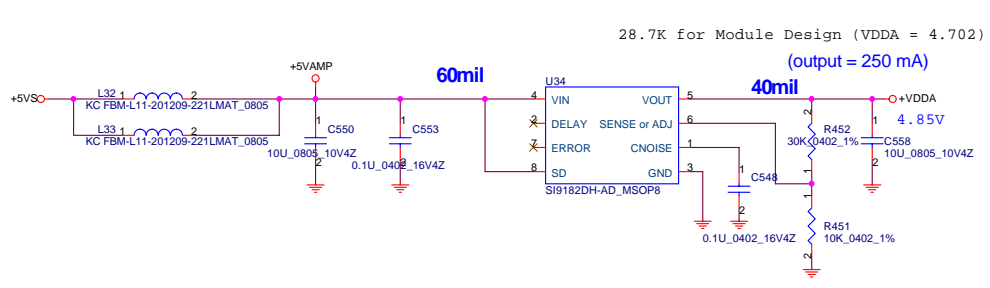
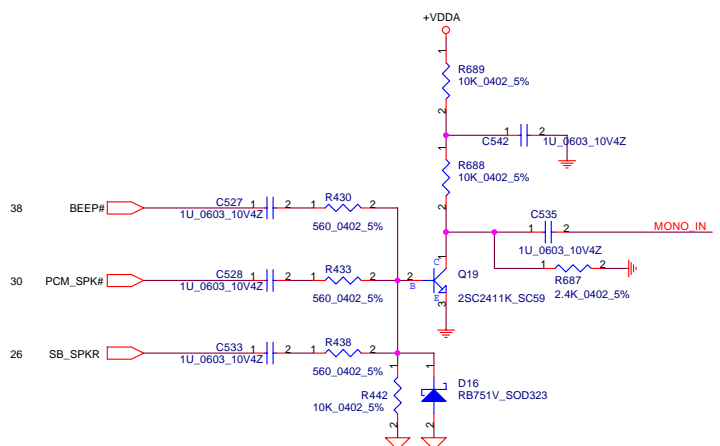
RTC Battery



To TP/B Conn.



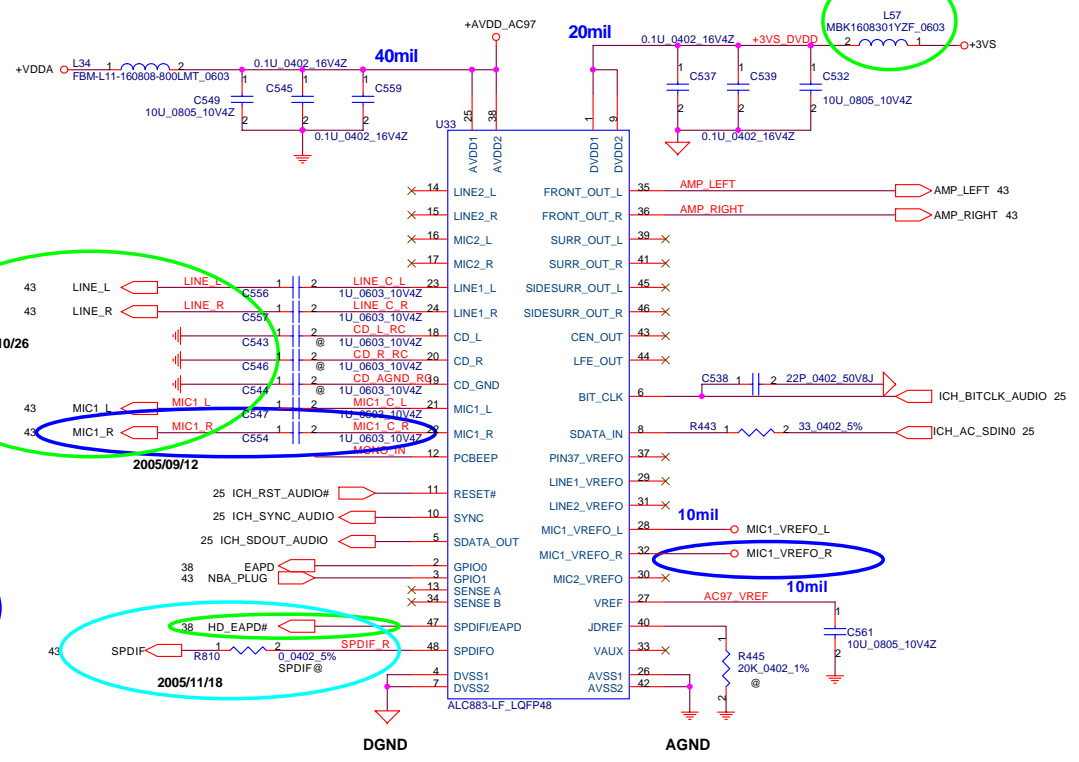
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28.7K for Module Design (VDDA = 4.702)

(output = 250 mA)

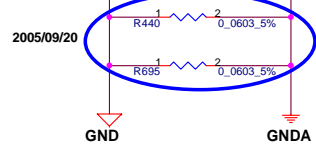
HD Audio Codec



2005/10/26

2005/09/12

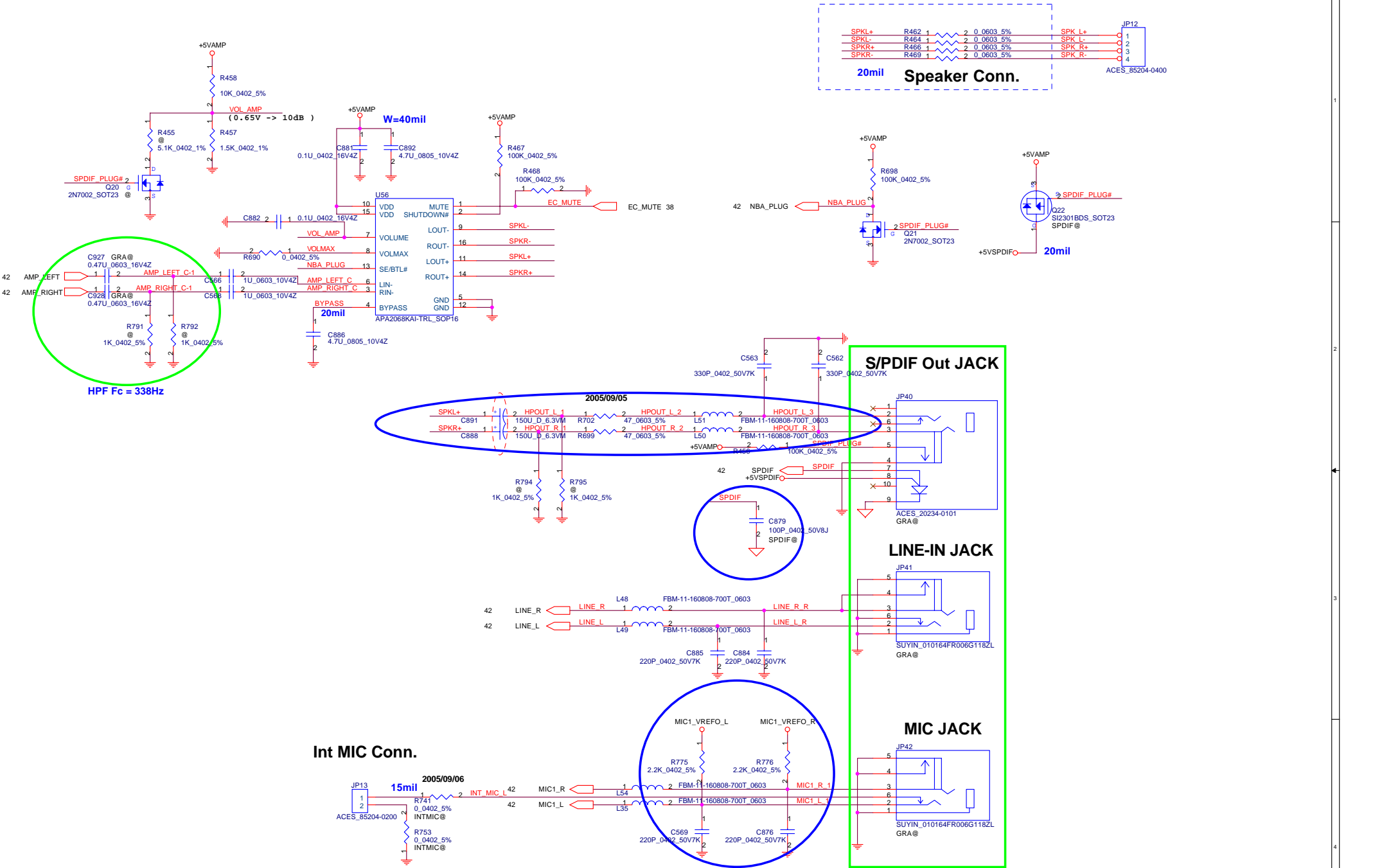
2005/11/18



DGND

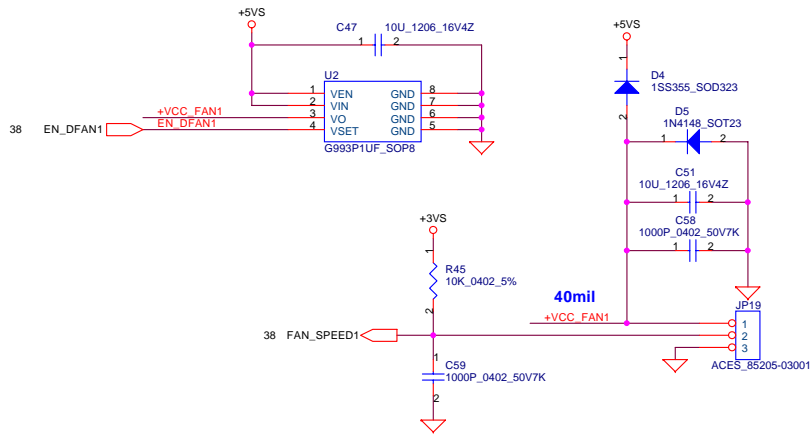
AGND

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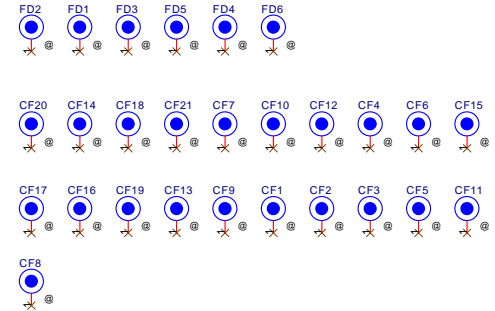
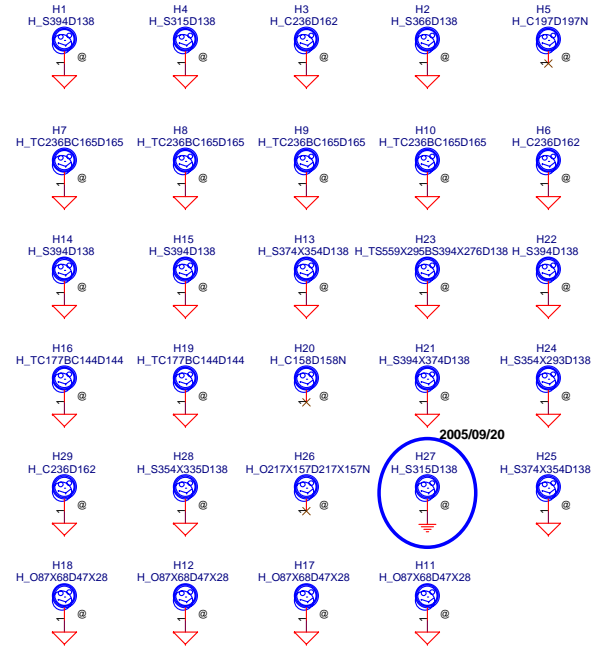
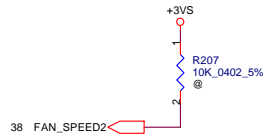


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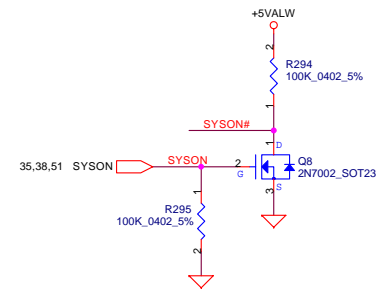
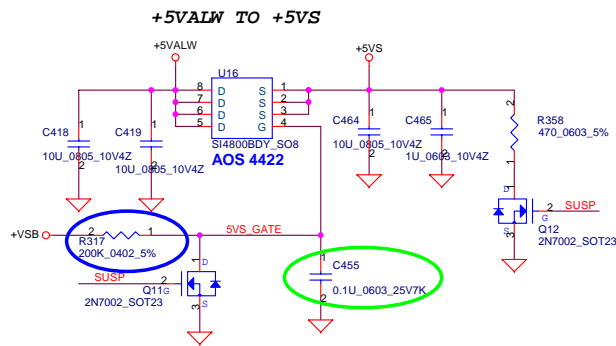
FAN1 Conn



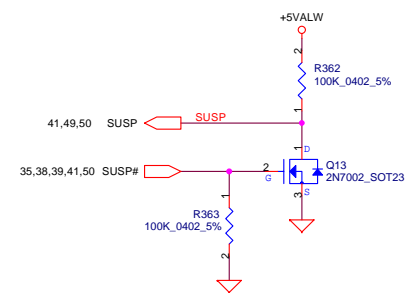
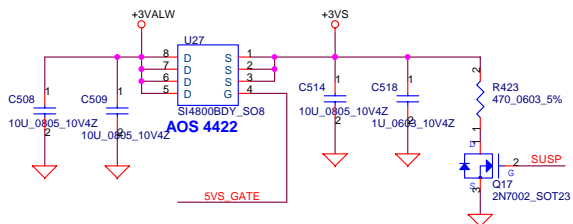
FAN2 Conn 2005/12/29: Remove 2nd FAN support components



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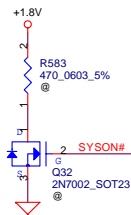
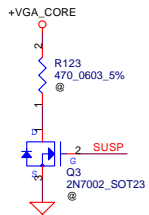
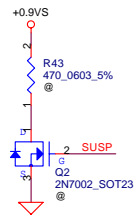
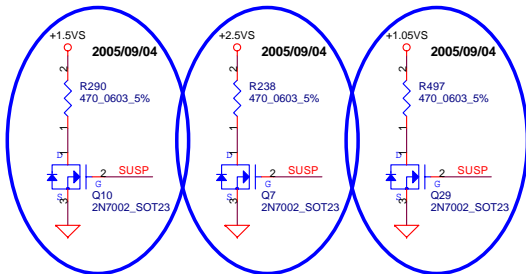
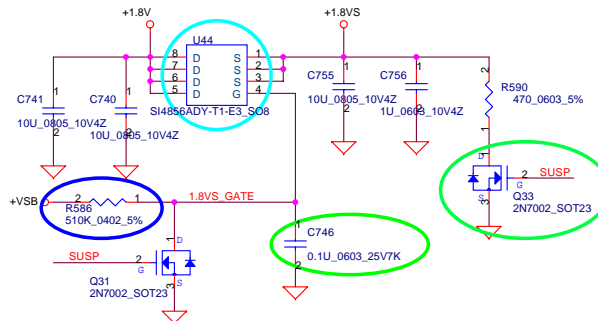


+3VALW TO +3VS

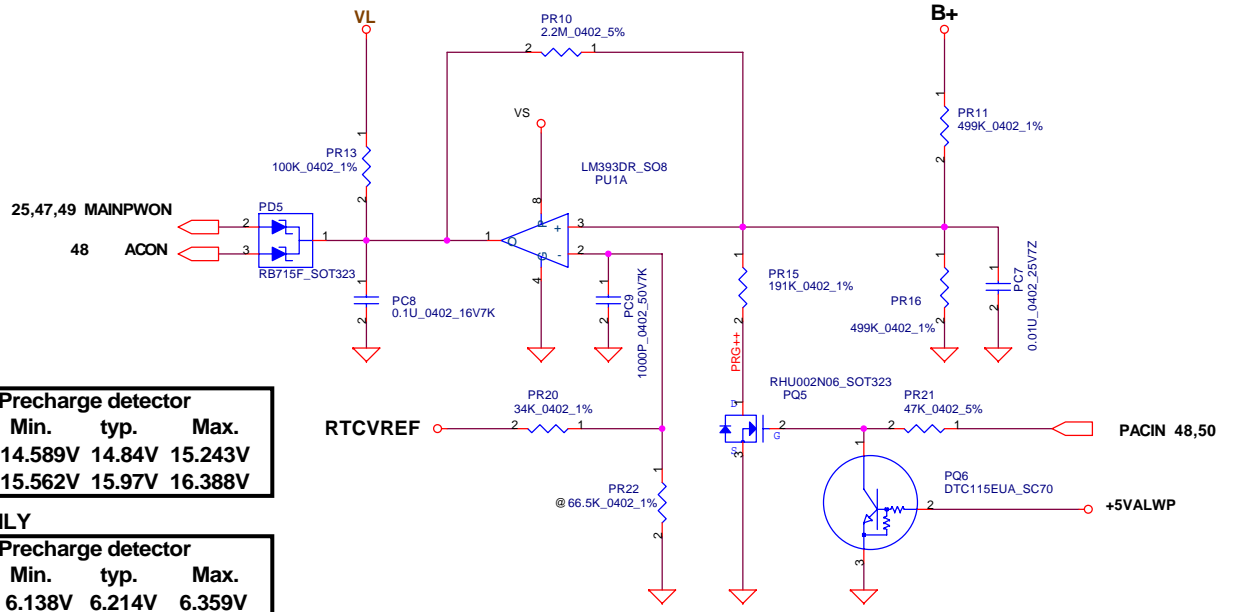
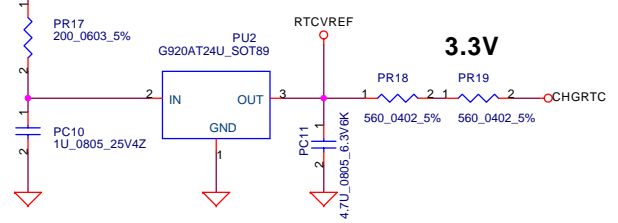
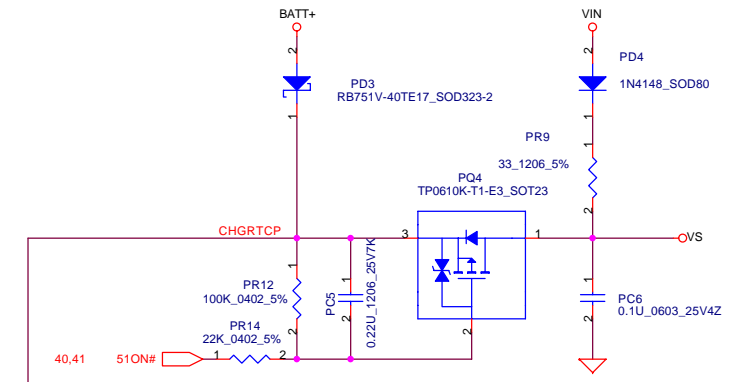
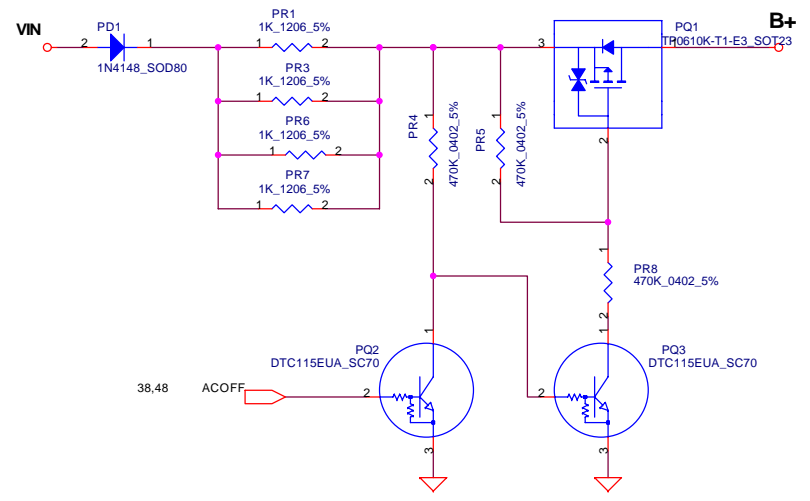
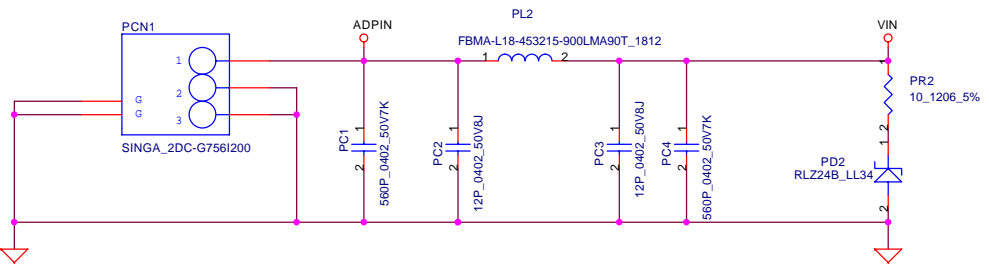


2005/12/18
Change P/N : SB000001Y00(New) SI4856ADY
SB54800310(Old)

+1.8V to +1.8VS



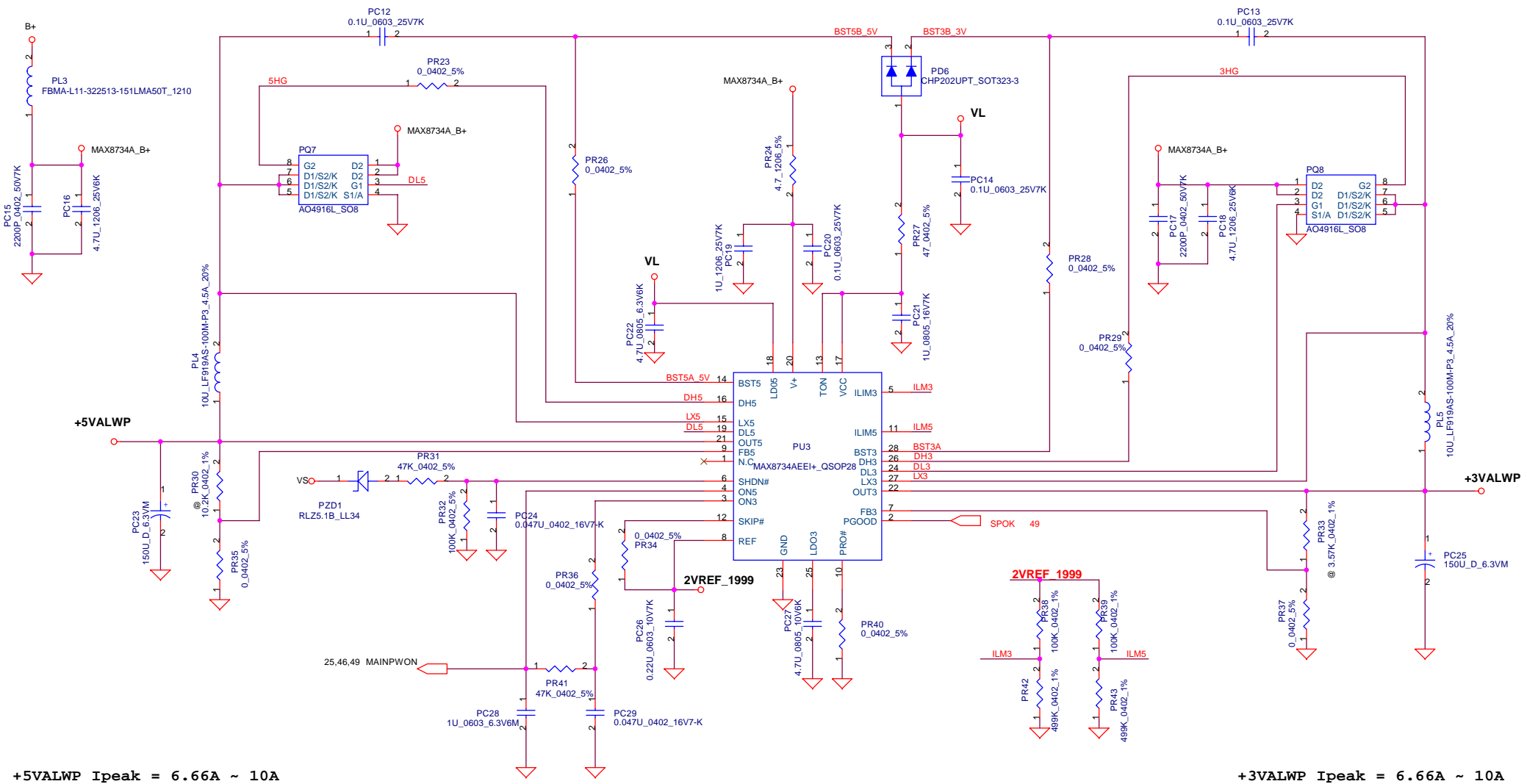
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ACIN			
Precharge detector			
	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

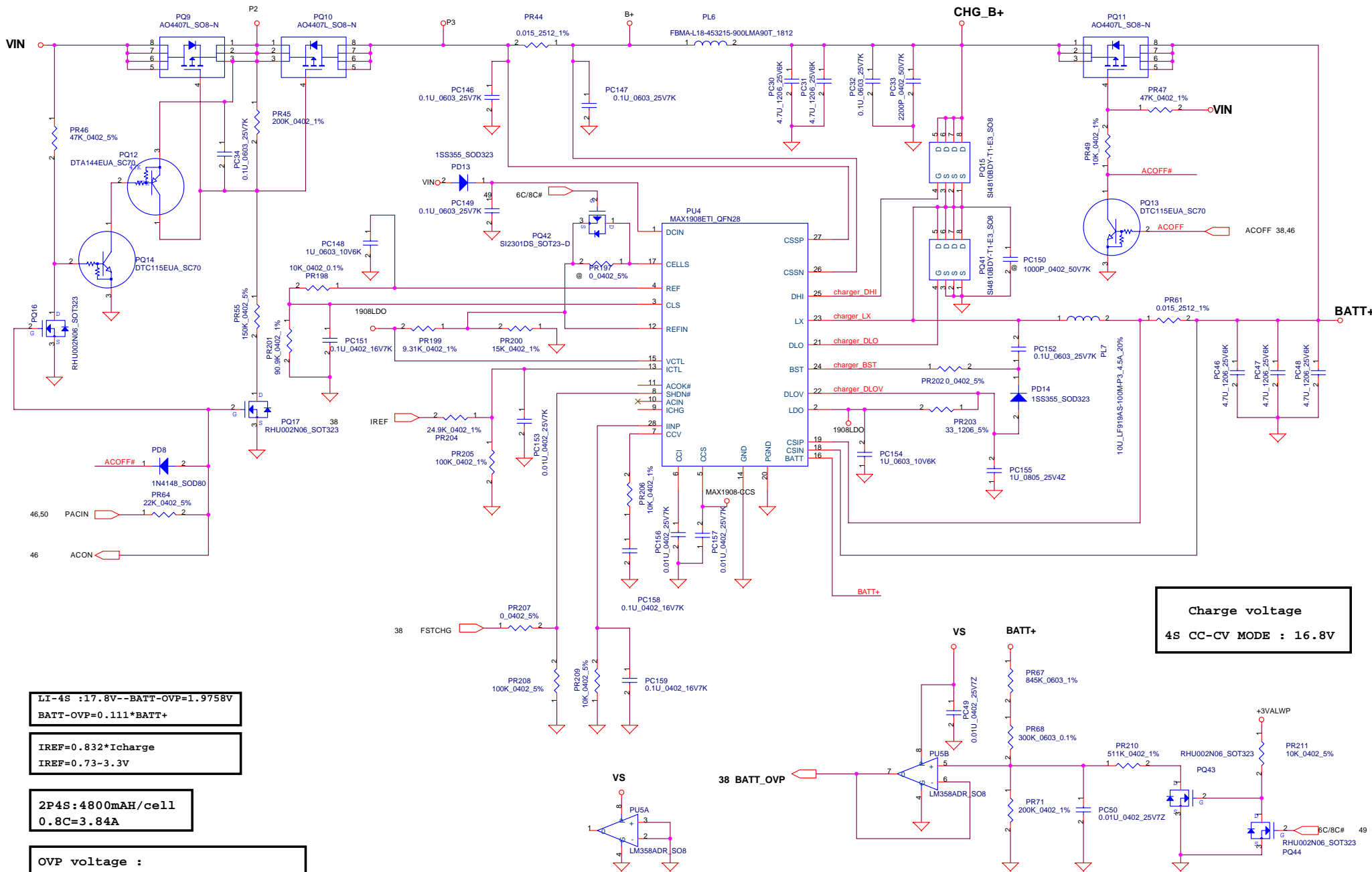
BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V

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I_{adp}=0~4.74A(90W)



Charge voltage
4S CC-CV MODE : 16.8V

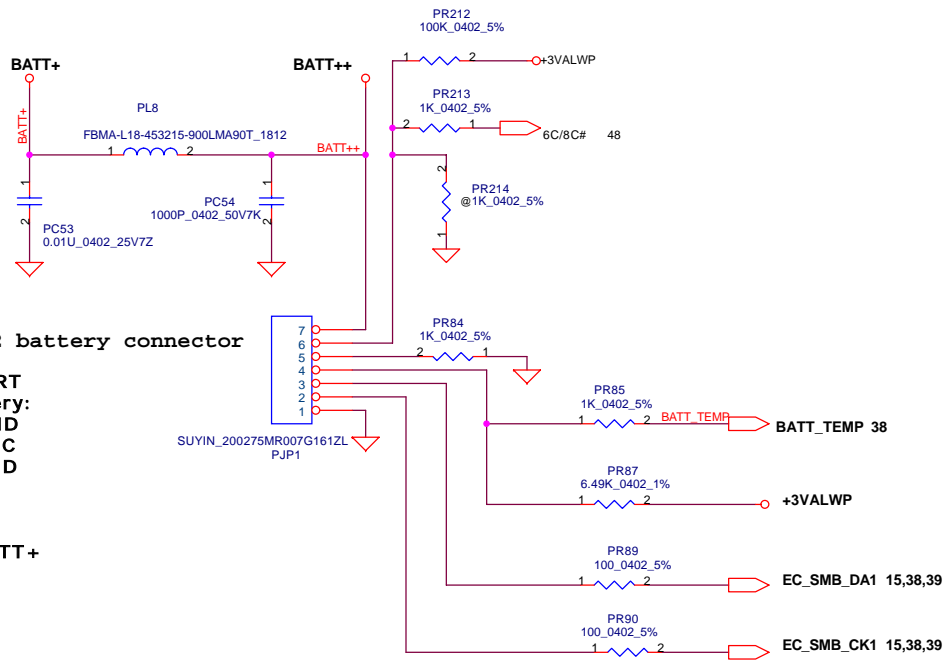
LI-4S : 17.8V--BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+

IREF=0.832*Icharge
IREF=0.73~3.3V

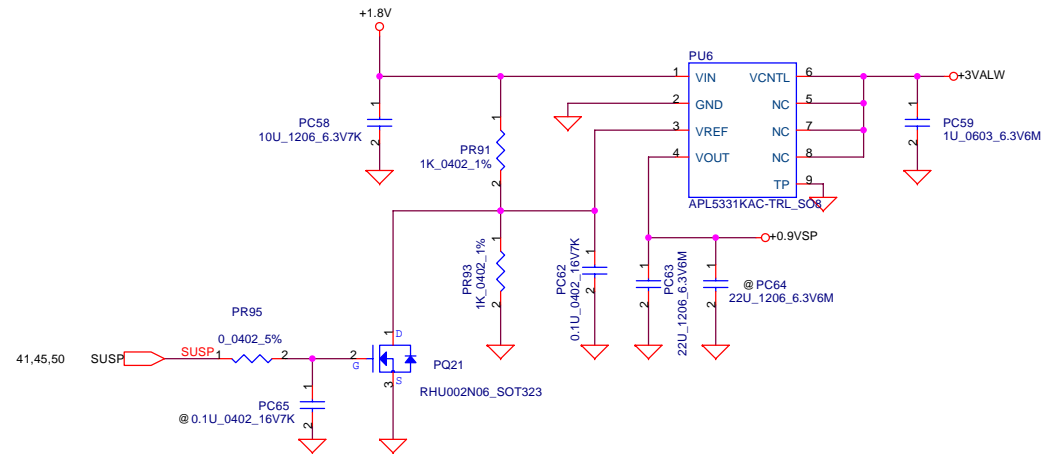
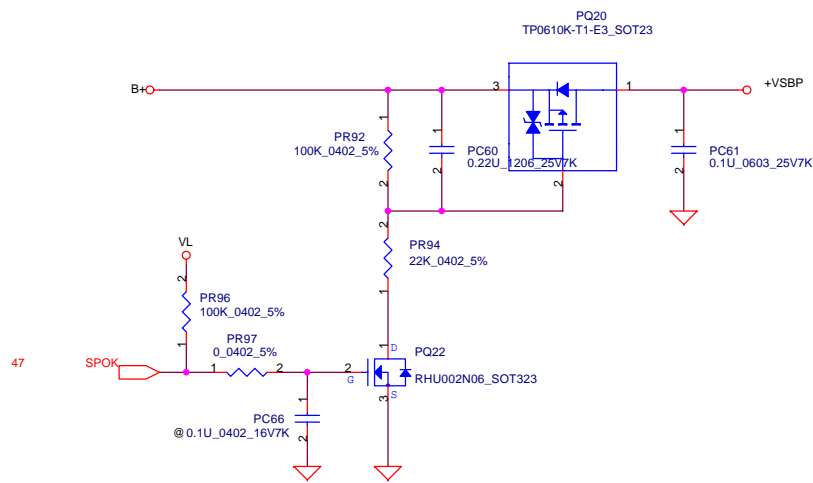
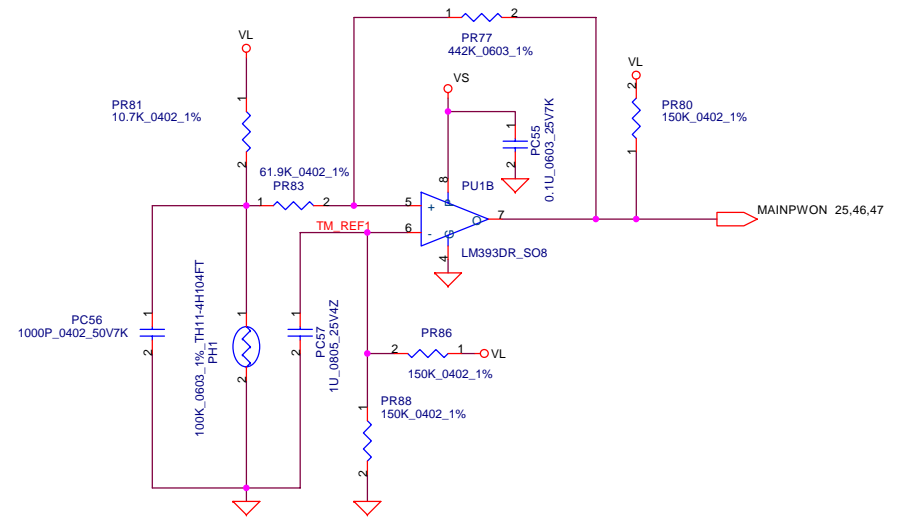
2P4S:4800mAh/cell
0.8C=3.84A

OVP voltage :
LI-3S : 17.8V---BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+

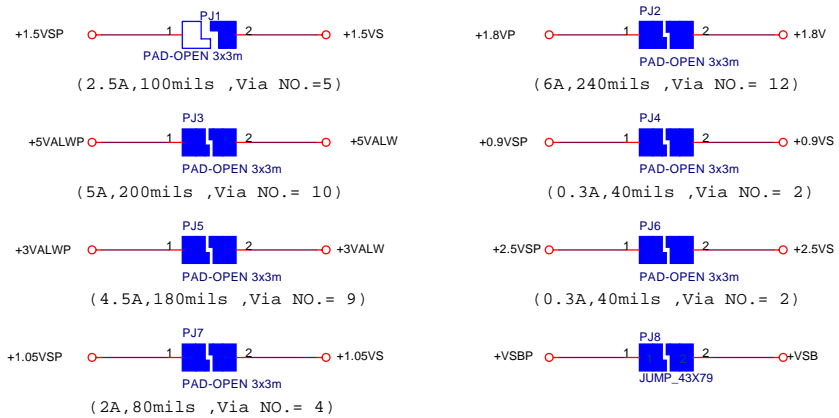
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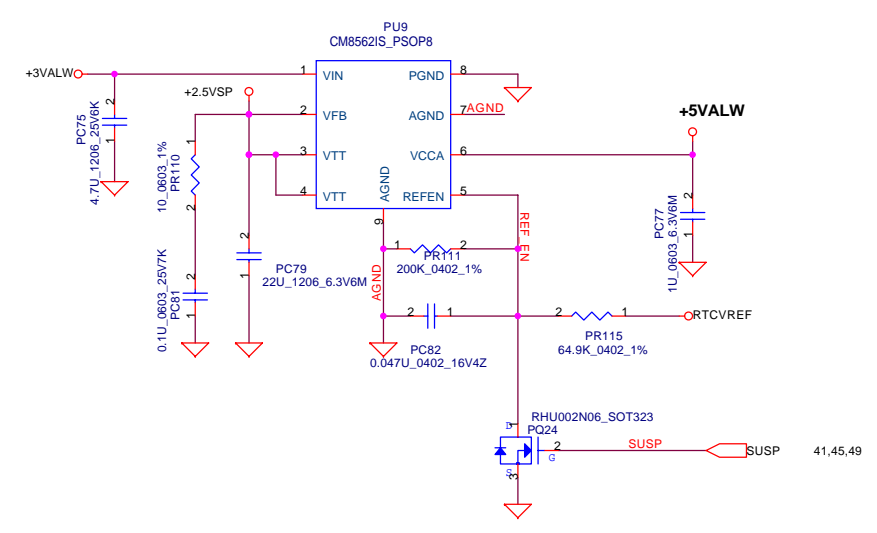
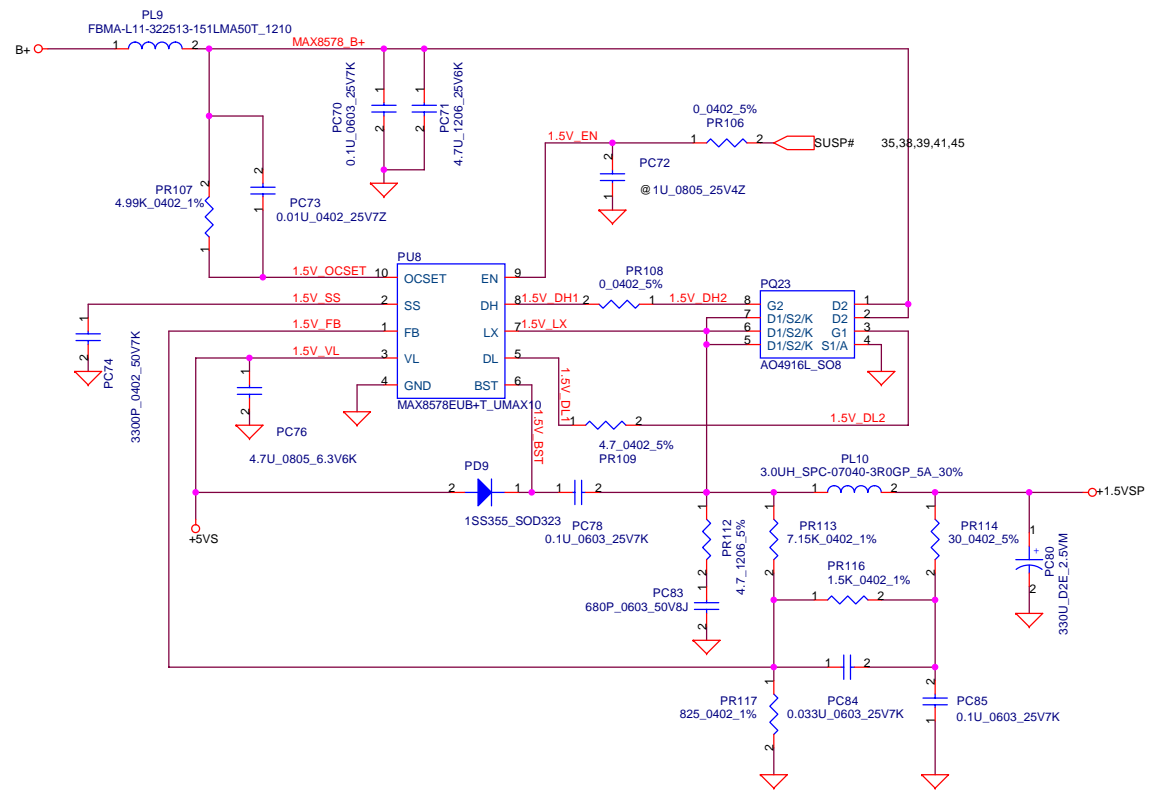
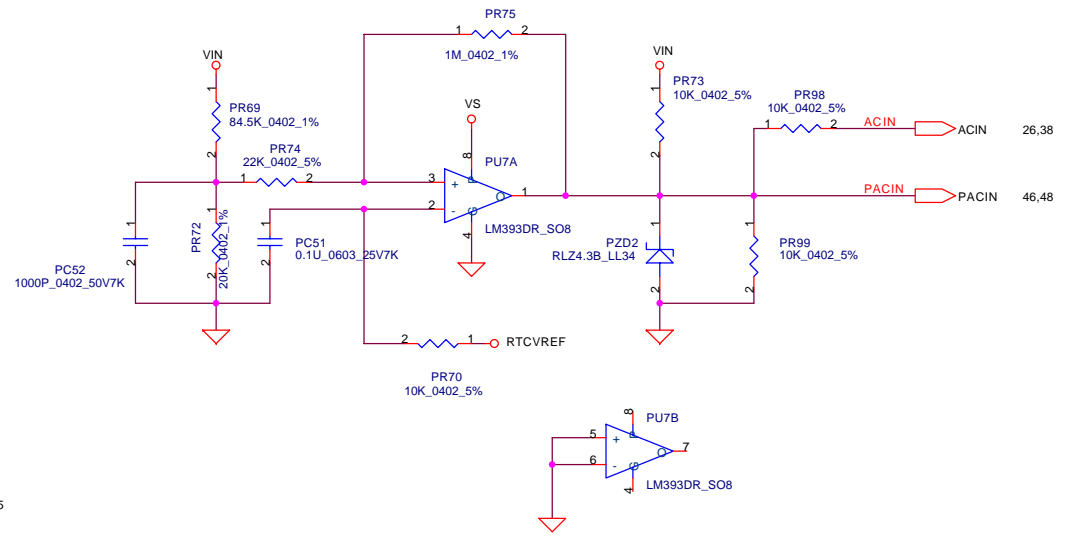
PH1 under CPU bottom side :
 CPU thermal protection at 80 degree C
 Recovery at 44(45) degree C



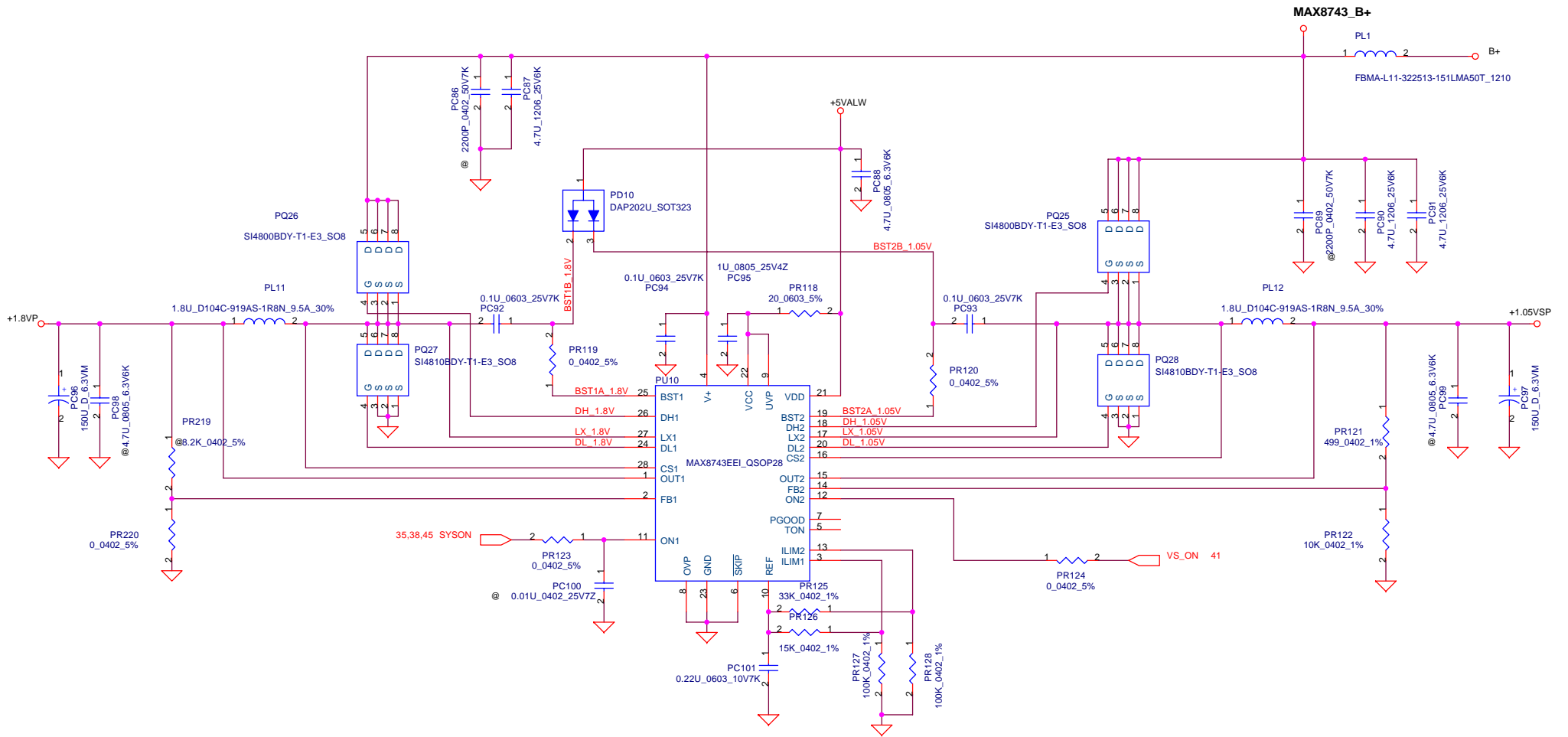
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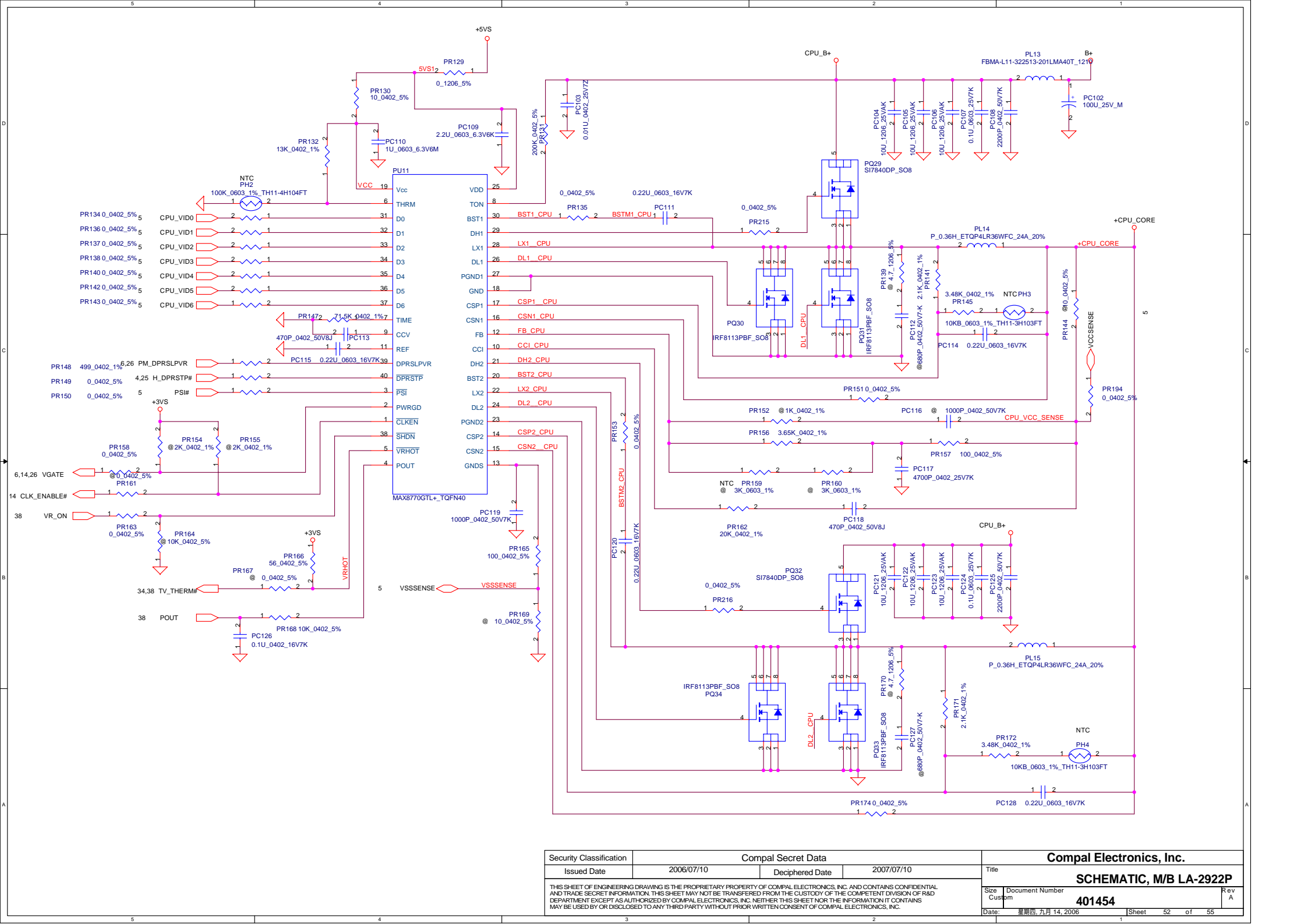
Vin Detector
17.90V/17.24V



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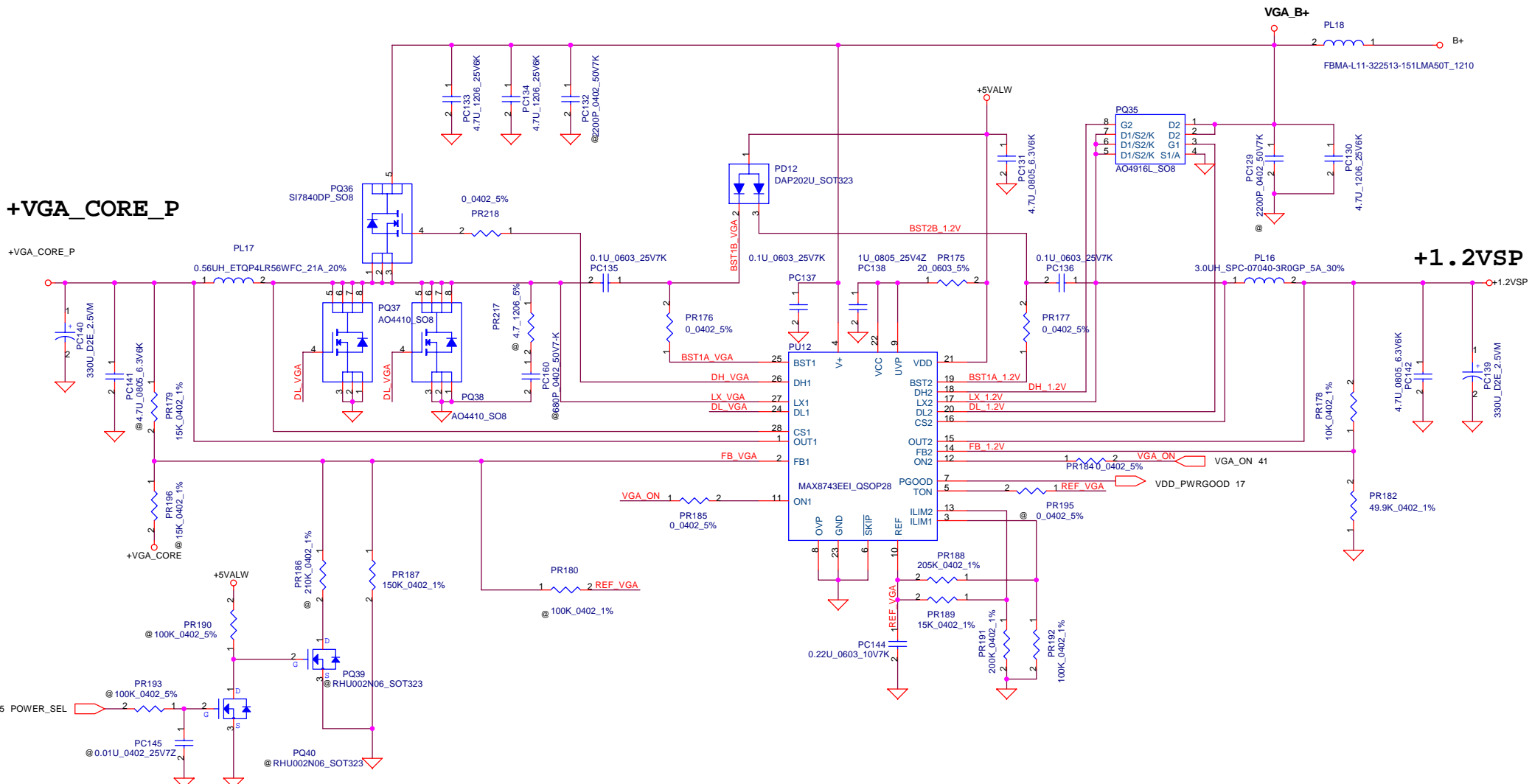


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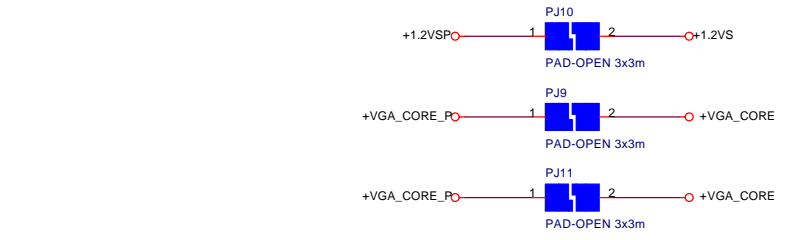
POWER_SEL	H	L
+VGA_CORE FOR G73.	+0.95V(VGA@+G72@)	+1.025V
+VGA_CORE FOR G72.	+1.1V(VGA@)	



+VGA_CORE_P

+VGA_CORE_P

15 POWER_SEL



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Rev 0.1 --> Rev 1.0 Change List

1. Page15 : Change BOM structure of R831 to VGA@
2. Page17 : Add C1110 to C1120 on power plane for EMI Require.
3. Page26 : Add BOM structure @ on D38 & R887

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