

Compal Confidential

KBLG0 Schematics Document

AMD Puma : Griffin Processor with RS780MN/SB700/M92-M2 XT

Tigris : Caspian Processor with RS880M/SB710/M92-M2 XT

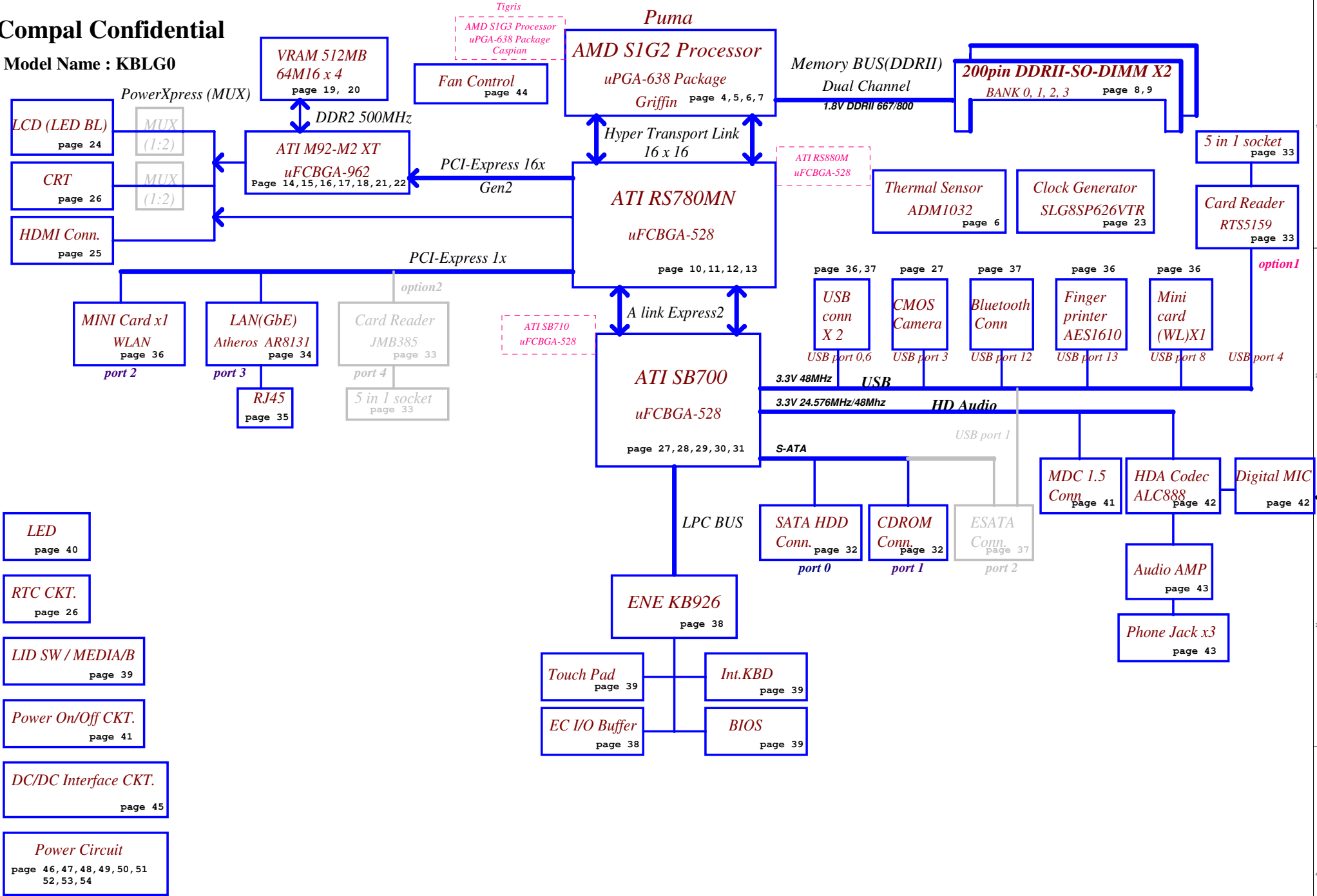
2009-03-11

REV: 1.0

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Model Name : KBLG0



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- LID SW / MEDIA/B page 39
- Power On/Off CKT. page 41
- DC/DC Interface CKT. page 45
- Power Circuit page 46, 47, 48, 49, 50, 51, 52, 53, 54

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Smart Battery	0001 011X b	16H	98H
ADI ADM1032 (CPU)	1001 100X b		9AH
GMT G781-1 (GPU)	1001 101X b		9CH
SB-Temp Sensor			

EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (CPU)	1001 100X b	98H
			GMT G781-1 (GPU)	1001 101X b	9AH
			SB-Temp Sensor		9CH

SB700

SM Bus 0 address

Device	Address	HEX	Device	Address
Clock Generator (SILEGO SLG8P626)	1101 001Xb	D2	New card	
DDR DIMM1	1001 000Xb	90		
DDR DIMM2	1001 010Xb	94		
Mini card				

SB700

SM Bus 1 address

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

BTO Option Table

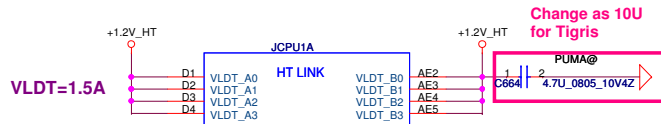
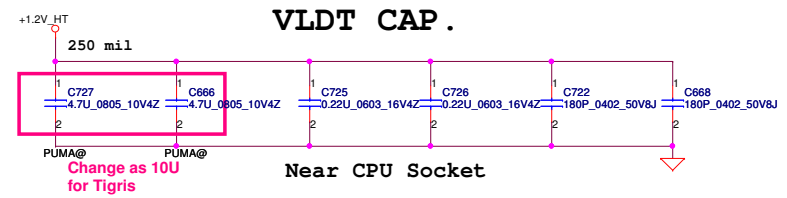
BTO Item	BOM Structure
Discrete	VGA@
UMA	UMA@
M92-M2 XT	M92@
VRAM STRAP	VRAM@
LAN 8121	8121@
LAN 8131	8131@
HDT debug	HDT@
JMB385 CR	JMB385@
RTS5159 CR	RTS5159@
FOR PUMA	PUMA@
FOR TIGRIS	TIGRIS@
FOR TEST	UB@

	SB700	SB700	RS780MN	DISPLAY OUTPUT
	PX_GPIO0	PX_GPIO1	PX_GPIO2	
Function Description	dGPU_Reset	dGPU_PWR_Enable	PX Mode Switch	
IGP only mode	X	X	X	
PowerXpress mode	H : Enable	H : Enable	L : IGPU(DC) / H : dGPU(AC)	LVDS / CRT

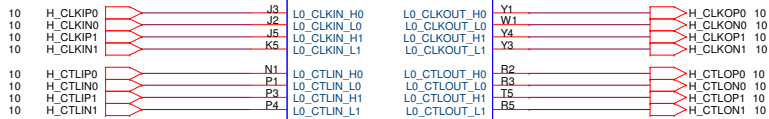
KB926						
	PX_GPIO1	PX_GPIO2	PX_+3VS	PX_+1.8VS	PX_+VGA_CORE	PX_GPIO2_NB
Function Description	Enable +1.1VS_PX	PX MODE SWITCH	Enable +3VS_DELAY	Enable +1.8VS_PX	Enable +VGA_CORE	Trigger from SB
IGP only mode	X	X	X	X	X	X
PowerXpress mode	H : Enable	Reserved	H : Enable	H : Enable	H : Enable	Reserved

KB926	
	PX_GPIO1_SB
Function Description	Trigger from SB to Enable (PX_GPIO1/PX_+3VS/PX_+1.8VS/PX_+VGA_CORE)
IGP only mode	X
PowerXpress mode	H : Enable

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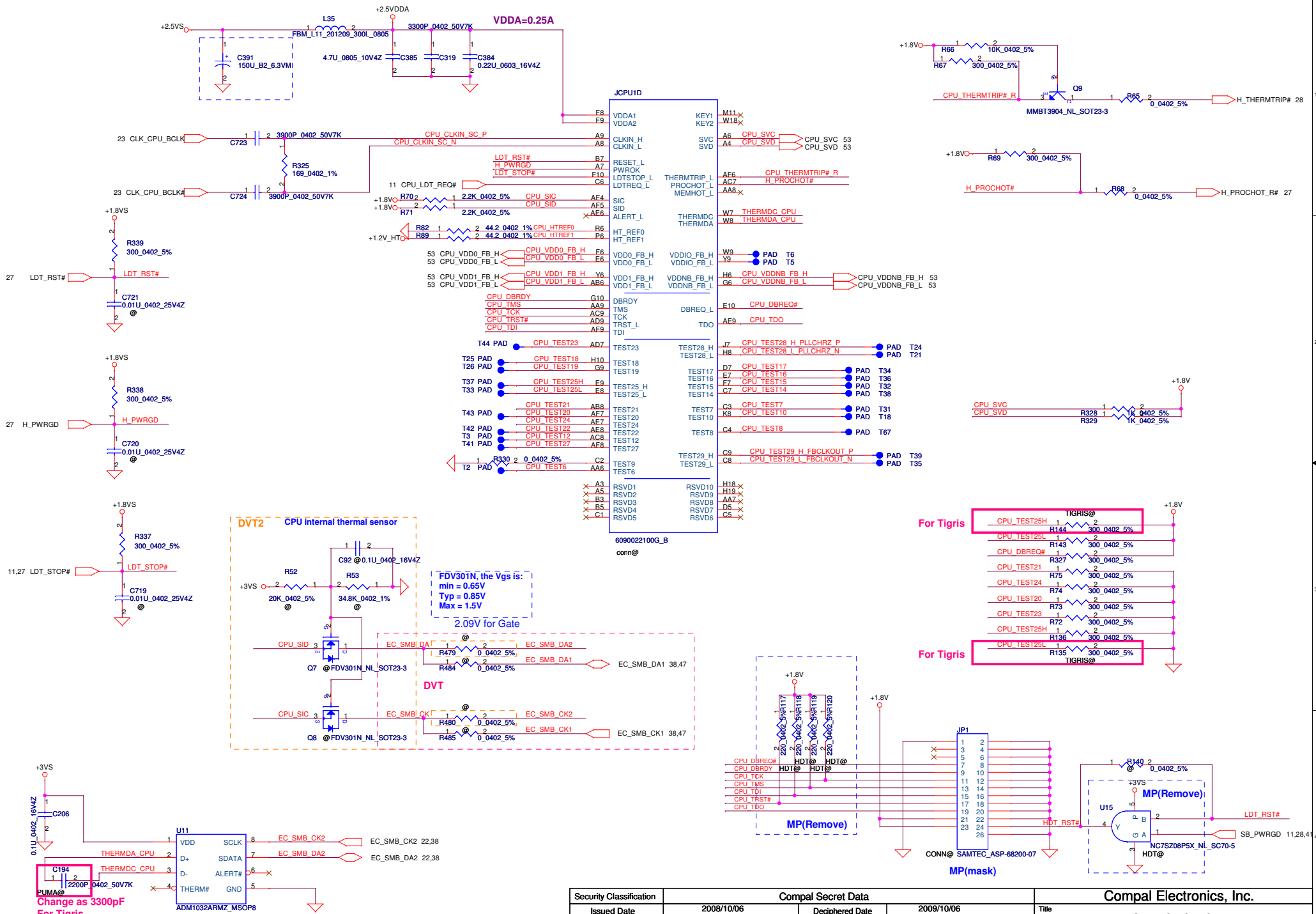


H_CADIP0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	H_CADOP0
H_CADIN0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	H_CADON0
H_CADIP1	F1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	H_CADON2
H_CADIP3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	H_CADOP3
H_CADIN3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	H_CADON3
H_CADIP4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	H_CADOP4
H_CADIN4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	H_CADON4
H_CADIP5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	H_CADOP5
H_CADIN5	L2	L0_CADIN_L5	L0_CADOUT_L5	L1	H_CADON5
H_CADIP6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	H_CADOP6
H_CADIN6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	H_CADON6
H_CADIP7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	H_CADOP7
H_CADIN7	E5	L0_CADIN_L7	L0_CADOUT_L7	R1	H_CADON7
H_CADIP8	N2	L0_CADIN_H8	L0_CADOUT_H8	AD4	H_CADOP8
H_CADIN8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	H_CADON8
H_CADIP9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	H_CADON9
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H_CADIN10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	H_CADON10
H_CADIP11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	H_CADOP11
H_CADIN11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	H_CADON11
H_CADIP12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	H_CADOP12
H_CADIN12	K4	L0_CADIN_L12	L0_CADOUT_L12	Y5	H_CADON12
H_CADIP13	L5	L0_CADIN_H13	L0_CADOUT_H13	W4	H_CADOP13
H_CADIN13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	H_CADON13
H_CADIP14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	H_CADOP14
H_CADIN14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	H_CADON14
H_CADIP15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	H_CADOP15
H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	H_CADON15



6090022100G_B conn@

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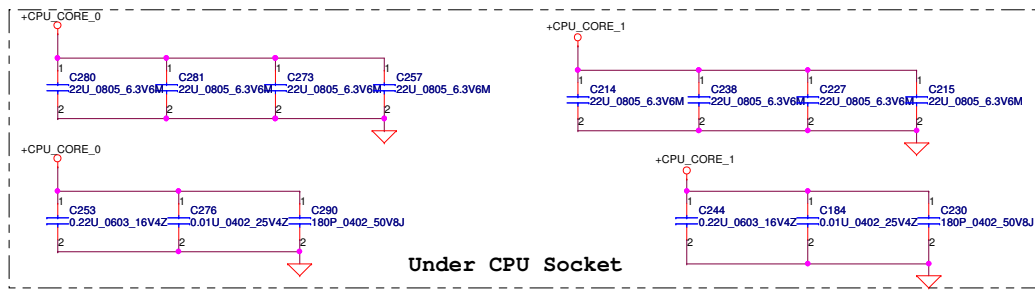
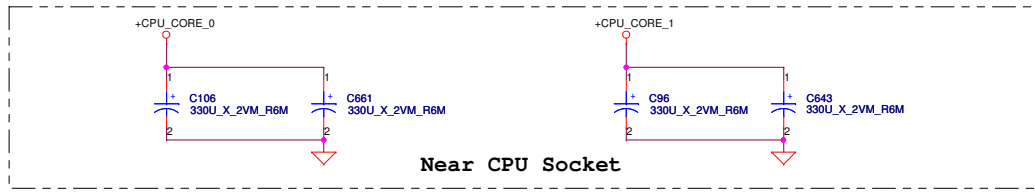


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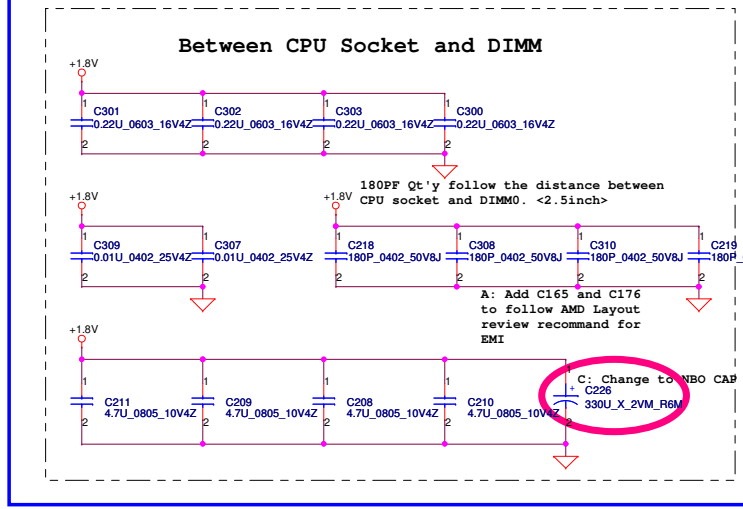
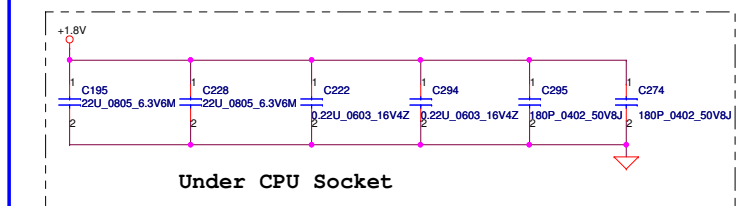
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AMD CPU S1G2 CTRL		
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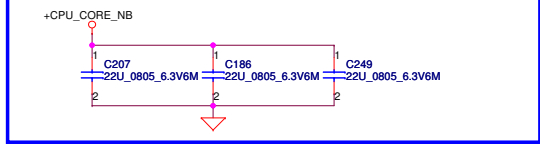
VDD (+CPU_CORE) decoupling.



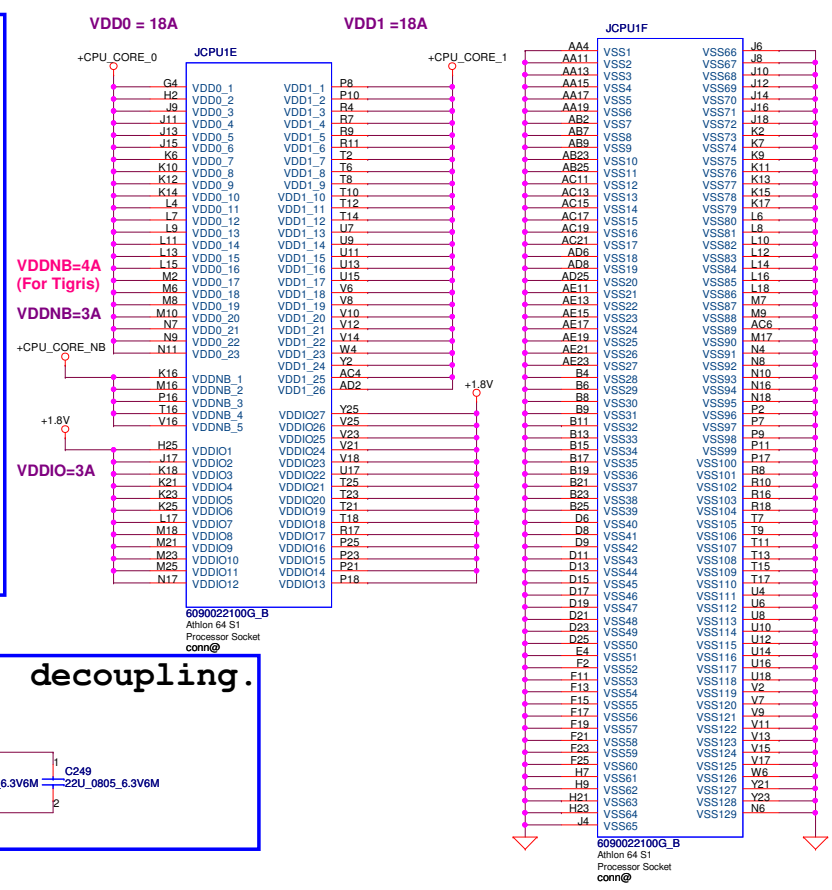
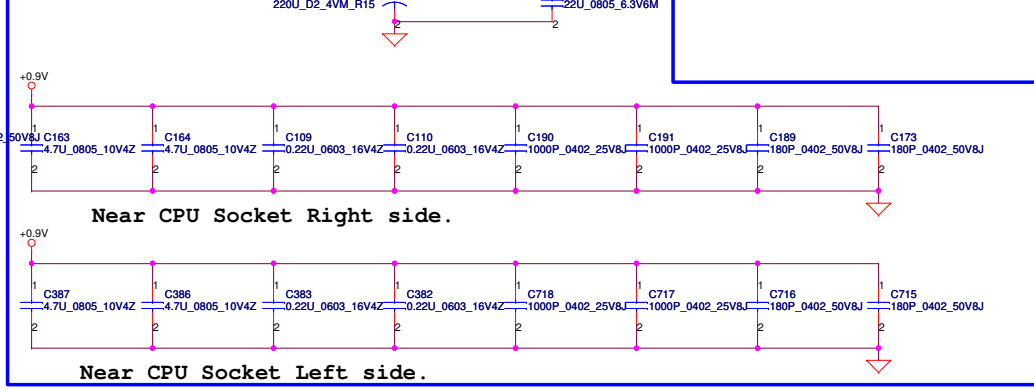
VDDIO decoupling.



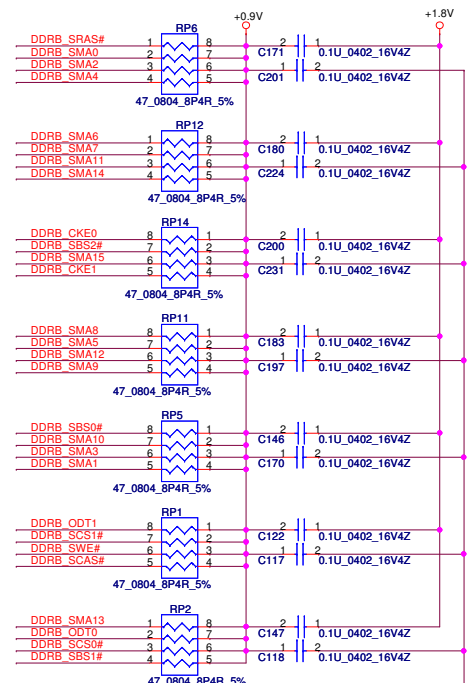
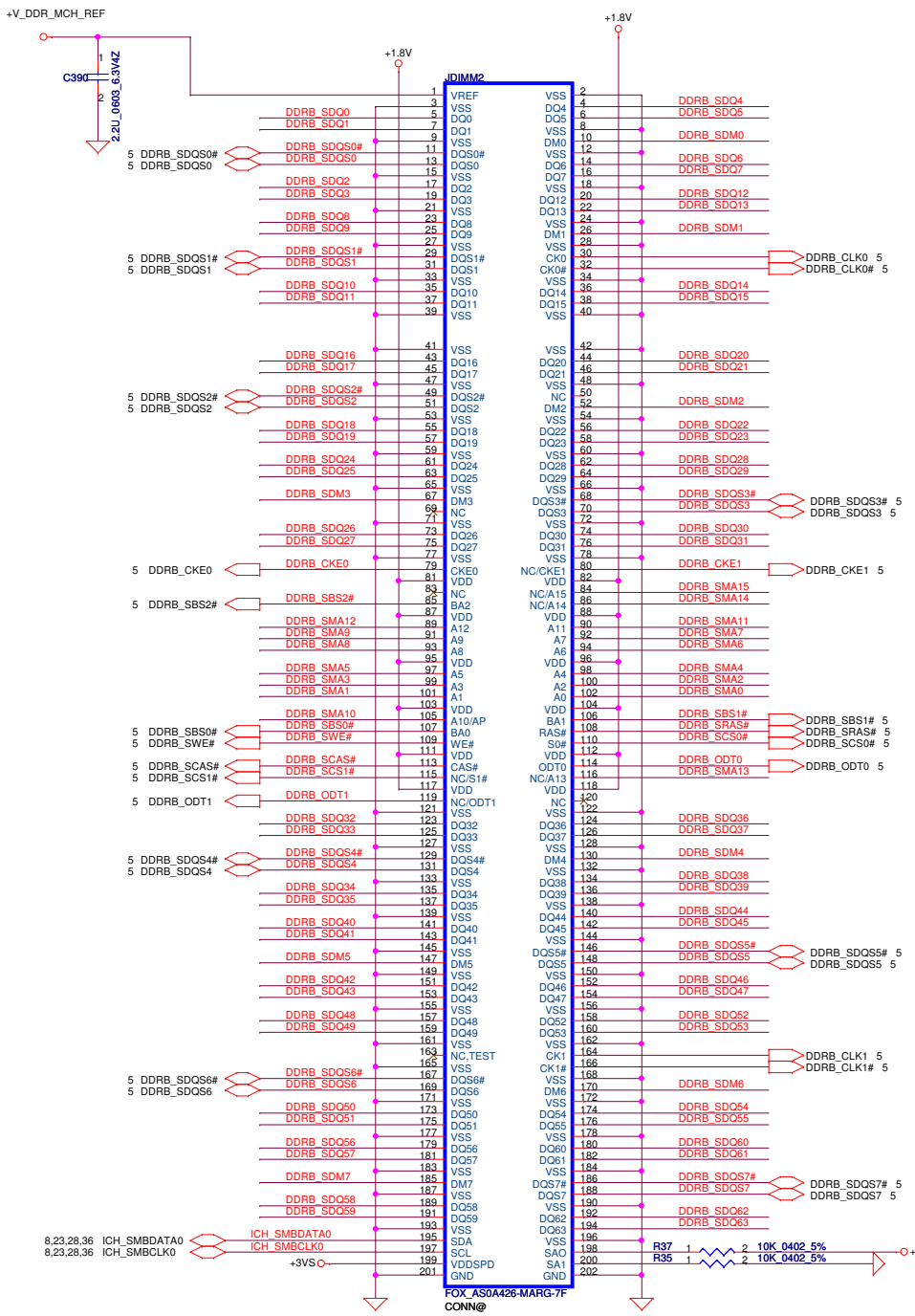
+CPU_CORE_NB decoupling.



VTT decoupling.



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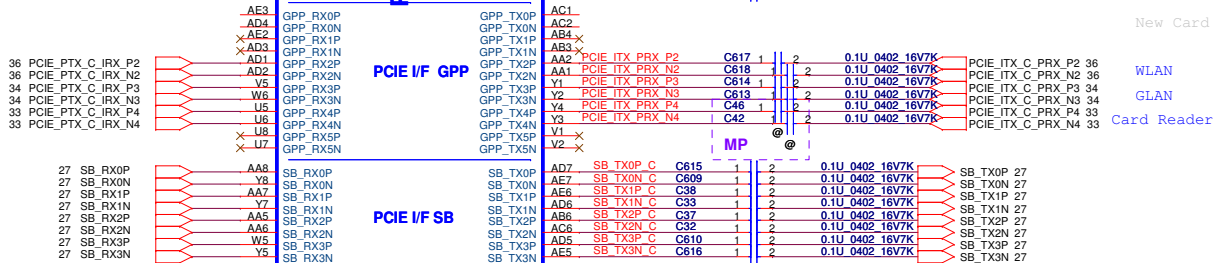
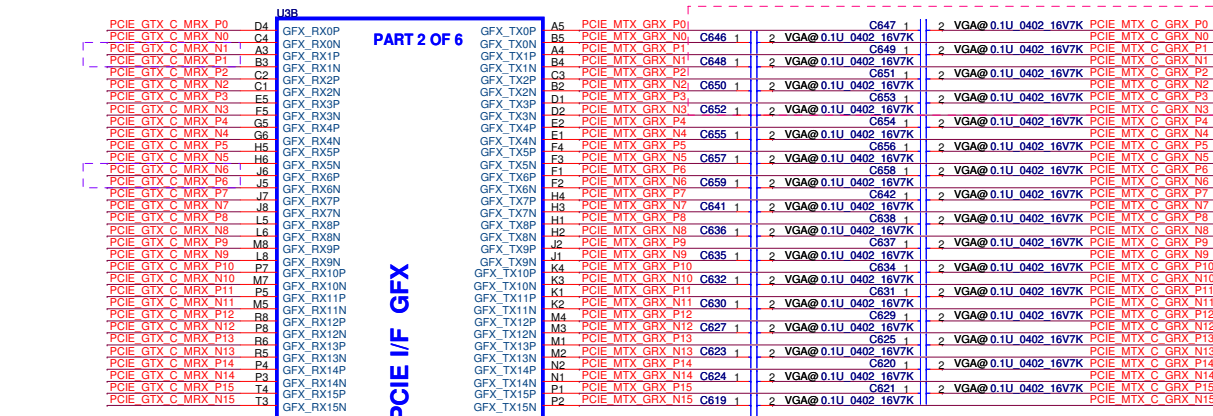
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14 PCIE GTX_C_MRX_P[0..15] PCIE GTX_C_MRX_P[0..15]
 14 PCIE GTX_C_MRX_N[0..15] PCIE GTX_C_MRX_N[0..15]

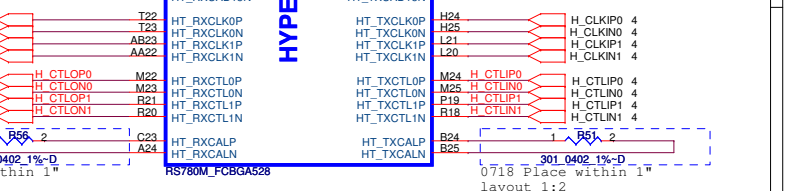
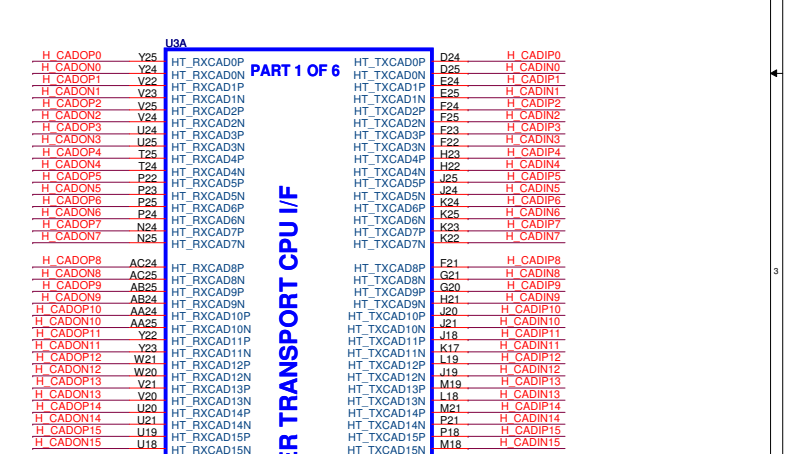
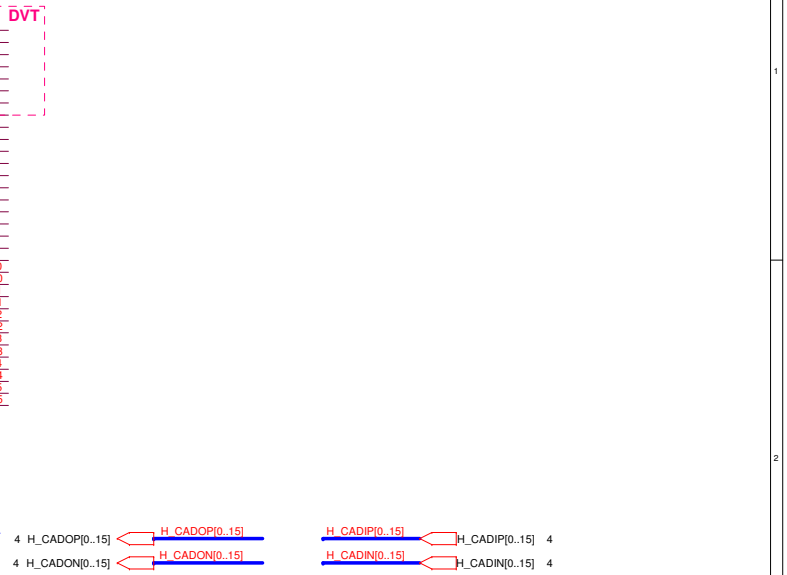
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 PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15] 14

PCIE_MTX_GRX_N[0..3] PCIE_MTX_GRX_N[0..3] 25
 PCIE_MTX_GRX_P[0..3] PCIE_MTX_GRX_P[0..3] 25



RS780M_FCBGA528
 RS780M Display Port Support (muxed on GFX)

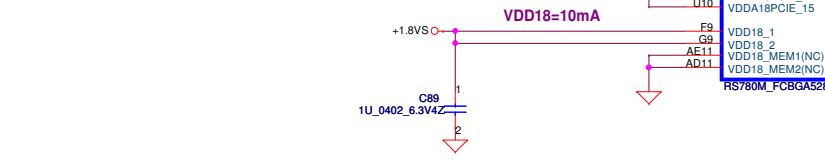
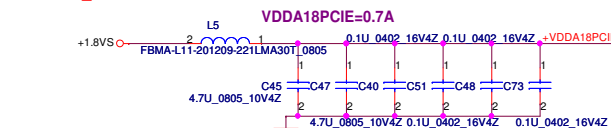
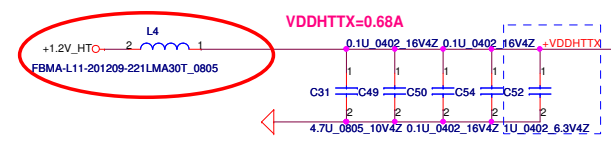
DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1



0718 Place within 1" layout 1:2
 RS780M_FCBGA528
 0718 Place within 1" layout 1:2

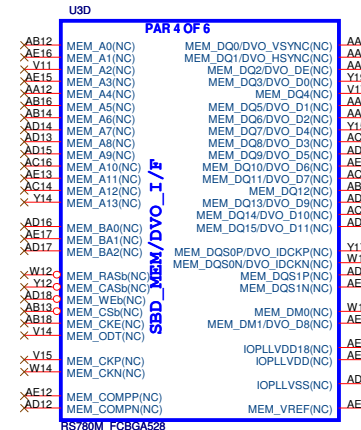
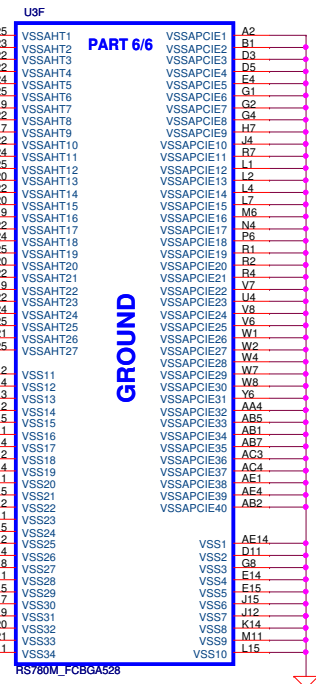
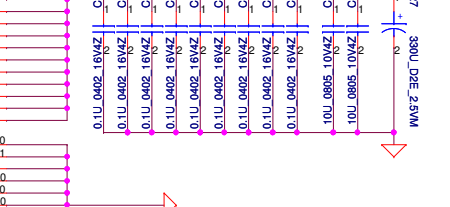
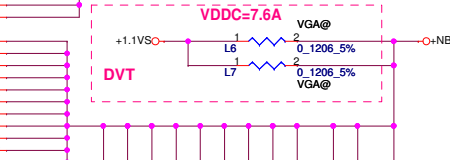
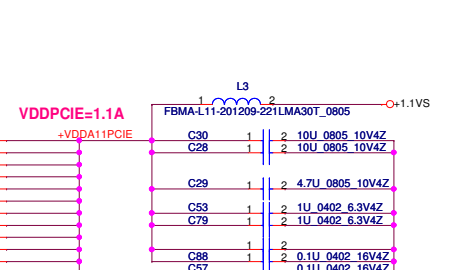
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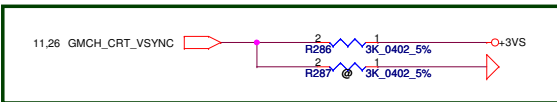
POWER

U3E	VDDHTRX_1	VDDPCIE_1	VDDPCIE_17
K16	VDDHT_2	VDDPCIE_2	VDDPCIE_18
L16	VDDHT_3	VDDPCIE_3	VDDPCIE_19
M18	VDDHT_5	VDDPCIE_4	VDDPCIE_20
P16	VDDHT_6	VDDPCIE_5	VDDPCIE_21
R16	VDDHT_7	VDDPCIE_6	VDDPCIE_22
T16	VDDHT_7	VDDPCIE_7	VDDPCIE_23
H18	VDDHTRX_1	VDDPCIE_8	VDDPCIE_24
G19	VDDHTRX_2	VDDPCIE_9	VDDPCIE_25
F20	VDDHTRX_3	VDDPCIE_10	VDDPCIE_26
E21	VDDHTRX_3	VDDPCIE_11	VDDPCIE_27
D22	VDDHTRX_4	VDDPCIE_12	VDDPCIE_28
C23	VDDHTRX_5	VDDPCIE_13	VDDPCIE_29
B23	VDDHTRX_6	VDDPCIE_14	VDDPCIE_30
A23	VDDHTRX_7	VDDPCIE_15	VDDPCIE_31
AE25	VDDHTRX_7	VDDPCIE_16	VDDPCIE_32
AD24	VDDHTRX_8	VDDPCIE_17	VDDPCIE_33
AC23	VDDHTRX_9	VDDPCIE_18	VDDPCIE_34
AB22	VDDHTRX_10	VDDPCIE_19	VDDPCIE_35
AA21	VDDHTRX_11	VDDPCIE_20	VDDPCIE_36
Y20	VDDHTRX_12	VDDPCIE_21	VDDPCIE_37
W19	VDDHTRX_13	VDDPCIE_22	VDDPCIE_38
V18	VDDHTRX_13	VDDPCIE_23	VDDPCIE_39
U17	VDDHTRX_13	VDDPCIE_24	VDDPCIE_40
T17	VDDHTRX_13	VDDPCIE_25	VDDPCIE_41
R17	VDDHTRX_13	VDDPCIE_26	VDDPCIE_42
P17	VDDHTRX_13	VDDPCIE_27	VDDPCIE_43
M17	VDDHTRX_13	VDDPCIE_28	VDDPCIE_44
J10	VDDA18PCIE_1	VDDPCIE_29	VDDPCIE_45
P10	VDDA18PCIE_2	VDDPCIE_30	VDDPCIE_46
K10	VDDA18PCIE_3	VDDPCIE_31	VDDPCIE_47
M10	VDDA18PCIE_4	VDDPCIE_32	VDDPCIE_48
L10	VDDA18PCIE_5	VDDPCIE_33	VDDPCIE_49
W9	VDDA18PCIE_6	VDDPCIE_34	VDDPCIE_50
H9	VDDA18PCIE_7	VDDPCIE_35	VDDPCIE_51
T10	VDDA18PCIE_8	VDDPCIE_36	VDDPCIE_52
R10	VDDA18PCIE_9	VDDPCIE_37	VDDPCIE_53
Y9	VDDA18PCIE_10	VDDPCIE_38	VDDPCIE_54
AE9	VDDA18PCIE_11	VDDPCIE_39	VDDPCIE_55
AD9	VDDA18PCIE_12	VDDPCIE_40	VDDPCIE_56
AE9	VDDA18PCIE_13	VDDPCIE_41	VDDPCIE_57
U10	VDDA18PCIE_14	VDDPCIE_42	VDDPCIE_58
F9	VDDA18PCIE_15	VDDPCIE_43	VDDPCIE_59
G9	VDDA18PCIE_15	VDDPCIE_44	VDDPCIE_60
AE11	VDDA18PCIE_15	VDDPCIE_45	VDDPCIE_61
AD11	VDDA18PCIE_15	VDDPCIE_46	VDDPCIE_62
F9	VDD18_1	VDDPCIE_47	VDDPCIE_63
G9	VDD18_2	VDDPCIE_48	VDDPCIE_64
AE11	VDD18_MEM1(NC)	VDDPCIE_49	VDDPCIE_65
AD11	VDD18_MEM2(NC)	VDDPCIE_50	VDDPCIE_66



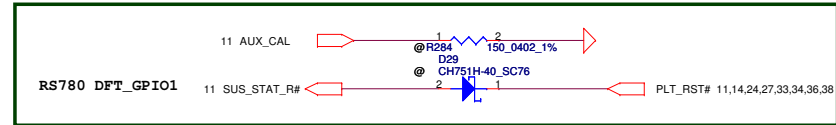
+1.8VS=W/S=20/10mil For Memory PLL power
+1.1VS=W/S=20/10mil For Memory PLL power

Security Classification	Compal Secret Data	Title		
Issued Date	2008/10/06	RS780 PWR/GND		
Deciphered Date	2009/10/06	Size	Document Number	Rev
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		Date:	Thursday, January 15, 2009	Sheet 12 of 57



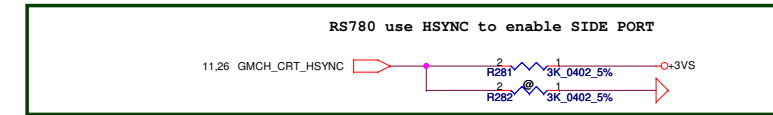
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO. (VSYNC)
 1 : Disable (RS780)
 0 : Enable (Rs780)



DFT_GPIO1:LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RS740/RX780: DFT_GPIO1 RS780:SUS_STAT



RS780 use HSYNC to enable SIDE PORT

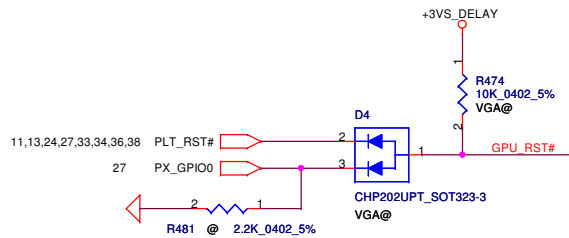
RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
 0 : Enable (RS780)
 1 : Disable(RS780)

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				Custom	KBLG0 LA-4921P
				Date:	Thursday, February 19, 2009
				Sheet	13 of 57
				Rev	0.1

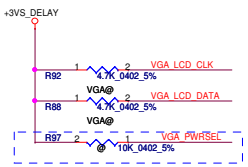
- 10 PCIE_GTX_C_MRX_P[0..15] ← PCIE GTX C MRX P[0..15]
- 10 PCIE_GTX_C_MRX_N[0..15] ← PCIE GTX C MRX N[0..15]
- 10 PCIE_MTX_C_GRX_P[0..15] ← PCIE MTX C GRX P[0..15]
- 10 PCIE_MTX_C_GRX_N[0..15] ← PCIE MTX C GRX N[0..15]

PCIE LANE REVERSAL

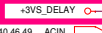
PCIE LANE REVERSAL



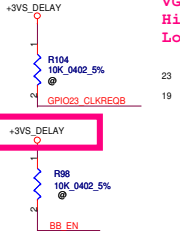
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Size	Document Number	KBLG0 LA-4921P		Rev	0.1
Custom	Date: Thursday, February 19, 2009				Sheet 14 of 57



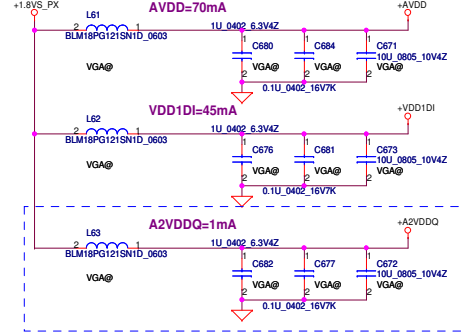
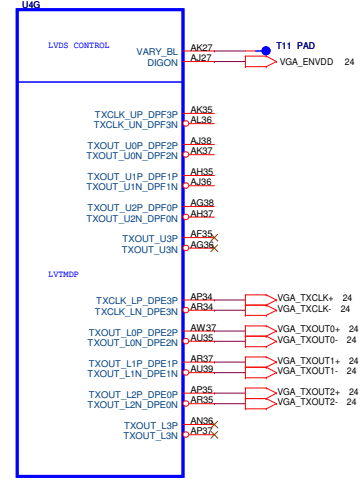
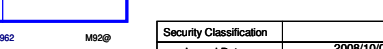
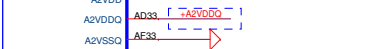
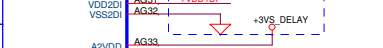
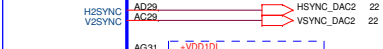
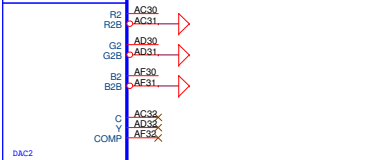
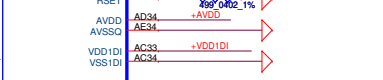
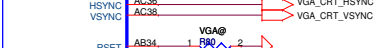
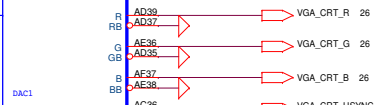
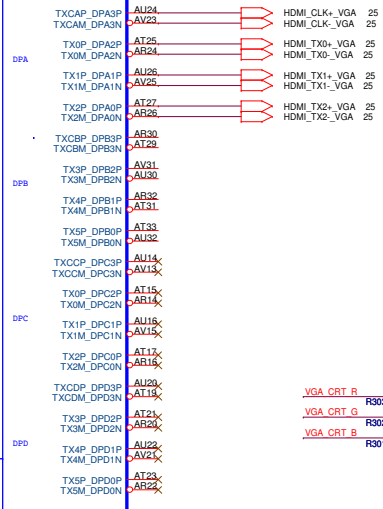
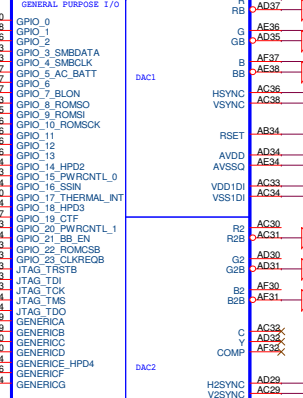
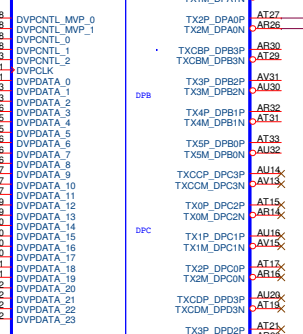
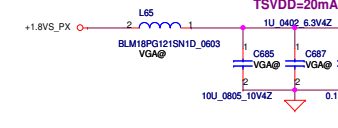
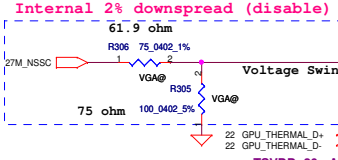
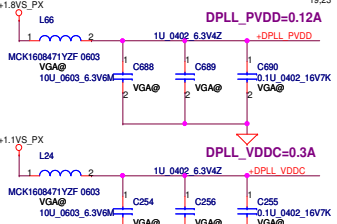
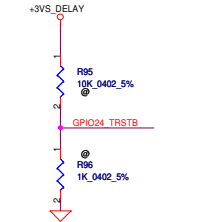
GPIO_5_AC_BATT
AC (Performance mode) = 3.3 V
Battery saving mode = 0.0 V



VGA_PWRSEL
High:VGA_CORE 0.95V
Low :VGA_CORE 1.2V

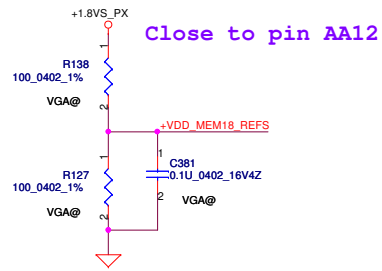
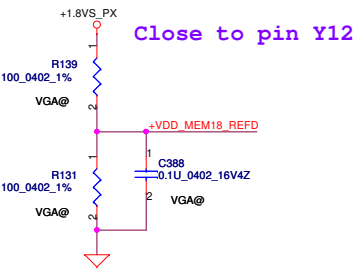
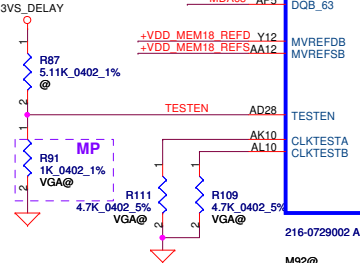
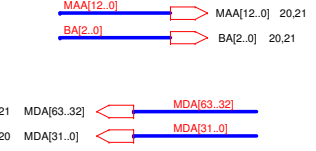
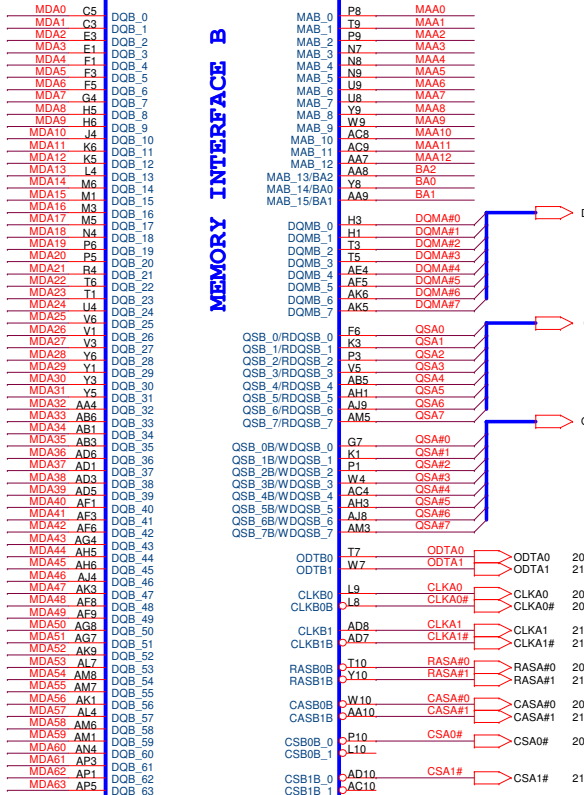


Back bias (BB) control
Back Bias Disabled :
GPIO_21_BB_EN = 0V
BBP connect directly to VDDC

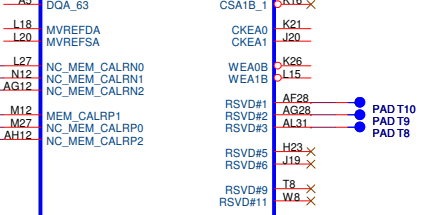
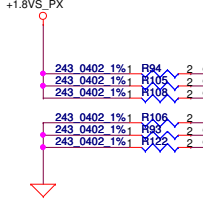


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MEMORY INTERFACE B

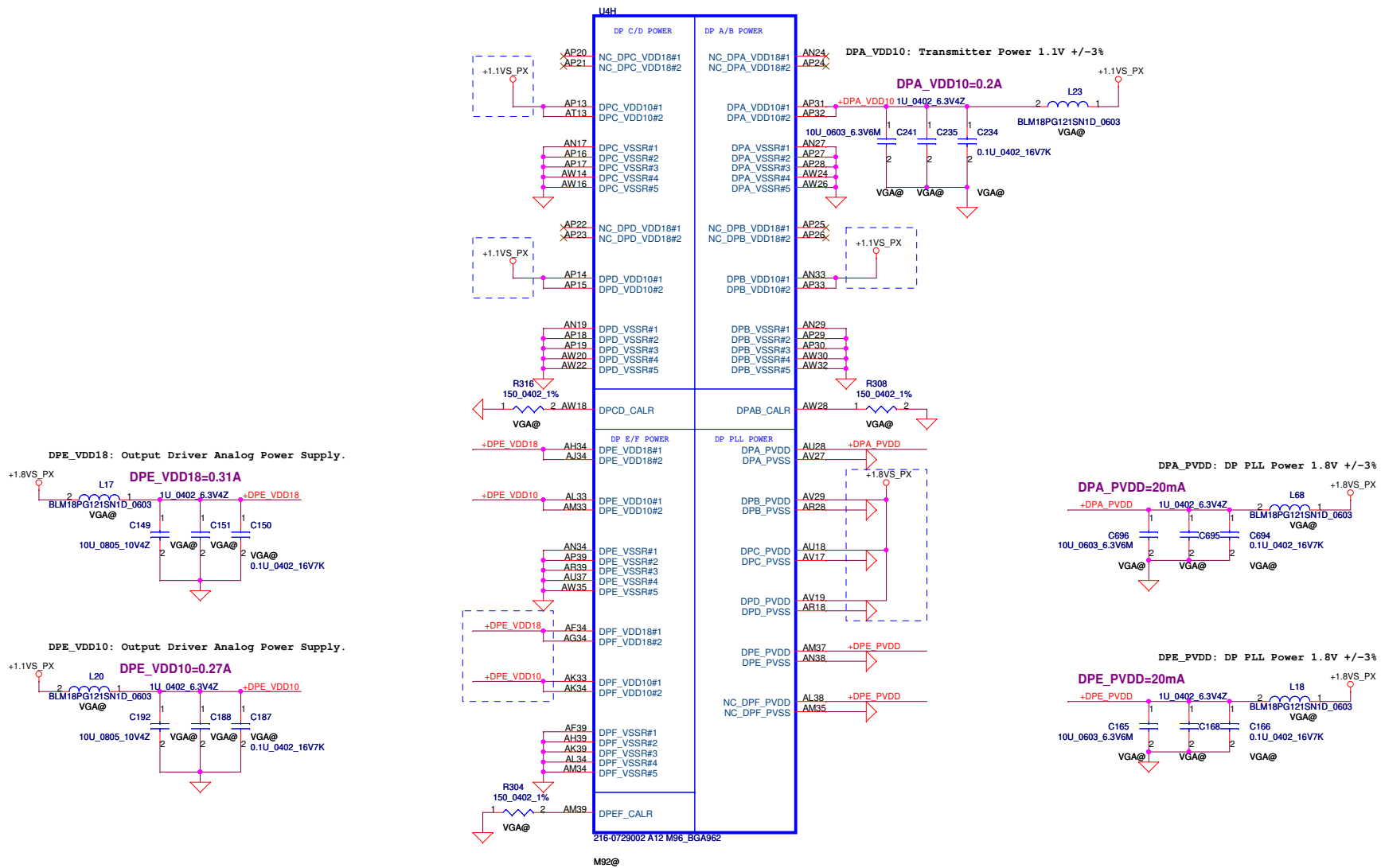


MEMORY INTERFACE A

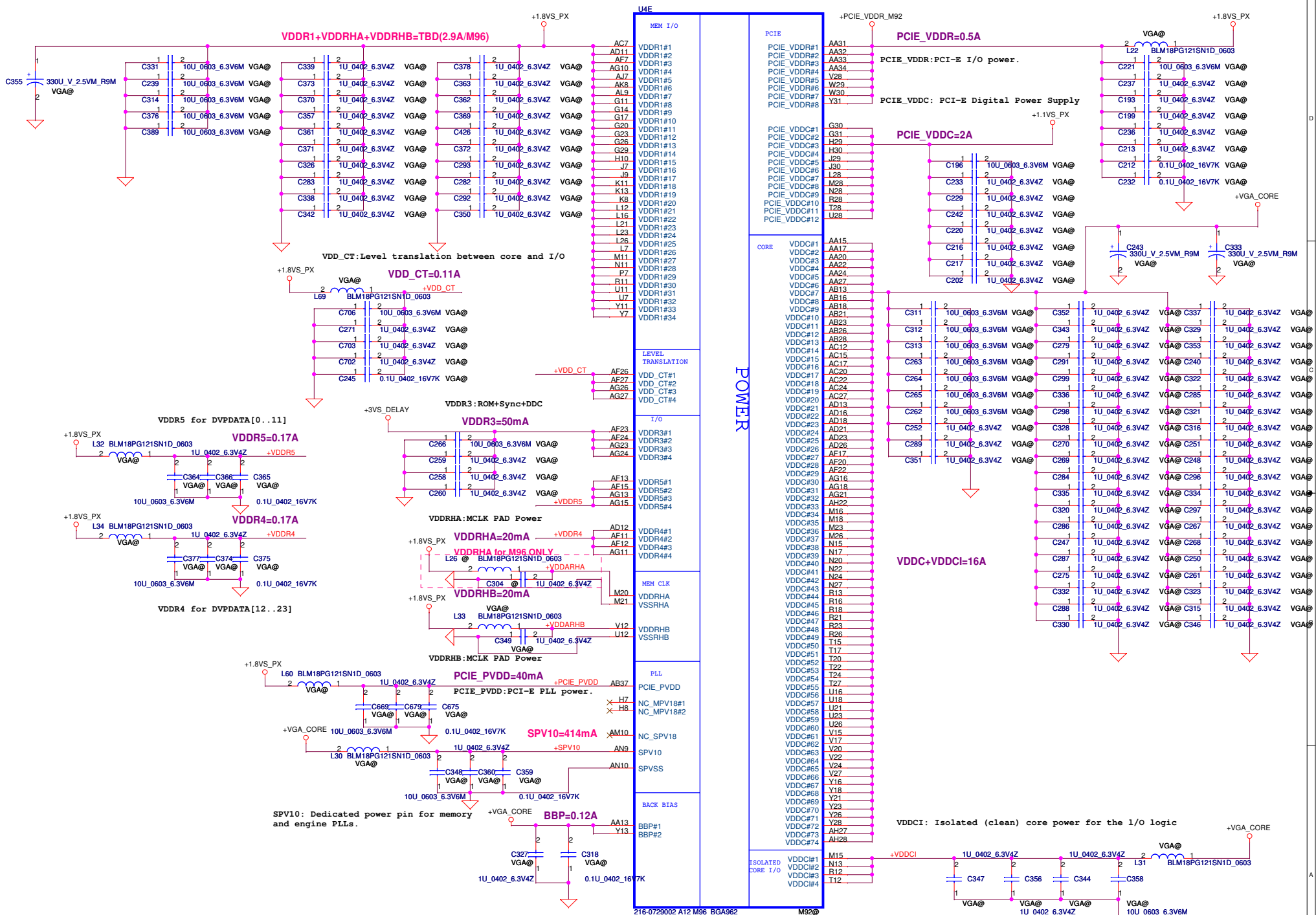


M92-S2 and M92-M use memory group A only while M92-M2 uses memory group B only.

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Date:	Thursday, January 15, 2009	Sheet	17	of 57



MEM I/O	VDDR1#1 VDDR1#2 VDDR1#3 VDDR1#4 VDDR1#5 VDDR1#6 VDDR1#7 VDDR1#8 VDDR1#9 VDDR1#10 VDDR1#11 VDDR1#12 VDDR1#13 VDDR1#14 VDDR1#15 VDDR1#16 VDDR1#17 VDDR1#18 VDDR1#19 VDDR1#20 VDDR1#21 VDDR1#22 VDDR1#23 VDDR1#24 VDDR1#25 VDDR1#26 VDDR1#27 VDDR1#28 VDDR1#29 VDDR1#30 VDDR1#31 VDDR1#32 VDDR1#33 VDDR1#34
LEVEL TRANSLATION	VDD_CT#1 VDD_CT#2 VDD_CT#3 VDD_CT#4
I/O	VDDR3#1 VDDR3#2 VDDR3#3 VDDR3#4 VDDR5#1 VDDR5#2 VDDR5#3 VDDR5#4 VDDR4#1 VDDR4#2 VDDR4#3 VDDR4#4
MEM CLK	VDDRHA VSSRHA VDDRHB VSSRHB
PLL	PCIE_PVDD NC_MPV18#1 NC_MPV18#2 NC_SPV18 SPV10 SPVSS
BACK BIAS	BBP#1 BBP#2
ISOLATED CORE I/O	VDDCI#1 VDDCI#2 VDDCI#3 VDDCI#4

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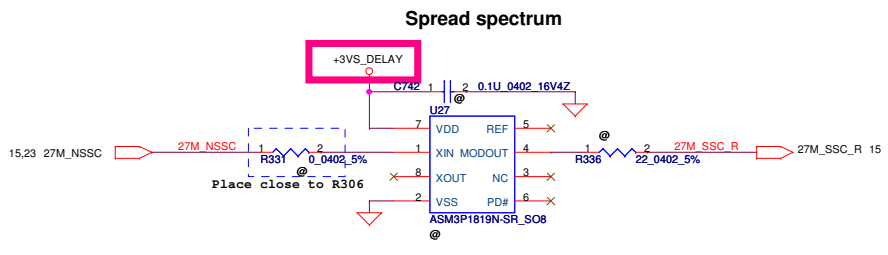
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E39	PCIE_VSS#2	GND#2	A37
F34	PCIE_VSS#3	GND#3	AA16
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G33	PCIE_VSS#5	GND#5	AA2
G34	PCIE_VSS#6	GND#6	AA21
H31	PCIE_VSS#7	GND#7	AA23
H34	PCIE_VSS#8	GND#8	AA26
H39	PCIE_VSS#9	GND#9	AA28
J1	PCIE_VSS#10	GND#10	AA6
J4	PCIE_VSS#11	GND#11	AB12
K31	PCIE_VSS#12	GND#12	AB15
K34	PCIE_VSS#13	GND#13	AB17
K39	PCIE_VSS#14	GND#14	AB20
L31	PCIE_VSS#15	GND#15	AB22
L34	PCIE_VSS#16	GND#16	AB24
M34	PCIE_VSS#17	GND#17	AB27
M39	PCIE_VSS#18	GND#18	AC11
N31	PCIE_VSS#19	GND#19	AC13
N34	PCIE_VSS#20	GND#20	AC16
P31	PCIE_VSS#21	GND#21	AC18
P34	PCIE_VSS#22	GND#22	AC2
P39	PCIE_VSS#23	GND#23	AC21
R34	PCIE_VSS#24	GND#24	AC23
T31	PCIE_VSS#25	GND#25	AC26
T34	PCIE_VSS#26	GND#26	AC28
T39	PCIE_VSS#27	GND#27	AC6
U31	PCIE_VSS#28	GND#28	AD15
U34	PCIE_VSS#29	GND#29	AD17
V34	PCIE_VSS#30	GND#30	AD20
V39	PCIE_VSS#31	GND#31	AD22
W31	PCIE_VSS#32	GND#32	AD24
W34	PCIE_VSS#33	GND#33	AD27
Y34	PCIE_VSS#34	GND#34	AD9
Y39	PCIE_VSS#35	GND#35	AE2
		GND#36	AE6
		GND#37	AF10
		GND#38	AF16
		GND#39	AF18
		GND#40	AF21
		GND#41	AG17
		GND#42	AG2
		GND#43	AG22
		GND#44	AG20
		GND#45	AG6
		GND#46	AG8
		GND#47	AH2
		GND#48	AH29
		GND#49	AJ10
		GND#50	AJ11
		GND#51	AJ2
		GND#52	AJ28
		GND#53	AJ6
		GND#54	AK11
		GND#55	AK31
		GND#56	AK7
		GND#57	AL11
		GND#58	AL14
		GND#59	AL17
		GND#60	AL2
		GND#61	AL20
		GND#62	AL21
		GND#63	AL23
		GND#64	AL26
		GND#65	AL32
		GND#66	AL6
		GND#67	AL8
		GND#68	AM11
		GND#69	AM31
		GND#70	AM9
		GND#71	AN11
		GND#72	AN30
		GND#73	AN2
		GND#74	AN6
		GND#75	AN8
		GND#76	AP11
		GND#77	AP7
		GND#78	AP9
		GND#79	AR5
		GND#80	AW34
		GND#81	B11
		GND#82	B13
		GND#83	B15
		GND#84	B17
		GND#85	B19
		GND#86	B21
		GND#87	B23
		GND#88	B25
		GND#89	B27
		GND#90	B29
		GND#91	B31
		GND#92	B33
		GND#93	B7
		GND#94	B9
		GND#95	C1
		GND#96	C39
		GND#97	E5
		GND#98	E5
		GND#99	F11
		GND#100	F13
F15	GND#101		
F17	GND#102		
F19	GND#103		
F21	GND#104		
F24	GND#105		
F25	GND#106		
F27	GND#107		
F29	GND#108		
F31	GND#109		
F33	GND#110		
F7	GND#111		
F9	GND#112		
G2	GND#113		
G6	GND#114		
H9	GND#115		
J2	GND#116		
J27	GND#117		
J6	GND#118		
J6	GND#119		
K14	GND#120		
K7	GND#121		
L11	GND#122		
L17	GND#123		
L2	GND#124		
L22	GND#125		
L24	GND#126		
L6	GND#127		
M17	GND#128		
M22	GND#129		
M24	GND#130		
N16	GND#131		
N18	GND#132		
N2	GND#133		
N21	GND#134		
N23	GND#135		
N26	GND#136		
N6	GND#137		
R15	GND#138		
R17	GND#139		
R2	GND#140		
R20	GND#141		
R22	GND#142		
R24	GND#143		
R27	GND#144		
R6	GND#145		
T11	GND#146		
T13	GND#147		
T16	GND#148		
T18	GND#149		
T21	GND#150		
T24	GND#151		
T26	GND#152		
U15	GND#153		
U17	GND#154		
U2	GND#155		
U20	GND#156		
U22	GND#157		
U24	GND#158		
U27	GND#159		
U6	GND#160		
V11	GND#161		
V16	GND#162		
V18	GND#163		
V21	GND#164		
V23	GND#165		
V26	GND#166		
W2	GND#167		
W6	GND#168		
Y15	GND#169		
Y17	GND#170		
Y20	GND#171		
Y22	GND#172		
Y24	GND#173		
Y27	GND#174		
U13	GND#175		
Y13	GND#176		

GND

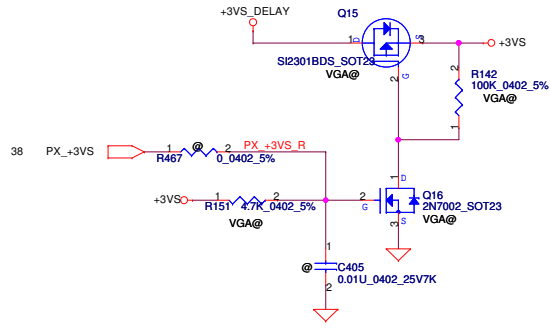
VSS_MECH#1
VSS_MECH#2
VSS_MECH#3

M92@

216-0729002 A12 M96_BGA962

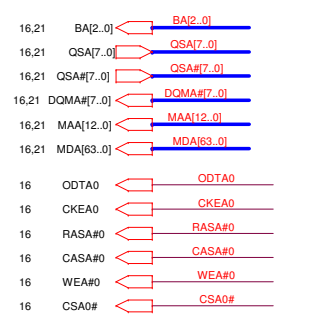
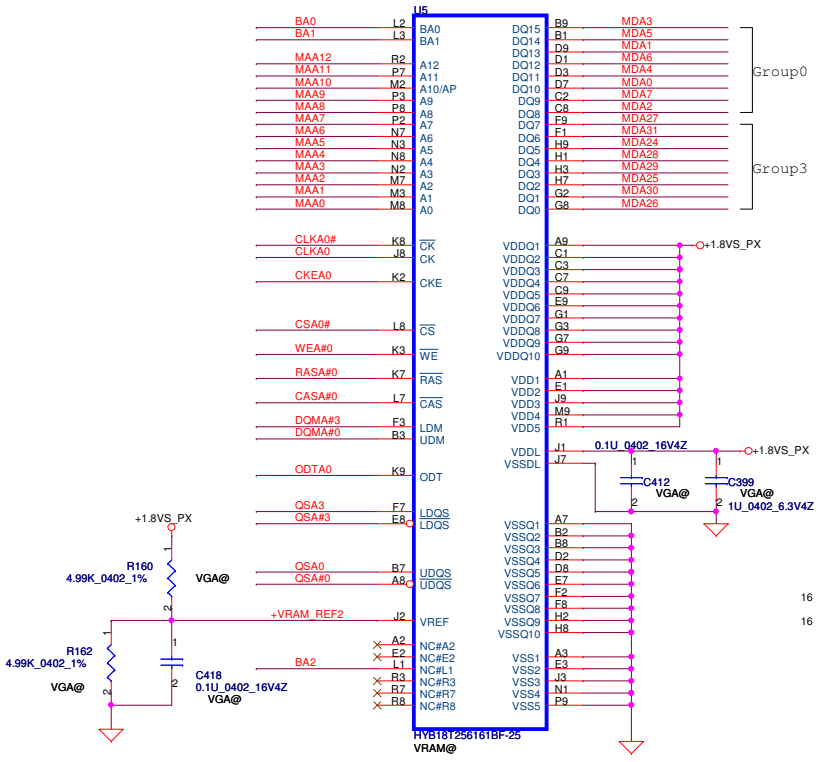
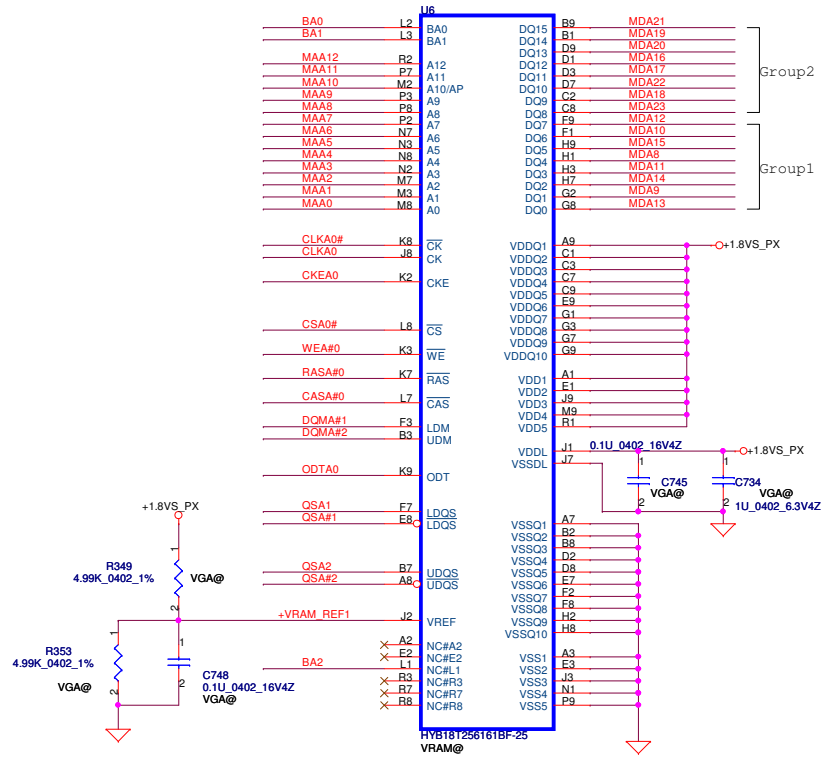


Spread spectrum

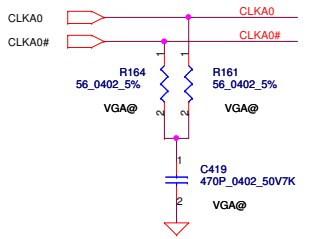
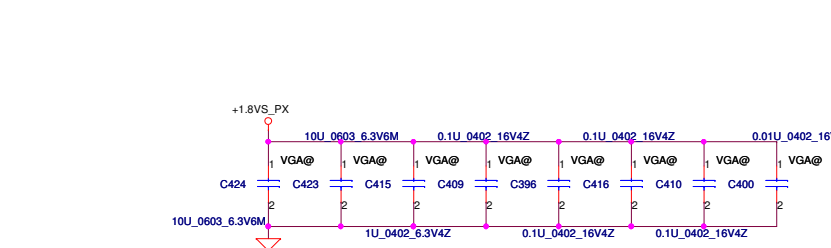
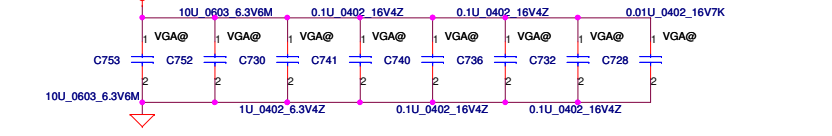


Use Delay 3.3V BUS (VDDR3) for GPIO/DCC Pull up to reduce Leakage to VDDR3 Bus.

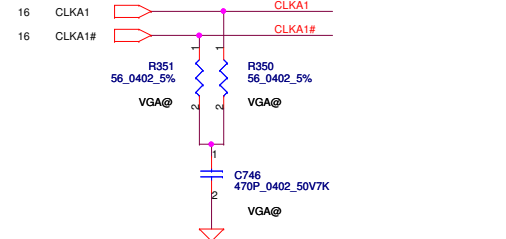
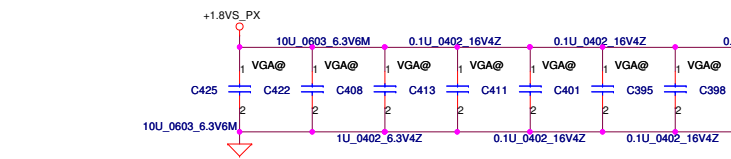
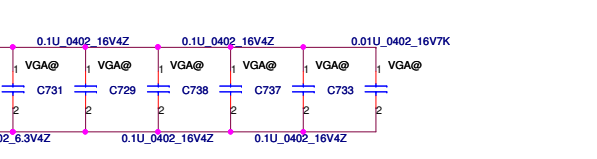
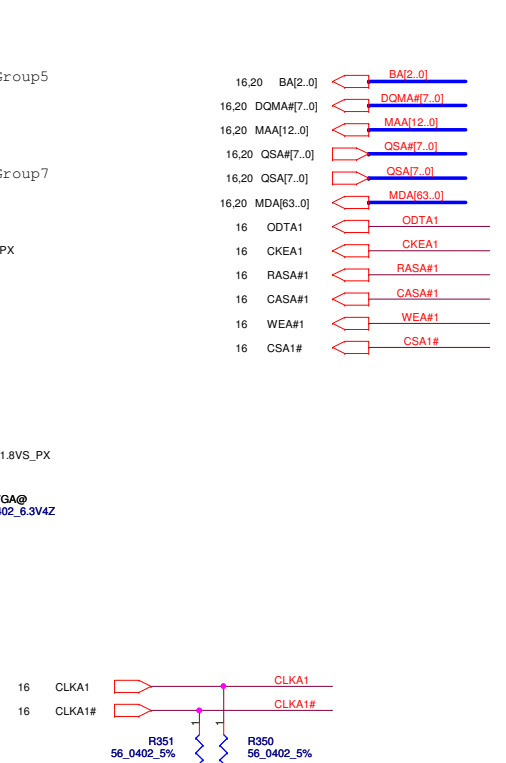
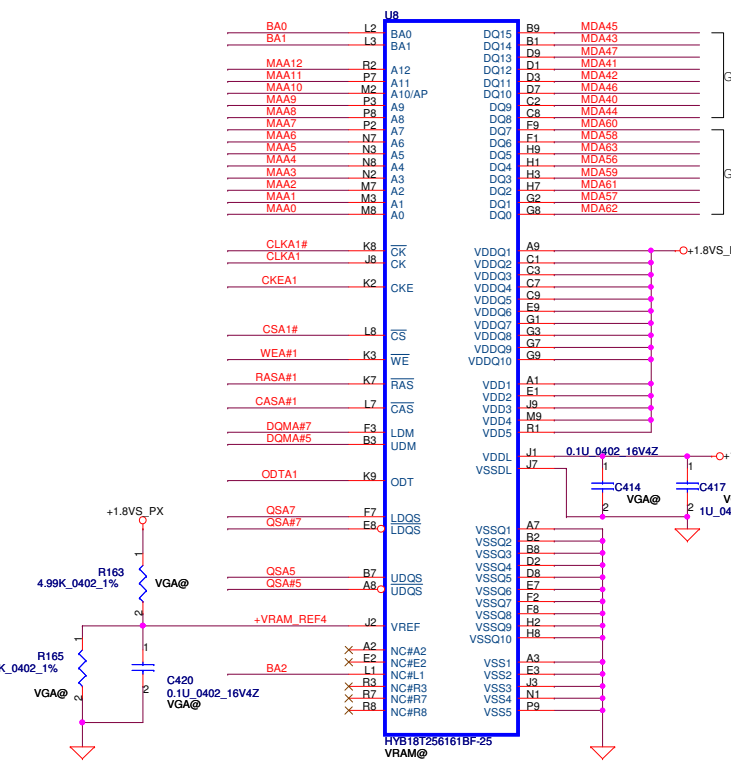
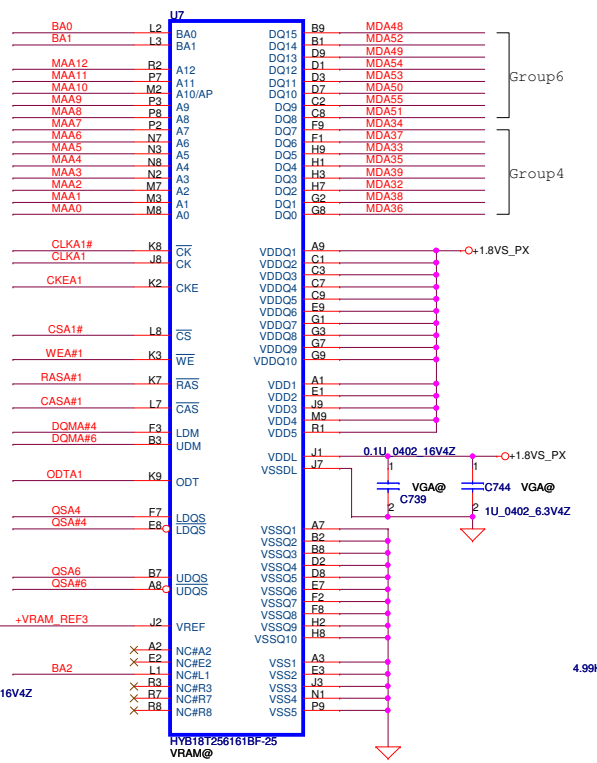
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Issued Date	2008/10/06	Deciphered Date	2009/10/06	M92 GND			
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				Date:	Thursday, February 19, 2009	Sheet	19 of 57



SA00002UH00 HYNIX S IC D2 64M16/500 HSPS1G63EPR-20L FBGA84
 SA00002MF00 Qimonda S IC D2 64M16/500 HYB181G161C2F-20
 SA00002MD00 Samsung S IC D2 64M16/500 K4N1G164Q0-HC20 FBGA84
 SA00003L000 Samsung S IC D2 64M16/500 K4N1G164Q0-HC20 FBGA 84P

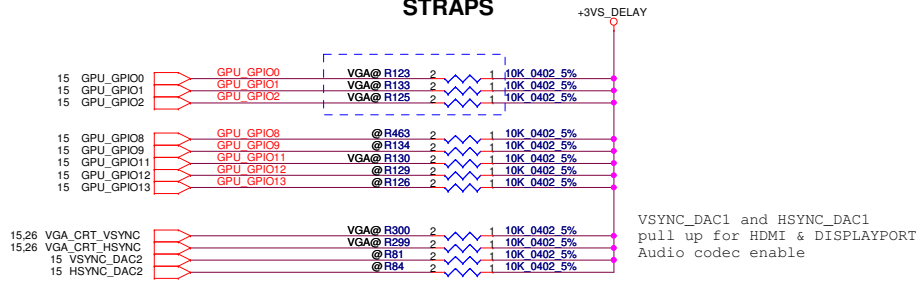


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				M92 VRAM	
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				Custom	KBLG0 LA-4921P
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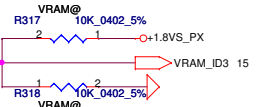
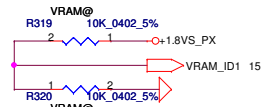
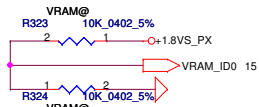
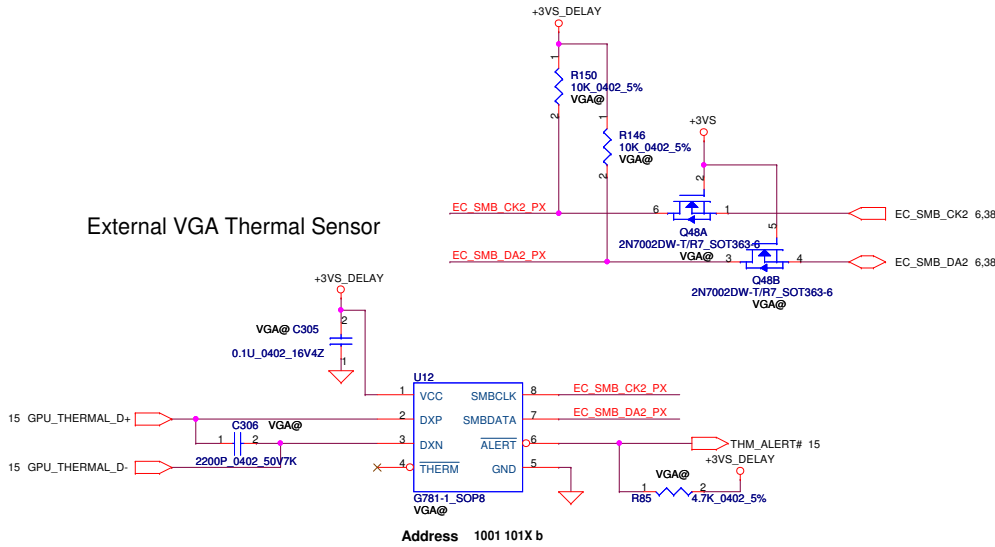


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				M92 VRAM	
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STRAPS



External VGA Thermal Sensor



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable	1 : PCIe bus Full Tx output swing 0 : PCIe bus 50% Tx output swing
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable	1 : Tx de-emphasis enabled 0 : Tx de-emphasis disabled
BIF_GEN2_EN_A	GPIO2	PCIe GNE2 ENABLED 0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0 (5.0 GT/s capability will be controlled by software)
VGA_DIS	GPIO9	VGA Disable determines whether or not the card will be recognized as the system's VGA controller	0 : VGA Controller capacity enabled 1 : The device will not be recognized as the system's VGA controller
CONFIG(20)	GPIO[13:11]	Size of the primary memory apertures	0 0 1
VIP_DEVICE_STRAP_EN	V2SYNC		0
RESERVED	H2SYNC		0
AUD[1]	HSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected	11
AUD[0]	VSYSN	1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	
RESERVED	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB		0: Disable external BIOS ROM device 1: Enable external BIOS ROM device
CCBPASS	GENERICC	IGNORE VIP DEVICE STRAPS	0
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0

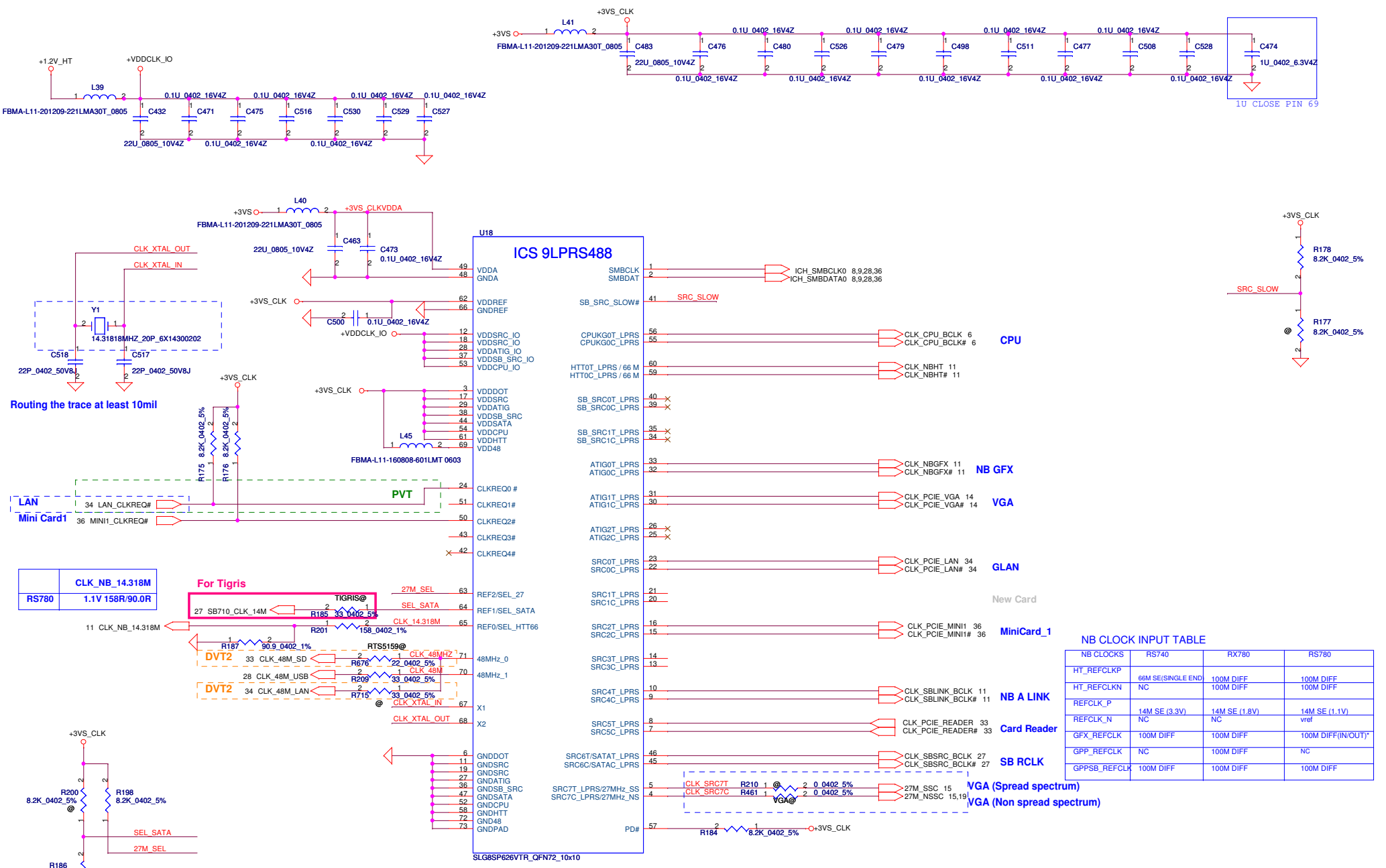
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO_28_TDO	GPIO21_BB_EN

STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 3,2,1,0
VRAM_ID[3:0]	DVPDATA (23,22,21,20)	M92-M2 XT	JV40-PU_KBLG0	512M(x4)	Samsung 64Mx16 1.8V (Q-die)	SA00002MD00	0 0 0 0
			JV40-PU_KBLG0	512M(x4)	Hynix 64Mx16 1.8V	SA00002UH20	0 0 0 1
			JV40-PU_KBLG0	512M(x4)	Qimonda 64Mx16 1.8V	SA00002MF00 PVT	0 0 1 0
			JV40-PU_KBLG0	512M(x4)	Samsung 64Mx16 1.8V (E-die)	SA000031O10	0 1 0 0

Security Classification	Compal Secret Data		Title	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	M92 Strap
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1st (SILEGO) : SA00001Z310 S IC SGL8SP626VTR QFN 72P CLK GEN
 2nd (ICS) : SA000023H10 S IC ICS9LPRS488CKLFT MLF 72P CLK GEN

NB CLOCK INPUT TABLE

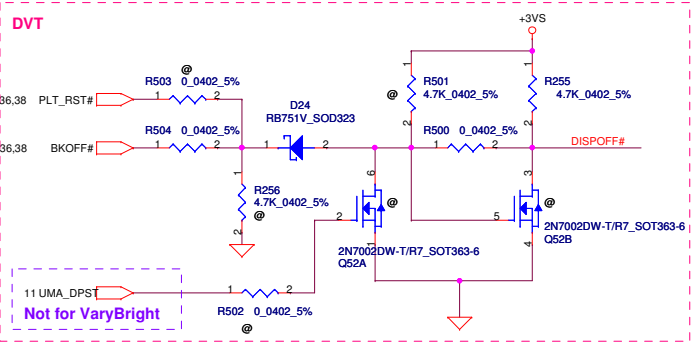
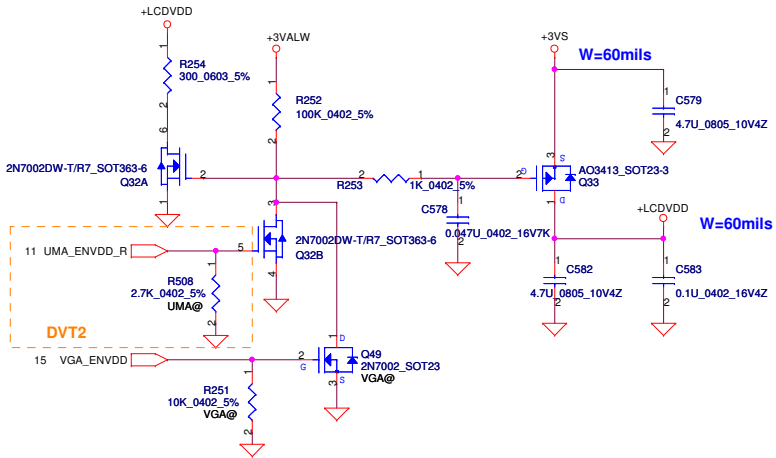
NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	68M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V) vref
REFCLK_N	NC	NC	NC
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF('N/OUT')
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

SEL_HTT66	1	single-ended 66MHz HTT output
	0*	differential 100MHz HTT output
SEL_SATA	1*	NON SPREAD 100M. SATA SRC6 output
	0	SPREAD 100M. SATA SRC6 output

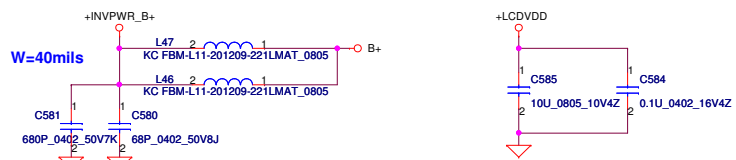
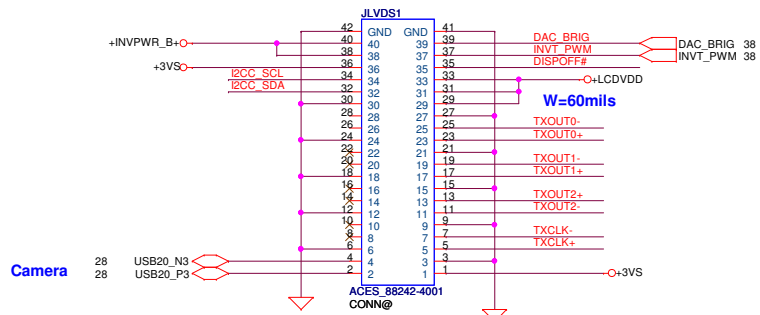
27M_SEL	1*	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC 7 output

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				Clock generator		
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				Custom	KBLG0 LA-4921P	0.1
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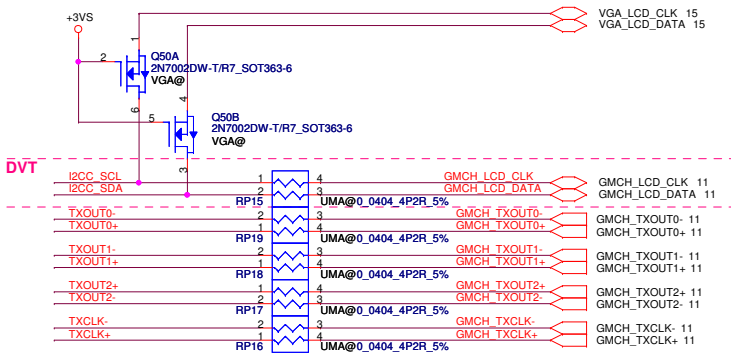
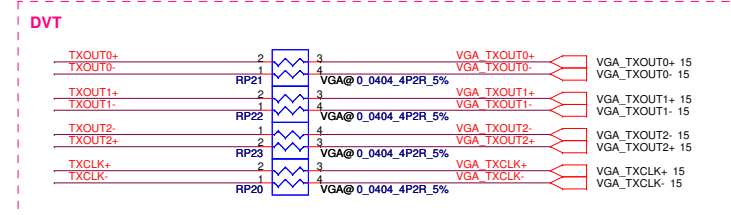
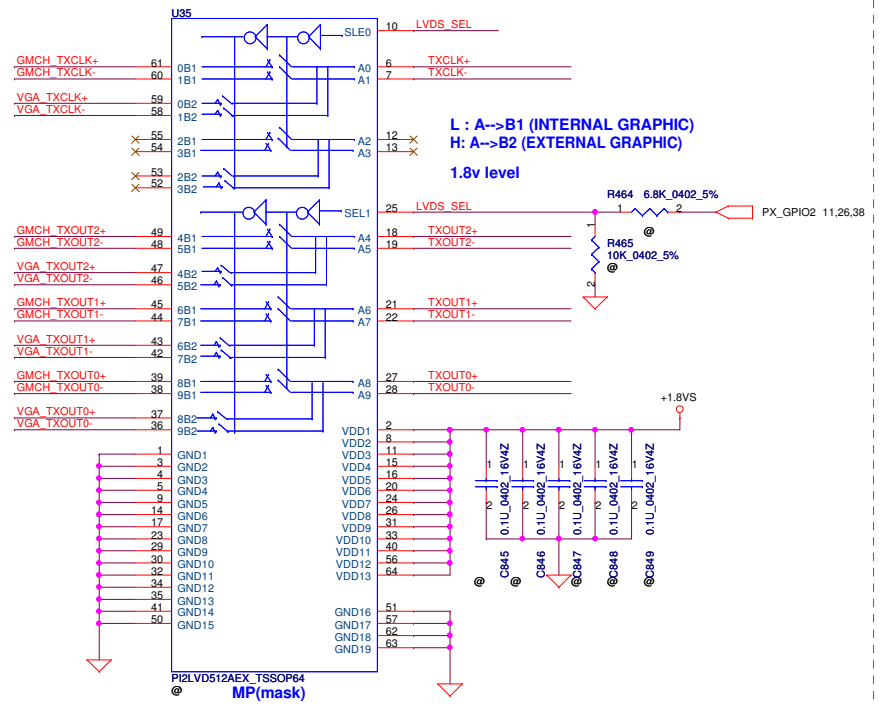
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.

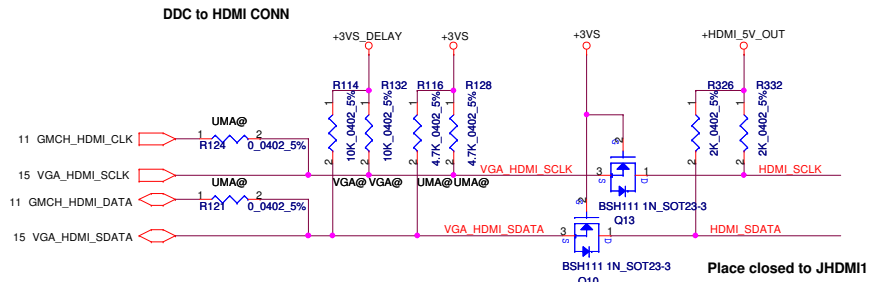


DVT

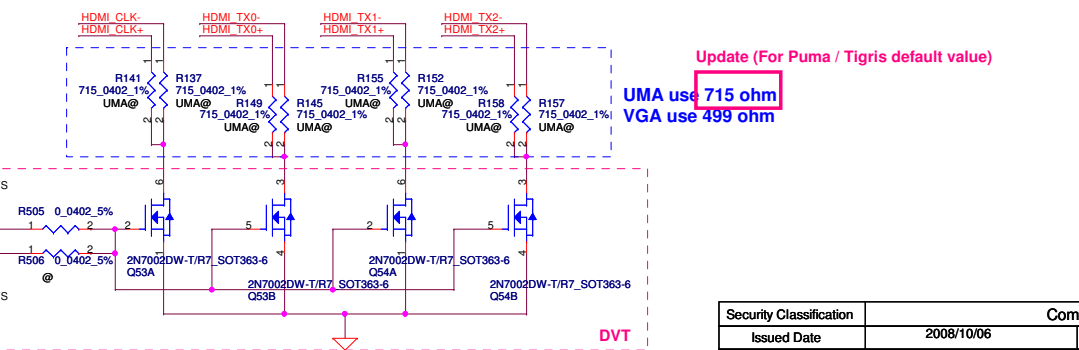
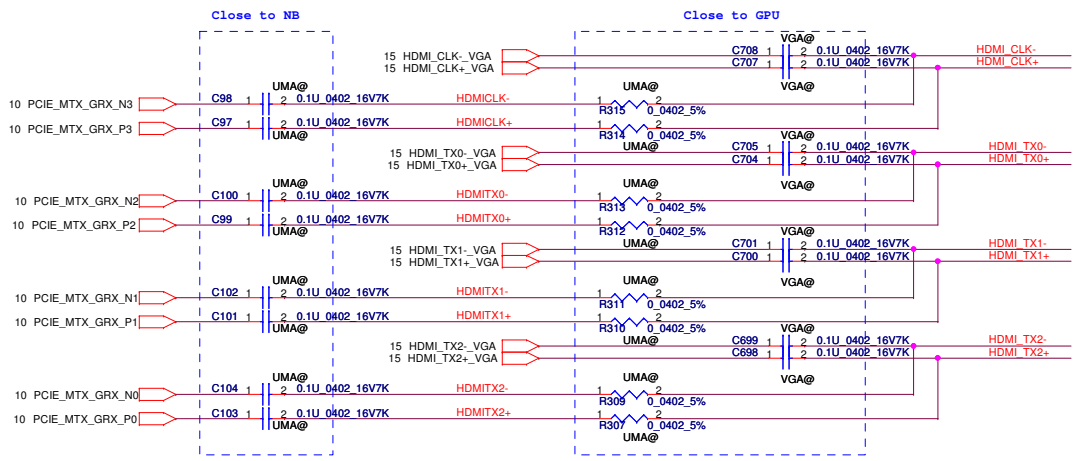
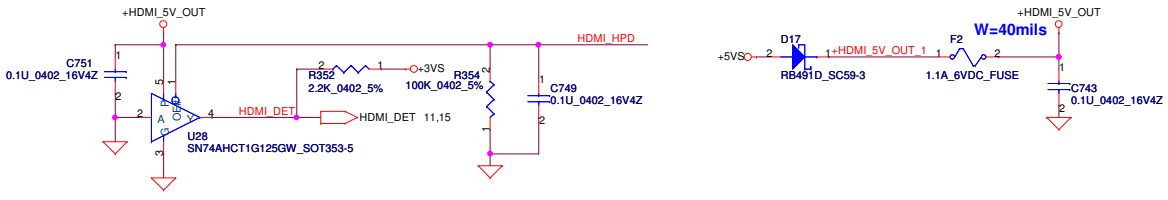
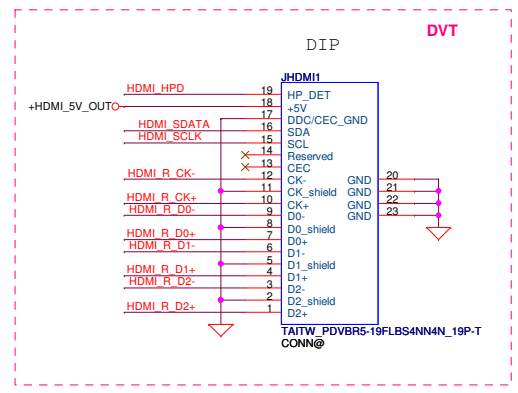


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				LVDS Connector	
Size	Document Number	Date		Rev	
B	KBLG0 LA-4921P	Wednesday, March 11, 2009		0.1	
				Sheet 24 of 57	

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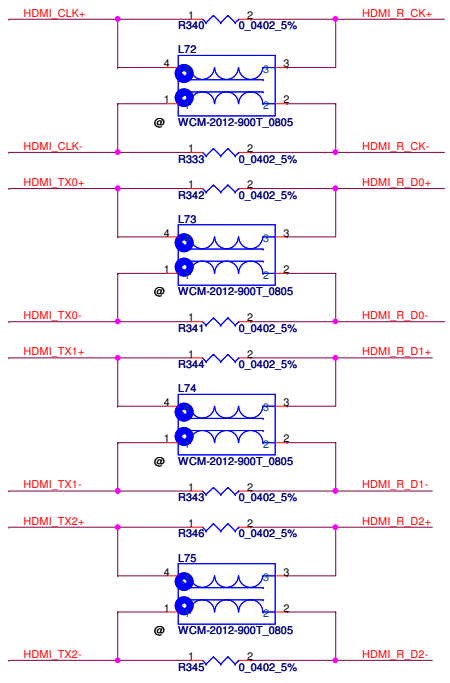


Place closed to JHDMI1



Update (For Puma / Tigris default value)

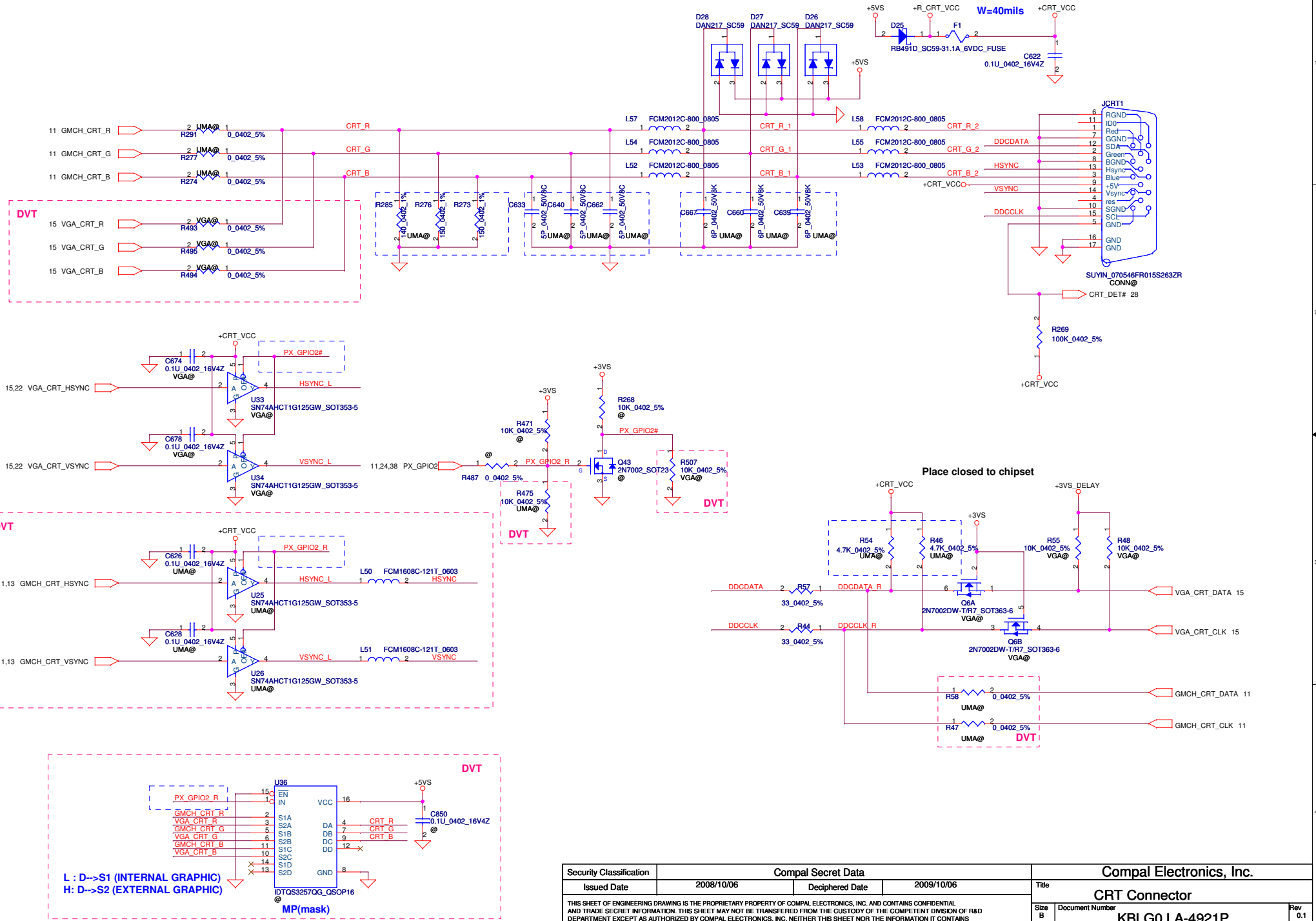
UMA use 715 ohm
VGA use 499 ohm



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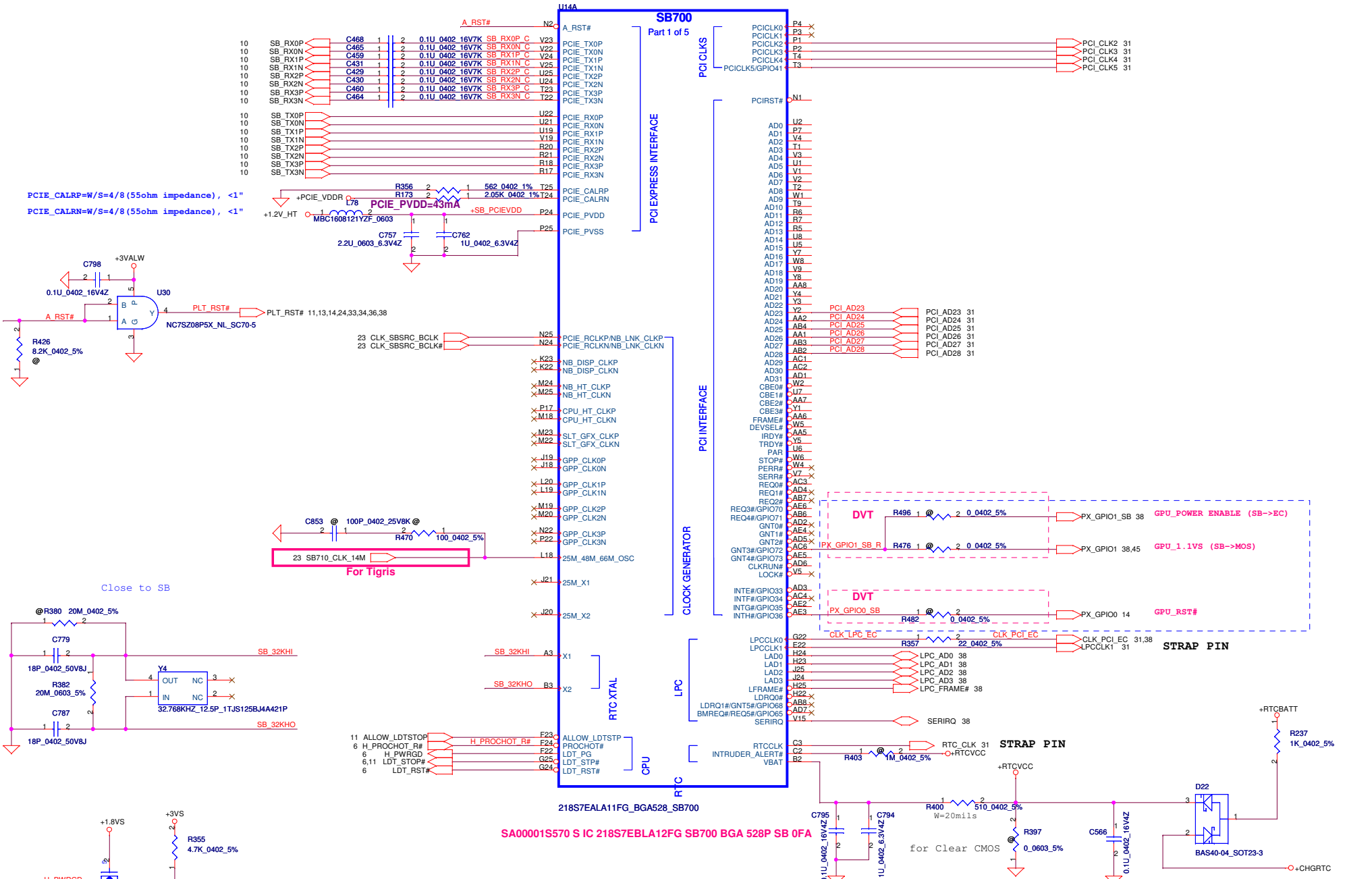
Compal Electronics, Inc.			
Title HDMI Connector			
Size	Document Number	Rev	
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CRT CONNECTOR



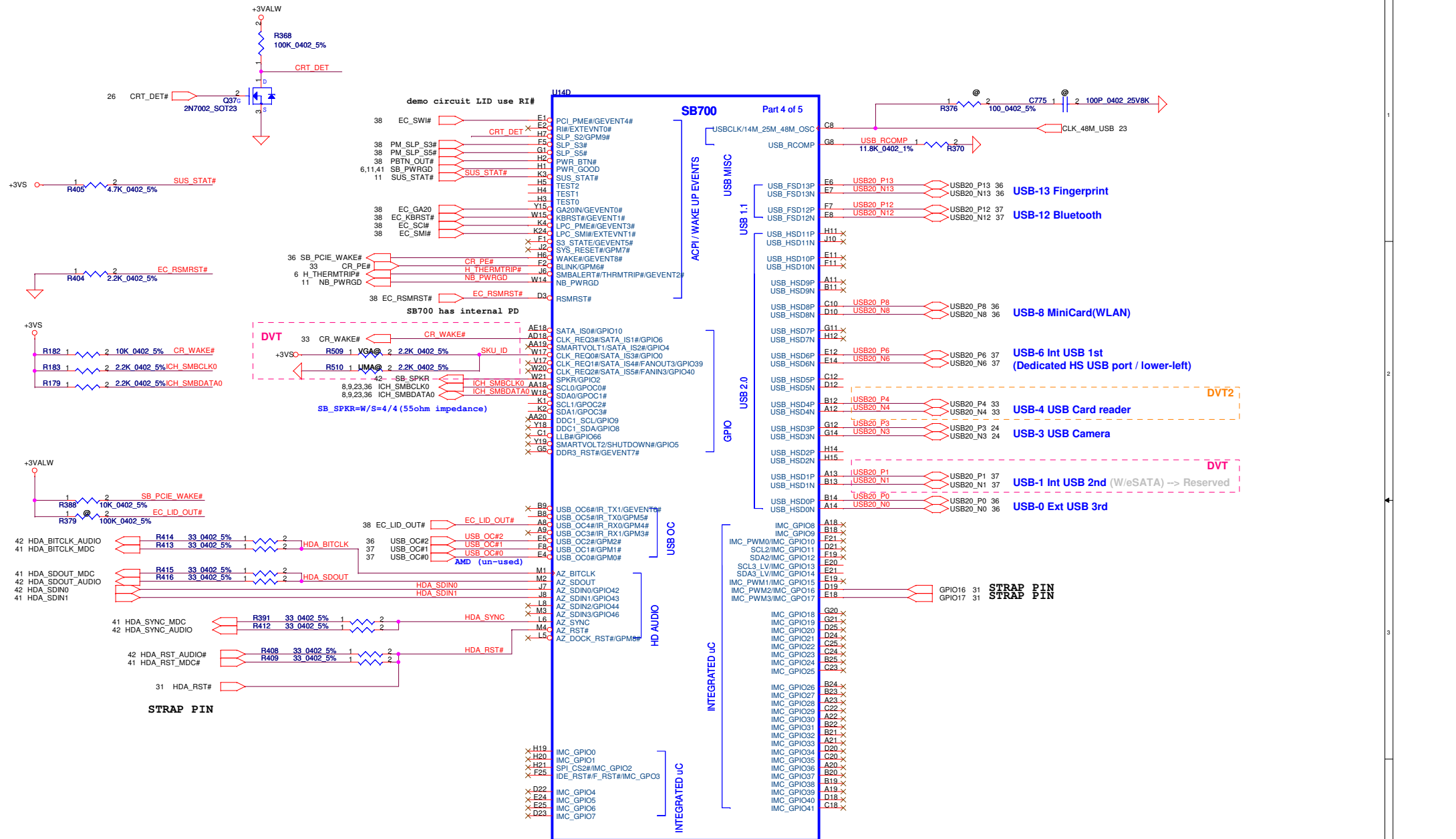
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CRT Connector			
Size B	Document Number	Rev	
	KBLG0 LA-4921P	0.1	
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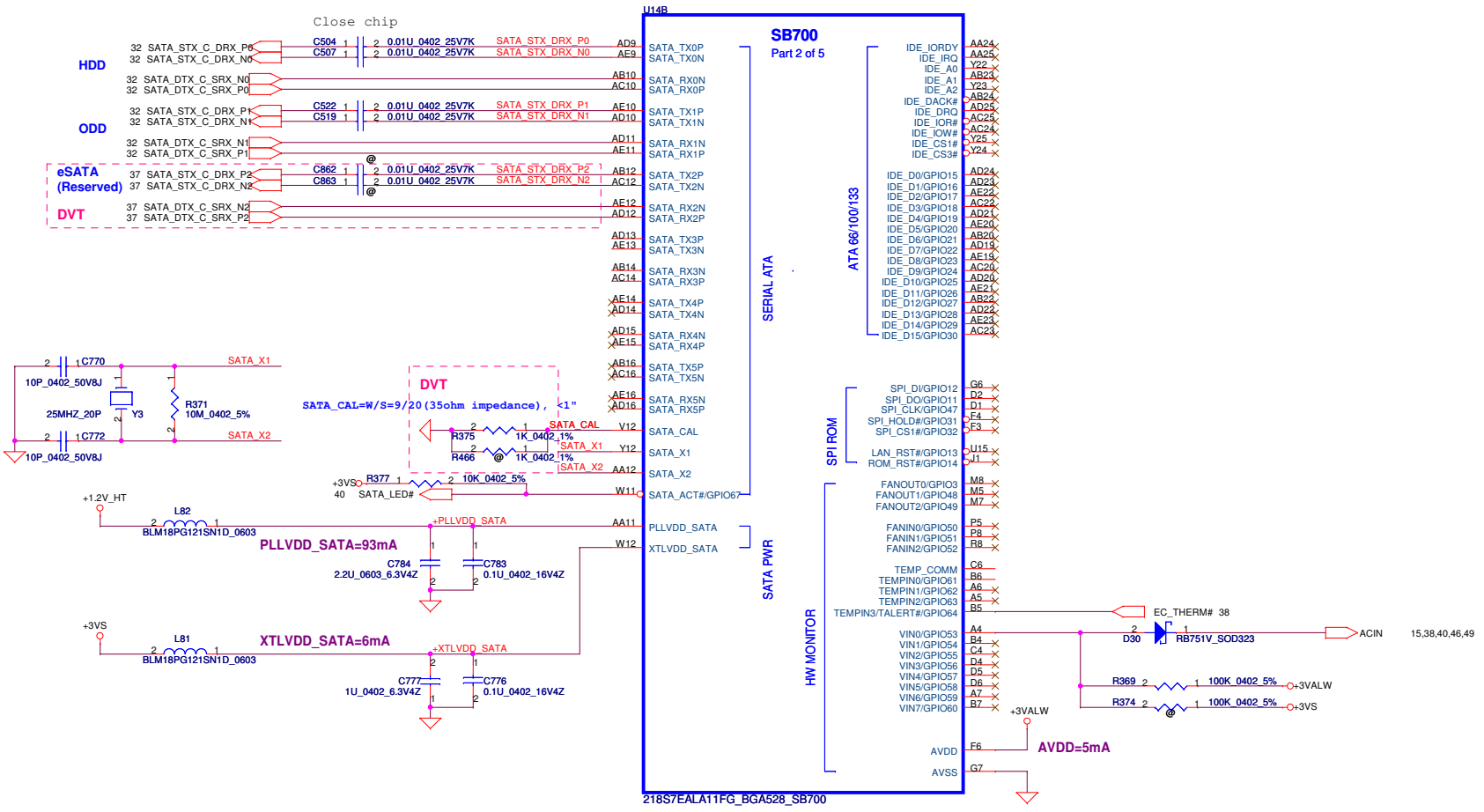
Security Classification	Compal Secret Data		Title	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	SB700-PCIE/PCI/ACPI/LPC/RTC
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level shift to ISL6265



21857/EAL11FG_BGA528_SB700

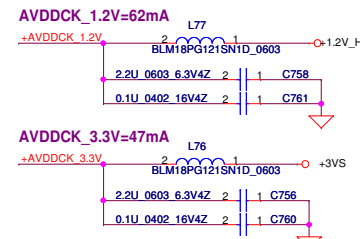
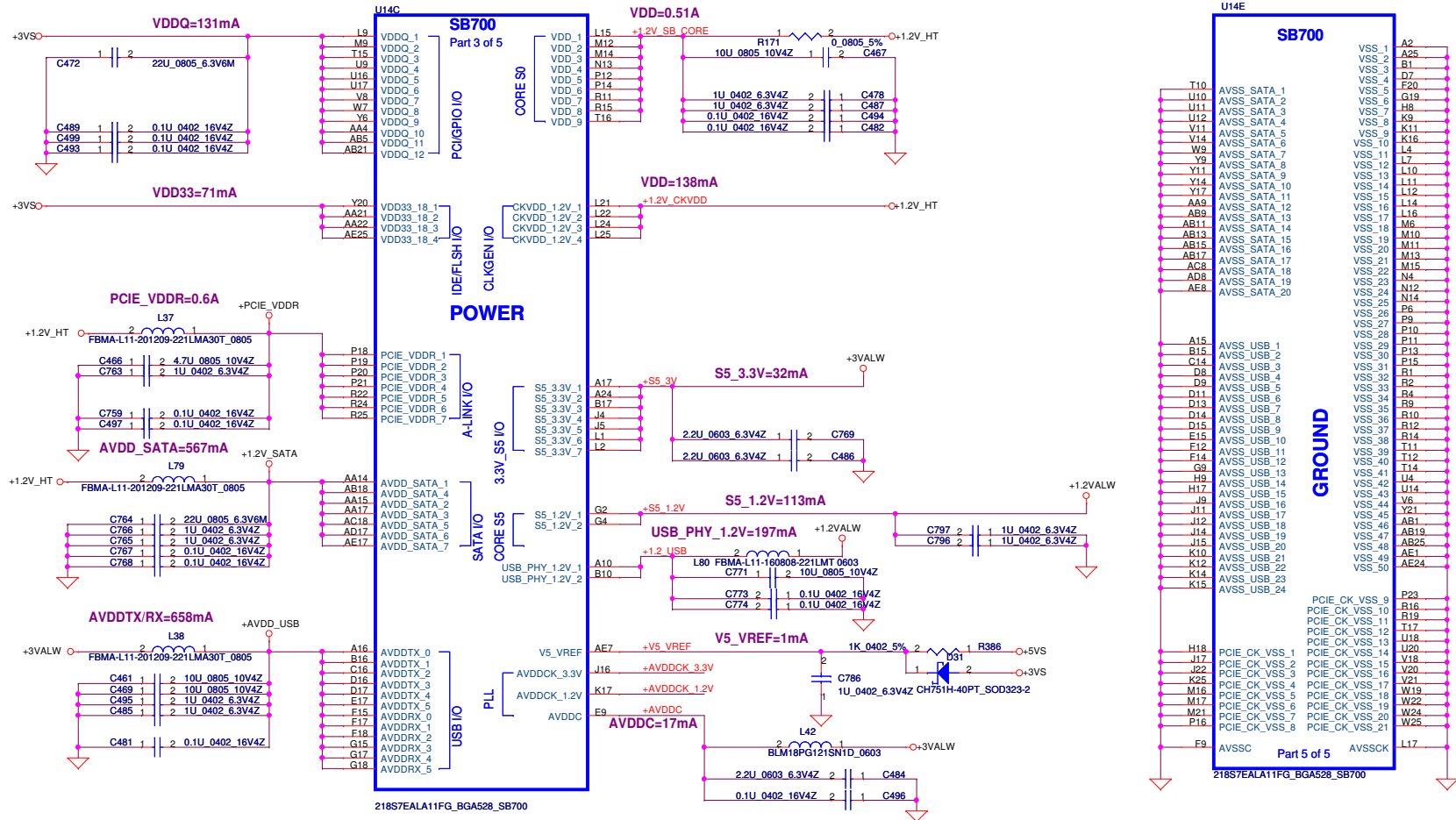
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Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title	
				SB700 USB/HD audio	
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Compal Electronics, Inc.		
Title		
SB700 SATA/IDE/SPI		
Size	Document Number	Rev
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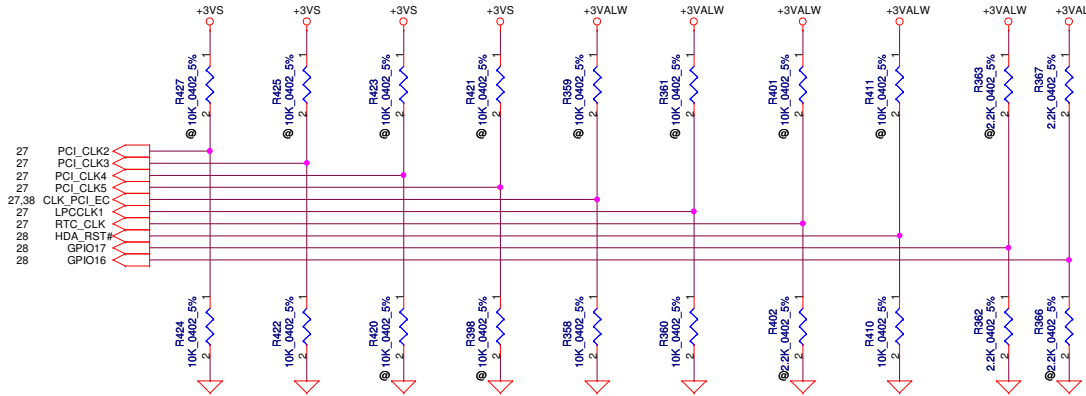
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Compal Electronics, Inc.		
Title		
SB700 power/GND		
Size	Document Number	Rev
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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

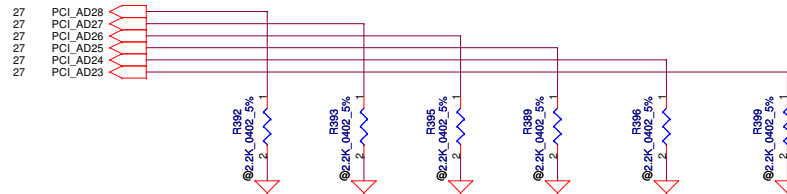
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default L,NC) LL = FWH ROM	



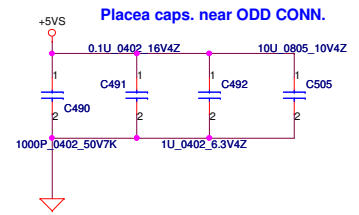
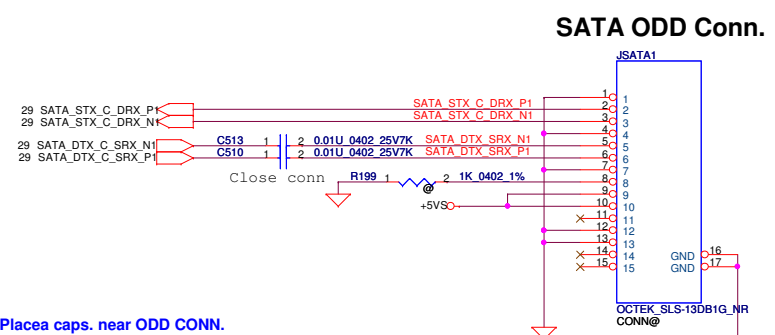
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

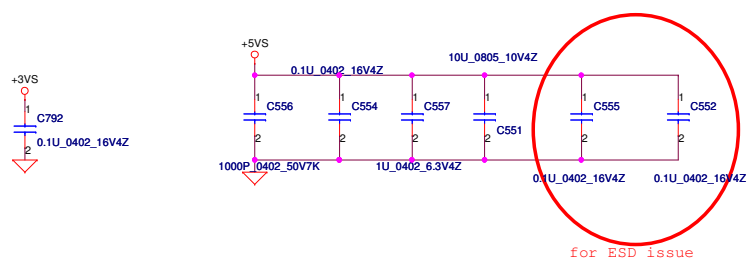
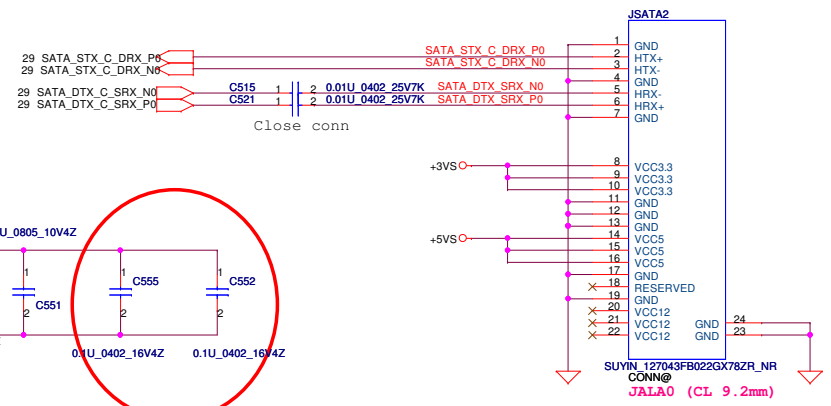
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



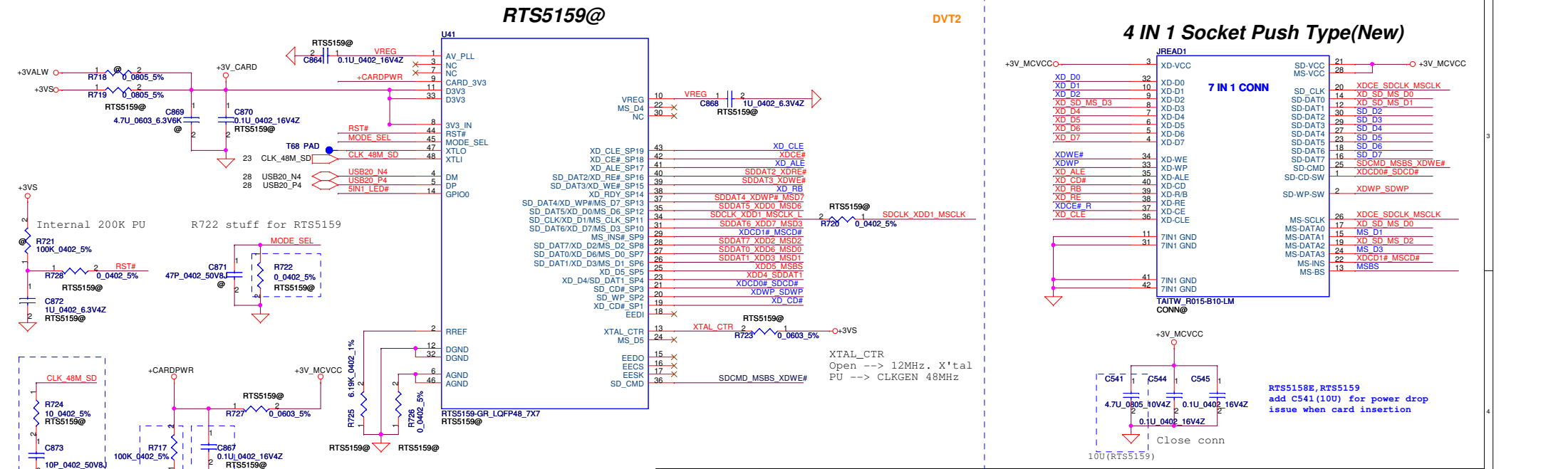
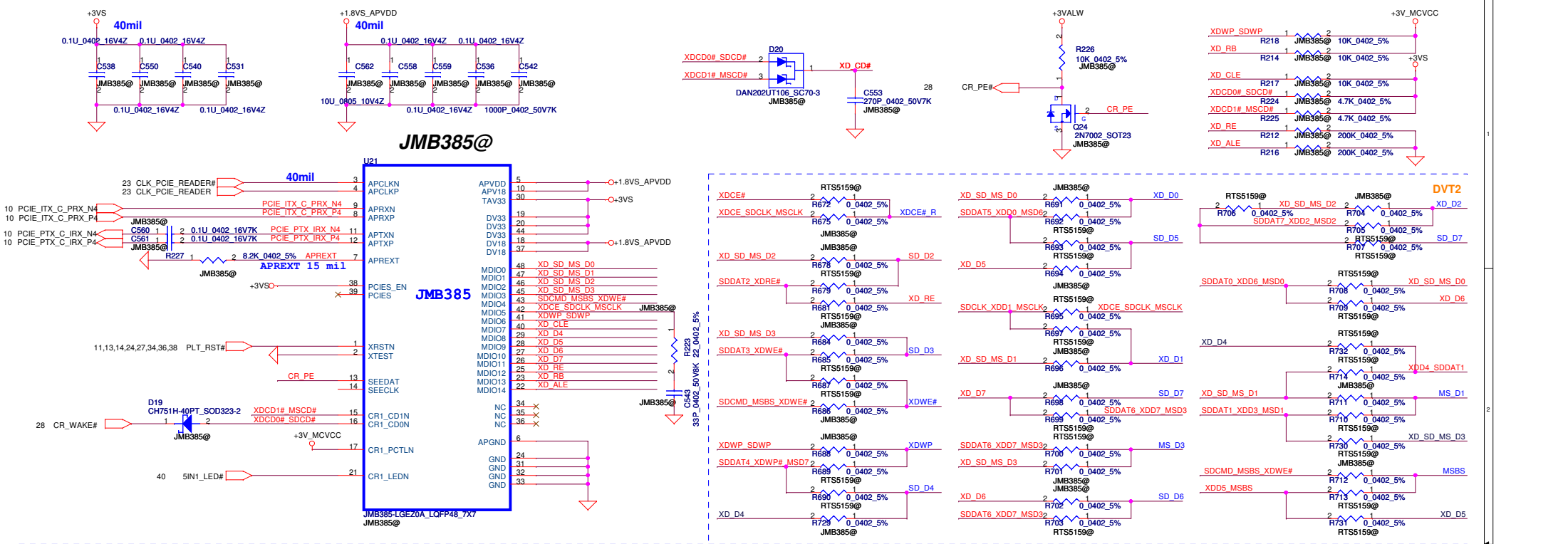
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Issued Date	2008/10/06	Deciphered Date	2009/10/06	
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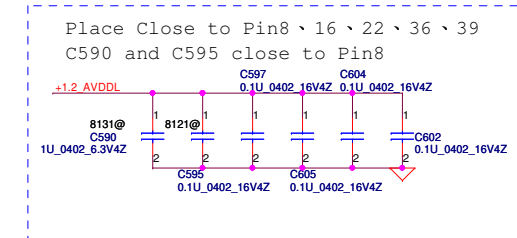
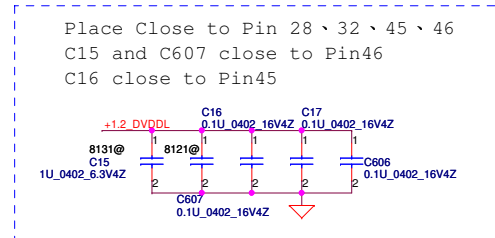
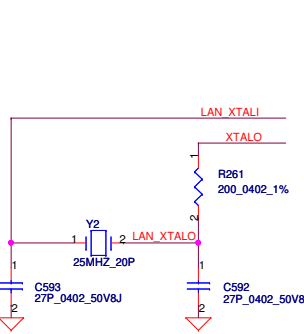
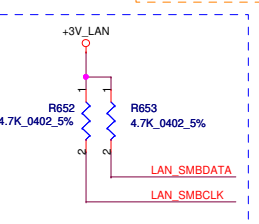
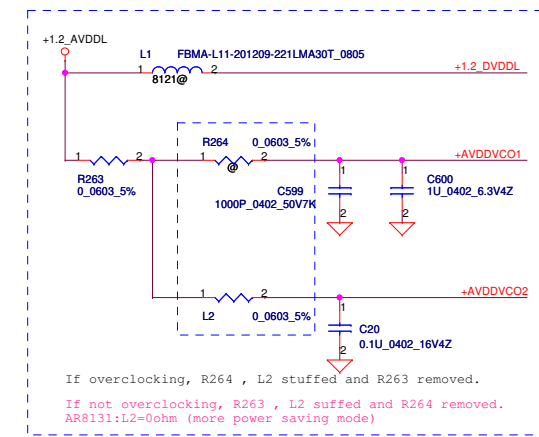
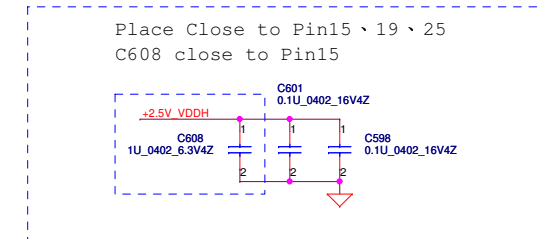
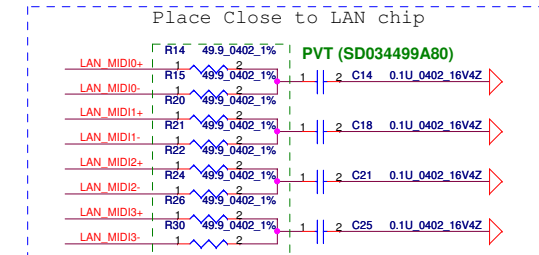
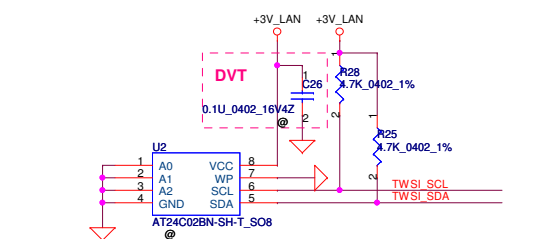
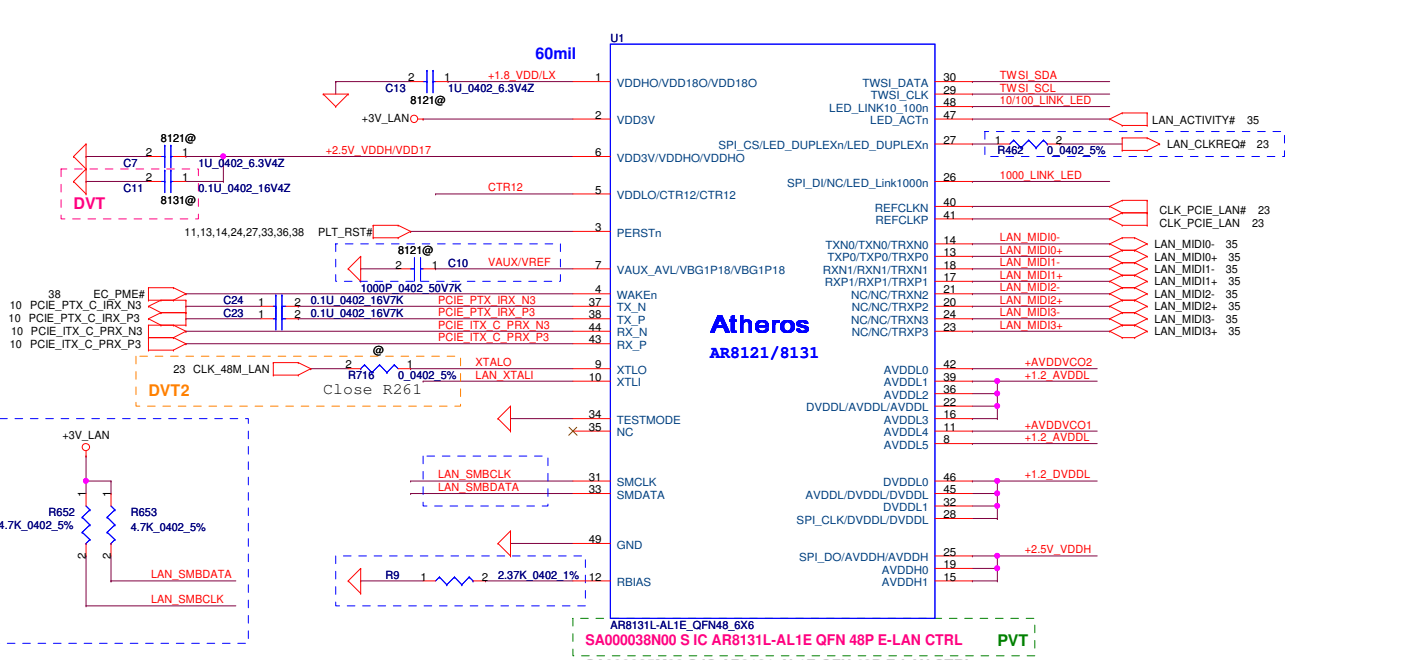
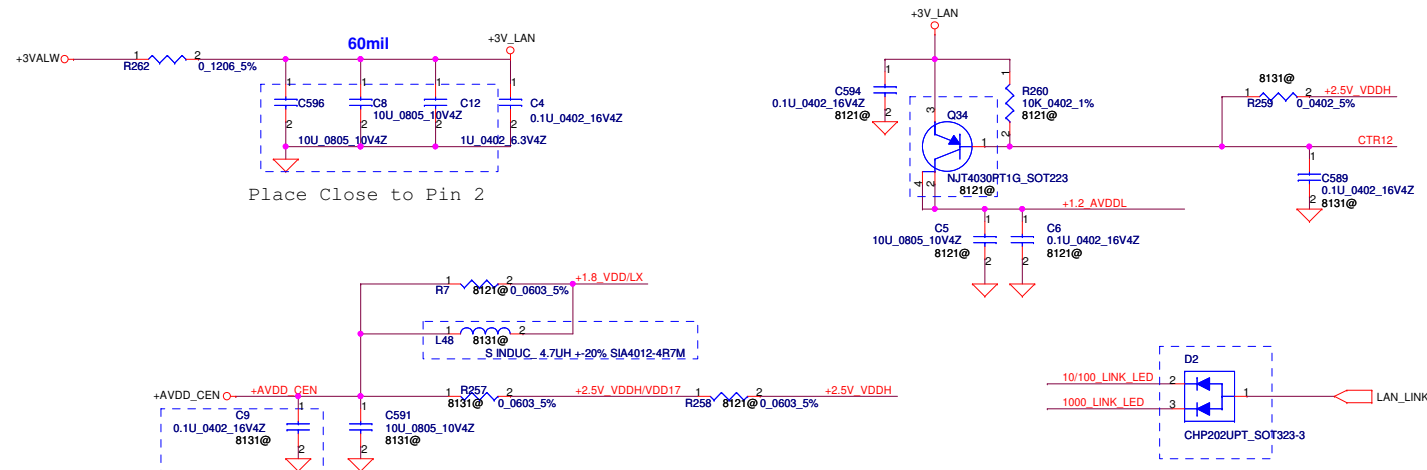
SATA HDD Conn.



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Issued Date	2008/10/06	Deciphered Date	2009/10/06	HDD & ODD Connector	
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Issued Date	2008/10/06	Deciphered Date	2009/10/06	RTS5159 / (JMB385) card reader
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<p>Issued Date: 2008/10/06</p>			<p>Rev: 0.1</p>	
<p>Deciphered Date: 2009/10/06</p>			<p>Date: Thursday, February 19, 2009</p>	
<p>Document Number: KBLG0 LA-4921P</p>			<p>Sheet: 33 of 57</p>	



Atheros
AR8121/8131

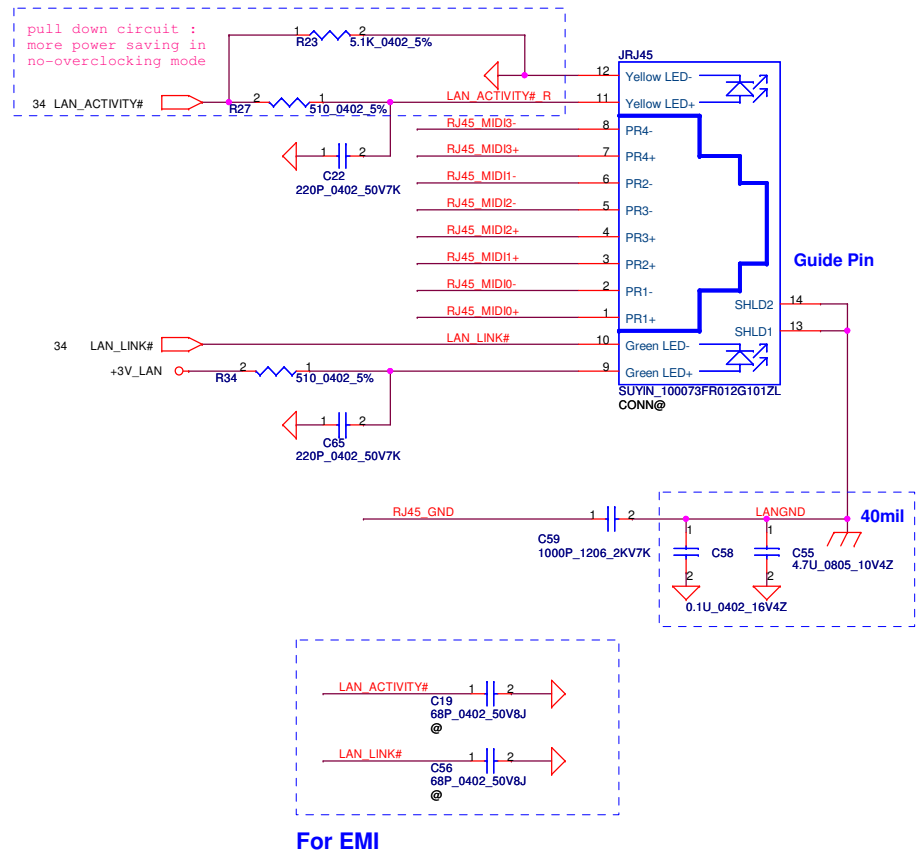
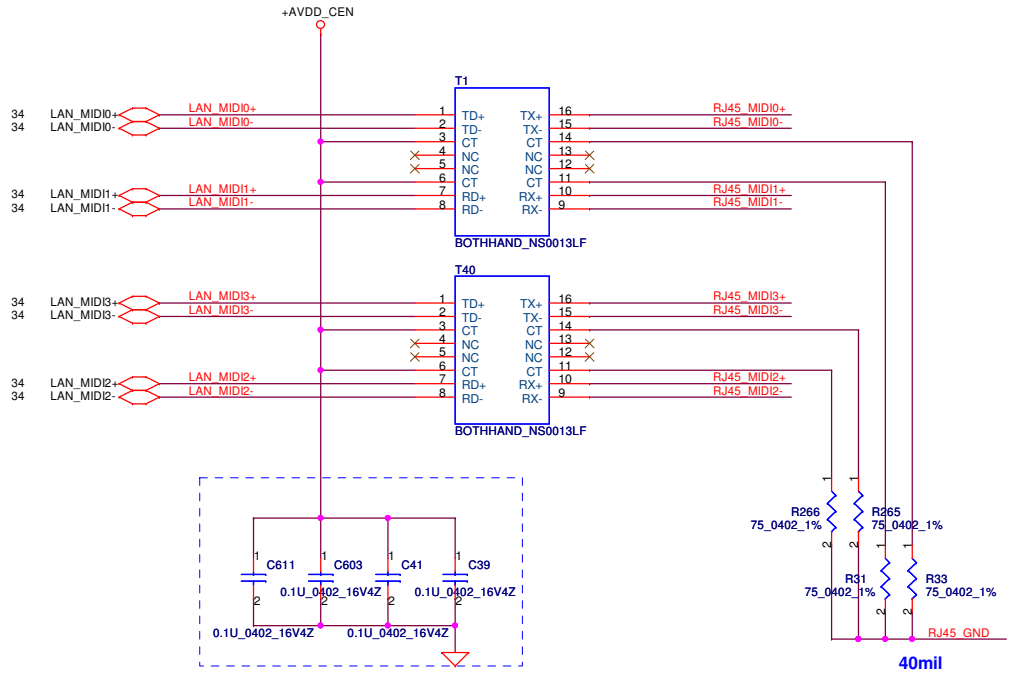
AR8131L-AL1E-QFN48_6X6
SA000038N00 S IC AR8131L-AL1E-QFN 48P E-LAN CTRL PVT
SA000025M00 S IC AR8121T-AL1E-QFN 48P E-LAN CTRL

Place Close to Pin 28、32、45、46
C15 and C607 close to Pin46
C16 close to Pin45

Place Close to Pin8、16、22、36、39
C590 and C595 close to Pin8

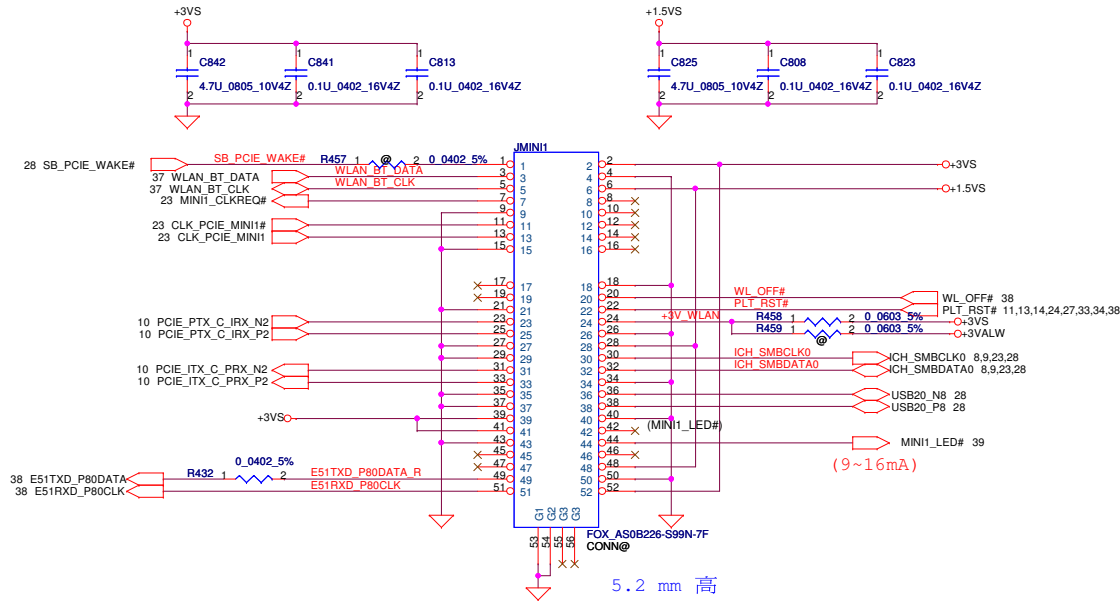
If overclocking, R264, L2 stuffed and R263 removed.
If not overclocking, R263, L2 stuffed and R264 removed.
AR8131:L2=0ohm (more power saving mode)

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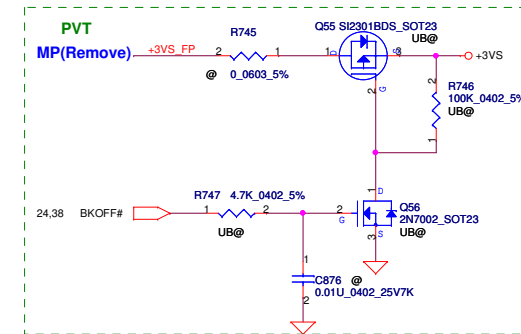
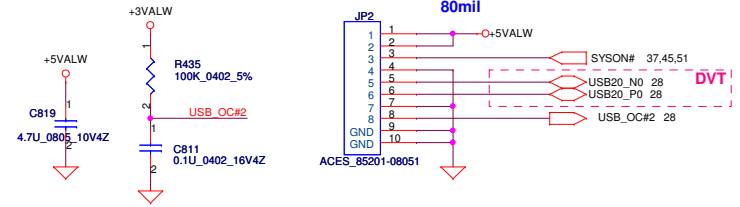
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title	
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				KBLG0 LA-4921P	
				Date:	Thursday, February 19, 2009
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For Wireless LAN

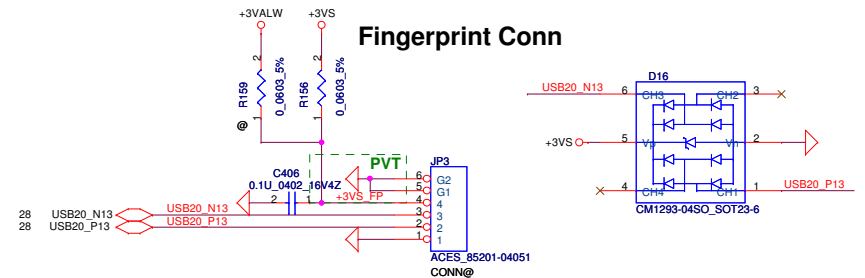


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	Normal
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

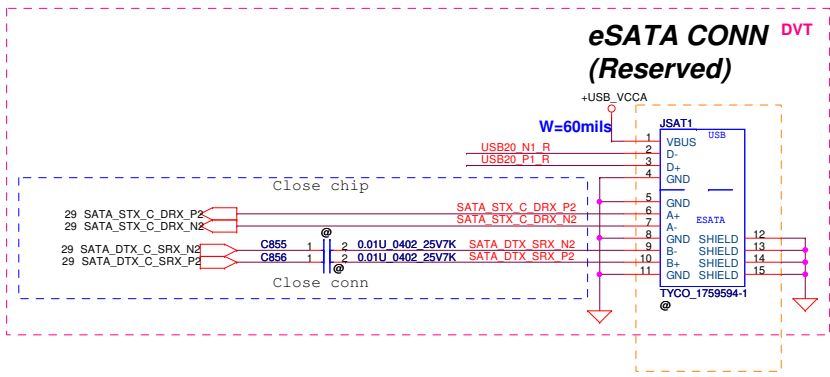
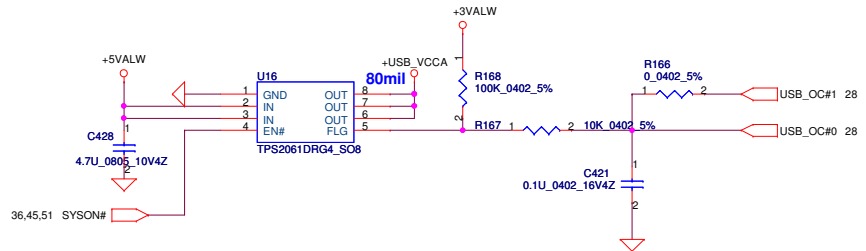
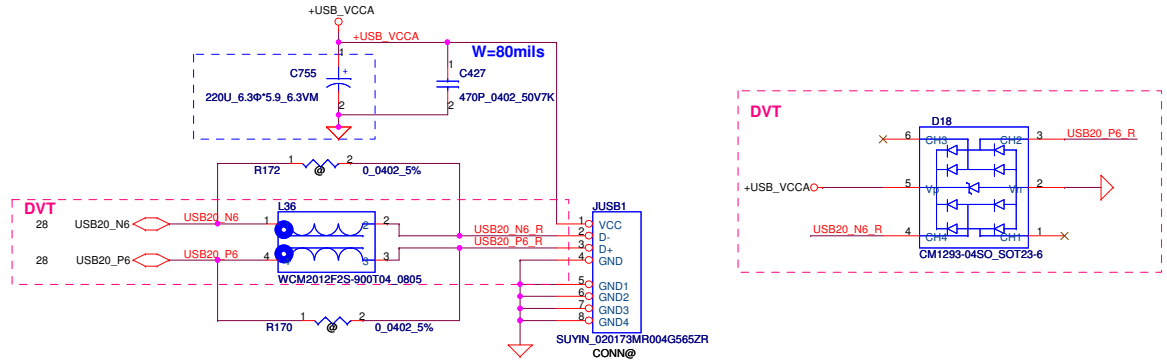
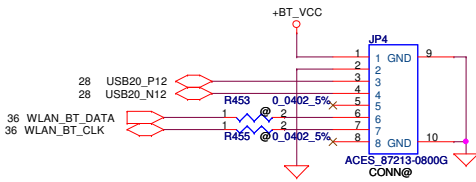
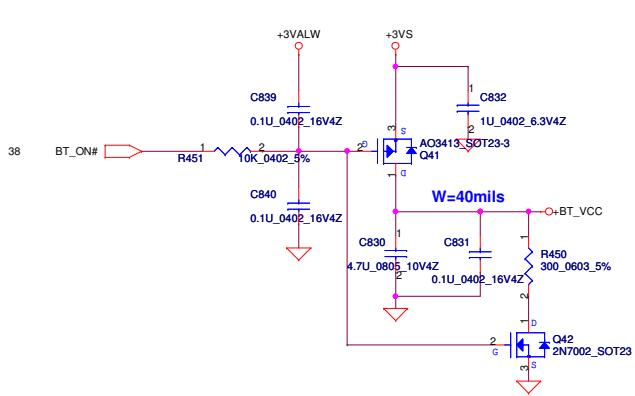
To USB/B Connector



Fingerprint Conn

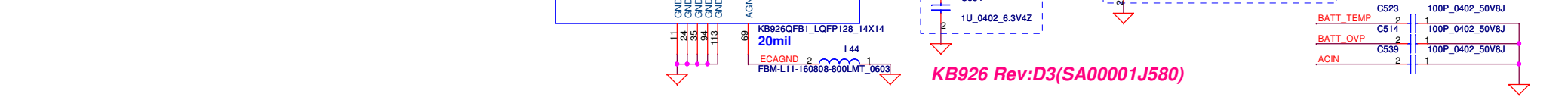
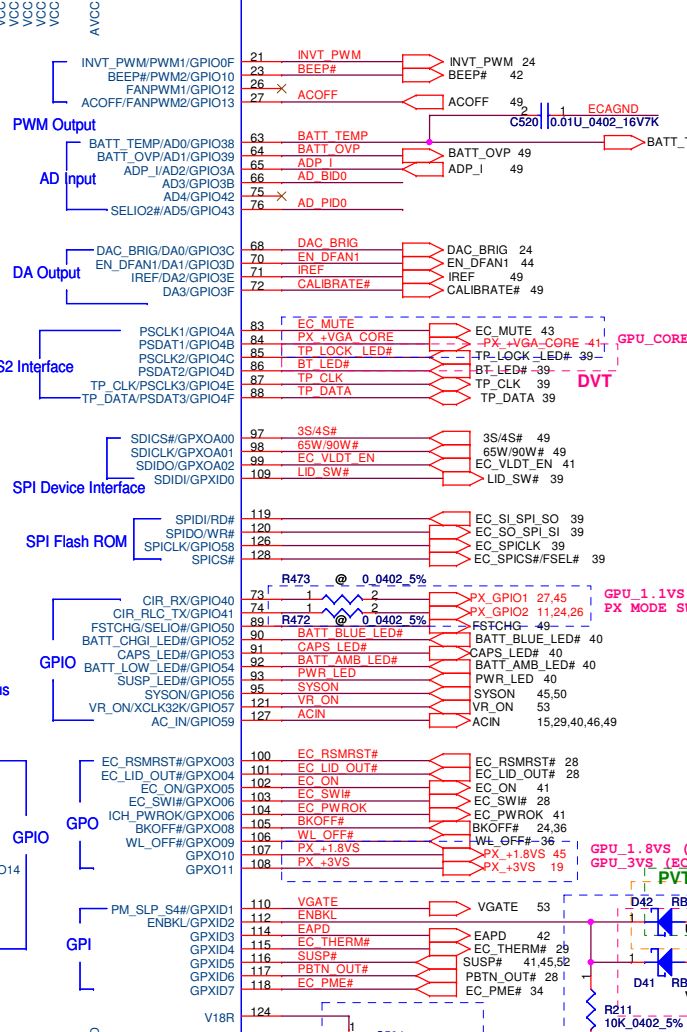
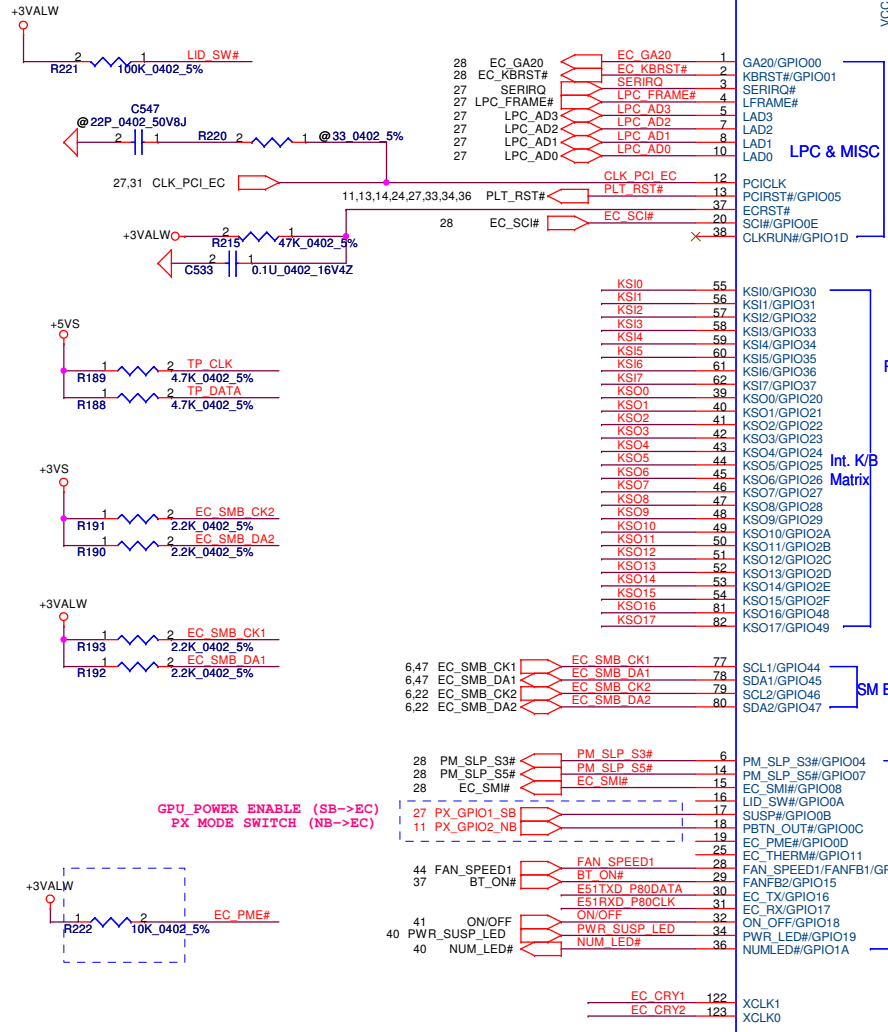
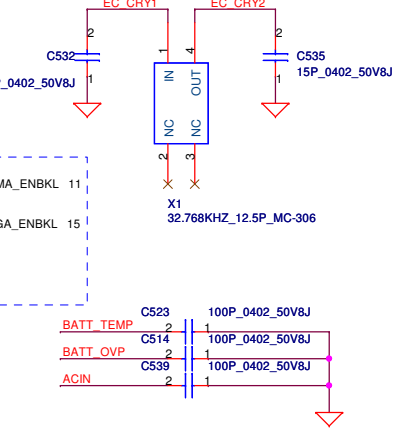
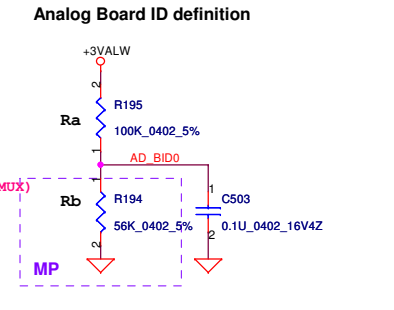
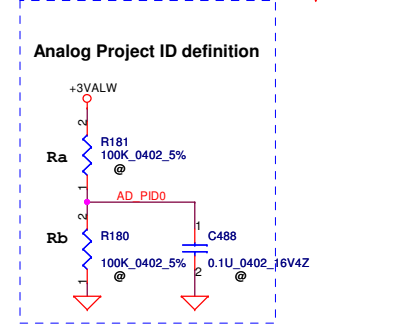
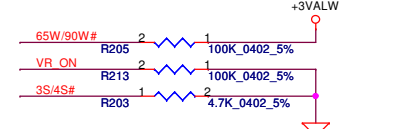
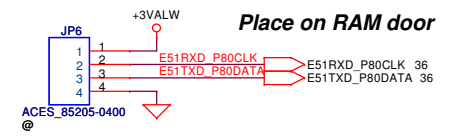
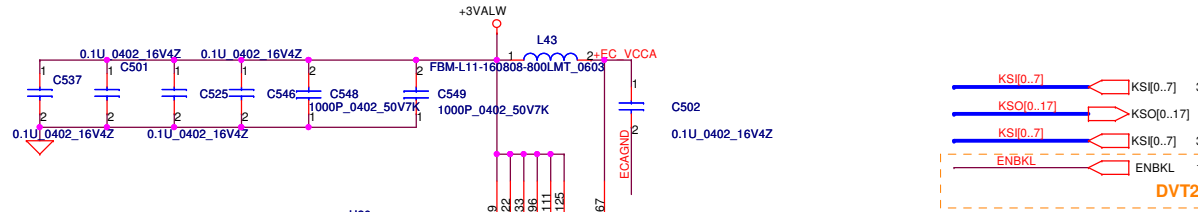


Bluetooth Conn.



DVT2
(PCB footprint : TYCO_1909574-1_11P-T)

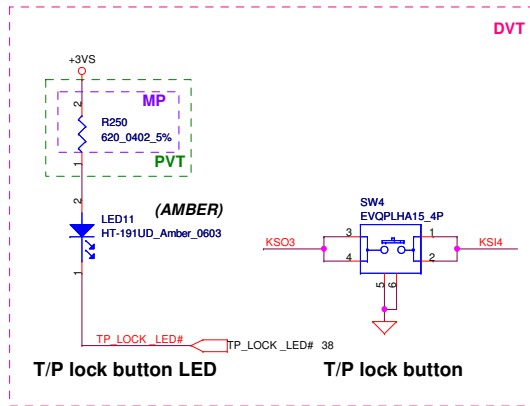
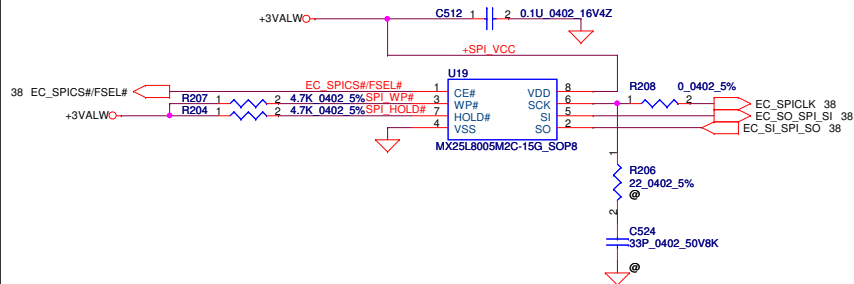
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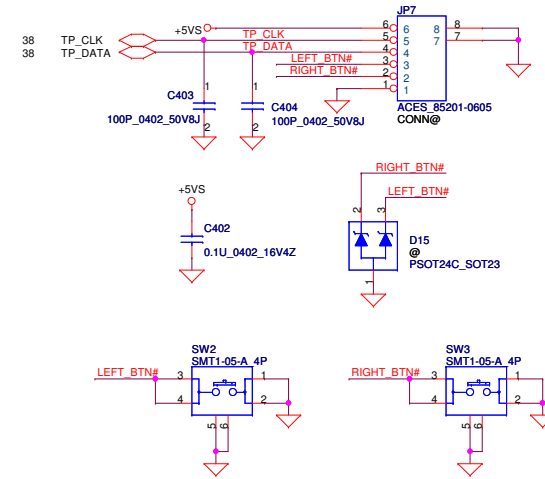
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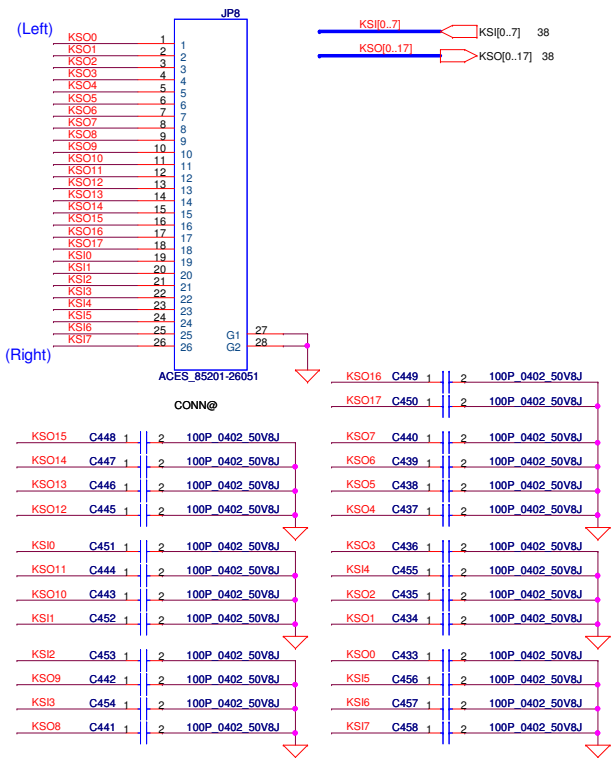
BIOS(SYS / EC / VGA)



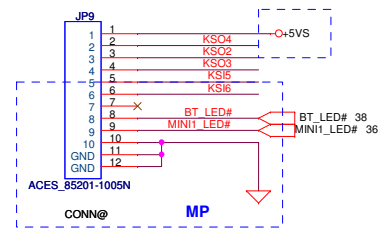
To TP/B Conn.



INT_KBD Conn.

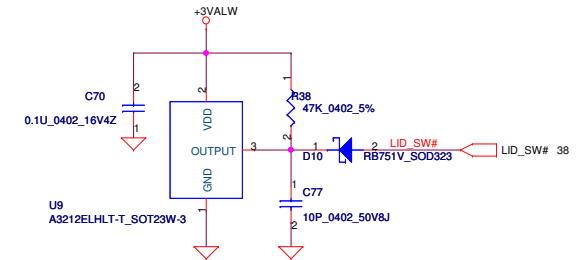


To FUN/B Conn (10PIN)

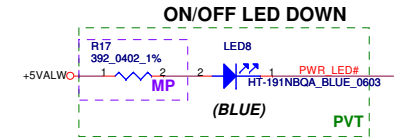
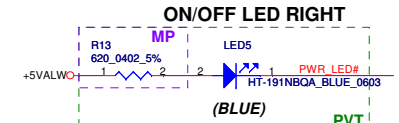
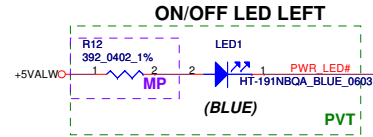
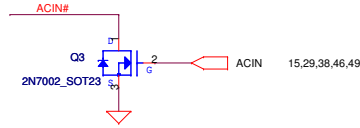
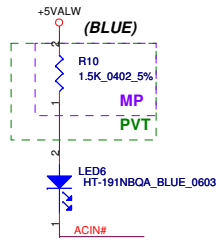
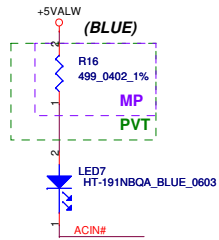


	KSO4	KSO2	KSO3
KSI5	WL_BTN#	Volume Down	Back Up
KSI6	BT_BTN#	Volume Up	Program (KBLG0) Battery (KALG0)
KSI4			T/P lock

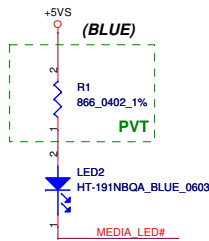
Lid Switch (Hall Effect Switch)



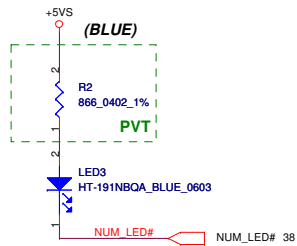
Enlightener LED



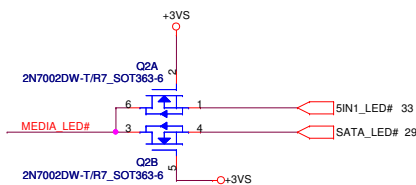
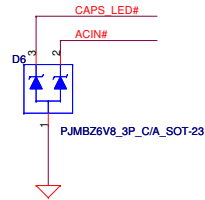
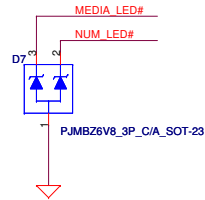
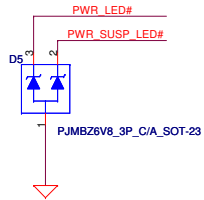
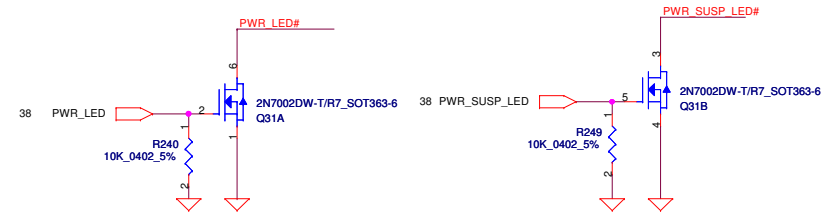
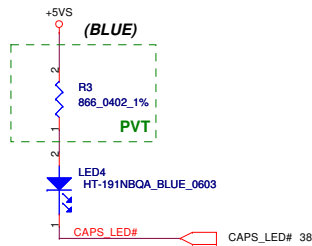
MEDIA_LED



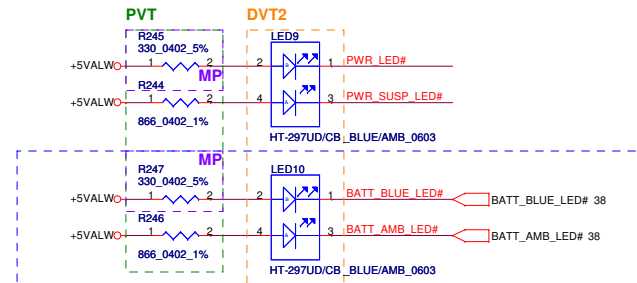
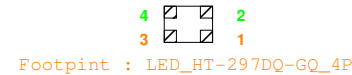
NUM_LED



CAPS_LED



Compal Footprint

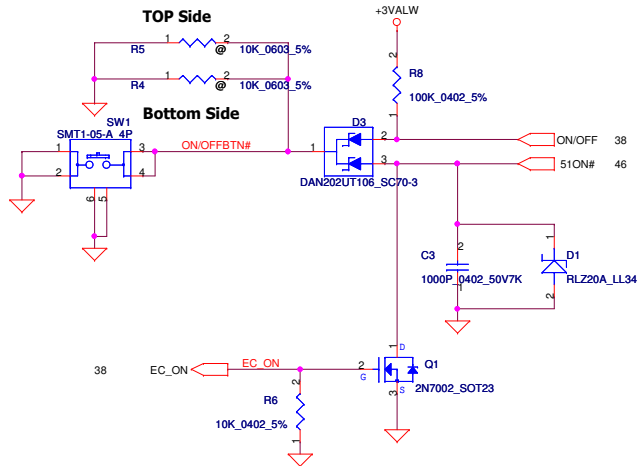


BLUE/AMBER

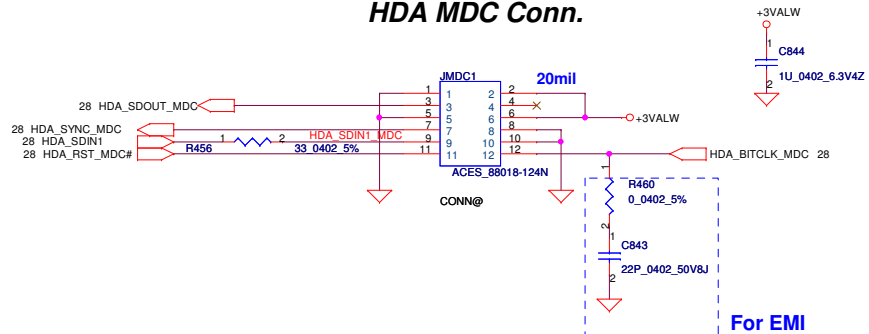
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Power Button

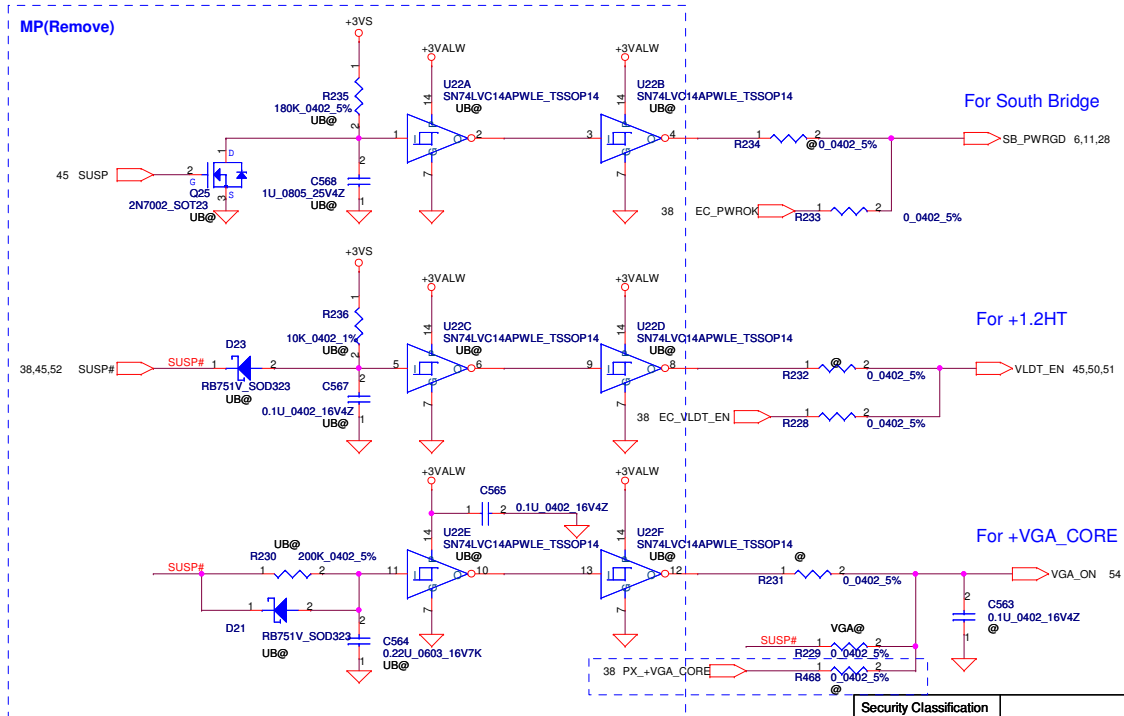
ON/OFF switch



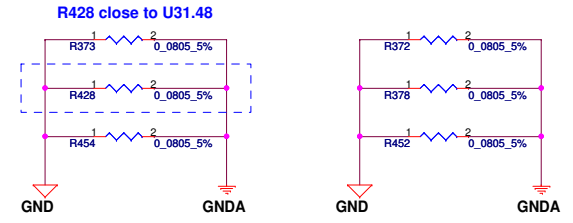
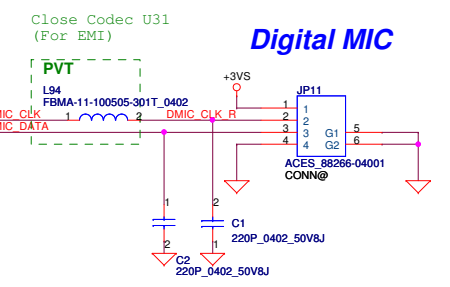
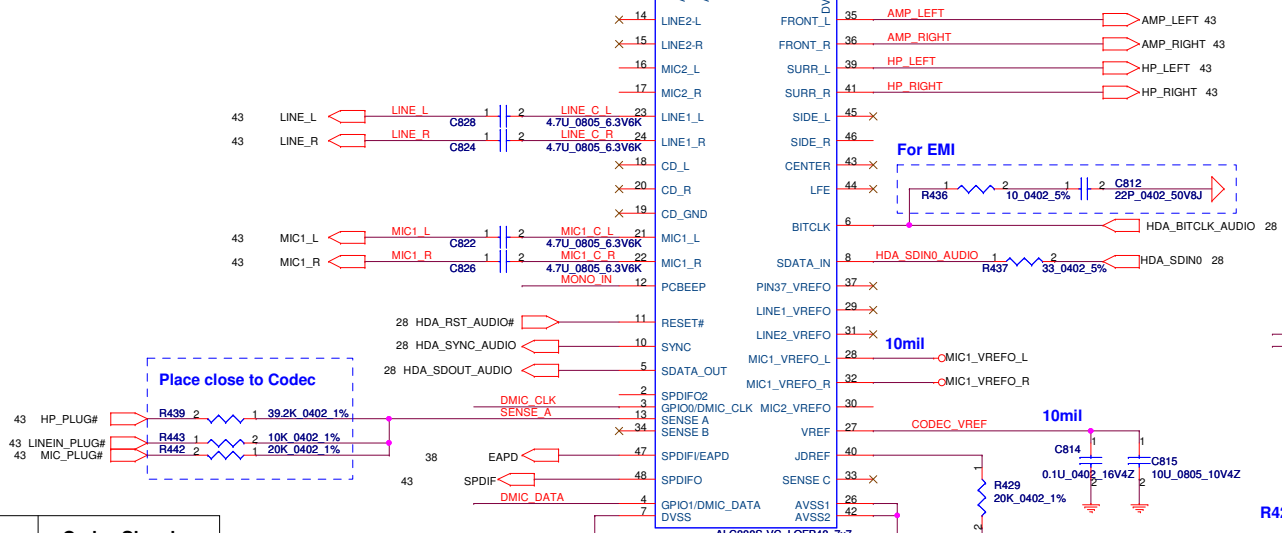
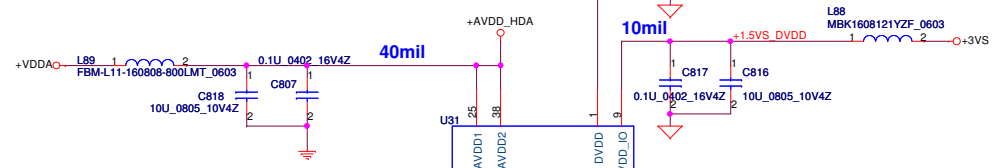
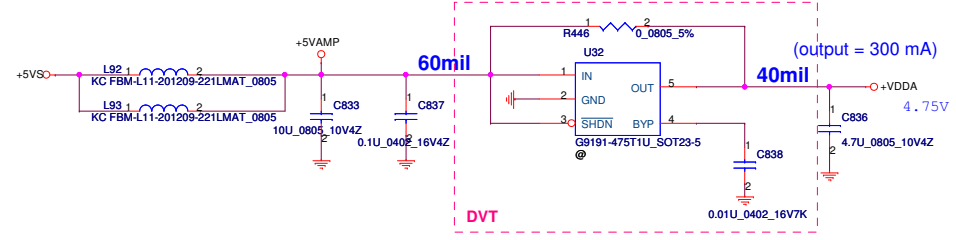
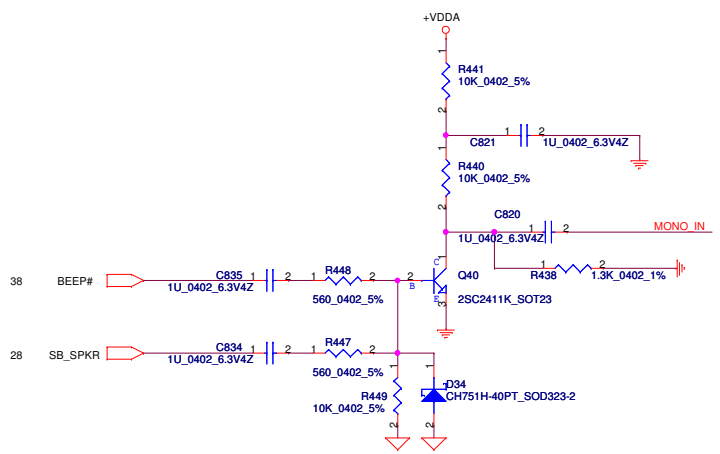
HDA MDC Conn.



Power ON Circuit

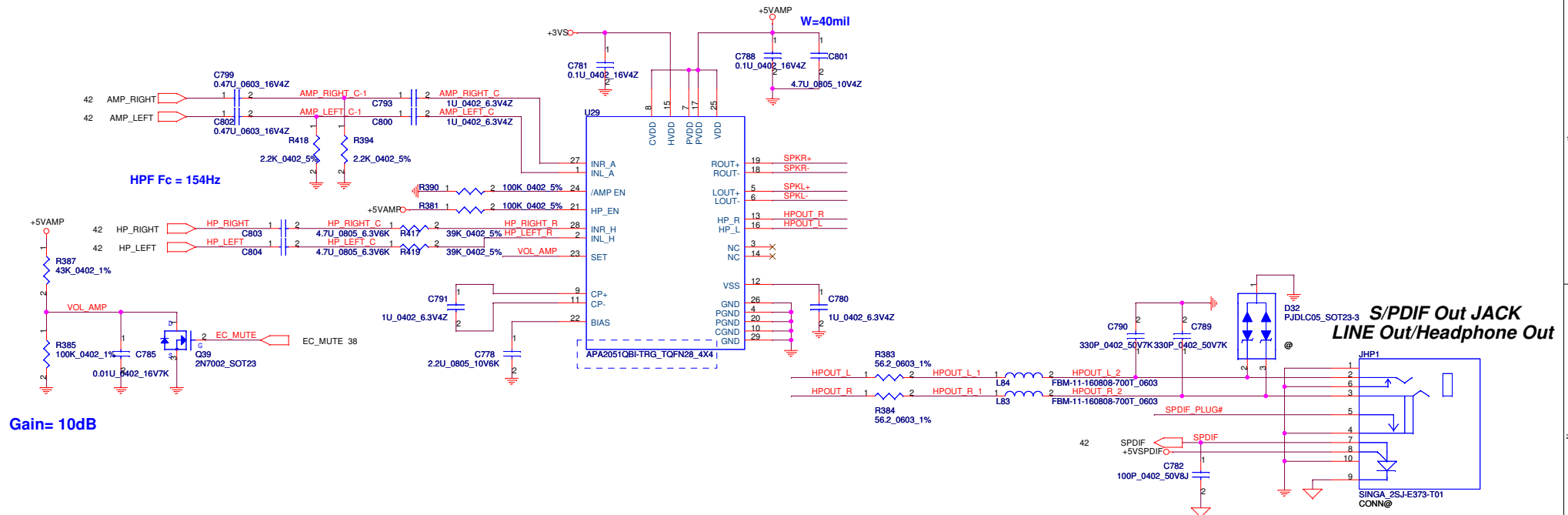


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				KBLG0 LA-4921P		
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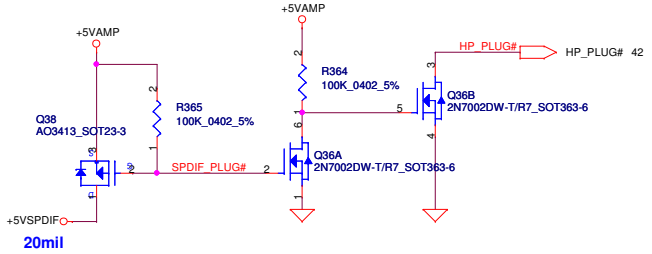
Place close to Codec

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



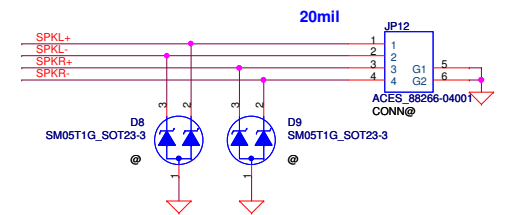
HPF Fc = 154Hz

Gain= 10dB

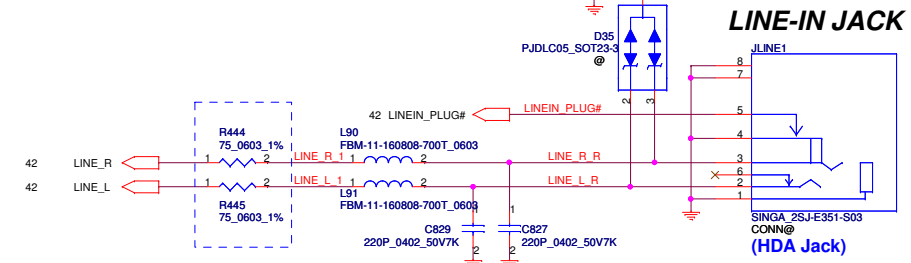


20mil

Int. Speaker Conn.

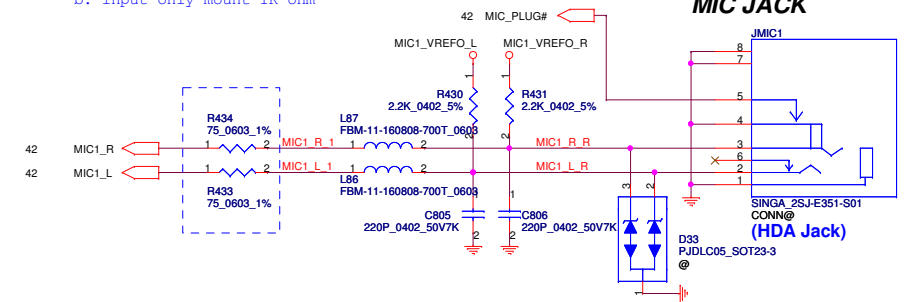


20mil



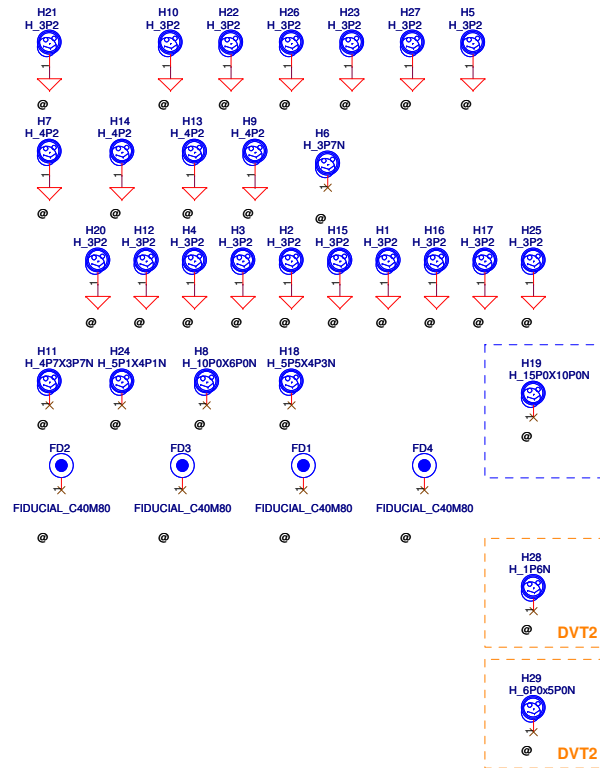
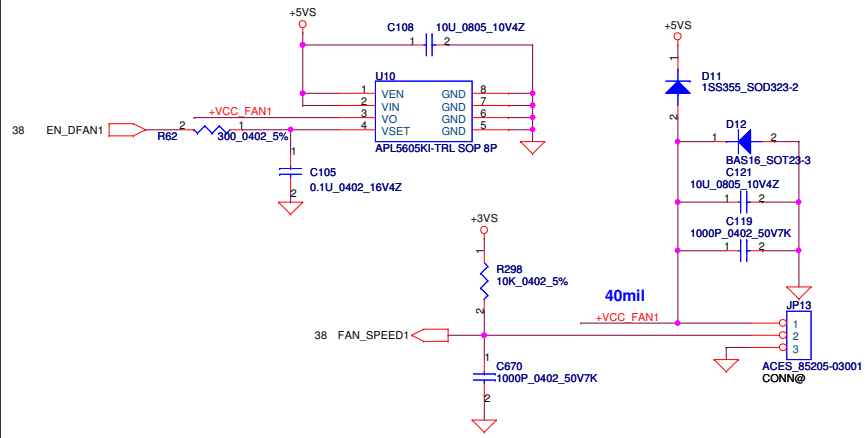
For ESD I/O status:
 a. input/output mount 75 ohm
 b. input only mount 1K ohm

MIC JACK



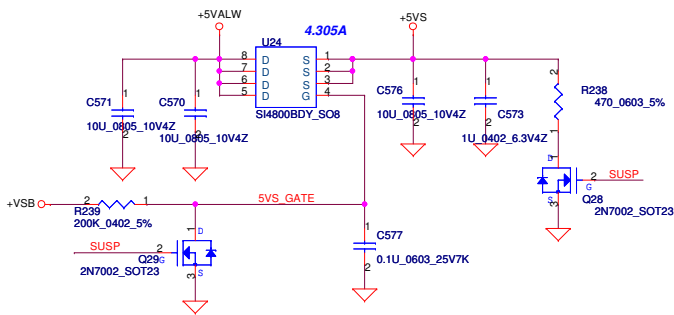
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	Amplifier & Audio Jack	
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FAN1 Conn

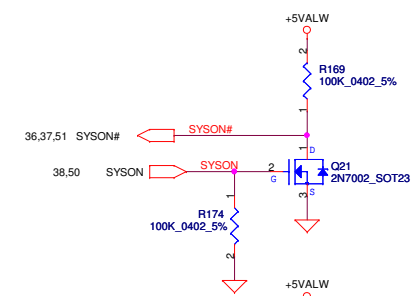
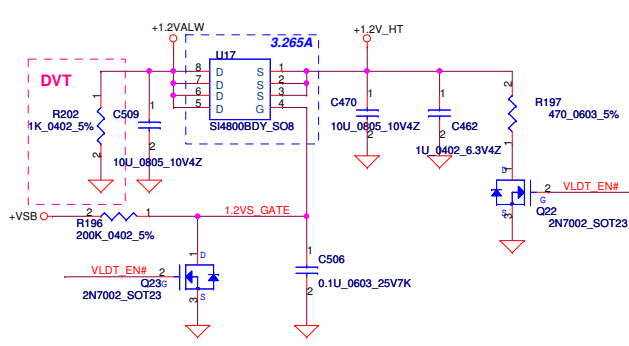


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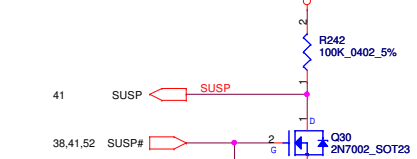
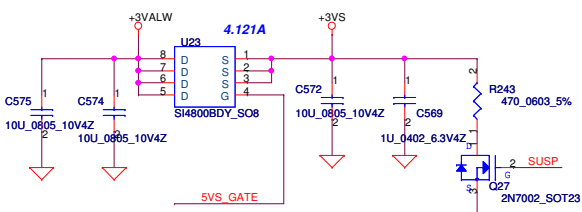
+5VALW TO +5VS



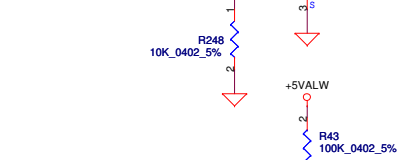
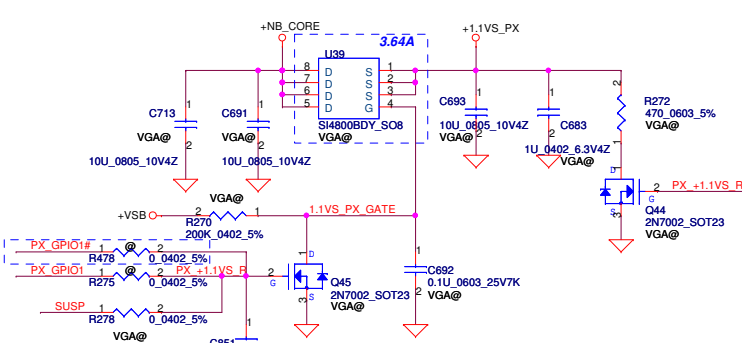
+1.2VALW TO +1.2V_HT



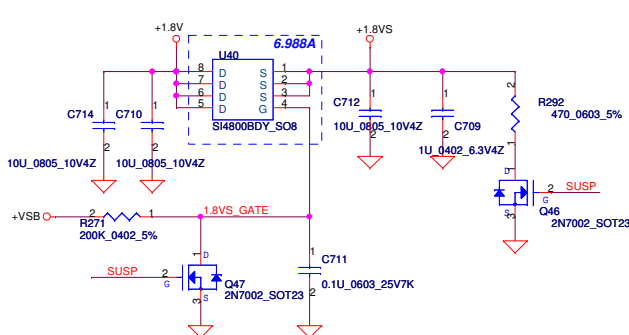
+3VALW TO +3VS



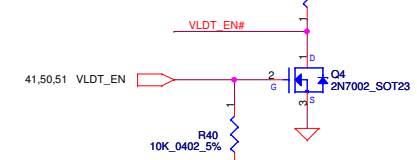
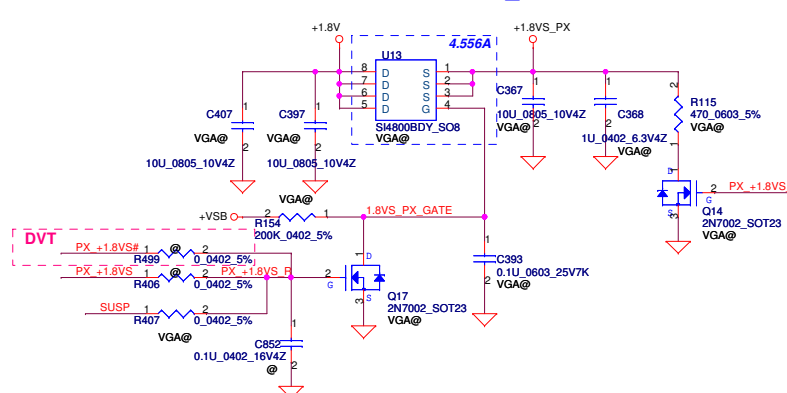
+NB_CORE TO +1.1VS_PX



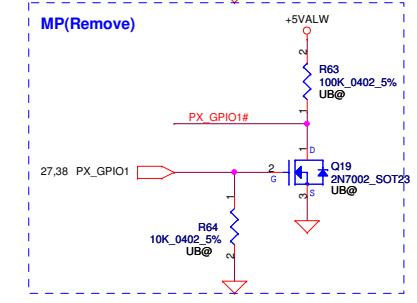
+1.8V to +1.8VS



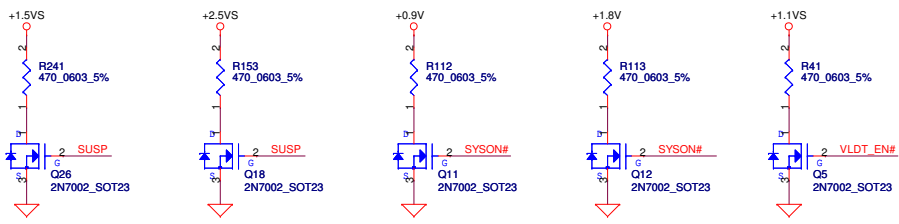
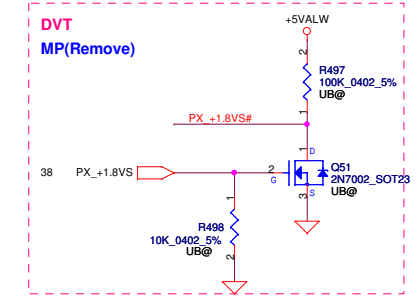
+1.8V to +1.8VS_PX



MP(Remove)



DVT MP(Remove)

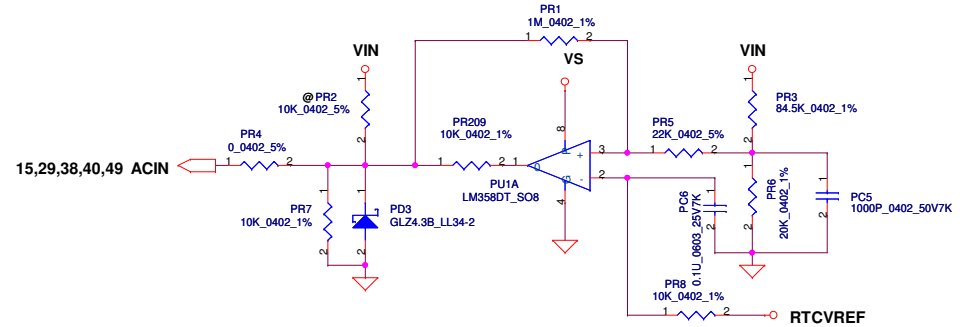
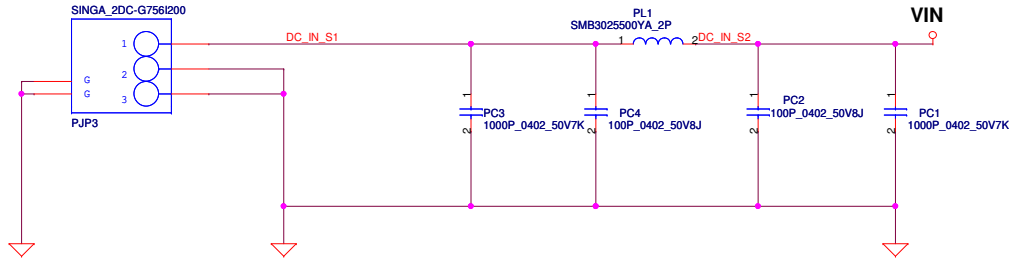


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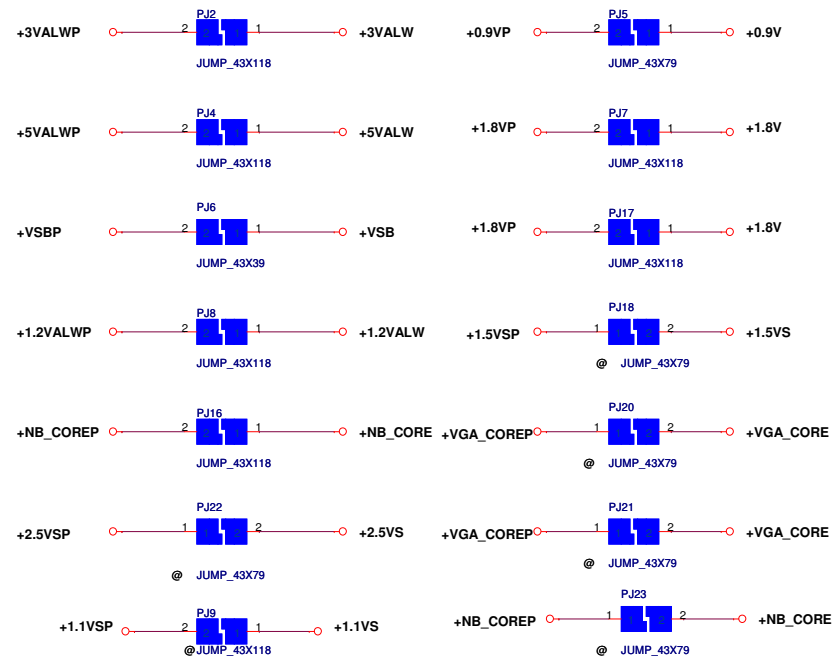
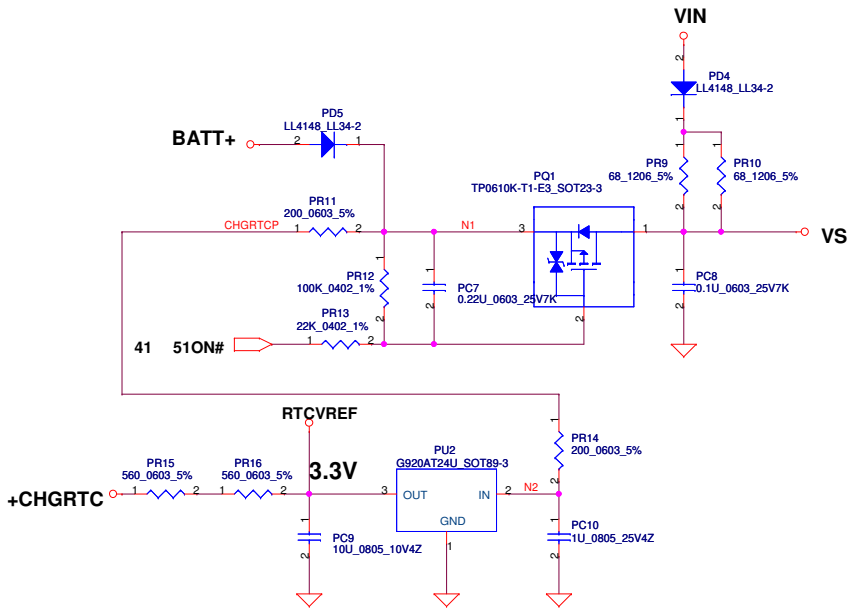
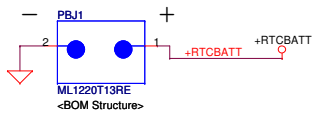
Compal Electronics, Inc.			
DC Interface			
Title	Document Number	Rev	
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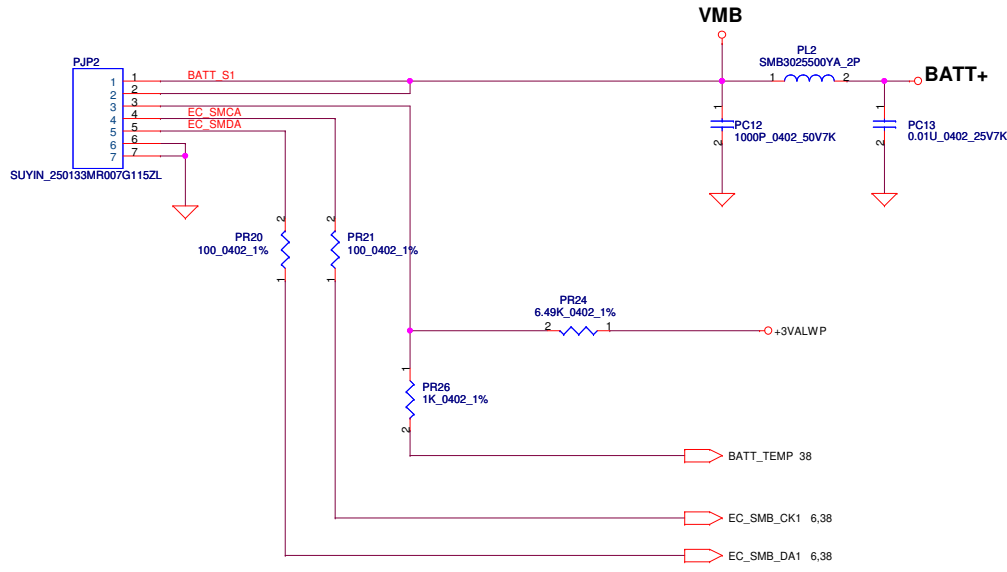
DC231000500

<BOM Structure>
SINGA_2DC-G756I200

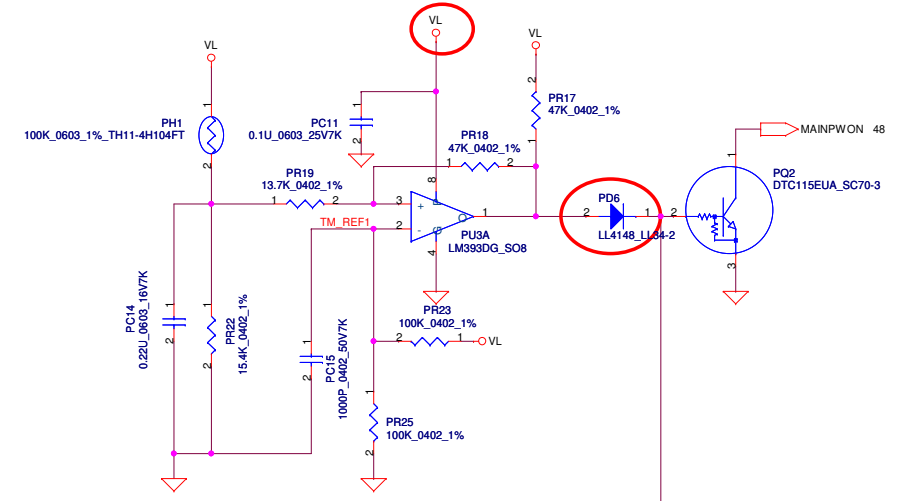


Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

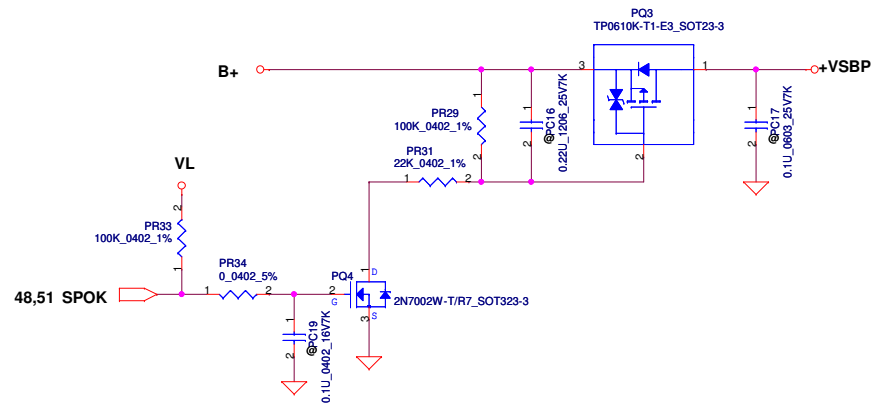
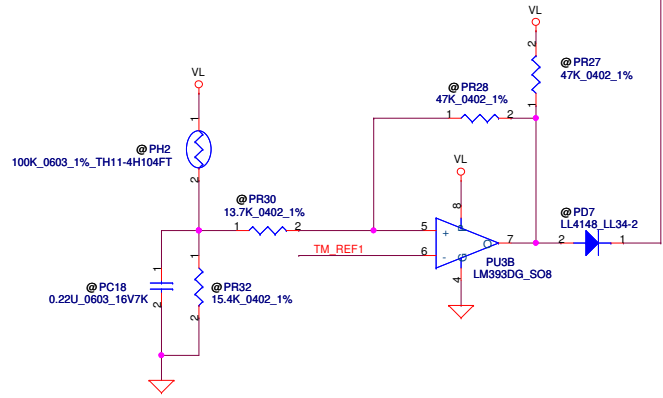




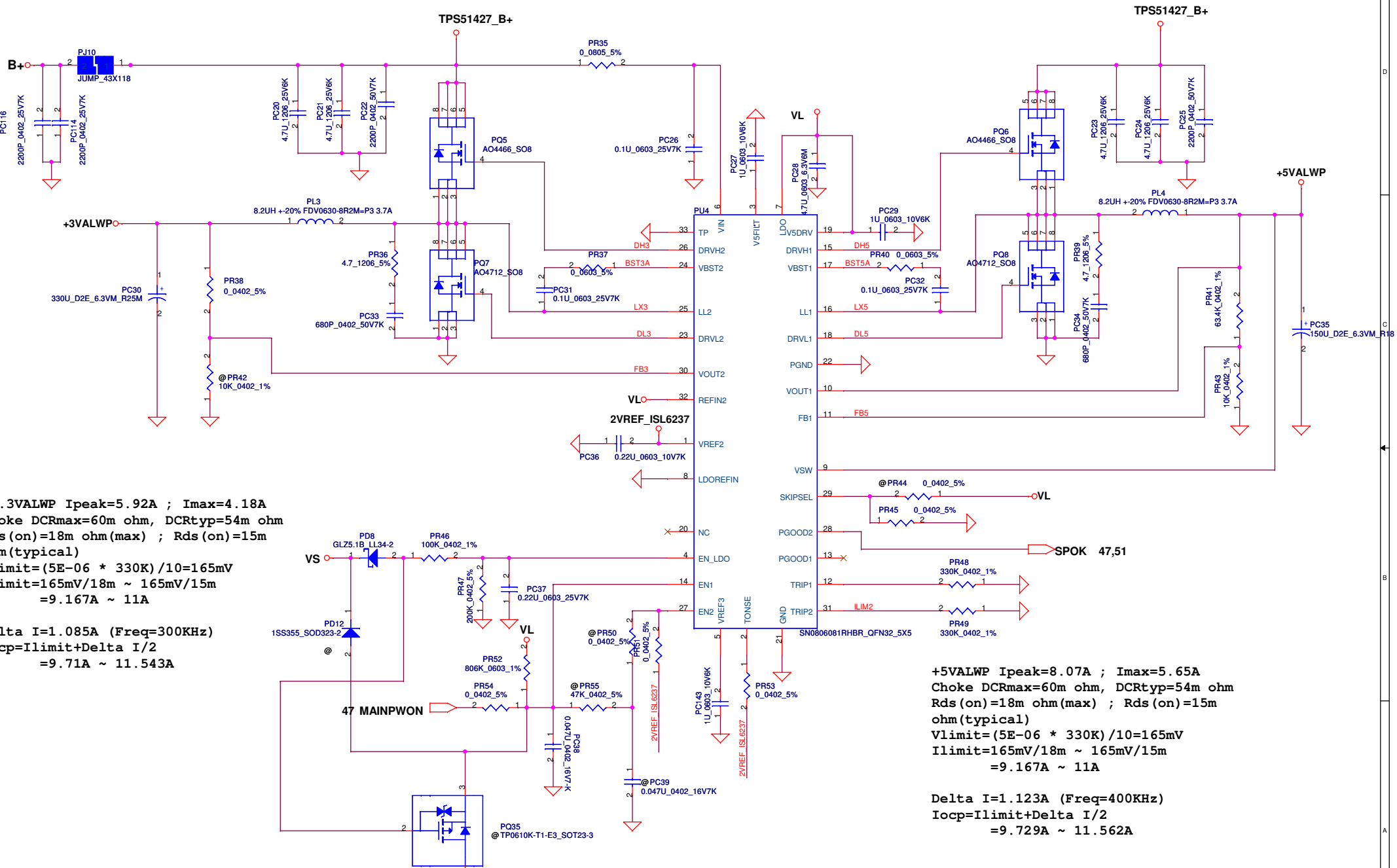
PH1 under CPU botten side :
 CPU thermal protection at 93 degree C
 Recovery at 57 degree C



PH2 near Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 47 degree C



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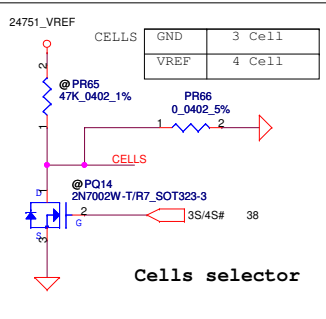
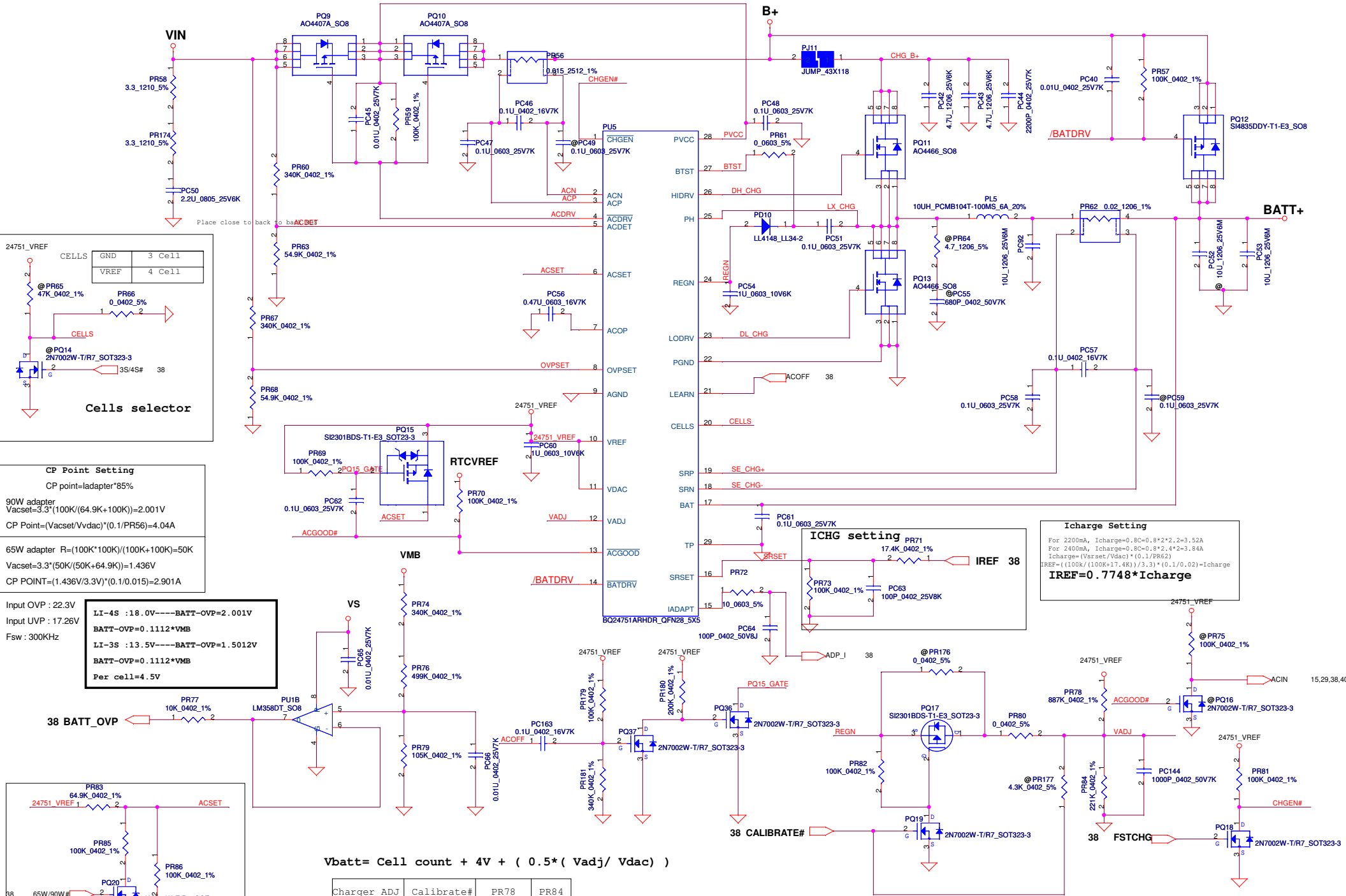
+3.3VALWP Ipeak=5.92A ; I_{max}=4.18A
 Choke DCR_{max}=60m ohm, DCR_{typ}=54m ohm
 R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
 V_{limit}=(5E-06 * 330K)/10=165mV
 I_{limit}=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A

 Delta I=1.085A (Freq=300KHz)
 I_{ocp}=I_{limit}+Delta I/2
 =9.71A ~ 11.543A

+5VALWP Ipeak=8.07A ; I_{max}=5.65A
 Choke DCR_{max}=60m ohm, DCR_{typ}=54m ohm
 R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
 V_{limit}=(5E-06 * 330K)/10=165mV
 I_{limit}=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A

 Delta I=1.123A (Freq=400KHz)
 I_{ocp}=I_{limit}+Delta I/2
 =9.729A ~ 11.562A

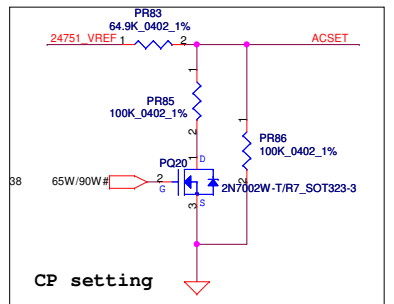
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CP Point Setting
 CP point=ladaprer*85%
 90W adapter
 $V_{ccset} = 3.3 * (100K / (64.9K + 100K)) = 2.001V$
 $CP\ Point = (V_{ccset} / V_{dacc}) * (0.1 / PR56) = 4.04A$
 65W adapter $R = (100K * 100K) / (100K + 100K) = 50K$
 $V_{ccset} = 3.3 * (50K / (50K + 64.9K)) = 1.436V$
 $CP\ POINT = (1.436V / 3.3V) * (0.1 / 0.015) = 2.901A$

Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz

LI-4S : 18.0V----BATT-OVP=2.001V
 BATT-OVP=0.1112*VMB
 LI-3S : 13.5V----BATT-OVP=1.5012V
 BATT-OVP=0.1112*VMB
 Per cell=4.5V



$V_{batt} = Cell\ count + 4V + (0.5 * (V_{adj} / V_{dacc}))$

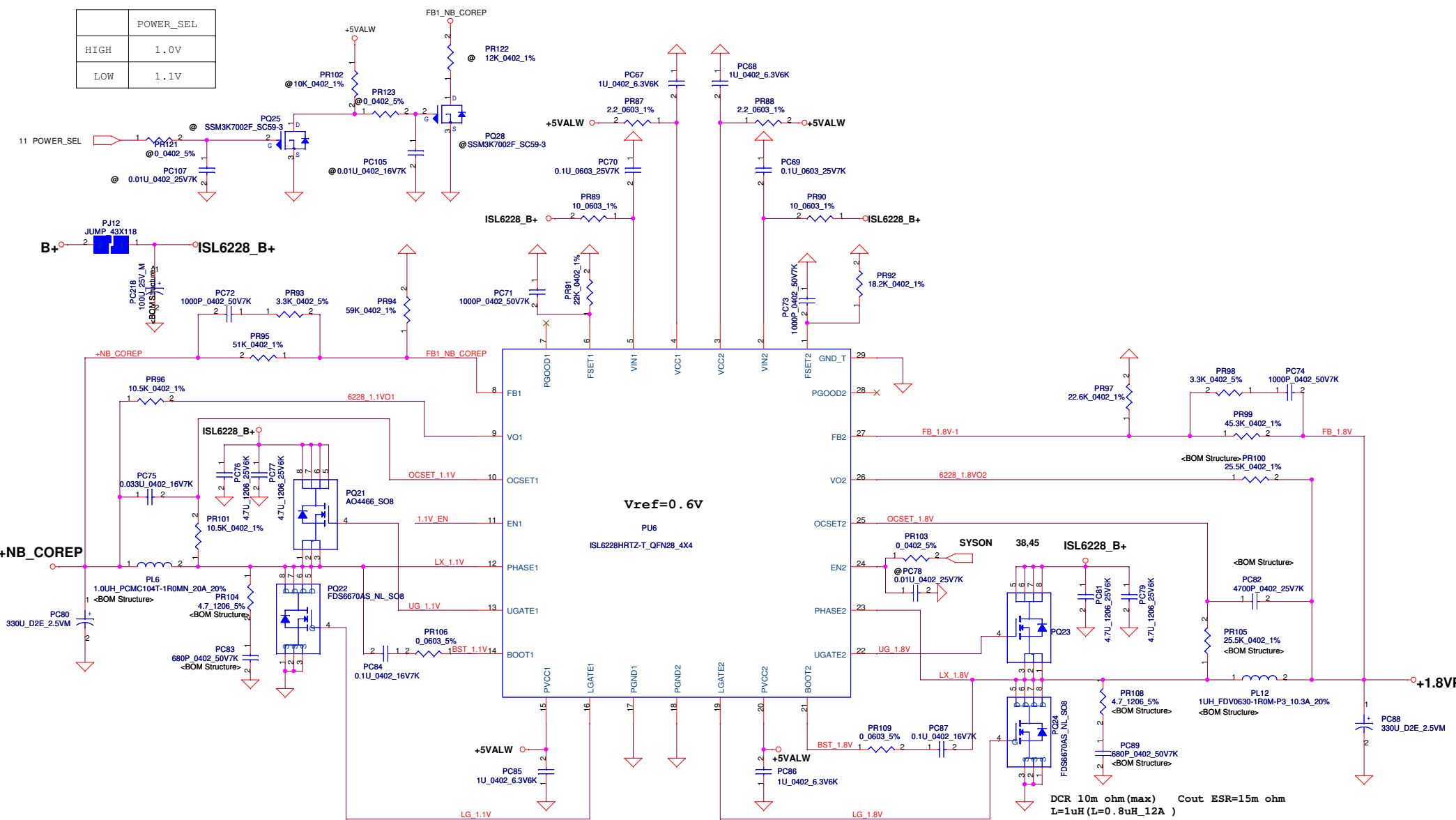
Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V (1.32)	H	@	@

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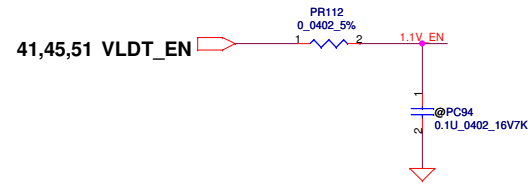
IChg setting
 For 2200mA, Icharge=0.8c=0.8*2*2.2=3.52A
 For 2400mA, Icharge=0.8c=0.8*2.4*2=3.84A
 $I_{charge} = (V_{ccset} / V_{dacc}) * (0.1 / PR62)$
 $I_{REF} = (100K / (100K + 17.4K)) / 3.3 * (0.1 / 0.02) = I_{charge}$
IREF=0.7748*IChg

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CHARGER			
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	POWER_SEL
HIGH	1.0V
LOW	1.1V

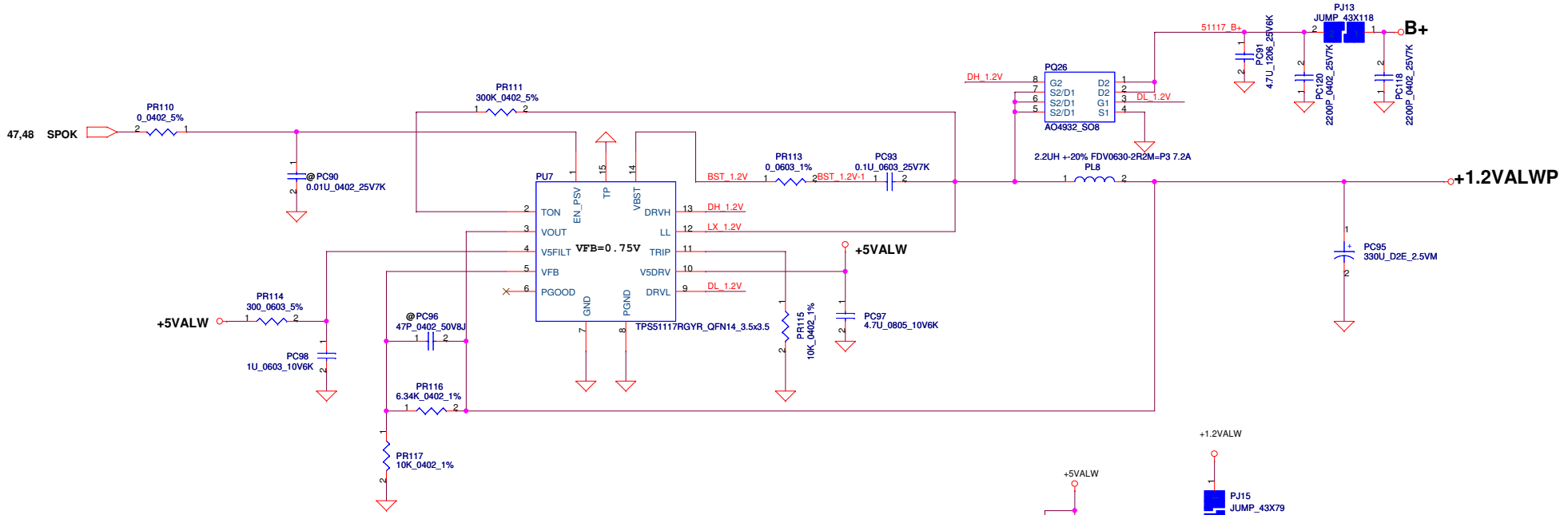


DCR3.5m ohm(max) Cout ESR=15m ohm
 NB_CORE (1.1VSP) OCP Setting
 $Fsw=1/1.5E-10*22k =303K$
 $Vo=Vref*((PR95+PR94)/PR94)$
 $Ipeak=17.53A, Imax=12.27A$
 $Iocp=17.53*1.2=21.04A$
 $Delta I=3.838A$
 $Iocp*DCR=(Rocset*9.5uA)=(21.04+1.92)*3.5m; Roset=8.44k$
 now chose Roset=8.66k
 $Csen=L/(DCR*Roset)=0.9uH/(3.5m*8.44k); Csen=0.031uF$
 now chose Csen=0.033uF
 $Iocp_min=(8.66k*9.5uA)/(3.5m\ ohm*1.3)=18.08A$
 $Iocp_max=(8.66*10.5uA)/(3m\ ohm*1.3)=23.32A$



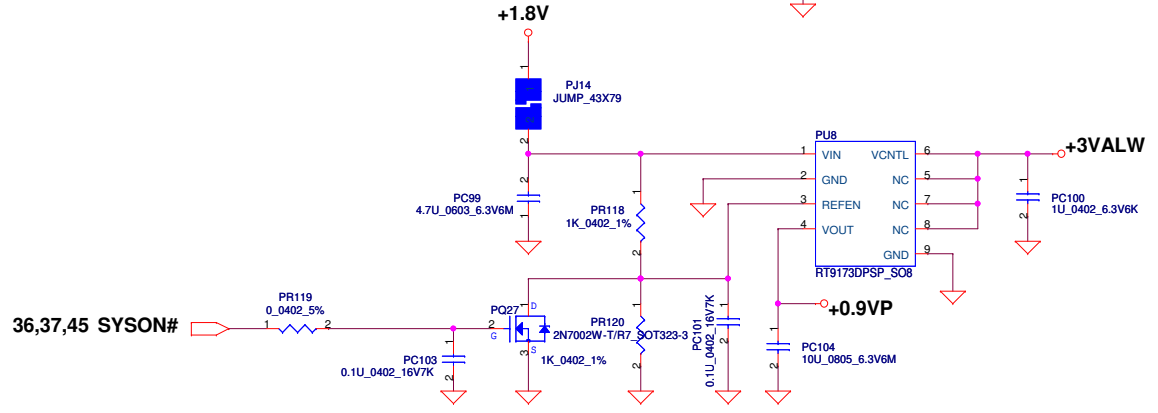
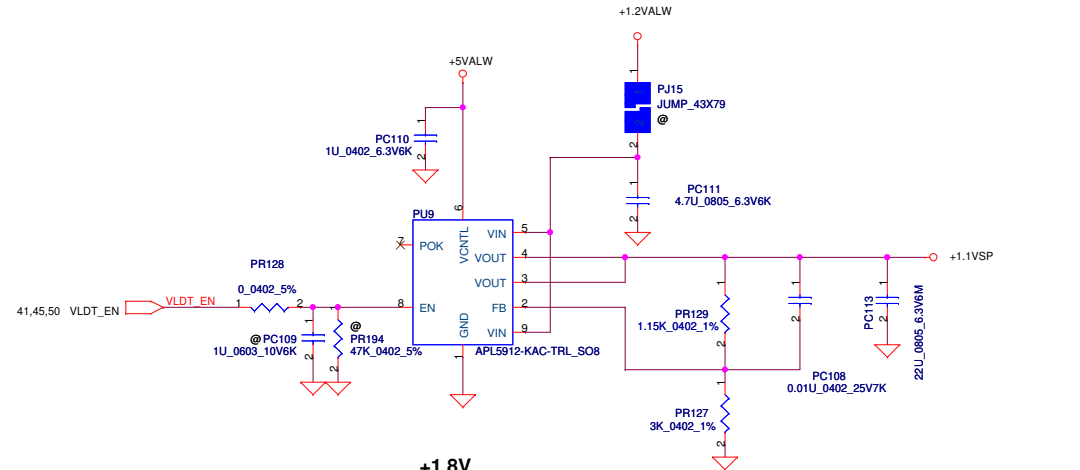
DCR 10m ohm(max) Cout ESR=15m ohm
 $L=1uH(L=0.8uH_{12A})$
 $1.8VP\ Ipeak=15.51A, Imax=10.86A$
 $Fsw=1/1.5E-10*18.2k =366K$
 $Vo=Vref*((PR97+PR99)/PR97)$
 $Ipeak=15.51A, Imax=10.86A$
 $Iocp=15.51*1.2=18.61A$
 $Delta I=5.565A$
 $Iocp*DCR=(Rocset*9.5uA)=(18.61+2.7825)*10m; Roset=22.5k$
 now chose Roset=22.6k
 $Csen=L/(DCR*Roset)=0.8uH/(10m*22.5k); Csen=3.56nF$
 now chose Csen=3300pF
 $Iocp_min=(22.6k*9.5uA)/(10m\ ohm*1.3)=16.52A$
 $Iocp_max=(22.6*10.5uA)/(10m\ ohm)=23.73A$

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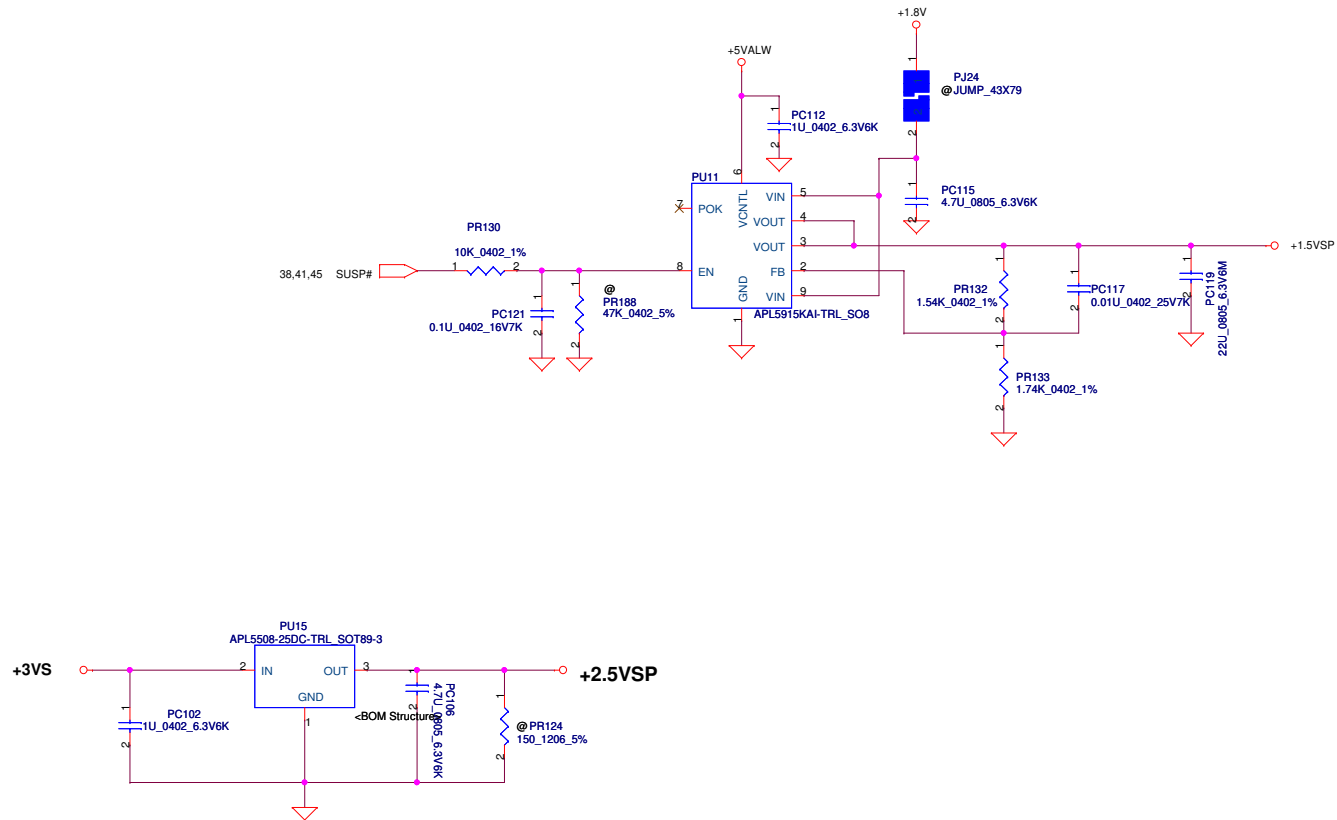


VFB=0.75V
 $V_o = VFB * (1 + PR116 / PR117) = 0.75 * (1 + 10K / 10K) = 1.5V$
 $Ton = 19E-12 * Ron * ((2/3) * V_o + 100mV) / v_{in} + 50ns = 3.2E-7$
 $F_{sw} = 200KHz$

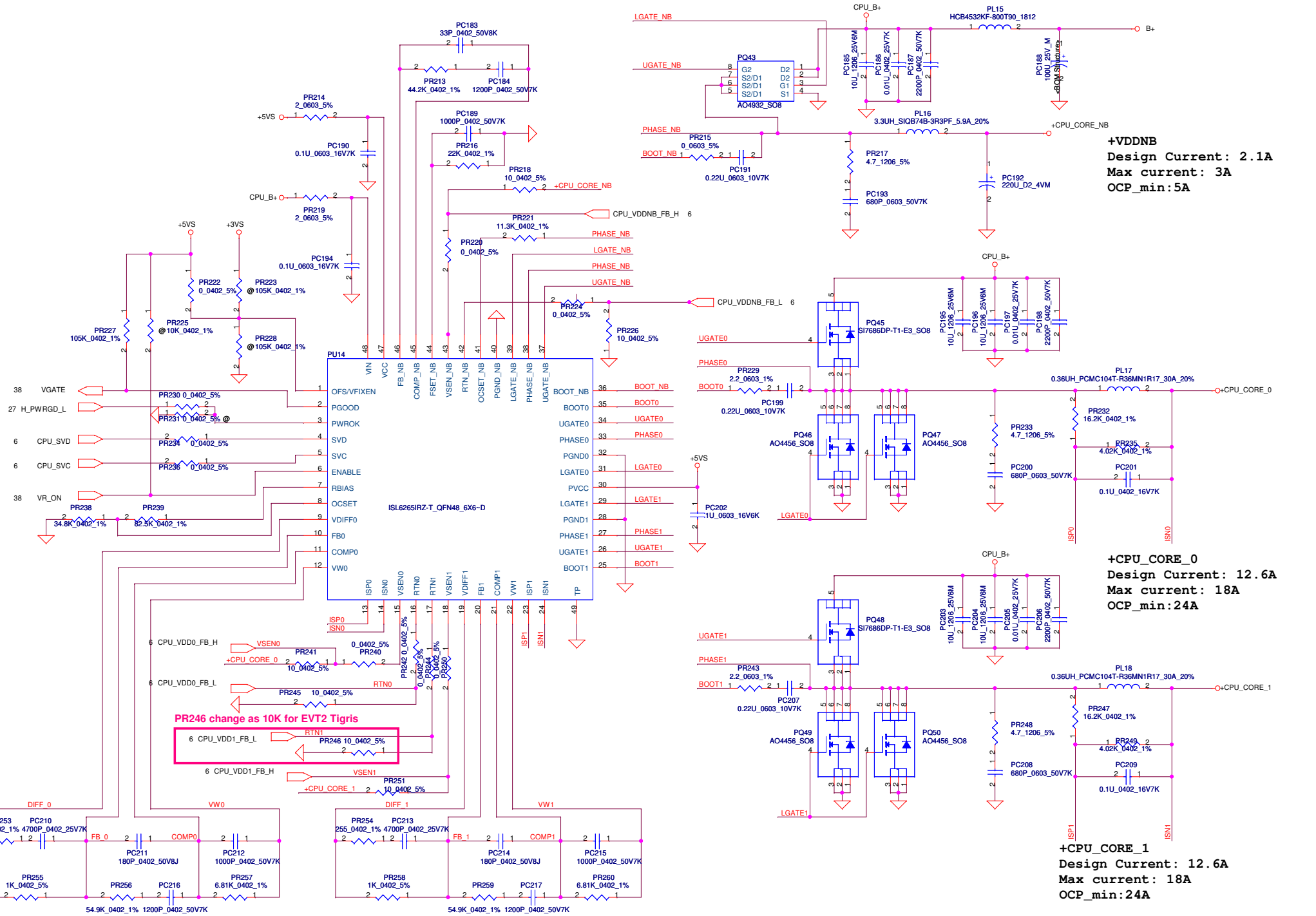
$C_{out} ESR = 15m\ ohm$
 $I_{peak} = 3.58A, I_{max} = 2.51A$
 $\Delta I = ((19 - 1.2) * (1.2 / 19)) / (L * F_{sw}) = 2.59A$
 $\Rightarrow 1/2 \Delta I = 1.295A$
 $V_{trip} = R_{trip} * I_{0uA} = 10K * 10uA = 0.1V$
 $I_{ocp_min} = V_{trip} / R_{dsonmax} * 1.4 + 1.295A = 0.1 / (0.0196 * 1.4) + 1.295 = 3.644A + 1.295A = 4.939A$
 $I_{ocpmax} = (0.1 / (0.016 * 1.2)) + 1.1.295A = 5.208A + 1.295A = 6.503A$
 $I_{ocp} = 6.503A \sim 4.939A$



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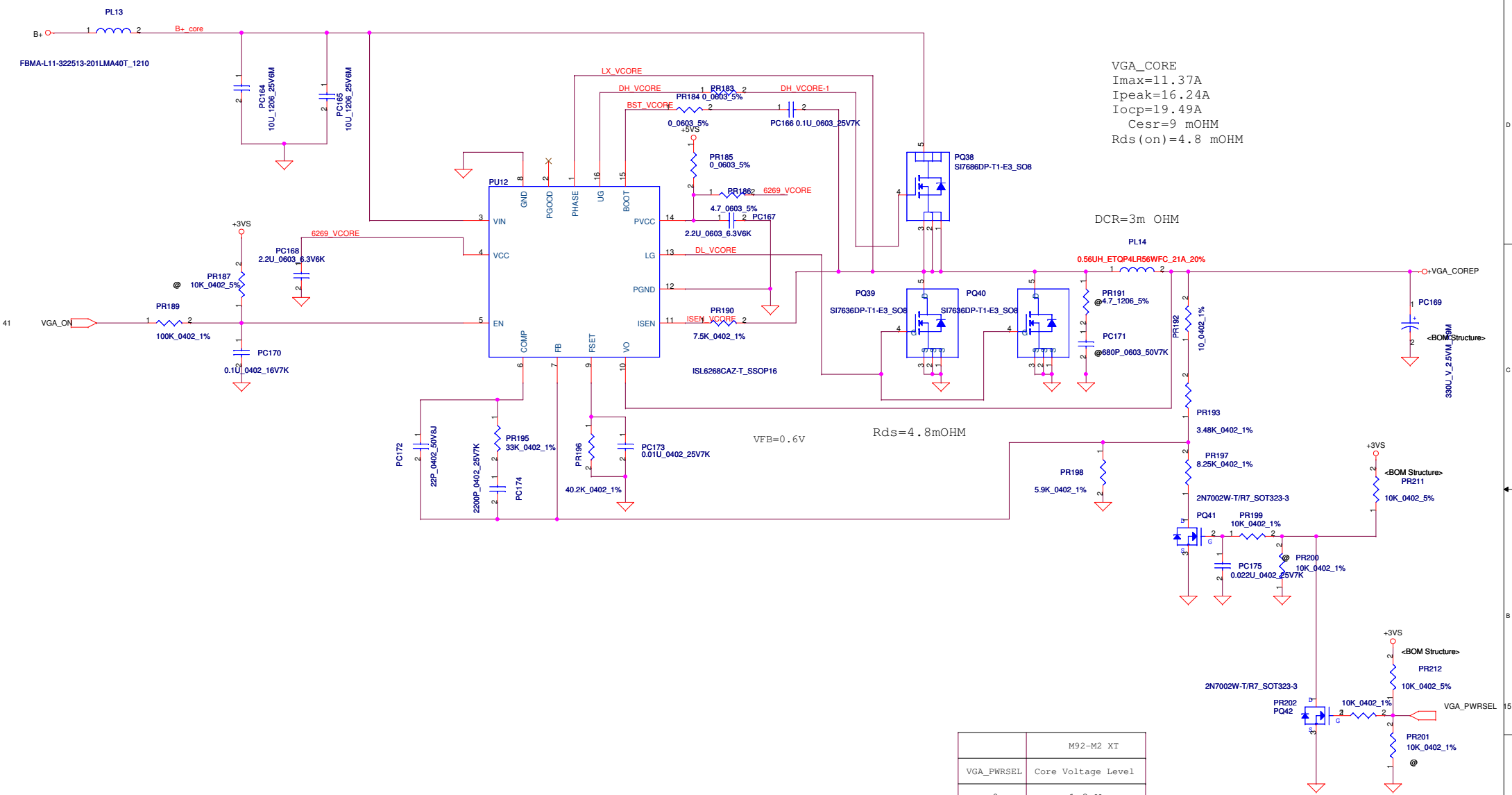
+VDDNB
 Design Current: 2.1A
 Max current: 3A
 OCP_min: 5A

+CPU_CORE_0
 Design Current: 12.6A
 Max current: 18A
 OCP_min: 24A

+CPU_CORE_1
 Design Current: 12.6A
 Max current: 18A
 OCP_min: 24A

PR246 change as 10K for EVT2 Tigris

Security Classification	Compal Secret Data		Title	
Issued Date	2008/04/16	Deciphered Date	2009/04/16	+CPU_CORE
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Security Classification		Compal Secret Data		Title VGA CORE	
Issued Date	2007/12/18	Deciphered Date	2008/12/18		
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				Rev	0.1

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ADD circuit	Switch NB_core voltage	0.1	50	ADD PC107, PC105, PR121, PR123, PR122, PR102, PQ25, PQ28 at UMA Sku	2009/01/04	DVT
2	ADD circuit	Switch NB_core voltage	0.1	51	ADD PC110, PC111, PC108, PC109, PC1113, PR1128, PR194, PR129, PR127 at UMA Sku	2009/01/04	DVT
3	ADD snubber	EMI requestmnt	0.1	50	Add PR104 4.7 ohm and PC83 680p	2009/01/04	DVT
4	ADD snubber	EMI requestmnt	0.1	50	Add PR108 4.7 ohm and PC89 680p	2009/01/04	DVT
5	ADD CPU boot	EMI requestmnt	0.1	53	Add PR229 2.2 ohm	2009/01/04	DVT
6	ADD CPU boot	EMI requestmnt	0.1	53	Add PR243 2.2 ohm	2009/01/04	DVT
7	Change resistance value	Switch NB_core voltage	0.1	50	Change PR95 from 51 Kohm to 39.2 Kohm	2009/01/04	DVT
8	Change resistance value	Switch NB_core voltage	0.1	50	Change PR122 from 12 Kohm to 226 Kohm	2009/01/04	DVT
9	Change resistance value	soft start of Switch NB_core voltage	0.1	50	Change PR123 from 0 ohm to 10 Kohm	2009/01/04	DVT
10	Change capacitor value	soft start of Switch NB_core voltage	0.1	50	Change PC105 from 0.01 uF to 0.1 uF	2009/01/04	DVT
11	Change IC part number	Change IC part number	0.1	48	Change PU4 part number to SA00002V400	2009/01/04	DVT

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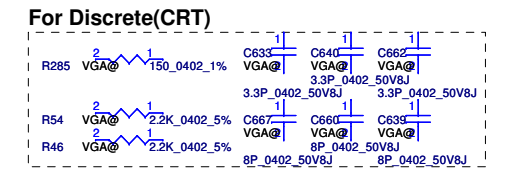
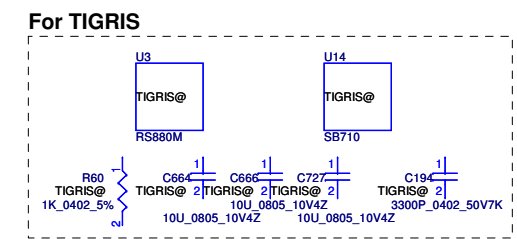
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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	PIR (PWR)		
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				Custom	KAL90	Custom-Doc	0.1
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Rev Code

PHASE	PAGE	MODIFICATION LIST	PURPOSE
DVT	P.6	Reserve R484/R485(0ohm_0402) for CPU SB temp sensor	Reserved EC SMBUS1 due to +3VS leakage when S3 entry with SMBUS2
	P.8	Add C174/C175/C176 (0.1u_0402)	EMI request
	P.10	C646/C647/C648/C649/C650/C651/C652/C653 with VGA@	BOM error
	P.11	Add R488/R489 (0ohm_0402) & reserve R491/R492 (0ohm_0402)	UMA HDMI I2C bus mainly to RS780MN DDC port1 & reserve to port0
	P.11	Reserve R490(0ohm_0402)	NA
	P.12	Change L6/L7 from 0ohm_0805 as 0ohm_1206 & with VGA@	For DIS +1.1VS power source from fixed +NB_CORE
	P.22	Remove VRAM Samsung(Q-die) & Qimonda type	Customer request
	P.24	U35/R464/R465/C845/C846/C847/C848/C849 with @ & RP15 with UMA@	Separately as DIS sku only & UMA sku only
	P.24	Add RP20/RP21/RP22/RP23(0ohm_0404_4P2R) with VGA@	For DIS sku only
	P.24	Reserve Q52/R501/R502/R503	Reserve for UMA sku white screen flash when boot issue check
	P.25	Change JHDMI1 from SMD type as DIP type(DC232000800)	DFX request
	P.25	Change single MOS as 2 dual N-ch MOS(Q53/Q54) & reserve R506	NA (Just no need to modify)
	P.26	R47/R58/U25/U26/C626/C628/R475 with UMA@ & R507 with VGA@ , U36/C850 with @ & delete R466 , add R493/R494/R495 with VGA@	Separately as DIS sku only & UMA sku only
	P.27	Add R496 with @ & R476/R482 with @	NA
	P.28	Add R509 with VGA@ & R510 with UMA@	Reserve SKU ID for SW even SW check device ID instead currently
	P.29	Reserve C862/C863/C855/C856	Reserve eSATA function for future request
	P.37	Change JUSB1 as SB700 USB port6	Dedicated HS port on lower-left position
	P.38	Change U20 as KB926 D3 version (SA00001J580)	NA
	P.38	D41 with VGA@ & D42 with UMA@	Separately as DIS sku only & UMA sku only
	P.38	U20.85 defined as TP_LOCK_LED# feature	LED control simultaneously with Tutch-Pad locked function
	P.38	Change R194 as 8.2kohm_0402	Change board ID as 1 (PCB revision : 0.2)

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				Date	Wednesday, March 11, 2009

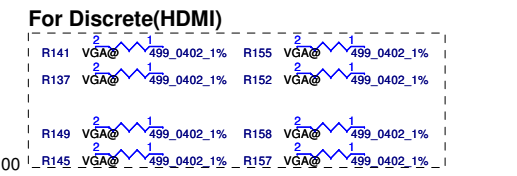
PHASE	PAGE	MODIFICATION LIST	PURPOSE
	P.39	Add R250/LED11/SW4	Add T/P lock button & T/P lock button LED
	P.45	Reserve R499 , R497/R498/Q51	NA
	P.45	Stuff R202	+1.2VALW leakage 640mv pulse when AC insertion & then might cause OVP
	P.34	C26 with @ & C11 as SE070104Z80	NA
	P.42	Stuff R446(0ohm_0805) & un-stuff U32(Audio LDO)	NA
DVT2	P.6	Remove CPU side-band(internal) temp sensor function	NA
	P.11/38	Add U49/C857/R744 (Reserve U48) & D42 with @, remove D42	NA
	P.23/34	Add R676 for CLK_48M_SD , reserve R715 / R716 for CLK_48M_LAN	NA
	P.24	Add R508(2.7K_0402) for ENVDD of UMA sku	NA
	P.28	SB700 USB port 4 for Realtek RTS5159 card reader	NA
	P.33	Add(co-layout) Realtek RTS5159 card reader	NA
	P.37	Change JSAT1 PCB footprint as TYCO_1909574-1_11P-T	NA
	P.38	R194 change as 18K_0402	Change board ID as 2 (PCB revision : 0.3)
	P.40	LED1 / 5 / 8 / 9 /10 PCB footprint change as LED_HT-297DQ-GQ_4P	For DFX
	P.44	Add H28 & H29	For thermal
PVT	P.11	Add R511 with @ & U50	For LCD white screen flash when coldboot issue
	P.11	Add C874 / C875 (1u_0402)	For CRT(acer lab) flicker
	P.11/38	C857 / U49 with @ , R744 / D42 with UMA@	NA
	P.42	Add L94(SM010027780) close to audio codec	For EMI
	P.40	Modify LED 1 / 5 / 8 from dual Blue/Amber LED as single Blue LED	Follow acer spec
	P.39/40	Modify R12/R13/R17/R16 (300->220ohm) , modify R1/R2/R3 (1.2K->866ohm) , modify R10 (300->715ohm) , modify R245/R247 (4.99K->750ohm) , modify R244/R246 (4.99K->866ohm) , modify R250 (1.2K->5.1K)	For LED brightness test
	P.23	Change LAN_CLKREQ# from U18.51 to U18.24 output	NA
	NA	Change test pad (except T8/T13/T15/T17/T18/T24/T28 /T29/T33/T45/T46/T48/T50/T56/T57/T12) from TPC12 to TPC24	NA
	P.36	Reserve Q55 / Q56 / R745 / R746 / R747 / C876 to turn off power of finger printer	NA
	P.38	R194 change as 18K_0402 for change board ID as 3 (PCB revision : 0.4)	NA
MP		Search for MP font	NA



PCB

PCB 047 LA-4921P REV1 M/B

LA4921MB Rev0: DA80000DP00
 LA4921MB Rev1: DA80000DP10
 LA4921MB with Sub/B Rev1: DAZ07R00100



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