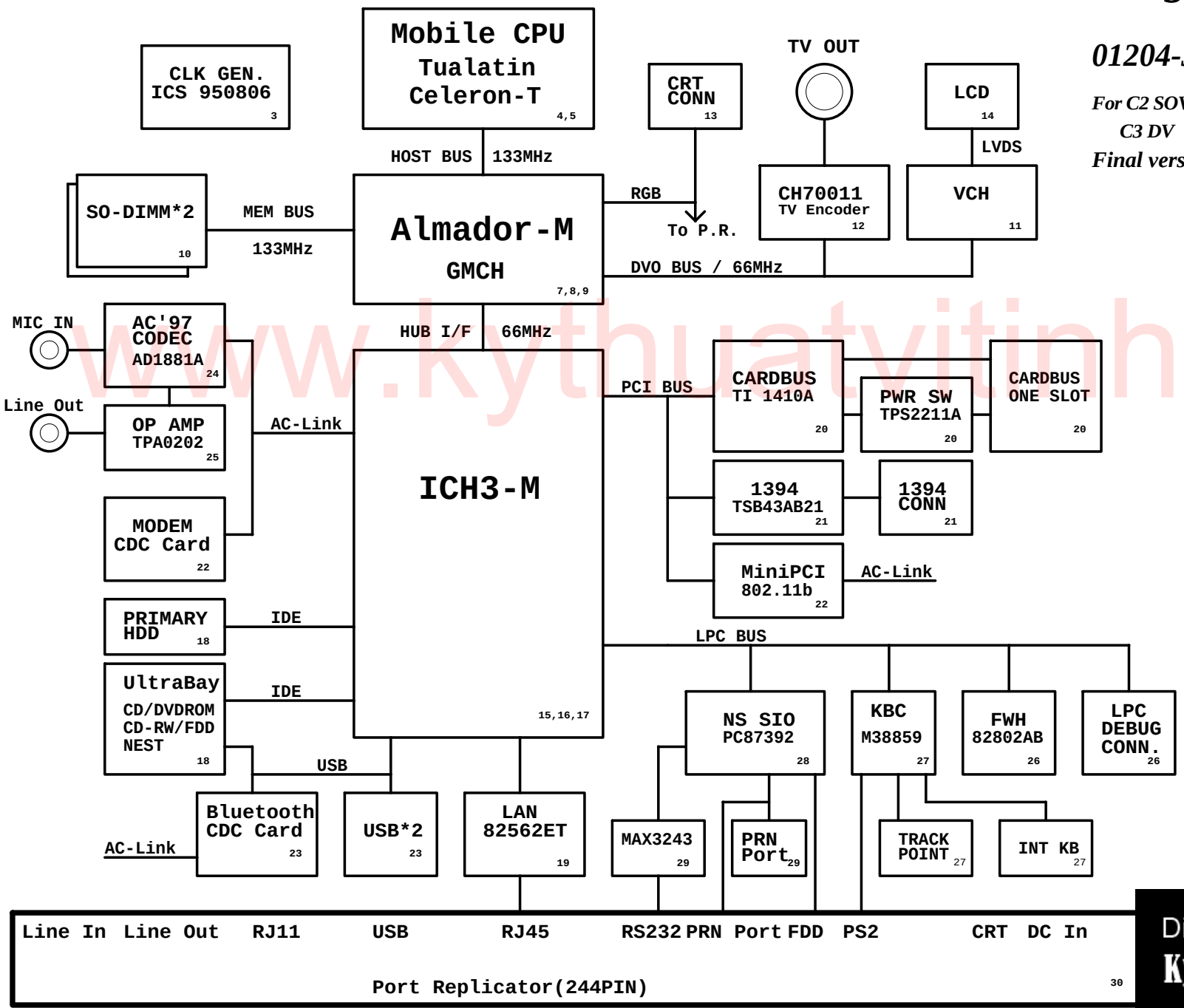
Jan. 11 2002

C-Note 2 Block Diagram

01204-3

For C2 SOVP
C3 DV
Final version



PCB LAYER
L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: GND
L6: POWER
L7: Signal 4(weak)
L8: Signal 5
L9: GND
L10:Signal 6

DC/DC&CHARGER
Switching Power
MAX1631/MAX1772

INPUTS	OUTPUTS
DCBATOUT	LAN+3VAUX UBAY+5V +3VSUS +5VSUS +3VRUN +5VRUN
AD+	BT+
	33,36

CPU DC/DC
Switching Power
MAX1718/MAX1714

INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE +VCCT
	31,32

OTHER DC/DC
MAX1644/MAX1792

INPUTS	OUTPUTS
+3.3VRUN +3.3VRUN	+1.8VRUN +1.5VRUN
	32

CG_* : CPU GTL+
CC_* : CPU CMOS
M_*   : MEMORY BUS
G_*   : AGP BUS
P_*   : PCI BUS
HL_* : HUB LINK I/F
LPC_* : LPC I/F
ICH_AC_* : AC'97 LINK I/F
IDE_* : IDE BUS

Cu-T & Tualatin SPEC Summary

July 3 '01

	Early Samples/ES	QS/ Production
Tualatin	VCC = 1.50V (perf mode)/ 1.15V (batt mode) VCCT = 1.3V (min), 1.365V (max) R143 16K5R3F R142 49K9R3F Tj (min) = 10C	VCC = 1.40V (perf mode)/ 1.15V (batt mode) ICC,MAX = 13.71A VCCDPRSLP=0.85V ICC,DSLP=2.09A VCCT = 1.25V +/- 5% (static) +/- 9%(transient) R143 2D49KR3 R142 10KR3F ICC =2.7A Tj (min) = 0C
Cu-T	VCC = 1.7V (perf Mode)/ 1.35V (Batt Mode) VCCT = 1.2V +/- 5% Functional at : VCCT = 1.3V (min), 1.365 (max)	VCC = 1.7V (perf Mode)/ 1.35V (Batt Mode) VCCT = 1.25V +/- 5% (static) +/- 9%(transient)
GMCH	VCC/VTT = 1.2V +/- 5% Functional at : VCC/VTT= 1.3V (min), 1.365V (max)	VCC/ VTT = 1.25V +/- 5%

MAX1718 Voltage Setting

D4	D3	D2	D1	D0	Vout (V)	
0	0	0	0	0	1.75	
0	0	0	0	1	1.70	Perf for Cu-T
0	0	0	1	0	1.65	
0	0	0	1	1	1.60	
0	0	1	0	0	1.55	
0	0	1	0	1	1.50	
0	0	1	1	0	1.45	Perf for Tualatin
0	0	1	1	1	1.40	Batt for Cu-T
0	1	0	0	0	1.35	
0	1	0	0	1	1.30	
0	1	0	1	0	1.25	
0	1	0	1	1	1.20	
0	1	1	0	0	1.15	Batt for Tualatin
0	1	1	0	1	1.10	
0	1	1	1	0	1.05	
0	1	1	1	1	1.00	

S1	S0	Vout (V)
GND	GND	0.975
GND	REF	0.950
GND	Float	0.925
GND	VCC	0.900
REF	GND	0.875
REF	REF	0.850
REF	Float	0.825
REF	VCC	0.800
Float	GND	0.775
Float	REF	0.750
Float	Float	0.725
Float	VCC	0.700
VCC	GND	0.675
VCC	REF	0.650
VCC	Float	0.625
VCC	VCC	0.600

ZMODE	SUS	Vout Determined by:
GND	GND	Logic Level of D0 - D4
VCC	GND	Impedance of D0 - D4
X	VCC	Logic Level of S0, S1

+VCCT +VCCT 3,4,5,6,9,32
+VCC_CORE +VCC_CORE 4,5,31
+1.5VRUN +1.5VRUN 4,5,6,7,8,9,11,12,17,26,32
+1.8VRUN +1.8VRUN 4,8,9,11,15,17,32
LAN+3VAUX LAN+3VAUX 15,17,19,22,30,34
+3VRUN +3VRUN 3,6,8,9,11,12,13,14,15,16,17,18,20,21,22,23,24,26,27,28,31,32,34,35,37
+3VSUS +3VSUS 6,9,10,14,18,20,23,27,31,32,34,35,37
+3VALW +3VALW 14,15,16,17,23,25,32,33,34,36
+3.3VRTC +3.3VRTC 16
+5VRUN +5VRUN 6,13,14,15,17,18,22,24,25,26,27,29,30,31,34,35,37
+1.8VALW +1.8VALW 17,34
+5VSUS +5VSUS 13,14,20,23,25,27,32,34,37
+5VALW +5VALW 14,17,18,30,33,34,36
LAN+1.8VAUX LAN+1.8VAUX 17,34
UBAY+5V UBAY+5V 18
+5VA +5VA 24,25
BT+ BT+ 35,36
+3VAUX +3VAUX 22,23
USB1_VCC USB1_VCC 23,30
LCDVDD LCDVDD 14
AC97_3V AC97_3V 23
CRT_VCC CRT_VCC 13,30
AD+ AD+ 35,36
AD+IN AD+IN 35,36
DCBATOUT DCBATOUT 14,31,32,33,34,35,36
DCBATOUT+ DCBATOUT+ 36
ICH_VBIAS ICH_VBIAS 16
VCC_RTC VCC_RTC 6,15,16,17
AD+_IN AD+_IN 30,36
MAX1631_VL MAX1631_VL 14,33
BT_VCC BT_VCC 23
FAN1_VCC FAN1_VCC 6
TV_DVDD TV_DVDD 12

TV_AVDD TV_AVDD 12
TV_VDD TV_VDD 12
+1.5VRUN_F +1.5VRUN_F 12
LCD_DCBAT LCD_DCBAT 14
LIGHT_PWR LIGHT_PWR 14

SLOTVCC SLOTVCC 20
SLOTVPP SLOTVPP 20
1394_AVDD 1394_AVDD 21
1394_PLLVDD 1394_PLLVDD 21
MOD_5VAD MOD_5VAD 22
USB0_VCC USB0_VCC 23
AUD_VREF AUD_VREF 25
OP+5V OP+5V 25
TP_VCC TP_VCC 27
1718_+5V 1718_+5V 31
M1772+3V M1772+3V 36
M1772_LDO M1772_LDO 36
DC+5V DC+5V 33
DC+3V DC+3V 33

PCI TABLE

DEVICE	IDSEL	IRQ	REQ# / GNT#
TI 1394	AD19	Auto	REQ2# / GNT2#
MINIPCI SLOT	AD21	C,E	REQ3# / GNT3#
PCMCIA TI1410	AD25	B,D	REQ1# / GNT1#
AGP	AD17(Int.)	A,B	
LAN	AD24(Int.)	E	
USB	AD29	A,D,C	
Hub-to-PCI	AD30		
LPC Bridge/ IDE/AC97/ SMBus	AD15		

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Title: TABLE OF CONTENT
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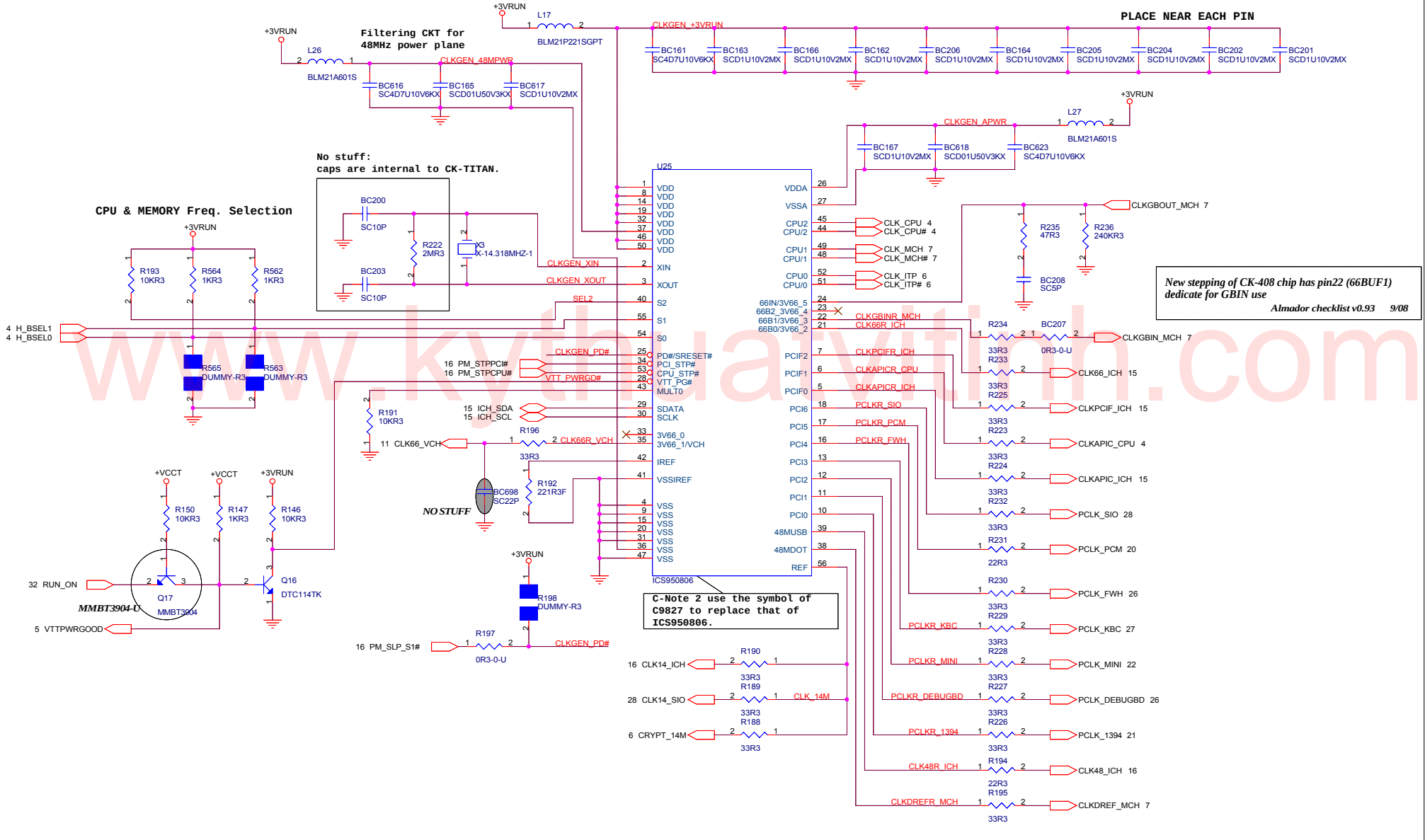

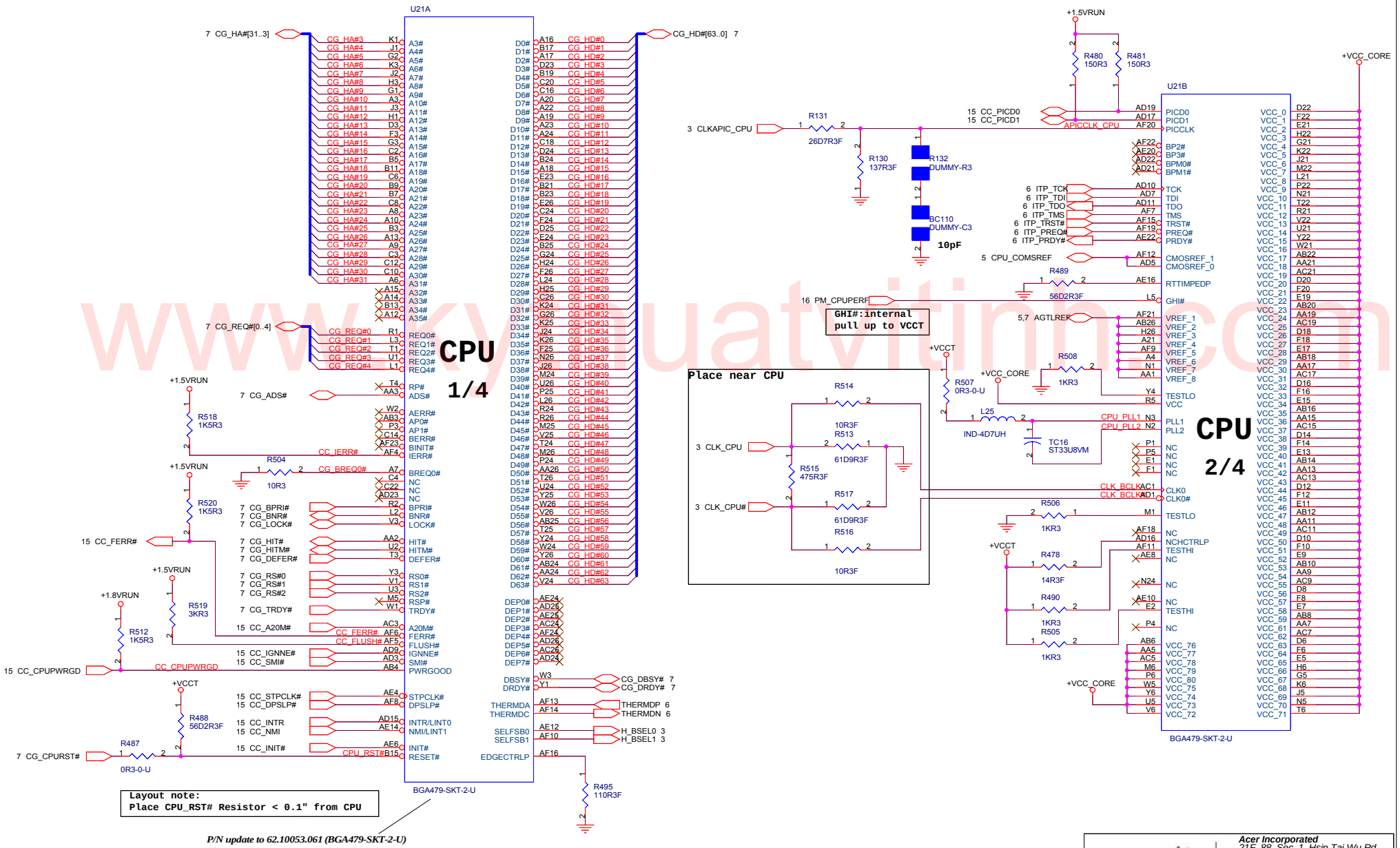

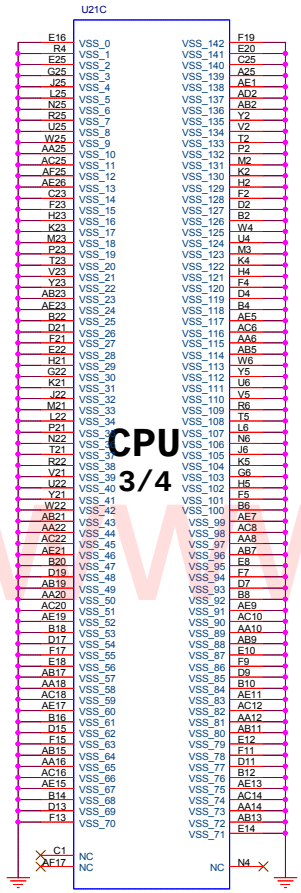

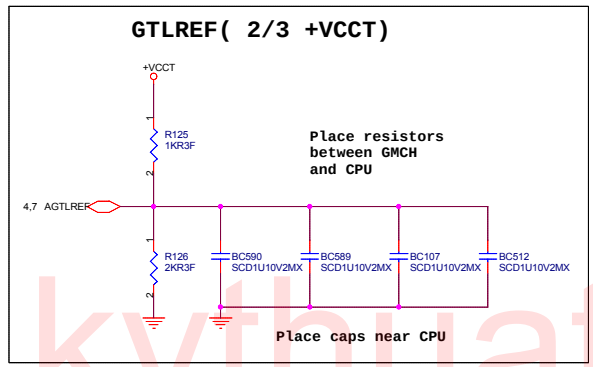

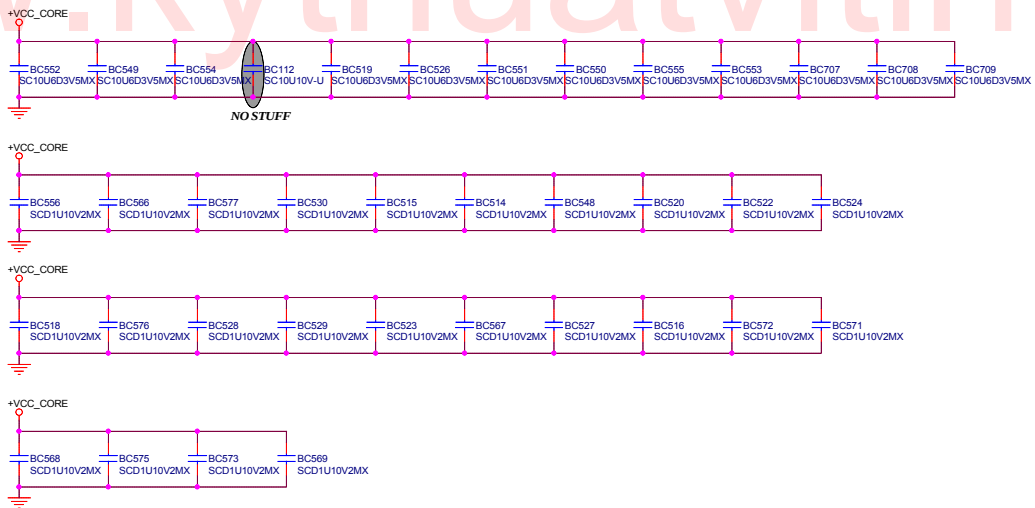

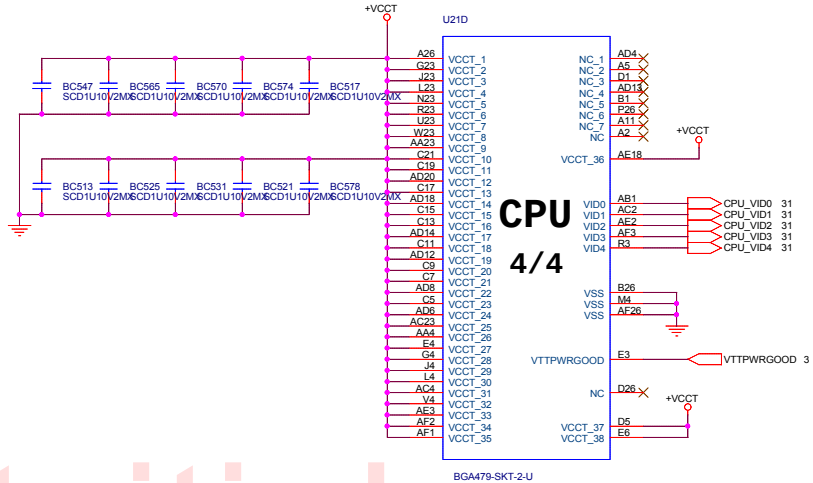

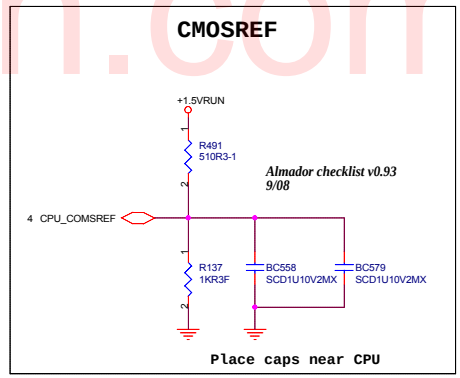

Decouping Recommendation — C-Note 2 — Kenora Ver 0.93

VCC_CORE	Underneath balls on solder side	0.22uF * 24	Use 2-3 vias per pad for reduced inductance during layout	0.1uF * 24	0.47uF * 24
	On the peripheral near balls	10uF / 6.3V * 10	Placement should be near processor for all	10uF / 10V * 10	10uF / 6.3V * 10 + 6 * NS
	Bulk Caps			220uF / 2.5V * 7	150uF / 4V * 12 + 2 * NS
VCCT	Place close to processor for all	1uF * 10	Use 2 vias per pad for reduced inductance during layout	0.1uF * 10	1uF * 10 + 2 * NS
	Bulk Caps			220uF / 2.5V * 2	150uF / 4V * 5 + 1 * NS

Almador-M Checklist Ver. 0.93 9/08

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Title: CPU CONFIGURATION

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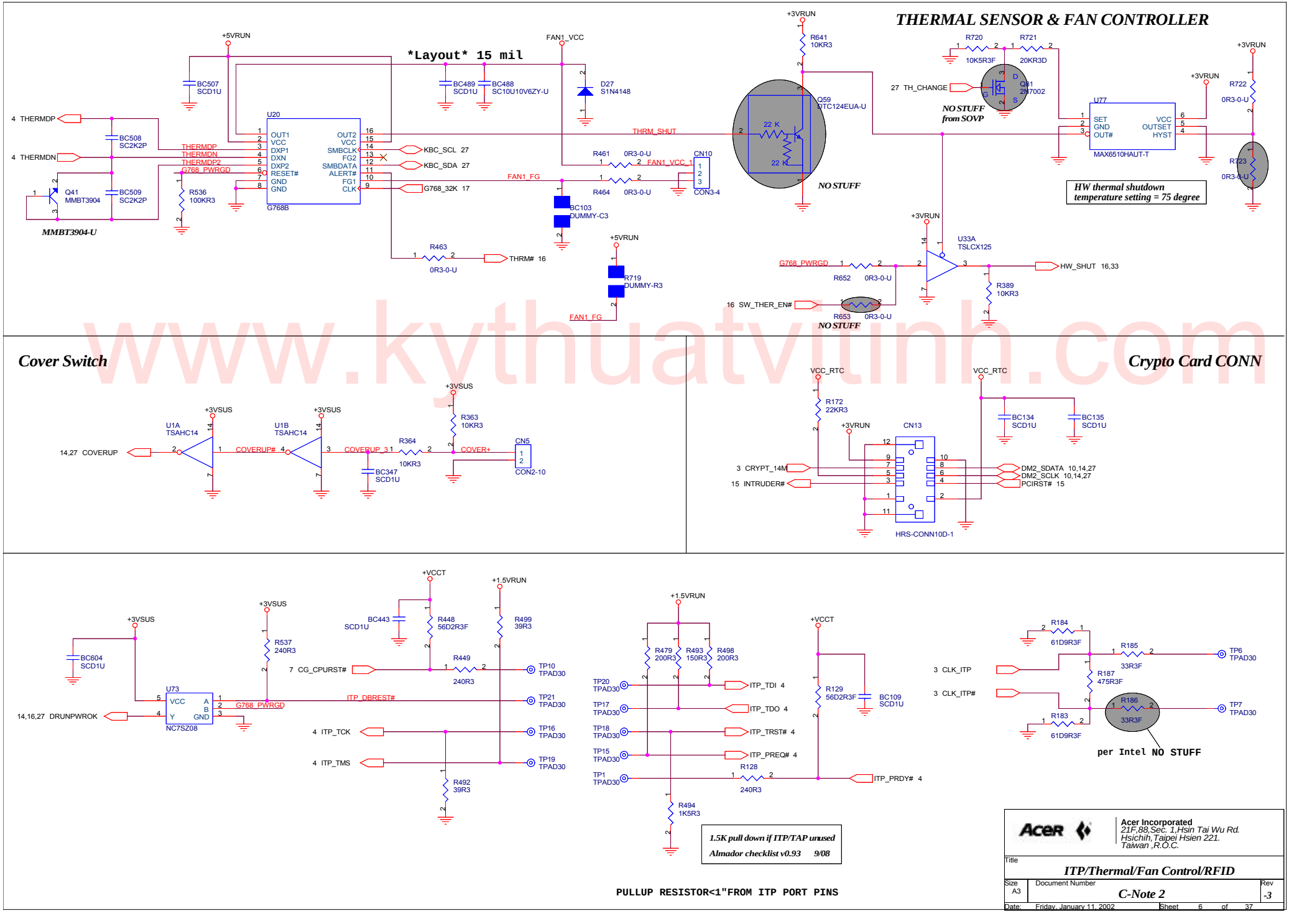

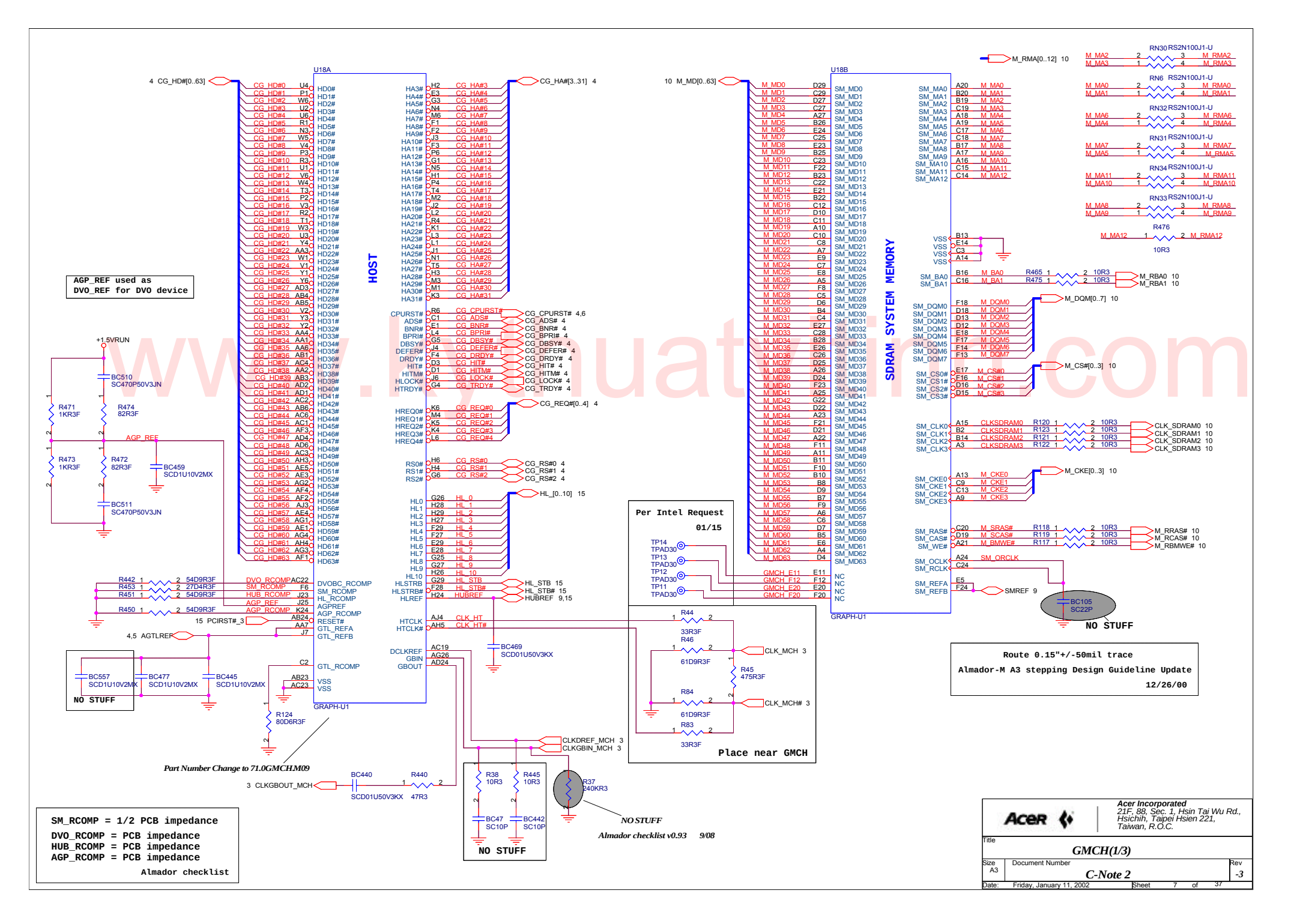
U18A
HOST
GRAPH-U1
U18B
SDRAM SYSTEM MEMORY
GRAPH-U1
AGP_REF used as
DVO_REF for DVO device
Per Intel Request
01/15
Place near GMCH
NO STUFF
NO STUFF
NO STUFF
Route 0.15"+/-50mil trace
Almador-M A3 stepping Design Guideline Update
12/26/00
SM_RCOMP = 1/2 PCB impedance
DVO_RCOMP = PCB impedance
HUB_RCOMP = PCB impedance
AGP_RCOMP = PCB impedance
Almador checklist
Part Number Change to 71.0GMCH.M09
NO STUFF
Almador checklist v0.93 9/08
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Title
GMCH(1/3)
Size A3
Document Number
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AGP_PAR	Pull-up 8.2K to 1.5VRUN	AGP device attached
	Pull-down 2.2K to GND	DVO device attached

Strapping Option for SW detection of AGP or DVO device

DVOA_CLK# (AG24) --> DVO_CLKIN1 (N8)
DVOA_CLK (AJ24) --> DVO_CLKIN0 (M8)
Almador EDS Rev 0.9 Apr.7

DVOA_D5 Int. P/D	0 = DESKTOP 1 = MOBILE	Pull-up 2.2K to V1.5S
DVOA_D6 Int. P/D	0 = Dual ended term. 1 = Single ended term.	Pull-up 2.2K to V1.5S
DVOA_D0 Int. P/U	0 = 200MHz 1 = 133MHz	Pull-down 2.2K to GND
DVOA_D1 Int. P/U	0 : IOQD = 1 1 : IOQD = 8	Pull-down 2.2K to GND

DVOA_D7 Int. P/D	0 : Normal mode 1 : Invoking the XOR Chain test mode
DVOA_D8 Int. P/D	0 : Normal mode 1 : Tri-stating all GMCH outputs when ICH3-M is in XOR Chain mode.

Per Intel GMCH EDS Rev0.7 12/22/2K

Add pull-ups to +1.5VRUN on G_FRAME#, G_IRDY#, G_TRDY#, G_DEVSEL# in SVT planar

Almador checklist v0.93 9/08

Be close to pin RDDP 1.0

4.7K RDDP1.0 P.72

9/13 per Intel

DVO port of GMCH is +1.5V Power plane

DVO port of VCH is +1.8V Power plane

DVO_INTR#	Pull-up 100K to 1.5VRUN	Pull-up/down required if DVOA not implemented.
DVO_FIELD	Pull-down 100K to GND	
DVO_CLKIN	Pull-up 100K to 1.5VRUN	

DDC1CLK DDC1DAT	Pull-up 2.2K to +5VRUN	Non-5V tolerant, Q-Switch required for 5V support
DDC2CLK DDC2DAT	Pull-up 10K to +5VRUN	
I2CCLK I2CDATA	Pull-up 10K to +3VRUN	

KODIAK 0.7b P.9 33MHz OSC
9/13 change to 32K OSC per Intel

Pull-up required for ext. AGP GFX and int. DVO GFX

Connect pin AE20, G24(VSSA_DPLL[0,1]) to the respective decoupling caps of pin AC20, F25(VCCA_DPLL[0,1])

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Title: GMCH(2/3)
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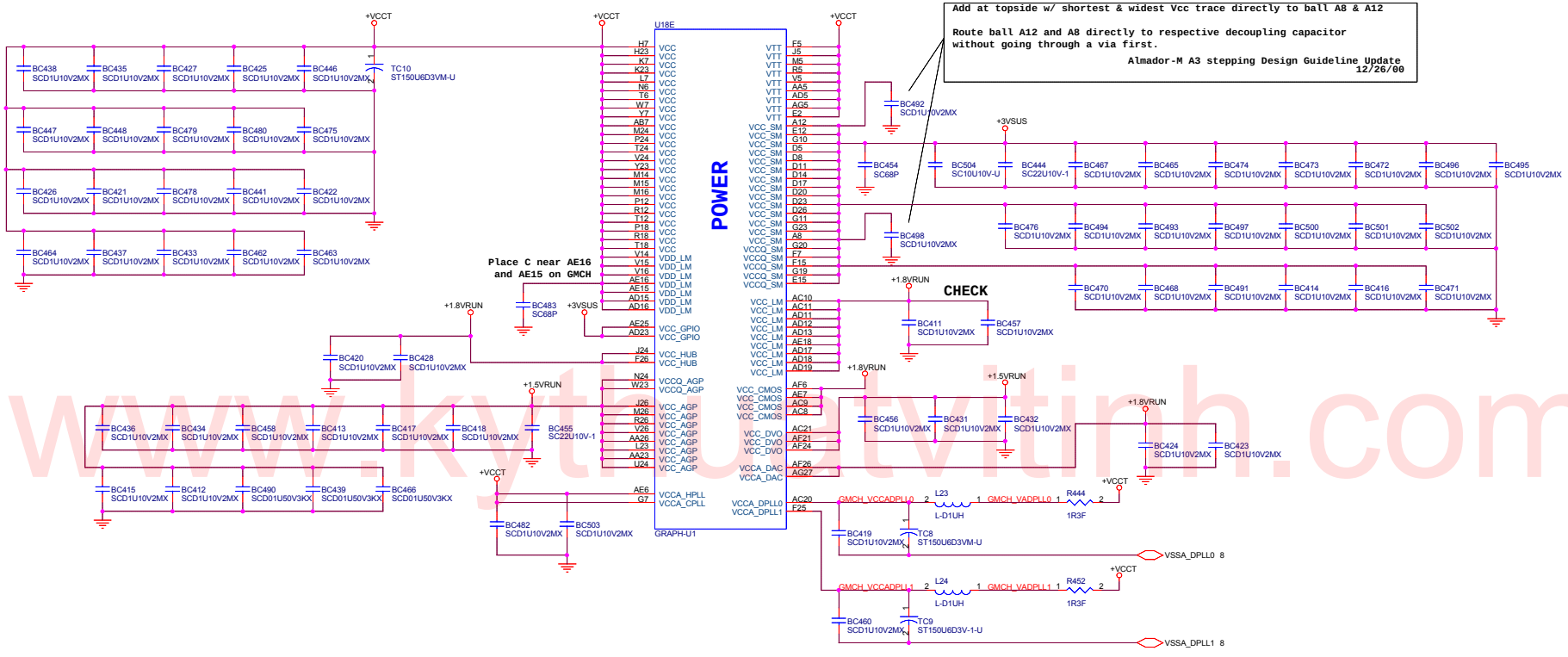
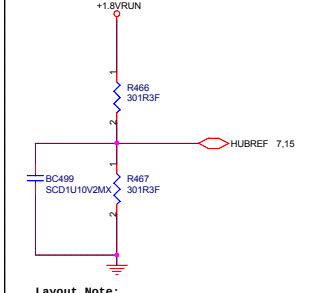


Decouping Recommendation

				C-Note 2	Kenora Ver 0.93
V1.2S_GMCH	Decoupling Caps	0.1uF * 10	Distribute as close as possible to GMCH-M processor Quadrant	0.1uF * 20 150uF / 6.3V * 2 68pF * 1 220uF / 2.5V * 2	0.1uF * 20
	Bulk Caps	10uF * 1			150uF / 4V * 5 + 1 * NS
V1.2S_GMCHCORE	Decoupling Caps	68pF * 1	Close to VDD_LM, near pins AE15 and AE16 on Almador		68pF * 1
		0.1uF * 10			0.1uF * 28
	Bulk Caps	10uF * 1			150uF / 4V * 6
V1.5S_GMCH	Decoupling Caps	0.1uF * 9 82pF * 4	Distribute as close as possible to GMCH-M AGP/DVO Quadrant	0.1uF * 11 0.01uF * 3 10uF /10V * 1	0.1uF * 9 82pF * 4
	Bulk Caps			22uF /10V * 1	22uF / 20V * 1
V1.8S_GMCH	Decoupling Caps	0.1uF * 4 + 2 82pF * 2	Distribute as close as possible to GMCH-M Local Memory Quadrant Additional 4* 0.1uF shall be distributed as close as possible to VCCPCMOS_LM	0.1uF * 6	0.1uF * 4 + 2 0.01uF *2 82pF * 2 22uF / 20V * 2
	Bulk Caps				68uF / 10V * 5
V3_GMCH	Decoupling Caps	0.1uF * 12 + 2 82pF * 4	Distribute as close as possible to GMCH-M System Memory Quadrant Additional 4* 0.1uF shall be distributed as close as possible to IO Quadrant	0.1uF * 20+2 22uF 10V * 1 10uF 10V * 1 82pF * 1	0.1uF * 12 + 2 82pF * 4 22uF / 20V * 2
	Bulk Caps				

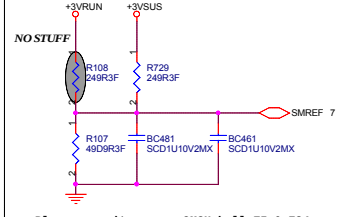
Almador-M Checklist Ver. 0.93 9/08

HUB INTERFACE REF 1/2*1.8V



Layout Note:
Place divider pair in middle of bus.
Place capacitors near GMCH.

SYSTEM MEMORY REF 0.55V



Place capacitor near GMCH ball E5 & F24.

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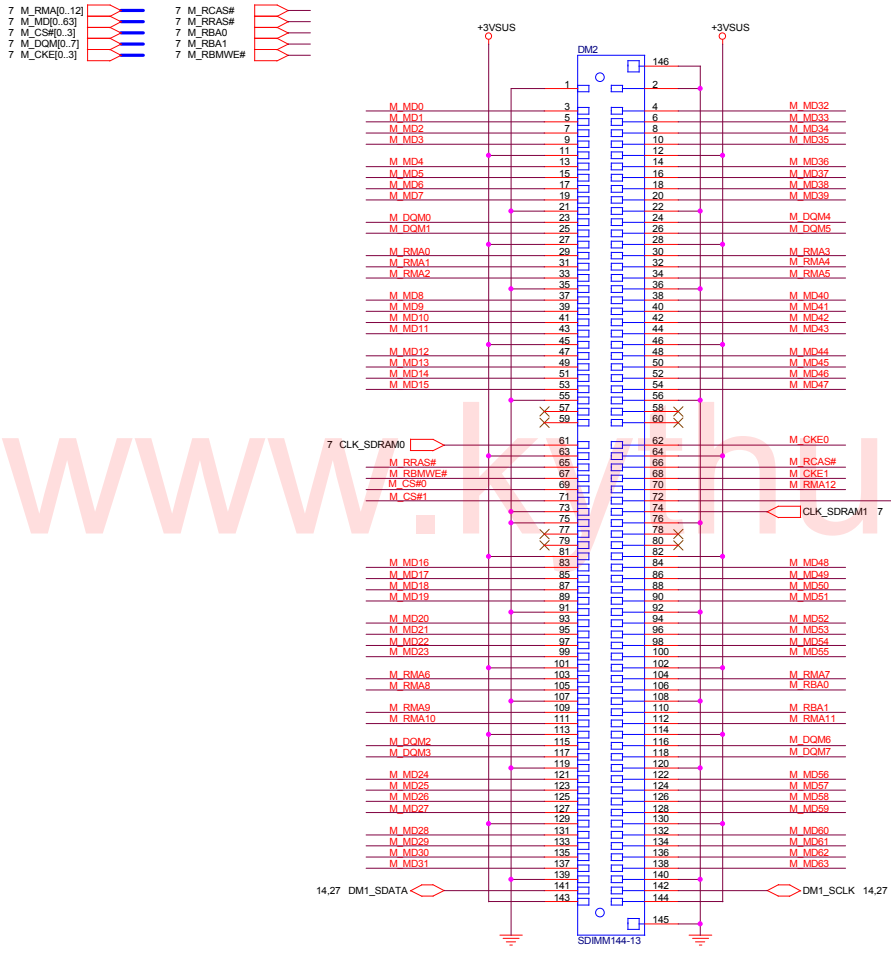
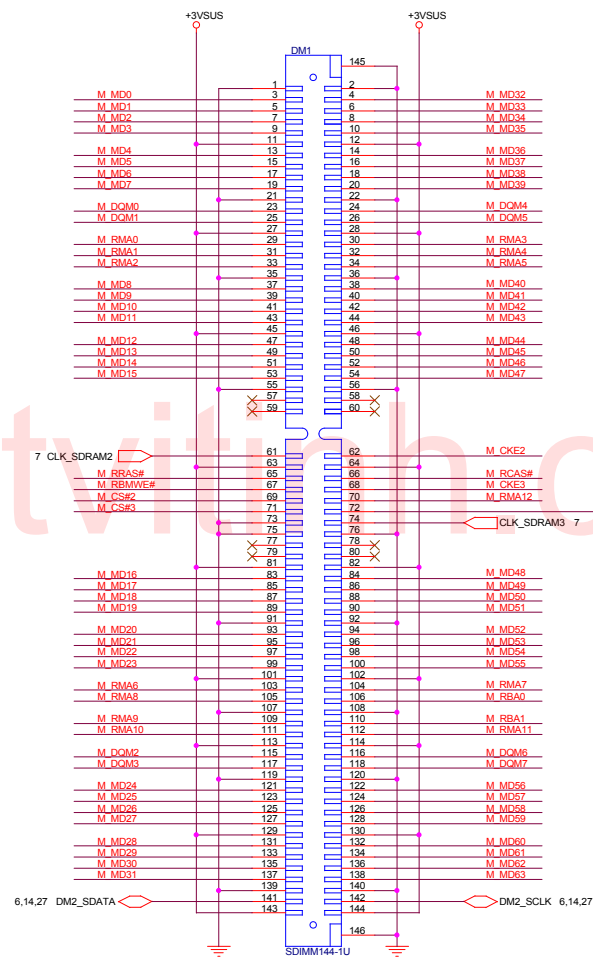
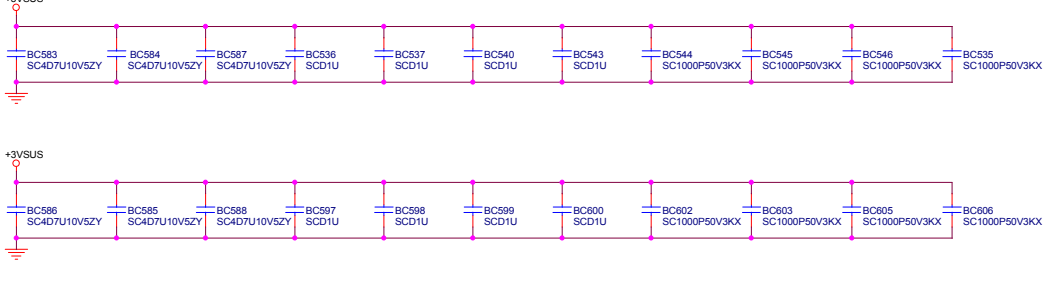
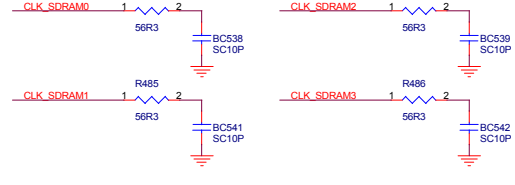
(Normal Type)



(Reverse Type)







SDRAM clock AC terminations change from 33 Ohm 22p to 56 Ohm 10p.

12/14/00

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Title: **SO-DIMM**

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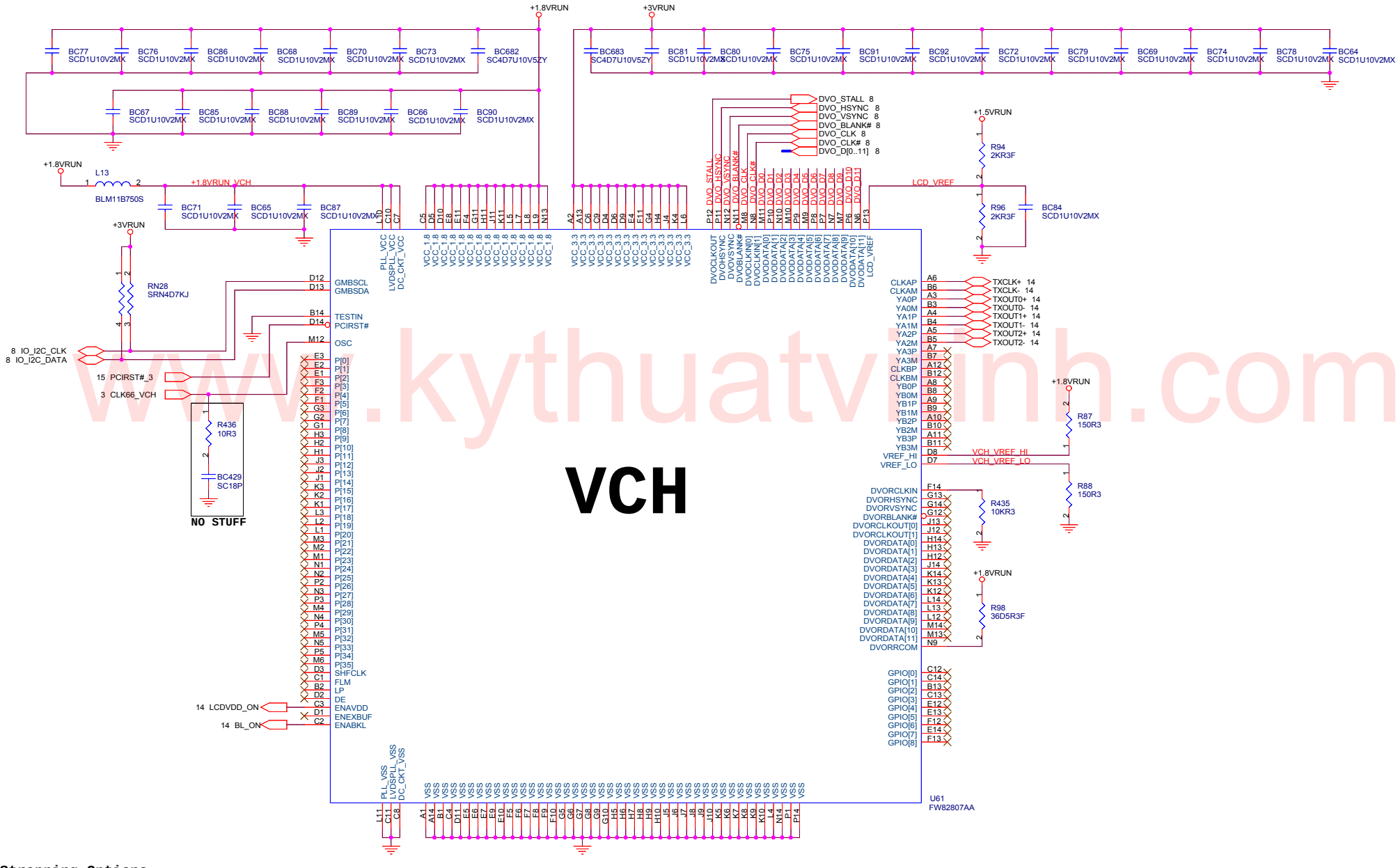

Strapping Options

GPIO[5:2]	10 - 4.7K Ohm	Can be used for panel ID select. Default state is GPI w/ int. weak pull down.
GPIO6	10 - 4.7K Ohm	For normal VCH operation pin has to be read as low. Default state is GPI w/ int. weak pull down.
GPIO[8:7]	10 - 4.7K Ohm	Used for GMBus base address select. Default state is GPI w/ int. weak pull down.

Almador checklist ver.0.93

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Title: VCH

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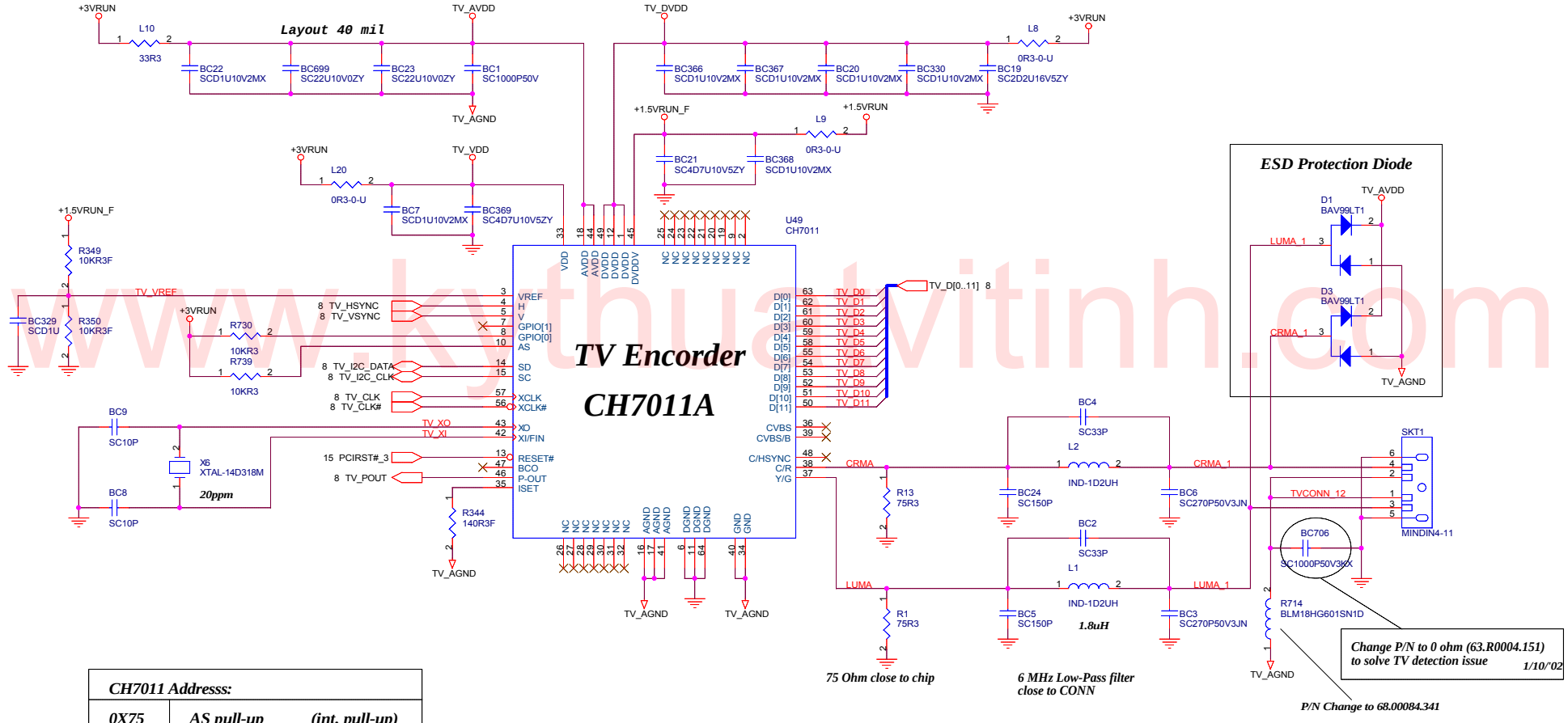

CH7011 Addresss:		
0X75	AS pull-up	(int. pull-up)
0X76	AS pull-down	

Power up default:		
NTSC	GPIO0 pull-up	(int. pull-up)
PAL	GPIO0 pull-down	

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Title: TV Encorder

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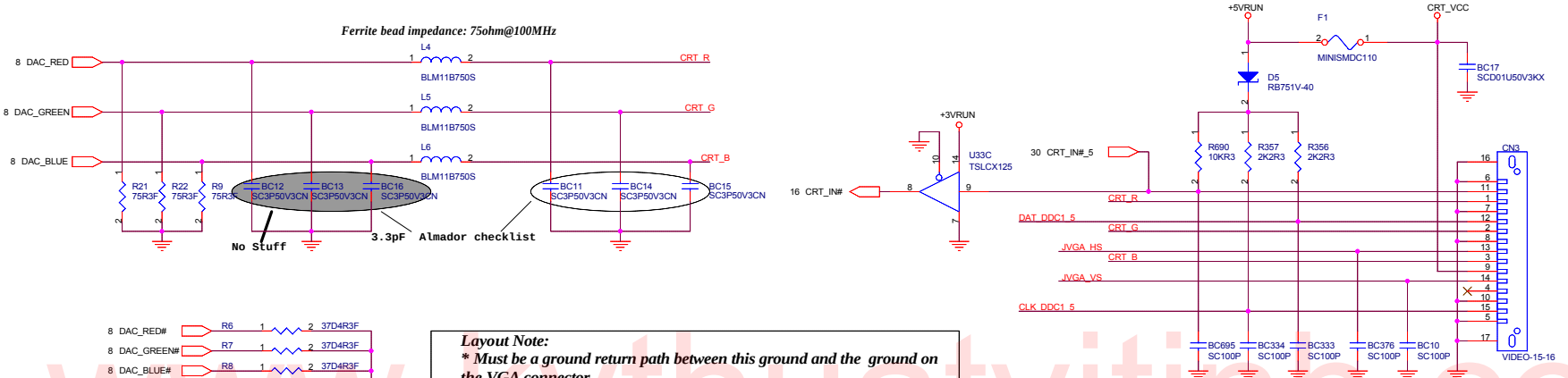
CRT I/F & CONN

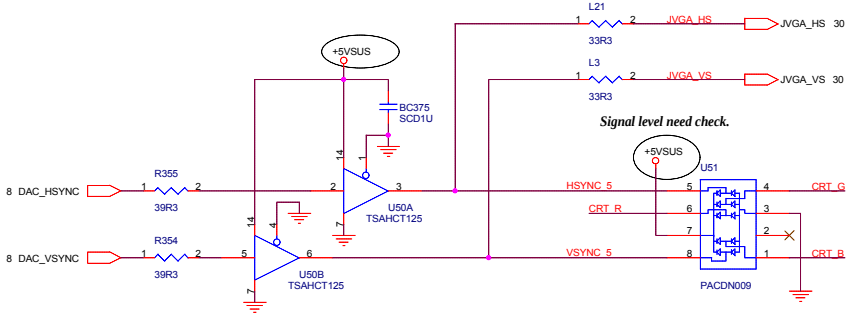


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
**** 37.4_1% resistors must be placed at the same place as the RGB 75 Ohm pull-down resistors.***

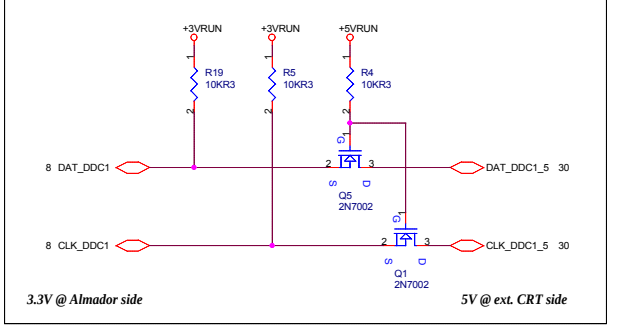
Pi-filter & 75 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

RDDP 1.0

Hsync & Vsync level shift



DDC_CLK & DATA level shift



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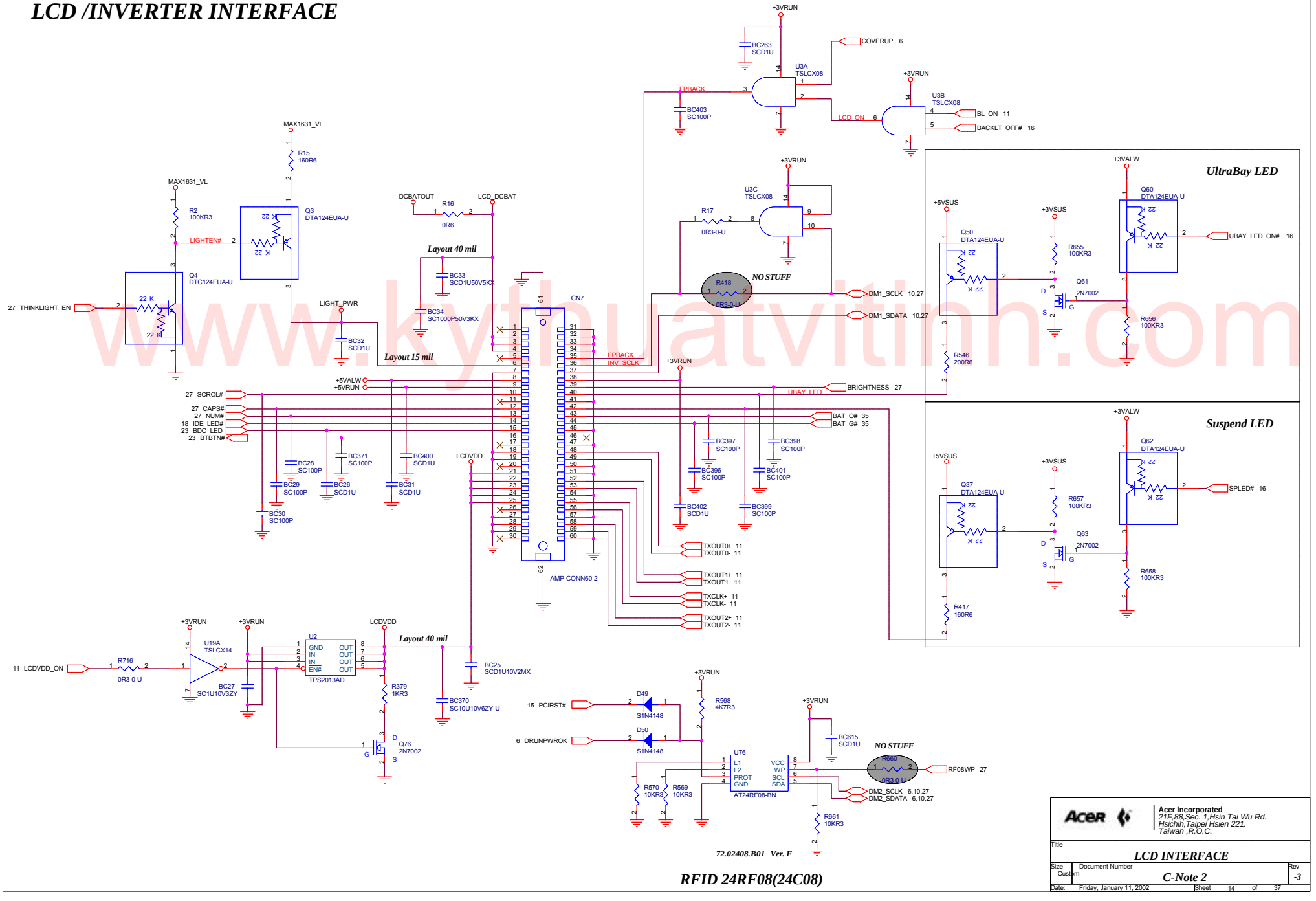
Title	CRT Connector	
Size: Custom	Document Number: C-Note 2	Rev: -3
Date: Friday, January 11, 2002	Sheet 13 of 37	

LCD /INVERTER INTERFACE



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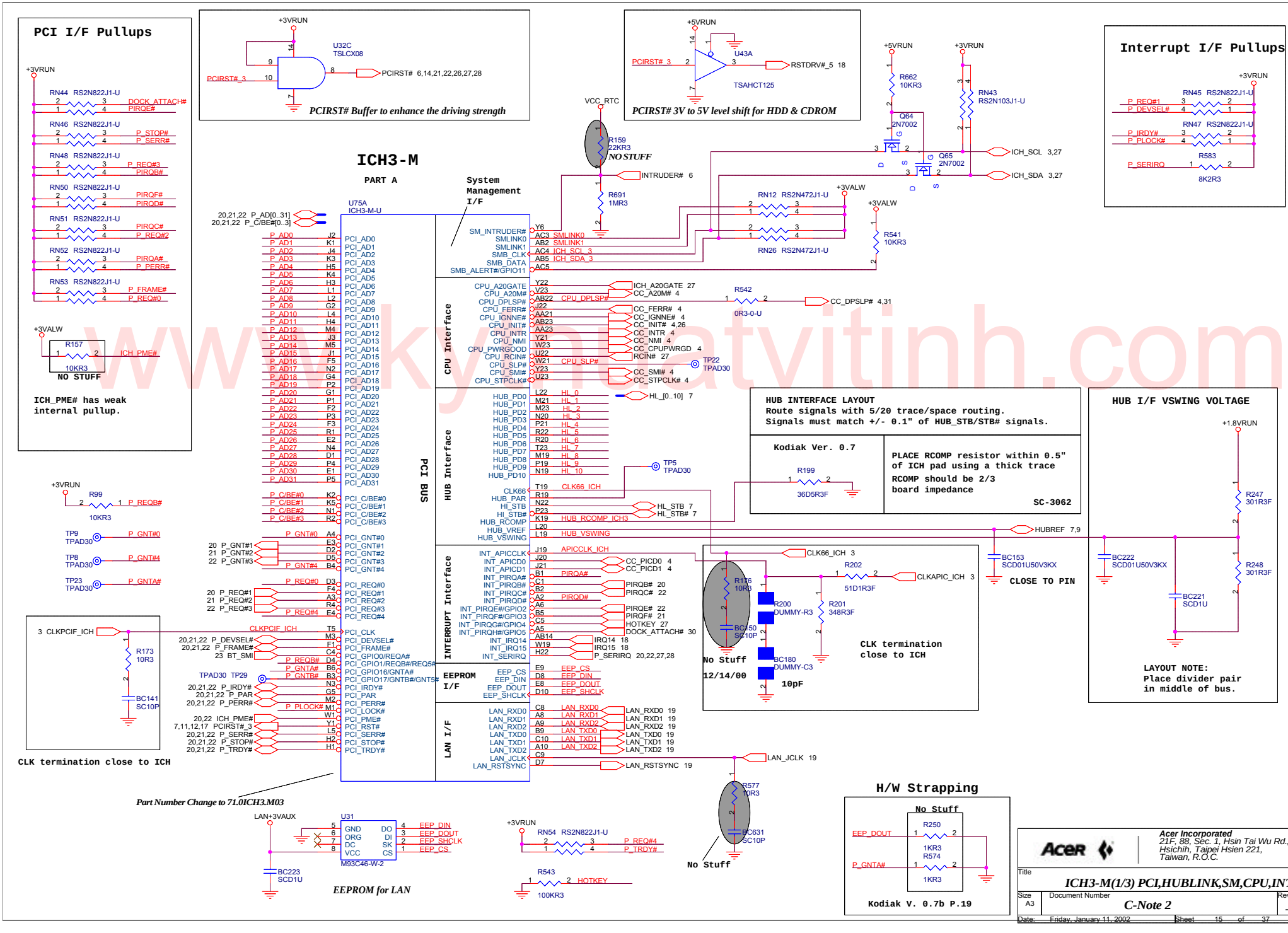
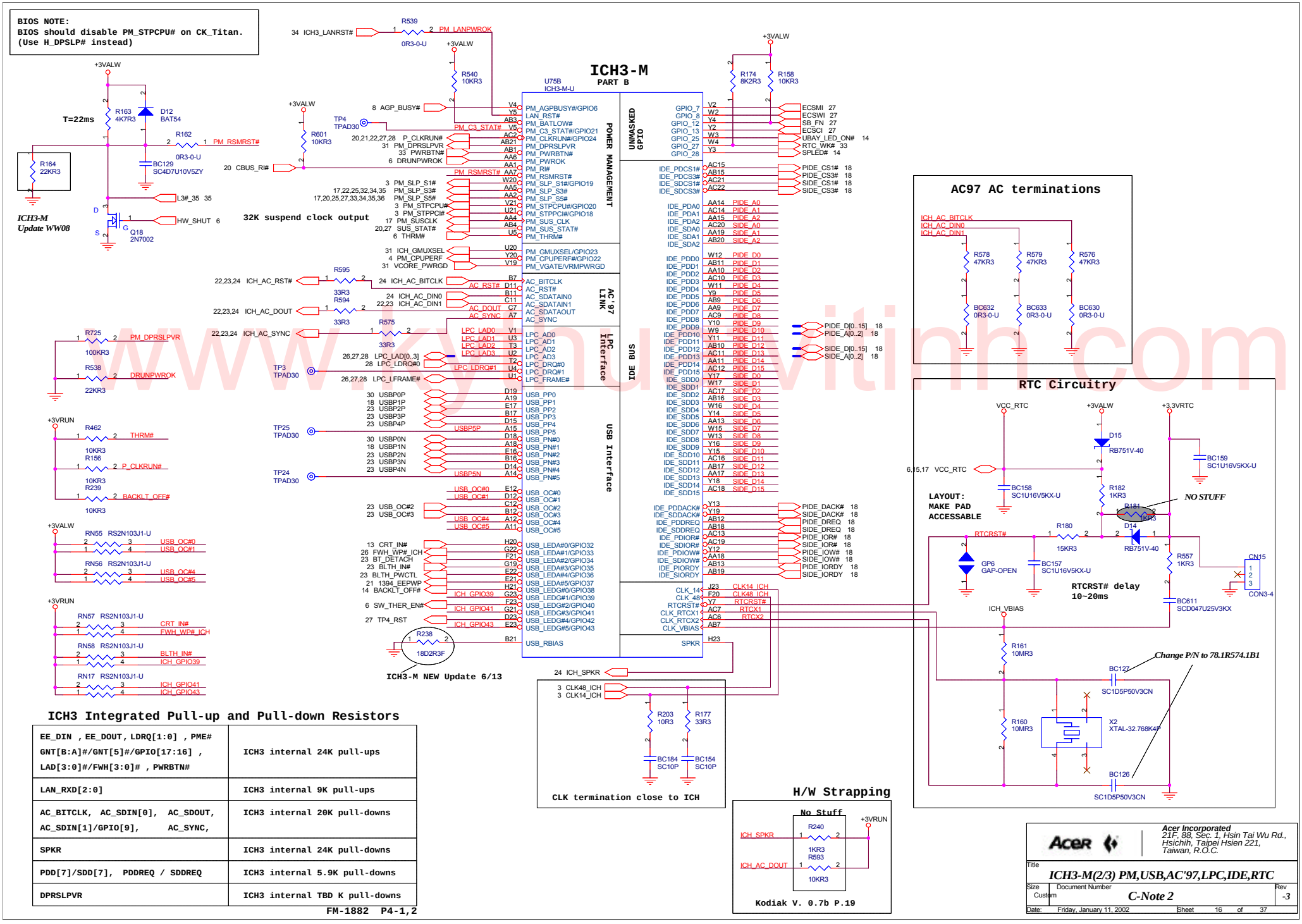
Taiwan ,R.O.C.

Title	LCD INTERFACE	
Size: Custom	Document Number: C-Note 2	Rev: -3
Date: Friday, January 11, 2002	Sheet 14 of 37	



BIOS NOTE:
BIOS should disable PM_STPCPU# on CK_Titan.
(Use H_DPSLP# instead)



ICH3 Integrated Pull-up and Pull-down Resistors

EE_DIN , EE_DOUT, LDRQ[1:0] , PME# GNT[B:A]#/GNT[5]#/GPIO[17:16] , LAD[3:0]#/FWH[3:0]# , PWRBTN#	ICH3 internal 24K pull-ups
LAN_RXD[2:0]	ICH3 internal 9K pull-ups
AC_BITCLK, AC_SDIN[0], AC_SDOUT, AC_SDIN[1]/GPIO[9], AC_SYNC,	ICH3 internal 20K pull-downs
SPKR	ICH3 internal 24K pull-downs
PDD[7]/SDD[7], PDDREQ / SDDREQ	ICH3 internal 5.9K pull-downs
DPRSLPVR	ICH3 internal TBD K pull-downs

FM-1882 P4-1,2

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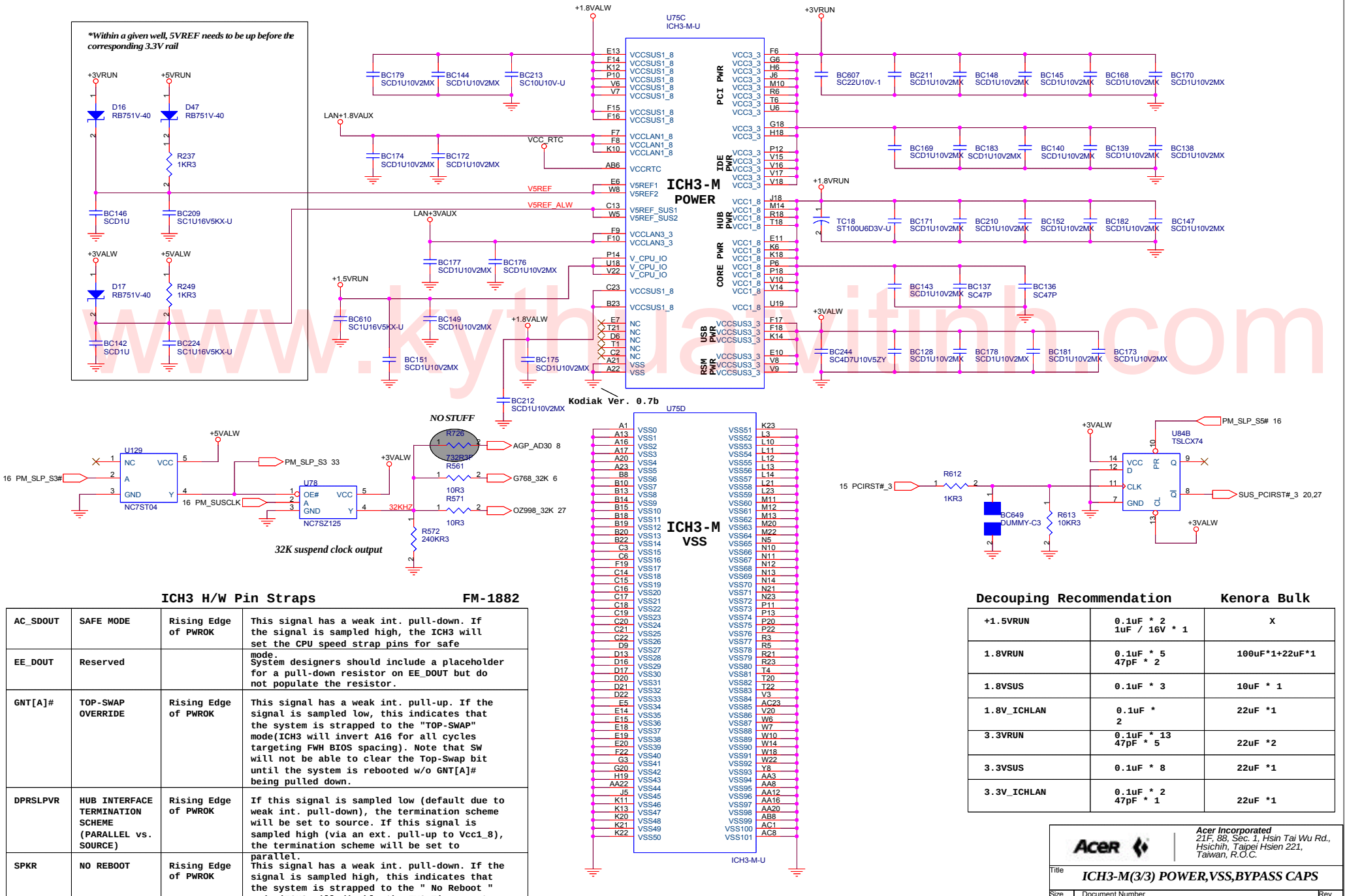
Taiwan, R.O.C.

Title: ICH3-M(2/3) PM,USB,AC'97,LPC,IDE,RTC

Size: Custom | Document Number: C-Note 2 | Rev: -3

Date: Friday, January 11, 2002 | Sheet 16 of 37



ICH3 H/W Pin Straps — FM-1882

AC_SDOUT	SAFE MODE	Rising Edge of PWROK	This signal has a weak int. pull-down. If the signal is sampled high, the ICH3 will set the CPU speed strap pins for safe mode.
EE_DOUT	Reserved		System designers should include a placeholder for a pull-down resistor on EE_DOUT but do not populate the resistor.
GNT[A]#	TOP-SWAP OVERRIDE	Rising Edge of PWROK	This signal has a weak int. pull-up. If the signal is sampled low, this indicates that the system is strapped to the "TOP-SWAP" mode(ICH3 will invert A16 for all cycles targeting FWH BIOS spacing). Note that SW will not be able to clear the Top-Swap bit until the system is rebooted w/o GNT[A]# being pulled down.
DPRSLPVR	HUB INTERFACE TERMINATION SCHEME (PARALLEL vs. SOURCE)	Rising Edge of PWROK	If this signal is sampled low (default due to weak int. pull-down), the termination scheme will be set to source. If this signal is sampled high (via an ext. pull-up to Vcc1_8), the termination scheme will be set to parallel.
SPKR	NO REBOOT	Rising Edge of PWROK	This signal has a weak int. pull-down. If the signal is sampled high, this indicates that the system is strapped to the " No Reboot " mode (ICH3 will disable the TXO Timer system reboot feature).

Decouping Recommendation — Kenora Bulk

+1.5VRUN	0.1uF * 2 1uF / 16V * 1	X
1.8VRUN	0.1uF * 5 47pF * 2	100uF*1+22uF*1
1.8VSUS	0.1uF * 3	10uF * 1
1.8V_ICHLAN	0.1uF * 2	22uF *1
3.3VRUN	0.1uF * 13 47pF * 5	22uF *2
3.3VSUS	0.1uF * 8	22uF *1
3.3V_ICHLAN	0.1uF * 2 47pF * 1	22uF *1

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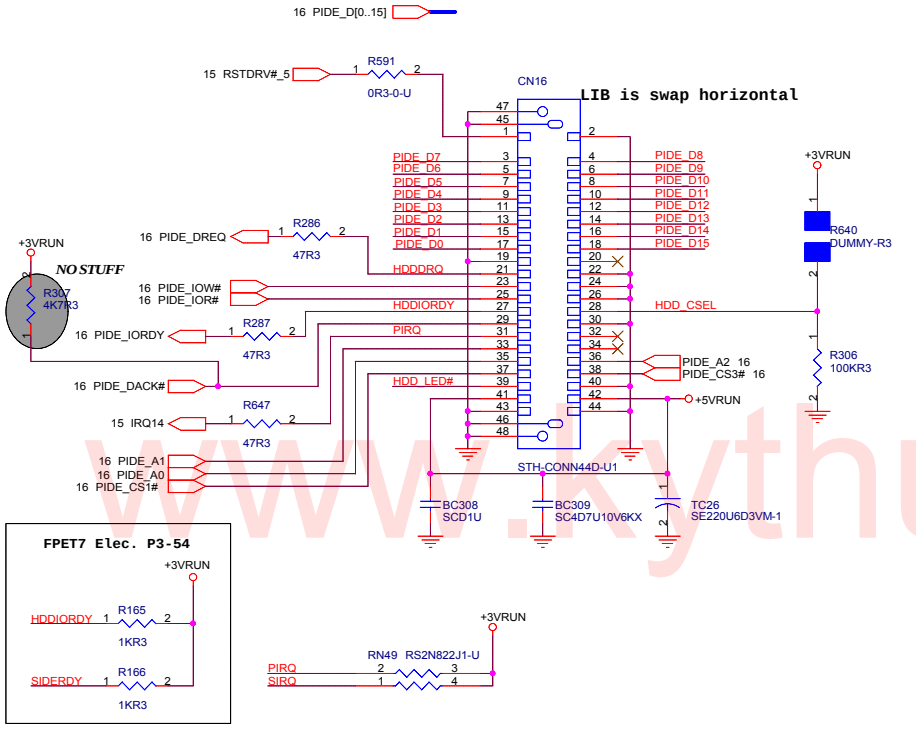
Title: ICH3-M(3/3) POWER,VSS,BYPASS CAPS

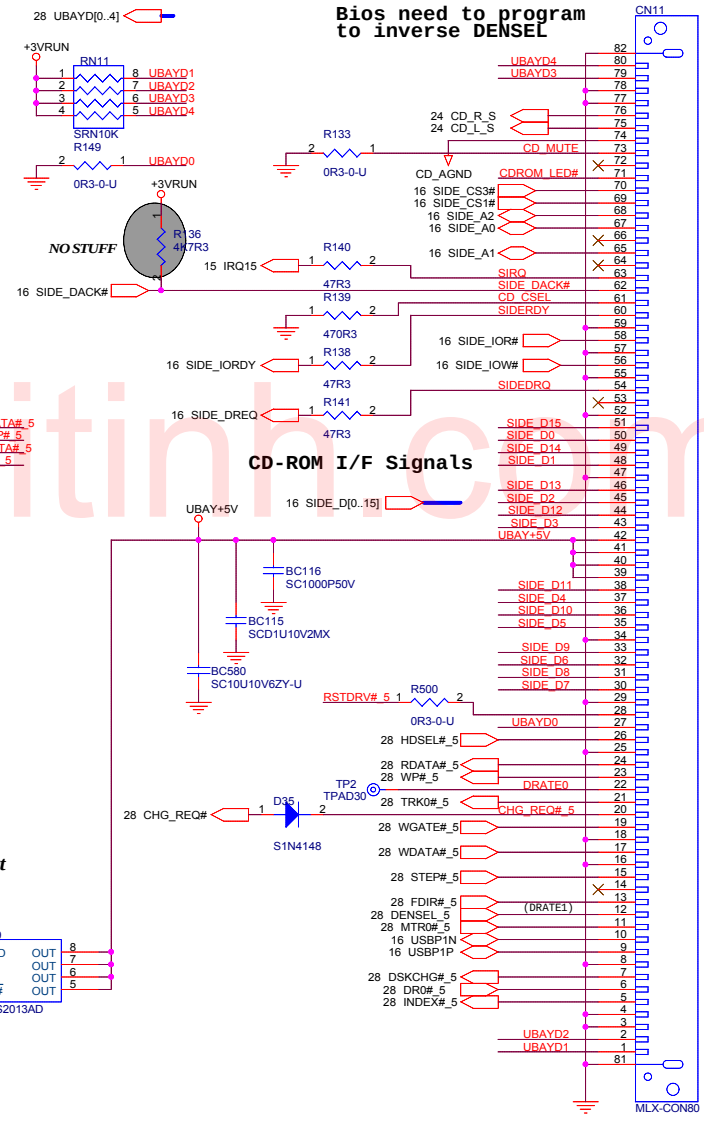
Size: A3 | Document Number: C-Note 2 | Rev: -3

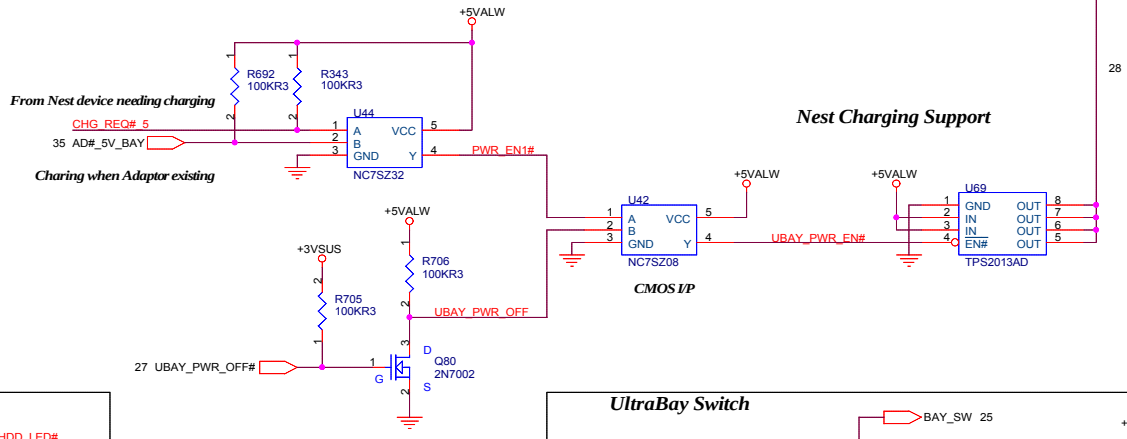
Date: Friday, January 11, 2002 | Sheet 17 of 37

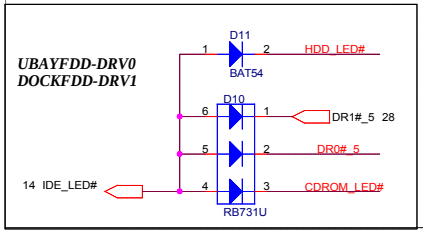
HDD CONN

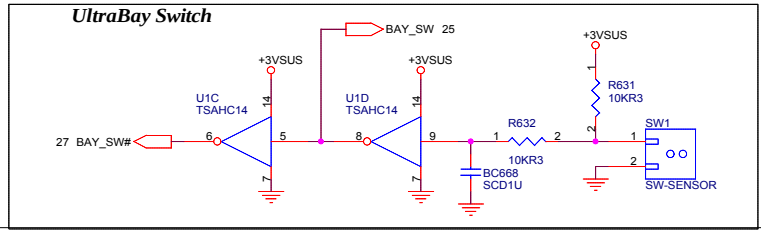


UltraBay CONN









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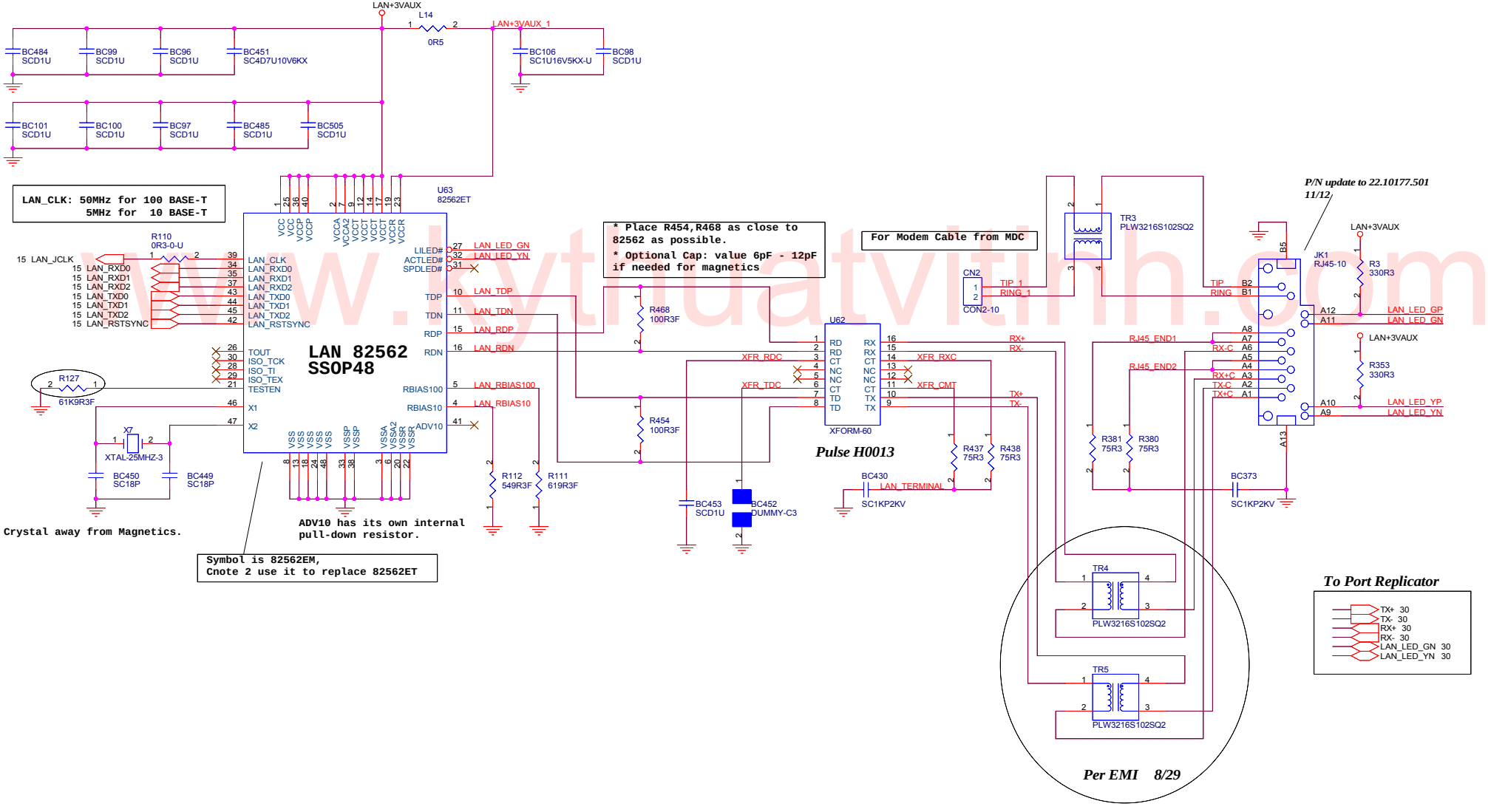
Taiwan ,R.O.C.

Title: IDE & USB INTERFACE

Size	Document Number	Rev
A3	C-Note 2	-3

Date: Friday, January 11, 2002 Sheet 18 of 37



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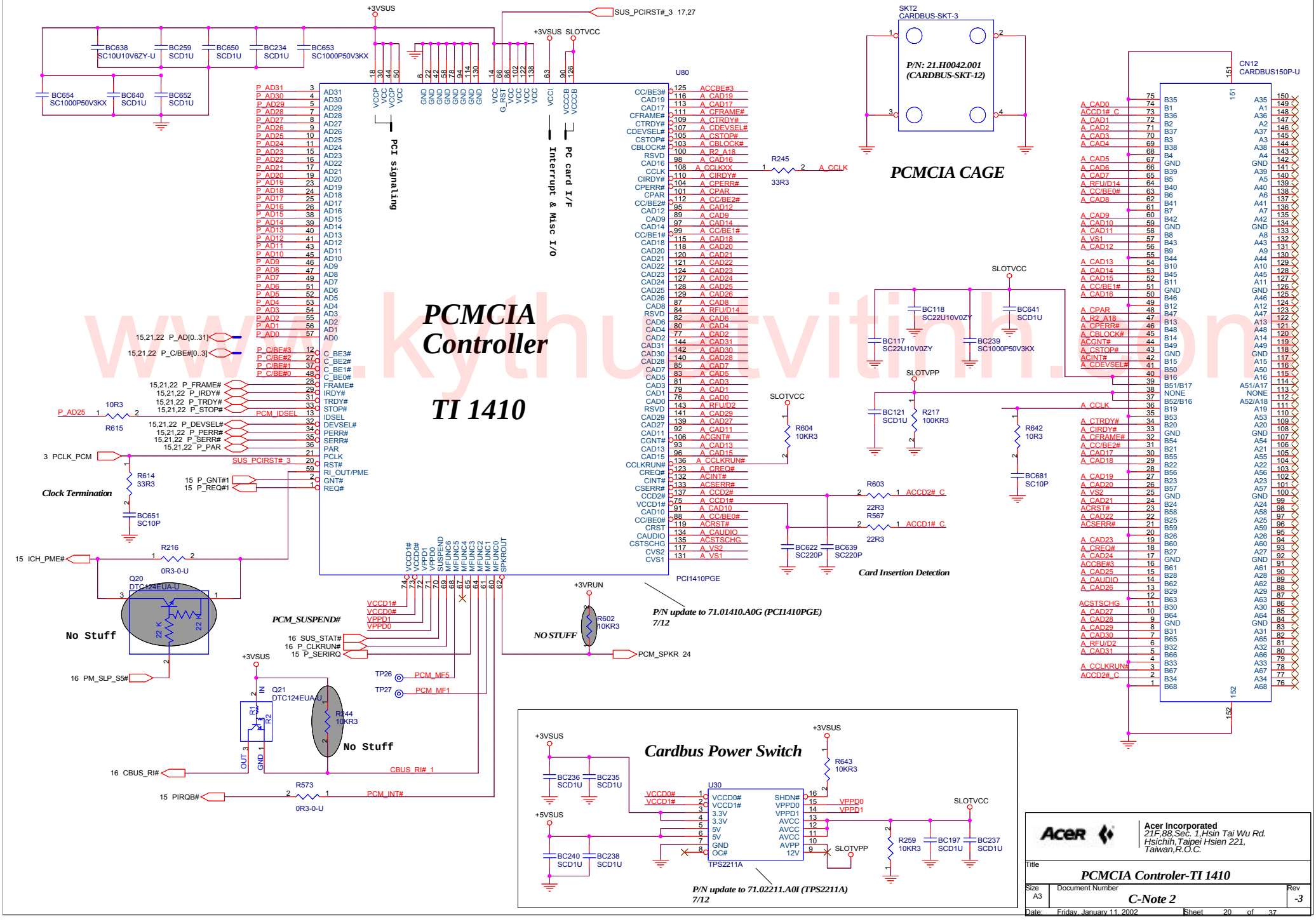
Title	LAN 82562ET
Size	A3
Document Number	C-Note 2
Rev	-3
Date:	Friday, January 11, 2002
Sheet	19 of 37


PCMCIA Controller
TI 1410
PCMCIA CAGE
Cardbus Power Switch
Clock Termination
Card Insertion Detection
No Stuff
PCI signaling
Interrupt & Misc I/O
PC card I/F
PCI1410PGE
TPS2211A
P/N update to 71.01410.A0G (PCI1410PGE) 7/12
P/N update to 71.02211.A0I (TPS2211A) 7/12
SKT2 CARDBUS-SKT-3
P/N: 21.H0042.001 (CARDBUS-SKT-12)
CN12 CARDBUS150P-U
Acer Incorporated
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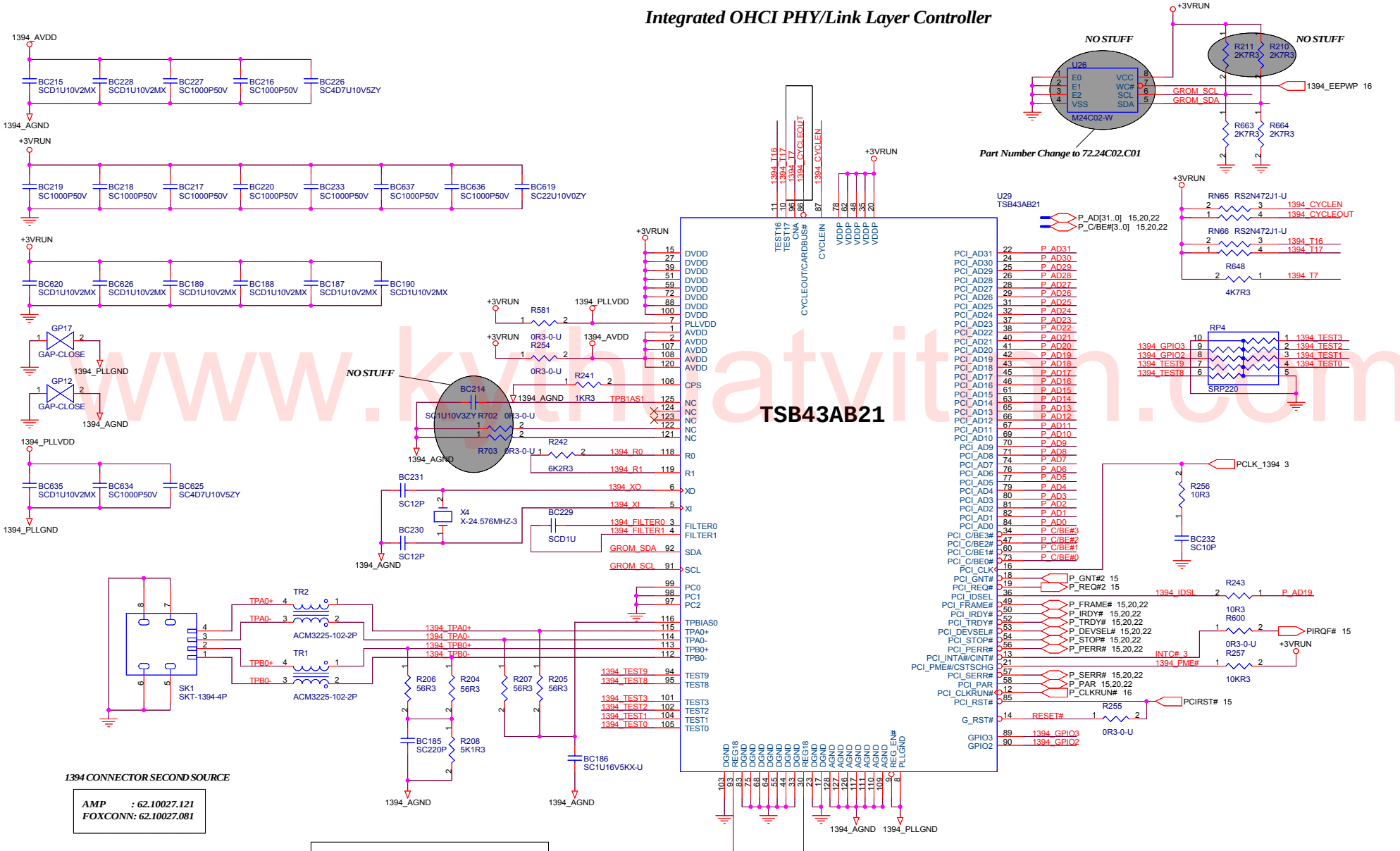
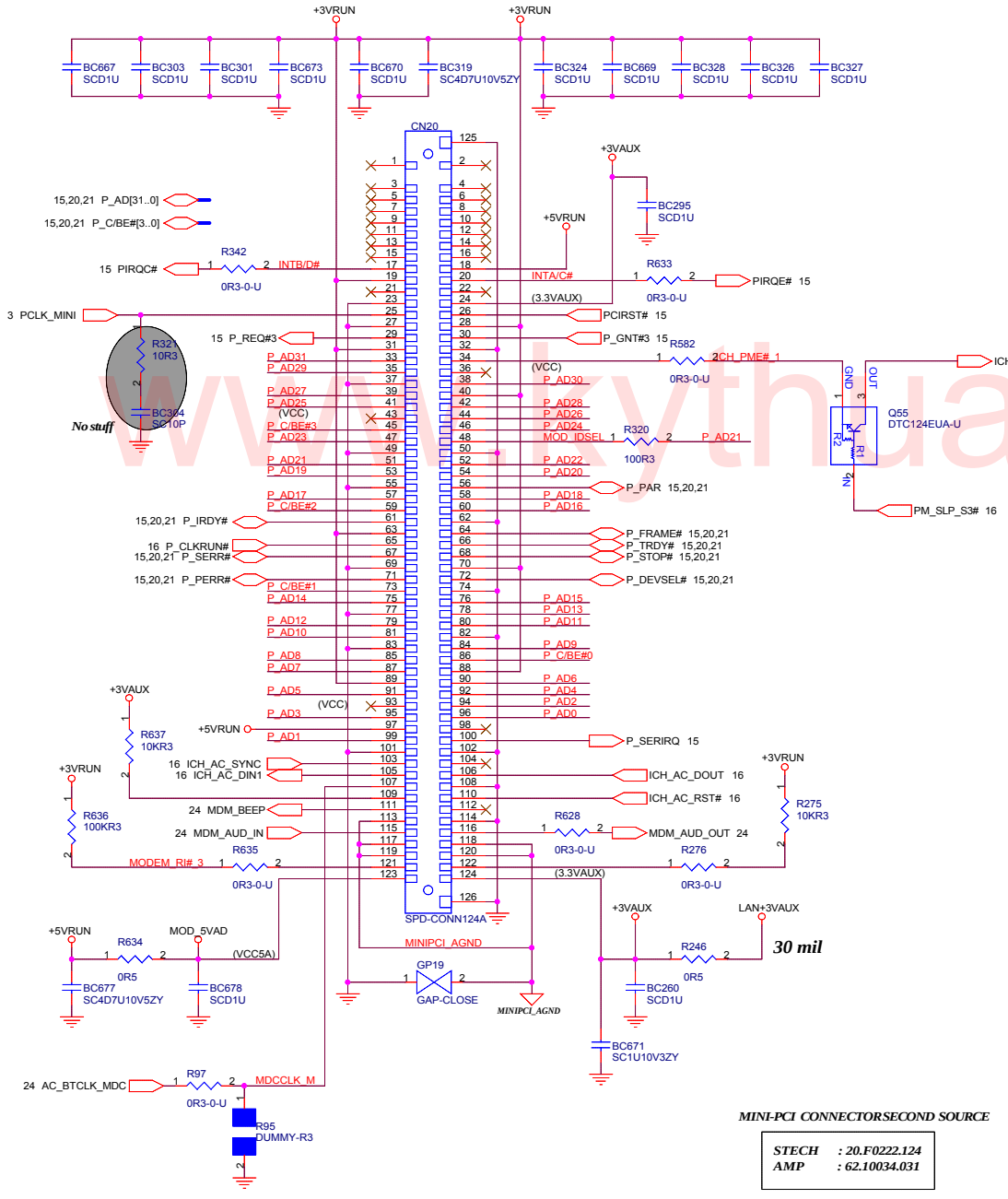
Taiwan,R.O.C.
PCMCIA Controler-TI 1410
C-Note 2
Friday, January 11, 2002

Integrated OHCI PHY/Link Layer Controller



MiniPCI Socket

20.F0222.124 4/18



MINI-PCI CONNECTORSECOND SOURCE

STECH	*: 20.F0222.124*
AMP	*: 62.10034.031*

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Title: ***Mini PCI SOCKET & MDC MODEM***

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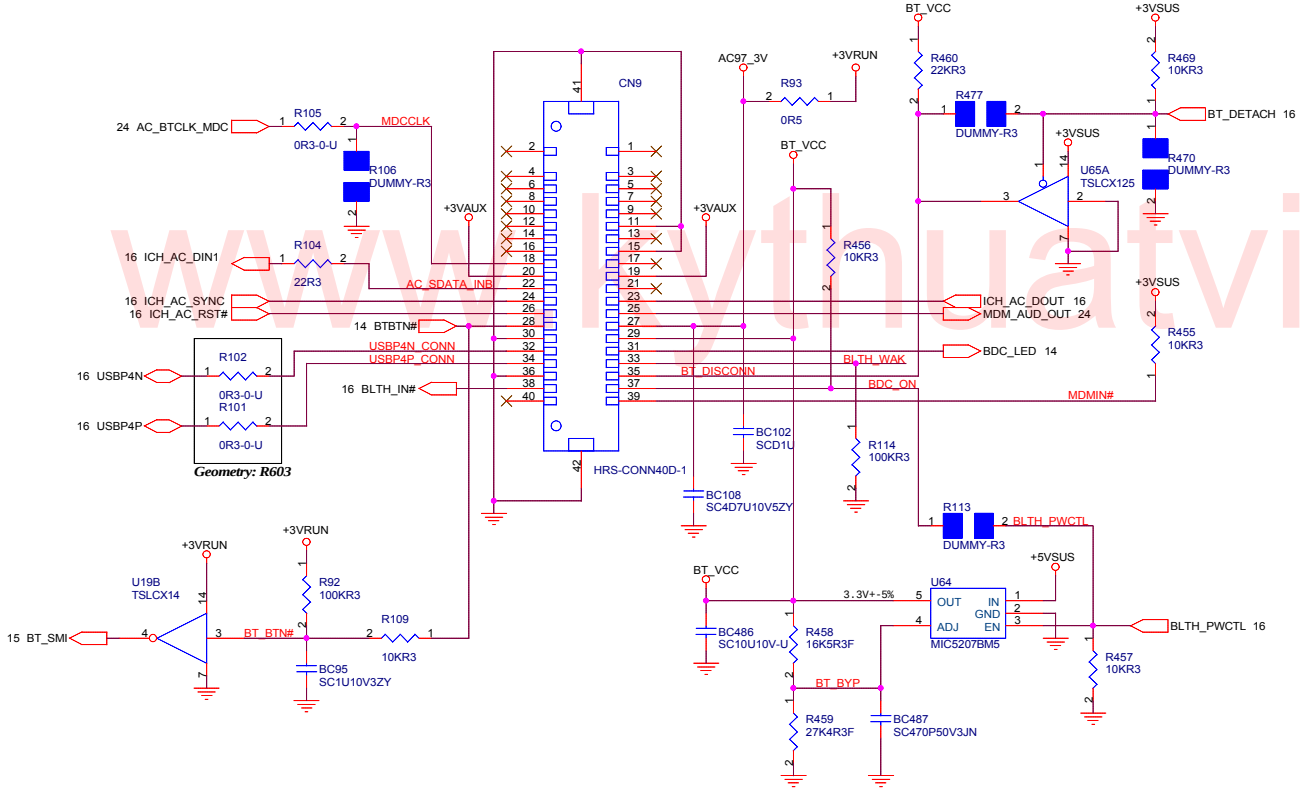
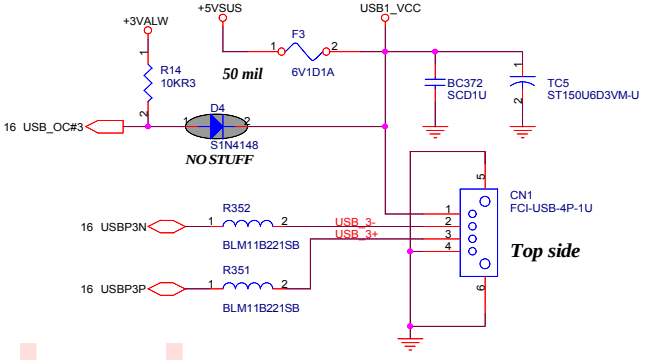
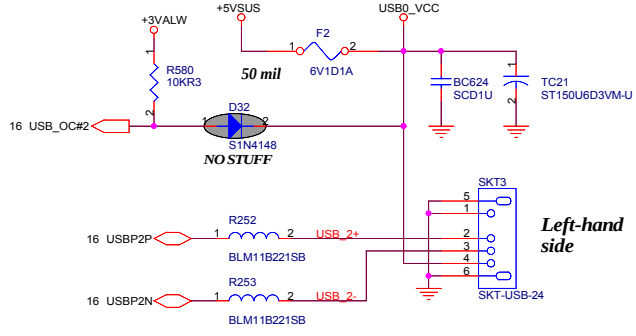
Date: Friday, January 11, 2002 | Sheet 22 of 37

CDC Connector





USB PORT



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Title: BLUETOOTH MODULE

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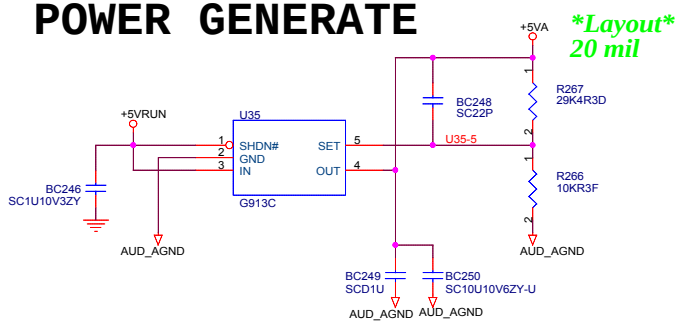
AD1881A AC97 AUDIO CODEC

POWER GENERATE

Layout
20 mil



Layout
AUDIO(analog)
(20,10) mil

Layout
AC-LINK(digital)
6 mil

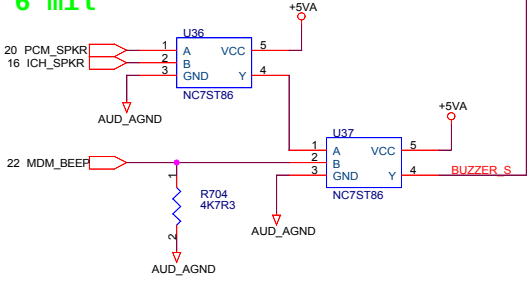
Layout
20 mil

Change P/N to 78.90034.1B1
11/09

Per EMI request
Jan 3 '02

BEEP SOUND LOGIC

Layout
locate near audio moat opening
6 mil



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Title	AC'97 CODEC - AD1881A		
Size A3	Document Number C-Note 2		Rev -3
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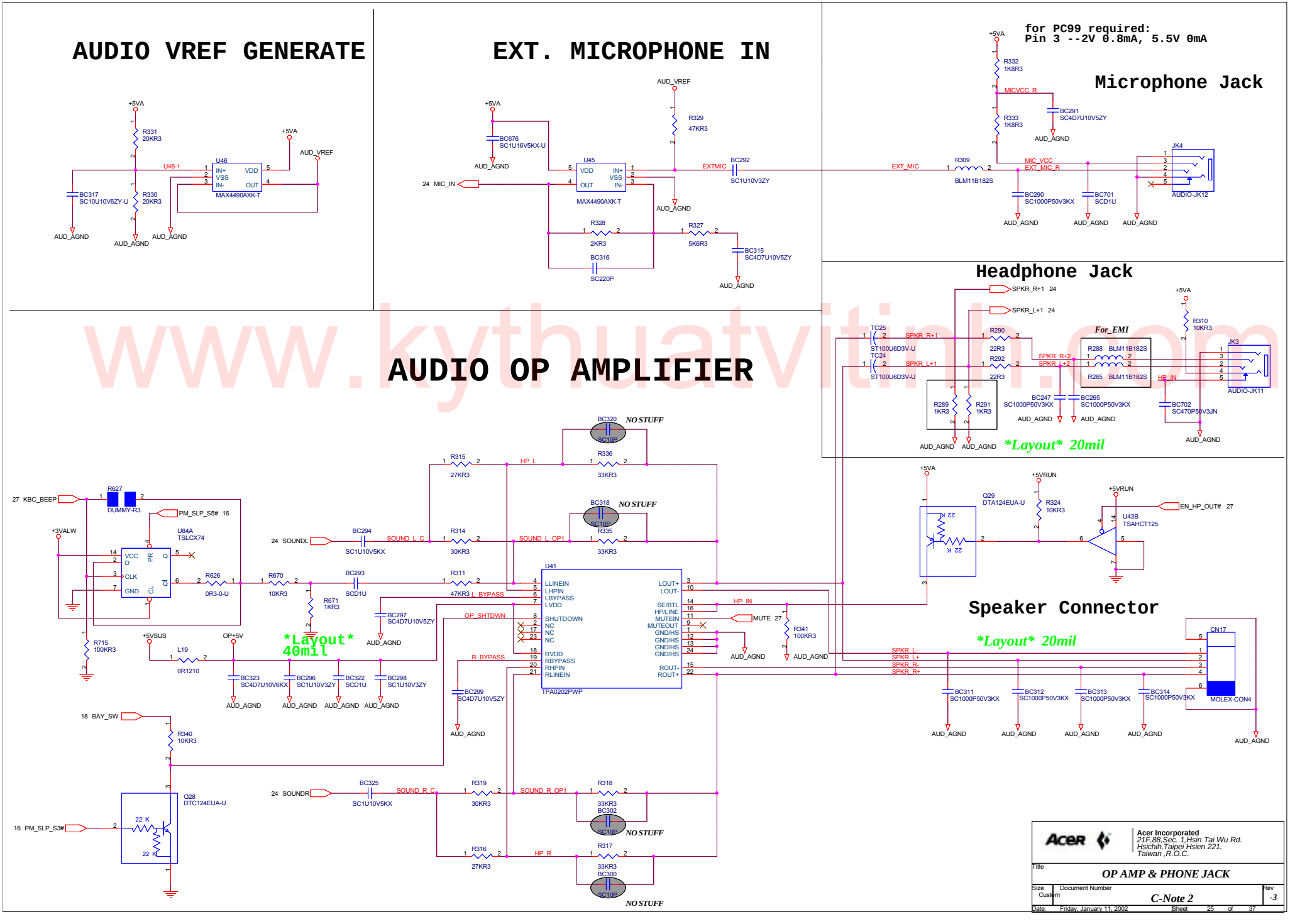
AUDIO VREF GENERATE
EXT. MICROPHONE IN
Microphone Jack
for PC99 required:
Pin 3 --2V 0.8mA, 5.5V 0mA
Headphone Jack
AUDIO OP AMPLIFIER
Speaker Connector
Layout 20mil
Layout 40mil
NO STUFF
www.kythuatvitinh.com
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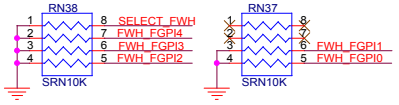
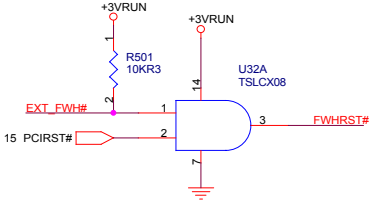
Taiwan ,R.O.C.
OP AMP & PHONE JACK
C-Note 2
Friday, January 11, 2002

Unused FGPI pins must not be float



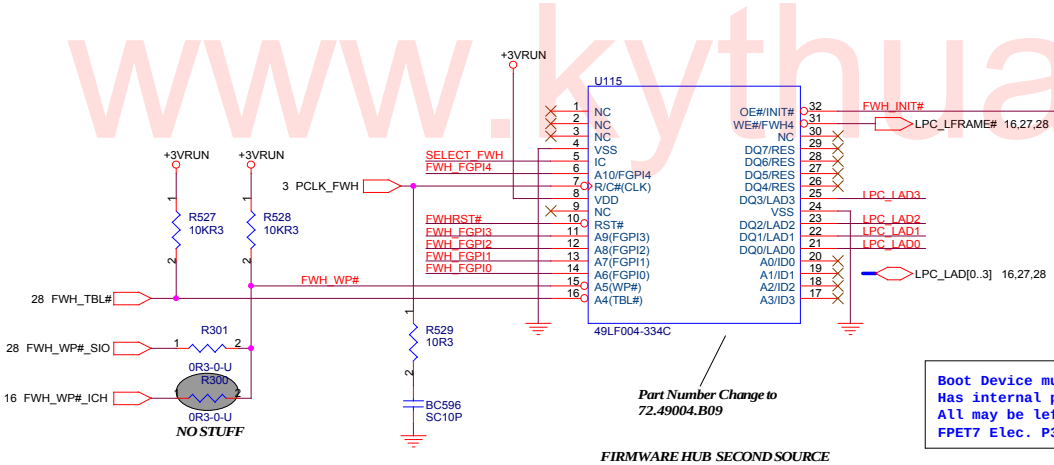


TOP VIEW

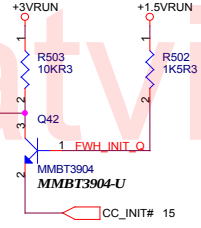
A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

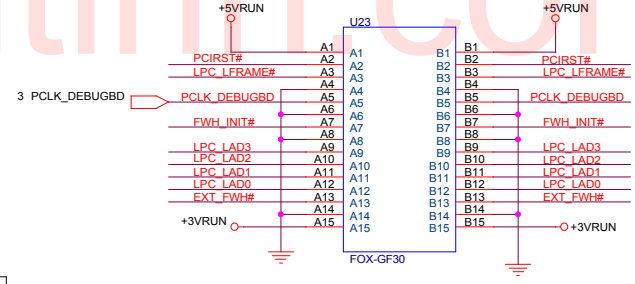
(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD



Part Number Change to 72.49004.B09

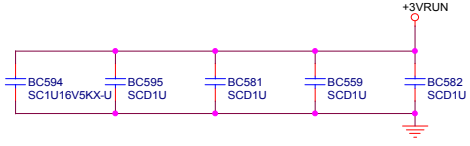


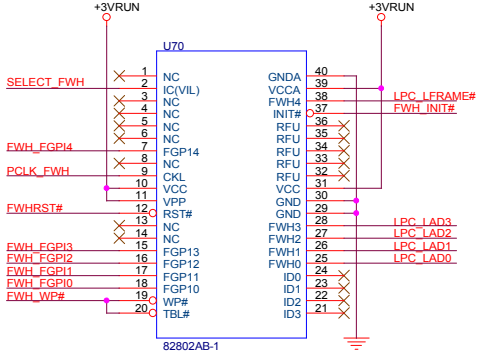


Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

FIRMWARE HUB SECOND SOURCE

SST : 72.49004.B09
STM : 72.50040.009





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Title: *FIRMWARE HUB & DEBUG PORT*

Size	Document Number	Rev
A3	*C-Note 2*	*-3*

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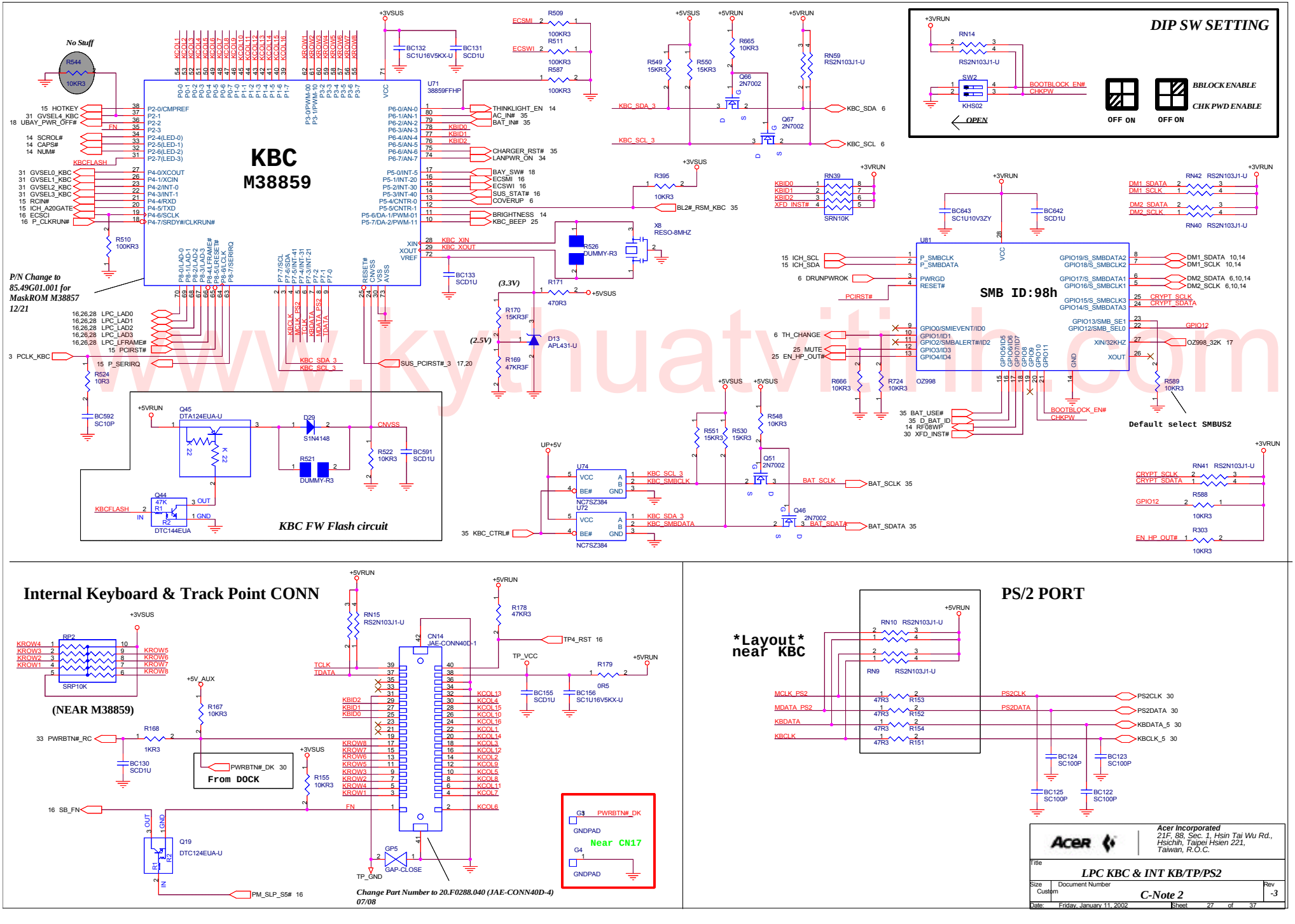

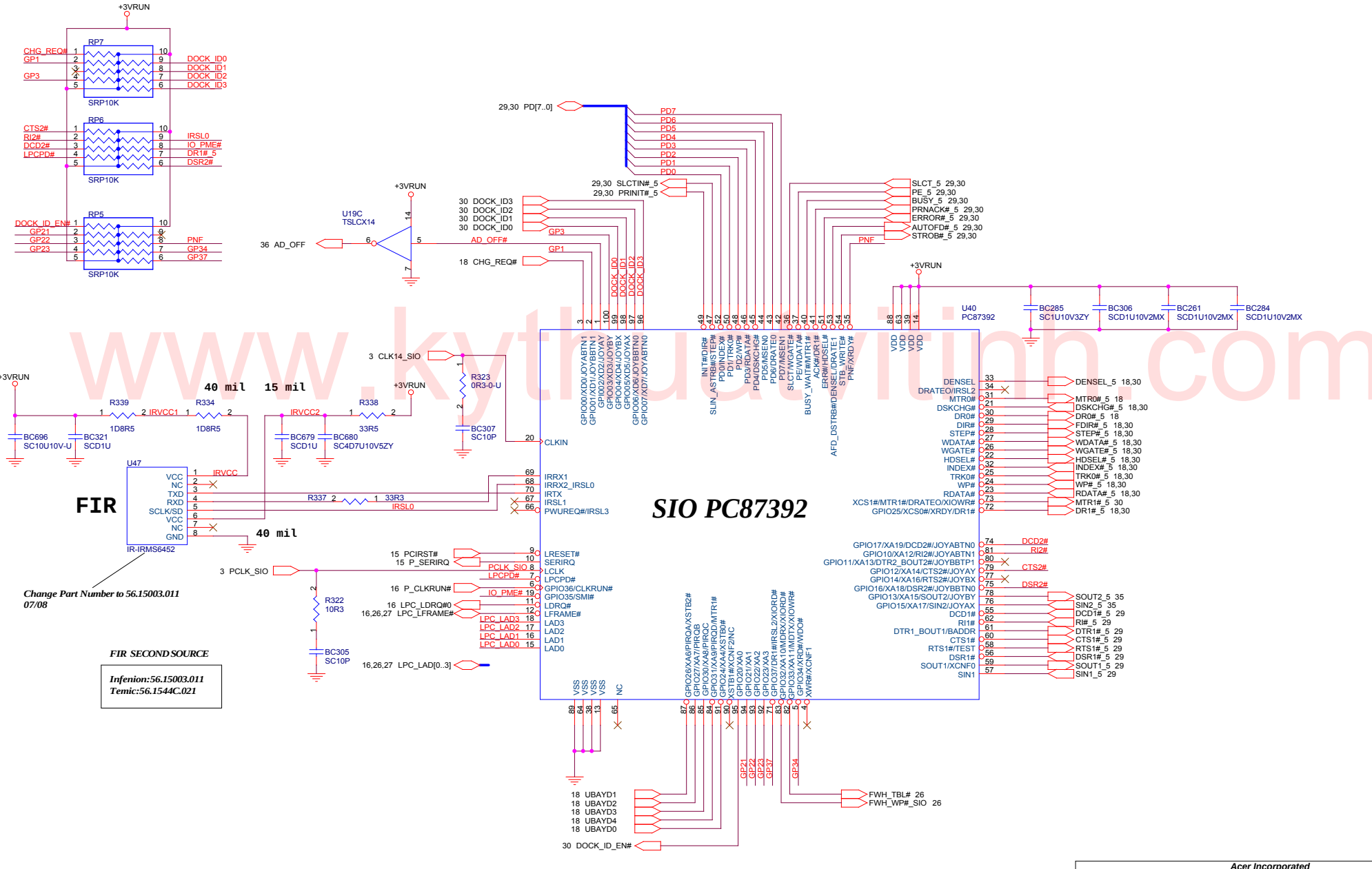

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Taiwan, R.O.C.

Title: LPC SIO

Size: A3 | Document Number: C-Note 2 | Rev: -3

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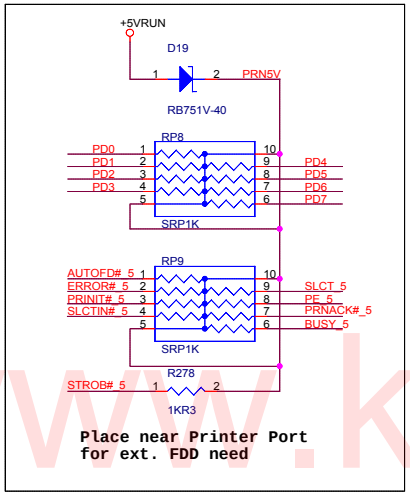
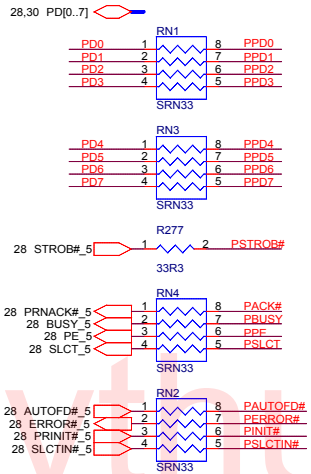
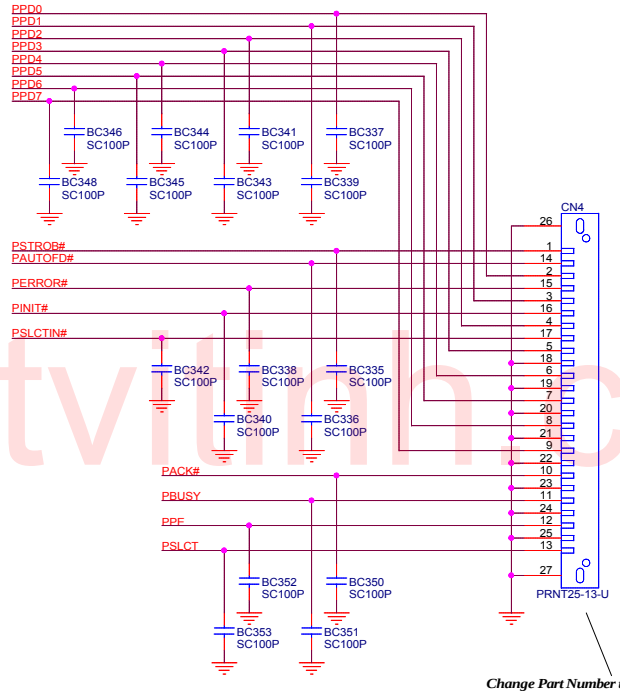


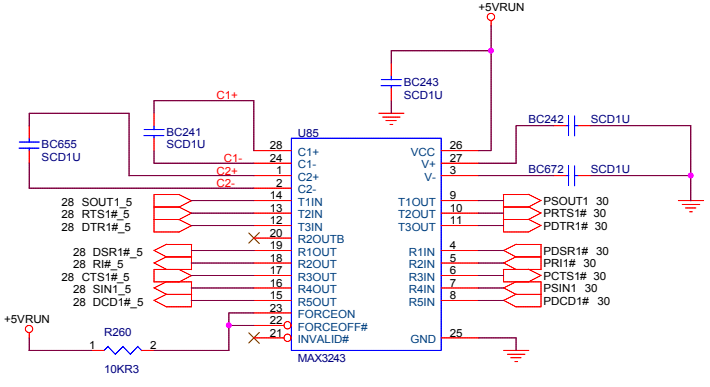


Place CAPs close to CONN

Printer Port



Change Part Number to 20.B0028.025 (AMP-CON25)
07/08



RS232 Transceiver

RS232 SECOND SOURCE

MAXIM:74.03243.0F9
TI :74.03243.FF9

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Taiwan, R.O.C.

Title: ***LPC SIO***

Size	Document Number	Rev
A3	*C-Note 2*	*-3*

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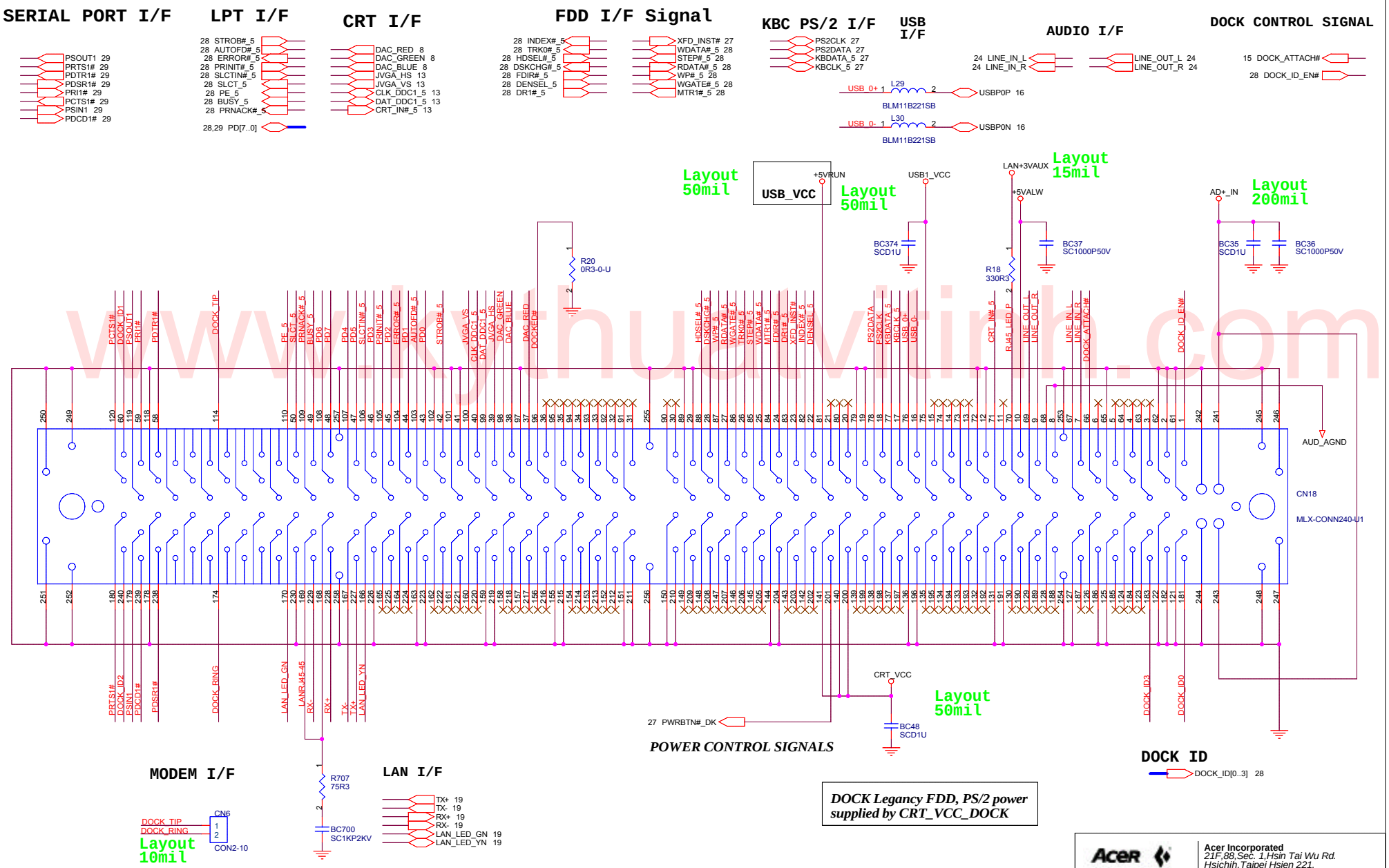
SERIAL PORT I/F
PSOUT1 29
PRTS1# 29
PDTR1# 29
PDSR1# 29
PRI1# 29
PCTS1# 29
PSIN1 29
PDCD1# 29
LPT I/F
28 STROB#_5
28 AUTOFD#_5
28 ERROR#_5
28 PRINIT#_5
28 SLCTIN#_5
28 SLCT_5
28 PE_5
28 BUSY_5
28 PRNACK#_5
28,29 PD[7..0]
CRT I/F
DAC_RED 8
DAC_GREEN 8
DAC_BLUE 8
JVGA_HS 13
JVGA_VS 13
CLK_DDC1_5 13
DAT_DDC1_5 13
CRT_IN#_5 13
FDD I/F Signal
28 INDEX#_5
28 TRK0#_5
28 HDSEL#_5
28 DSKCHG#_5
28 FDIR#_5
28 DENSEL_5
28 DR1#_5
XFD_INST# 27
WDATA#_5 28
STEP#_5 28
RDATA#_5 28
WP#_5 28
WGATE#_5 28
MTR1#_5 28
KBC PS/2 I/F
PS2CLK 27
PS2DATA 27
KBDATA_5 27
KBCLK_5 27
USB I/F
USB_0+ 1
L29
2
USBP0P 16
BLM11B221SB
USB_0- 1
L30
2
USBP0N 16
BLM11B221SB
AUDIO I/F
24 LINE_IN_L
24 LINE_IN_R
LINE_OUT_L 24
LINE_OUT_R 24
DOCK CONTROL SIGNAL
15 DOCK_ATTACH#
28 DOCK_ID_EN#
Layout 50mil
USB_VCC
+5VRUN
USB1_VCC
Layout 50mil
LAN+3VAUX
+5VALW
Layout 15mil
AD+_IN
Layout 200mil
BC374 SCD1U
BC37 SC1000P50V
BC35 SCD1U
BC36 SC1000P50V
R18 330R3
R20 0R3-0-U
AUD_AGND
CN18
MLX-CONN240-U1
CRT_VCC
Layout 50mil
BC48 SCD1U
27 PWRBTN#_DK
POWER CONTROL SIGNALS
DOCK ID
DOCK_ID[0..3] 28
MODEM I/F
DOCK_TIP
DOCK_RING
CN6
CON2-10
Layout 10mil
R707 75R3
BC700 SC1KP2KV
LAN I/F
TX+ 19
TX- 19
RX+ 19
RX- 19
LAN_LED_GN 19
LAN_LED_YN 19
DOCK Legacy FDD, PS/2 power supplied by CRT_VCC_DOCK
Acer Incorporated
21F,88,Sec. 1,Hsin Tai Wu Rd.
Hsichih,Taipei Hsien 221.
Taiwan ,R.O.C.
Title
PORT REPLICATOR
Size A3
Document Number
C-Note 2
Rev -3
Date: Friday, January 11, 2002
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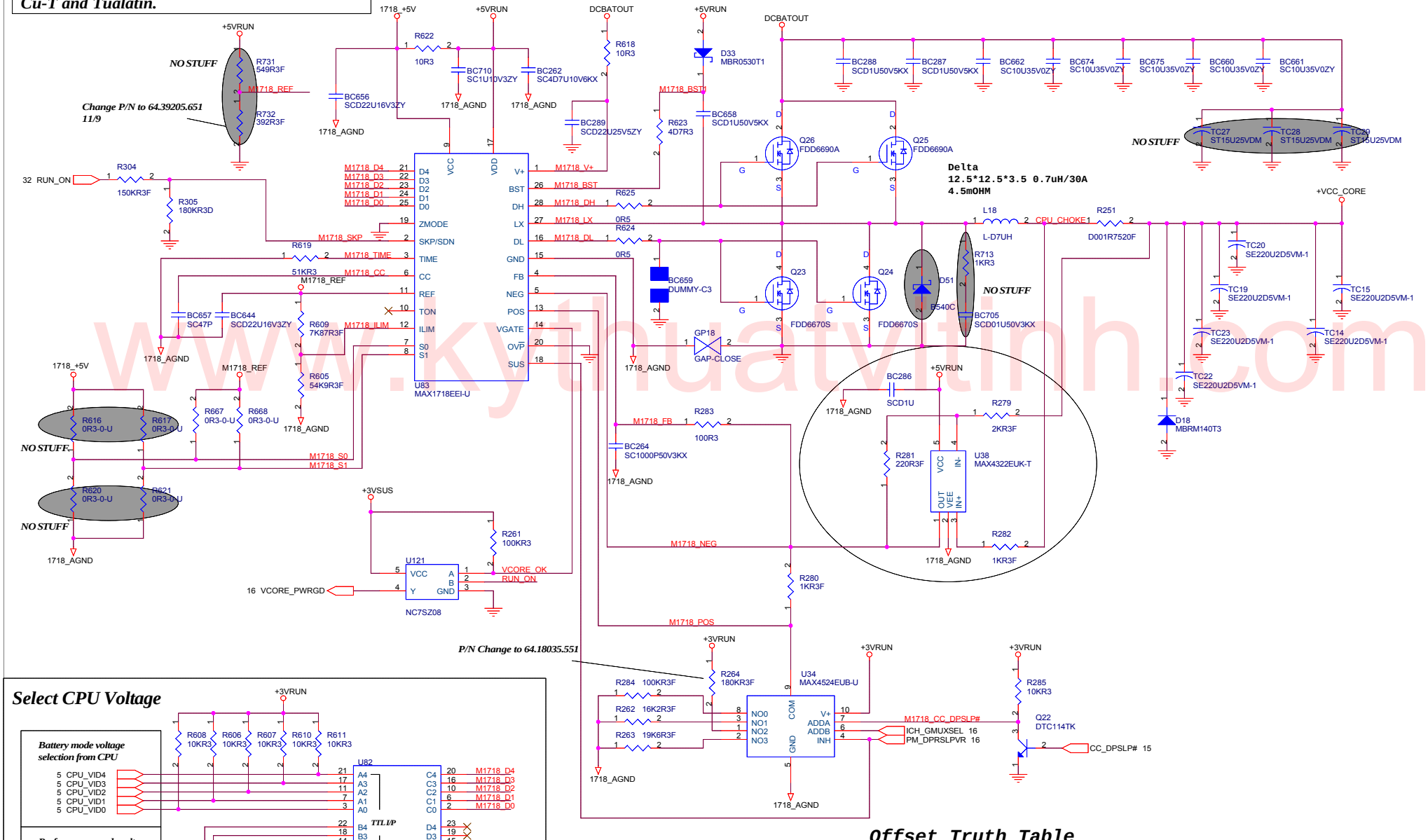
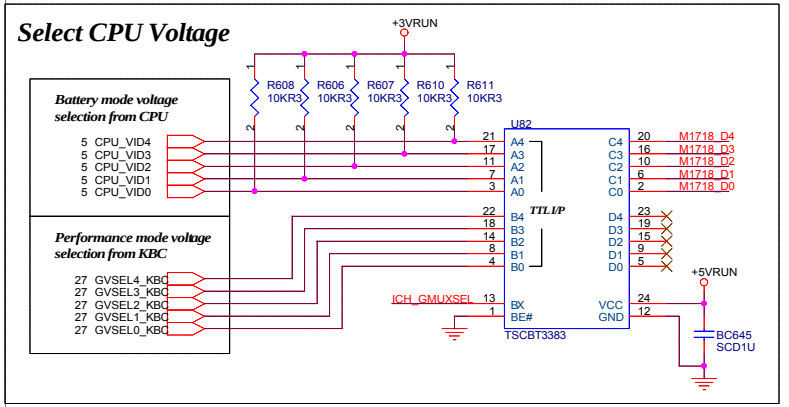
Plz refer to P.2 for the Setting Difference between Cu-T and Tualatin.



Select CPU Voltage



Offset Truth Table

PM_DPRSLPVR	CC_DPSLP#	ICH_GMUXSEL	Voffset
1	X	X	0mV
0	0	0	-59mV
0	0	1	-52mV
0	1	0	-29mV
0	1	1	-3mV

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Title: **CPU VCORE**

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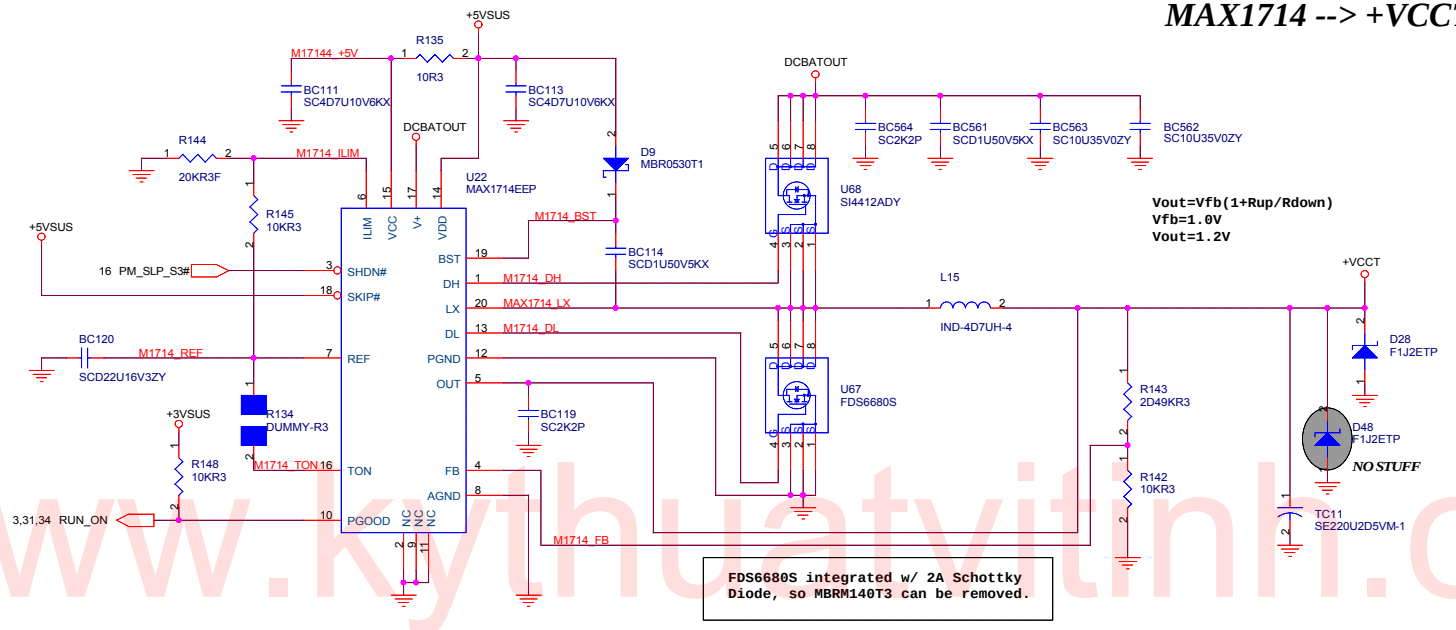
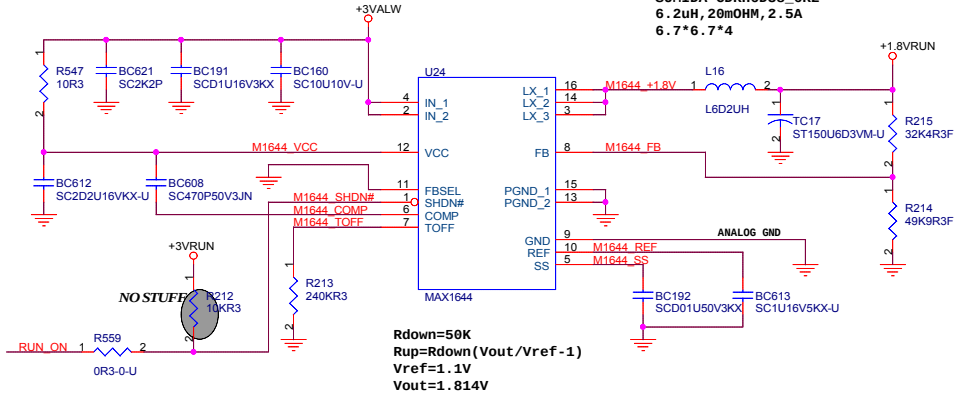
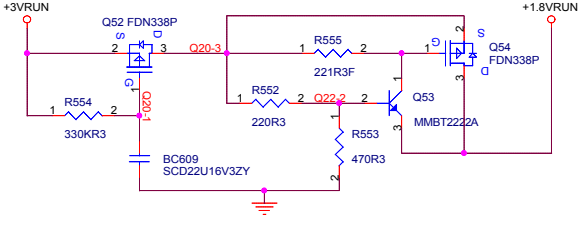
MAX1714 --> +VCCT (CPU_I/O 1.25V)



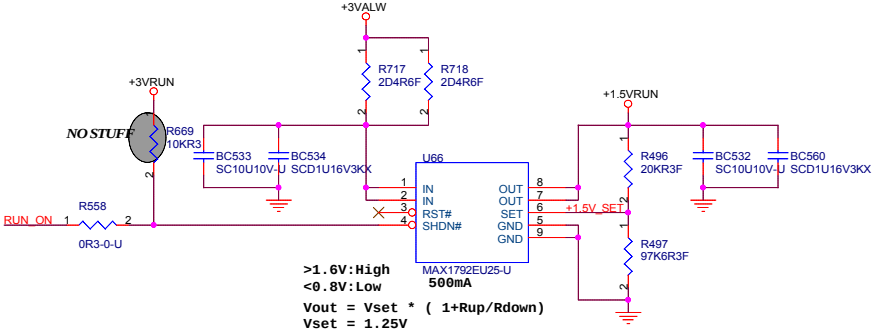
MAX1644 --> 1.8VRUN





To make sure the delta-V between +3VALW & +1.8VALW power plane will not exceed 2V at any time.

MAX1792 --> 1.5VRUN



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Taiwan, R.O.C.

Title: CPUIO 1.25V,1.5V,1.8V

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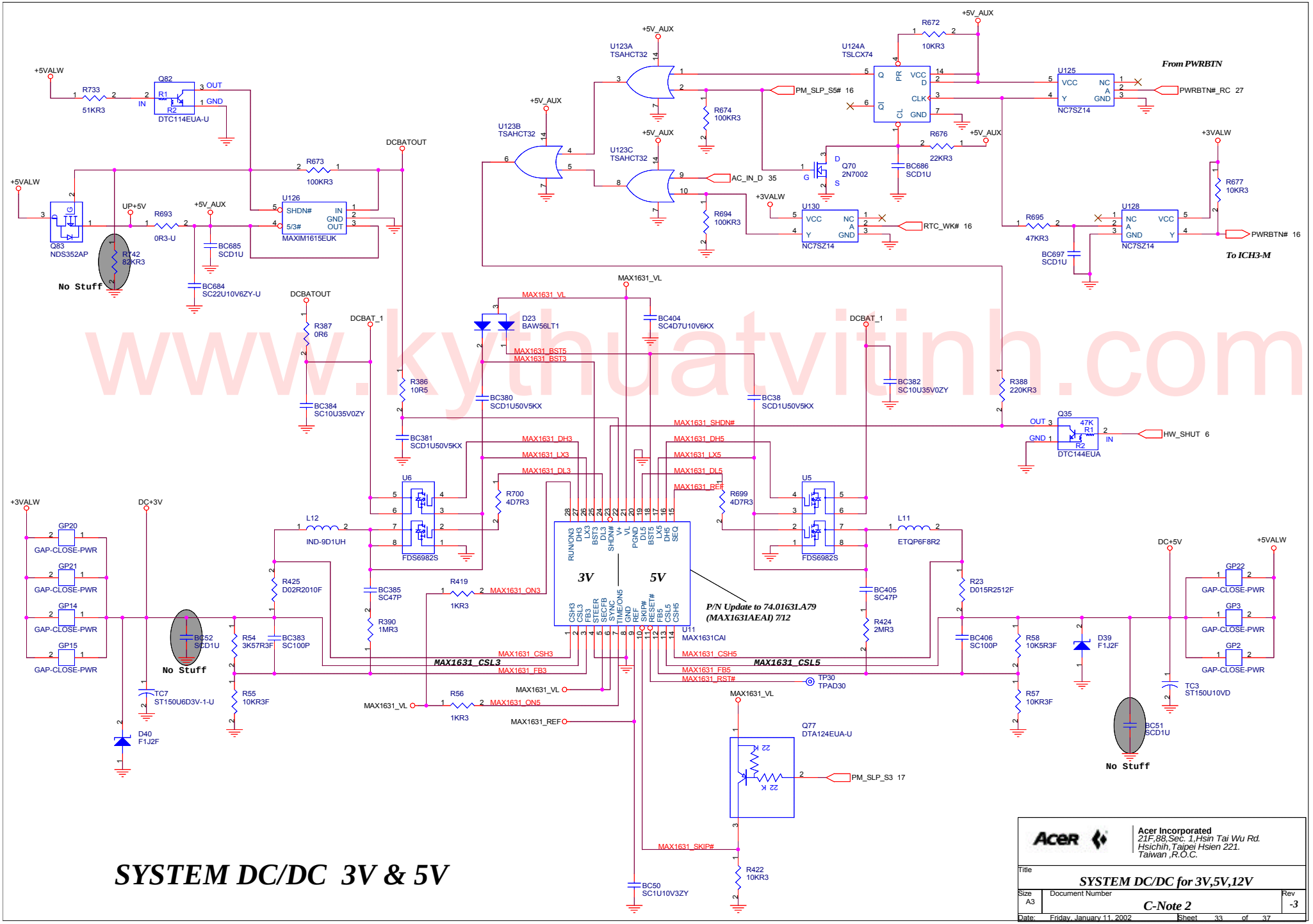

SYSTEM DC/DC 3V & 5V

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Taiwan ,R.O.C.

Title: SYSTEM DC/DC for 3V,5V,12V

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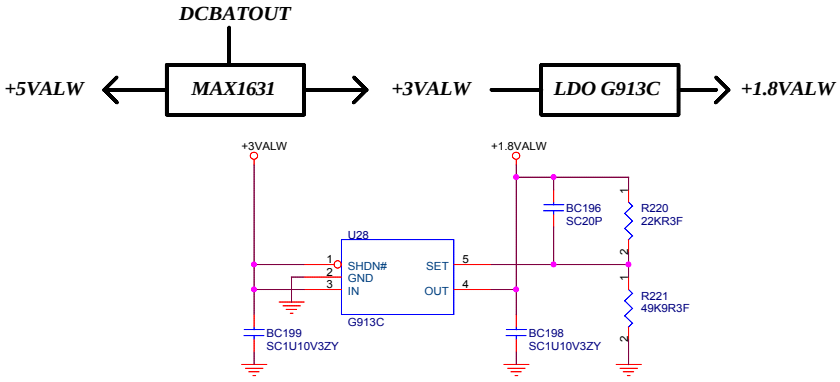
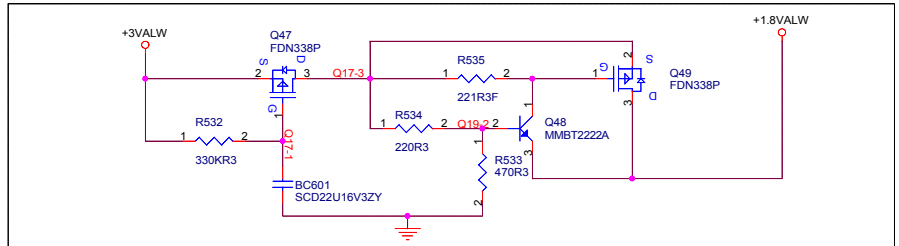
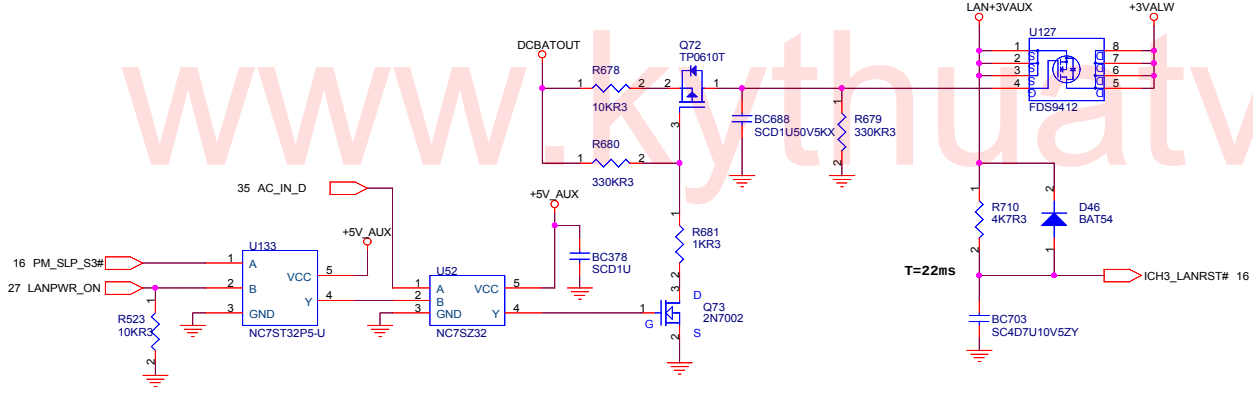
Always Power

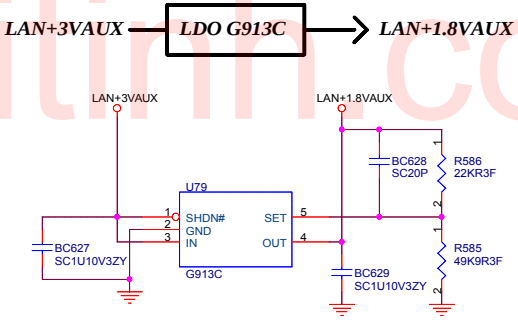




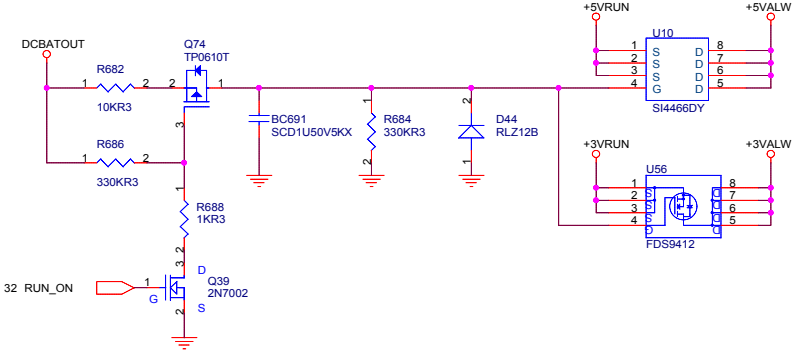
To make sure the delta-V between +3VALW & +1.8VALW power plane will not exceed 2V at any time.

LAN+3VAUX

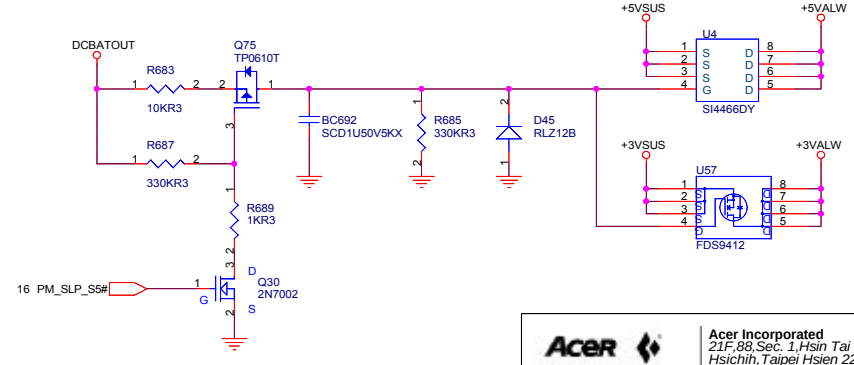




Run Power



Suspend Power



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Title: **PWR PLANE & RESET LOGIC**

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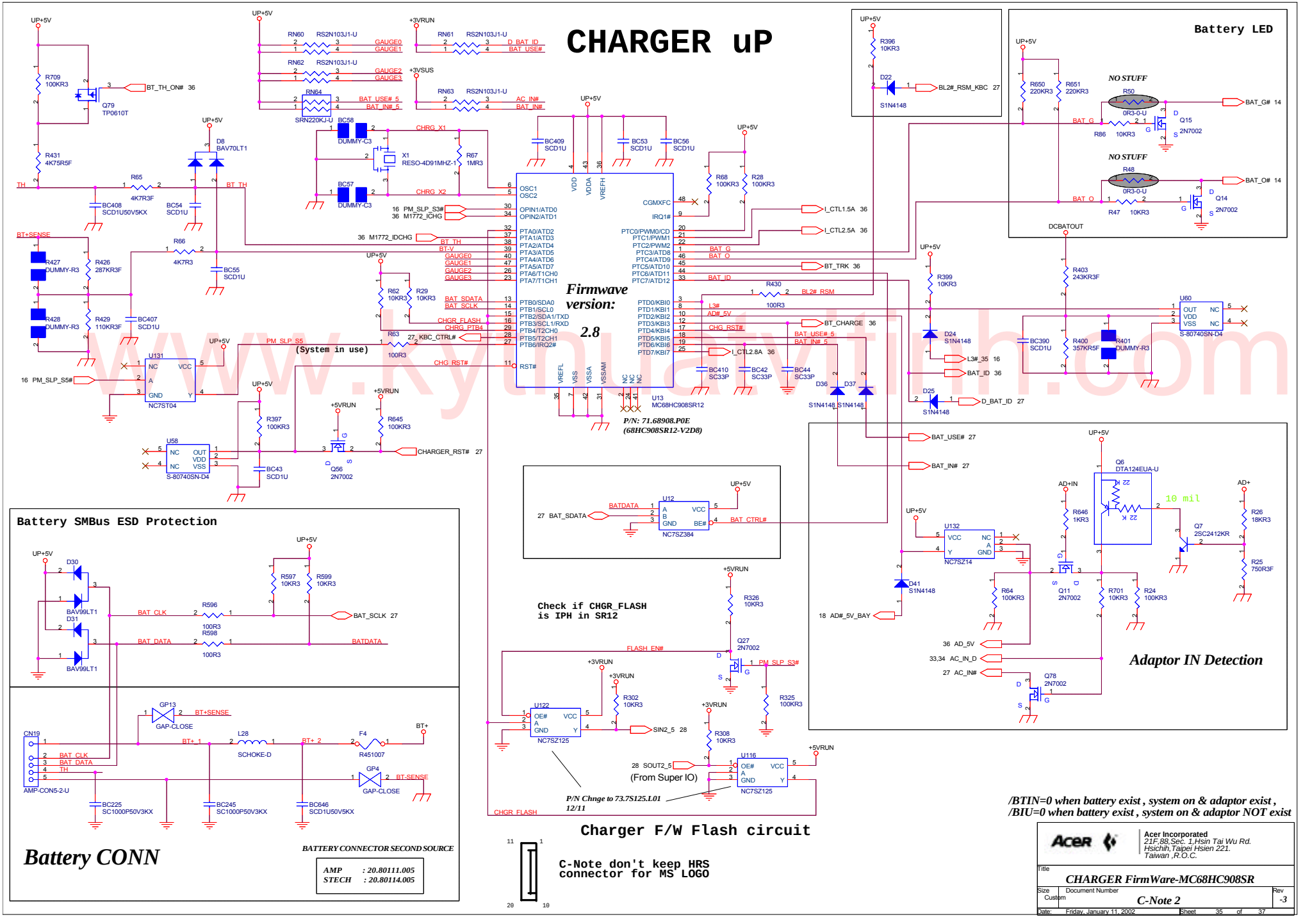
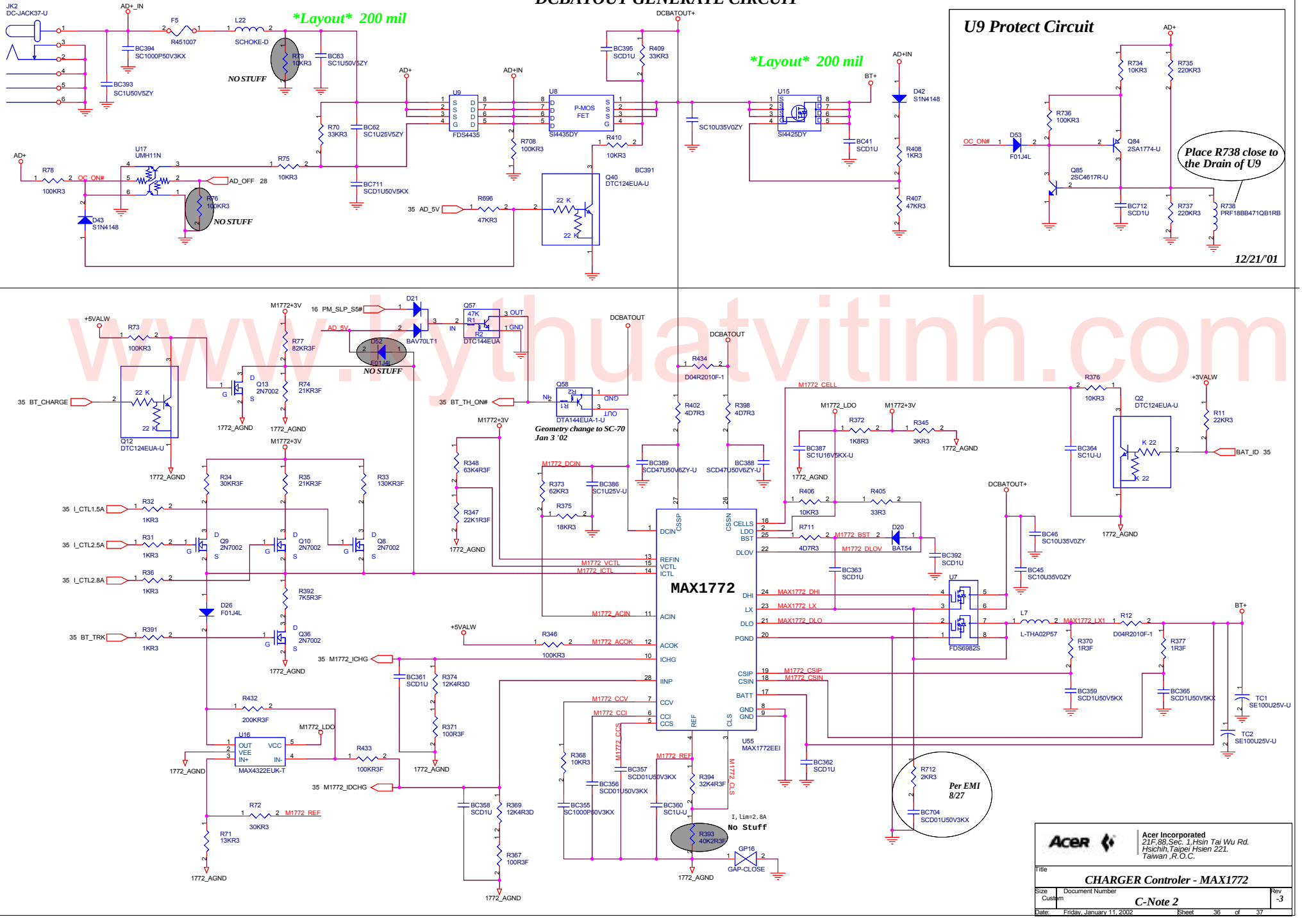
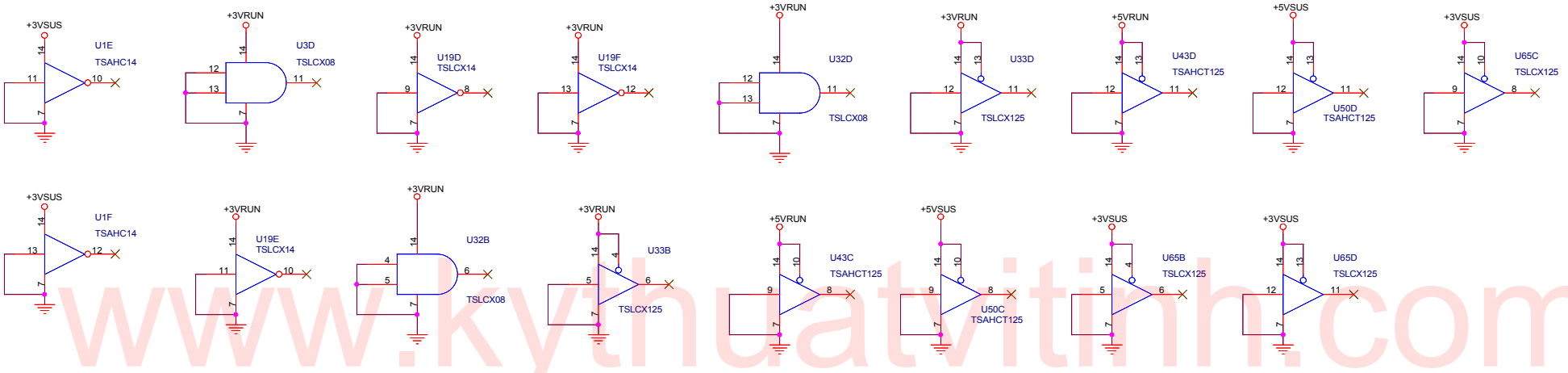
CHARGER uP

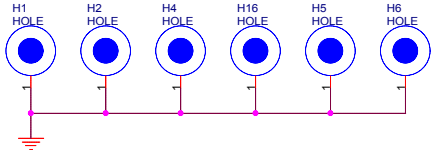


DCBATOUT GENERATE CIRCUIT

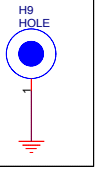


NO USE LOGIC

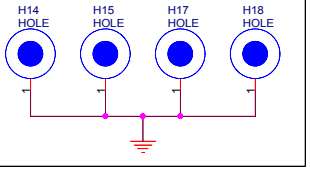




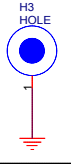
CDC BOSS
34.42G11.001



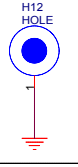
CPU BOSS
34.49G03.001

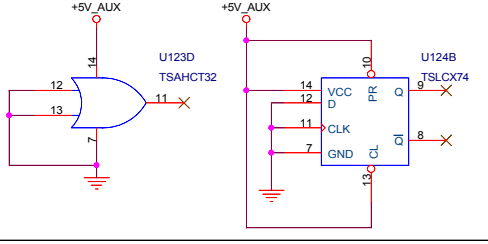


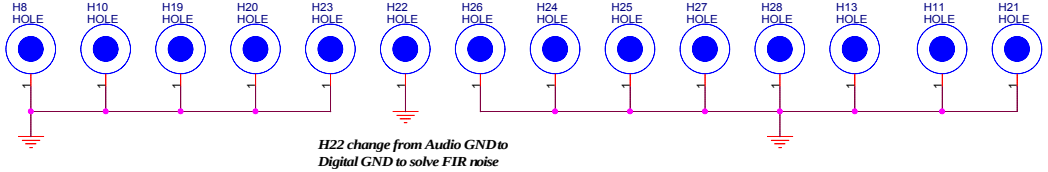
LCD BOSS
34.42G10.001



HEAT SINK
34.47R08.001

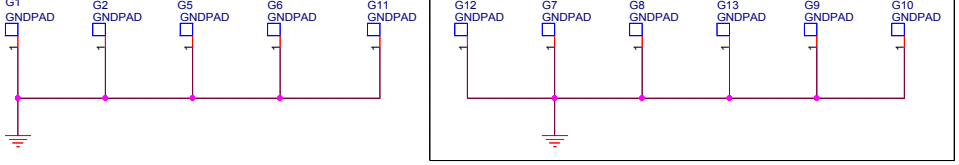




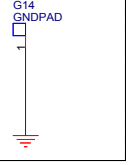


H22 change from Audio GND to Digital GND to solve FIR noise Jan 04 '02

EMI SPRING
34.42P26.001



EMI SPRING (LCD)
34.47R27.001



EMI SPRING (DIMM)
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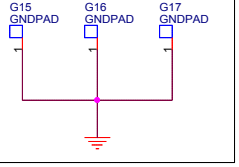

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Title
HOLES, GND PADS & No-use GATES

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