

- 5V / 3.3V / 12V**
Page : 35
- 1.8V / 0.9V**
Page : 36
- 1.5V / 1.05V / 1.8V**
Page : 37
- CPU CORE**
Page : 34
- +1.2V**
Page : 38
- BATTERY CHARGER**
Page : 39
- BATTERY SELECT**
Page : 40

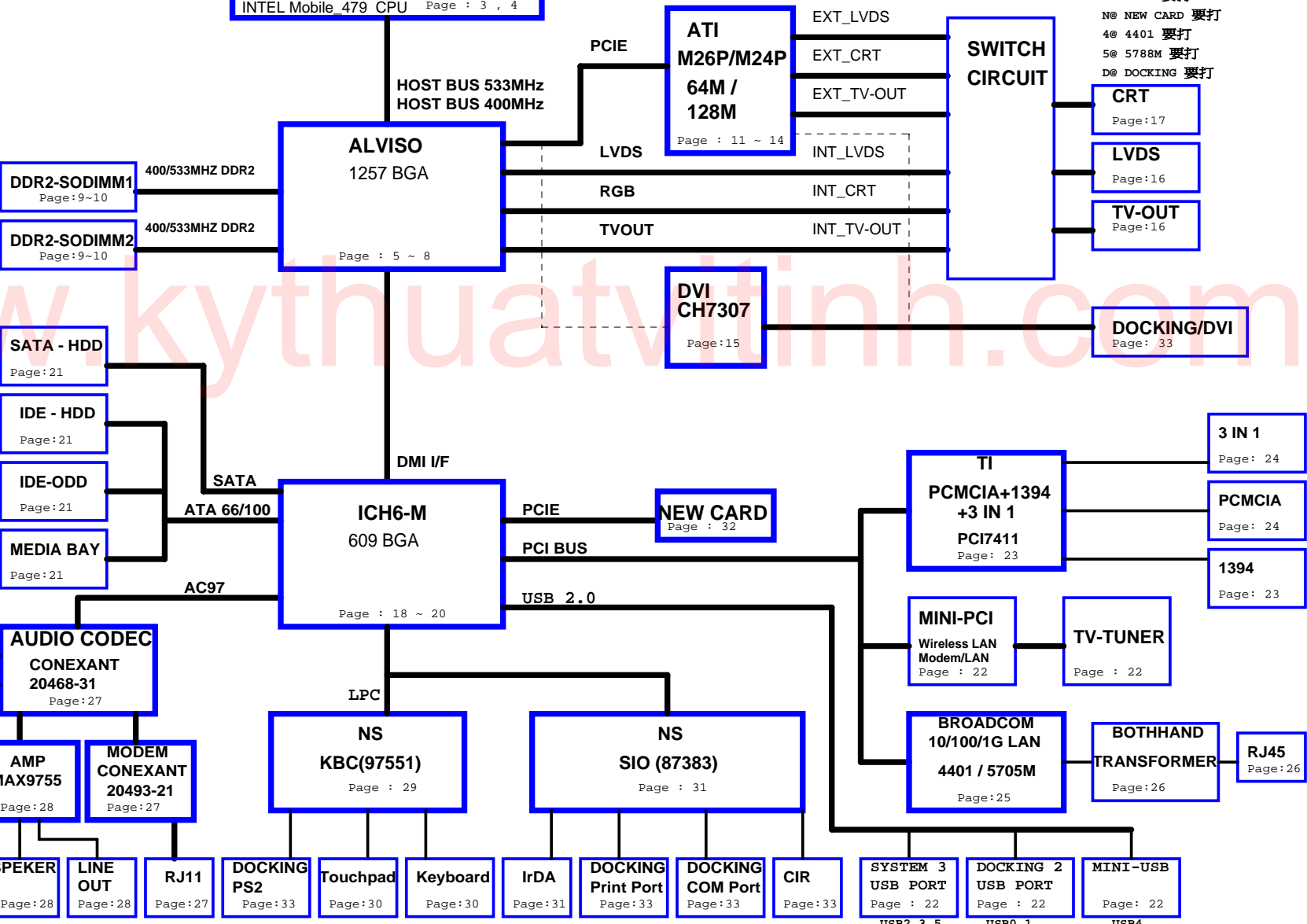
- 5VPCU
- 3V_ALWAYS
- +12V
- +5V
- 3V_S5
- 3VSUS
- 5VSUS
- 2.5VSUS
- +2.5V
- +1.8V
- MVREF_DM
- SMDDR_VTERM
- 1.5V_S5
- +1.5V
- AGP_VCC (+1.5V)
- 1.2VCCT
- VTT
- VCC_CORE
- VGA_CORE
- 2.5V_VGA

CLOCK GEN ICS
ICS954217
Page : 2

Centrino
DO THAN
CELEROM-M
INTEL Mobile 479 CPU Page : 3 , 4

CRANE3 (ZL7)

- ED@ INT. VGA WITH DOCK
- ID@ INT. VGA WITH DOCK
- ND@ W/O DOCKING 要打
- BOM MARK
- E@ EXT VGA 要打
- I@ INTVGA 要打
- SA@ SATA 要打
- F@ FIXED ODD 要打
- SW@ SWAPPABLE ODD 要打
- 3@ 3in1 要打
- N@ NEW CARD 要打
- 4@ 4401 要打
- 5@ 5788M 要打
- D@ DOCKING 要打



PCI ROUTING TABLE IDSEL INTERRUPT DEVICE USB2,3,5 USB0,1 USB4

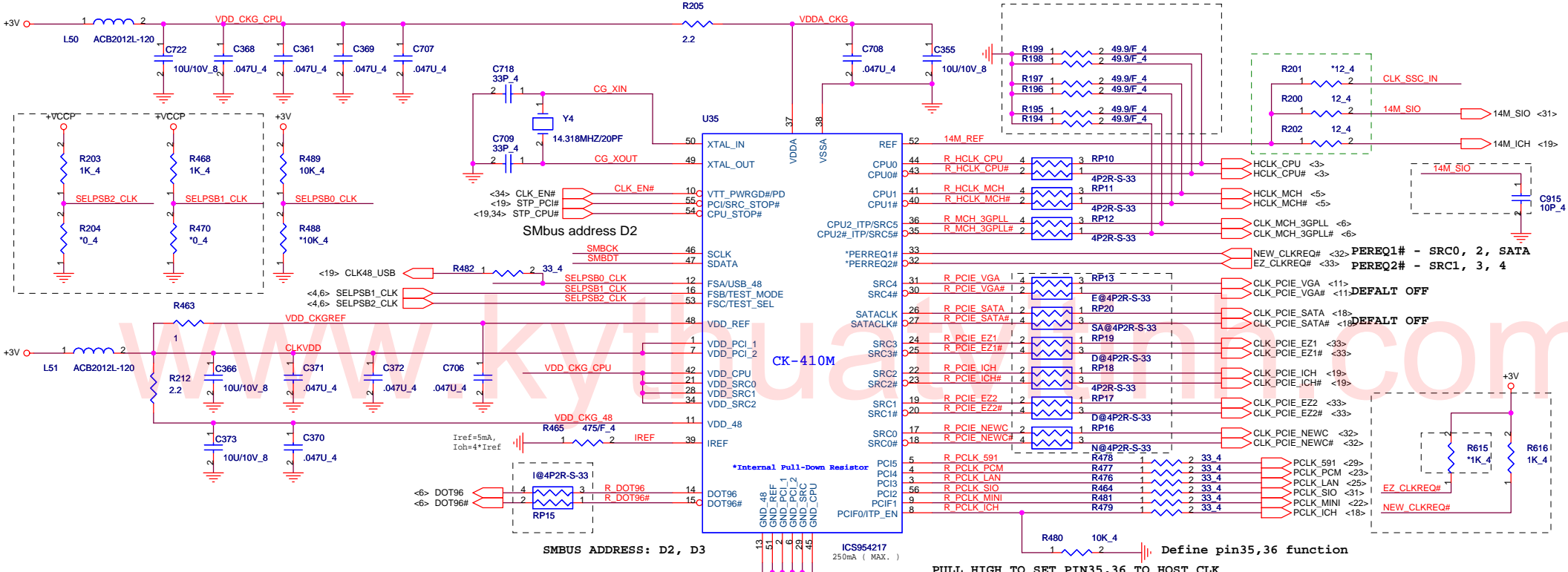
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REQ2# / GNT2#	AD19	INTB# , INTD#	MINI-PCI
REQ1# / GNT1#	AD17	INTC# , INTD# , INTA#	TI 7411
REQ3# / GNT3#	AD18	INTB# , INTD#	MINI-PCI (TV Tuner)

REV.C

PROJECT : ZL7
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	C
Date:	Thursday, June 23, 2005	Sheet 1 of 40

Place these termination to close CK410M.



Smbus address D2

SMBUS ADDRESS: D2, D3

SMBUS ADDRESS: D4, D5

	FSC	FSB	FSA	CPU	SRC	PCI
DOETHAN-A 400	1	0	1	100	100	33
DOETHAN-A 533	0	0	1	133	100	33
	0	1	1	166	100	33
	0	1	0	200	100	33
	0	0	0	266	100	33
	1	0	0	333	100	33
	1	1	0	400	100	33
	1	1	1	RSVD	100	33

Place these termination to close CK410M.

QUANTA COMPUTER

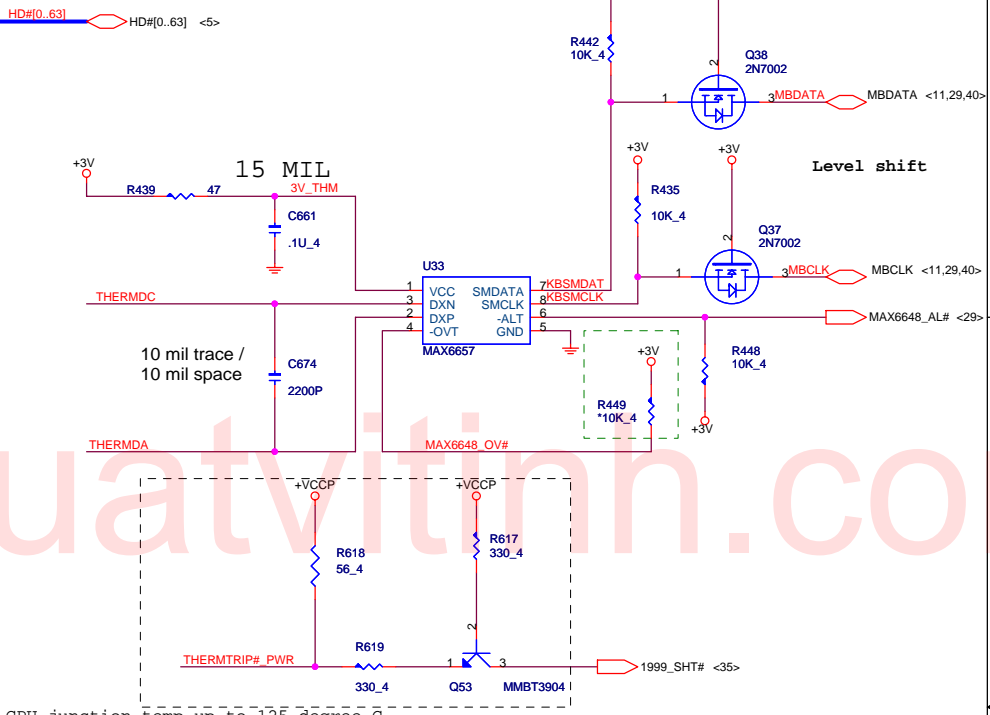
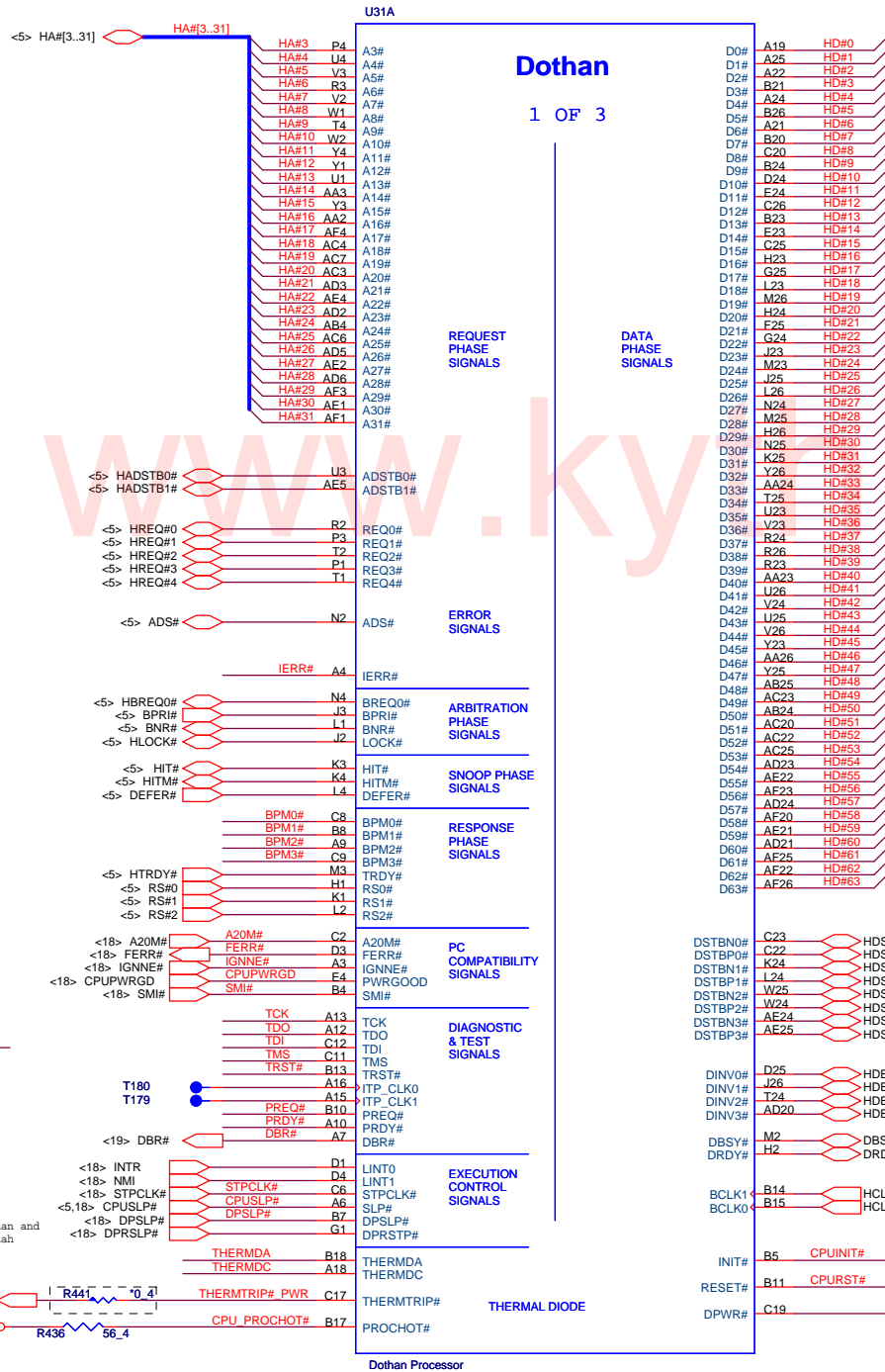
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Size: Document Number ZL7

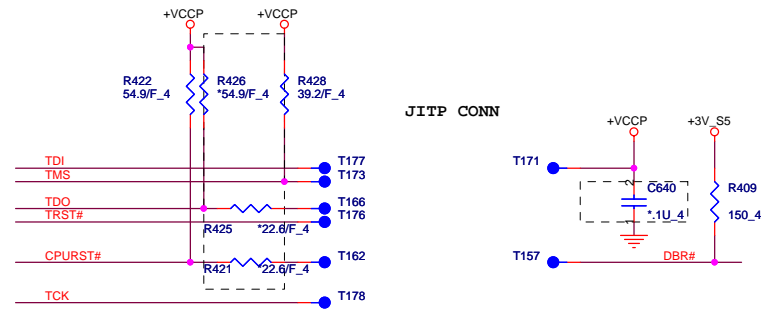
Date: Thursday, June 23, 2005

Sheet 2 of 40

Rev C



CPU junction temp up to 125 degree C
output signal. shut down system
DEPOP R425, R426, R421, C640 WHEN NO JITP

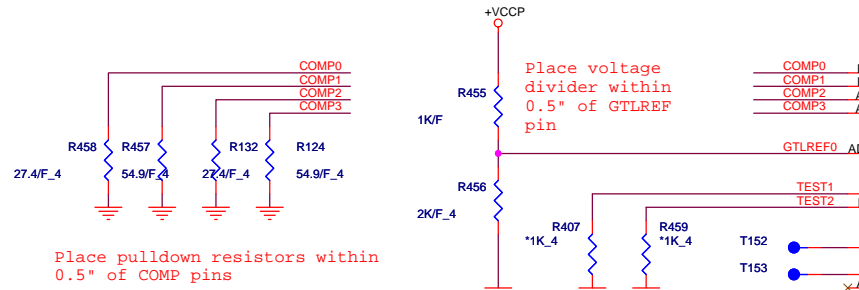


QUANTA COMPUTER

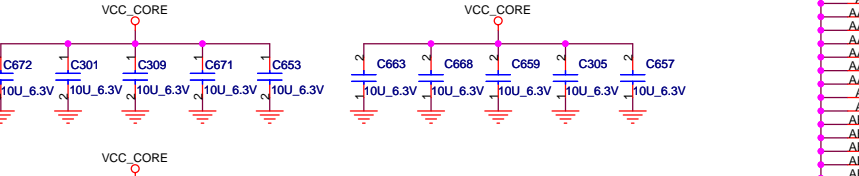
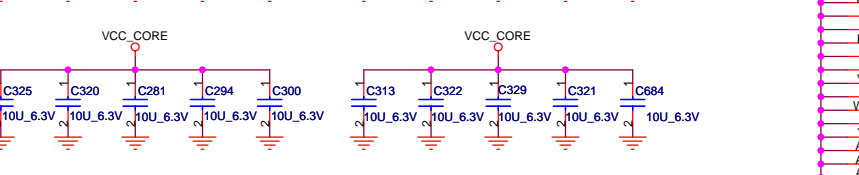
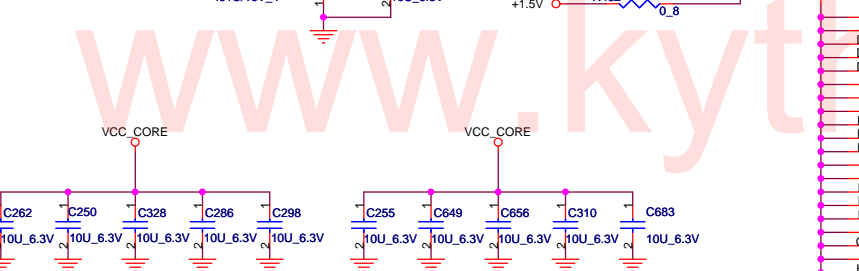
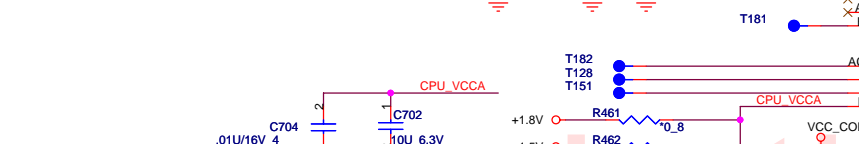
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Size: Document Number ZL7

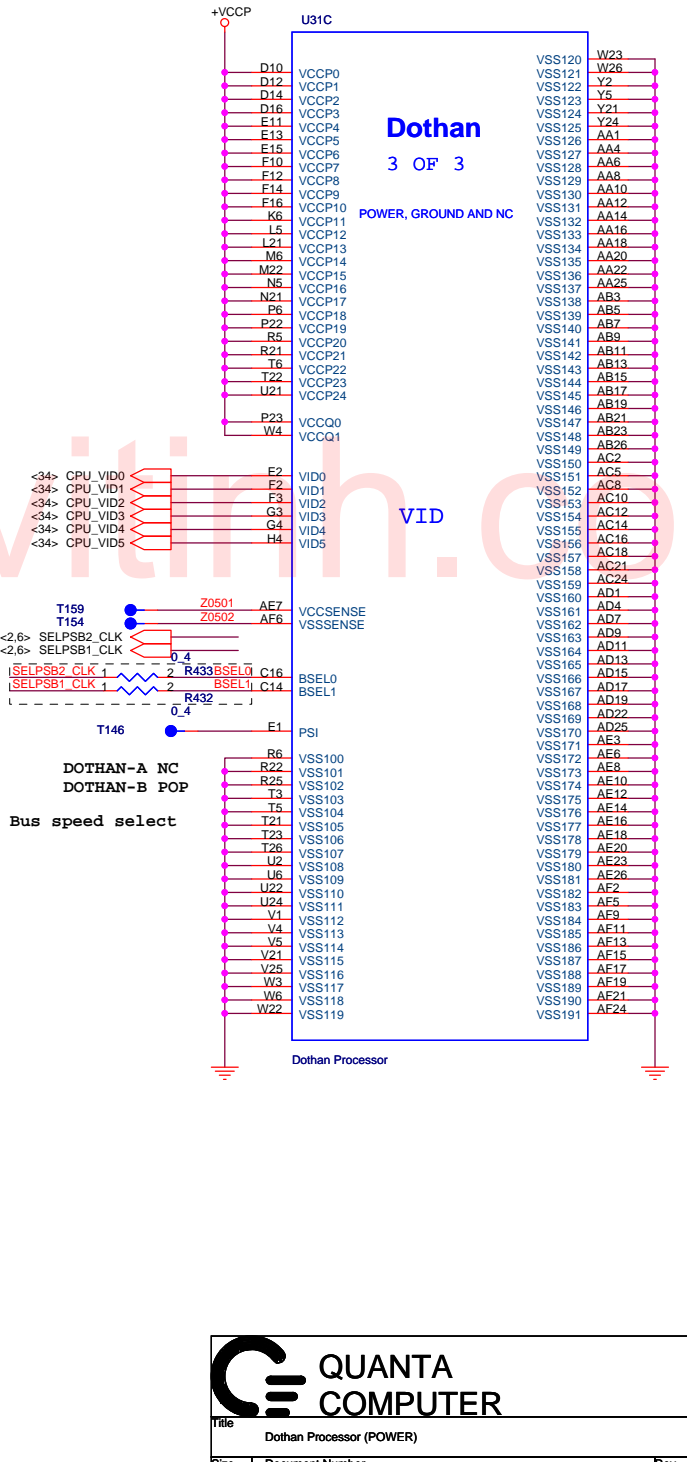
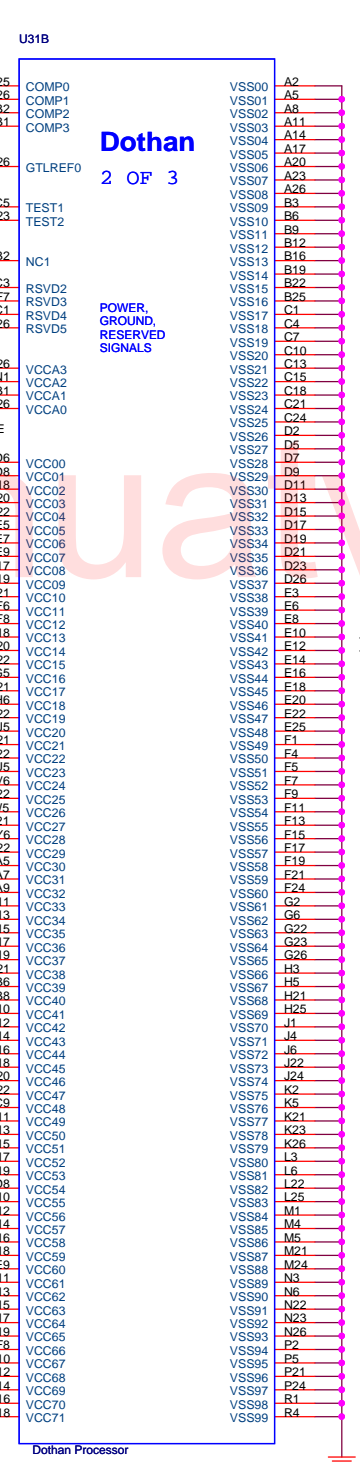
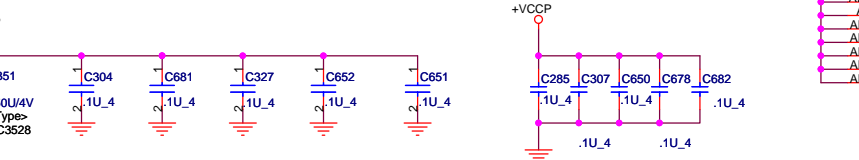
Date: Thursday, June 23, 2005 Sheet 3 of 40 Rev C



Place pull-down resistors within 0.5" of COMP pins



Total caps = 2633 uF
ESR = 15m ohm/5 // 5m ohm/25 // 5m ohm/15

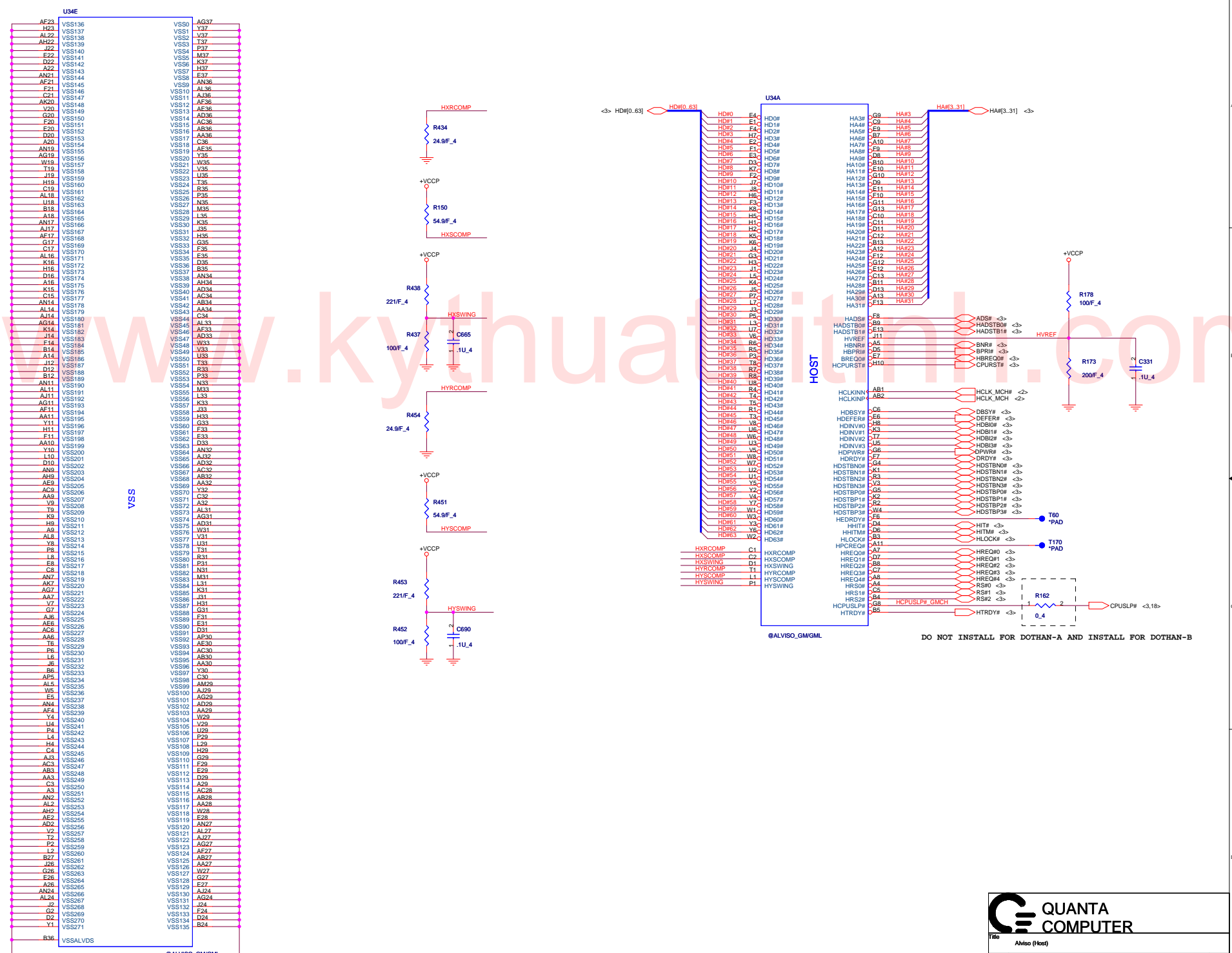


QUANTA COMPUTER

Title: Dothan Processor (POWER)

Size: Document Number ZL7

Date: Thursday, June 23, 2005 Sheet 4 of 40 Rev C

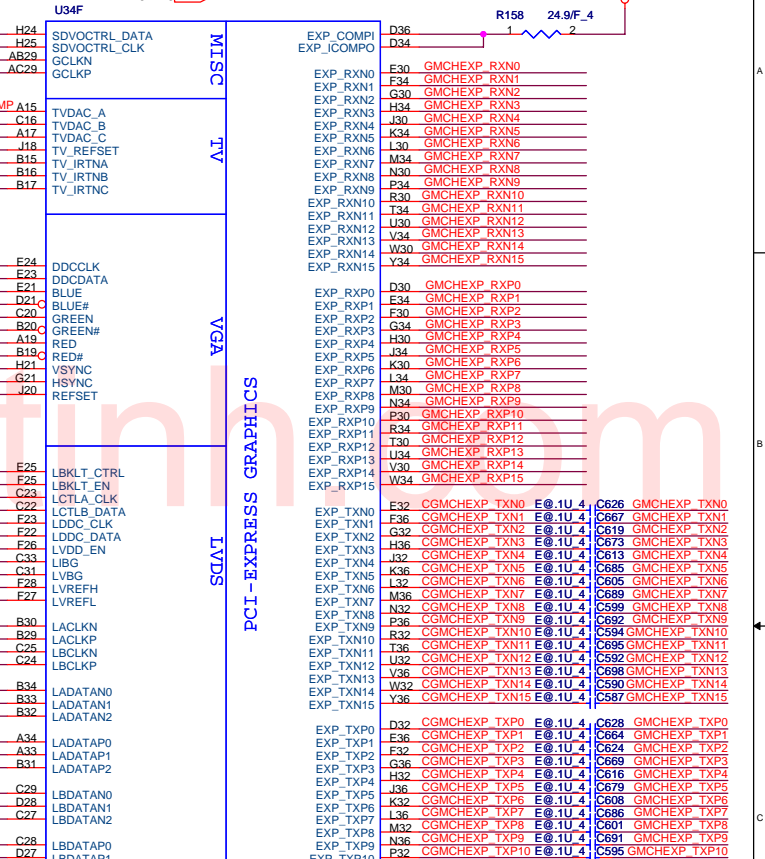
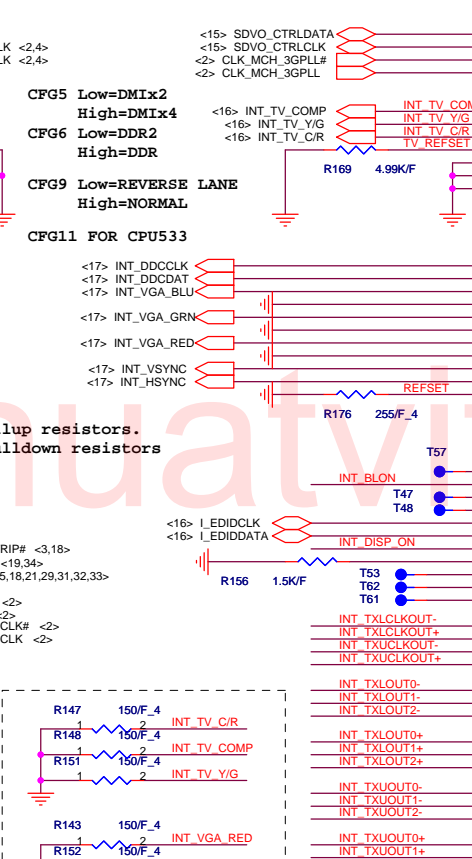
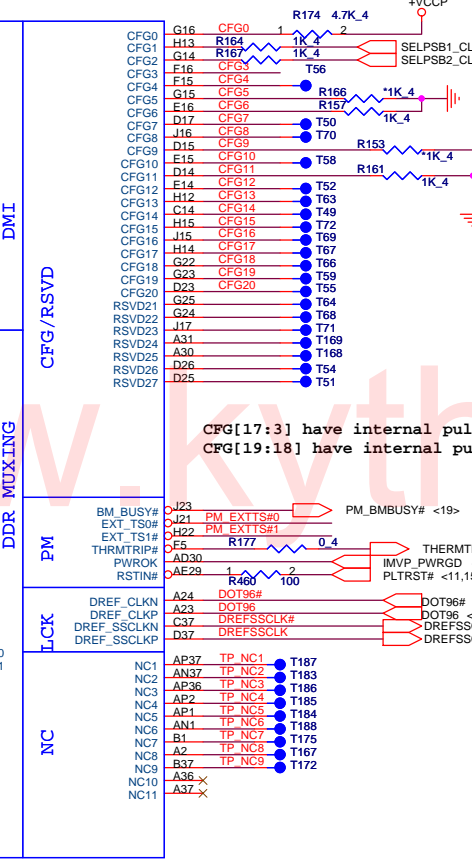
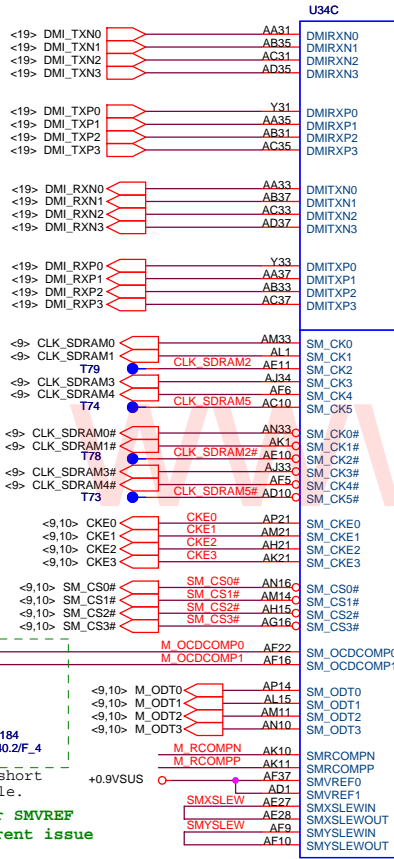


DO NOT INSTALL FOR DOTAN-A AND INSTALL FOR DOTAN-B

QUANTA COMPUTER

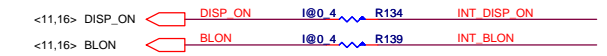
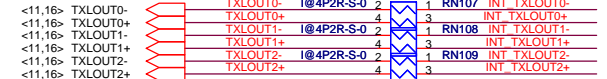
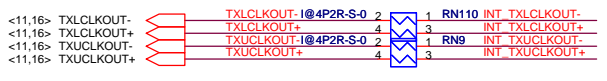
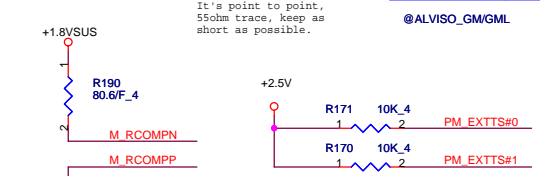
Title: Alviso (Host)
 Size: C, Document Number: ZL7, Rev: C
 Date: Thursday, June 23, 2005, Sheet: 5 of 40

CFG[0:2]=100 FOR FSB 533
CFG[0:2]=101 FOR FSB 400

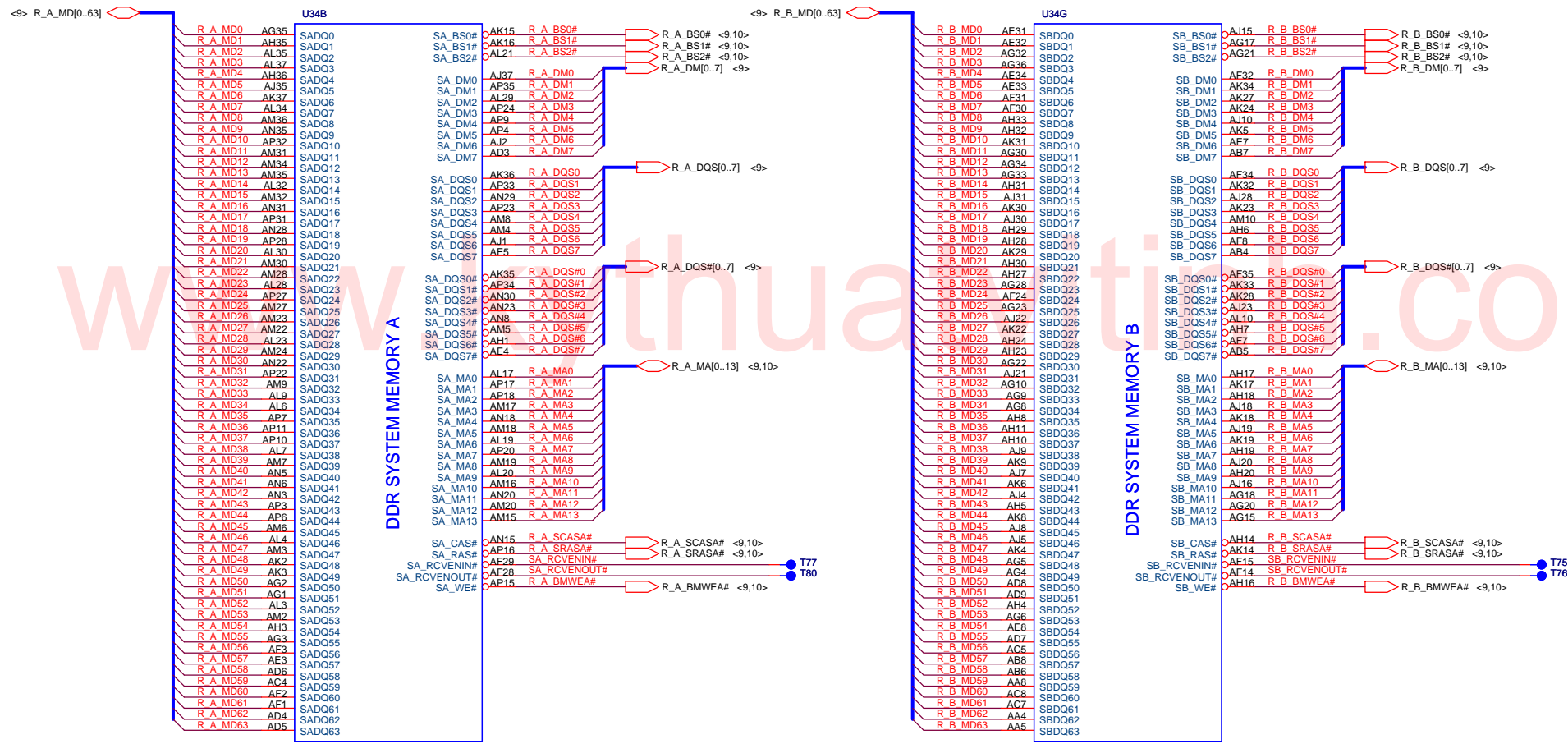


CFG[17:3] have internal pullup resistors.
CFG[19:18] have internal pulldown resistors

Depop for SMVREF over current issue

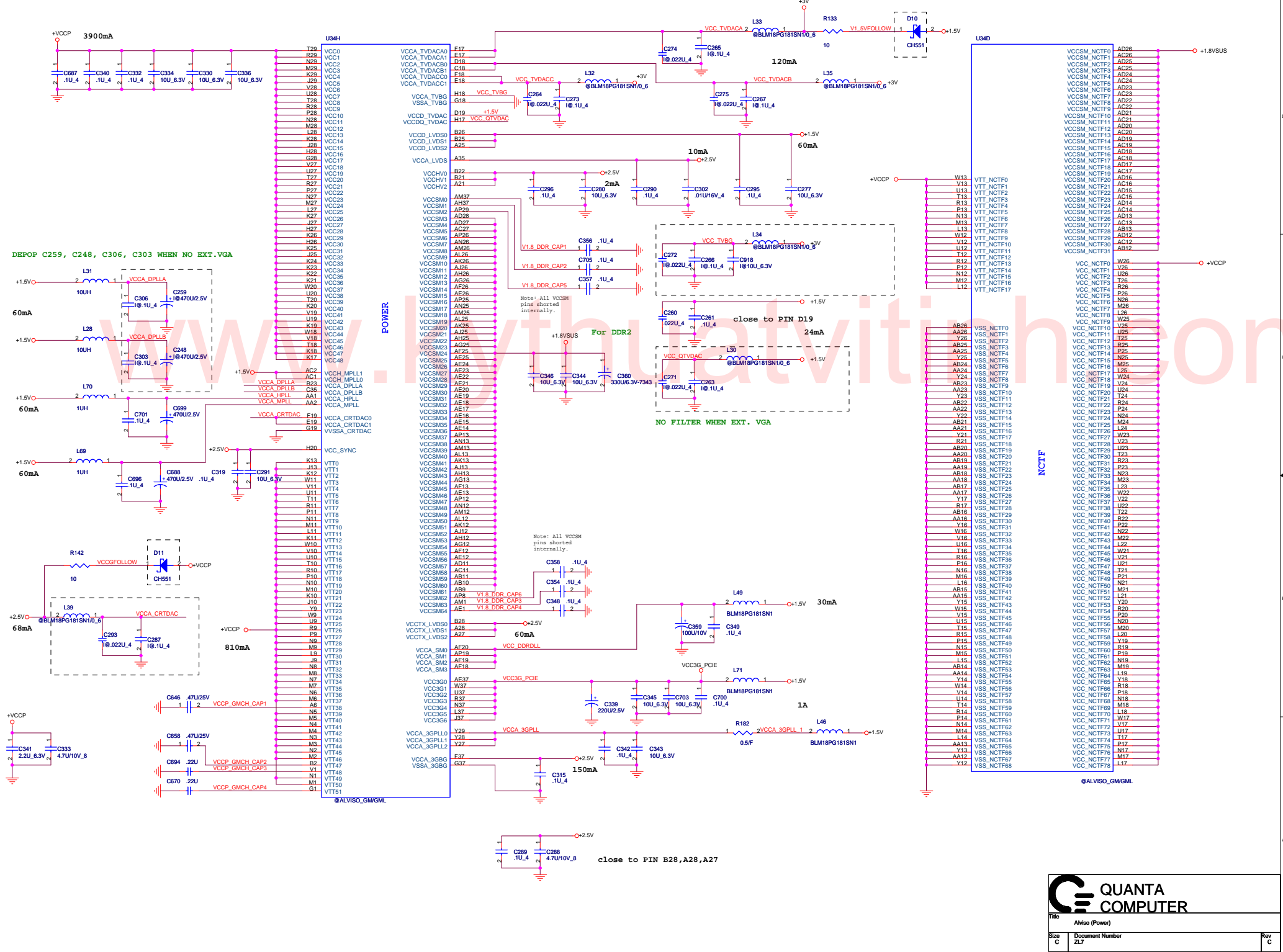


Aviso (VGA,DMI)
Title
Sustaining Document Number ZL7
Date: Thursday, June 23, 2005
Sheet 6 of 40
Rev C



@ALVISO_GM/GML

@ALVISO_GM/GML

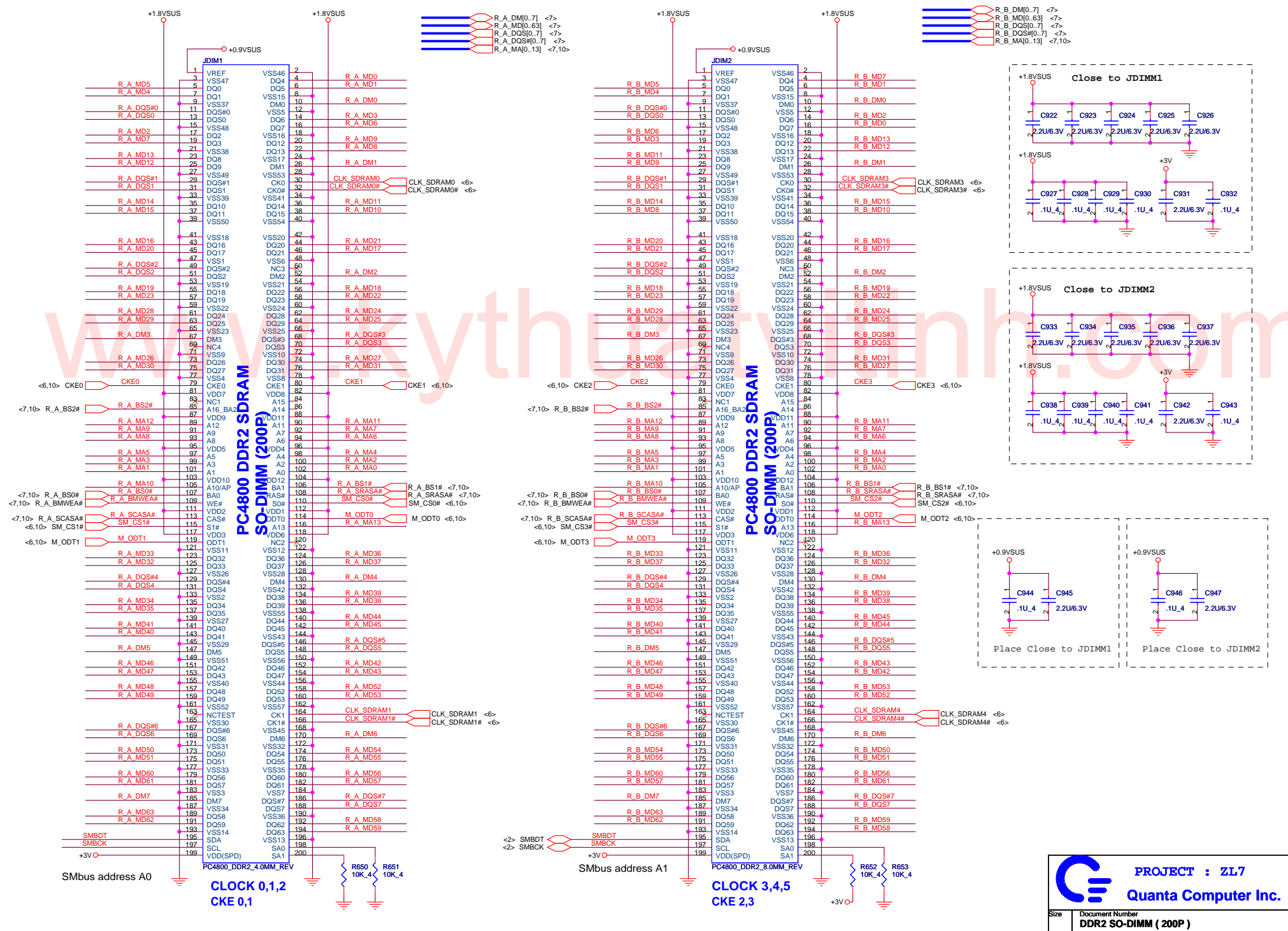


QUANTA COMPUTER

File: Alvico (Power)

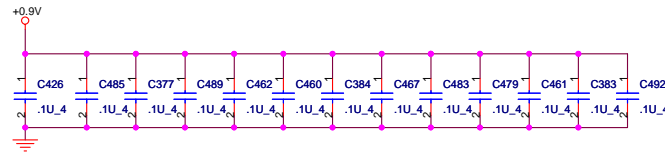
Size	Document Number	Rev
C	ZL7	C

Date: Thursday, June 23, 2005 Sheet 8 of 40

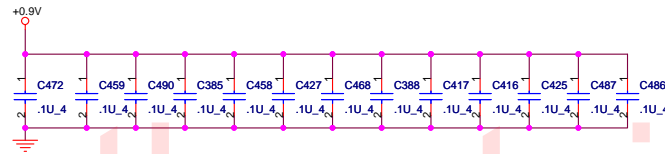


PROJECT : ZL7
Quanta Computer Inc.

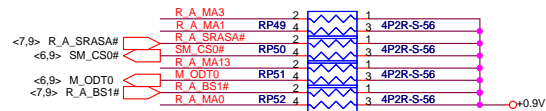
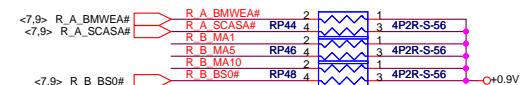
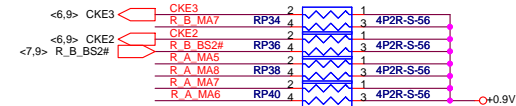
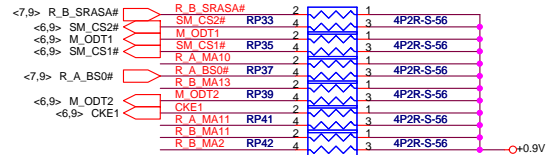
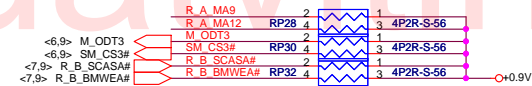
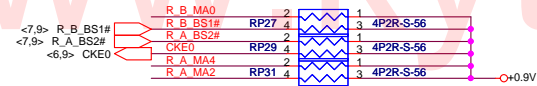
Size	Document Number	Rev
	DDR2 SO-DIMM (200P)	C
Date:	Thursday, June 23, 2005	Sheet 9 of 40



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V

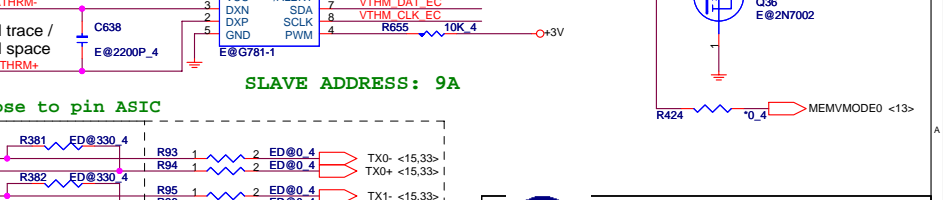
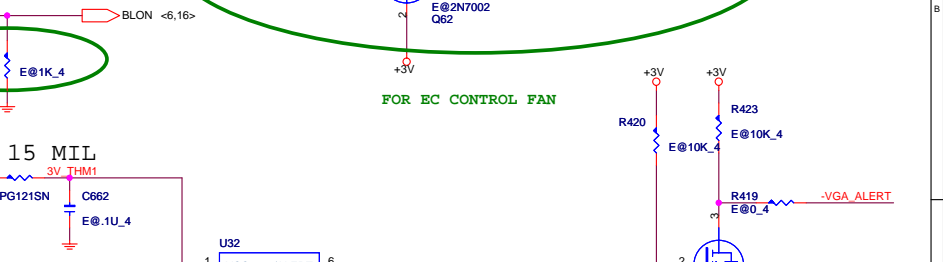
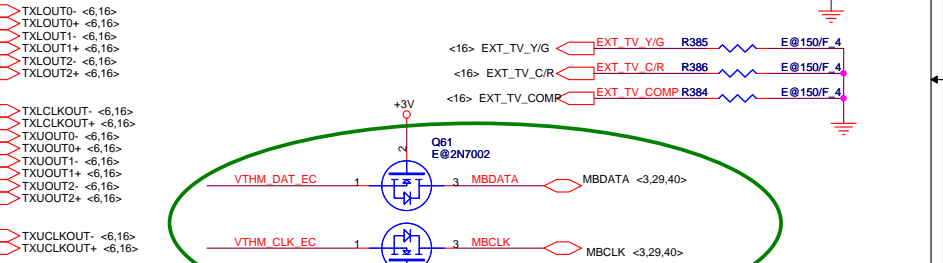
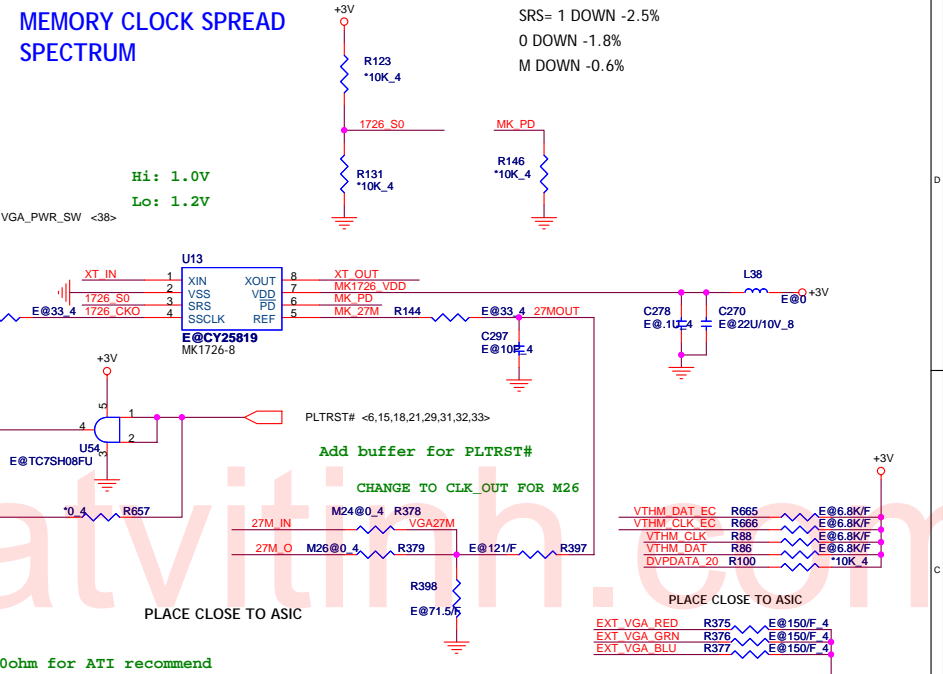
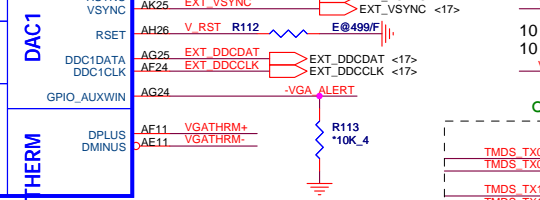
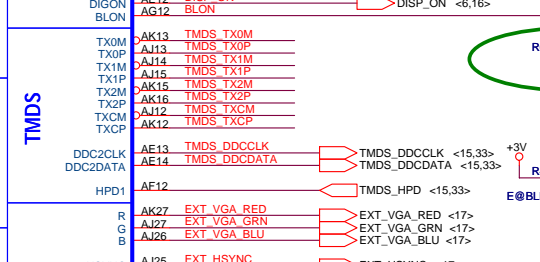
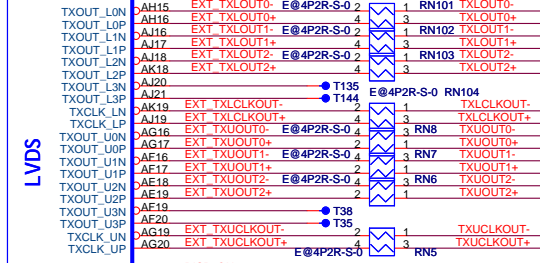
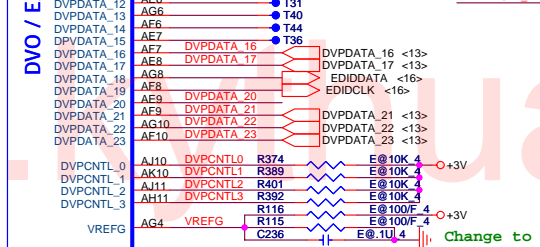
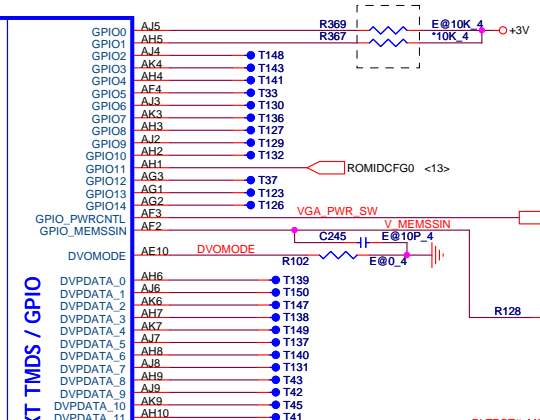
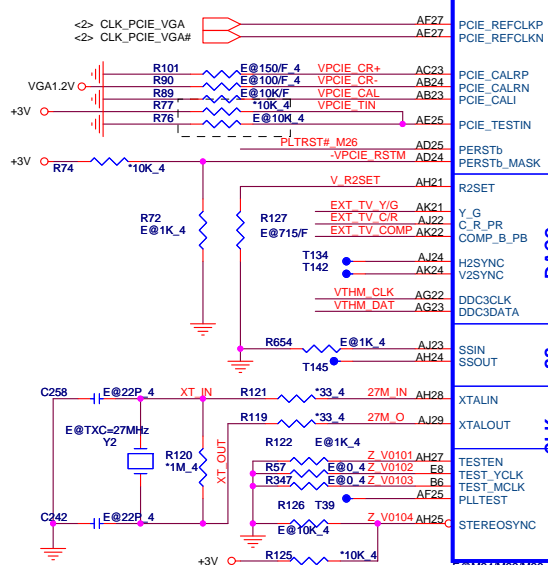


Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V



<6>	GMCEXP_TXP0[0..15]	GMCEXP_TXP0 AH30	PCIE_RX0P
<6>	GMCEXP_TXN0[0..15]	GMCEXP_TXN0 AG30	PCIE_RX0N
<6>	GMCEXP_TXP1[0..15]	GMCEXP_TXP1 AF29	PCIE_RX1P
<6>	GMCEXP_TXN1[0..15]	GMCEXP_TXN1 AE29	PCIE_RX1N
<6,15>	GMCEXP_RXP0[0..15]	GMCEXP_RXP2 AE29	PCIE_RX2P
<6,15>	GMCEXP_RXN0[0..15]	GMCEXP_RXN2 AE30	PCIE_RX2N
		GMCEXP_TXP3 AD30	PCIE_RX3P
		GMCEXP_TXN3 AD29	PCIE_RX3N
		GMCEXP_TXP4 AD29	PCIE_RX4P
		GMCEXP_TXN4 AB29	PCIE_RX4N
		GMCEXP_TXP5 AB30	PCIE_RX5P
		GMCEXP_TXN5 AA30	PCIE_RX5N
		GMCEXP_TXP6 AA29	PCIE_RX6P
		GMCEXP_TXN6 Y29	PCIE_RX6N
		GMCEXP_TXP7 W29	PCIE_RX6N
		GMCEXP_TXN7 W30	PCIE_RX7N
		GMCEXP_TXP8 V30	PCIE_RX8P
		GMCEXP_TXN8 V29	PCIE_RX8N
		GMCEXP_TXP9 U29	PCIE_RX9P
		GMCEXP_TXN9 T29	PCIE_RX9N
		GMCEXP_TXP10 T30	PCIE_RX10P
		GMCEXP_TXN10 R30	PCIE_RX10N
		GMCEXP_TXP11 P29	PCIE_RX11P
		GMCEXP_TXN11 N29	PCIE_RX11N
		GMCEXP_TXP12 N30	PCIE_RX12P
		GMCEXP_TXN12 M30	PCIE_RX12N
		GMCEXP_TXP13 M29	PCIE_RX13P
		GMCEXP_TXN13 L29	PCIE_RX13N
		GMCEXP_TXP14 L29	PCIE_RX14P
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		GMCEXP_TXP15 K30	PCIE_RX15P
		GMCEXP_TXN15 J30	PCIE_RX15N

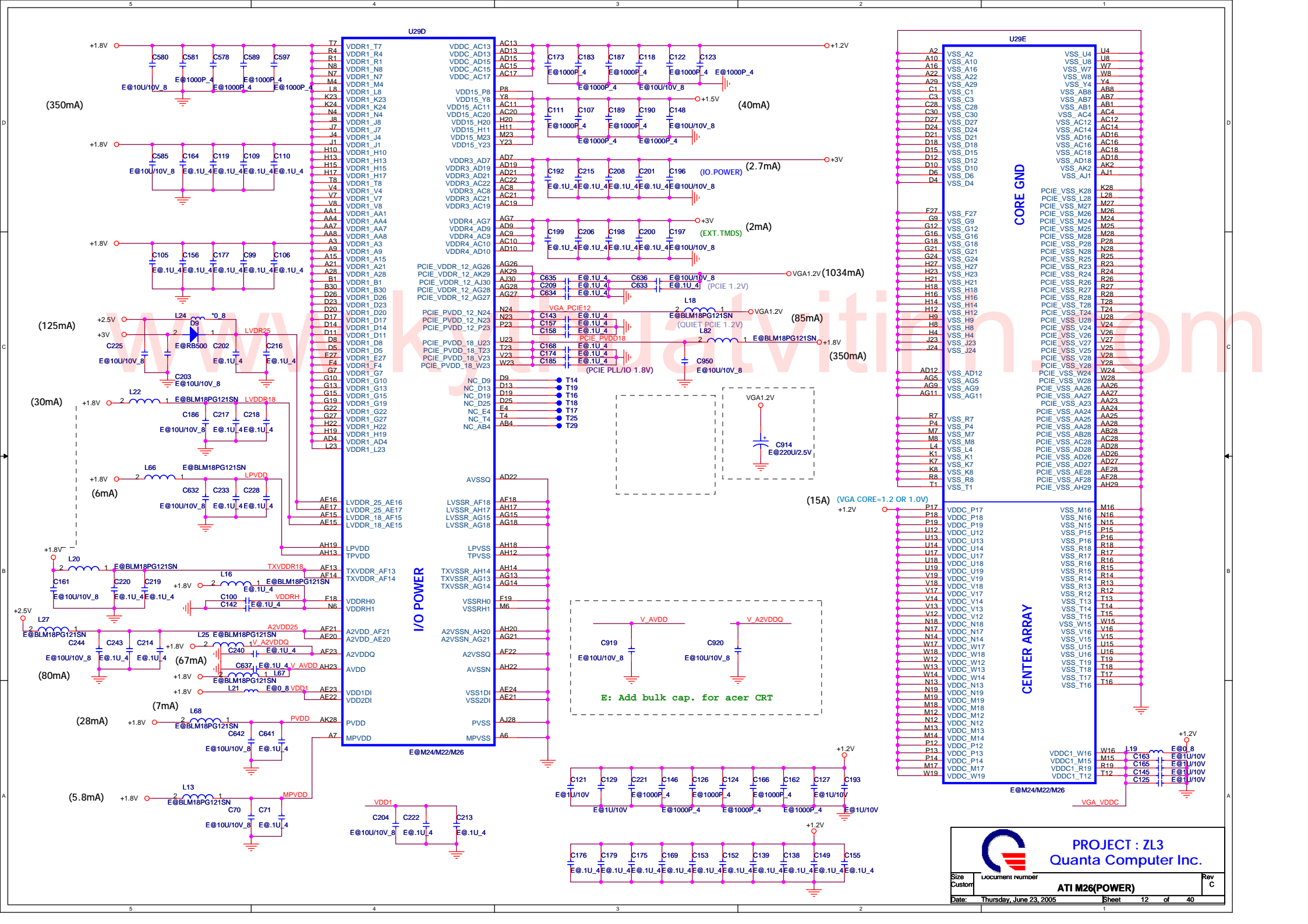
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GMCEXP_RXP1	C227	E@1U 4 V GMCEXP_RXP1	AE25	PCIE_TX1P
GMCEXP_RXN1	C224	E@1U 4 V GMCEXP_RXN1	AB25	PCIE_TX1N
GMCEXP_RXP2	C211	E@1U 4 V GMCEXP_RXP2	AC27	PCIE_TX2P
GMCEXP_RXN2	C205	E@1U 4 V GMCEXP_RXN2	AB27	PCIE_TX2N
GMCEXP_RXP3	C212	E@1U 4 V GMCEXP_RXP3	AC26	PCIE_TX3P
GMCEXP_RXN3	C207	E@1U 4 V GMCEXP_RXN3	AB26	PCIE_TX3N
GMCEXP_RXP4	C194	E@1U 4 V GMCEXP_RXP4	Y25	PCIE_TX4P
GMCEXP_RXN4	C188	E@1U 4 V GMCEXP_RXN4	W25	PCIE_TX4N
GMCEXP_RXP5	C195	E@1U 4 V GMCEXP_RXP5	Y27	PCIE_TX5P
GMCEXP_RXN5	C191	E@1U 4 V GMCEXP_RXN5	W27	PCIE_TX5N
GMCEXP_RXP6	C178	E@1U 4 V GMCEXP_RXP6	Y26	PCIE_TX6P
GMCEXP_RXN6	C171	E@1U 4 V GMCEXP_RXN6	W26	PCIE_TX6N
GMCEXP_RXP7	C160	E@1U 4 V GMCEXP_RXP7	U25	PCIE_TX7P
GMCEXP_RXN7	C154	E@1U 4 V GMCEXP_RXN7	T25	PCIE_TX7N
GMCEXP_RXP8	C159	E@1U 4 V GMCEXP_RXP8	U26	PCIE_TX8P
GMCEXP_RXN8	C151	E@1U 4 V GMCEXP_RXN8	T27	PCIE_TX8N
GMCEXP_RXP9	C182	E@1U 4 V GMCEXP_RXP9	U26	PCIE_TX9P
GMCEXP_RXN9	C172	E@1U 4 V GMCEXP_RXN9	T26	PCIE_TX9N
GMCEXP_RXP10	C140	E@1U 4 V GMCEXP_RXP10	P25	PCIE_TX10P
GMCEXP_RXN10	C131	E@1U 4 V GMCEXP_RXN10	N25	PCIE_TX10N
GMCEXP_RXP11	C141	E@1U 4 V GMCEXP_RXP11	P27	PCIE_TX11P
GMCEXP_RXN11	C135	E@1U 4 V GMCEXP_RXN11	N27	PCIE_TX11N
GMCEXP_RXP12	C116	E@1U 4 V GMCEXP_RXP12	P26	PCIE_TX12P
GMCEXP_RXN12	C112	E@1U 4 V GMCEXP_RXN12	N26	PCIE_TX12N
GMCEXP_RXP13	C117	E@1U 4 V GMCEXP_RXP13	P25	PCIE_TX12P
GMCEXP_RXN13	C113	E@1U 4 V GMCEXP_RXN13	K25	PCIE_TX13N
GMCEXP_RXP14	C96	E@1U 4 V GMCEXP_RXP14	L27	PCIE_TX14P
GMCEXP_RXN14	C94	E@1U 4 V GMCEXP_RXN14	K27	PCIE_TX14N
GMCEXP_RXP15	C98	E@1U 4 V GMCEXP_RXP15	L26	PCIE_TX15P
GMCEXP_RXN15	C95	E@1U 4 V GMCEXP_RXN15	K26	PCIE_TX15N



PROJECT : ZL7
Quanta Computer Inc.

Size Custom Document Number **VGA HOST(ATI M26)** Rev C

Date: Thursday, June 23, 2005 Sheet 11 of 40



(125mA)

(30mA)

(6mA)

(80mA)

(7mA)

(5.8mA)

(40mA)

(2mA)

(85mA)

(350mA)

(15A)

CORE GND

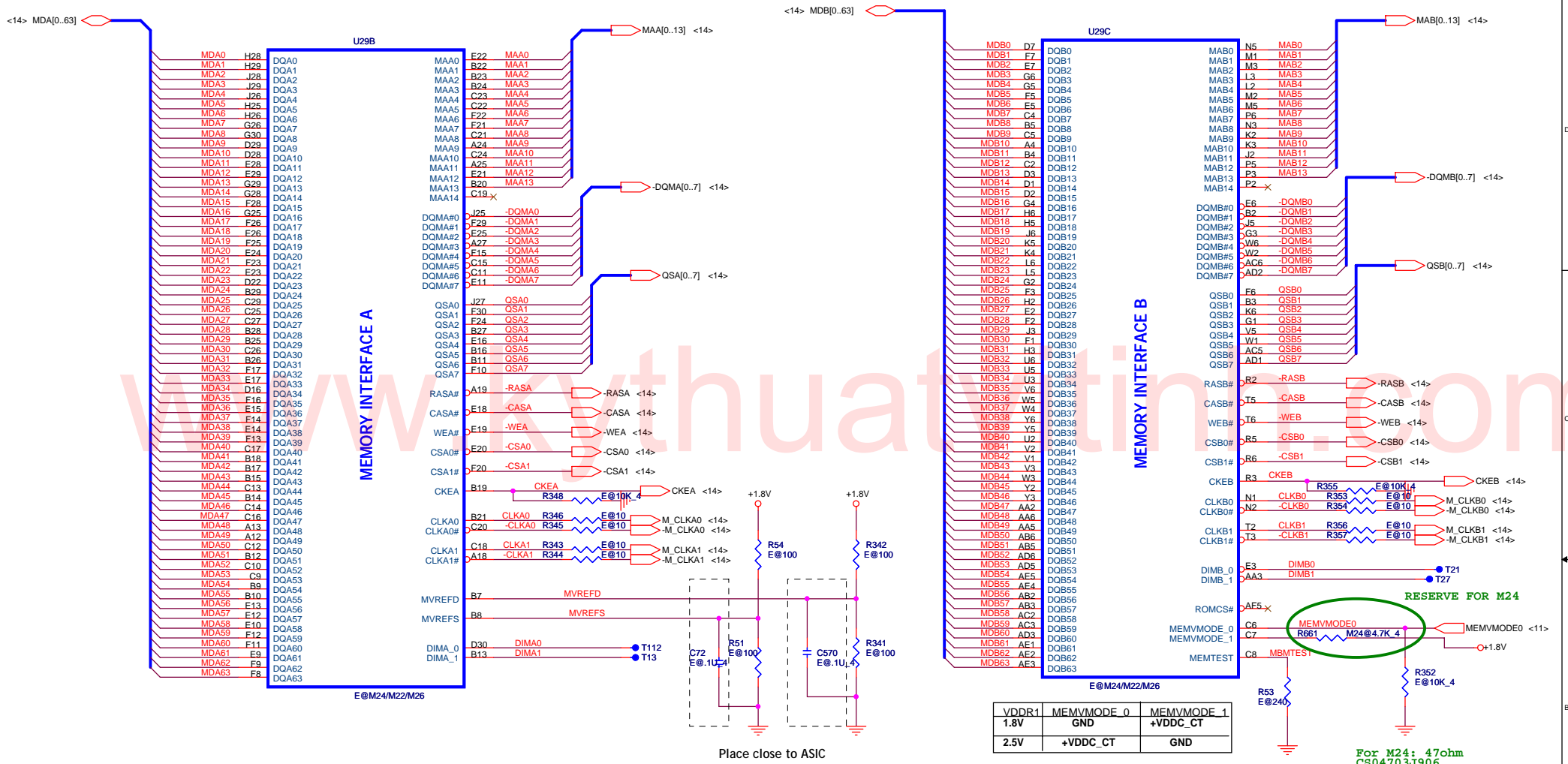
CENTER ARRAY

PROJECT : ZL3
Quanta Computer Inc.

ATI M26(POWER)

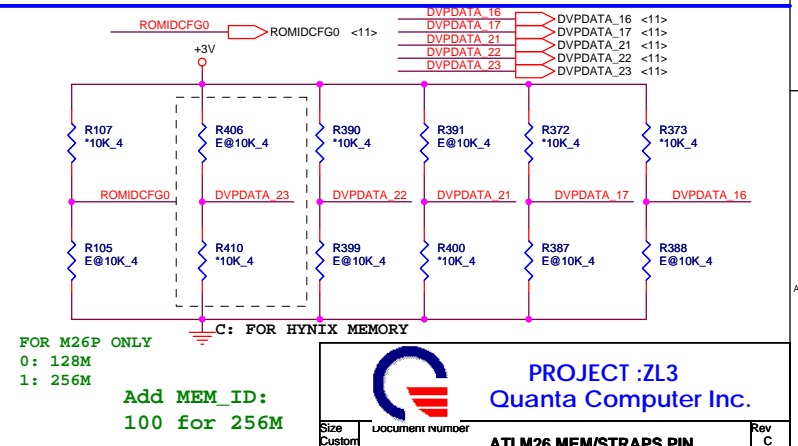
Size: Custom Document number: Rev: C

Date: Thursday, June 23, 2005 Sheet: 12 of 40



GPIO	Function
GPIO_0	PCI-Express Current Calibration Bandgap Backup 0: use reference voltage from Bandgap 1: use reference voltage from resistor divider
GPIO_1	PCI-Express PLL Calibration force enable 0: Disable PLL force calibration 1: Enable PLL force calibration
GPIO_(3,2)	00: PCI Express 1.0 mode 01: RESERVED 10: PCI Express 1.0 mode 11: RESERVED
GPIO_4	Turn off PCI-Express impedance / strength calibration 0: enable 1: disable
GPIO_5	Bypass PCI-Express PLL

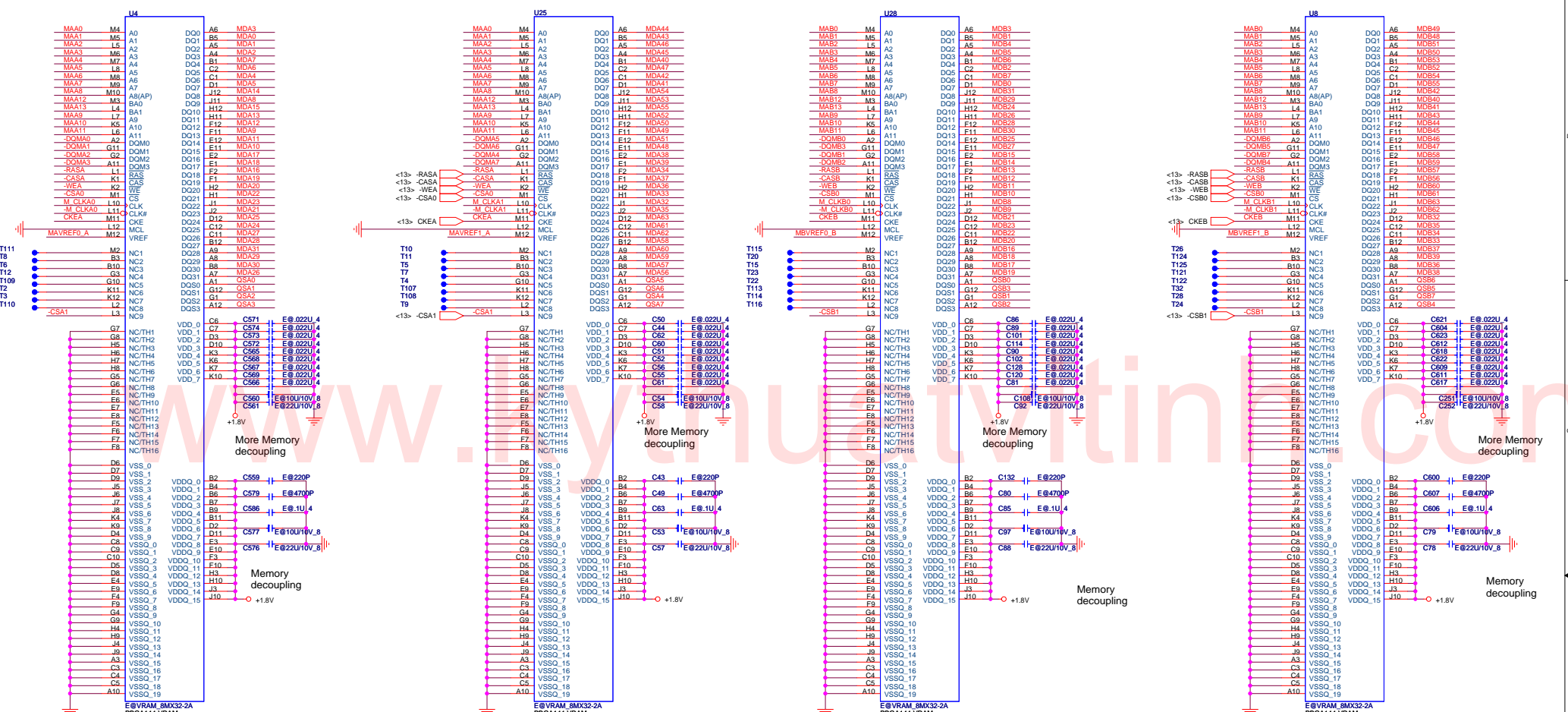
GPIO	Function
GPIO_6	PCI-Express transmitter current compensation 0: Normal 1: Inject extra current for output buffer switching
GPIO_8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible
GPIO(9,13:11)	ROMIDCFG 0x0x: No ROM, CHG_ID=0 0x1x: No Rom, CHG_ID=1 1000: Parallel ROM, Chip ID'S from ROM 1000: Parallel ROM, Chip ID'S from ROM
DVPDATA_21-23	DVPDATA_21: 0=4Mx32 1=8Mx32 DVPDATA_22: 0=128M 1=64M DVPDATA_23: 0=Hynix 1=Samsung



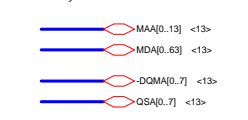
PROJECT :ZL3
Quanta Computer Inc.

Size: Custom | Document number: ATi M26 MEM/STRAPS PIN | Rev: C

Date: Thursday, June 23, 2005 | Sheet: 13 of 40

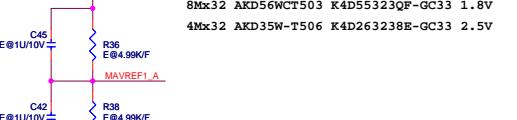


VGA DDR MEMORY A
 @64/128MBytes DDR 128Mbit 1MX32X4 uBGA

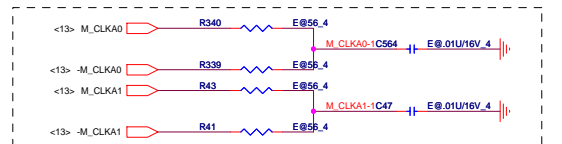


Place close to memory

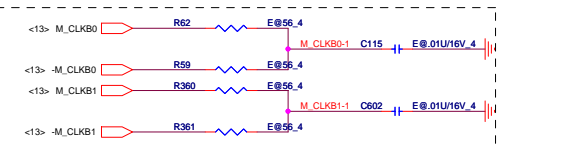
VGA DDR MEMORY B
 @64/128MBytes DDR 128Mbit 1MX32X4 uBGA



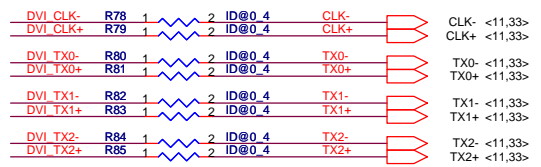
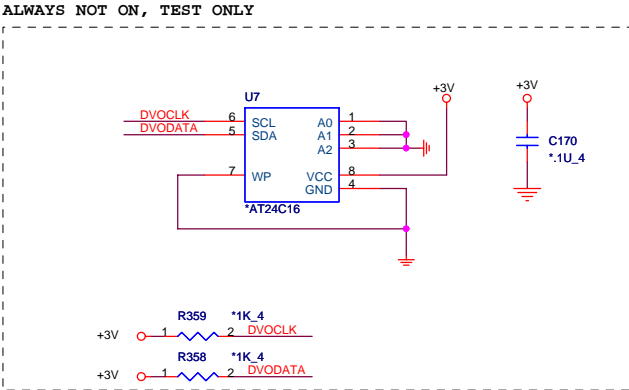
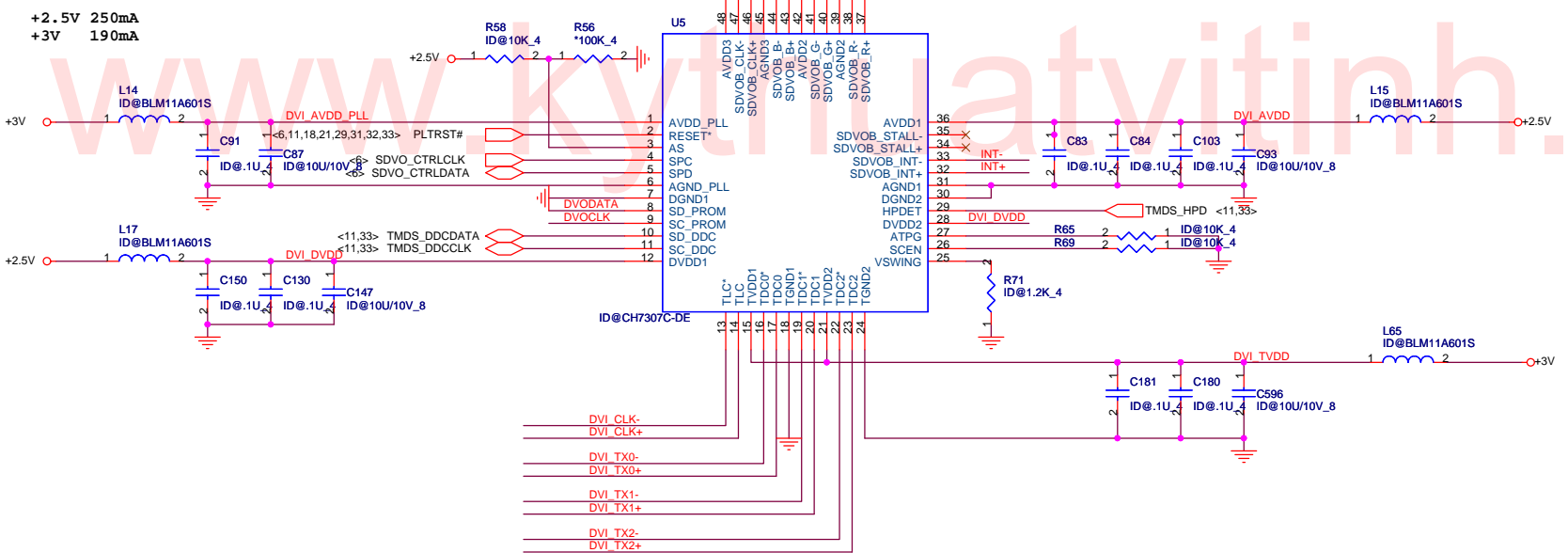
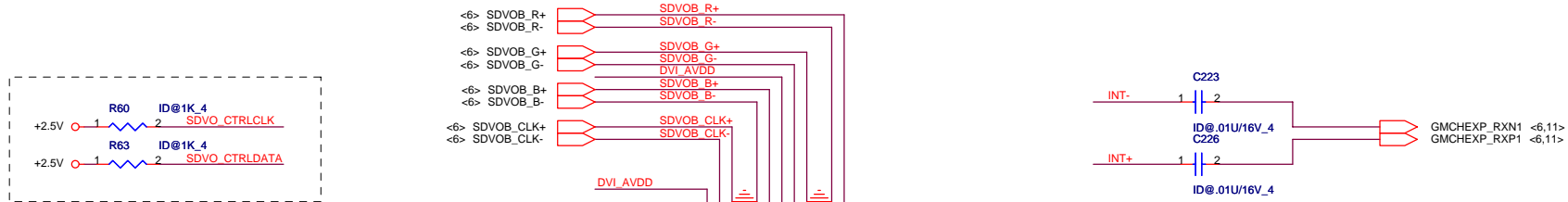
Place close to memory

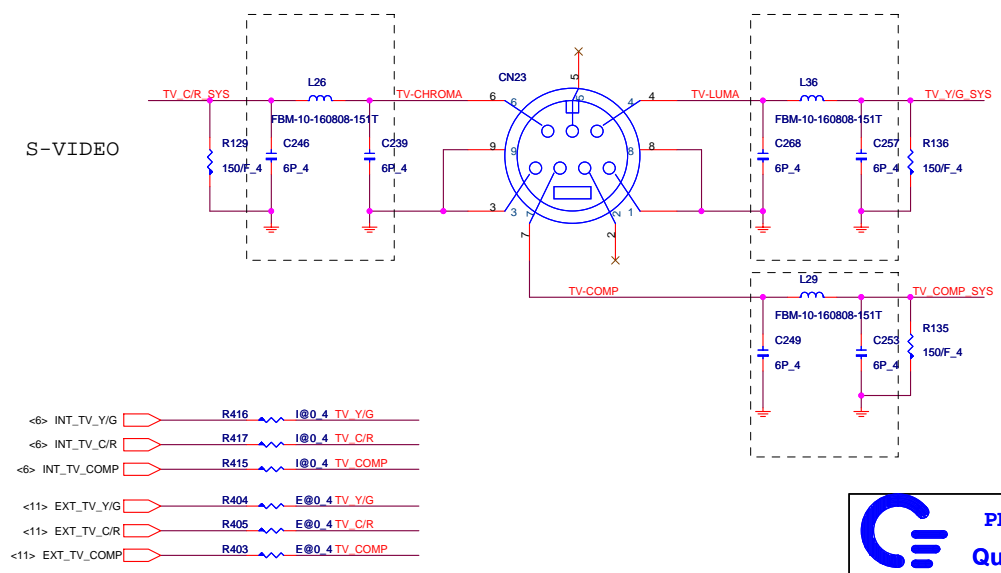
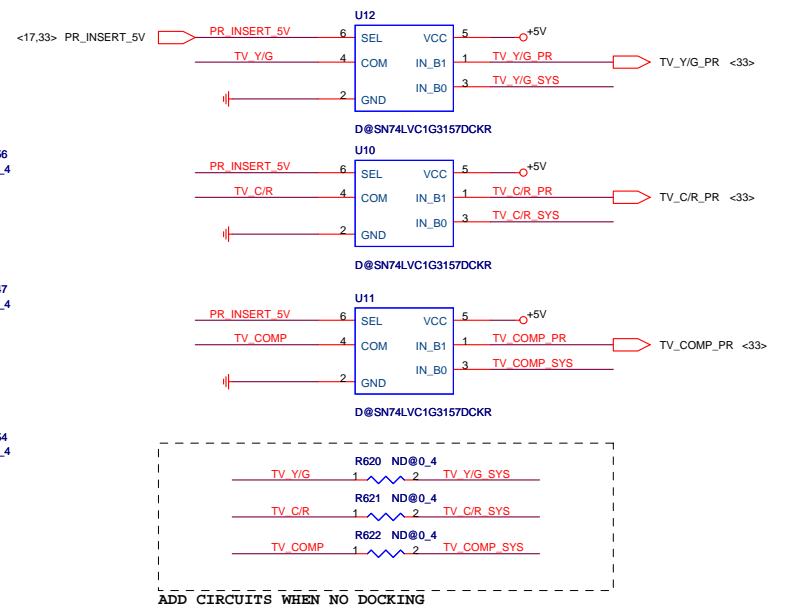
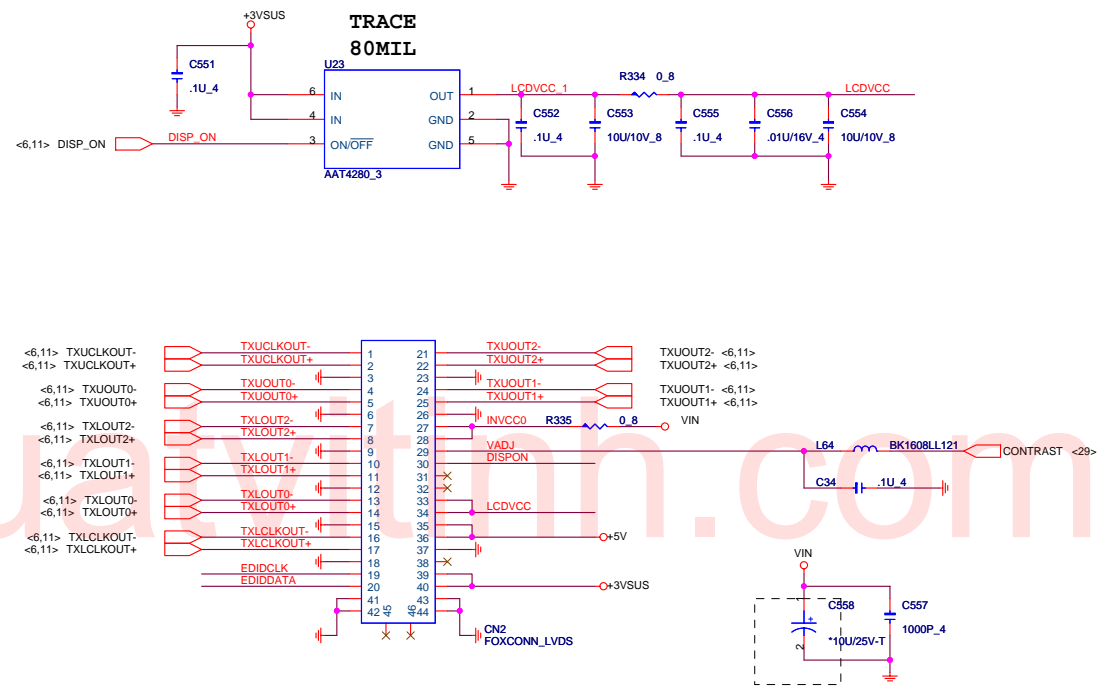
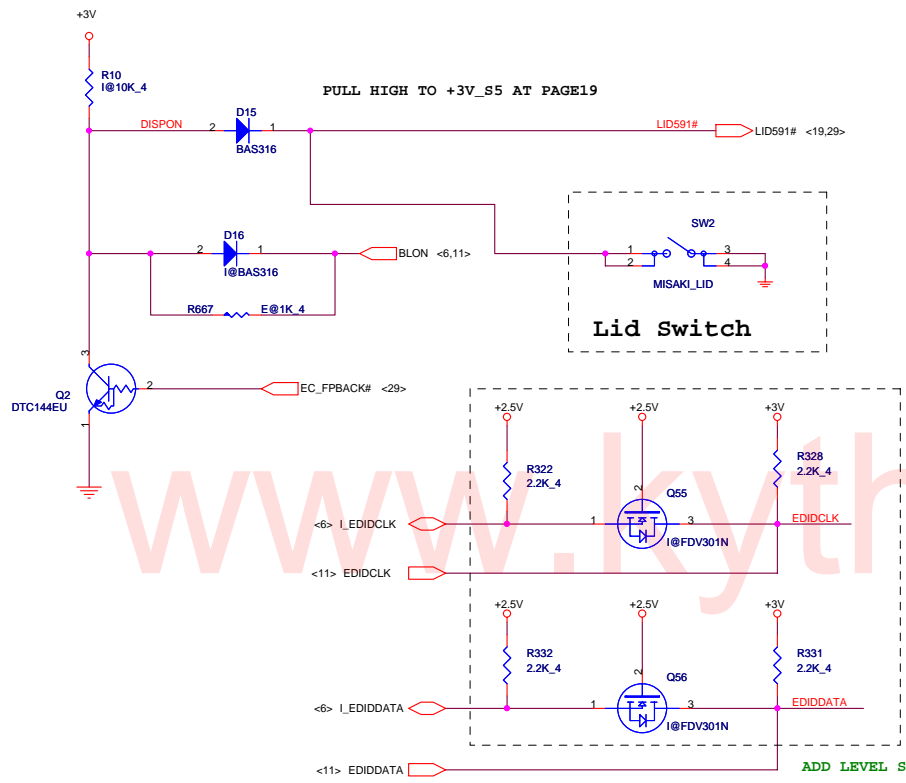


At least a 2.5:1 spacing between the pair
 These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory



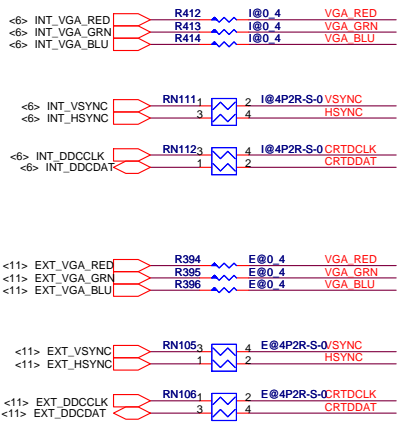
At least a 2.5:1 spacing between the pair
 These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory



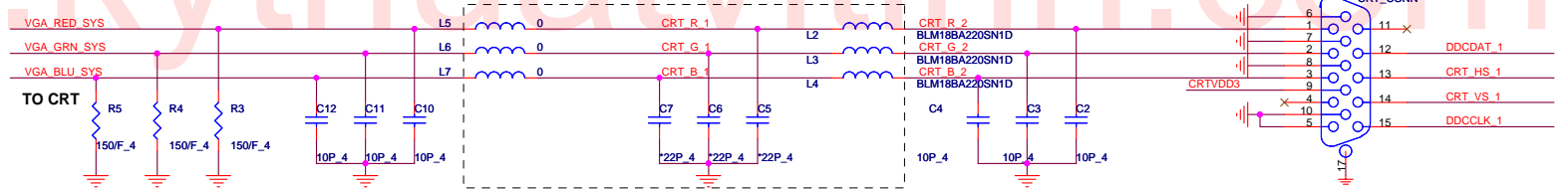
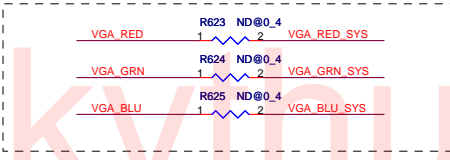
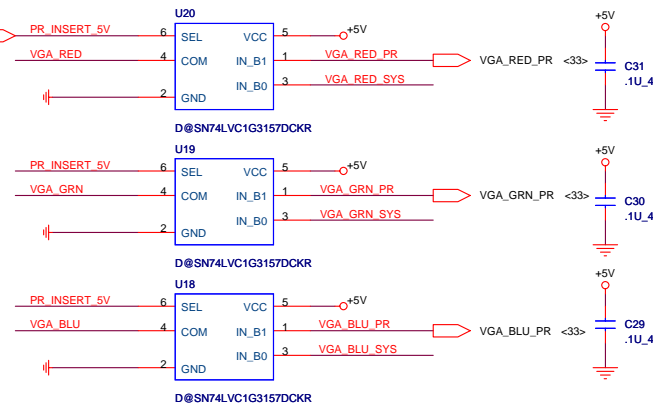


PROJECT : ZL7
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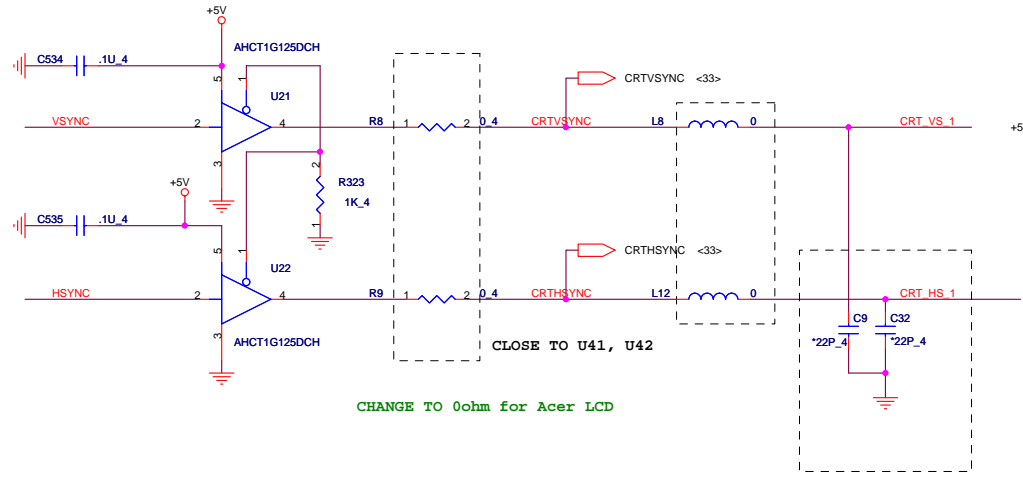
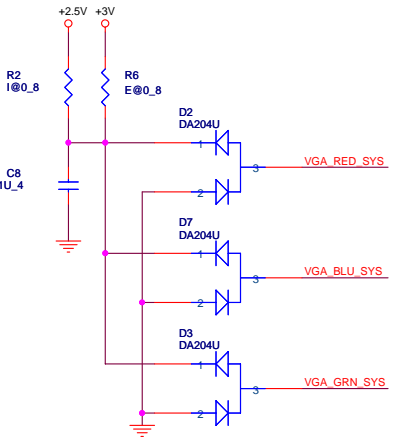
Size	Document Number	Rev
	DVO CH7011A & RJ45-11 CON	C
Date:	Thursday, June 23, 2005	Sheet 16 of 40



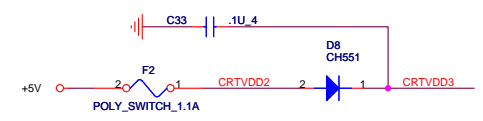
SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

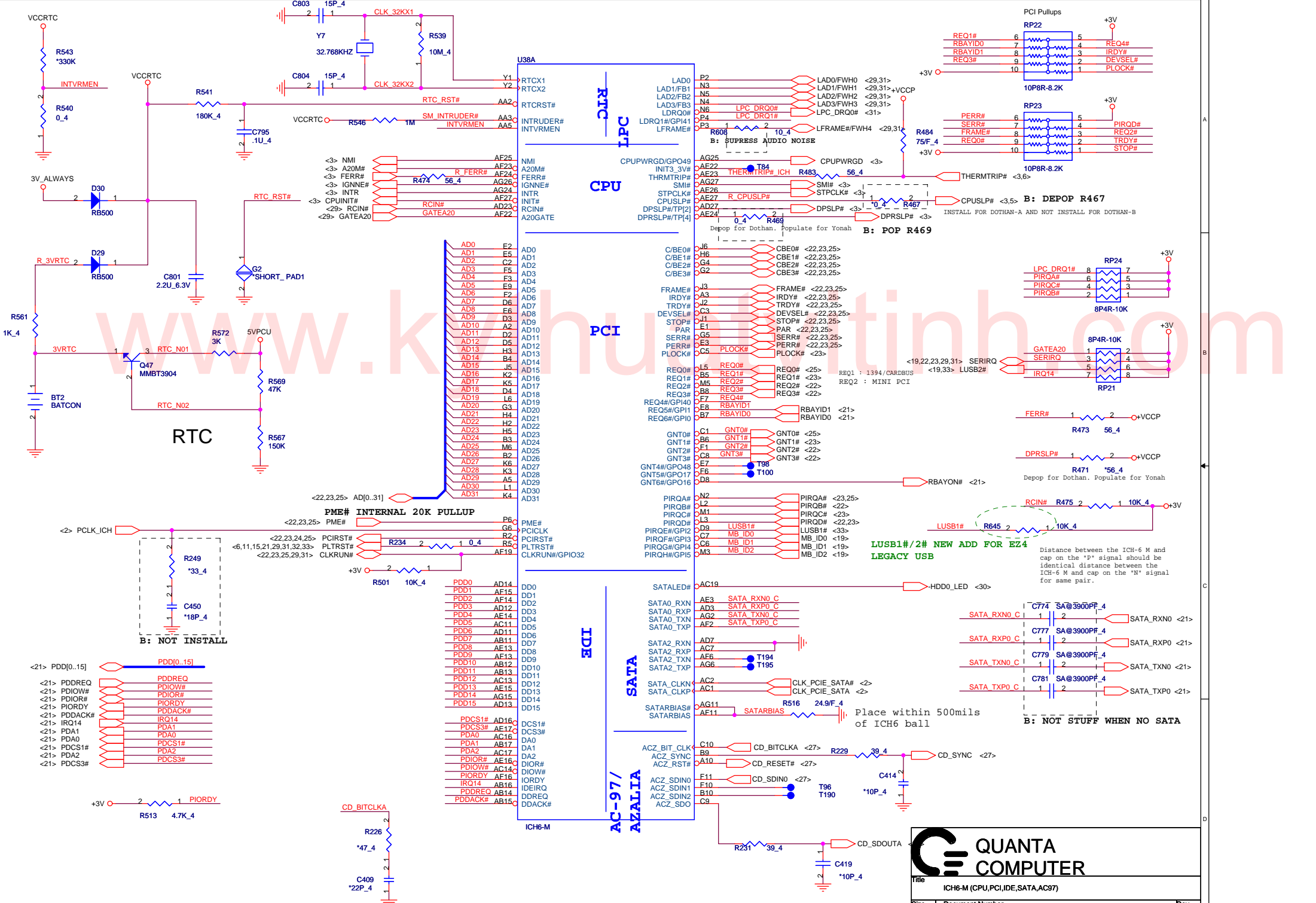


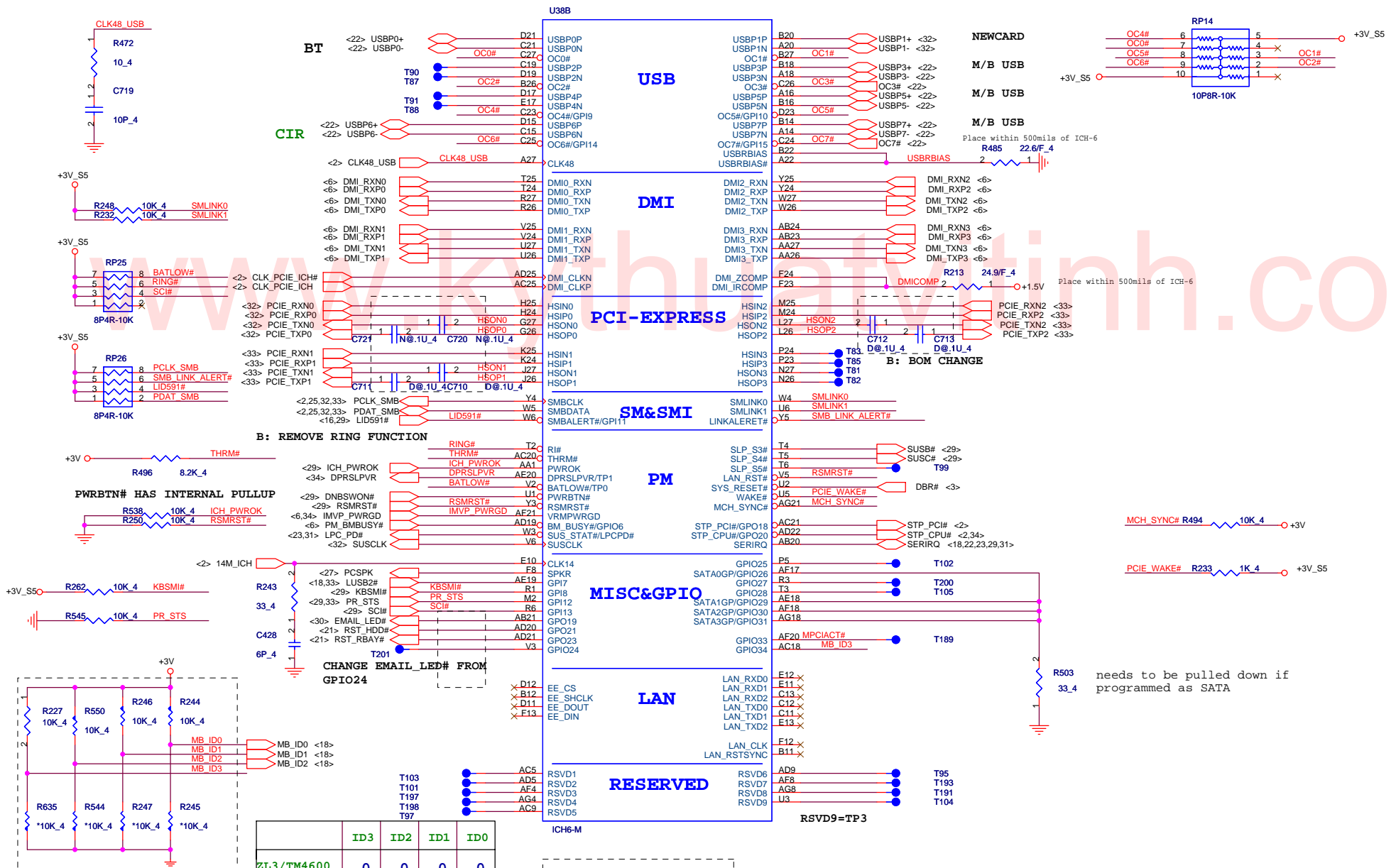
Change to FDV301N for Vgs issue.



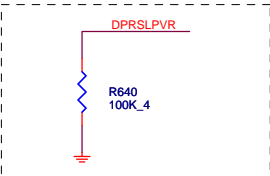
CHANGE TO 0ohm for Acer LCD



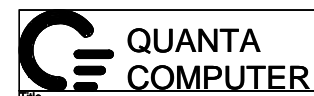


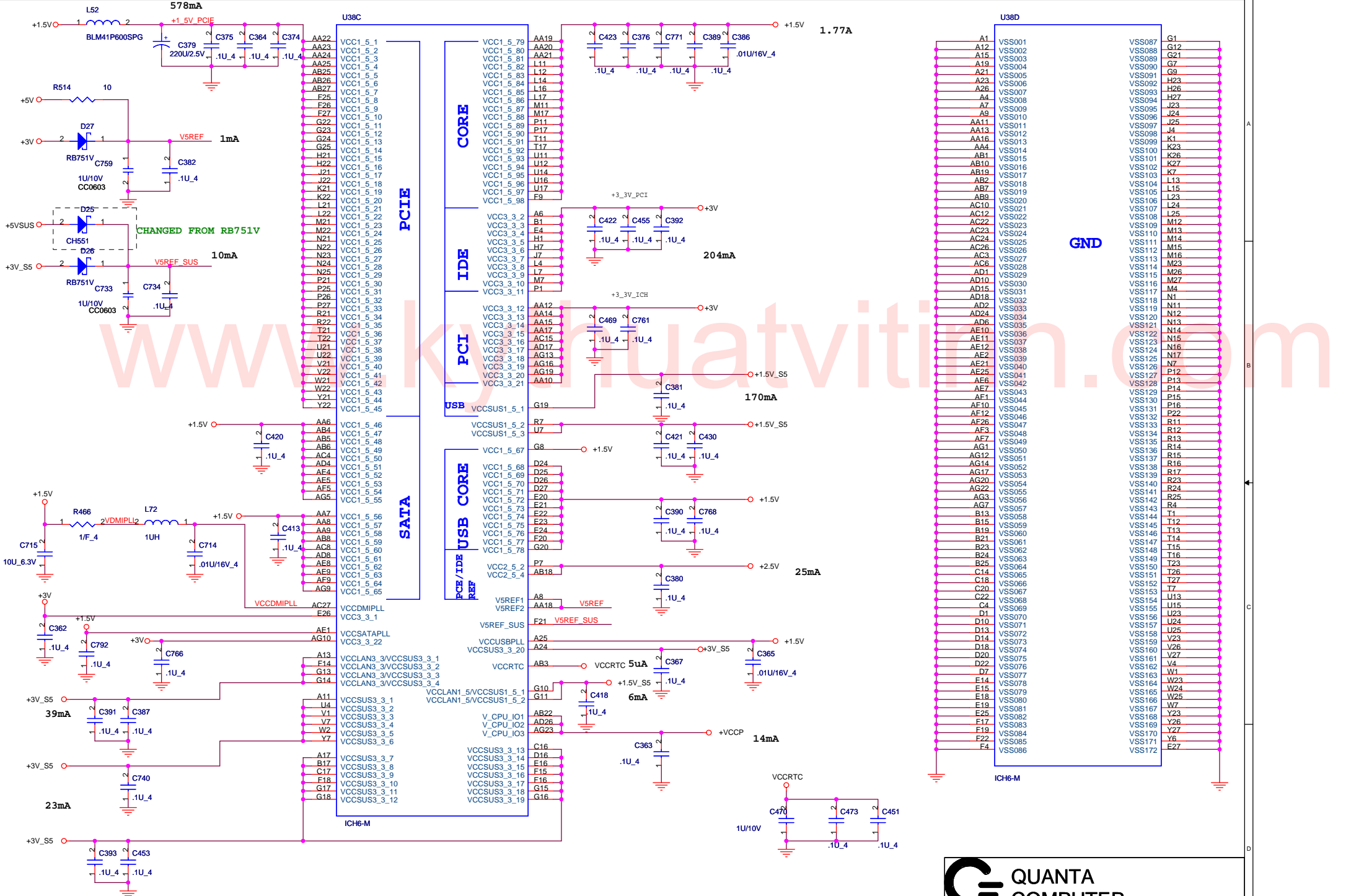


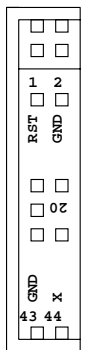
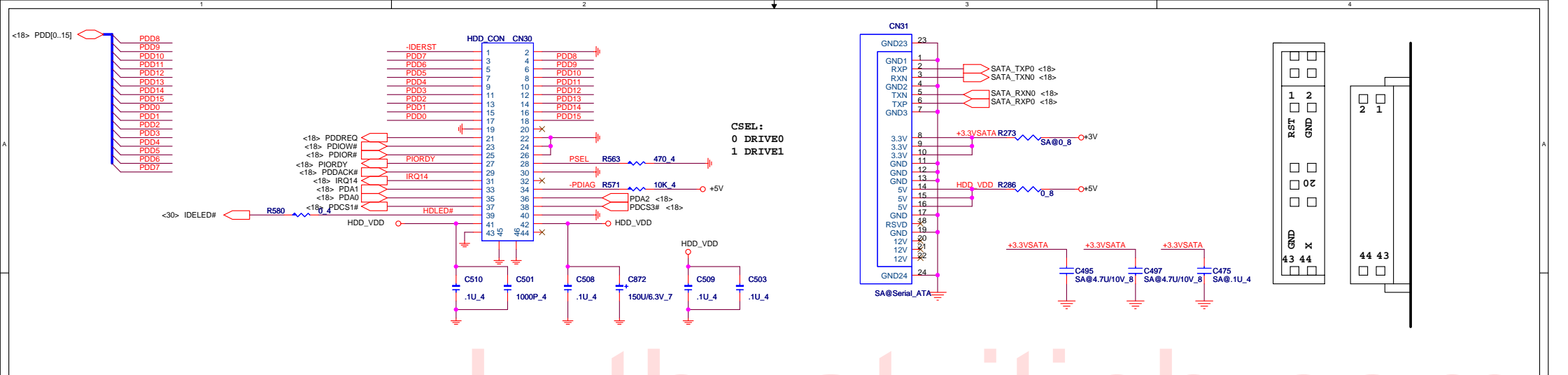
	ID3	ID2	ID1	ID0
ZL3/TM4600	0	0	0	0
ZL3B/TM4100	0	0	1	0
ZL3D/AS1690	0	1	0	0
ZL3F/AS3510	0	1	1	0
ZL3C/EX4100	1	0	1	1



ADD PULLLOW





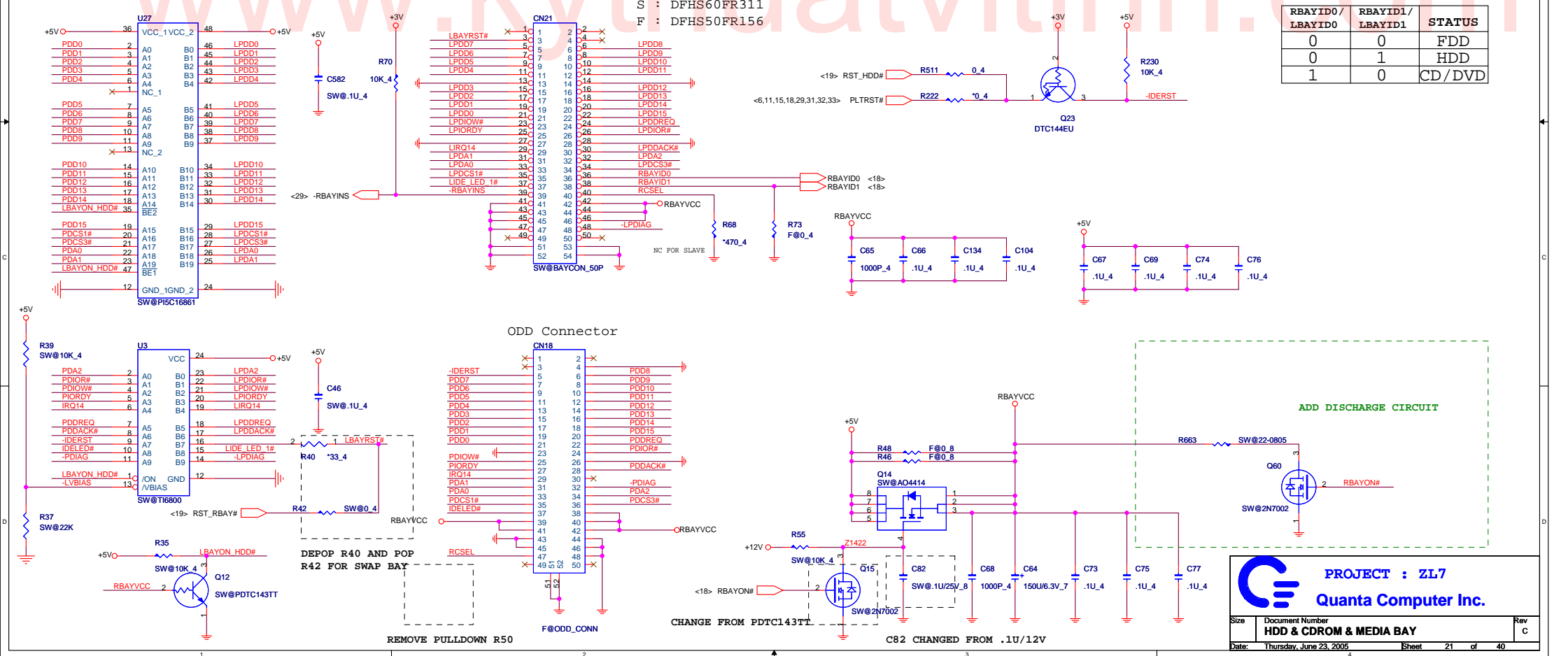


Media Bay Connector

S : DFHS60FR311
F : DFHS50FR156

BAY ID STATUS

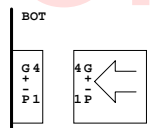
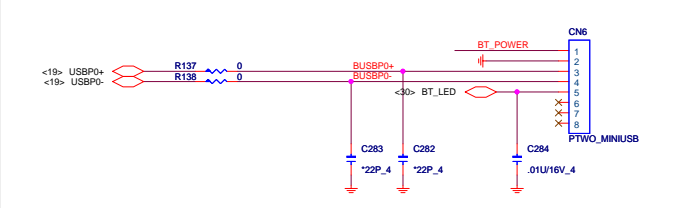
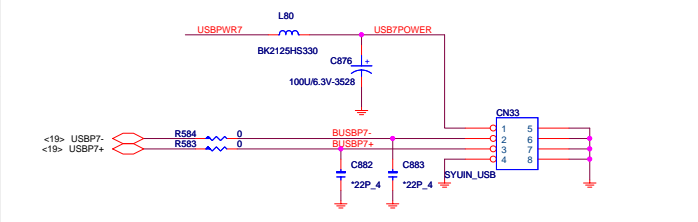
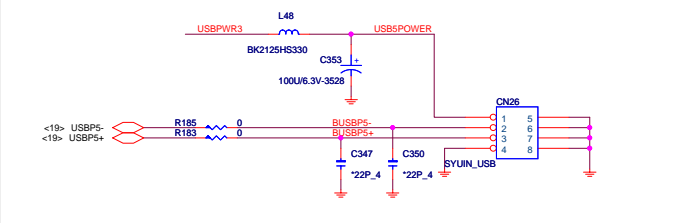
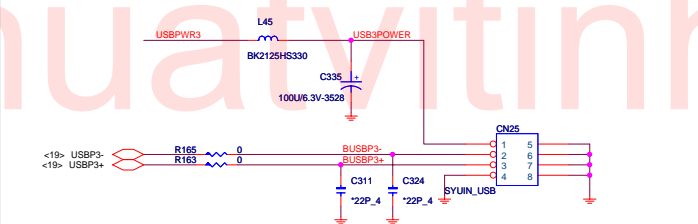
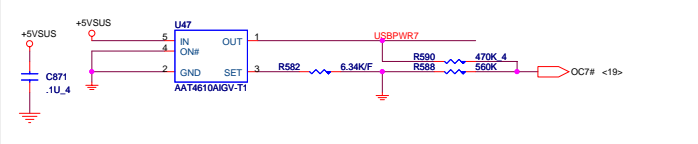
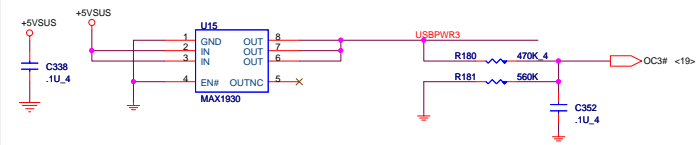
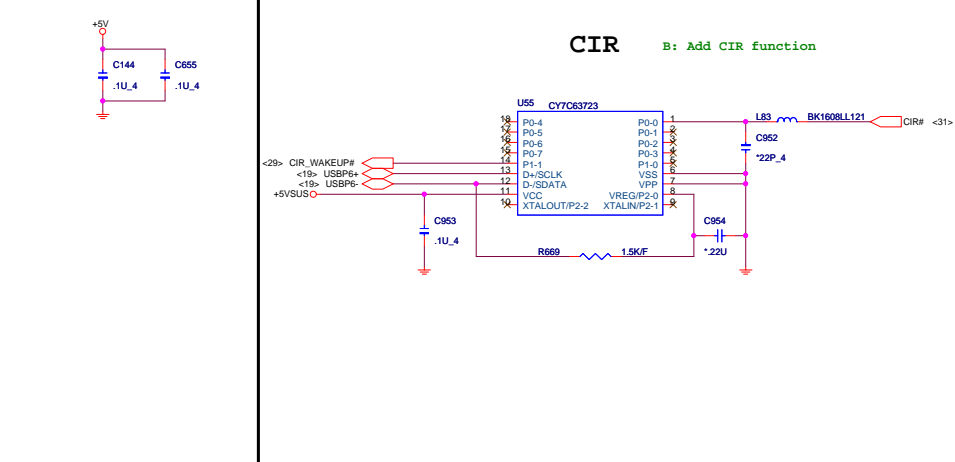
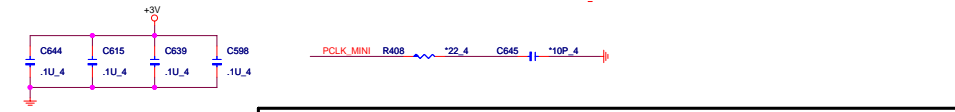
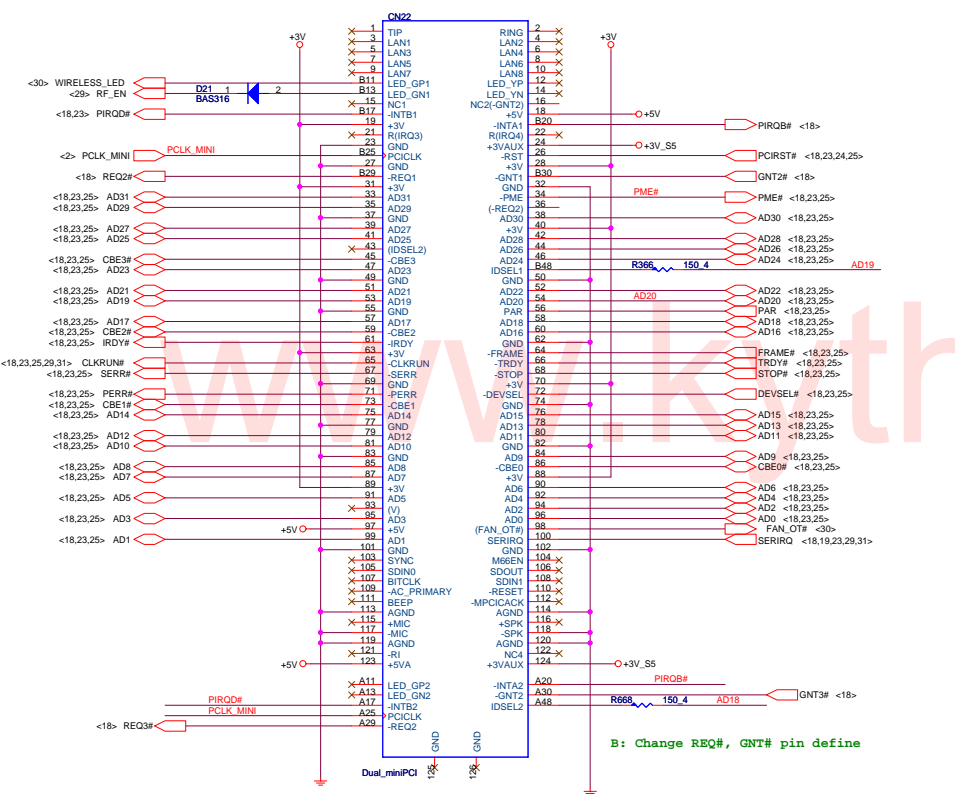
RBAYID0 / LBAYID0	RBAYID1 / LBAYID1	STATUS
0	0	FDD
0	1	HDD
1	0	CD/DVD

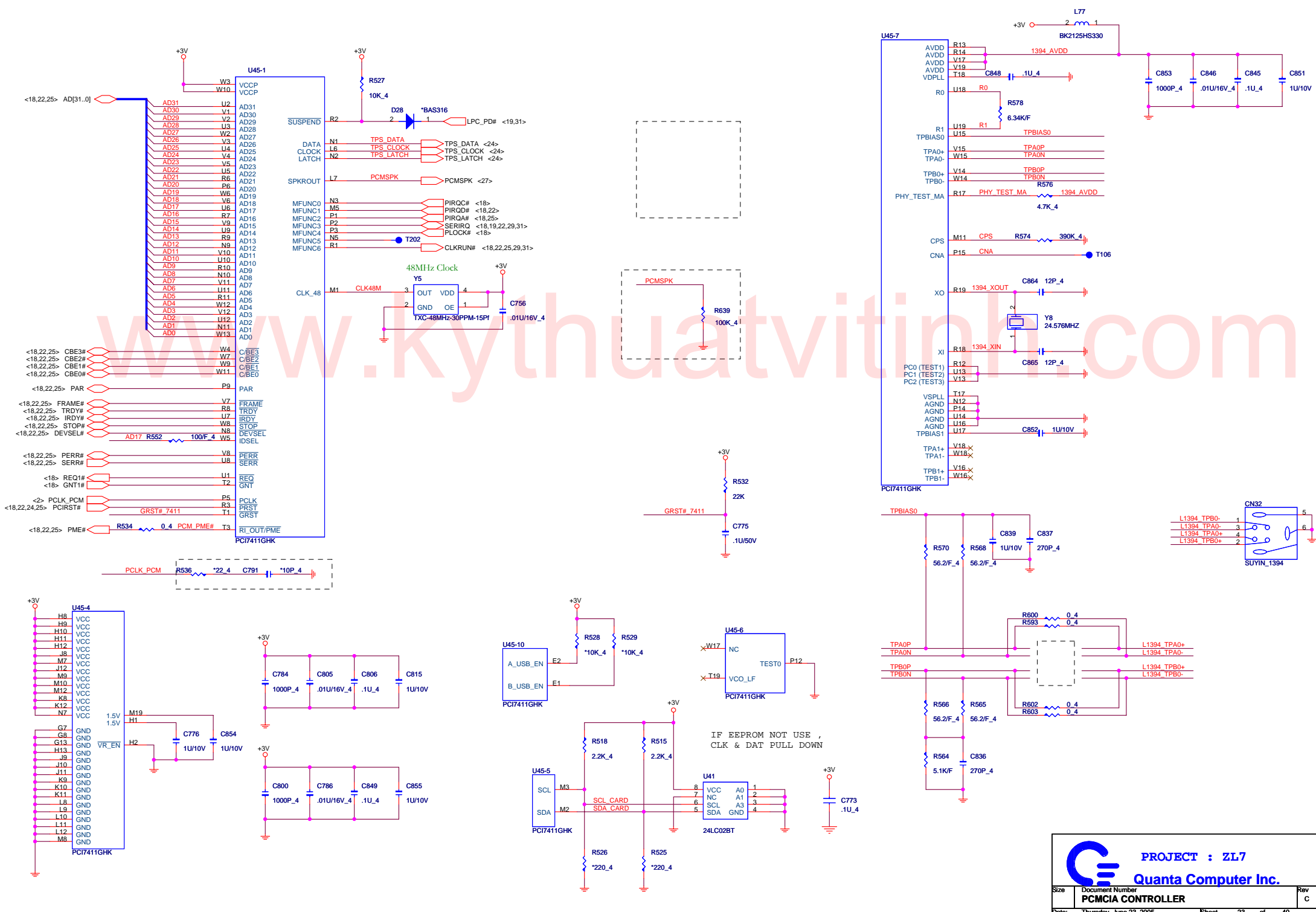


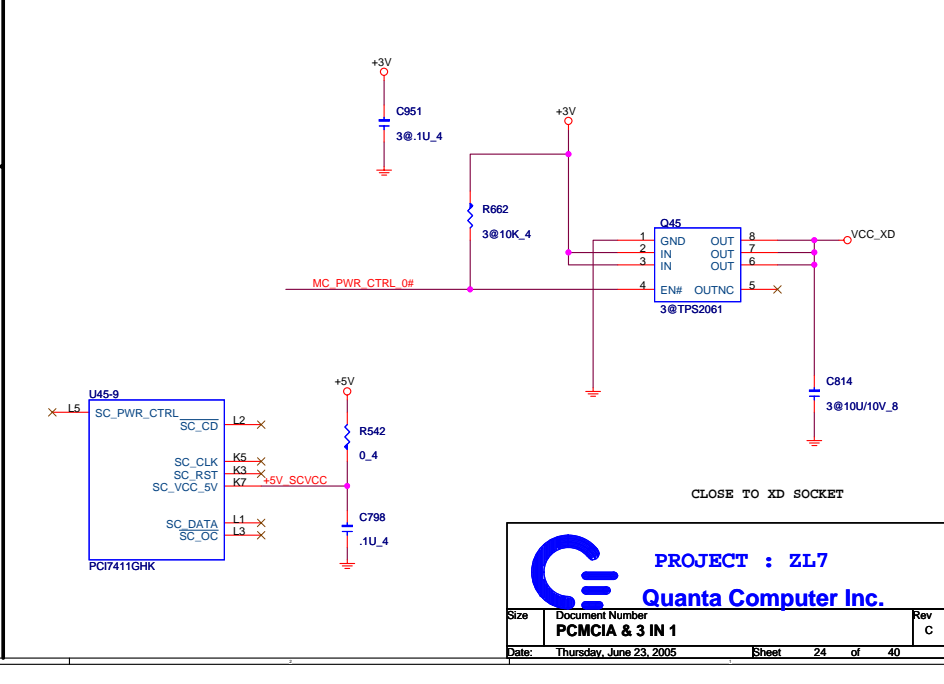
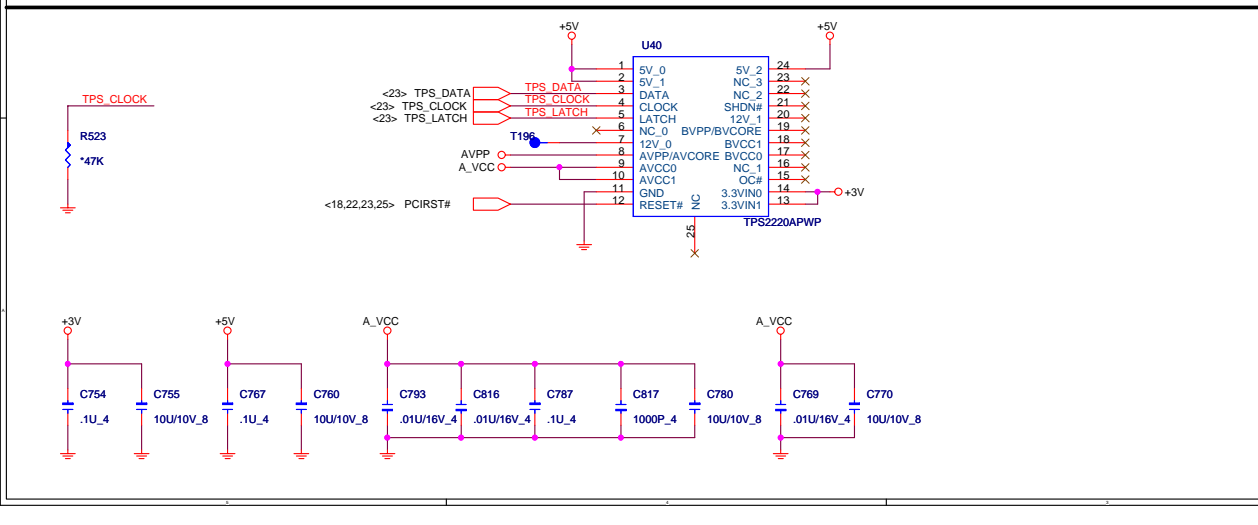
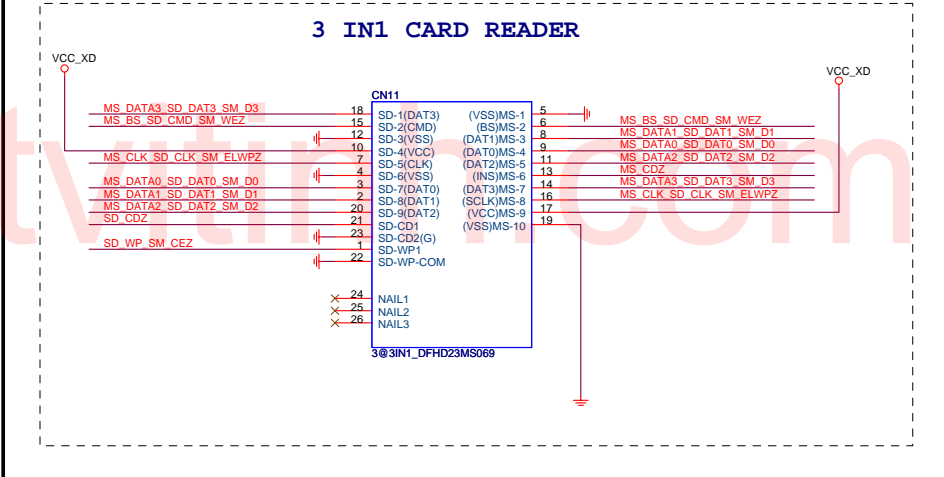
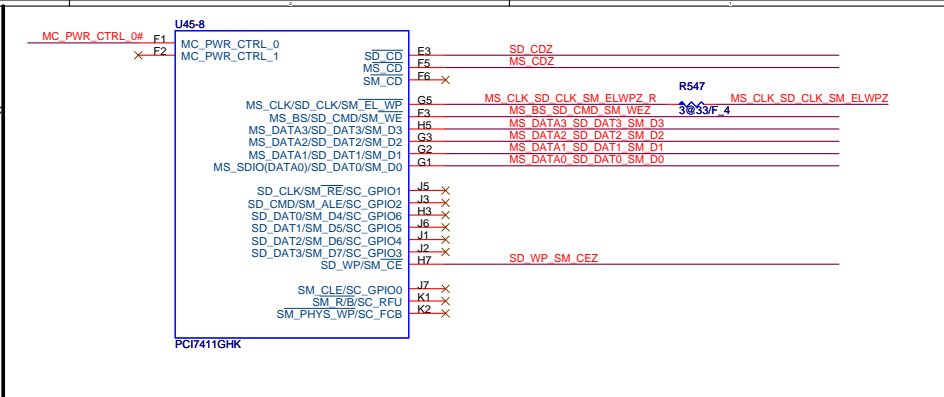
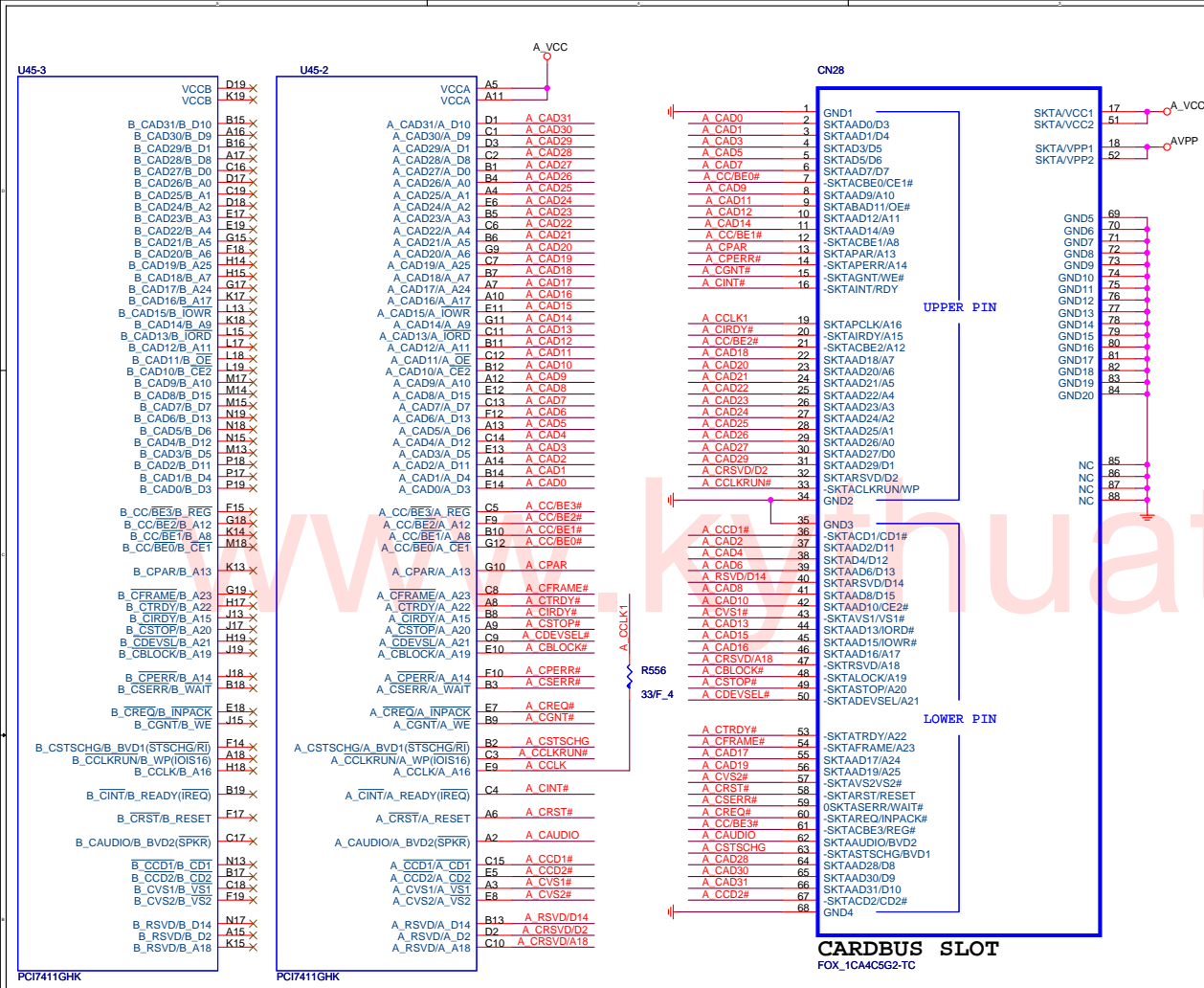
PROJECT : ZL7
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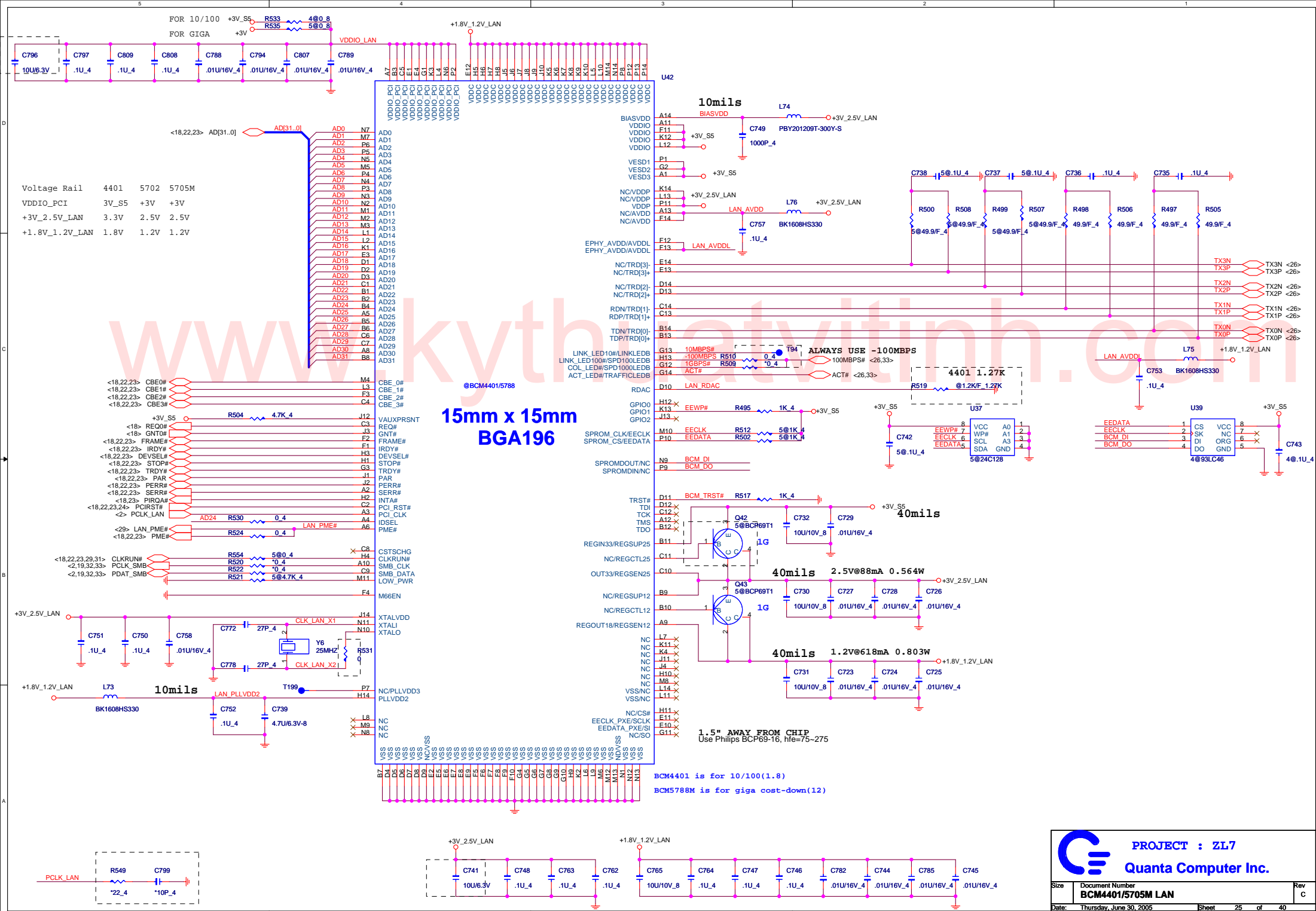
Size	Document Number	Rev
	HDD & CDROM & MEDIA BAY	C
Date:	Thursday, June 23, 2005	Sheet 21 of 40

MINI-PCI







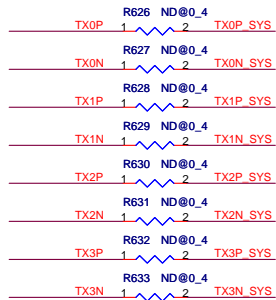
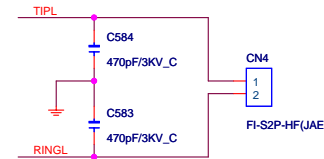
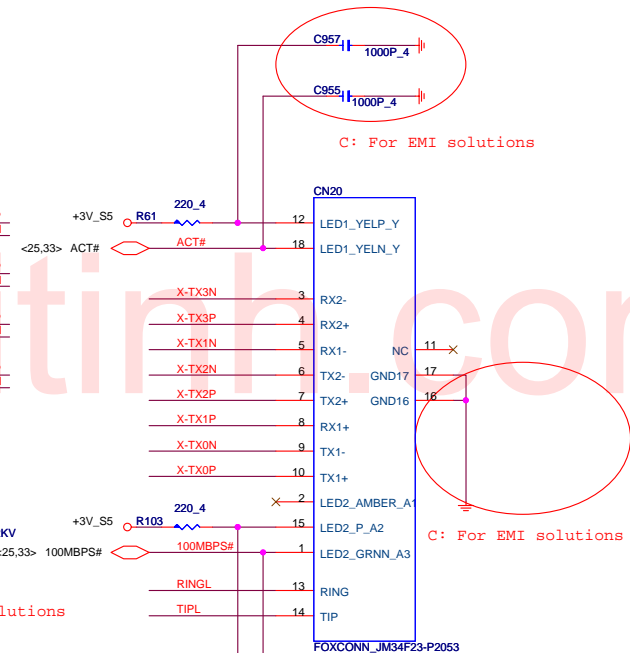
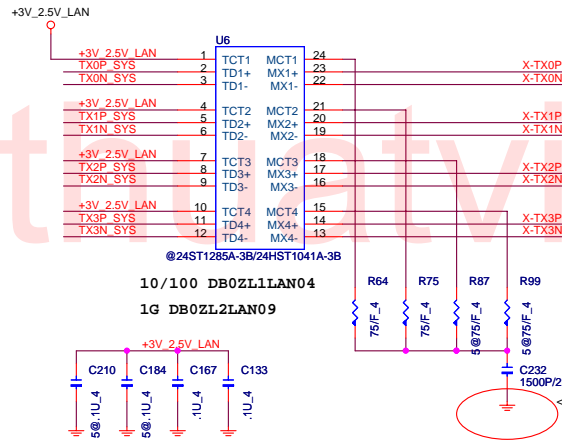
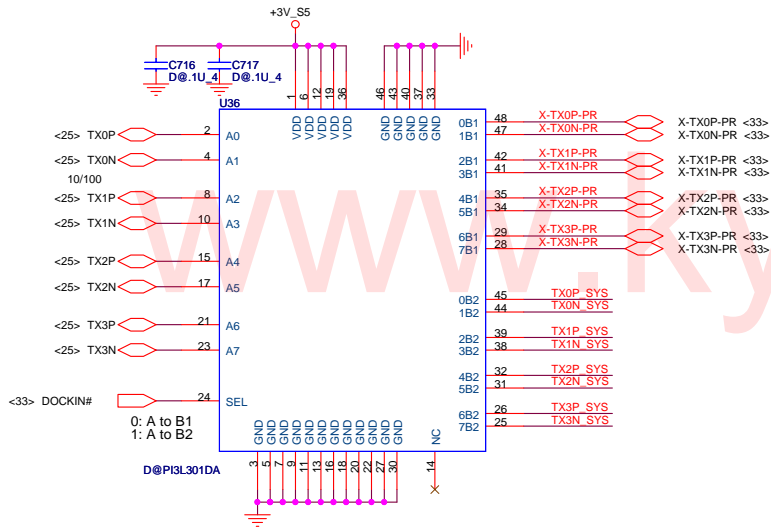


Voltage Rail

4401	5702	5705M
VDDIO_PCI	3V_S5	+3V
+3V_2.5V_LAN	3.3V	2.5V
+1.8V_1.2V_LAN	1.8V	1.2V

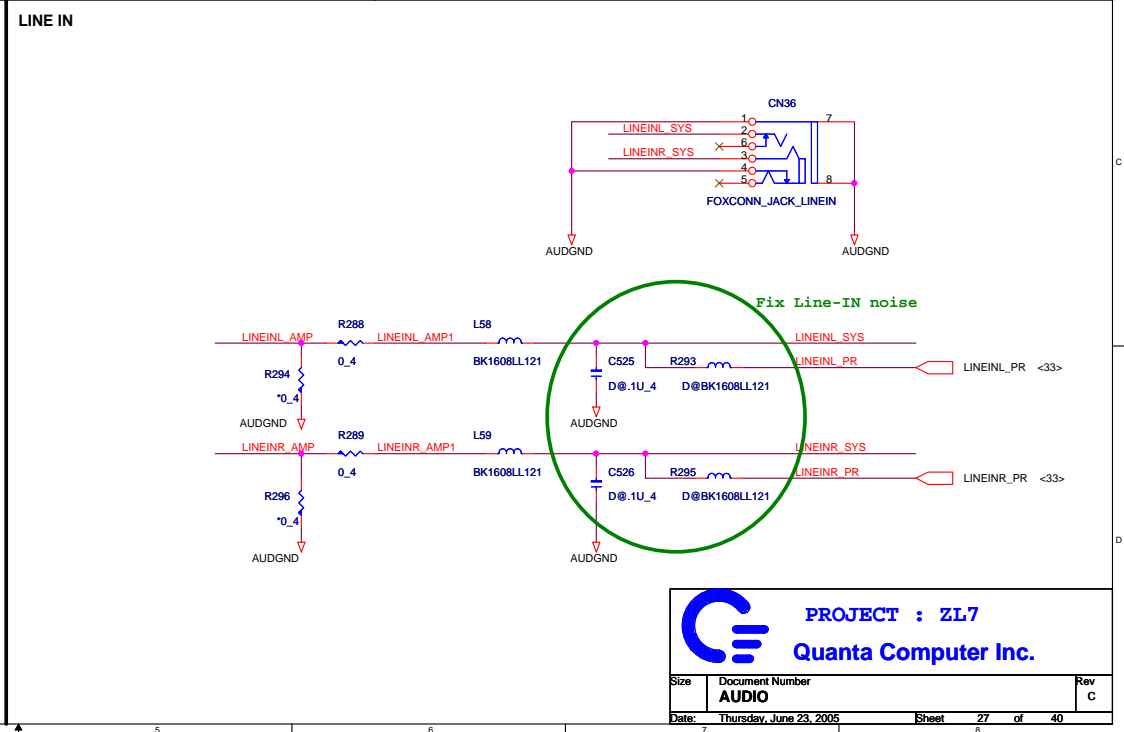
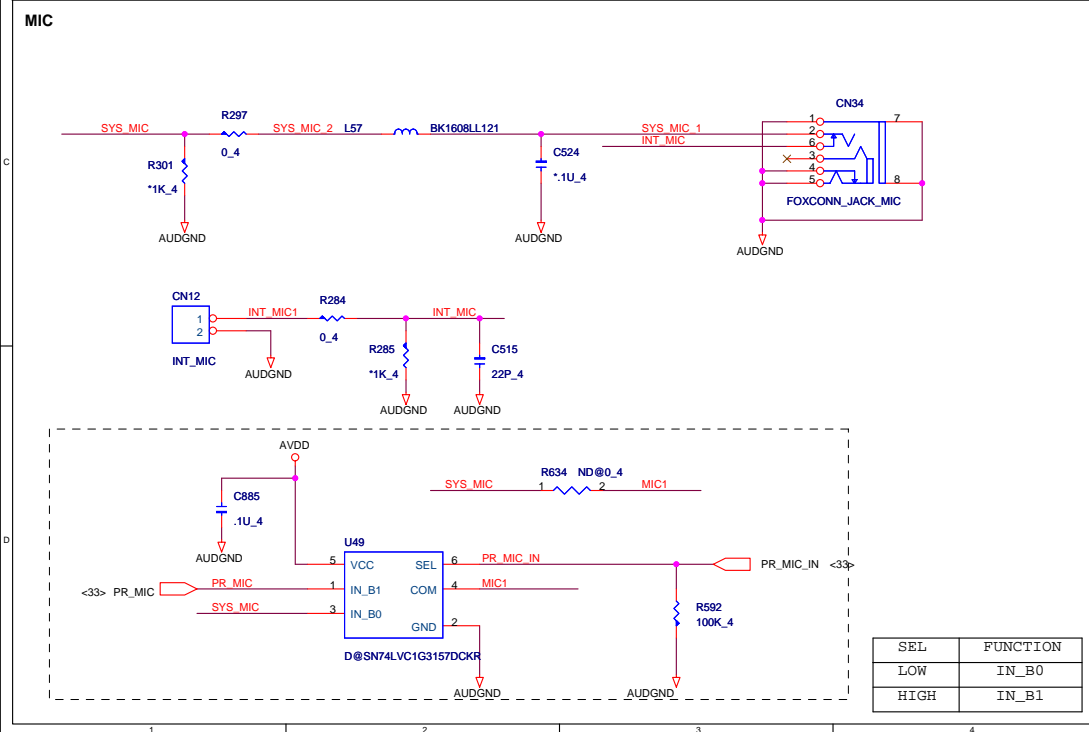
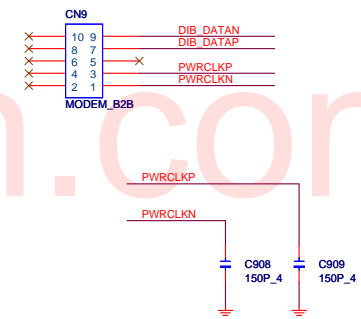
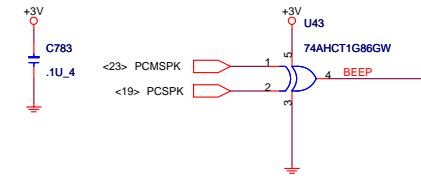
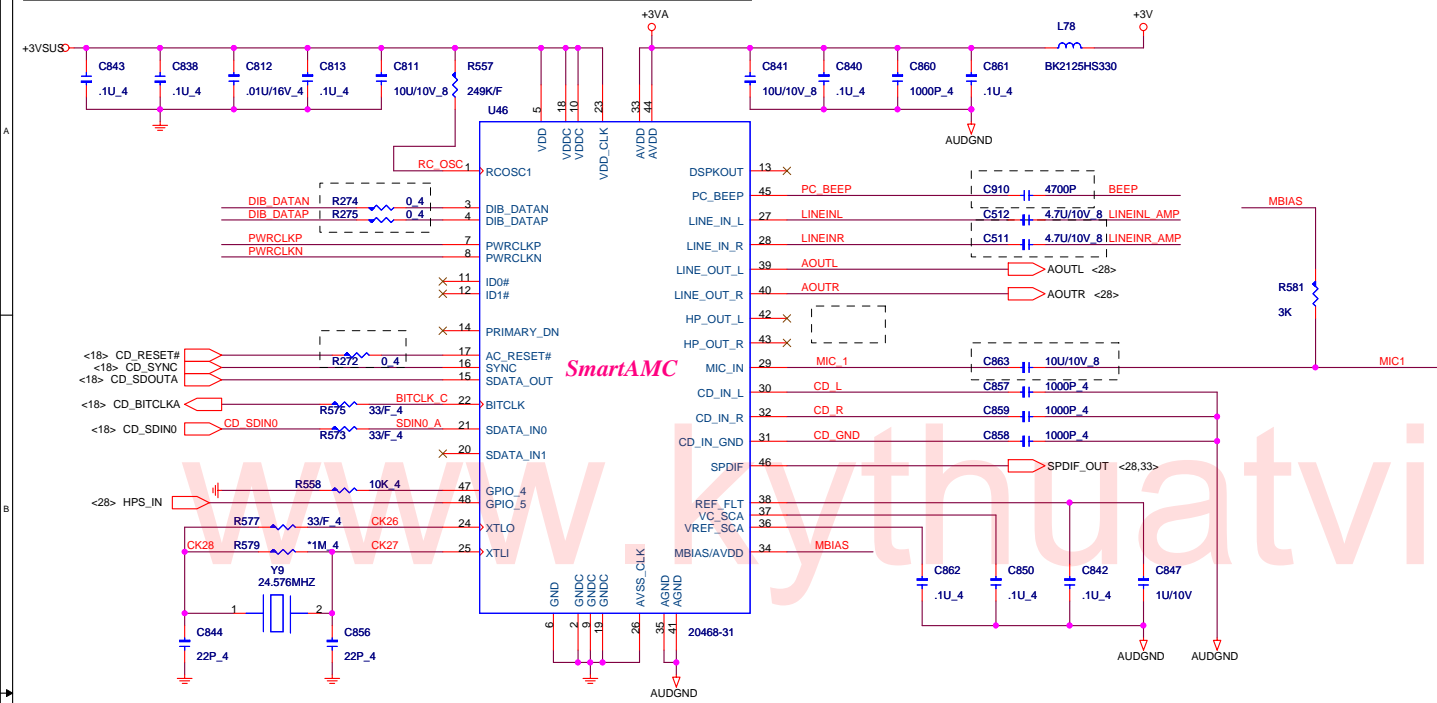
**15mm x 15mm
BGA196**

BCM4401 is for 10/100(1.8)
BCM5788M is for giga cost-down(12)

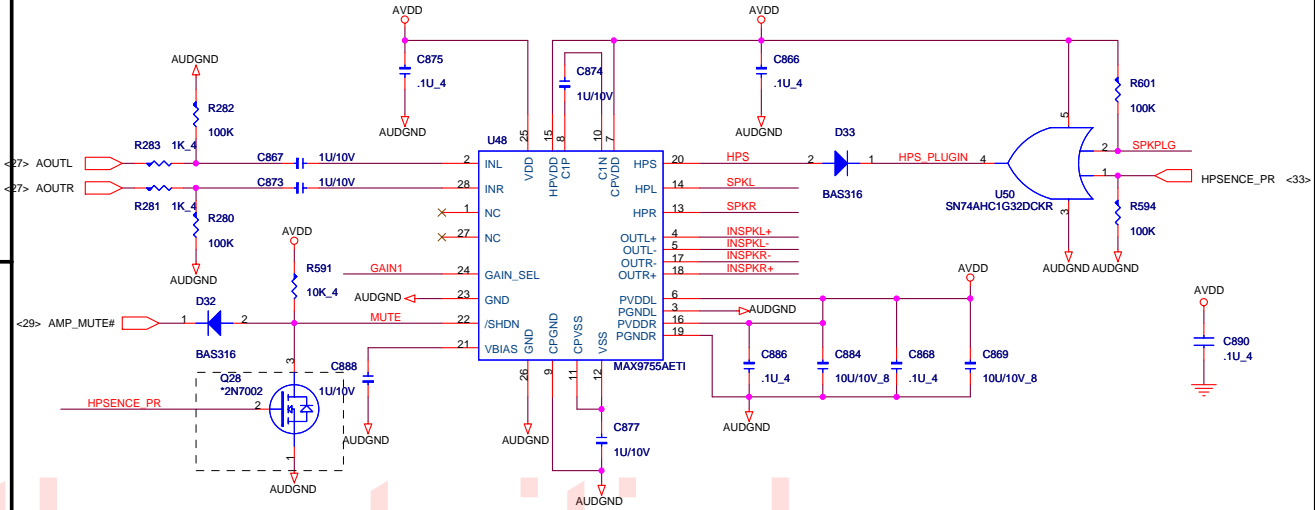
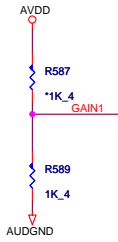


ADD CIRCUITS WHEN NO DOCKING

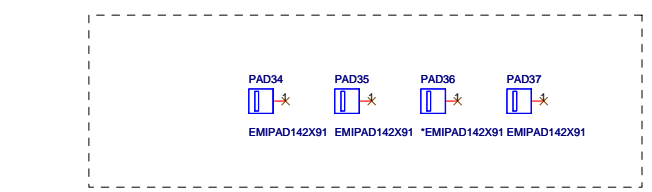
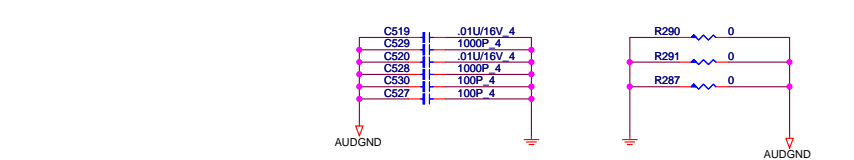
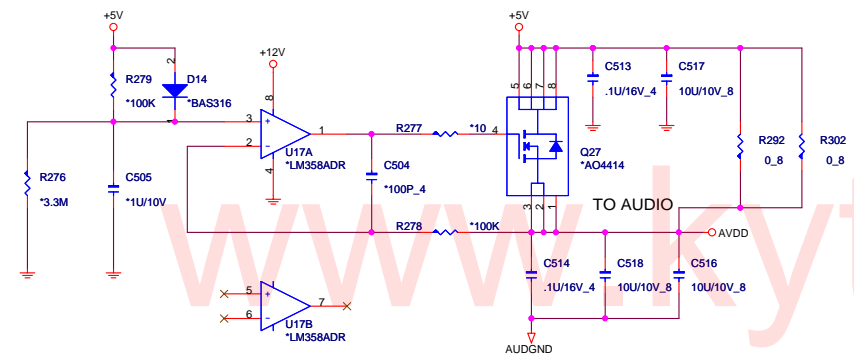
The AMC20463-004 modem is used for mother board family MBAMC20463-004.



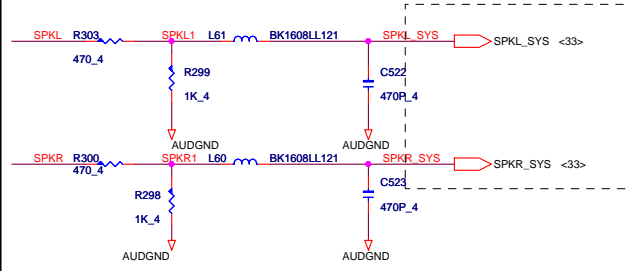
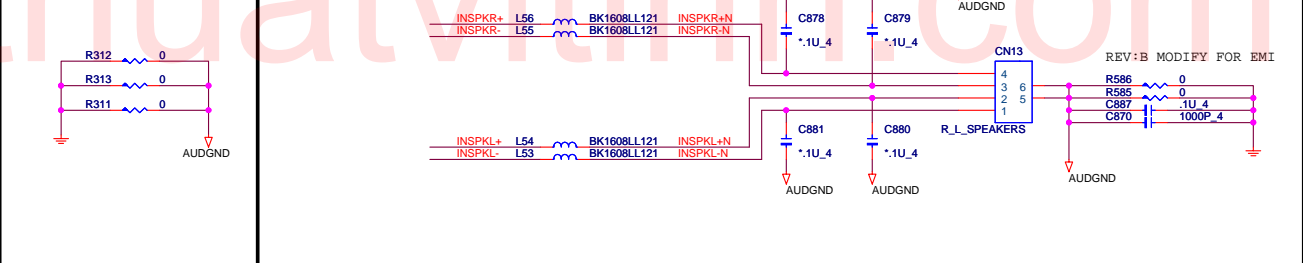
GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0



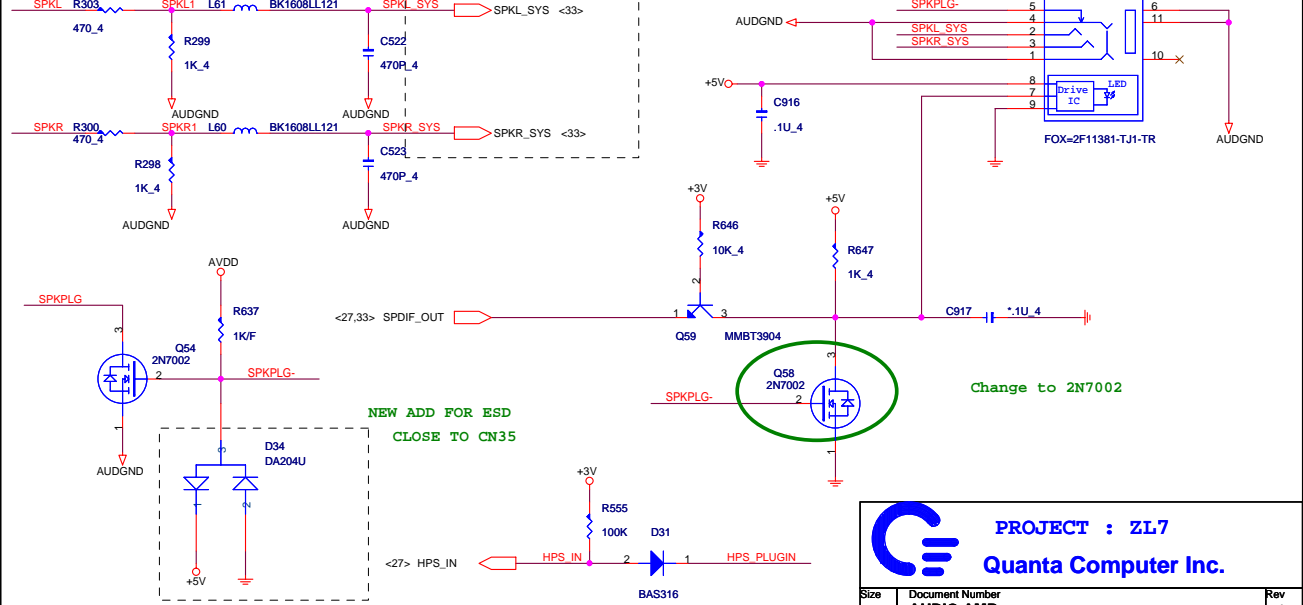
AMP POWER



SPEAKER CON.



LINE OUT&SPDIF

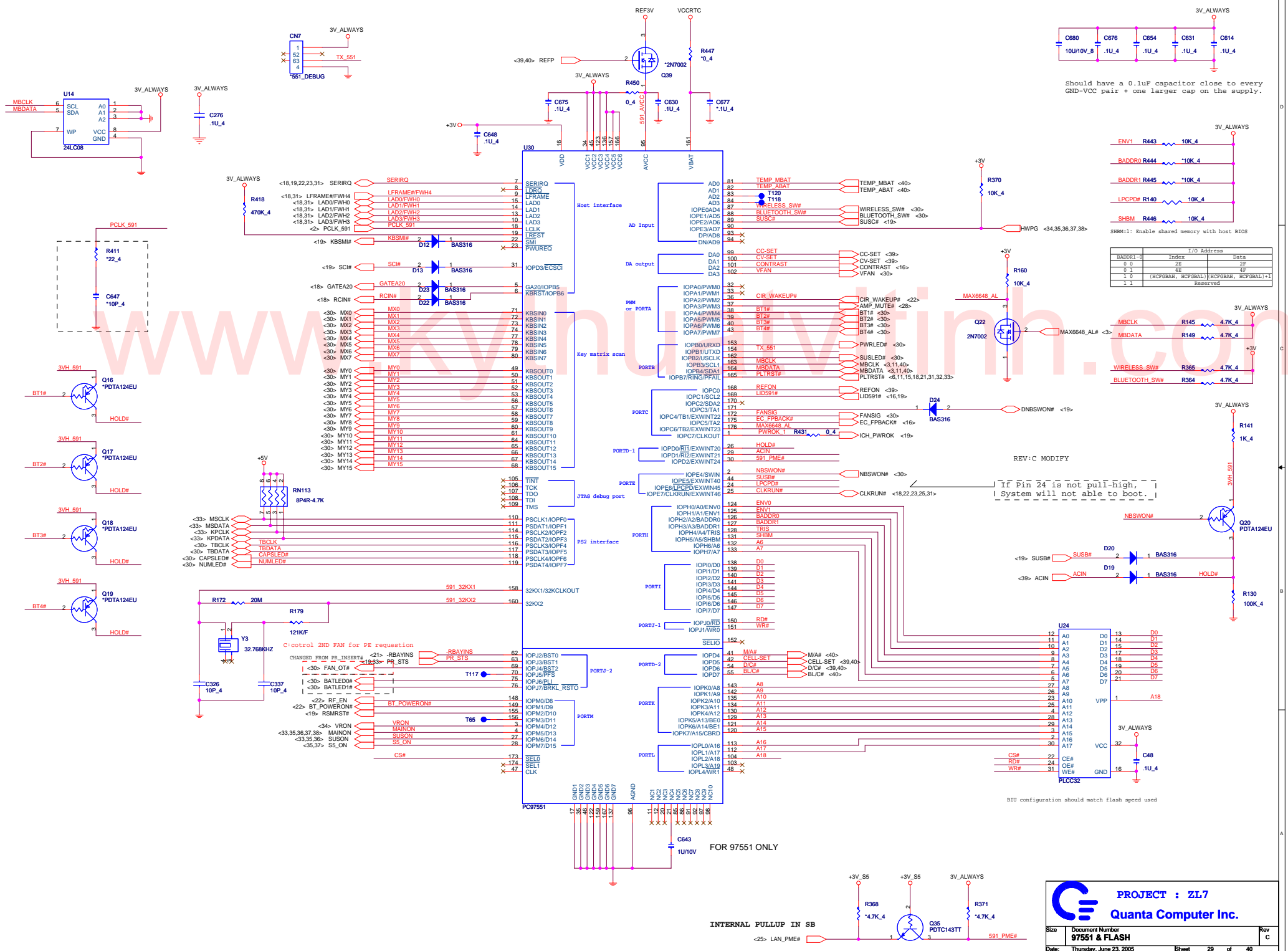


NEW ADD FOR ESD
CLOSE TO CN35

Change to 2N7002

PROJECT : ZL7
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LDRQ#(pin 8) internal is no use



Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

I/O Address	Index	Data
BADR[1:0]		2F
0	0	4F
1	0	Reserved
1	1	Reserved

SBM#1: Enable shared memory with host BIOS

REV:C MODIFY
If Pin 24 is not pull-high, System will not able to boot.

BIU configuration should match flash speed used

PROJECT : ZL7

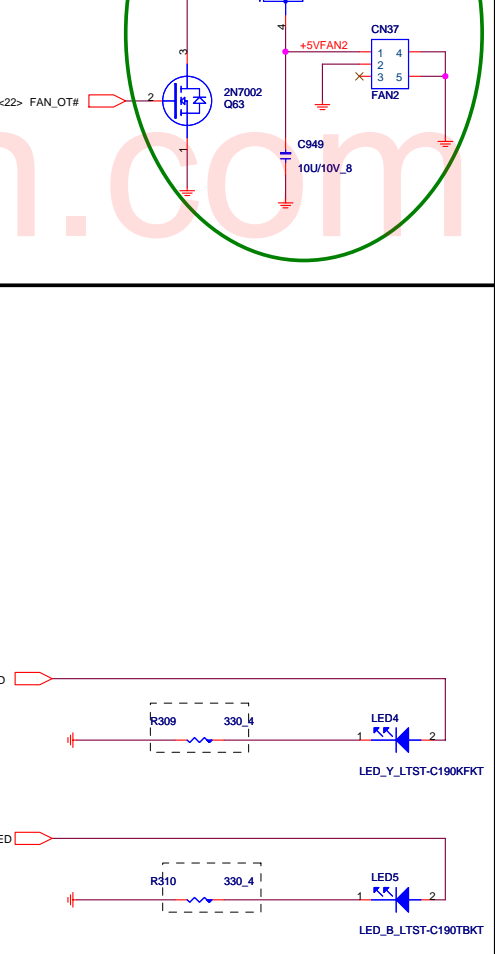
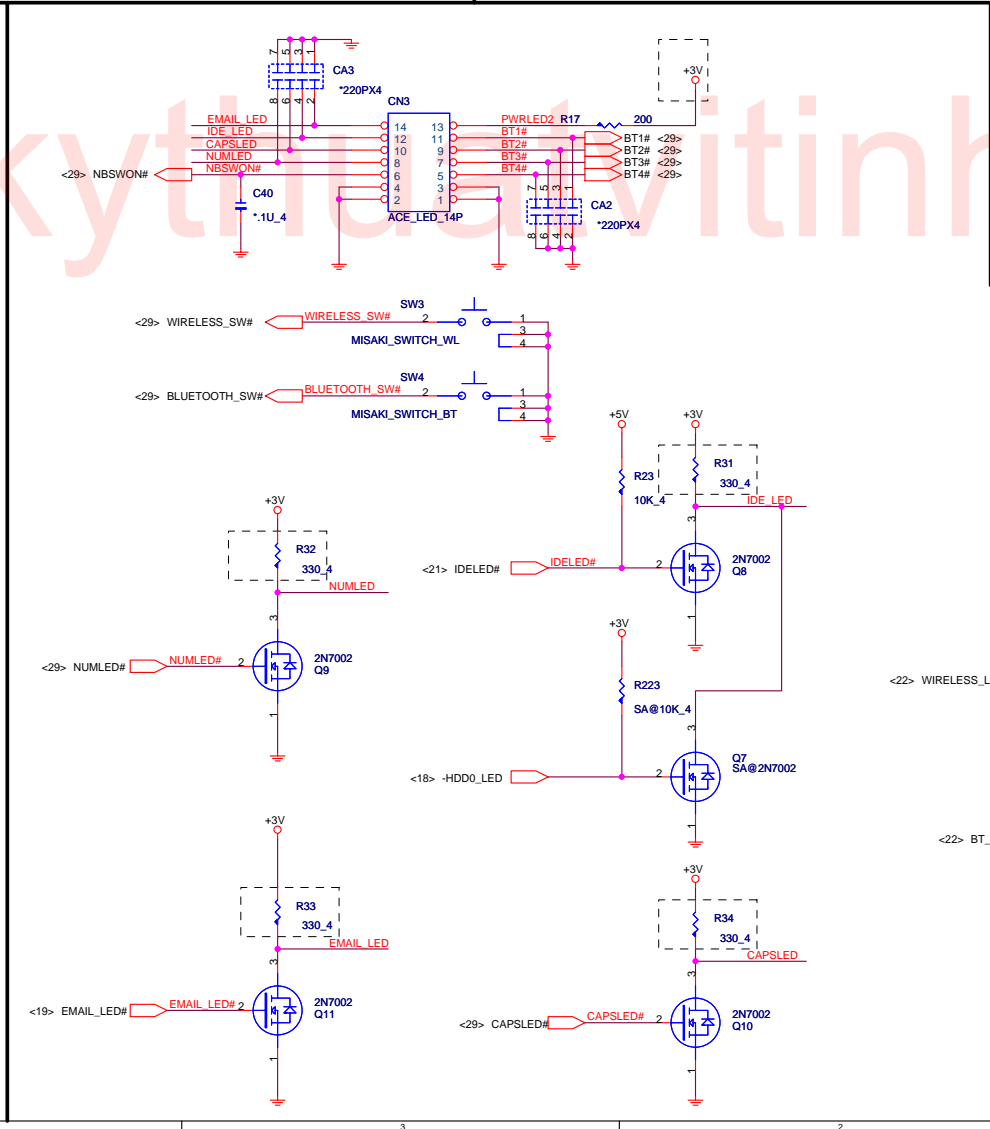
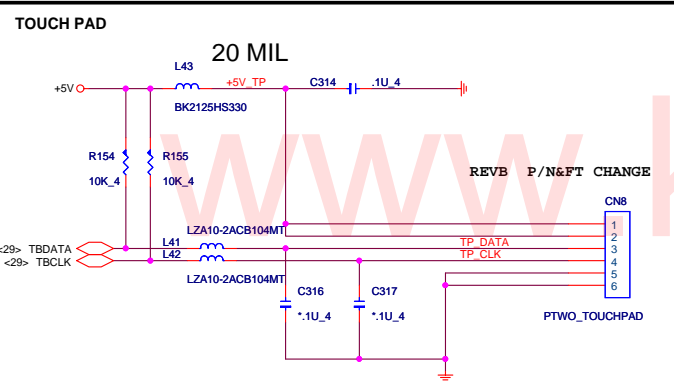
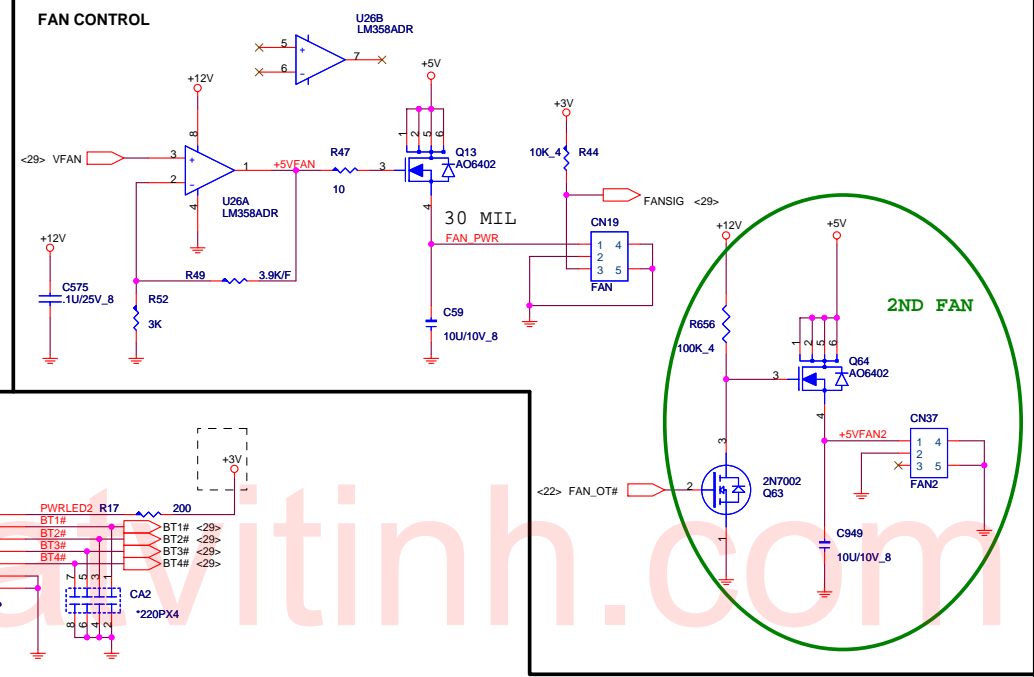
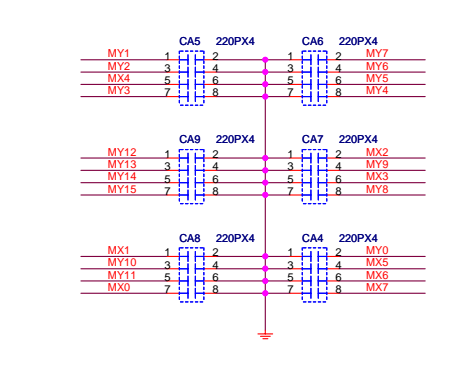
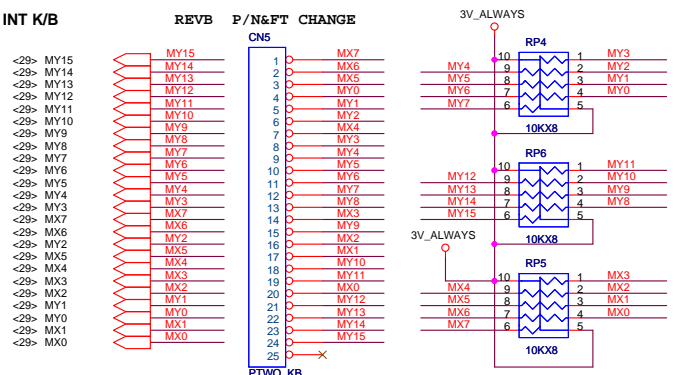
Quanta Computer Inc.

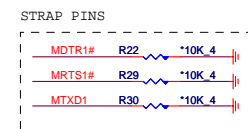
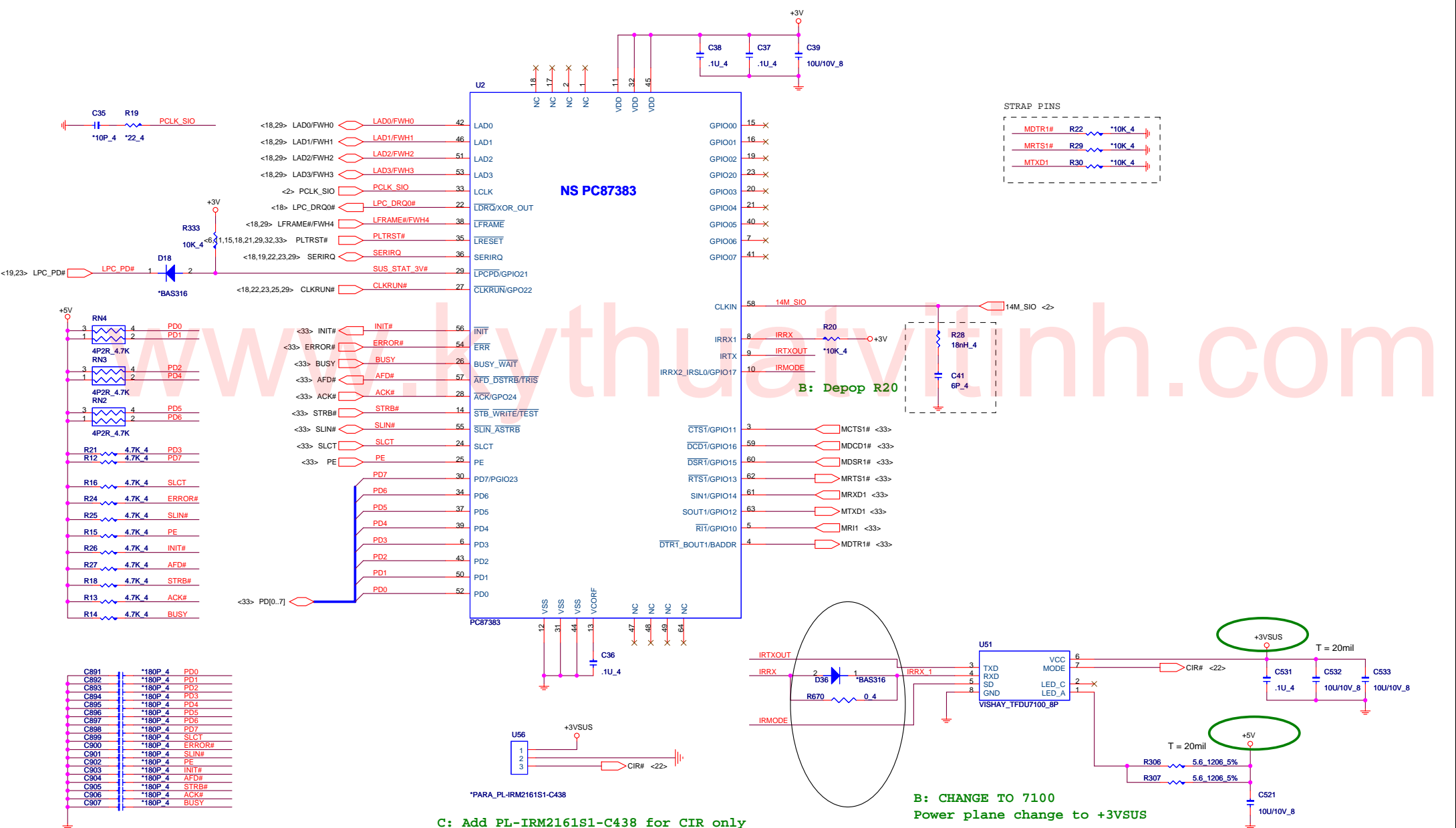
Size	Document Number	Rev
	97551 & FLASH	C
Date:	Thursday, June 23, 2005	Sheet 29 of 40

INTERNAL PULLUP IN SB
<25> LAN_PME#

FOR 97551 ONLY

PLCC32





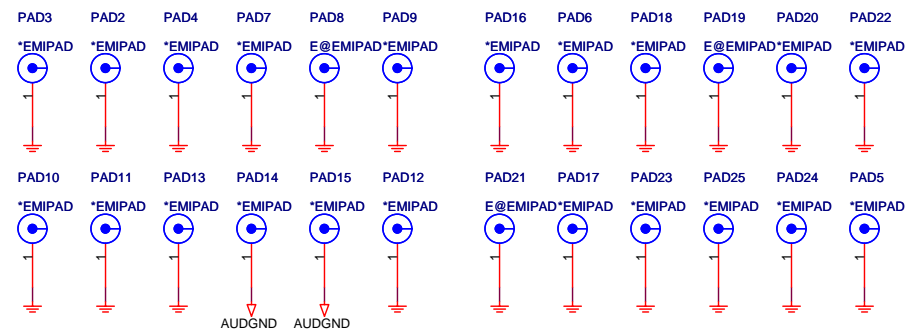
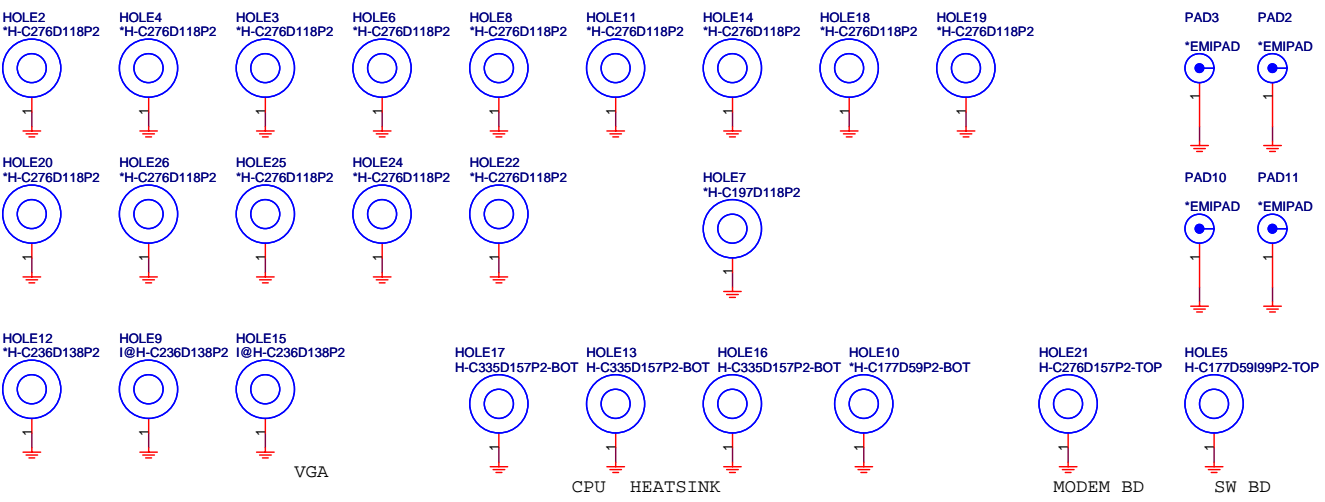
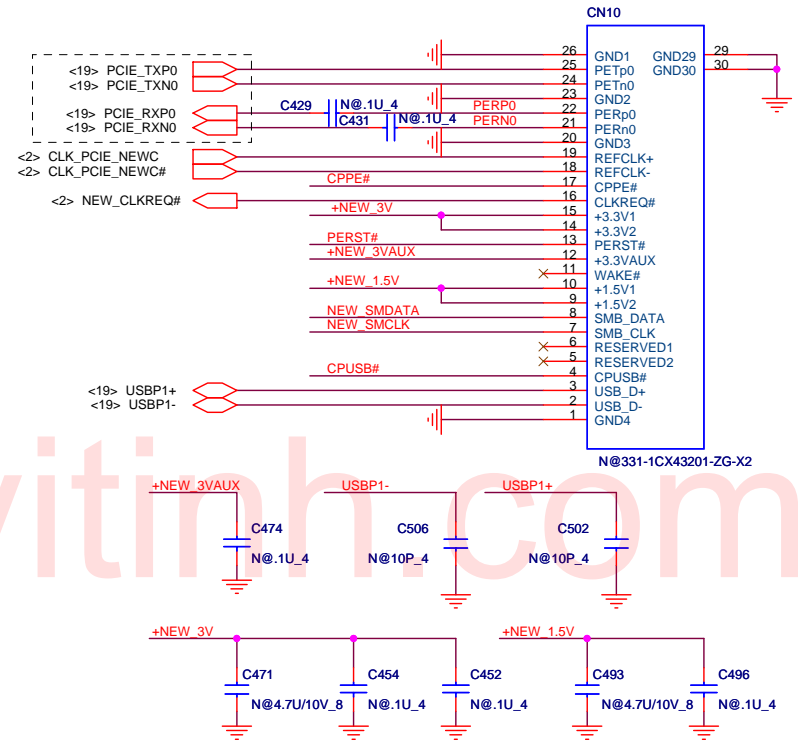
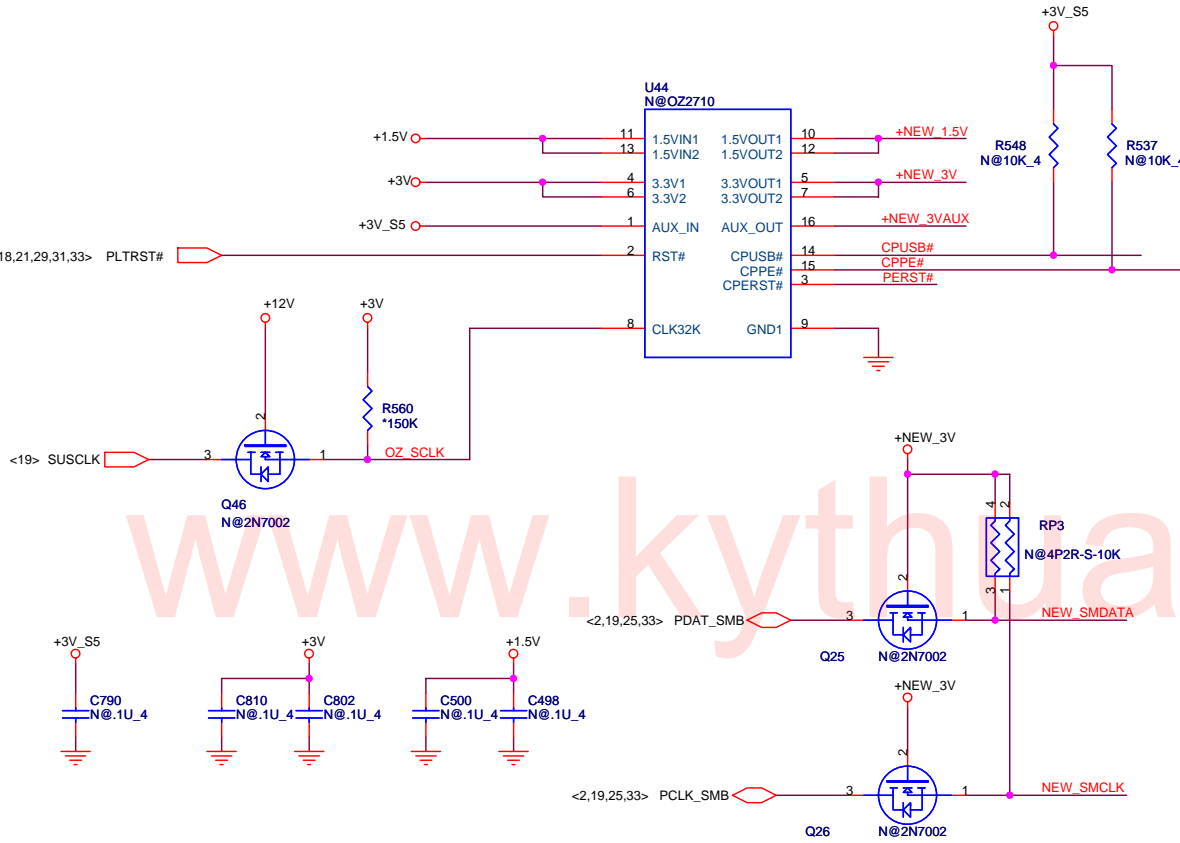
B: Depop R20

B: CHANGE TO 7100
Power plane change to +3VSUS

C: Add PL-IRM2161S1-C438 for CIR only

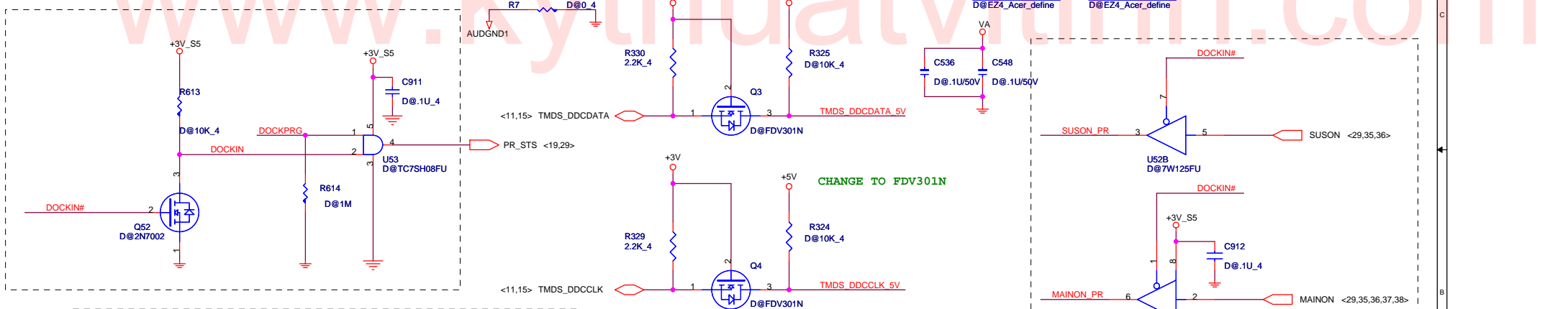
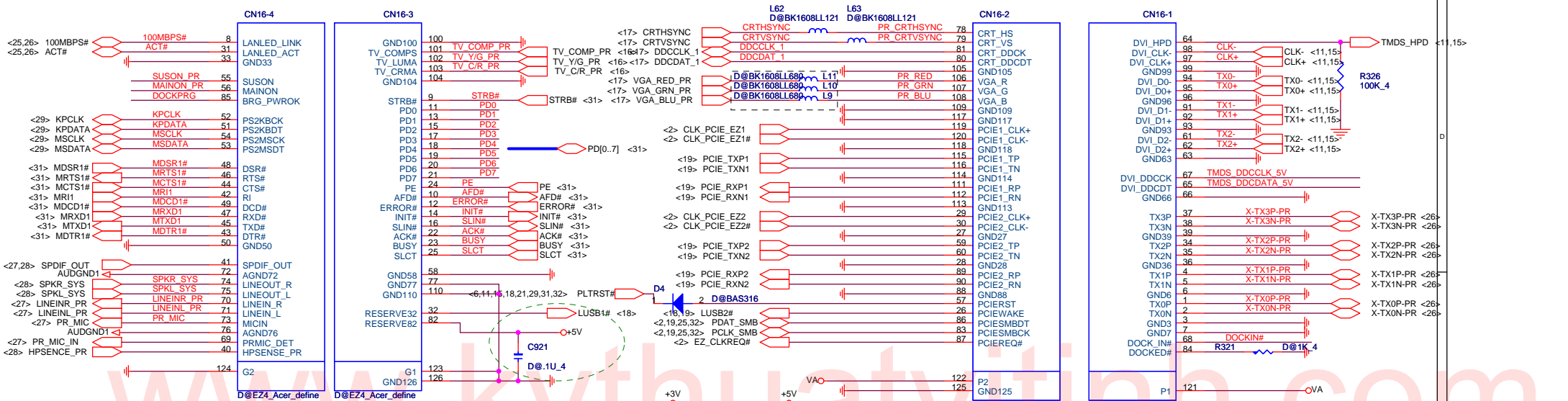
PROJECT : ZL7
Quanta Computer Inc.

Size	Document Number	Rev
	EZ PORT & SIO (87383) & CIR	C
Date:	Thursday, June 30, 2005	Sheet 31 of 40

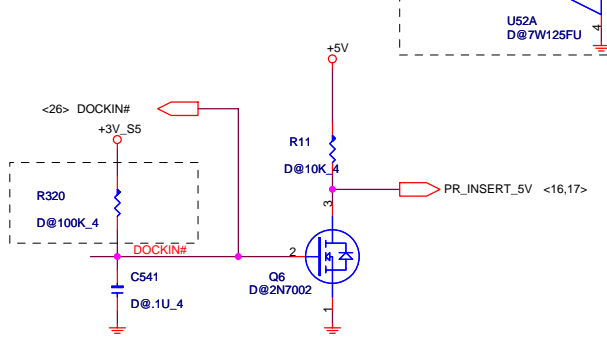



PROJECT : ZL7
Quanta Computer Inc.

Size	Document Number	Rev
	EZ PORT & SIO (87383)	C
Date:	Thursday, June 23, 2005	Sheet 32 of 40

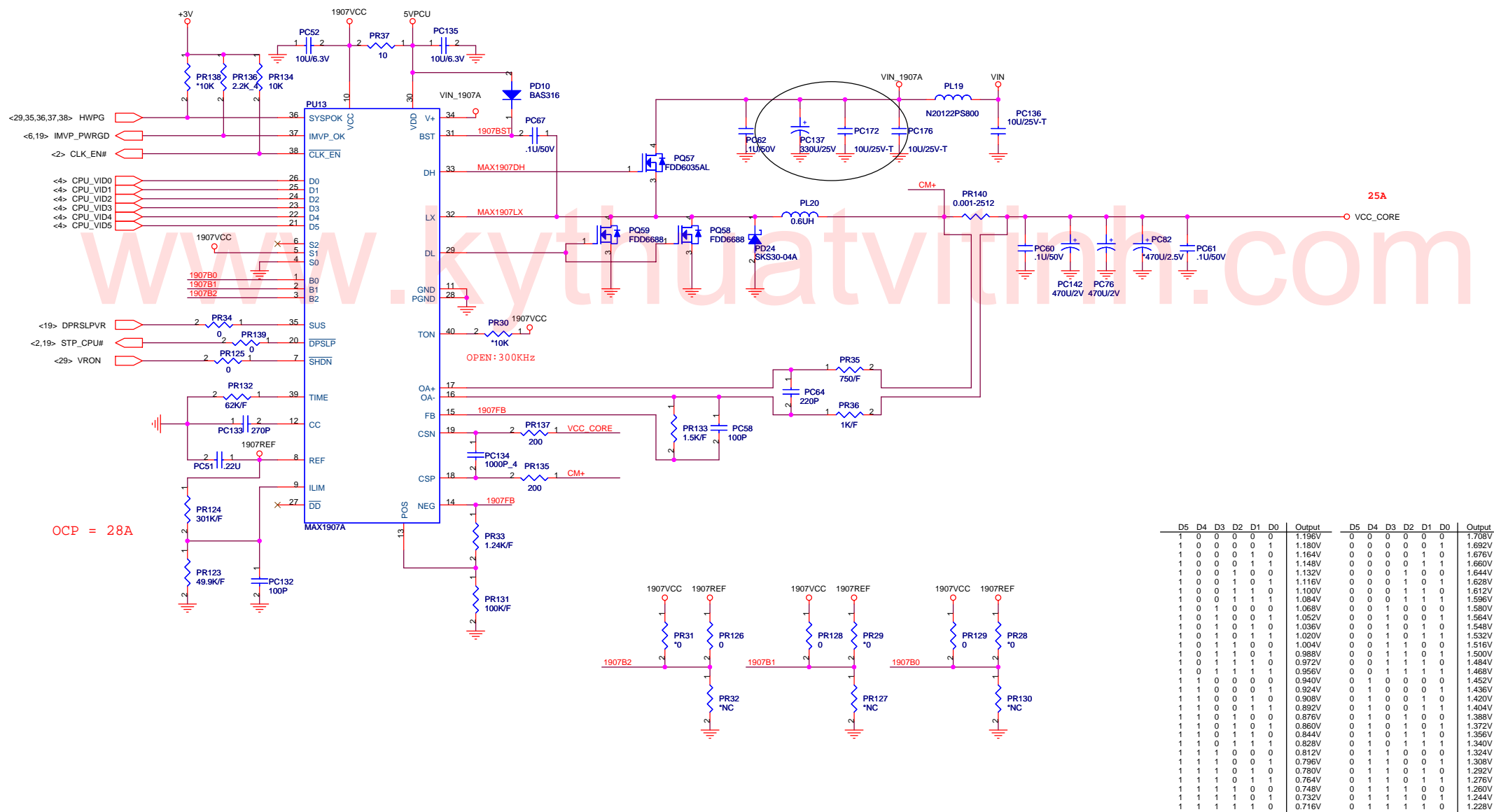


SPKL_SYS	C543	D@220P_4	PR CRTHSYNC	C544	*10P_4
SPKR_SYS	C542	D@220P_4	PR CRTVSYNC	C545	*10P_4
LINEINL_PR	C27	D@220P_4	PR BLU	C24	D@10P_4
LINEINR_PR	C28	D@220P_4	PR GRN	C25	D@10P_4
PR MIC_IN	C13	D@47P_4	PR RED	C26	D@10P_4
PR MIC	C23	D@47P_4	CRTVSYNC	C549	*10P_4
100MBPS#	C14	D@1000P_4	CRTVSYNC	C550	*10P_4
ACT#	C17	D@1000P_4	DDCCLK_1	C547	D@10P_4
TV_COMP_PR	C20	D@10P_4	DDCDAT_1	C546	D@10P_4
TV_C/R_PR	C22	D@10P_4	X-TX1P-PR	C16	D@10P_4
TV_Y/G_PR	C21	D@10P_4	X-TX1N-PR	C15	D@10P_4
			X-TX0P-PR	C18	D@10P_4
			X-TX0N-PR	C19	D@10P_4
			X-TX3P-PR	C539	D@10P_4
			X-TX3N-PR	C540	D@10P_4
			X-TX2P-PR	C537	D@10P_4
			X-TX2N-PR	C538	D@10P_4




PROJECT : ZL7
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Size	Document Number	Rev
	EZ PORT & SIO (87383)	C
Date:	Thursday, June 23, 2005	Sheet 33 of 40



OCP = 28A


SUSPEND MODE (SUS=HIGH)

S2	S1	S0	Output
✓ OPEN	VCC	GND	0.748V

VCC_BOOT

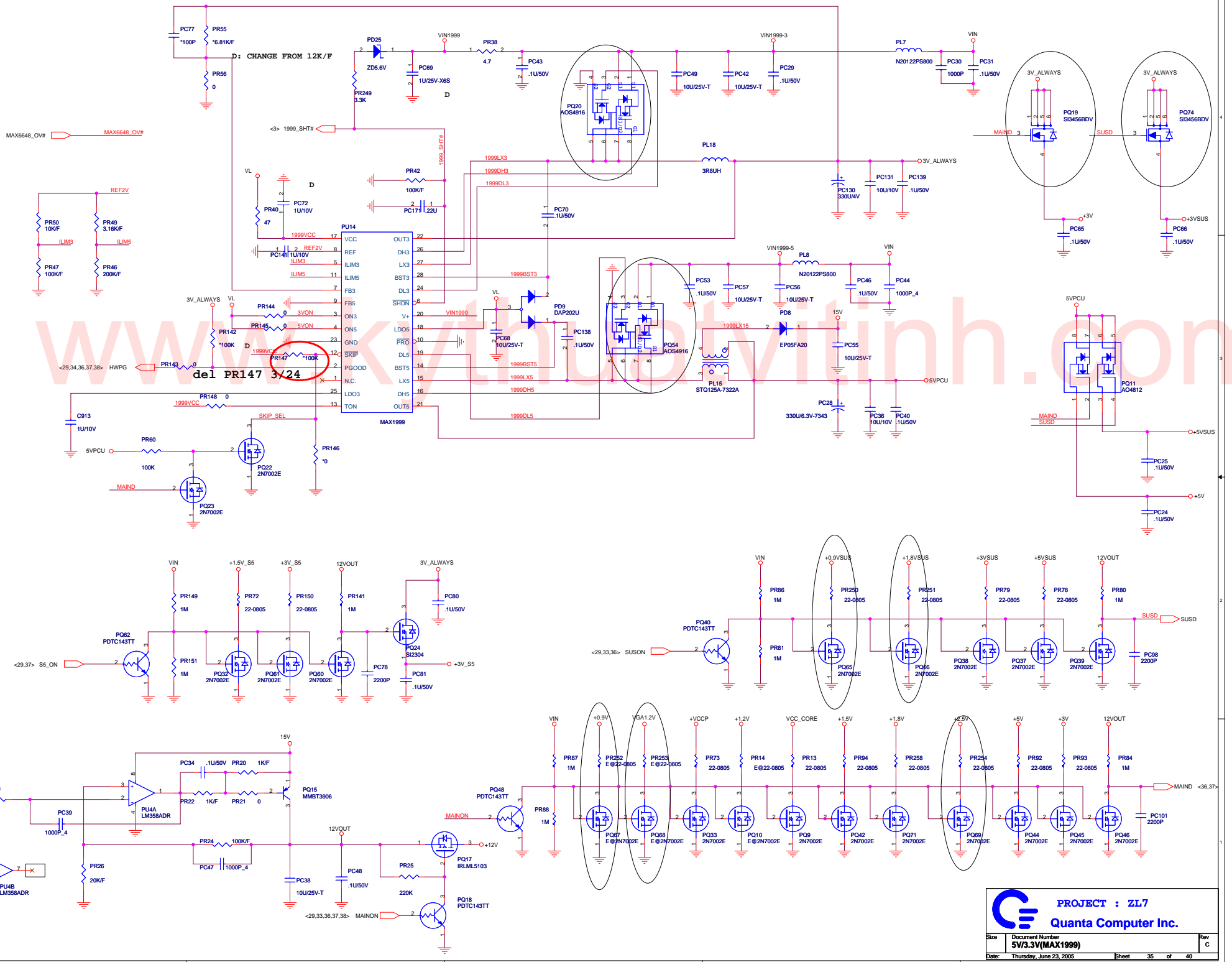
B2	B1	B0	Output
GND	GND	GND	1.708V
REF	REF	REF	1.372V
OPEN	OPEN	OPEN	1.036V
VCC	VCC	VCC	0.700V
✓ REF	VCC	VCC	1.212V

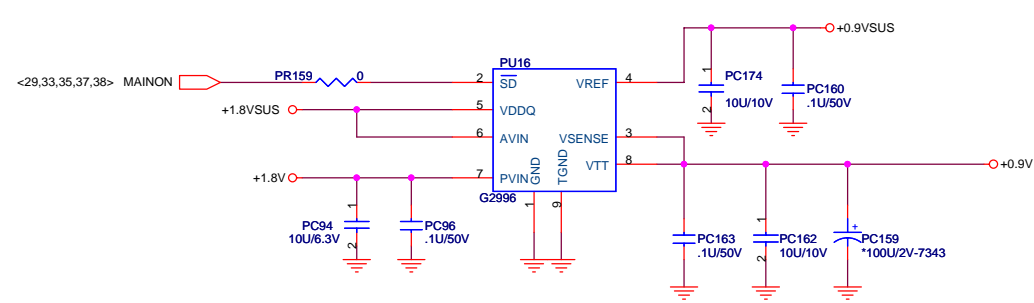
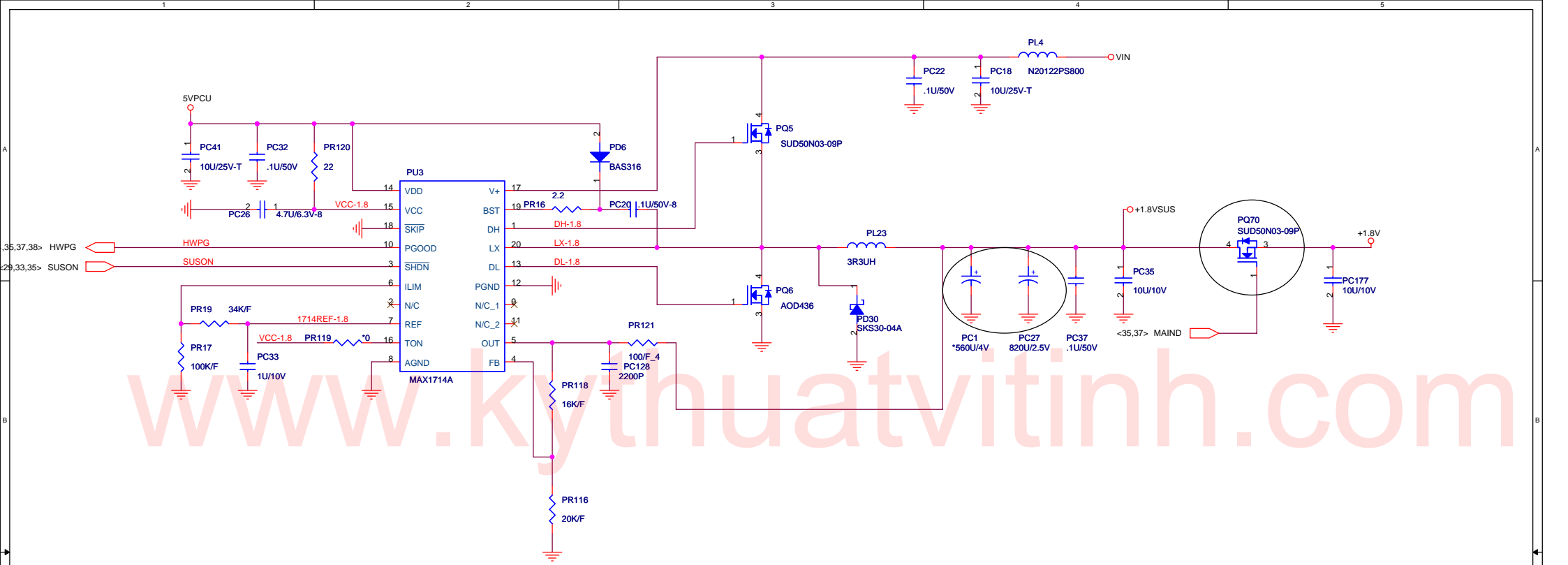
D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	0	1	1.628V
1	0	0	1	1	0	1.100V	0	0	0	1	1	0	1.612V
1	0	0	1	1	1	1.084V	0	0	0	1	1	1	1.596V
1	0	1	0	0	0	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	0	1	1.052V	0	0	1	0	0	1	1.564V
1	0	1	0	1	0	1.036V	0	0	1	0	1	0	1.548V
1	0	1	0	1	1	1.020V	0	0	1	0	1	1	1.532V
1	0	1	1	0	0	1.004V	0	0	1	1	0	0	1.516V
1	0	1	1	0	1	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	0	0.972V	0	0	1	1	1	0	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	1	0	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	0	1.420V
1	1	0	0	1	1	0.892V	0	1	0	0	1	1	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	0	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	0	1	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	1	0	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V



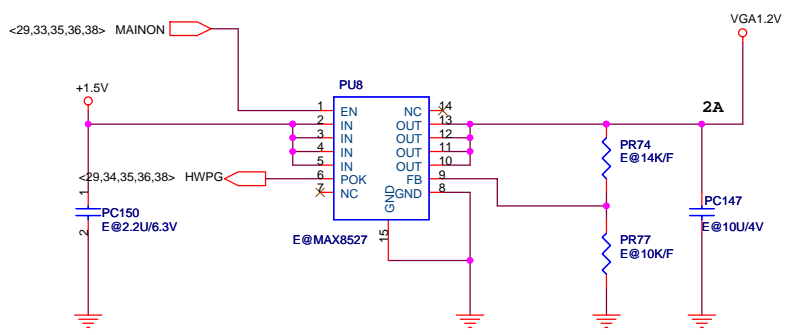
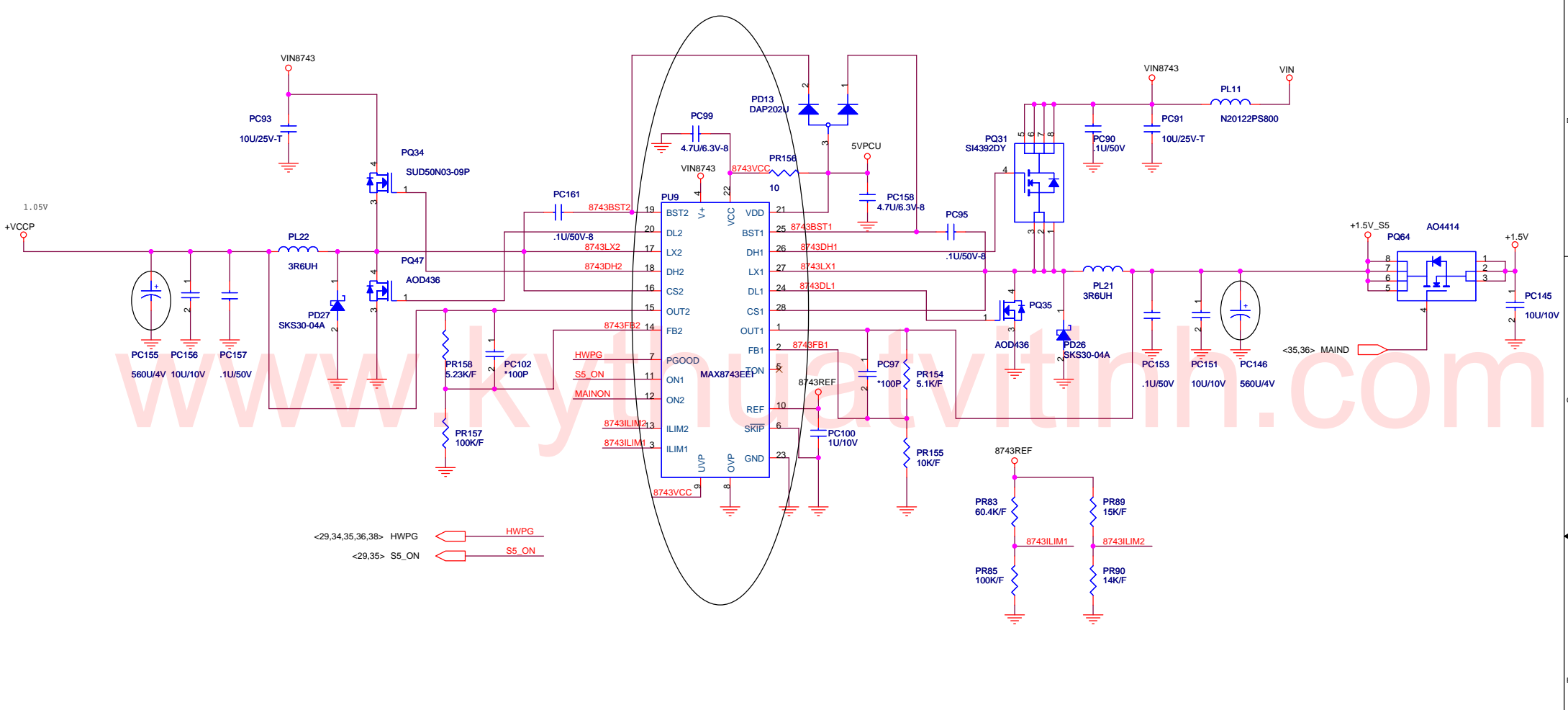
PROJECT : ZL7
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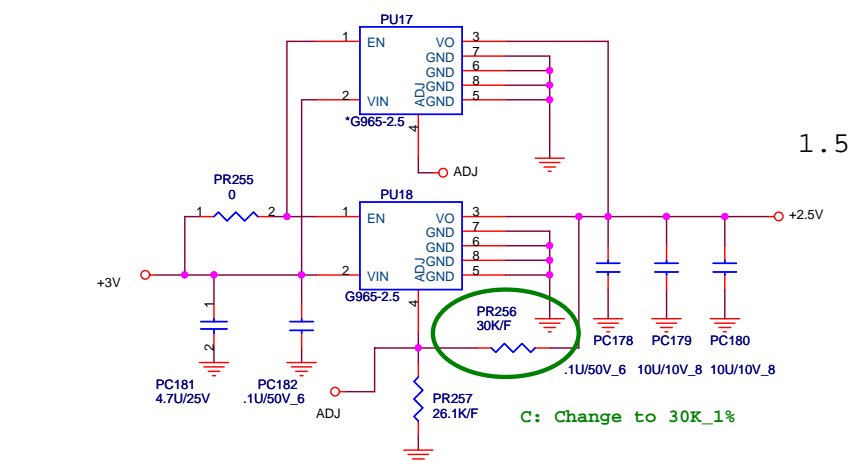
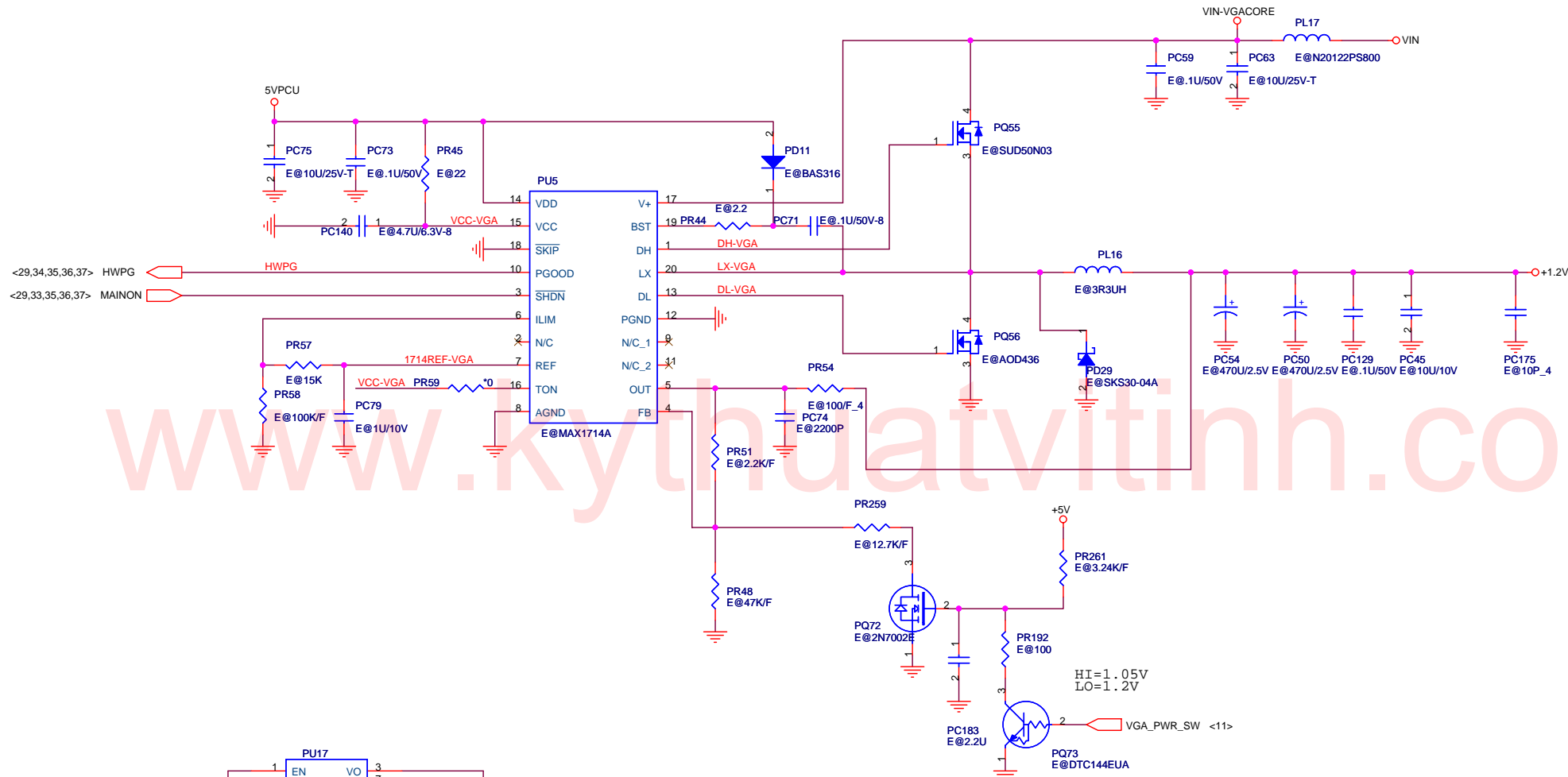
Size	Document Number CPU CORE (MAX1907)	Rev C
Date:	Thursday, June 23, 2005	Sheet 34 of 40





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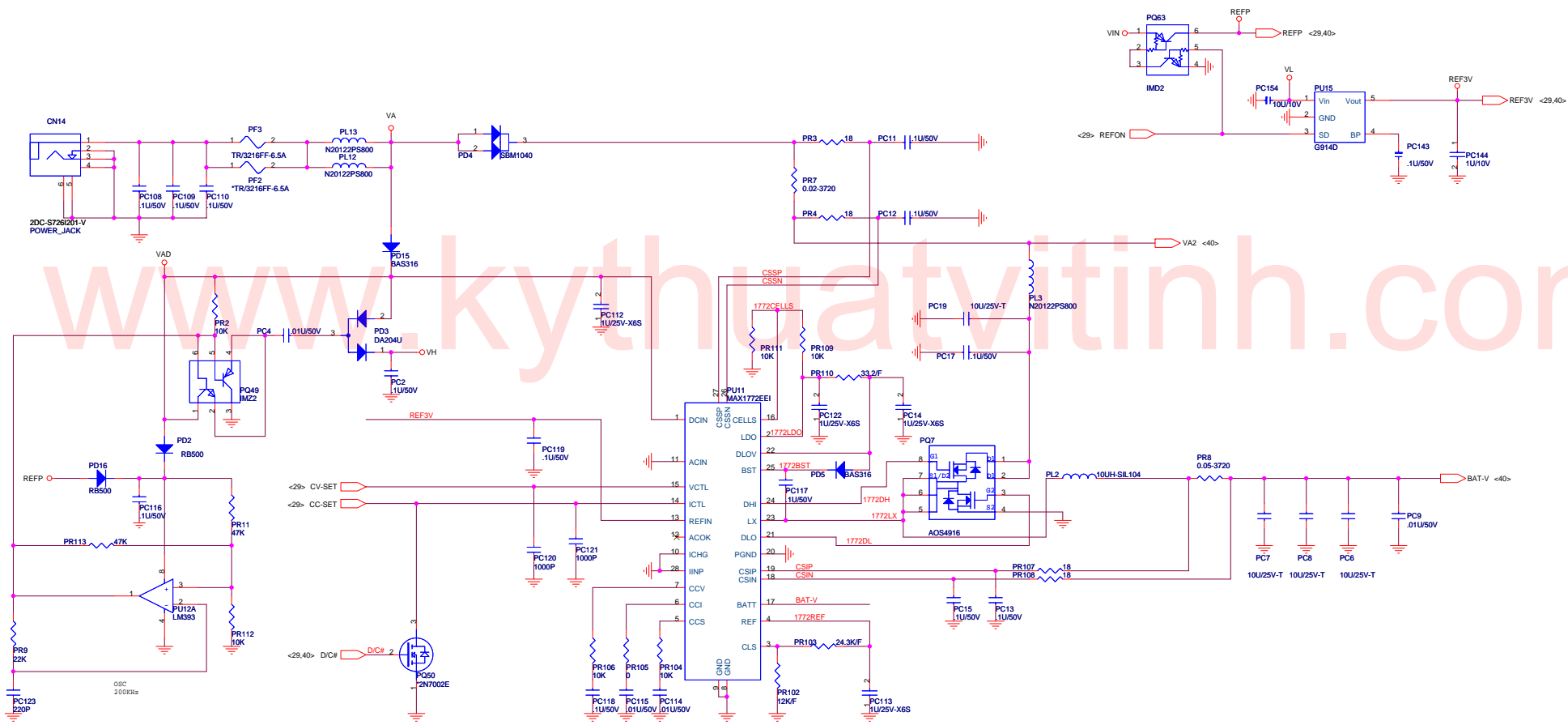




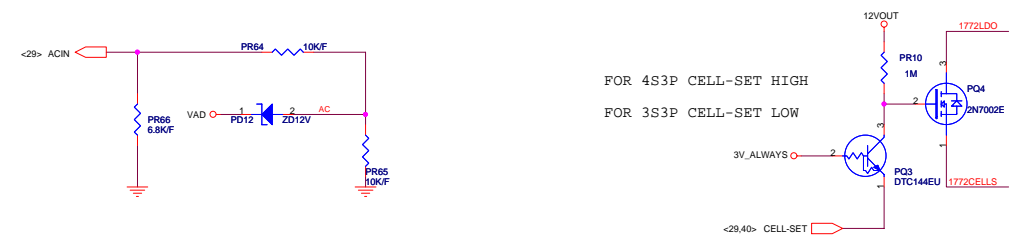
1.5 / 3A

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Size	Document Number	Rev
	+1.2V/+1.8V	C
Date:	Thursday, June 23, 2005	Sheet 38 of 40

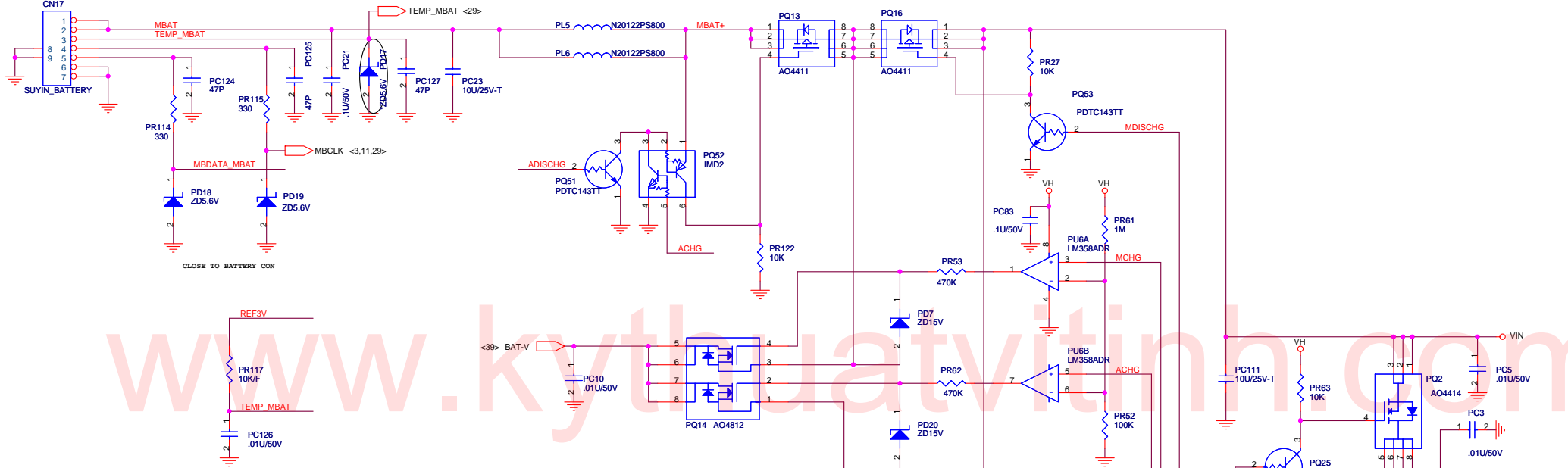


FOR 120W 6.2A

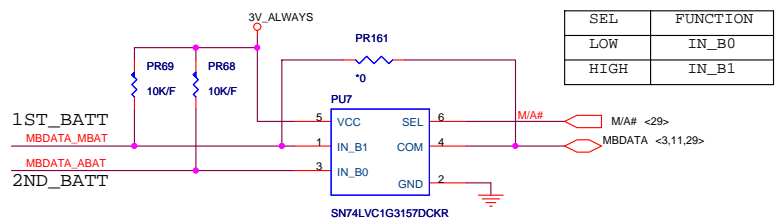
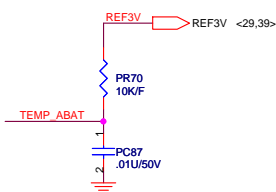
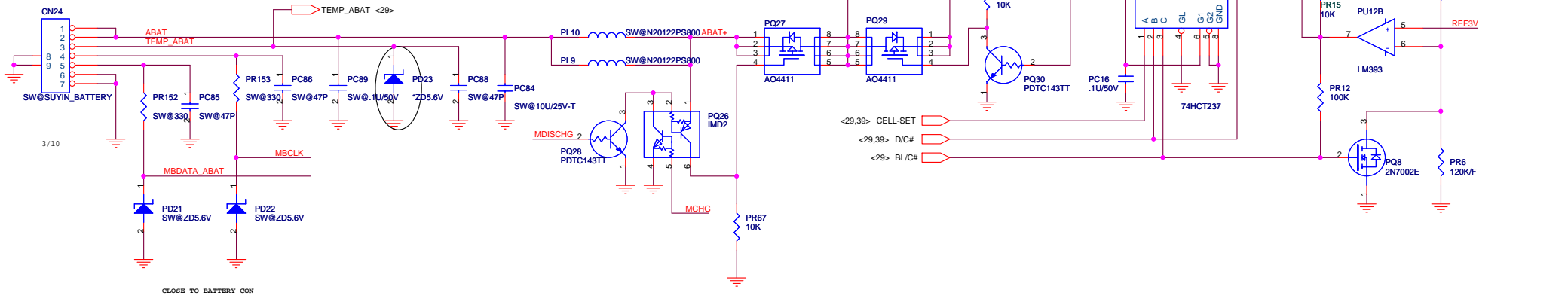


FOR 4S3P CELL-SET HIGH
FOR 3S3P CELL-SET LOW

1ST_BATT_CONN



2ND_BATT_CONN



SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

PROJECT : ZL7
Quanta Computer Inc.

Size: Document Number
BATTERY SELECT

Date: Thursday, June 23, 2005 Sheet 40 of 40