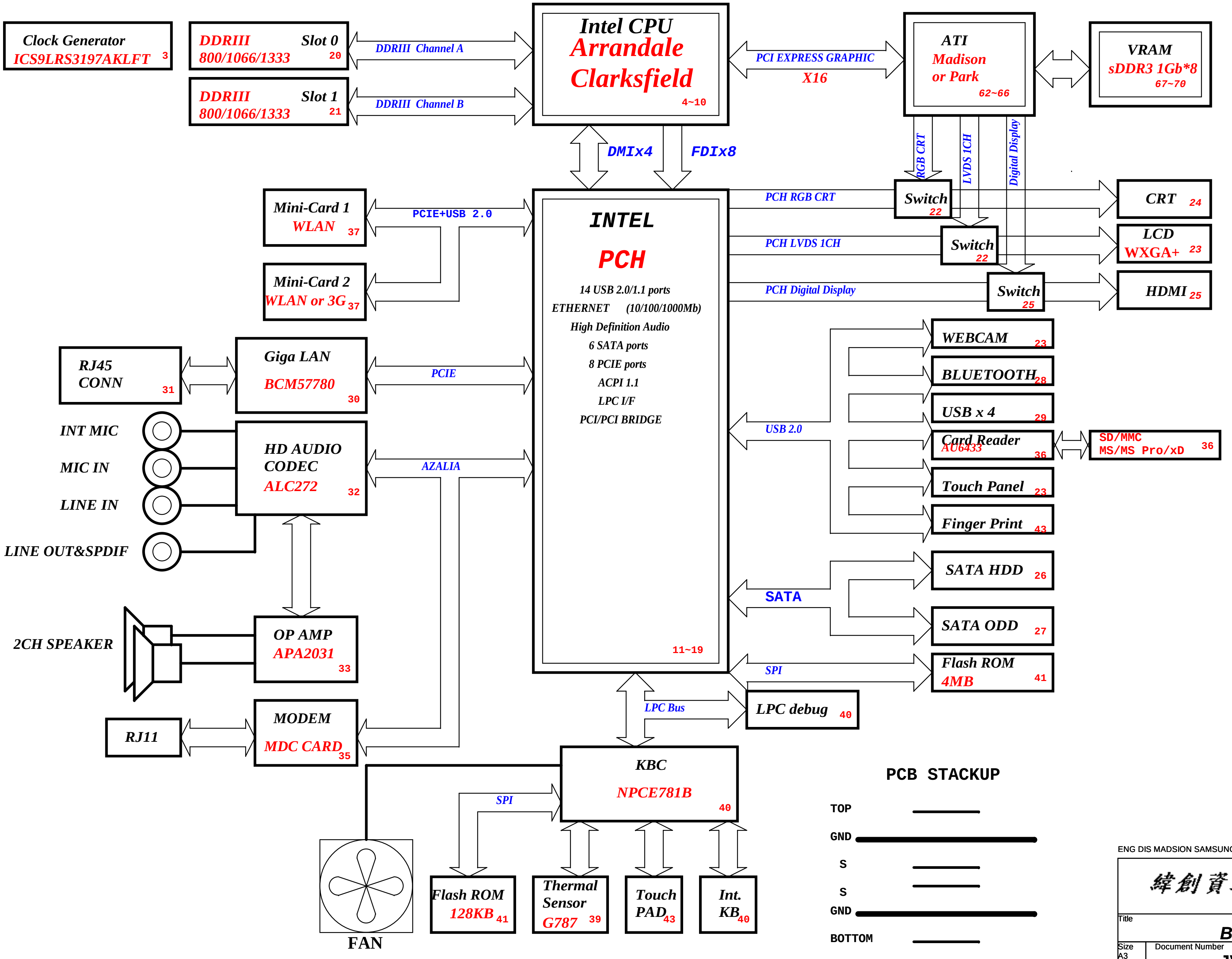
JV50-CP Block Diagram

Project code: 91.4GD01.001
PCB P/N : 48.4GD01.0SB
REVISION : SB 09285



INPUTS	OUTPUTS
CPU DC/DC ISL62882	
DCBATOUT	VCC_CORE 47,48
SYSTEM DC/DC TPS51123	
DCBATOUT	5V_S5 3D3V_S5 49
SYSTEM DC/DC TPS51117	
DCBATOUT	1D5V_S3 50
SYSTEM DC/DC TPS51117	
DCBATOUT	1D05V_S0 50
SYSTEM DC/DC TPS51117	
DCBATOUT	1D05V_VTT 51
RT9025	
3D3V_S0	1D8V_S0 50
G2997	
1D5V_S3	0D75_S0 52
SYSTEM DC/DC ISL62881	
DCBATOUT	VCC_GFXCORE 54
SYSTEM DC/DC TPS51117	
DCBATOUT	+VGA_CORE 55
CHARGER ISL88731A	
DCBATOUT	BT+ 53

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Title
Block Diagram

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE1	**LAN**
LANE2	**MiniCard1**
LANE3	**MiniCard2**

USB Table

Pair	*Device*
0	*USB3*
1	*USB2*
2	*USB4*
3	*MINICARD1*
4	*WECAM*
5	*Touch Panel*
6	*NC*
7	*NC*
8	*NC*
9	*USB1(HS)*
10	*Finger Print*
11	*Blue Tooth*
12	*MINIC2*
13	*Cardreader*

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Title
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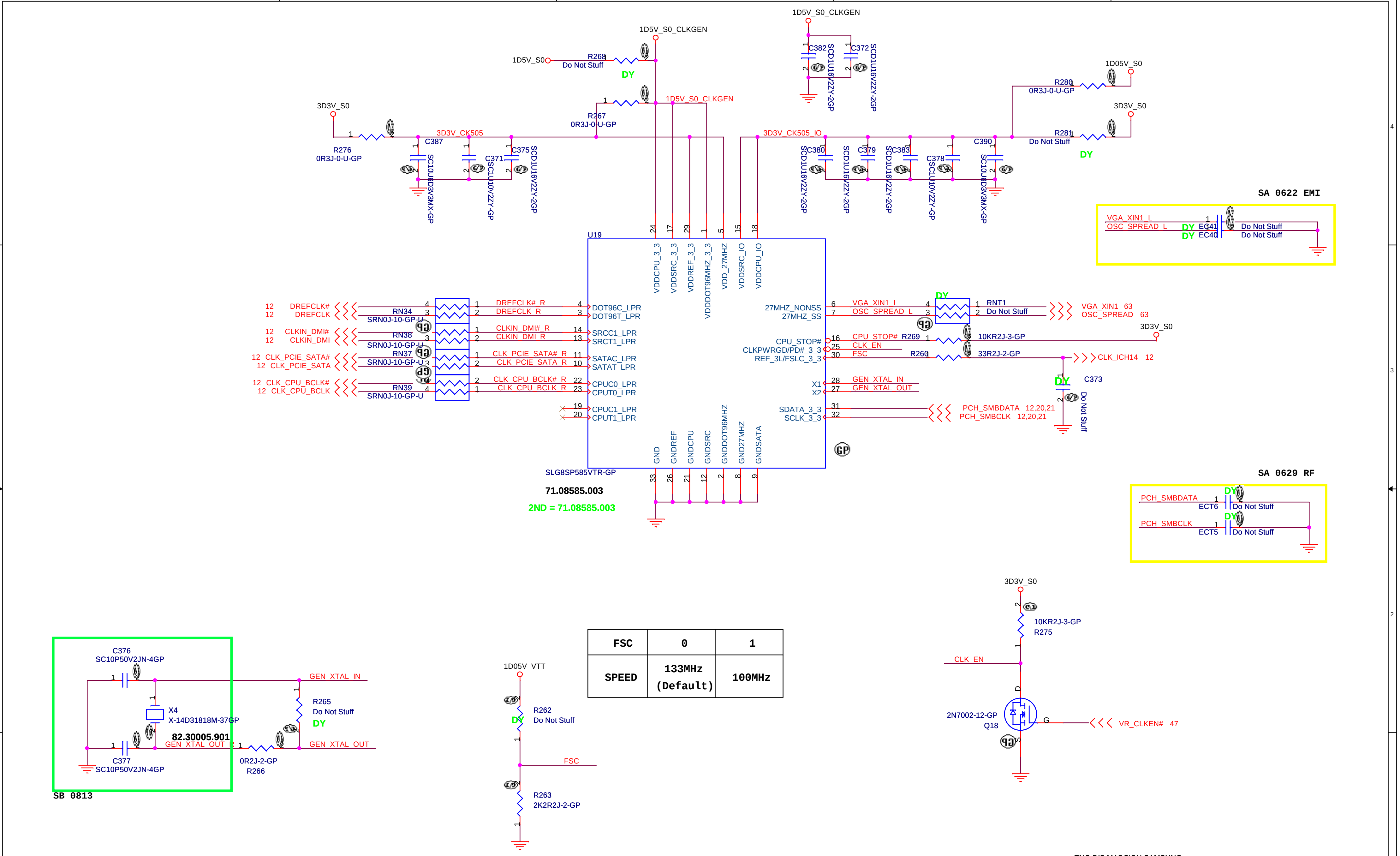

FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title
Clock Generator

Size A3
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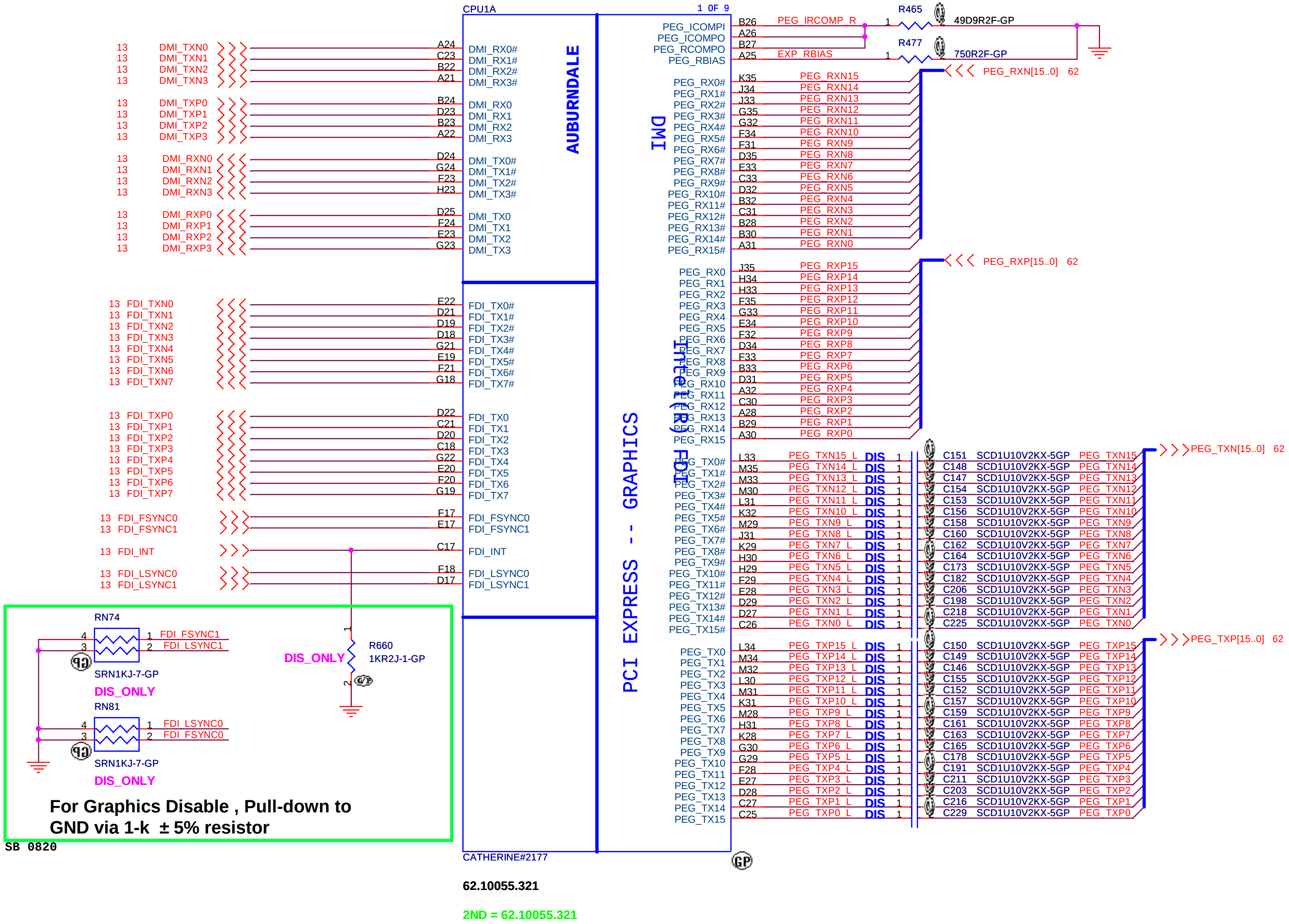

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Title	CPU (1/7)	
Size A3	Document Number JV50-CP	Rev SA
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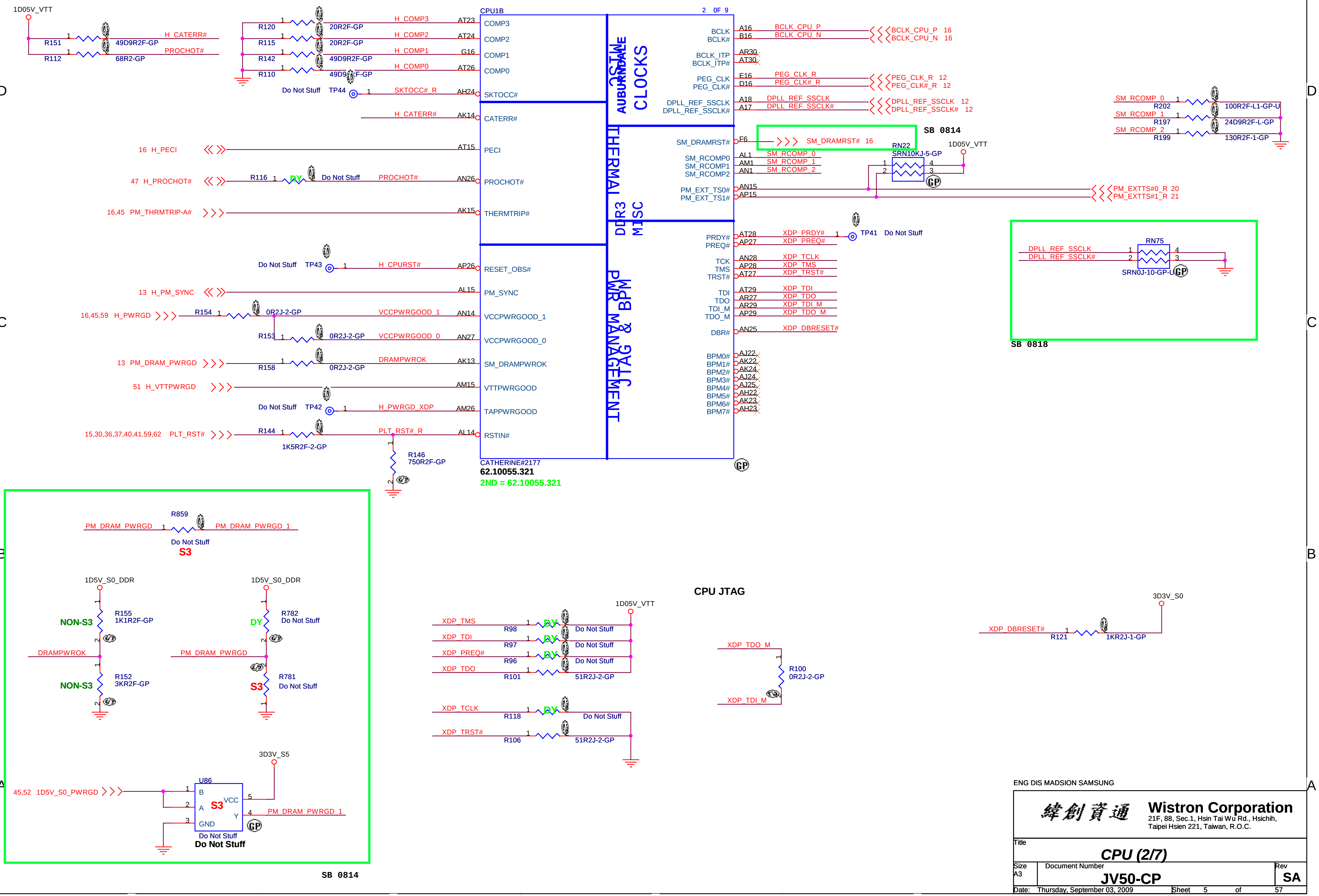

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Title
CPU (2/7)

Size	Document Number	Rev
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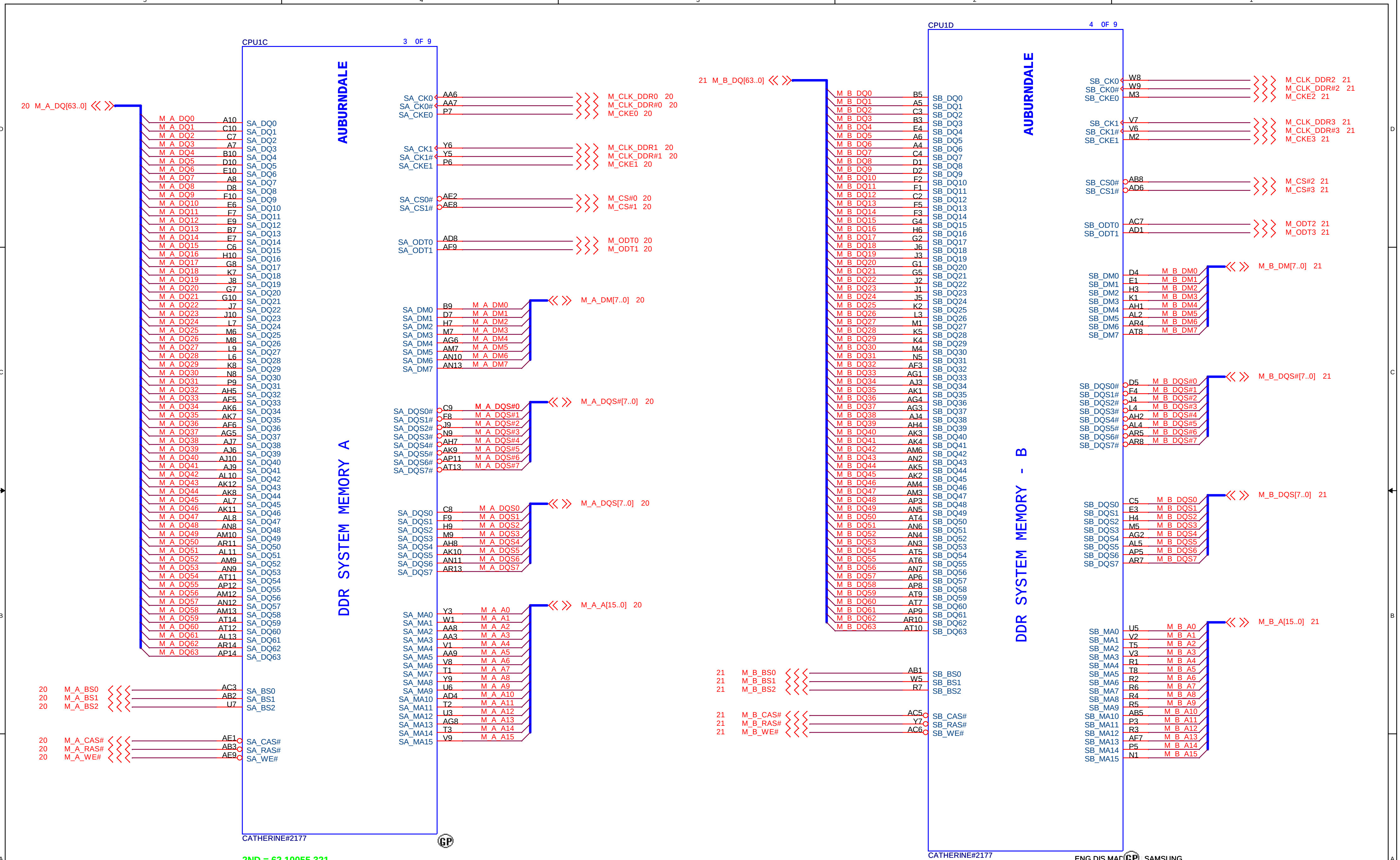

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Title	CPU (3/7)
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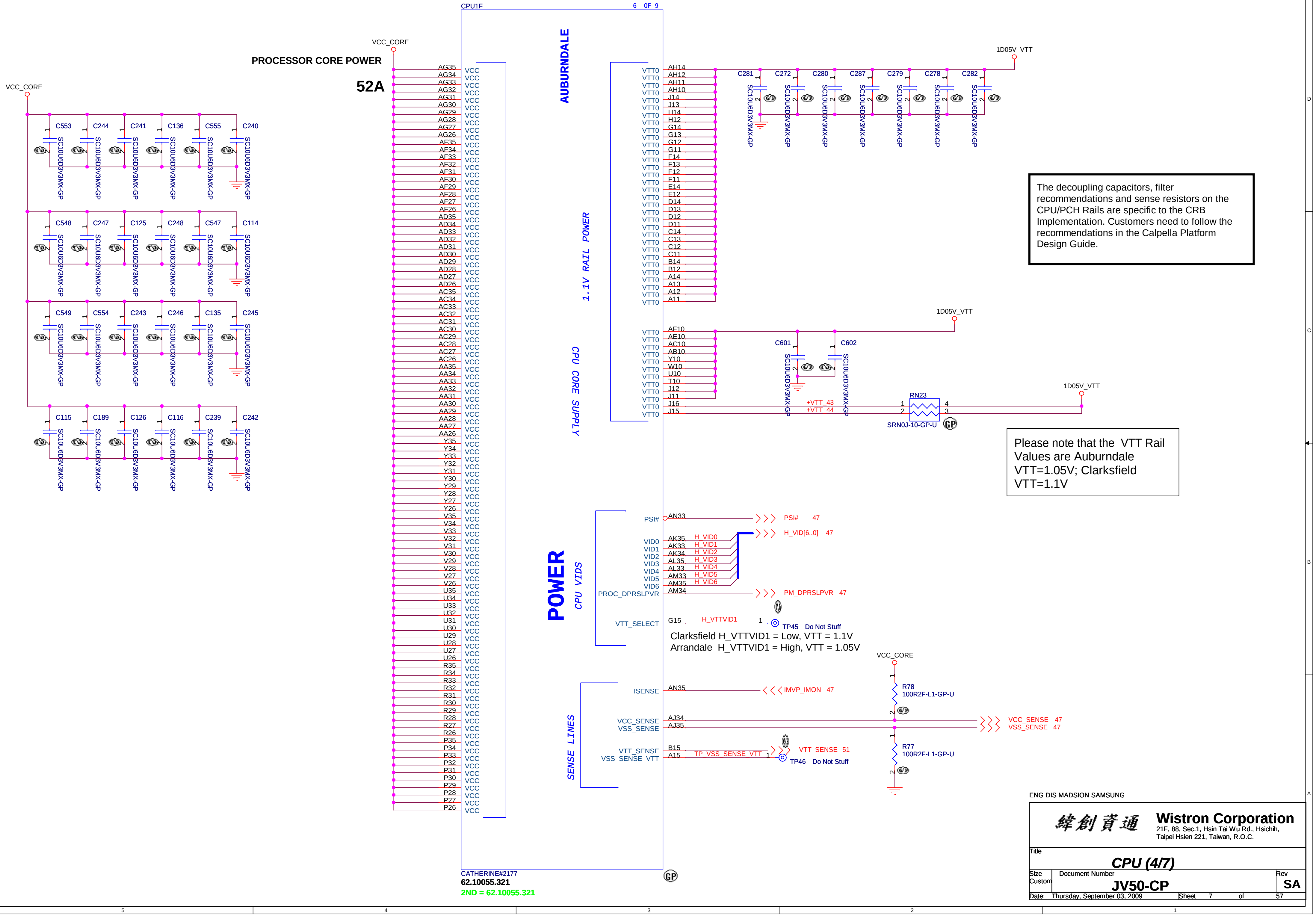

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V

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Title
CPU (4/7)

Size Custom
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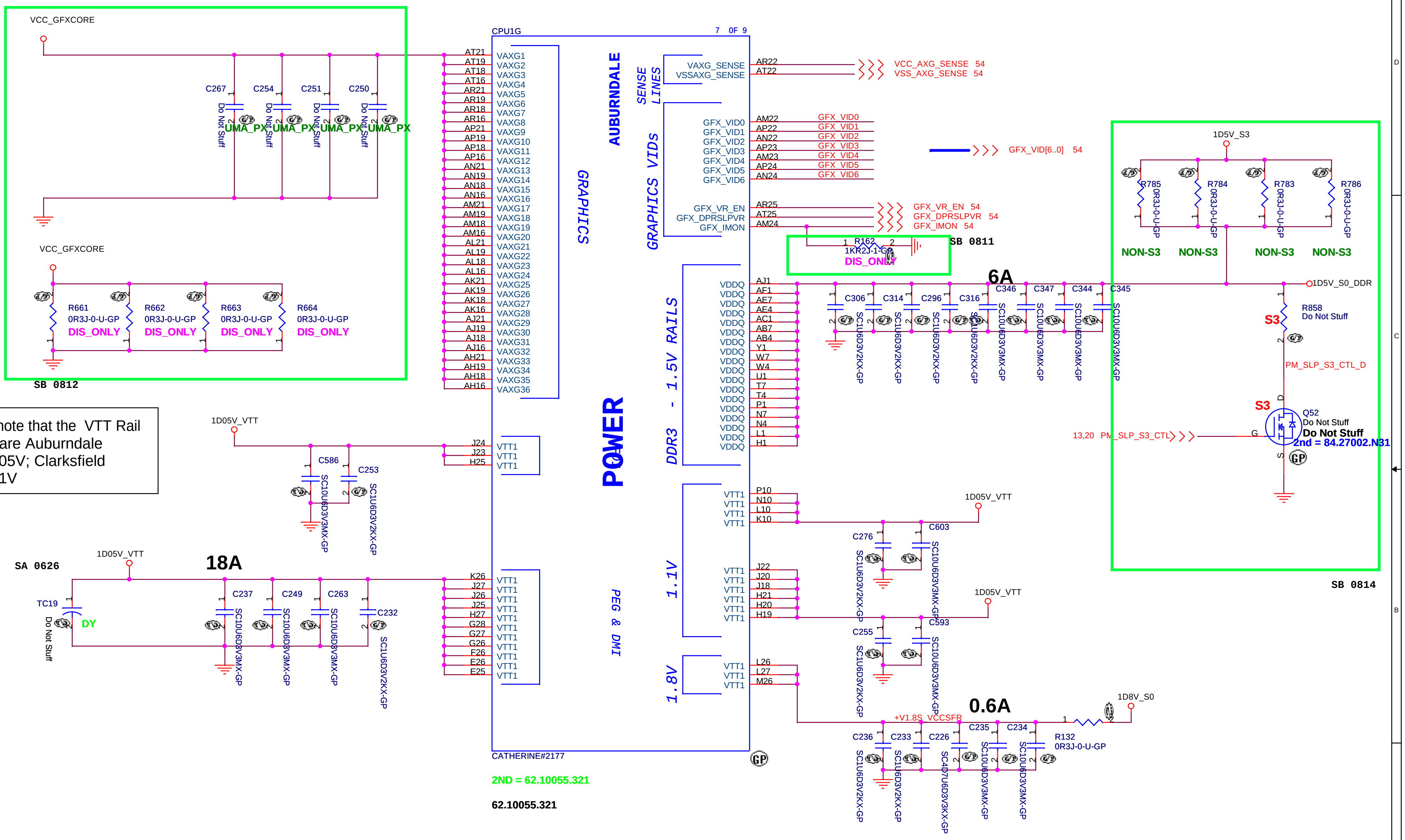

Please note that the VTT Rail
Values are Auburndale
VTT=1.05V; Clarksfield
VTT=1.1V

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Title		
	CPU (5/7)	
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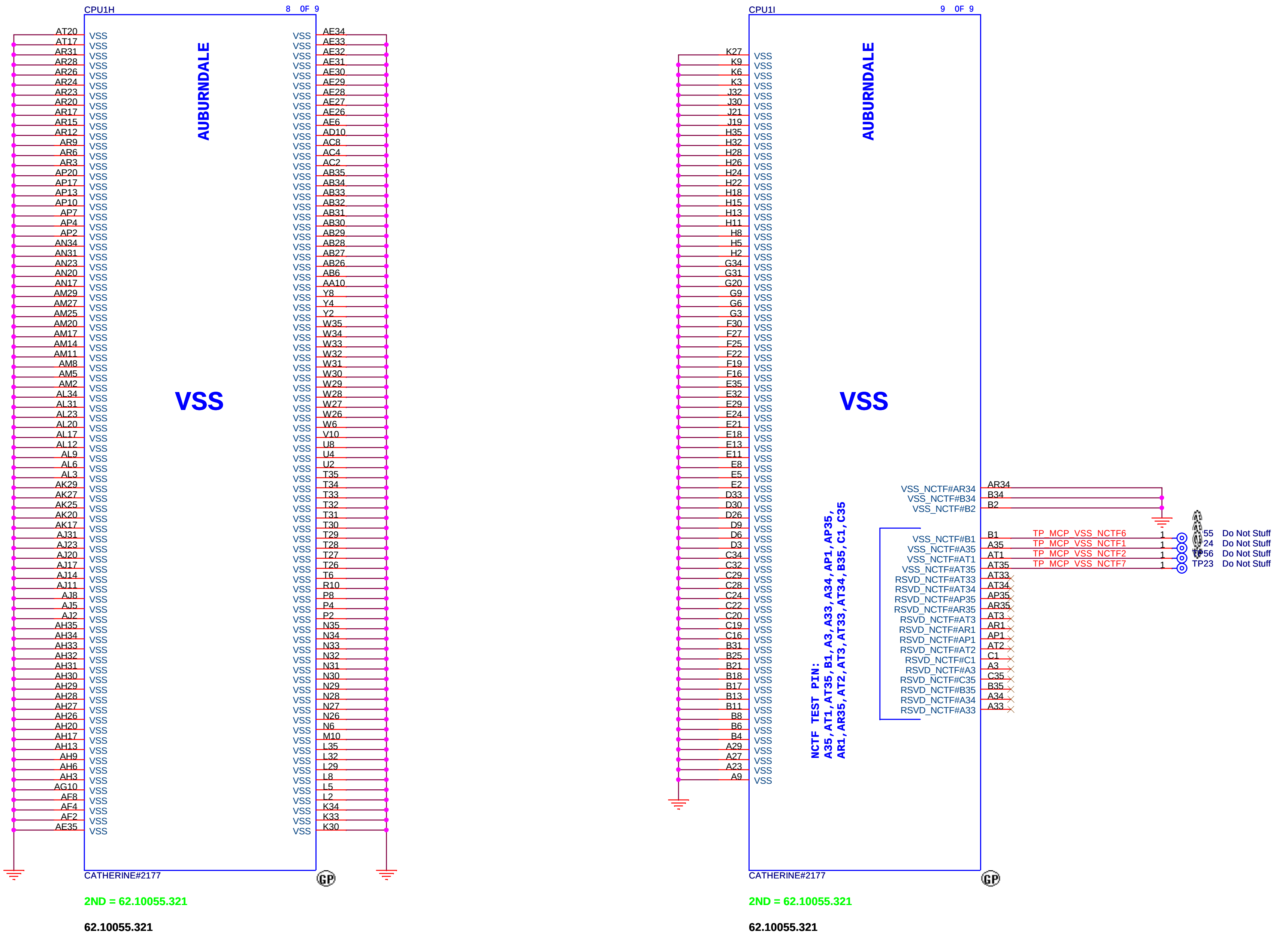

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Title		
CPU (6/7)		
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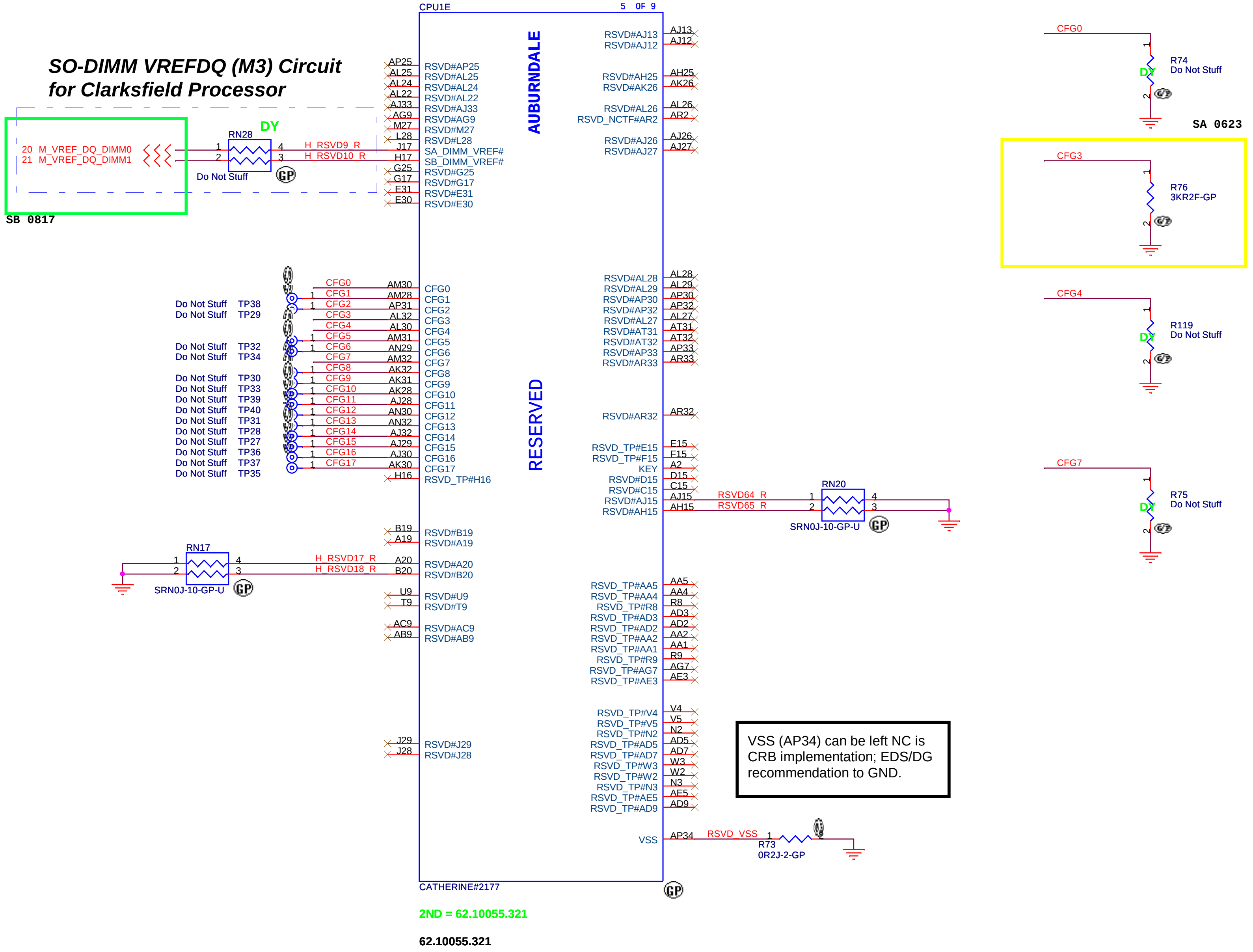
SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

2ND = 62.10055.321

62.10055.321

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [for details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

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Title
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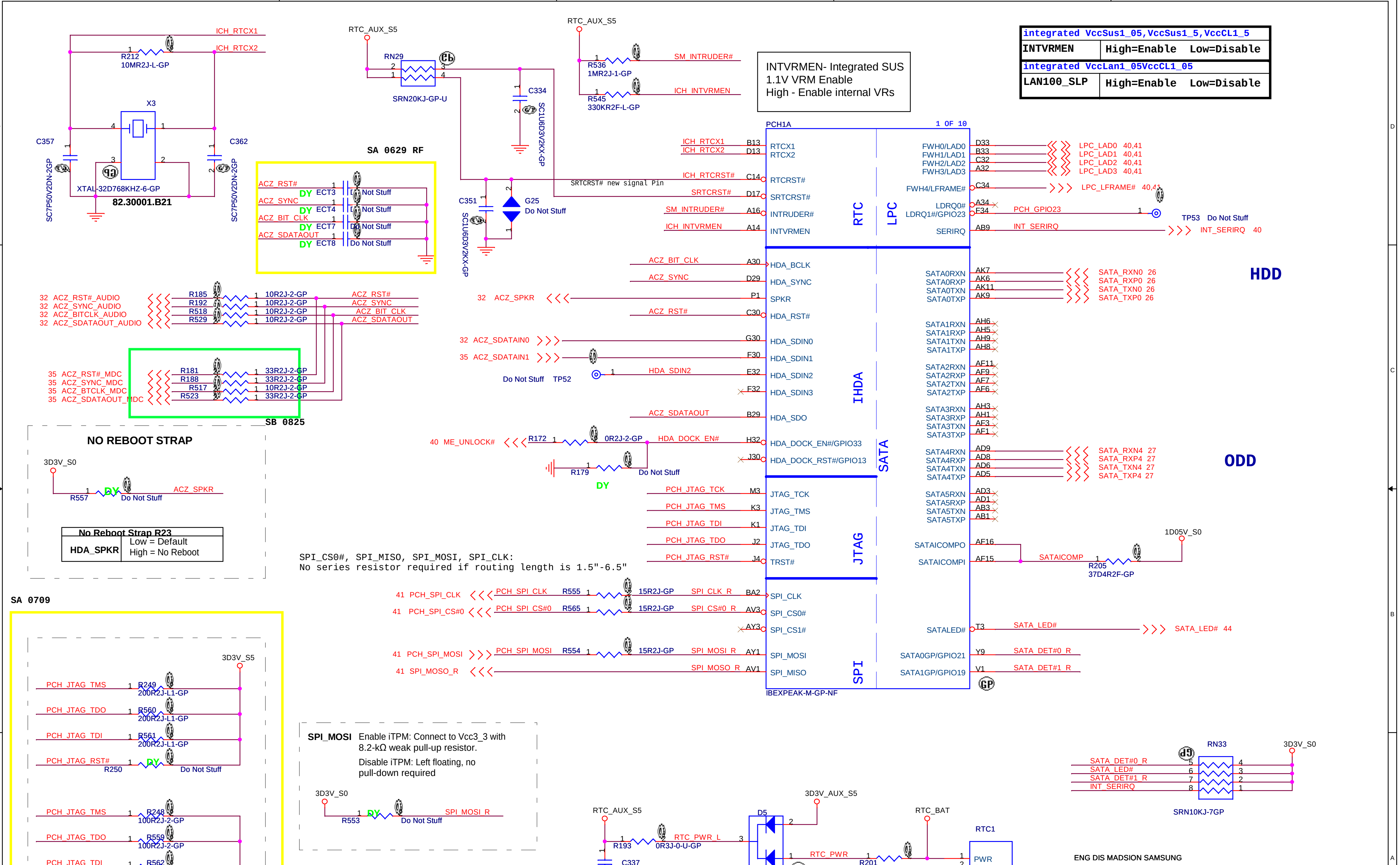

integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

INTVRMEN- Integrated SUS
1.1V VRM Enable
High - Enable internal VRs

NO REBOOT STRAP

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"

When unused all JTAG pins may be NC

SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required

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Title: **PCH (1/9)**

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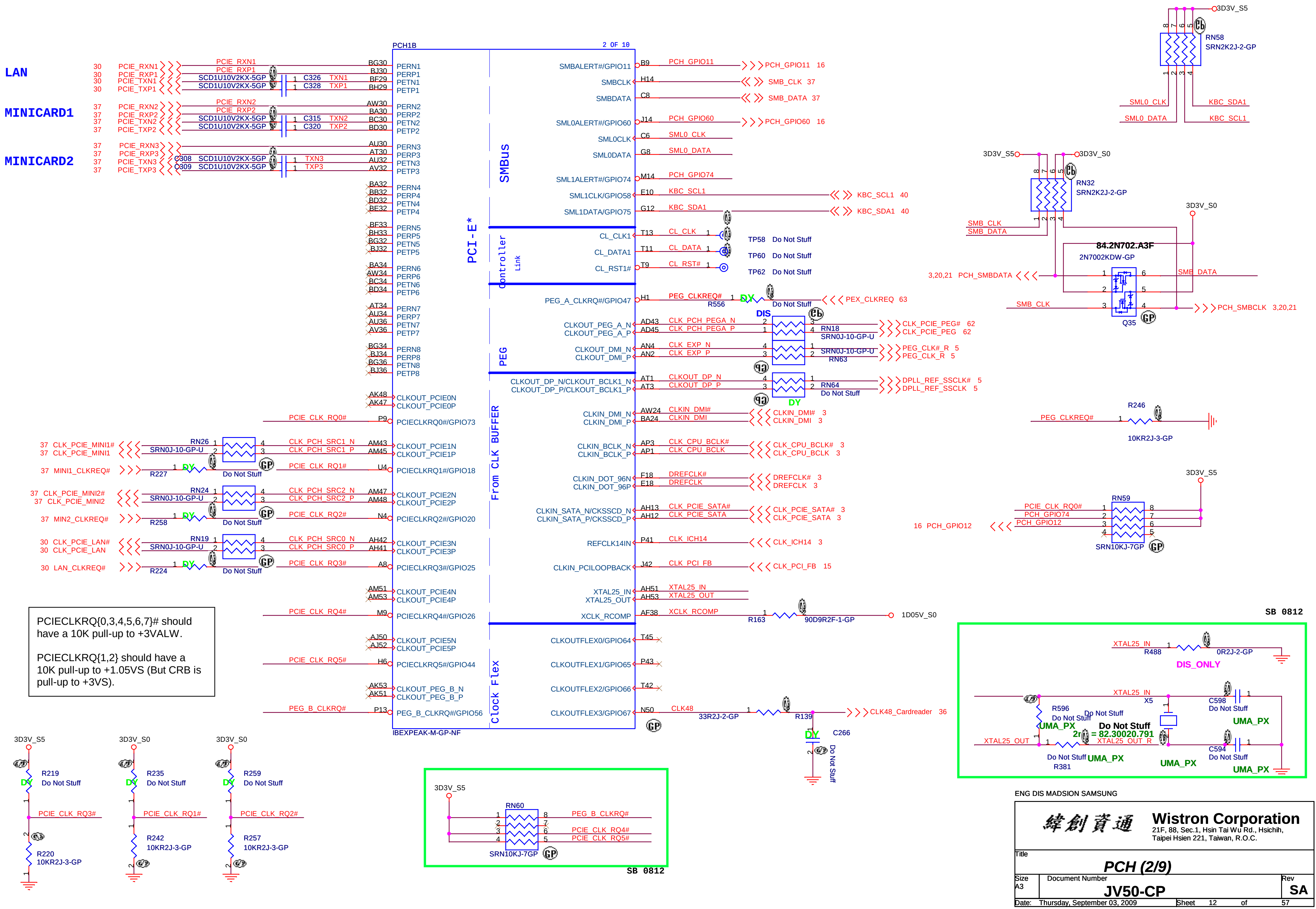

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).

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Title: PCH (2/9)

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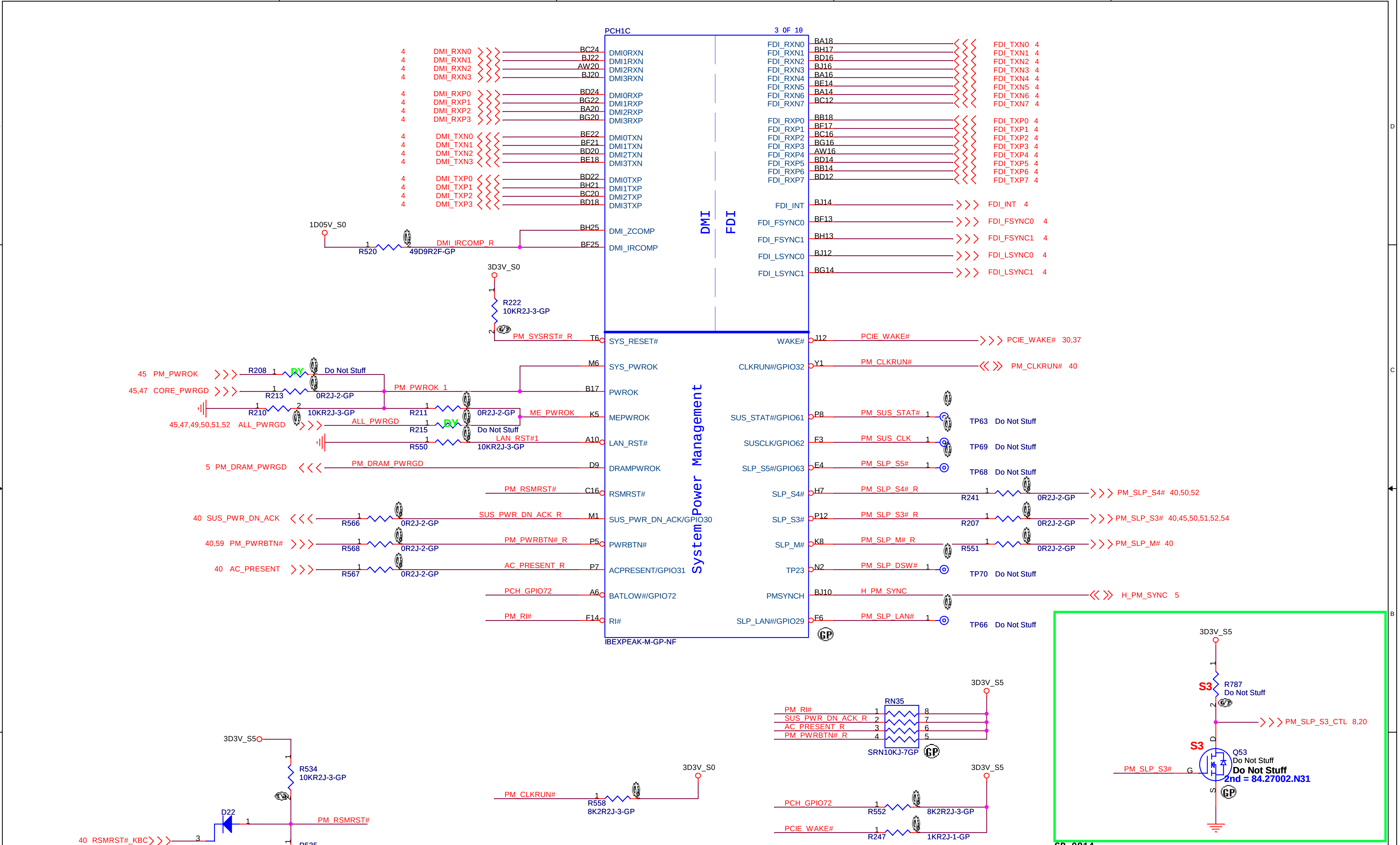

SB 0814

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Title
PCH (3/9)

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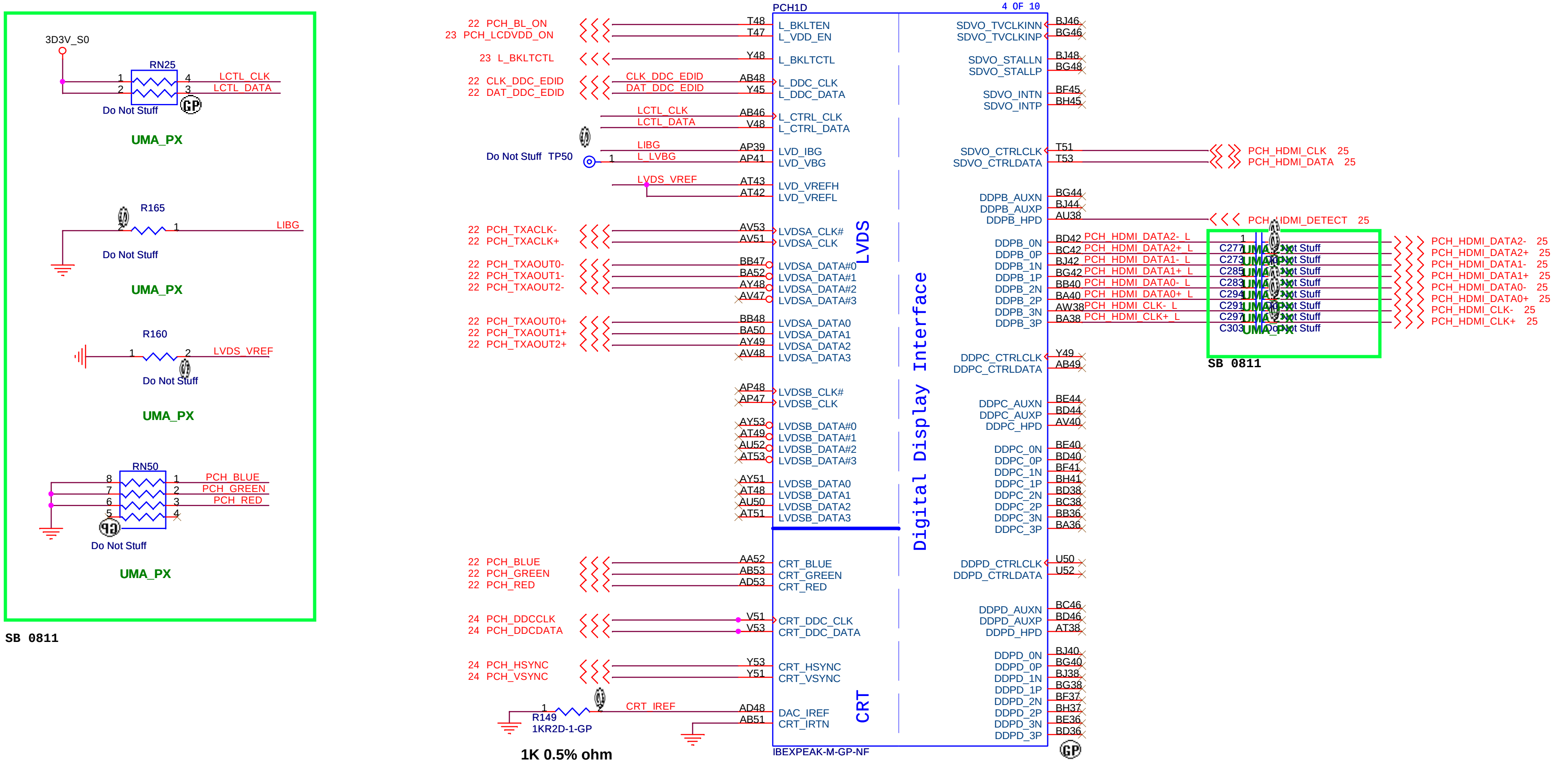

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Title		
	PCH (4/9)	
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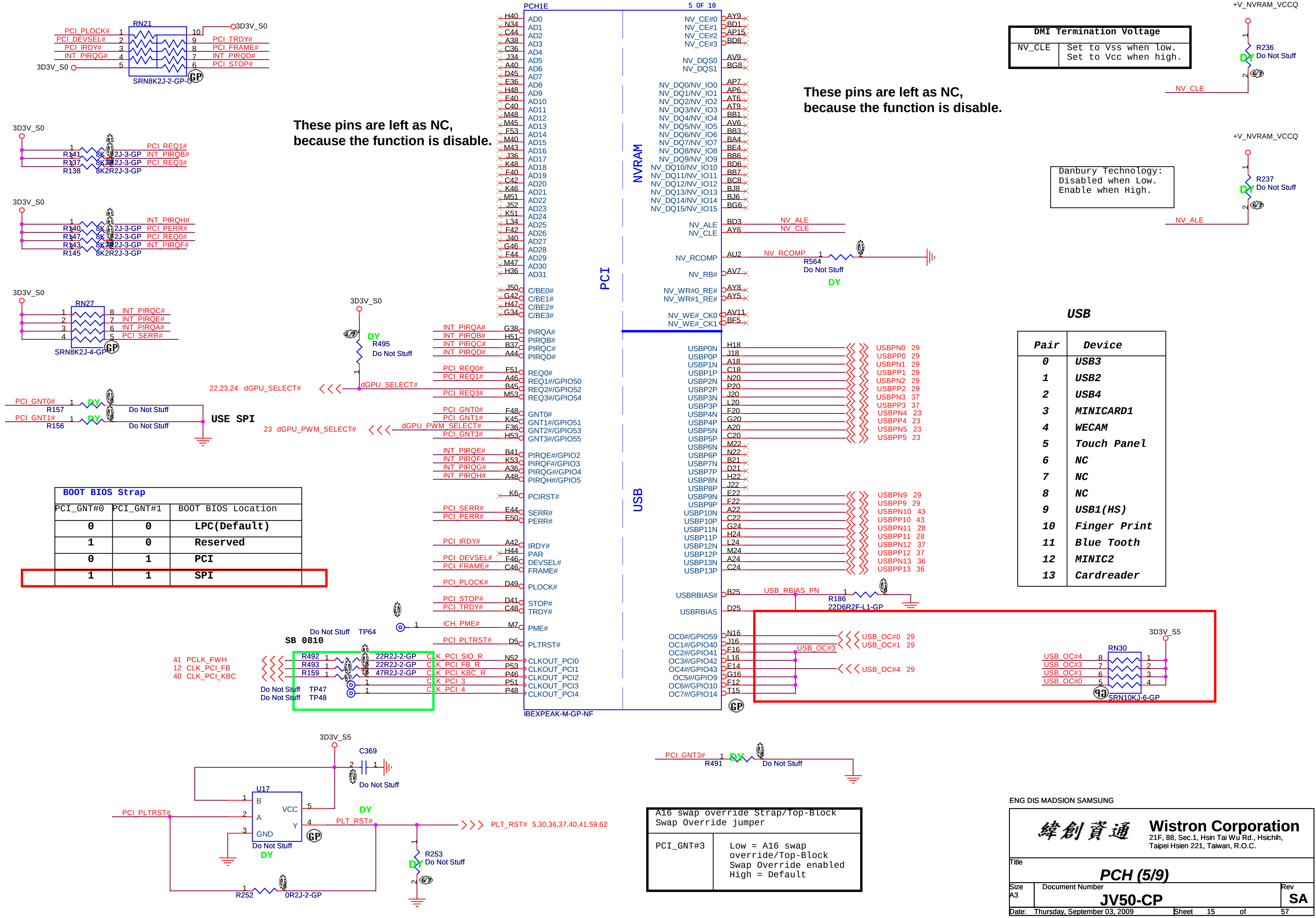

These pins are left as NC, because the function is disable.

These pins are left as NC, because the function is disable.

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

Danbury Technology:
Disabled when Low.
Enable when High.

USB

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1(HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

BOOT BIOS Strap

PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

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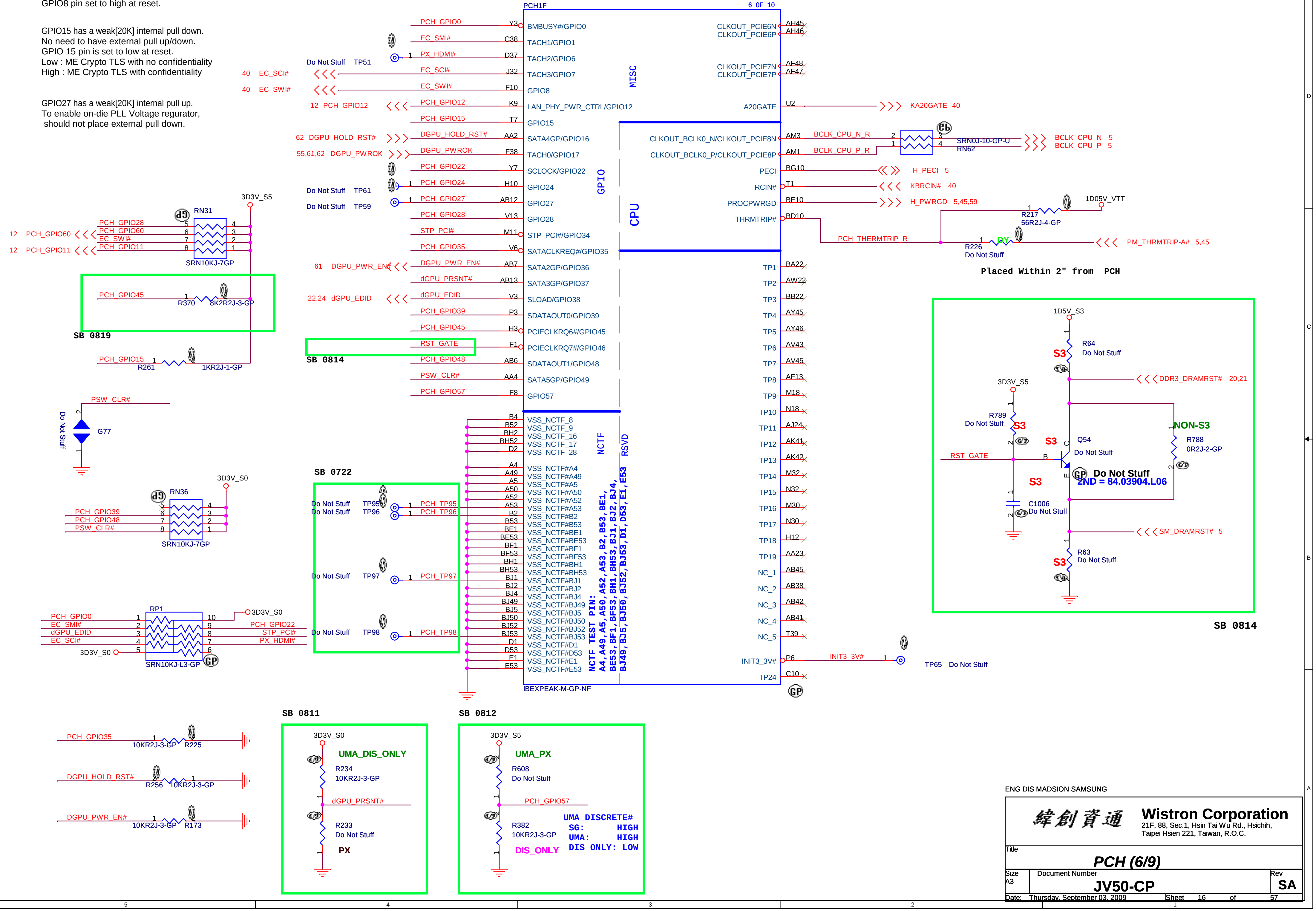
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.



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Title		
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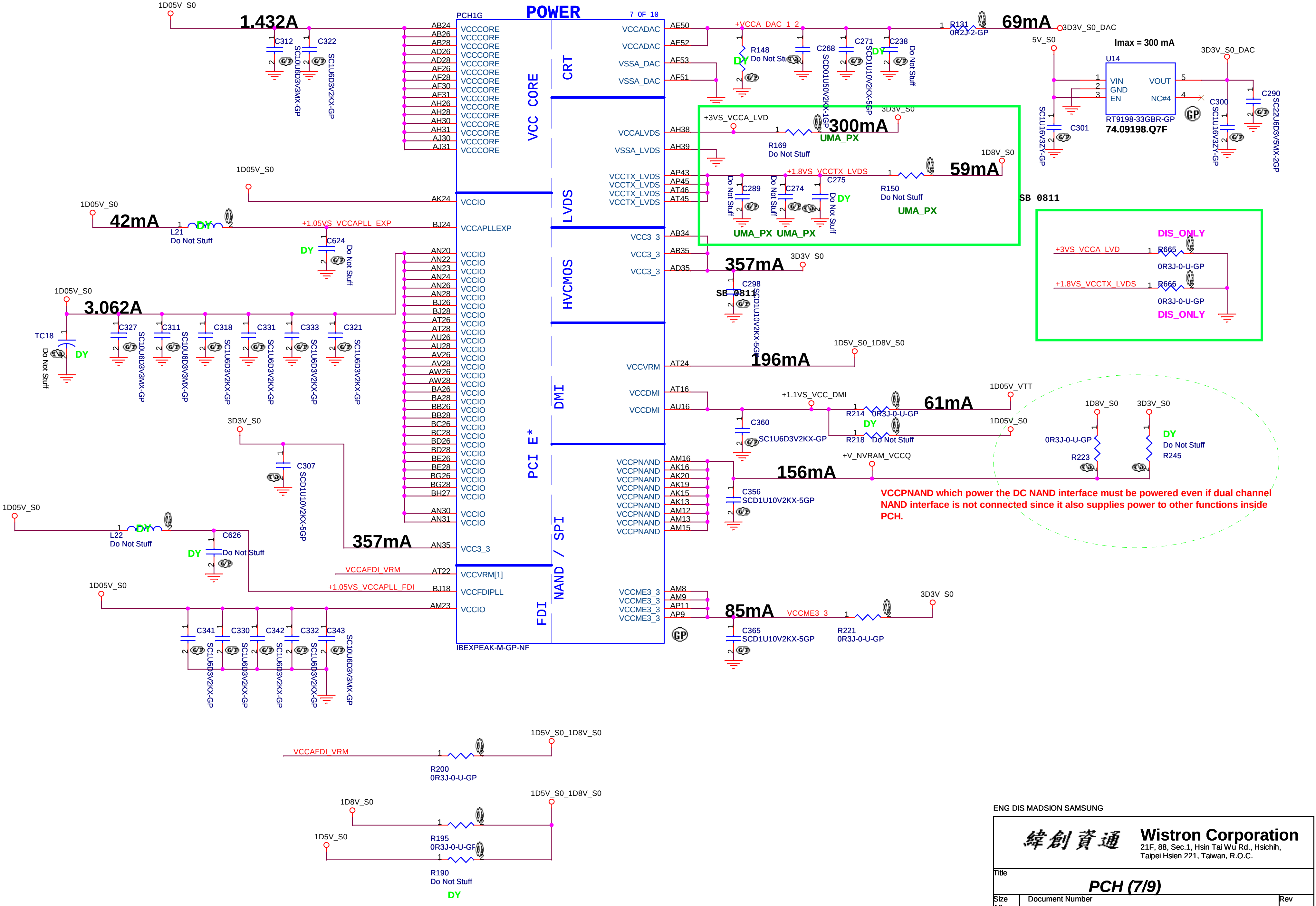

VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.

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Title
PCH (7/9)

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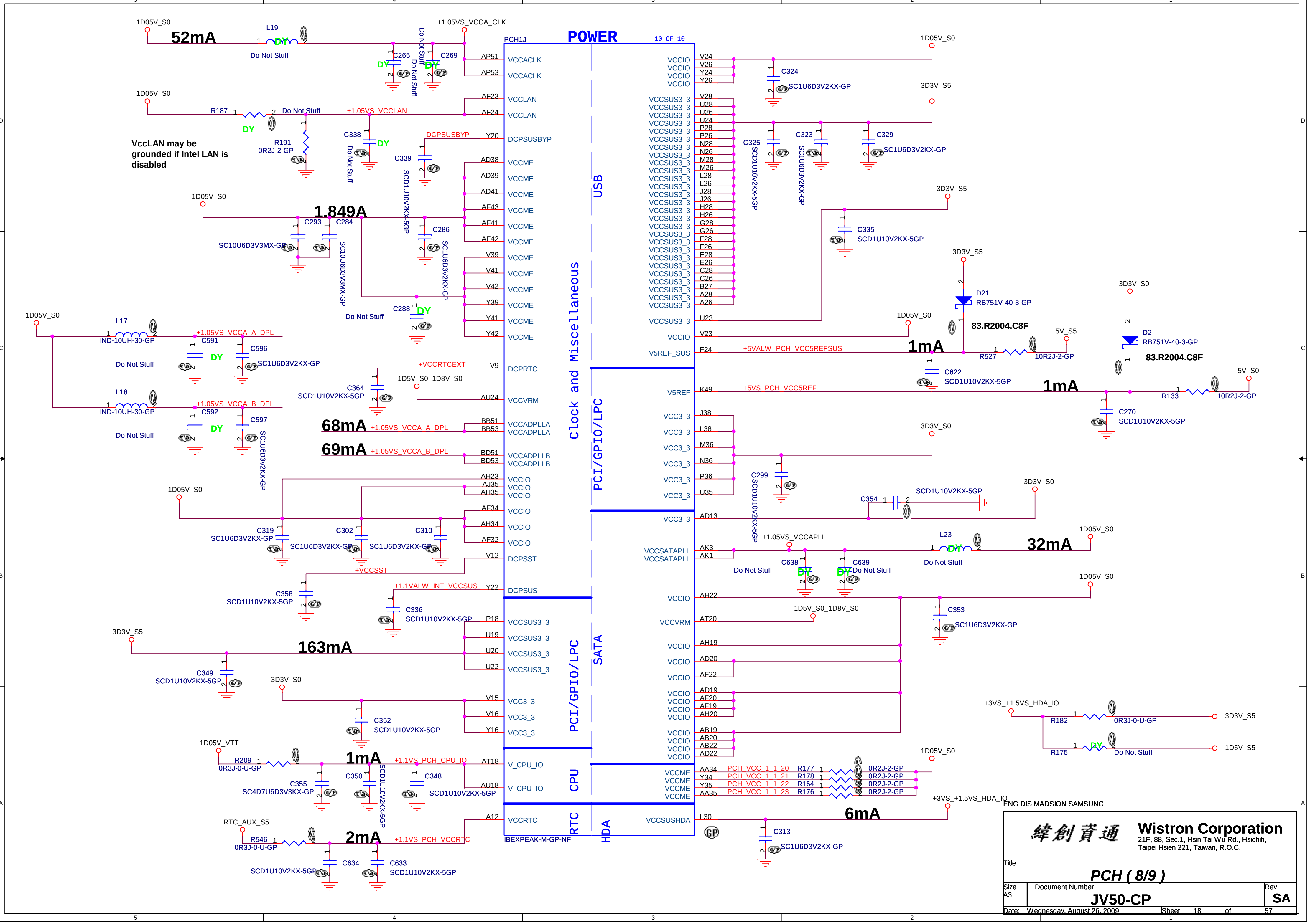

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Title
PCH (8/9)

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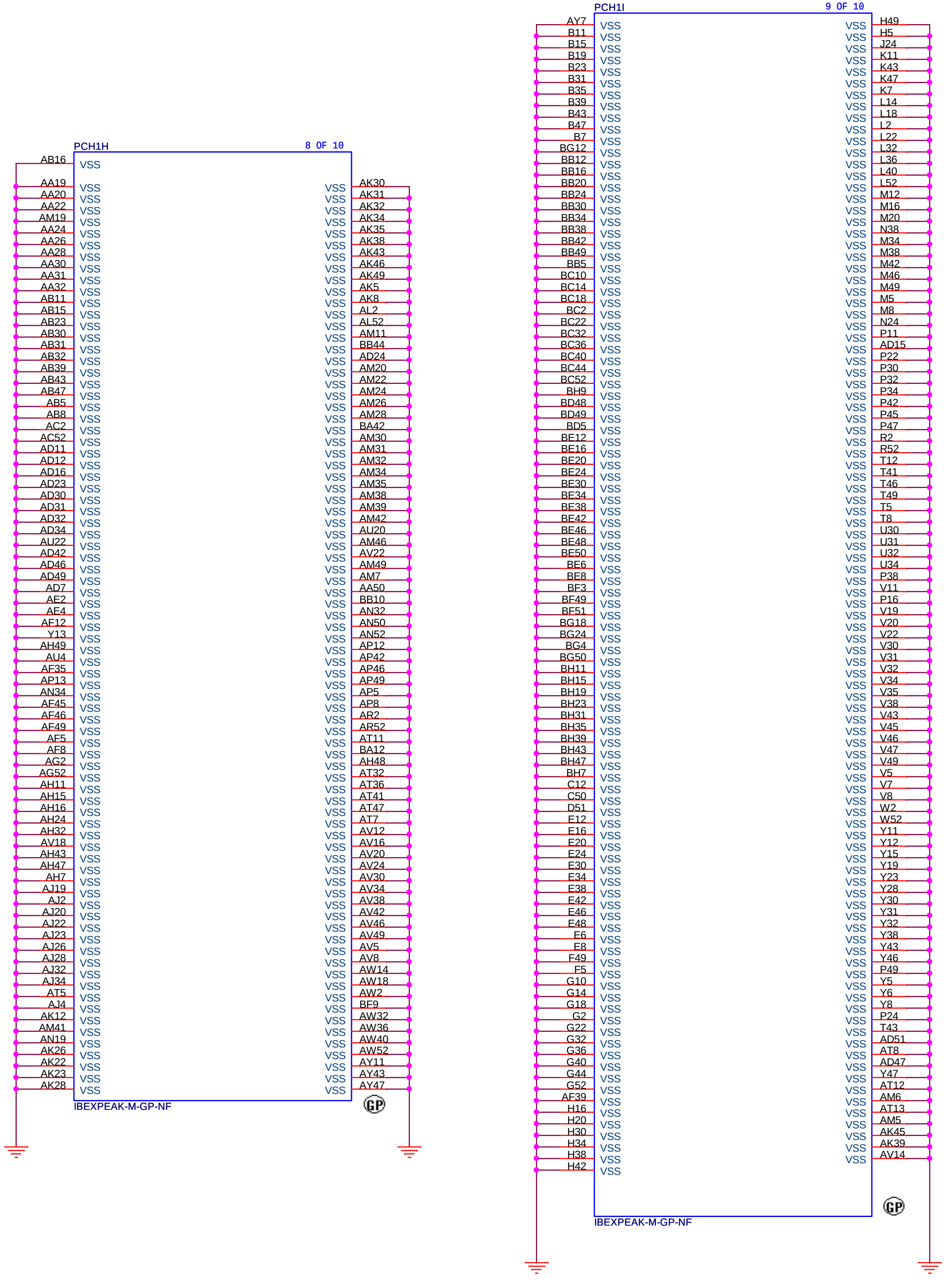

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Title
PCH (9/9)

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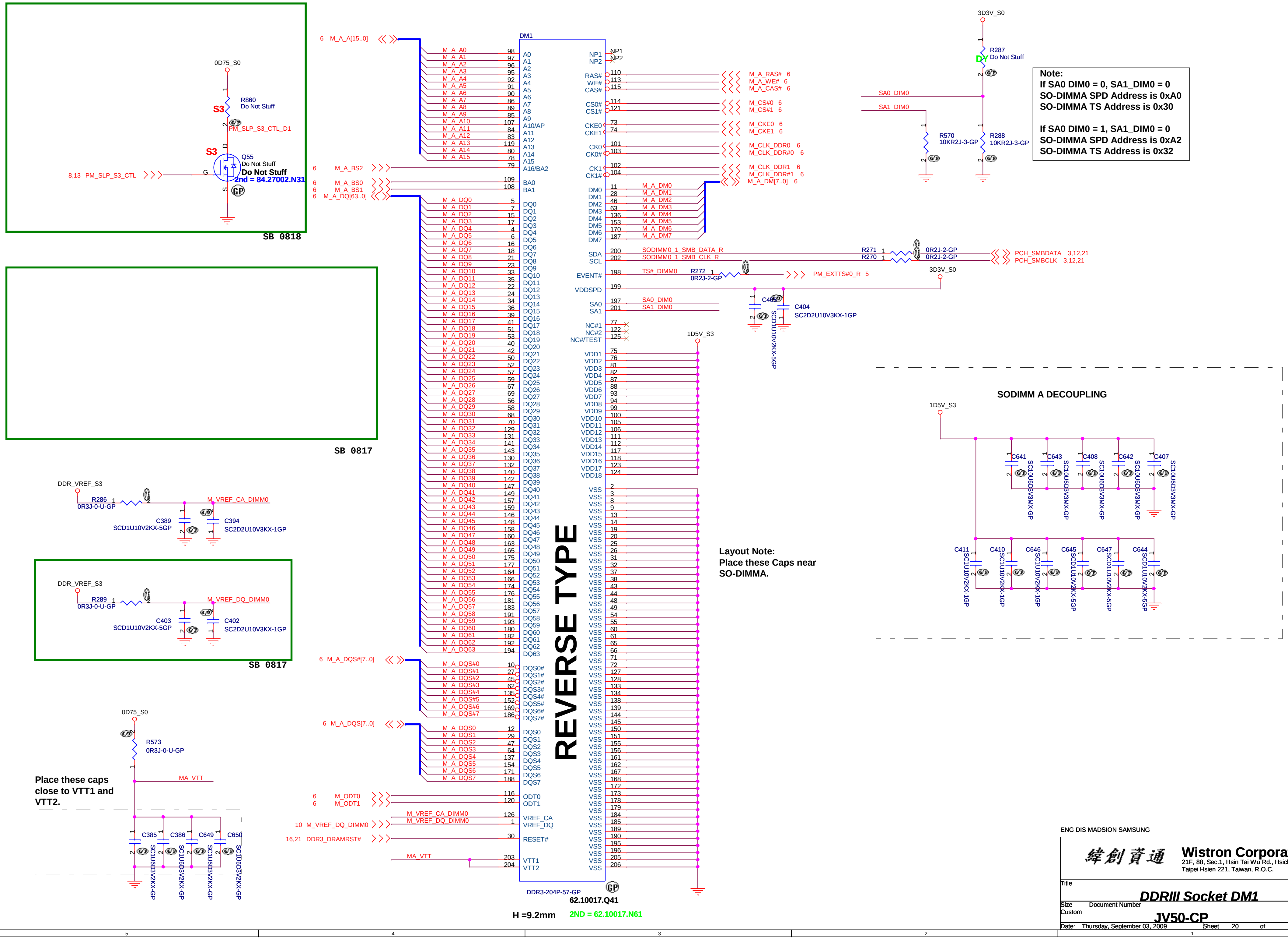

Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Layout Note:
Place these Caps near
SO-DIMMA.

Place these caps
close to VTT1 and
VTT2.

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Title
DDRIII Socket DM1

Size Custom
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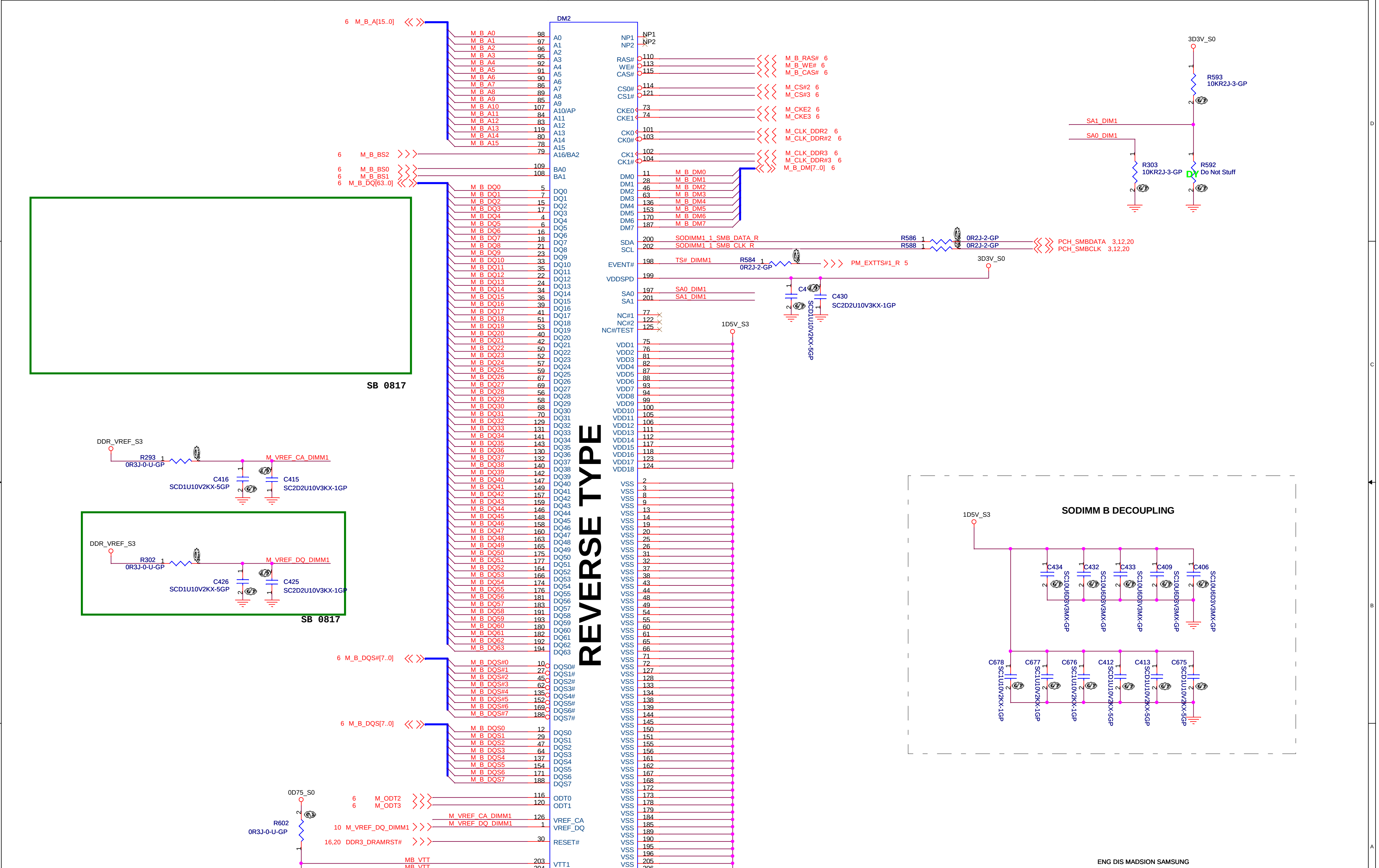

Place these caps close to VTT1 and VTT2.

H = 5.2mm

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

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Title
DDRIII Socket DM2

Size	Document Number	Rev
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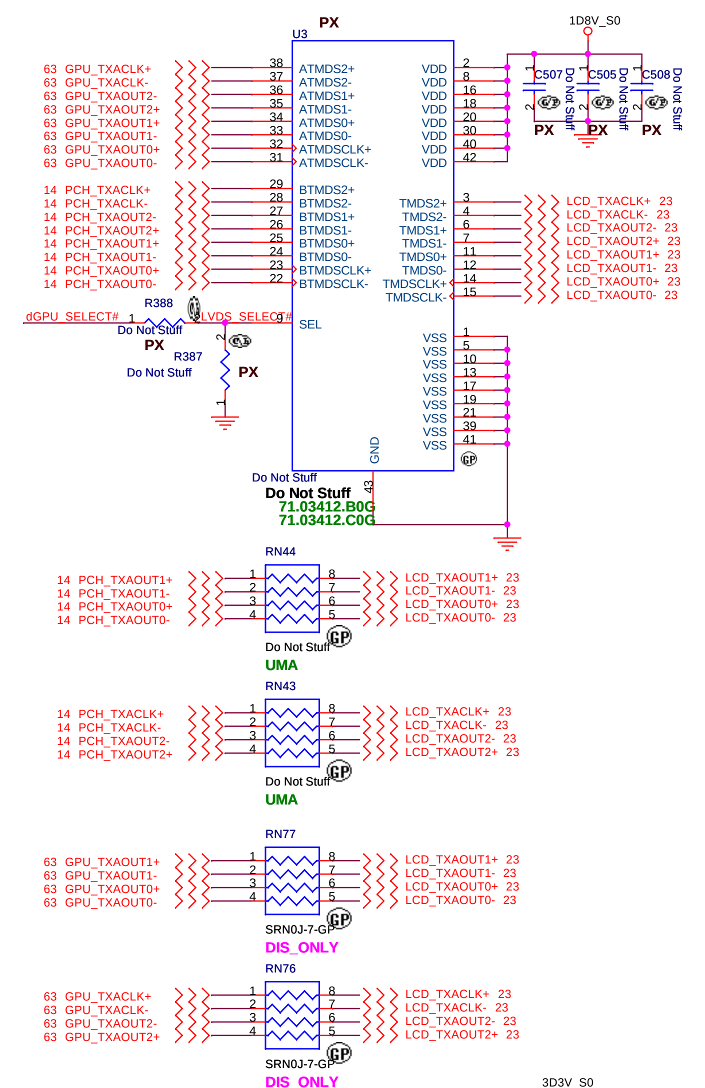
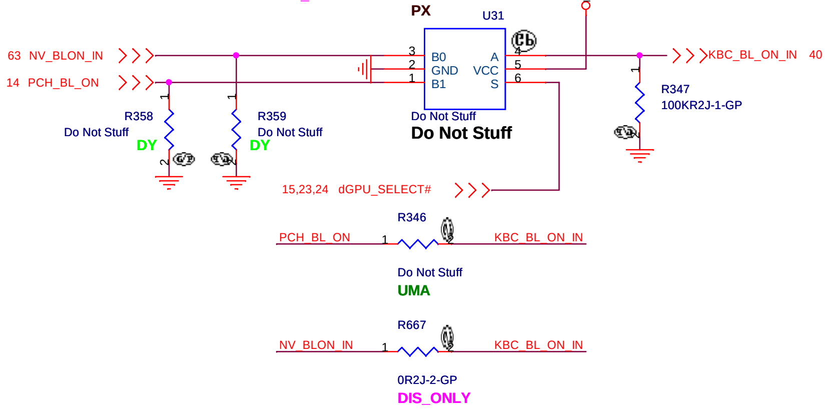
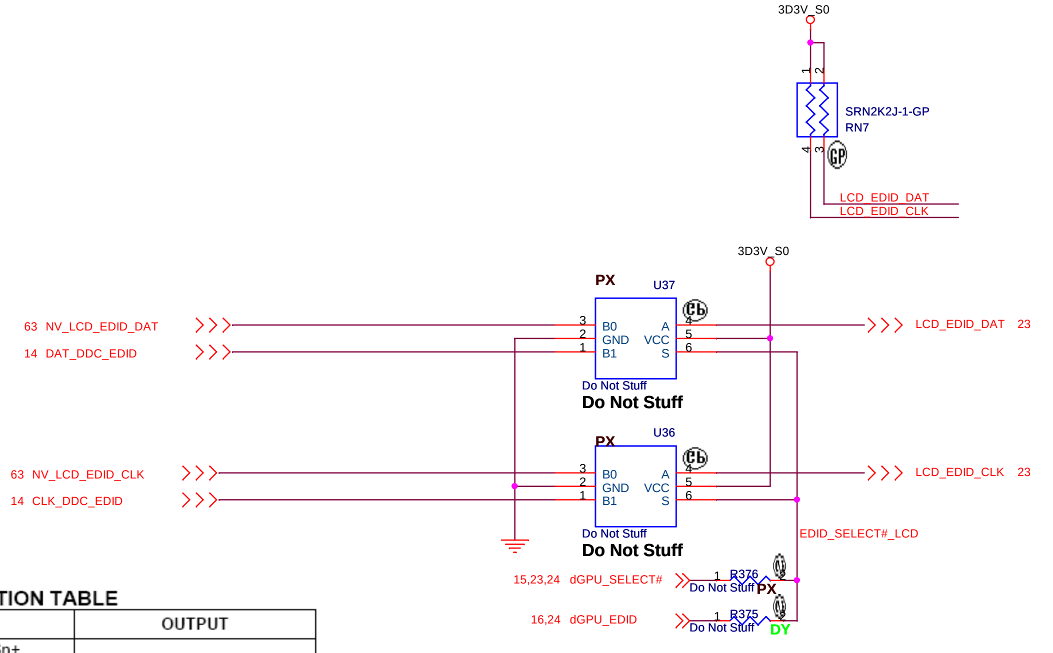
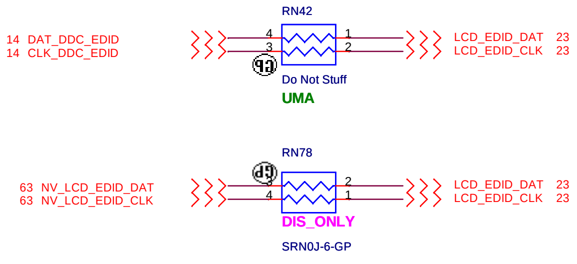


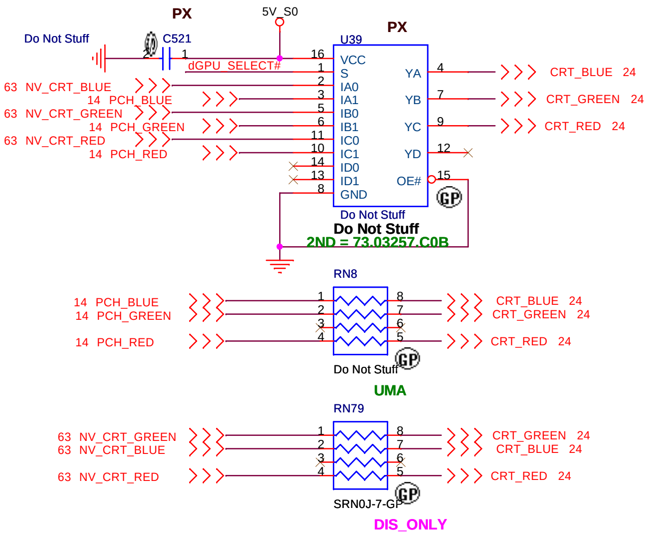




FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-





$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

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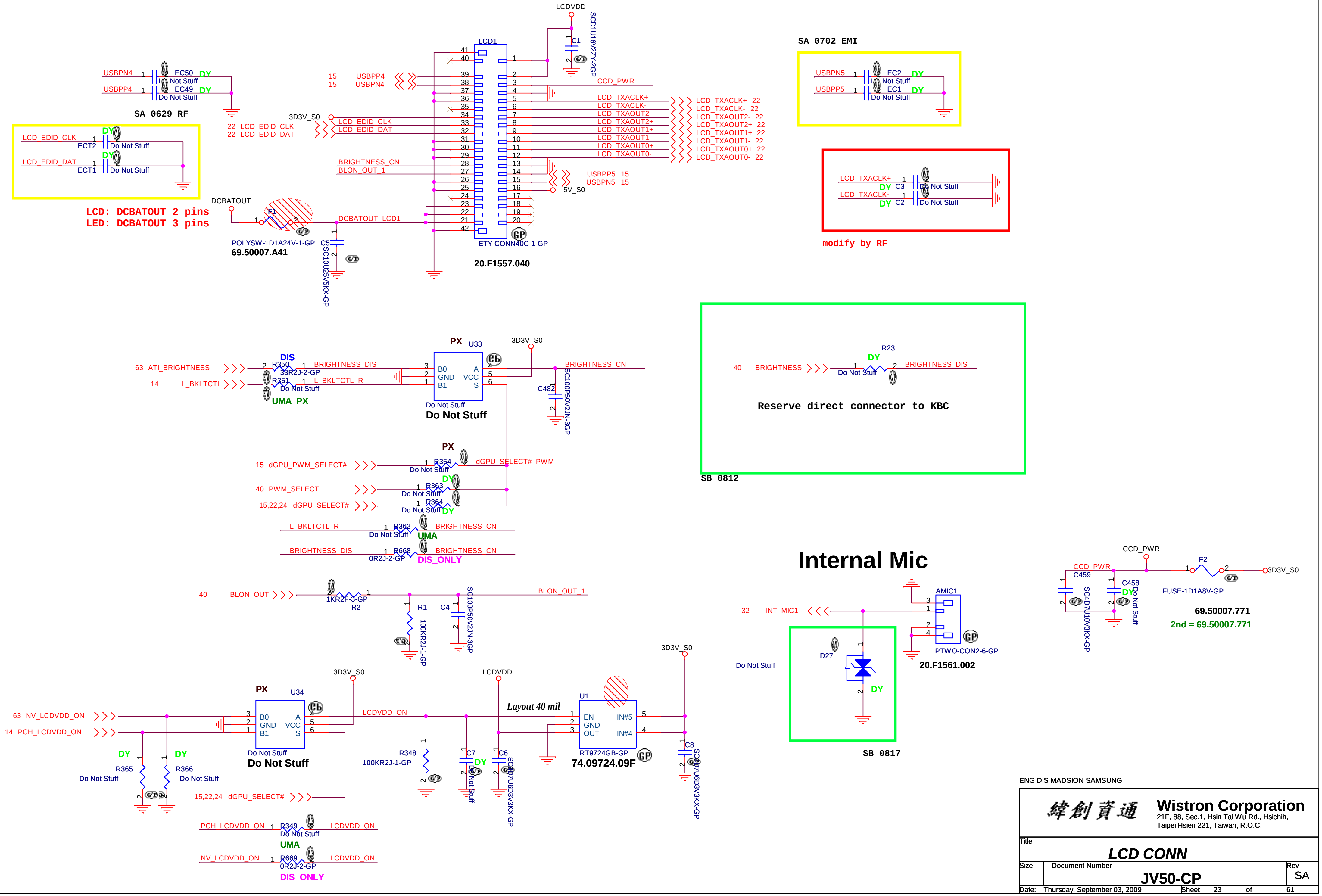
Taipei Hsien 221, Taiwan, R.O.C.

Title
PX SWITCH

Size A3 | Document Number **JV50-CP** | Rev **SA**

Date: Thursday, September 03, 2009 | Sheet 22 of 57

LCD/INVERTER/CCD CONN



ENG DIS MADSION SAMSUNG

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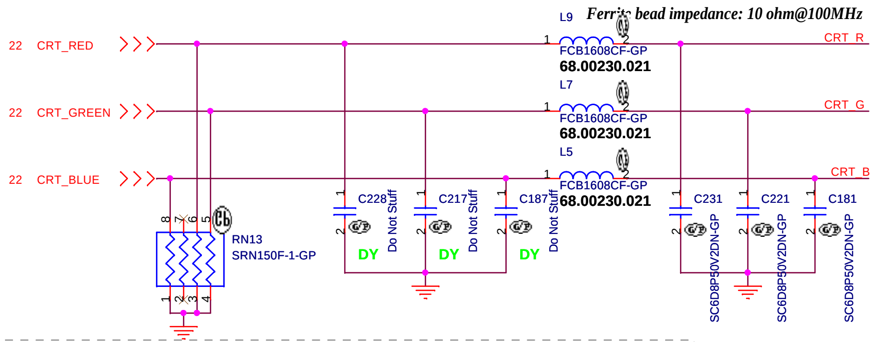
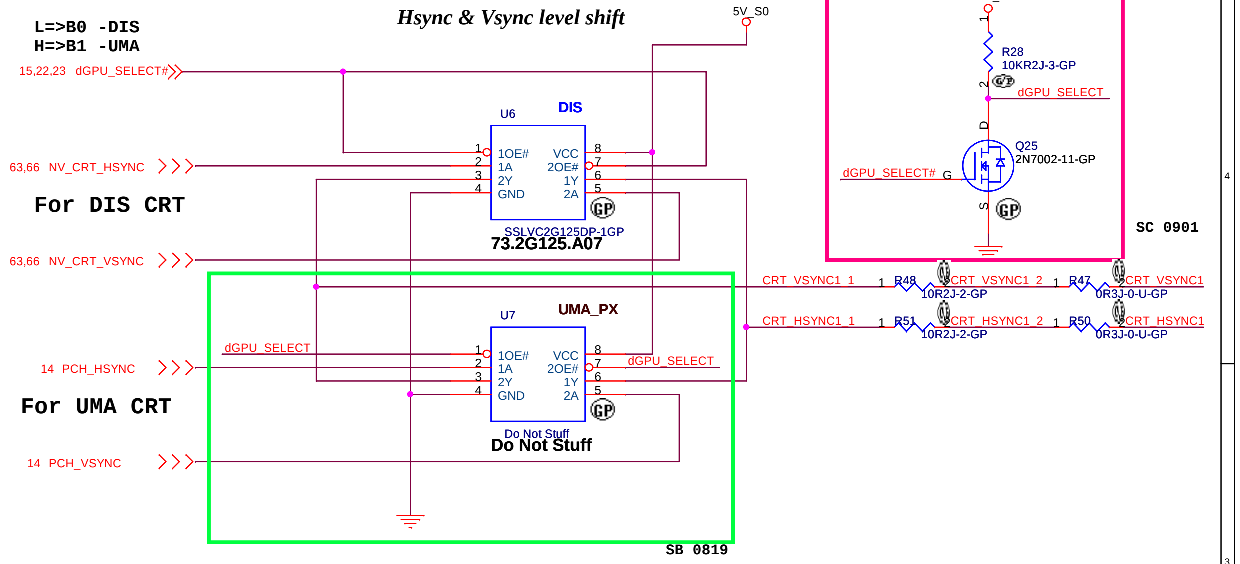
Title	LCD CONN	
Size	Document Number: JV50-CP	Rev: SA
Date: Thursday, September 03, 2009	Sheet 23 of 61	

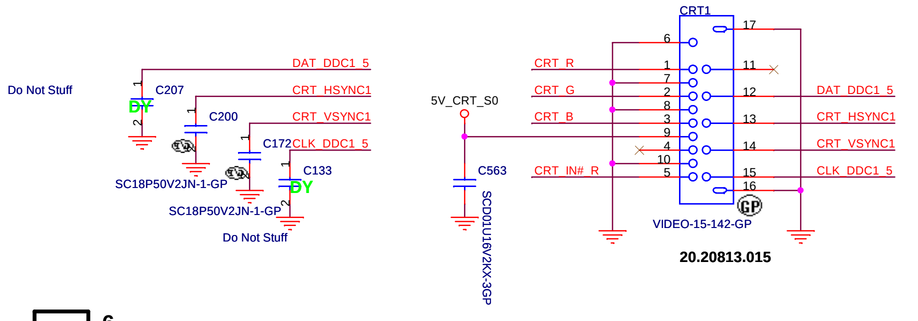
Layout Note:
Place these resistors
close to the CRT-out
connector

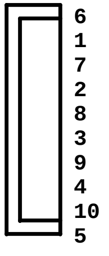


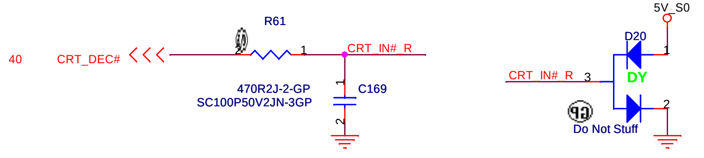
Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

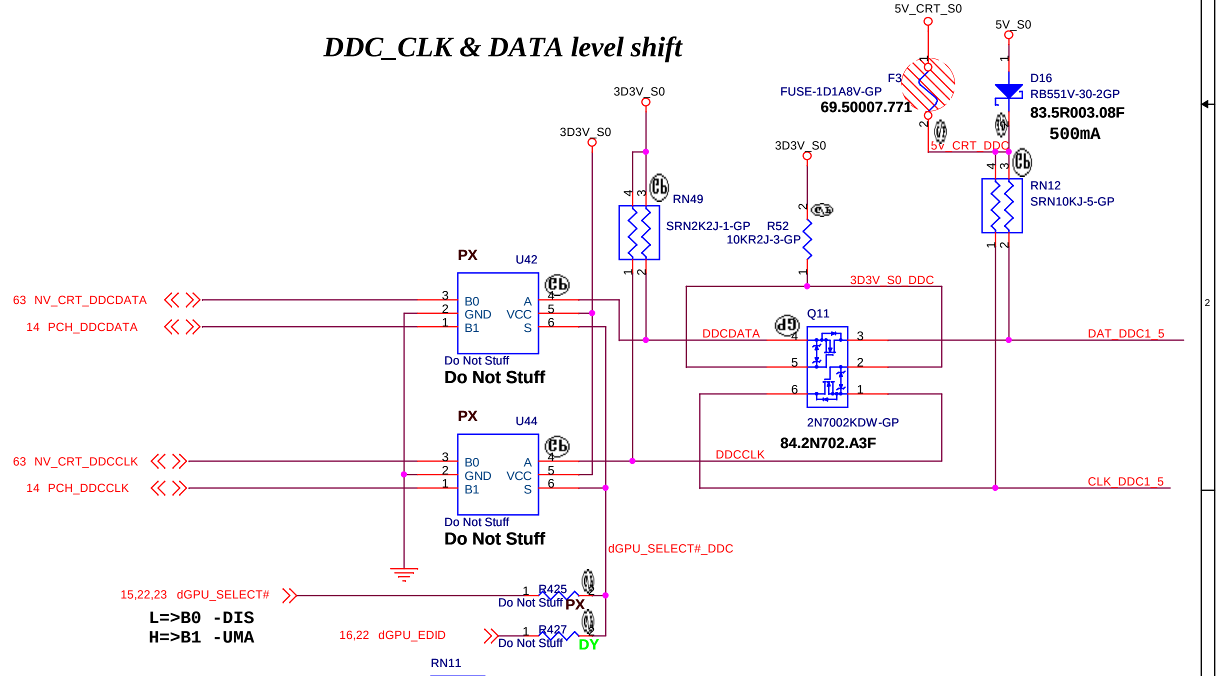


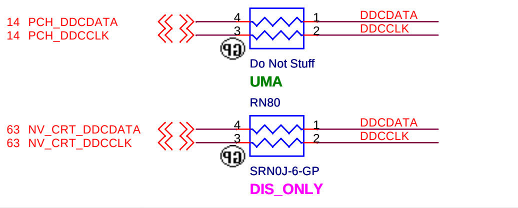
CRT I/F & CONNECTOR











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Title
CRT CONN

Size | Document Number | Rev
JV50-CP | SA

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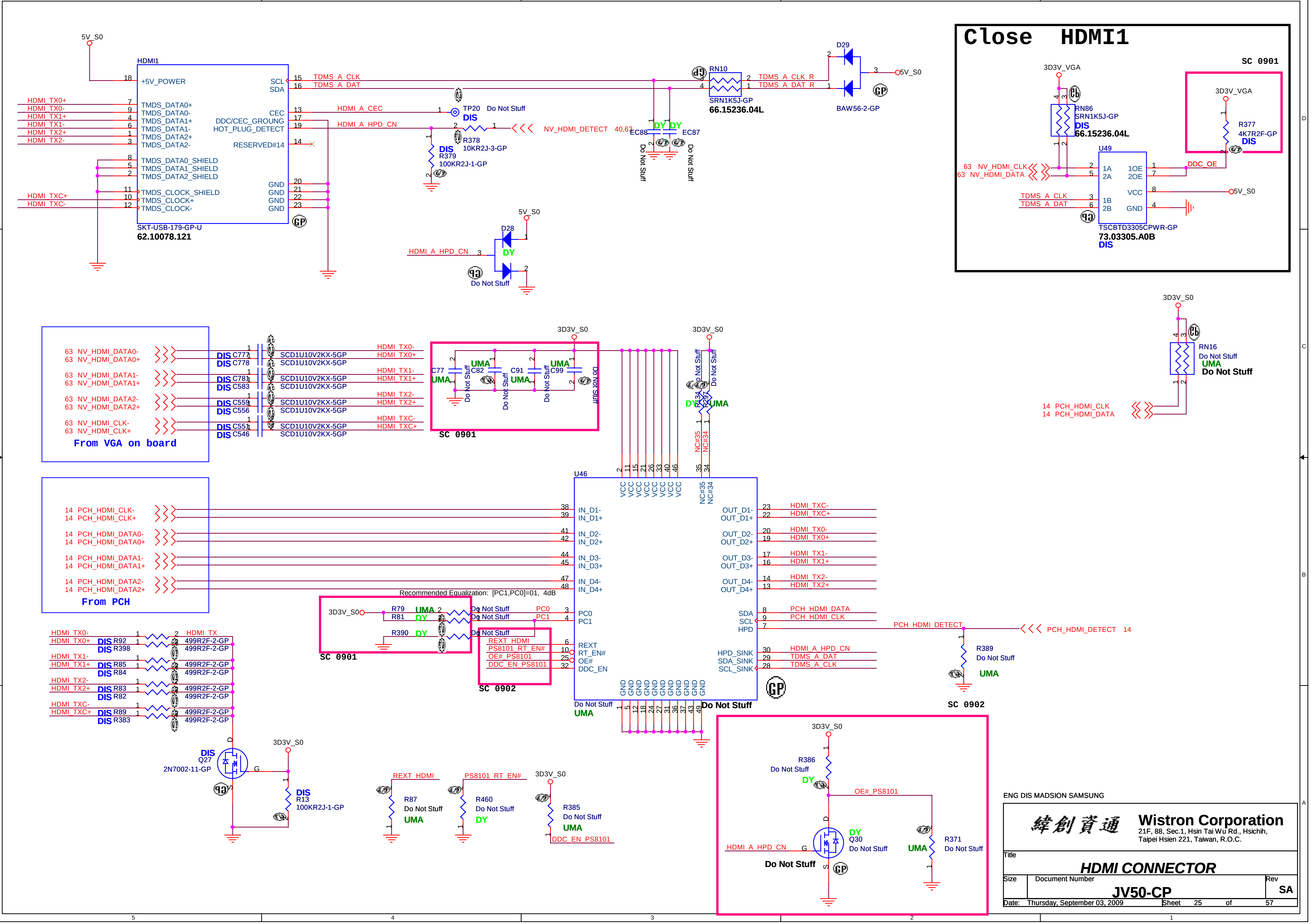

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
HDMI CONNECTOR

Size | Document Number | Rev
JV50-CP | SA

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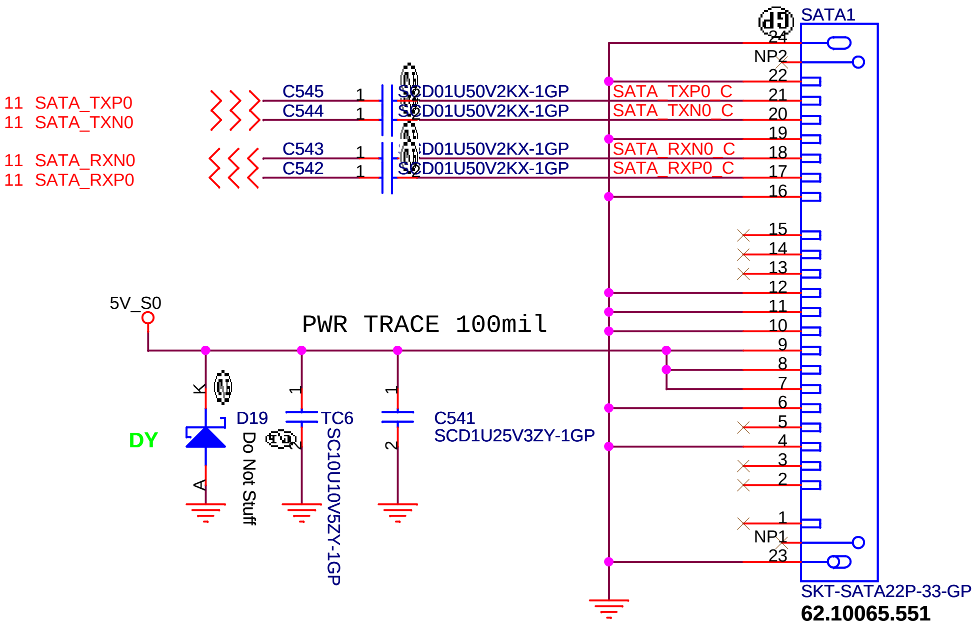
SATA Connector



ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
HDD CONN

Size Document Number
JV50-CP
Rev SA

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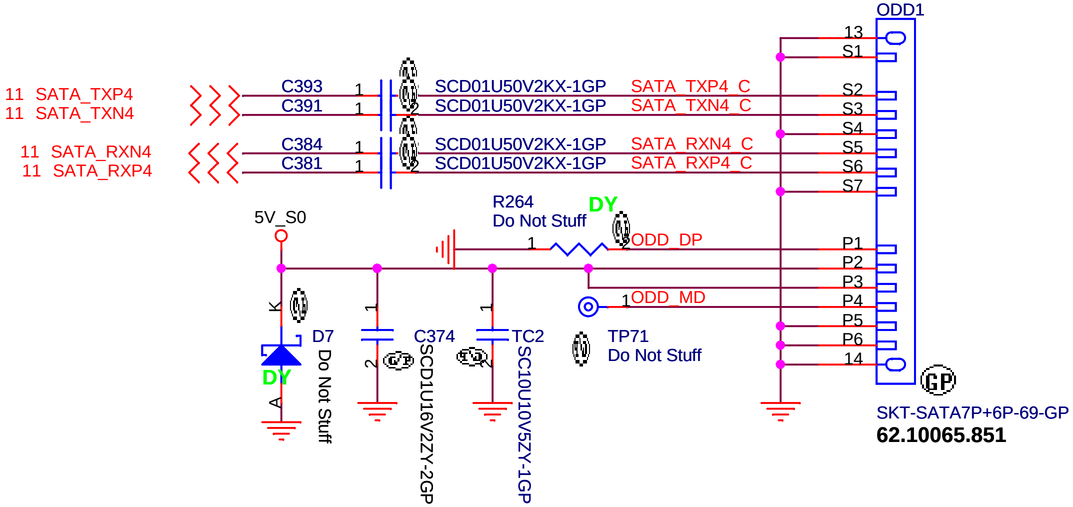
ODD Connector



ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
ODD

Size
Document Number
JV50-CP
Rev
SA

Date: Thursday, September 03, 2009
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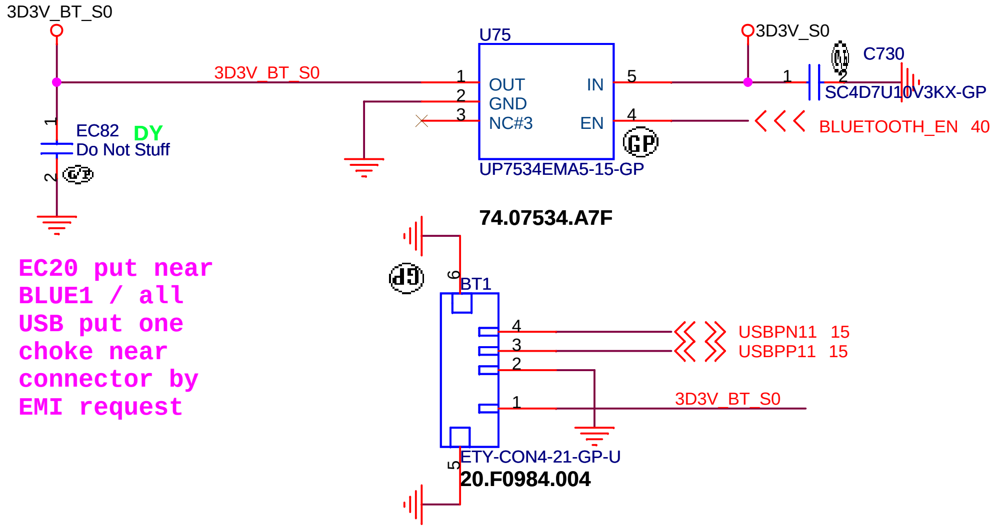
BLUETOOTH MODULE



EC20 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
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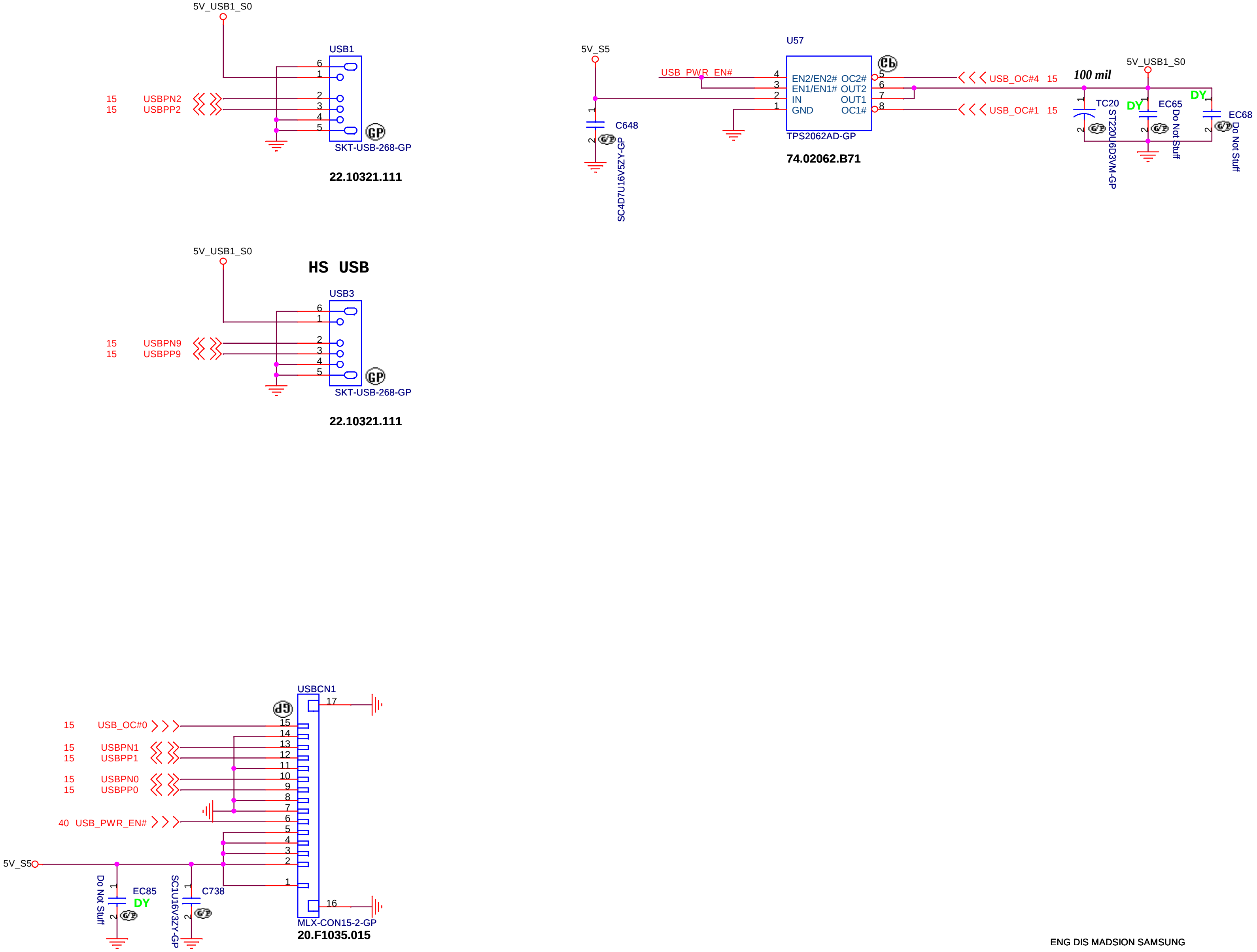
Taipei Hsien 221, Taiwan, R.O.C.

Title
BLUETOOTH

Size
Document Number
JV50-CP
Rev
SA

Date: Thursday, September 03, 2009 Sheet 28 of 61



ENG DIS MADSION SAMSUNG

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
USB CONN

Size Document Number
JV50-CP
Rev SA

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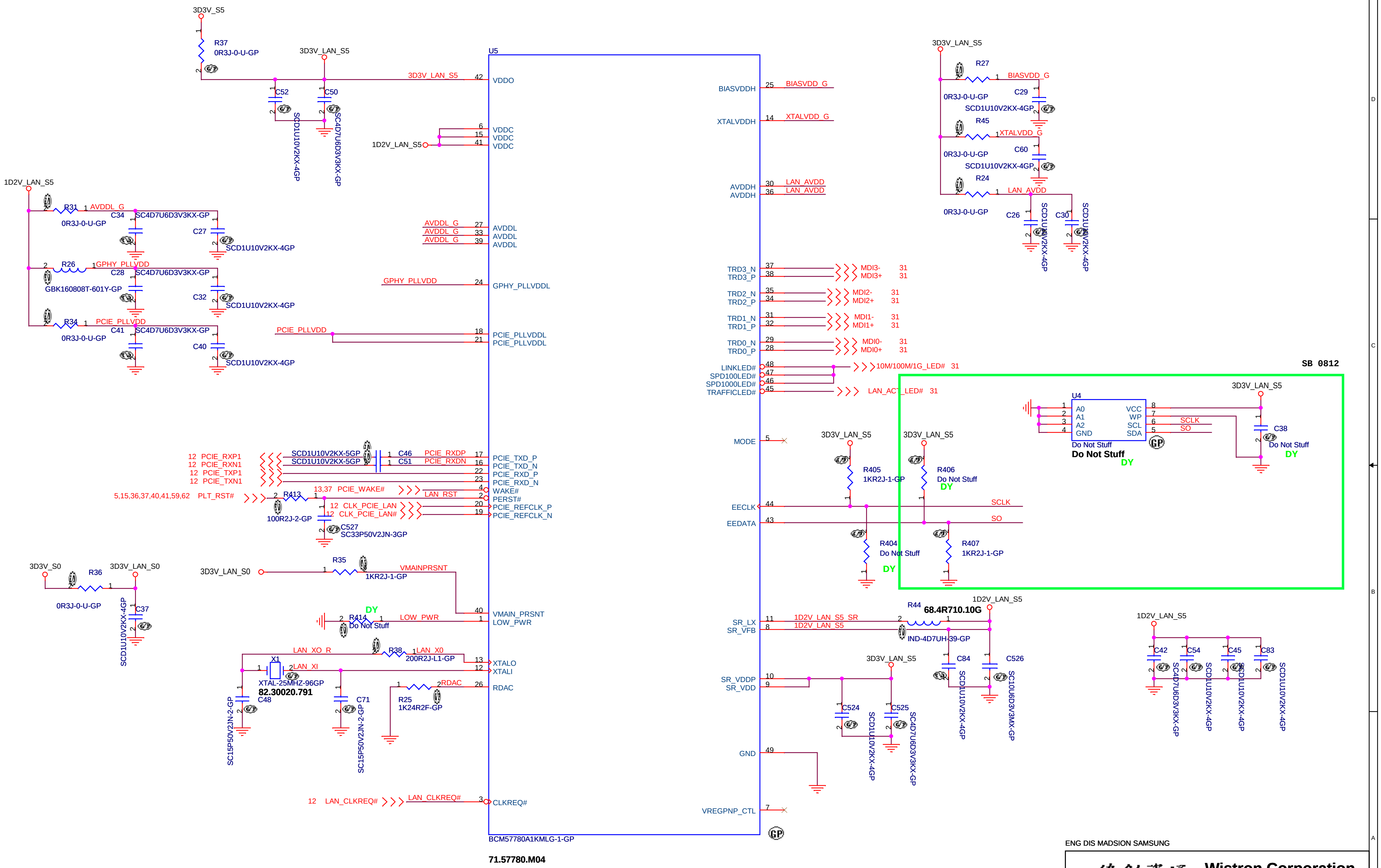

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
BCM57780

Size Custom
Document Number JV50-CP
Rev SA

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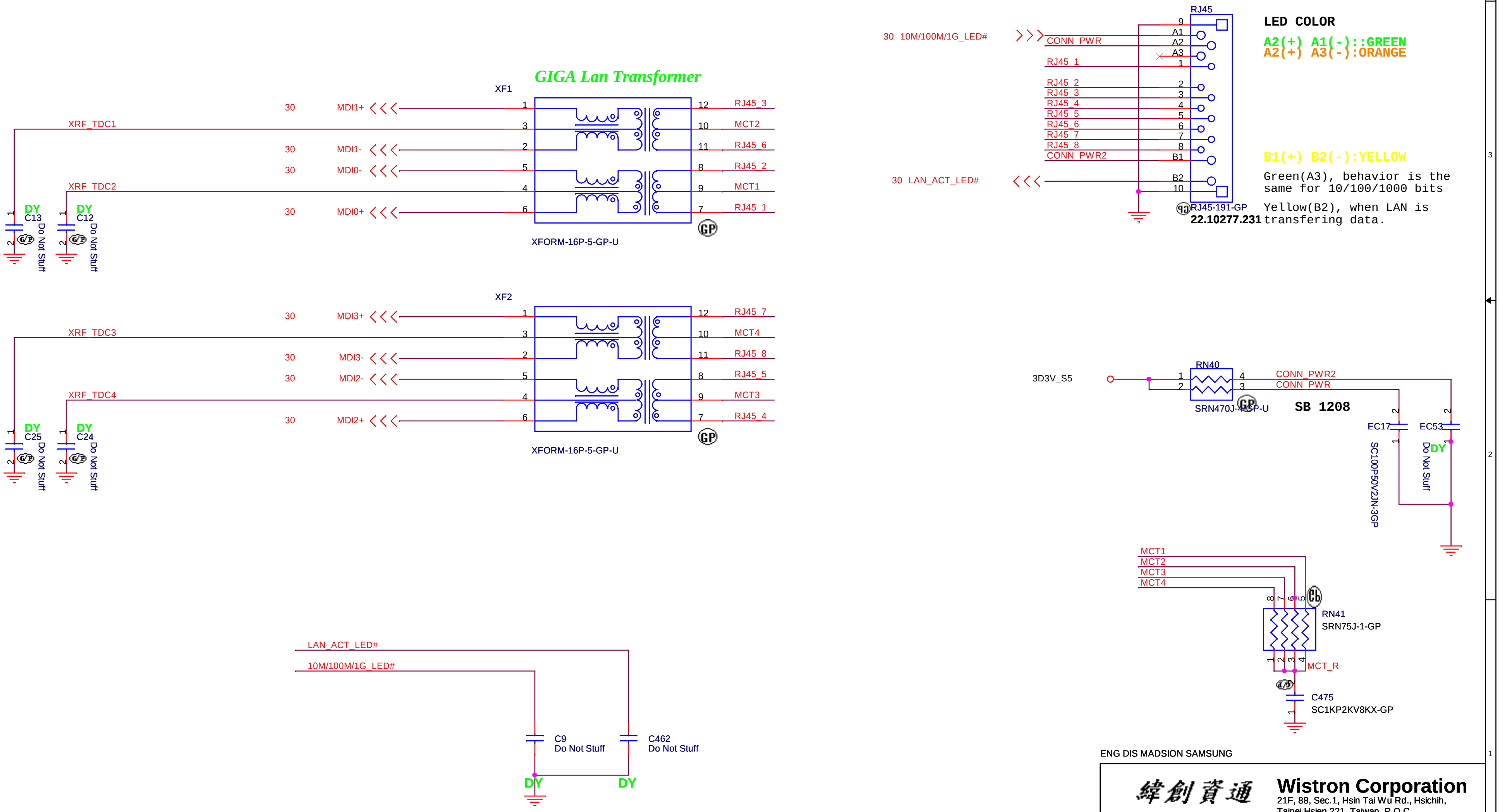
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector

LAN Connector



ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
LAN CONN

Size A3
Document Number JV50-CP
Rev SA

Date: Thursday, September 03, 2009
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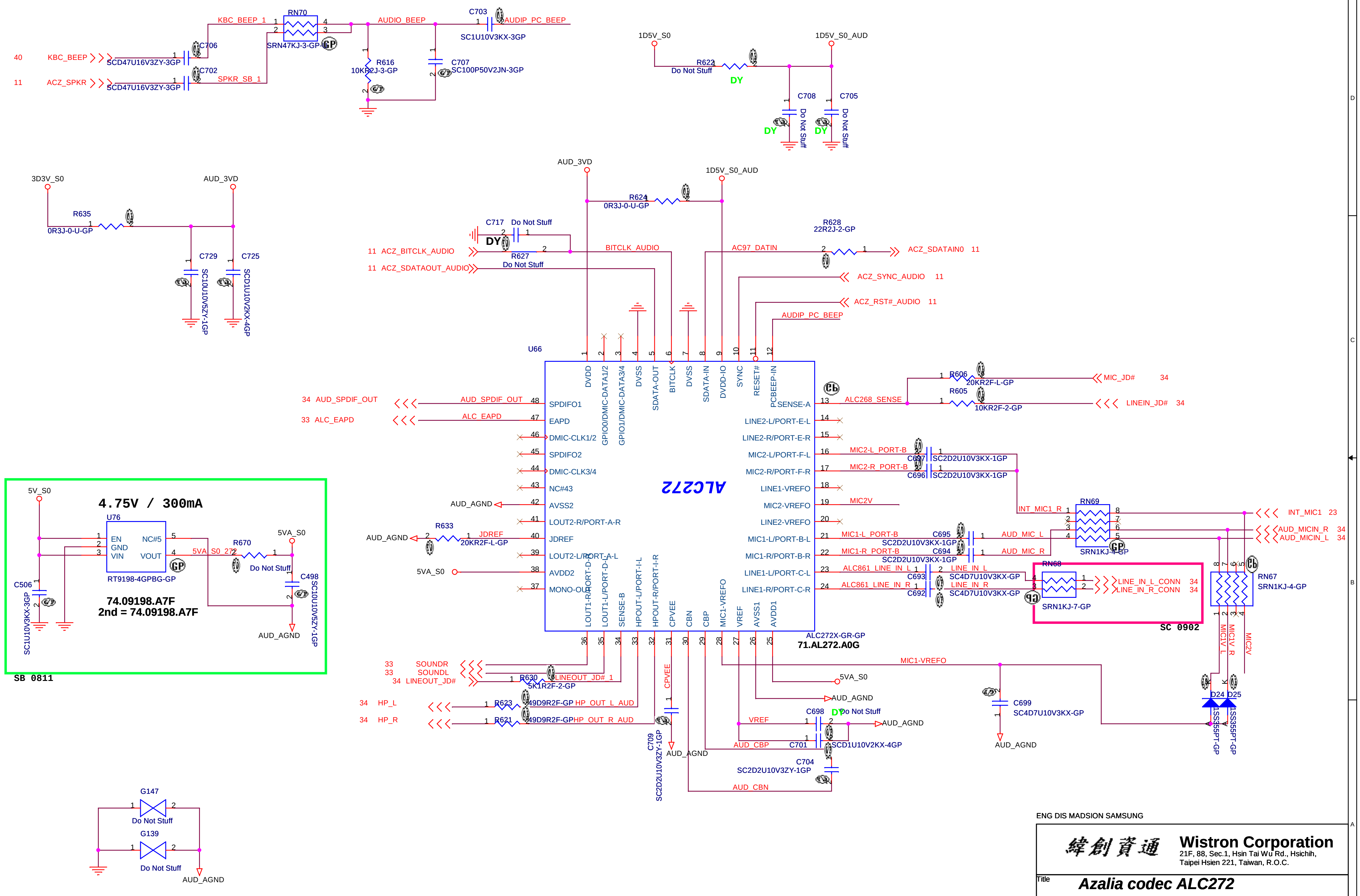

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Azalia codec ALC272

Size	Document Number	Rev
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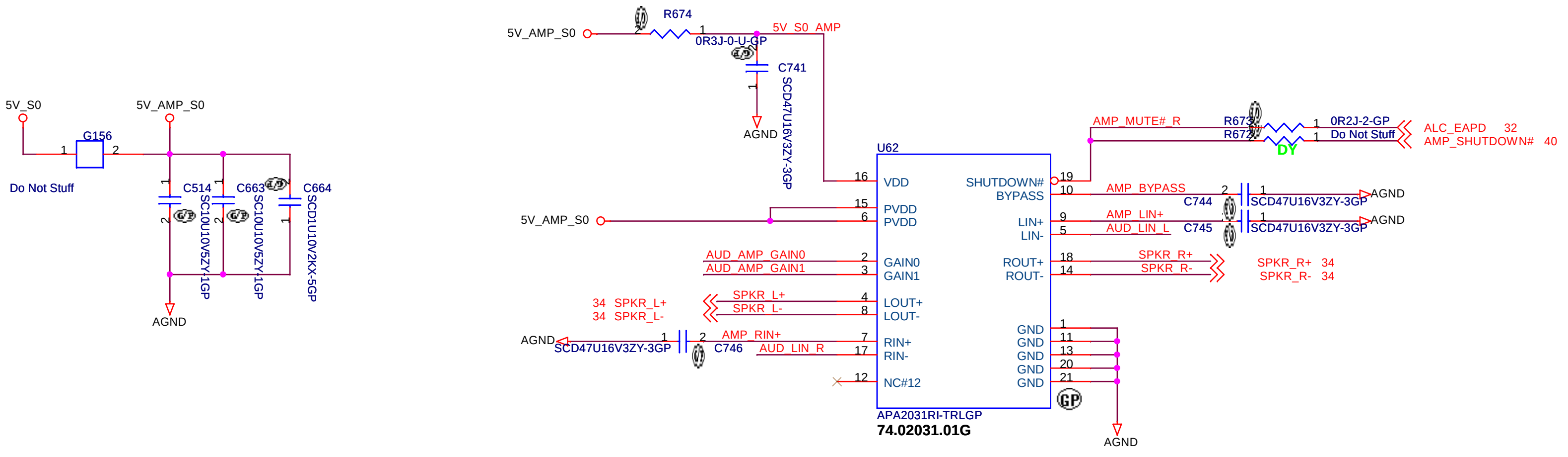
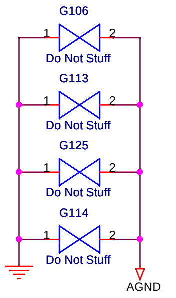
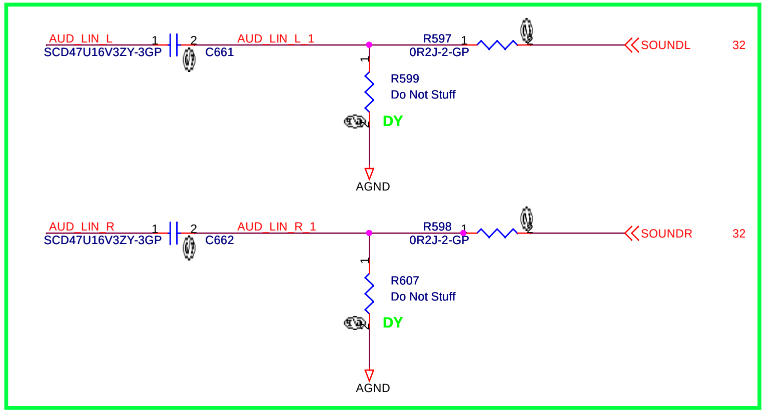
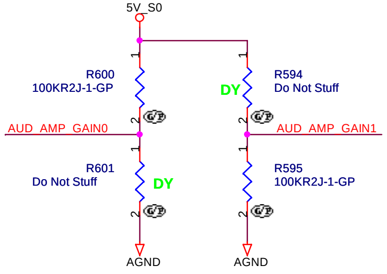






SB 0814

GAIN SETTING



GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
AUDIO AMP

Size
Document Number
JV50-CP
Rev
SA

Date: Thursday, September 03, 2009
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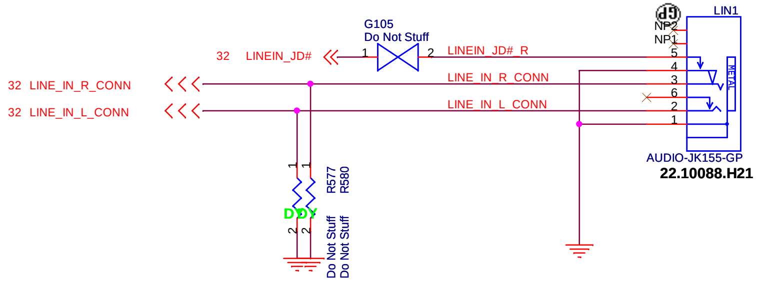
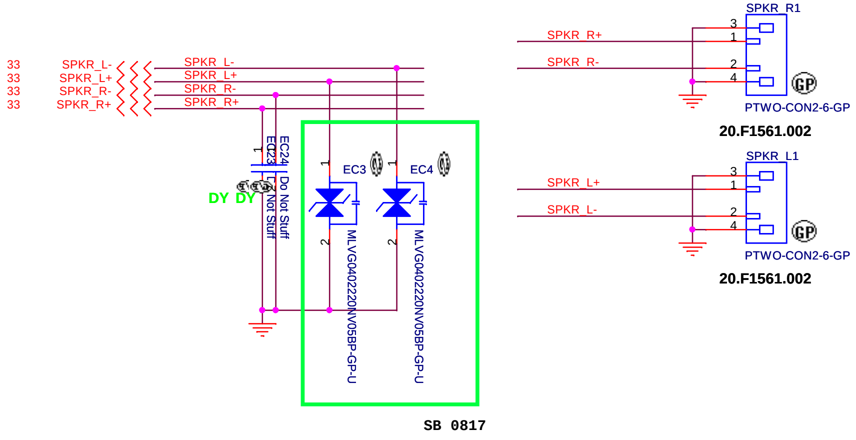
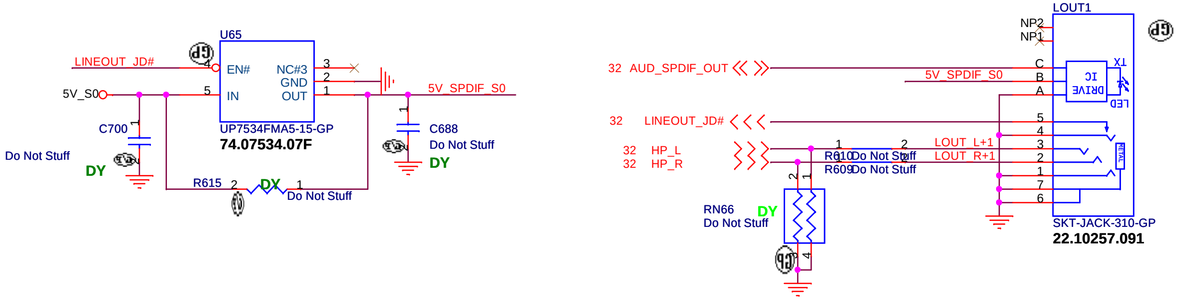
LINE IN

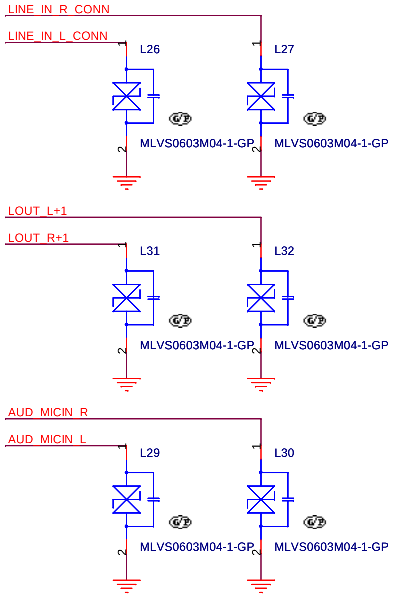


Internal Speaker

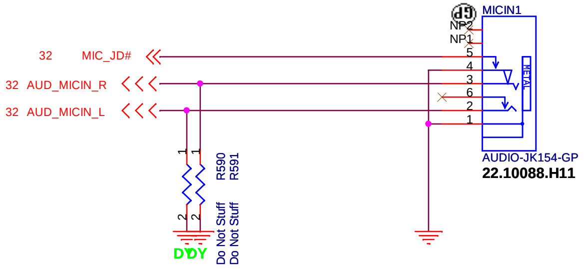


LINE OUT





MIC IN



ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
	AUDIO jack	
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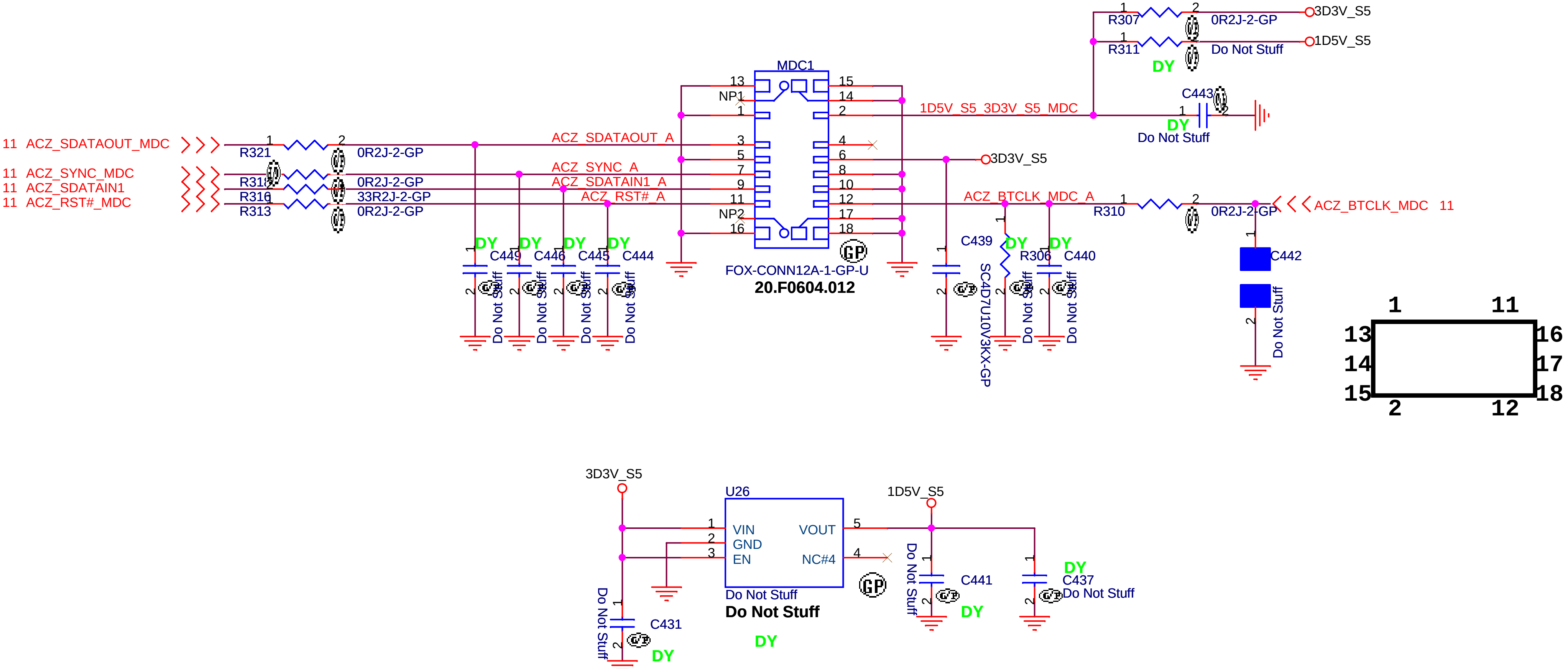
MDC 1.5 CONN



ENG DIS MADSION SAMSUNG

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	MDC		
Size	Document Number JV50-CP		Rev SA
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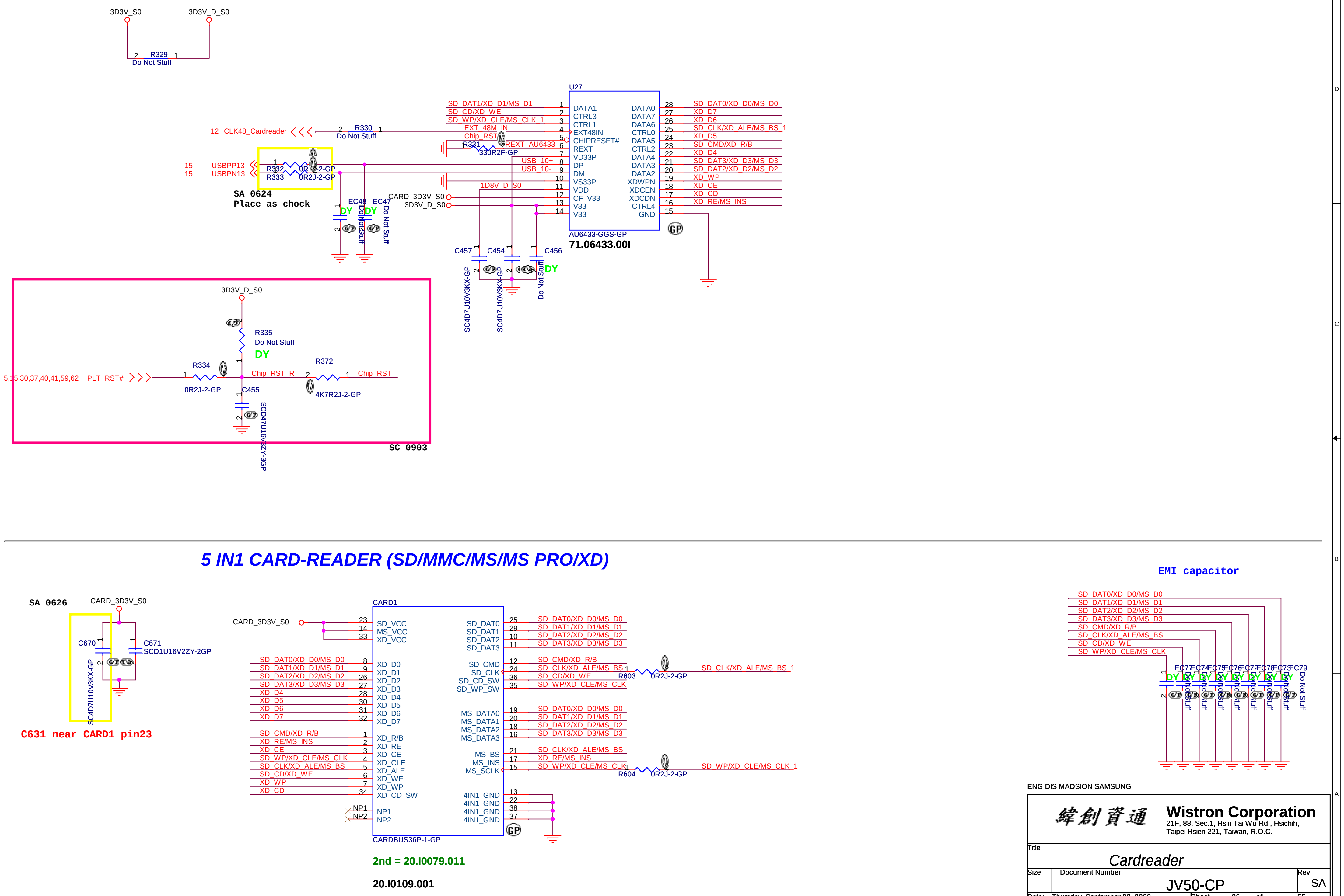
5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cardreader
Size
Document Number: JV50-CP
Rev: SA
Date: Thursday, September 03, 2009
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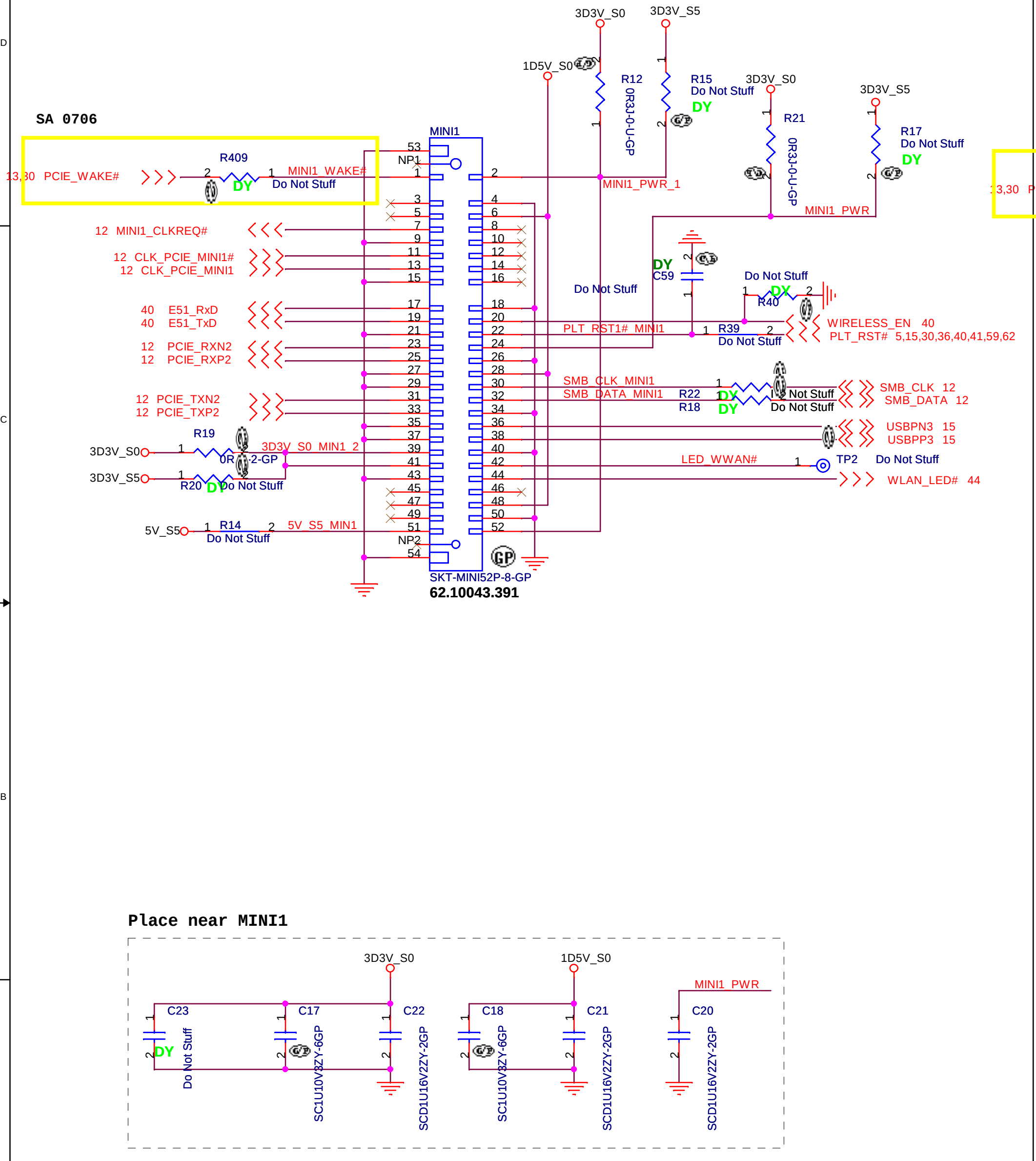
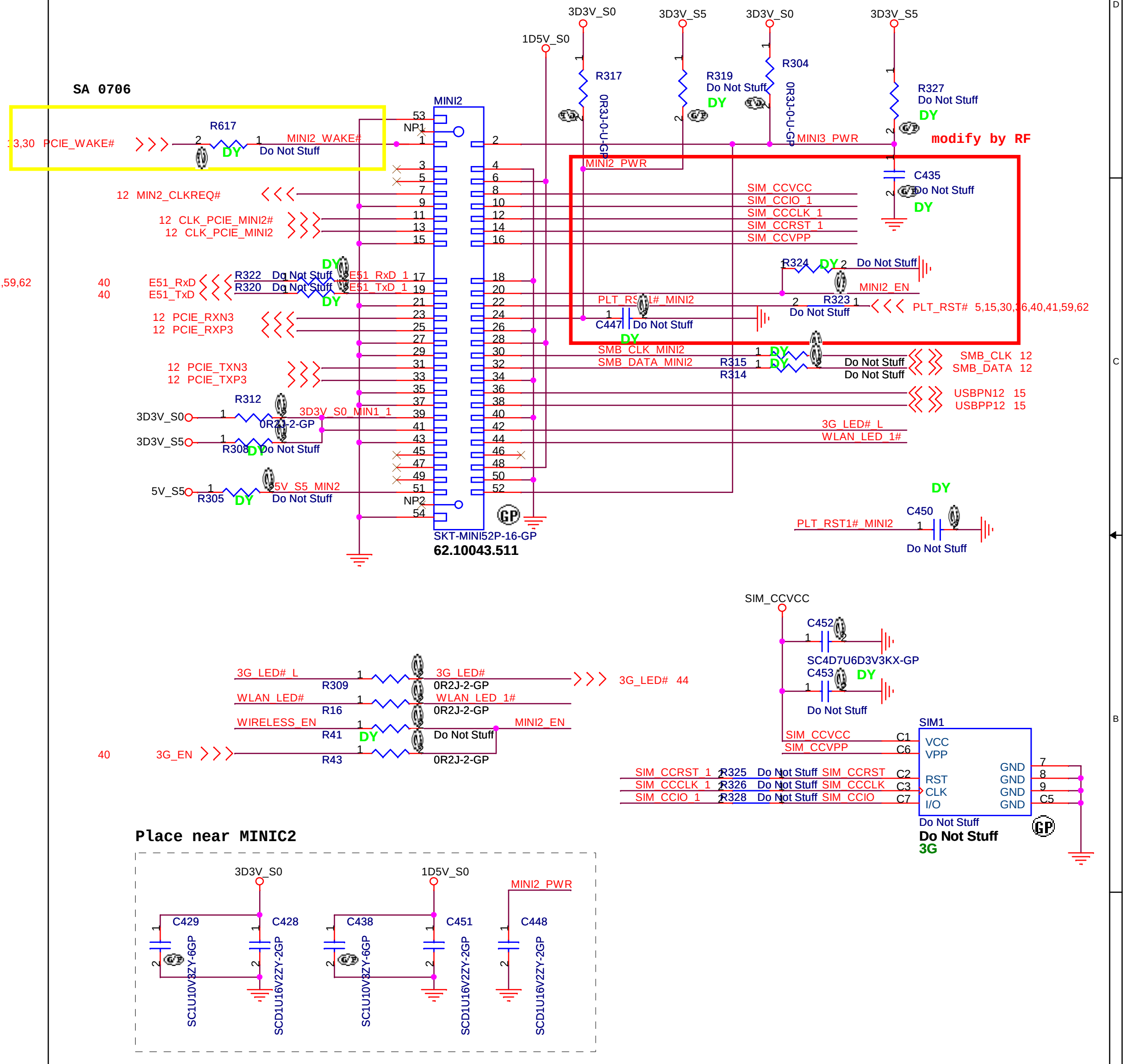
Mini Card Connector(WLAN)
Support debug-card



Mini Card Connector(Robson2 and 3G)



ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
MINI CARD

Size	Document Number	Rev
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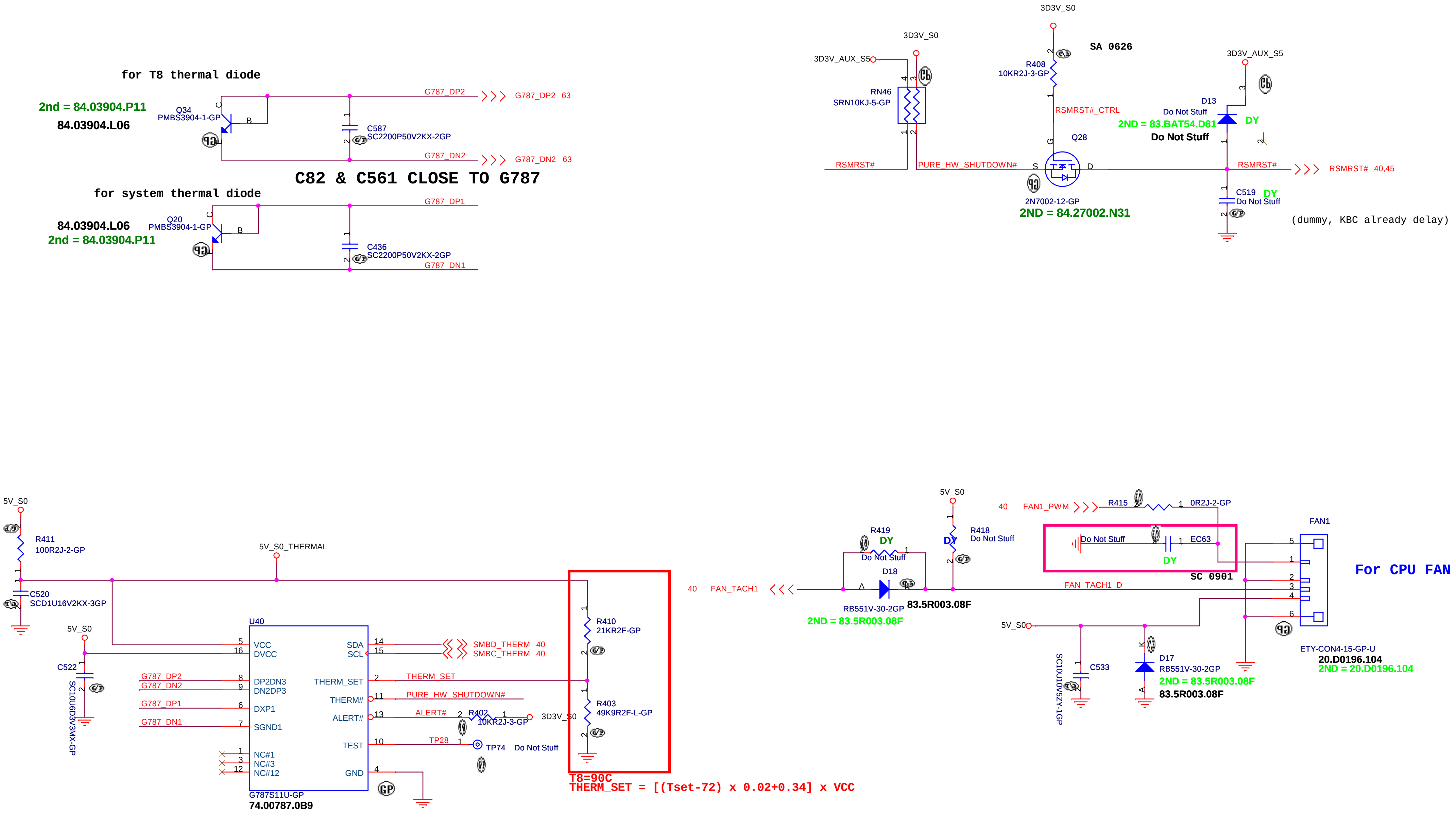

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Thermal/Fan_Connector

Size	Document Number	Rev
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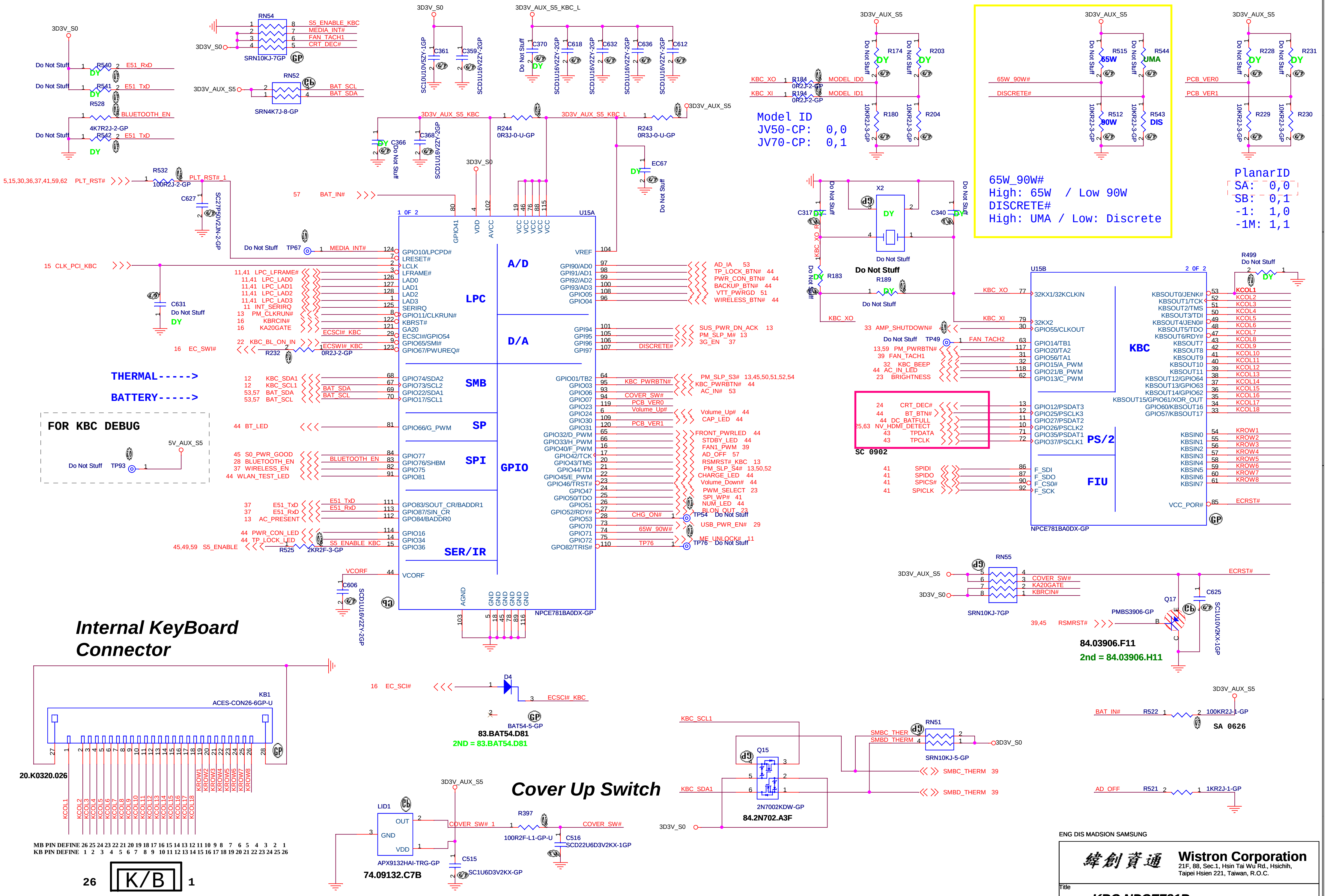

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
KBC NPCE781B

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JV50-CP
Rev SA

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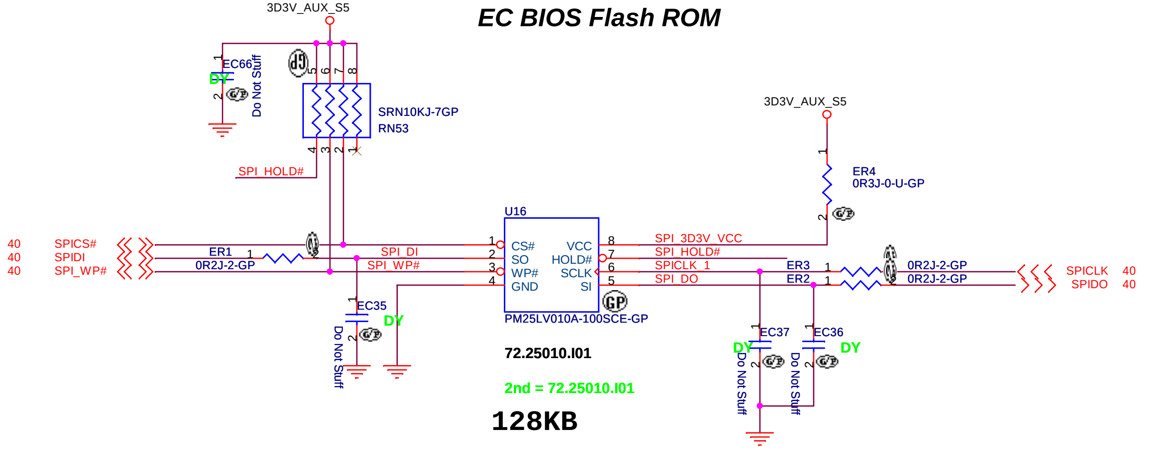
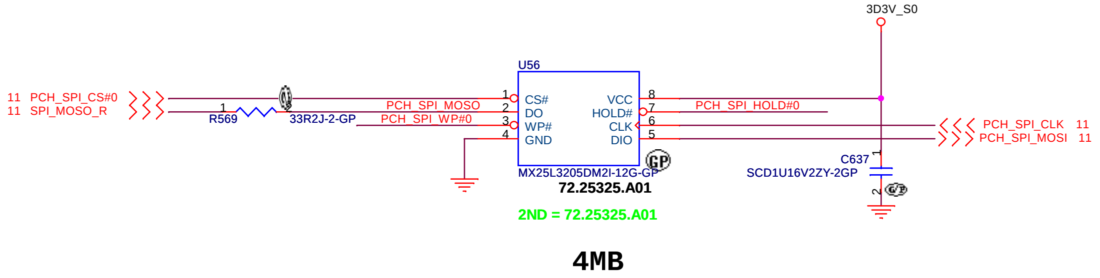
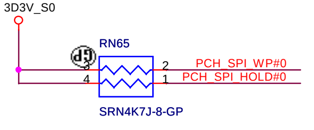
EC BIOS Flash ROM

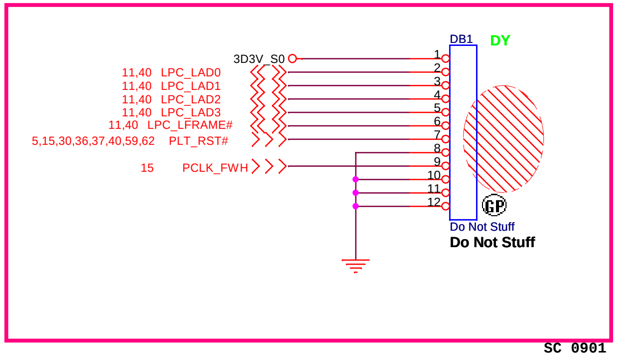


System BIOS Flash ROM





GOLDEN FINGER FOR DEBUG BOARD



SC 0901

ENG DIS MADSION SAMSUNG

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BIOS		
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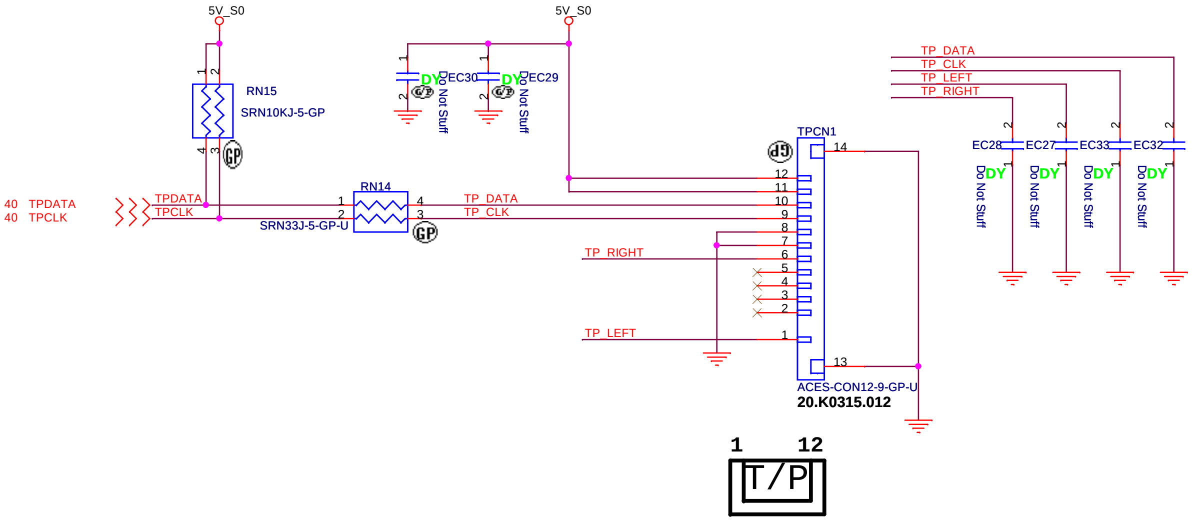
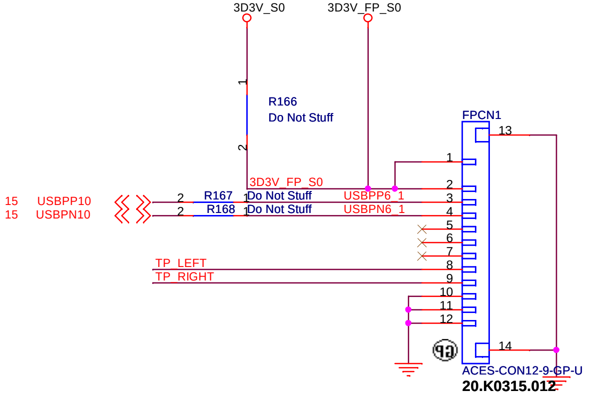
Date: Thursday, September 03, 2009	Sheet 41 of 57	

TOUCH PAD



Finger printer



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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Touch PAD and FP

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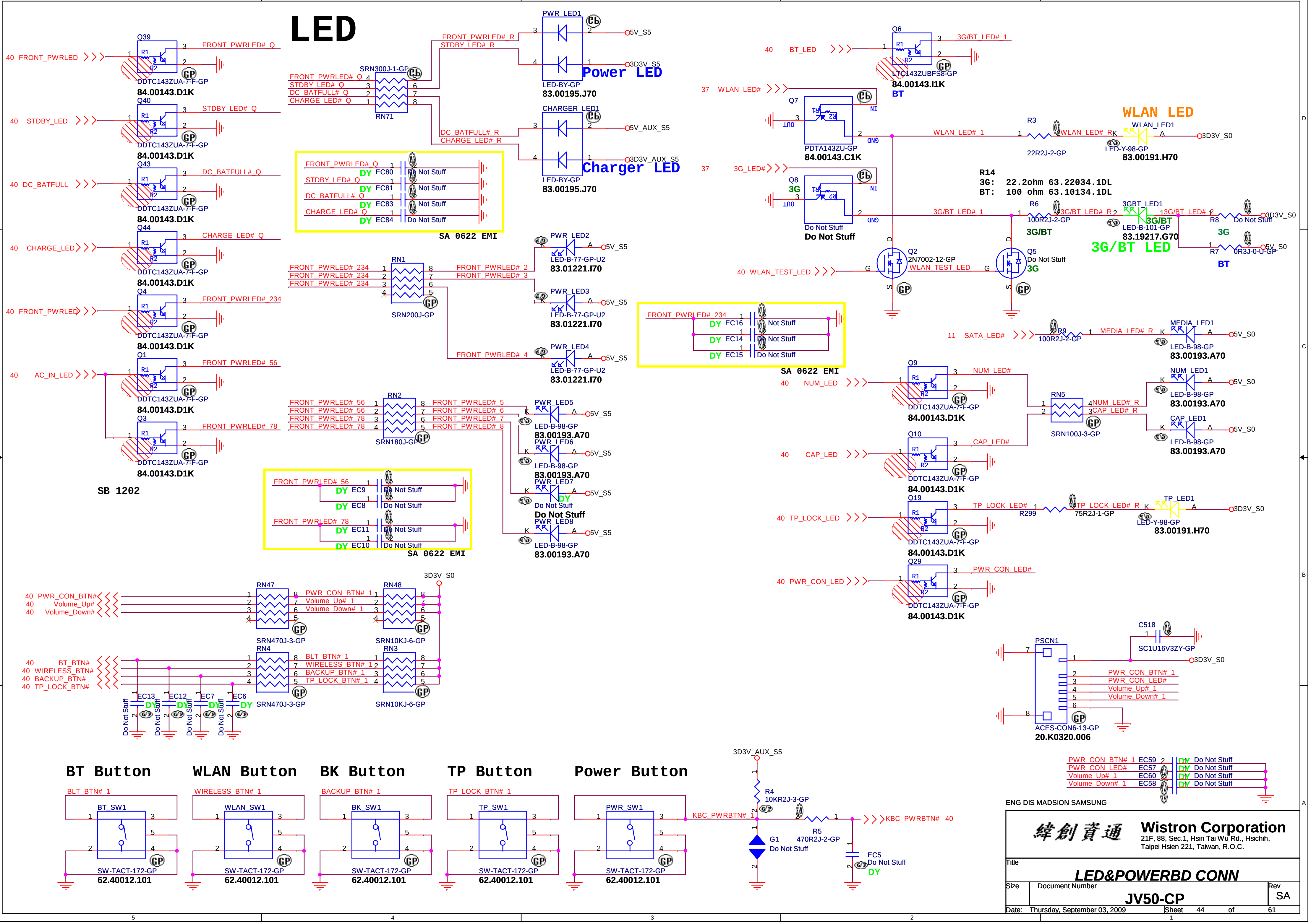
	JV50-CP	SA

Date: Thursday, September 03, 2009 Sheet 43 of 61

LED



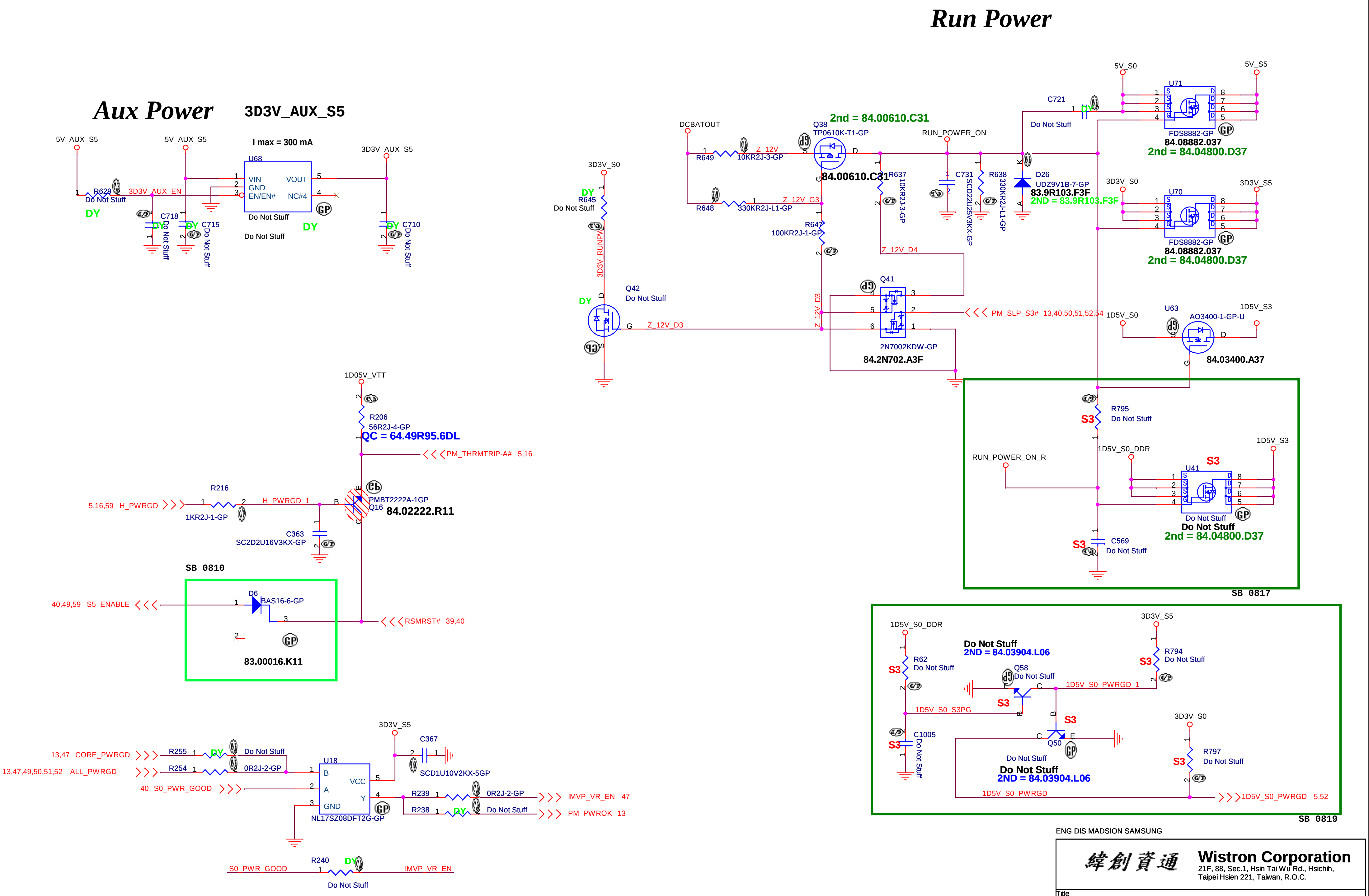
ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LED&POWERBD CONN**

Size | Document Number: **JV50-CP** | Rev: SA

Date: Thursday, September 03, 2009 | Sheet 44 of 61

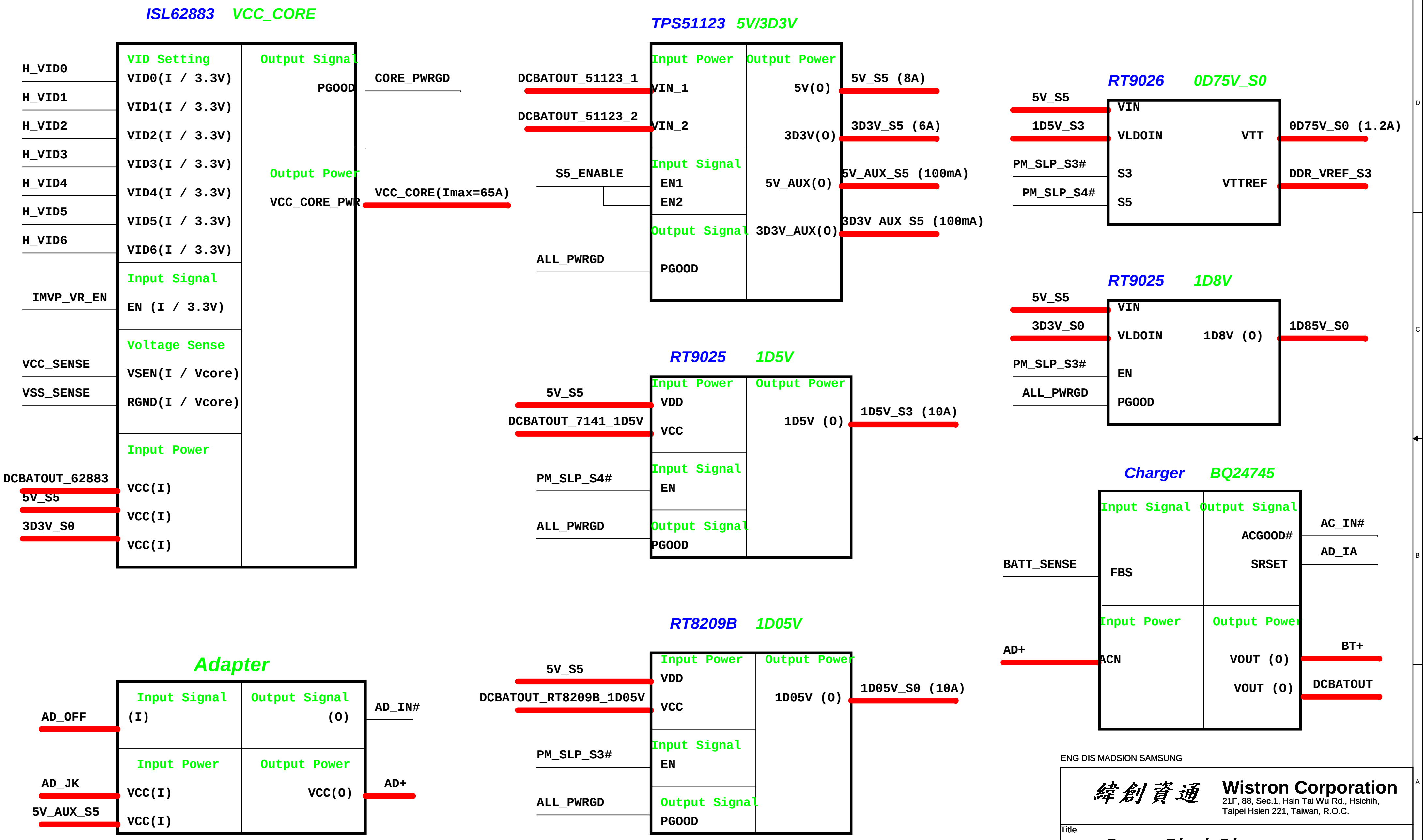


ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
	RUN POWER and 3D3V_AUX_S5	
Size	Document Number **JV50-CP**	Rev **SA**
Date: Thursday, September 03, 2009	Sheet 45 of 57	



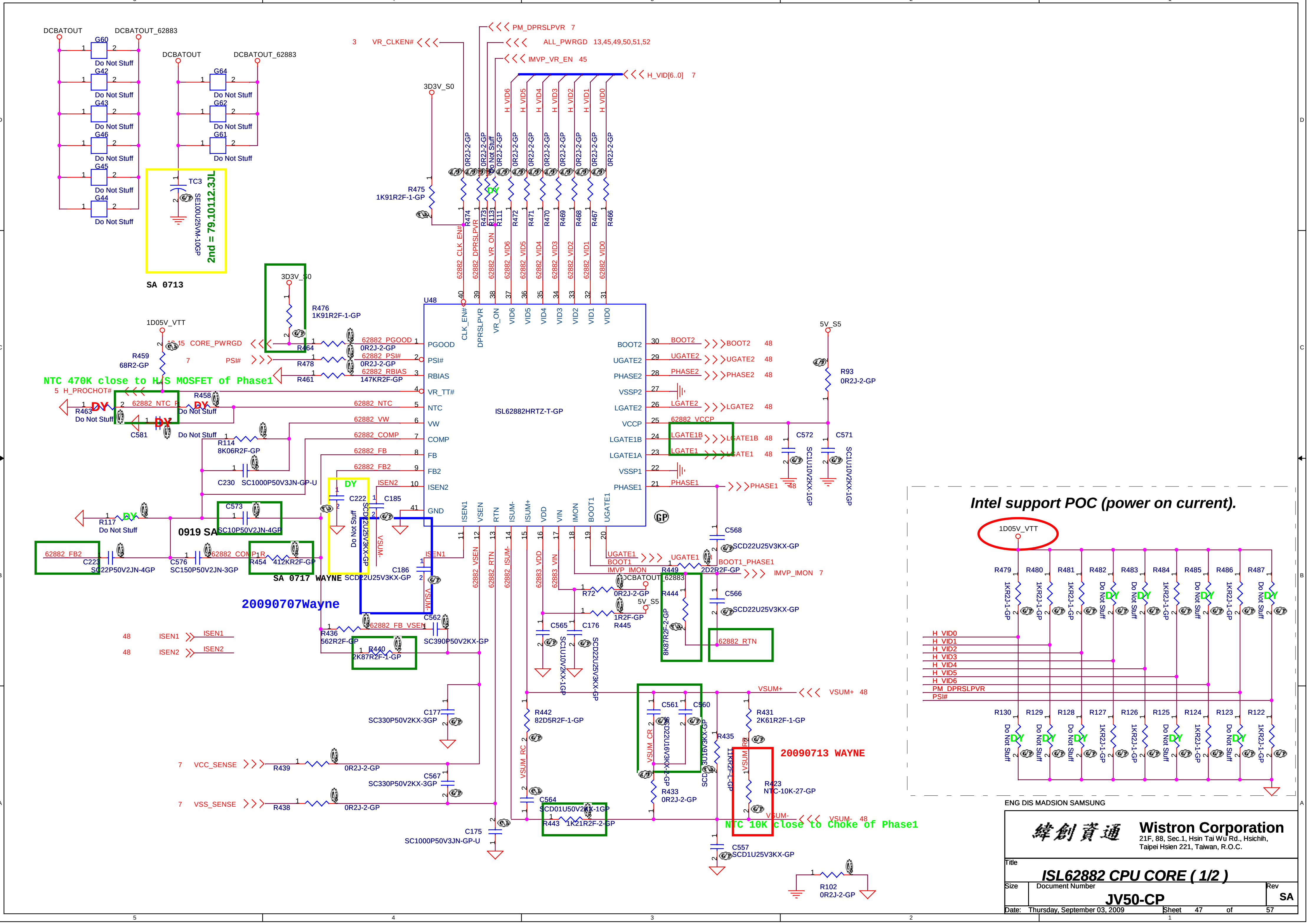
ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Power Block Diagram

Size Document Number Rev
JV50-CP SA

Date: Tuesday, August 18, 2009 Sheet 46 of 57



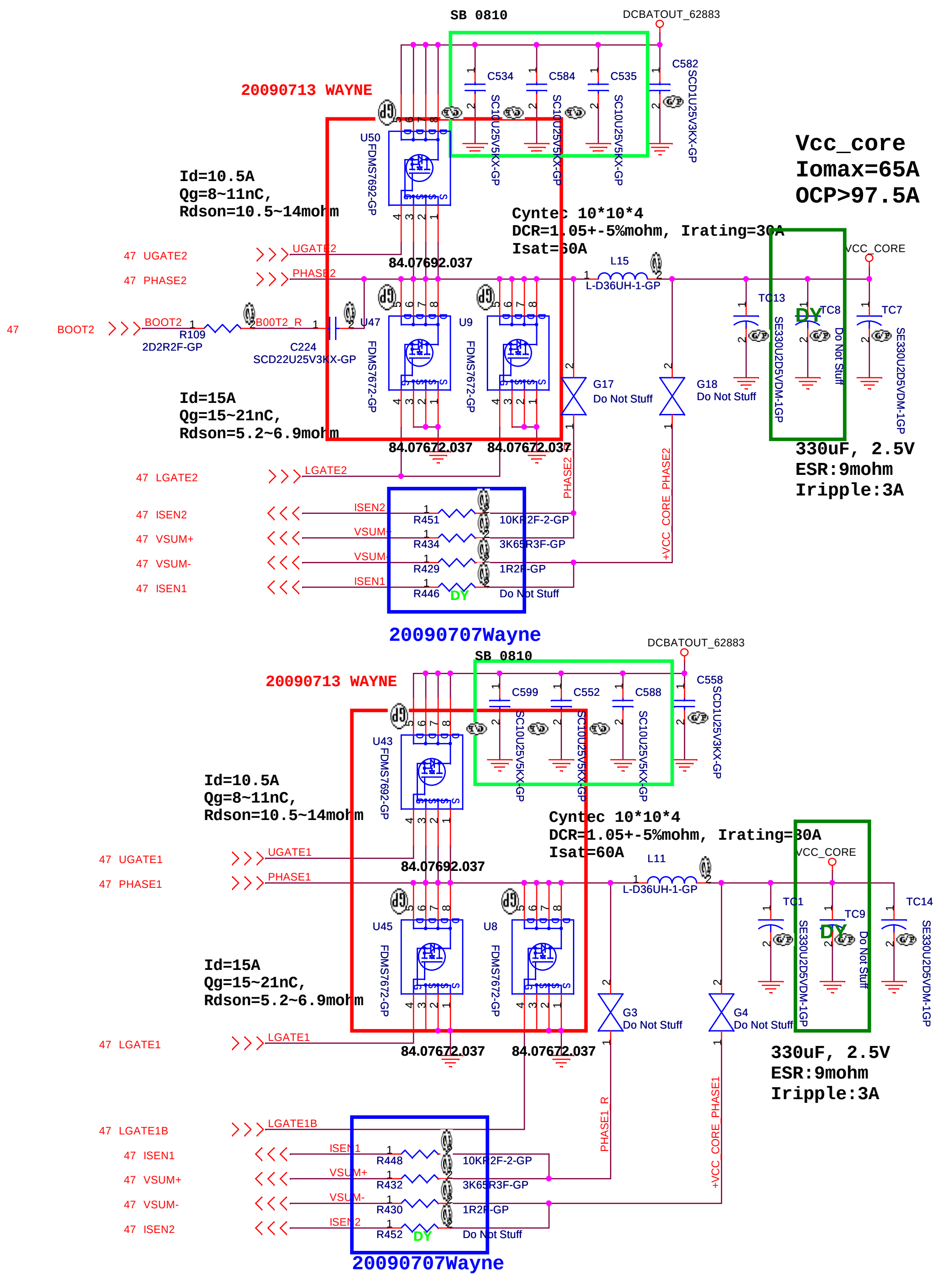
ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
ISL62882 CPU CORE (1/2)

Size	Document Number	Rev
	JV50-CP	SA

Date: Thursday, September 03, 2009 Sheet 47 of 57



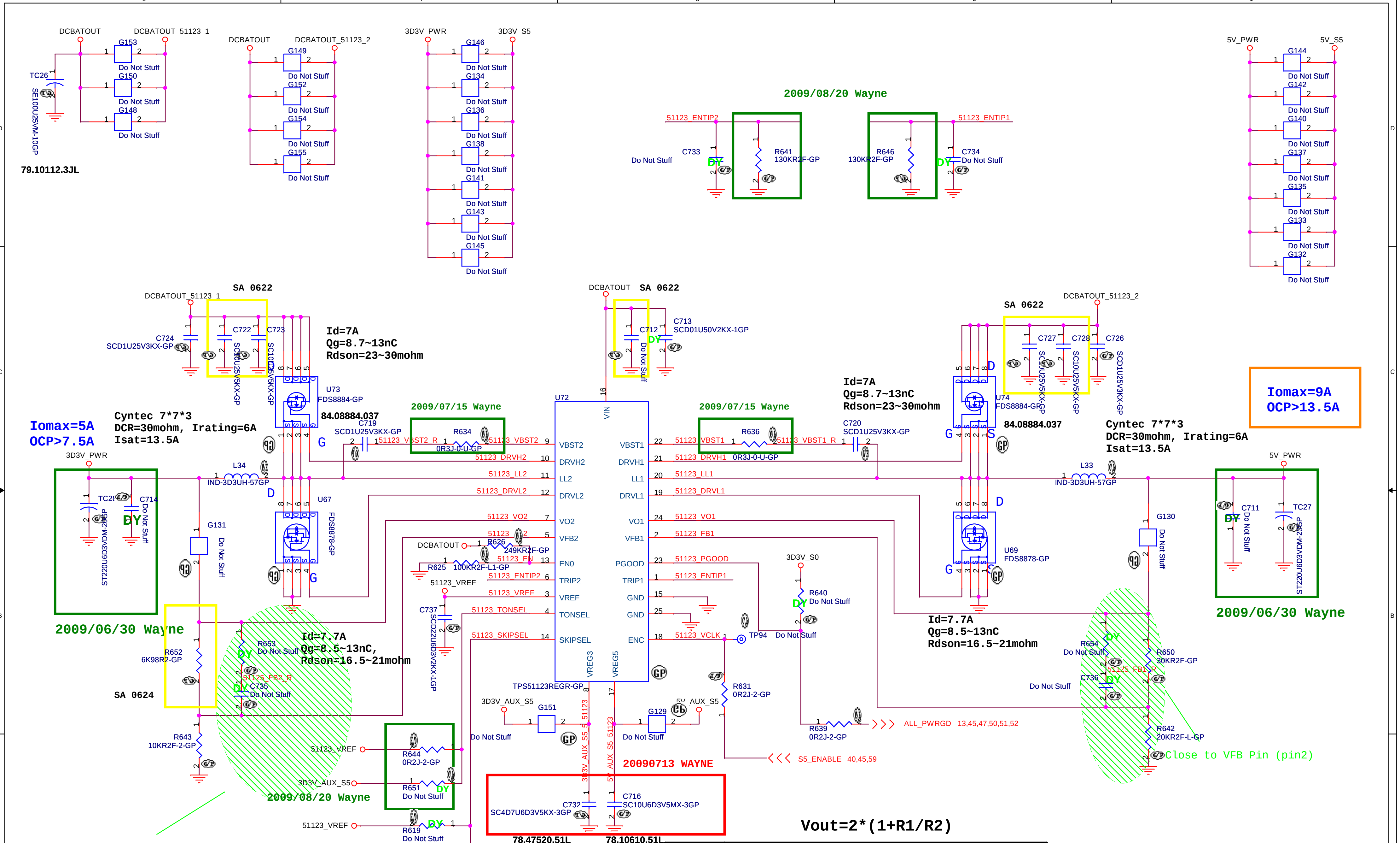
ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
ISL62882 CPU CORE (1/2)

Size Document Number **JV50-CP** Rev **SA**

Date: Thursday, September 03, 2009 Sheet 48 of 57



Vout=2*(1+R1/R2)

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
TPS51123 5V/3D3V

Size
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JV50-CP
Rev
SA

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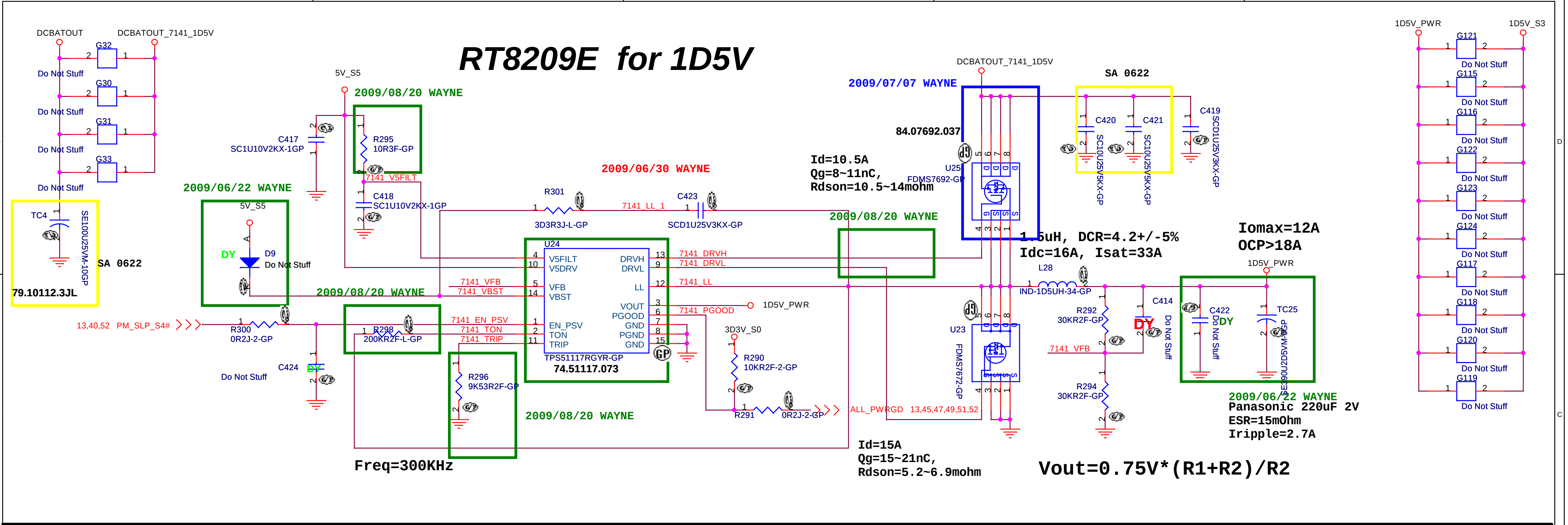
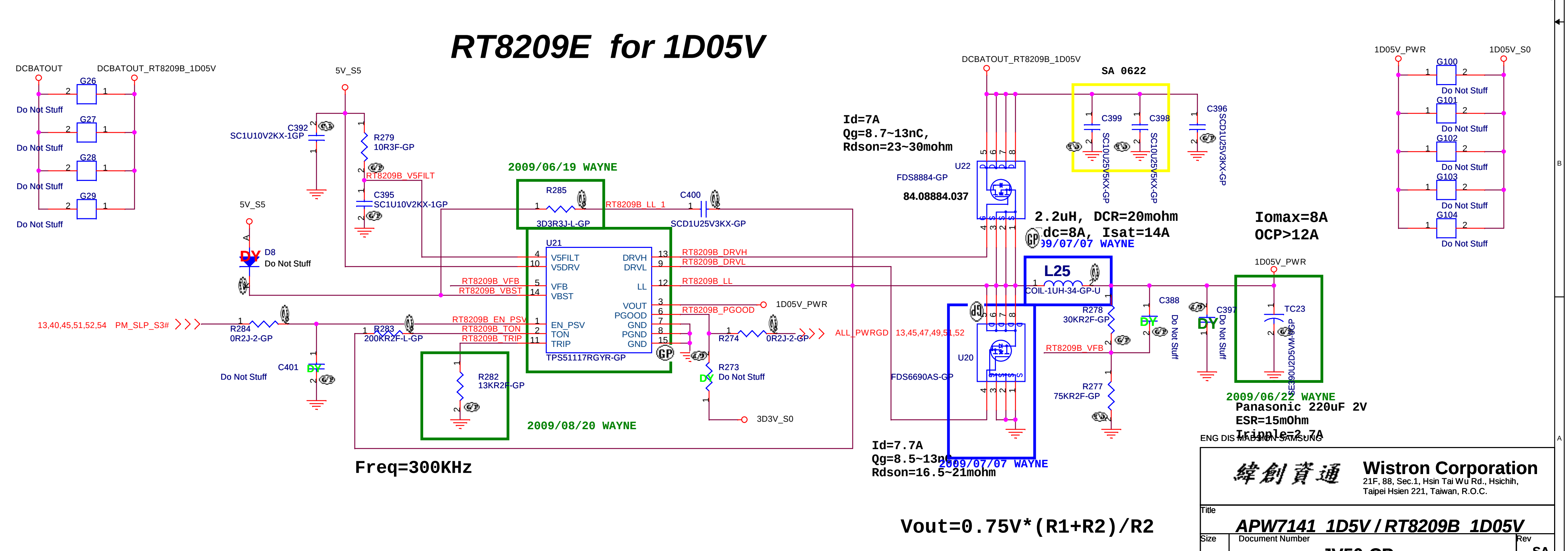
RT8209E for 1D5V



RT8209E for 1D05V



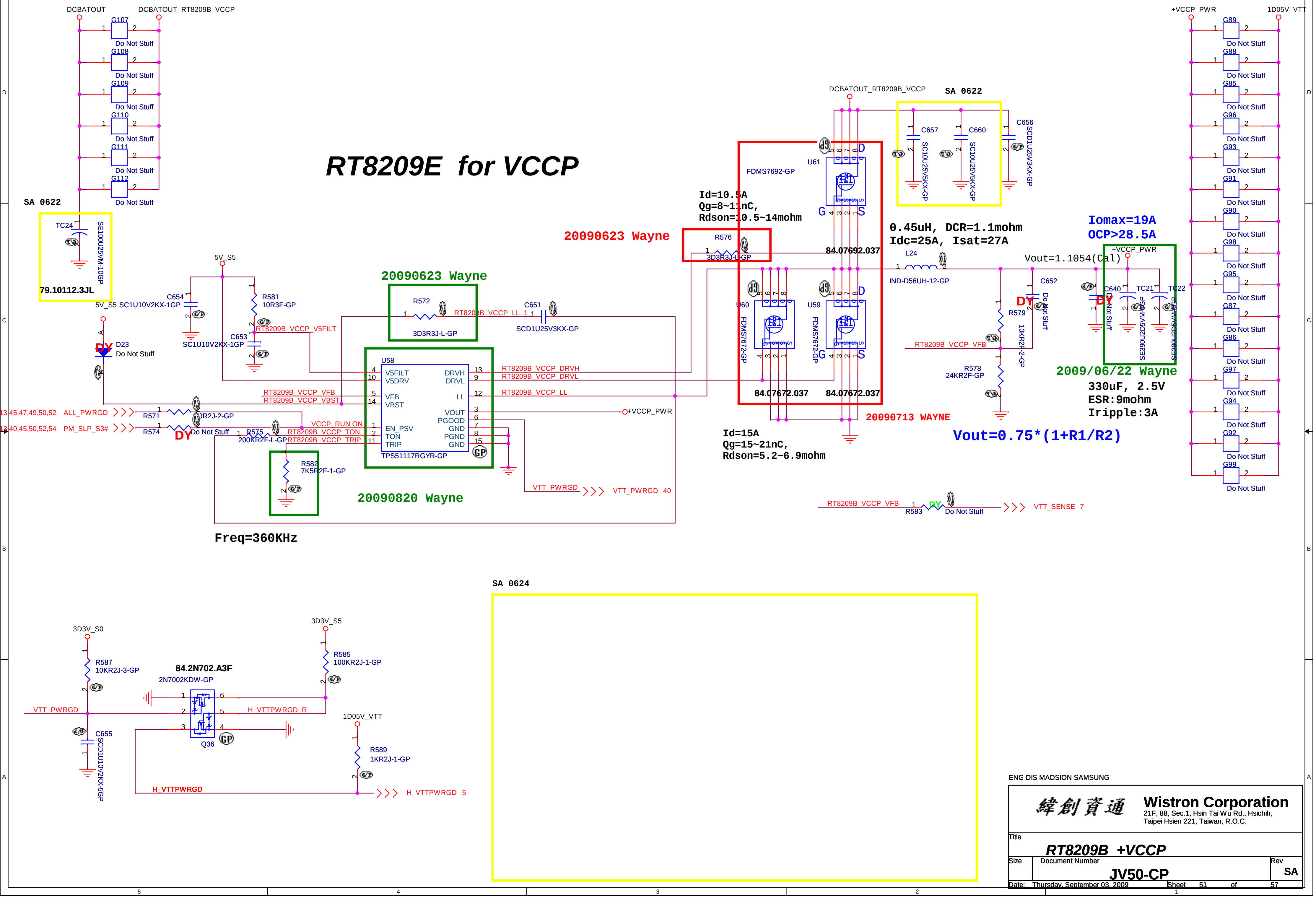
ENG DIS MADISON SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
APW7141 1D5V / RT8209B 1D05V

Size
Document Number
JV50-CP
Rev
SA

Date: Thursday, September 03, 2009
Sheet 50 of 57



ENG DIS MADSION SAMSUNG

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

RT8209B +VCCP

Size Document Number

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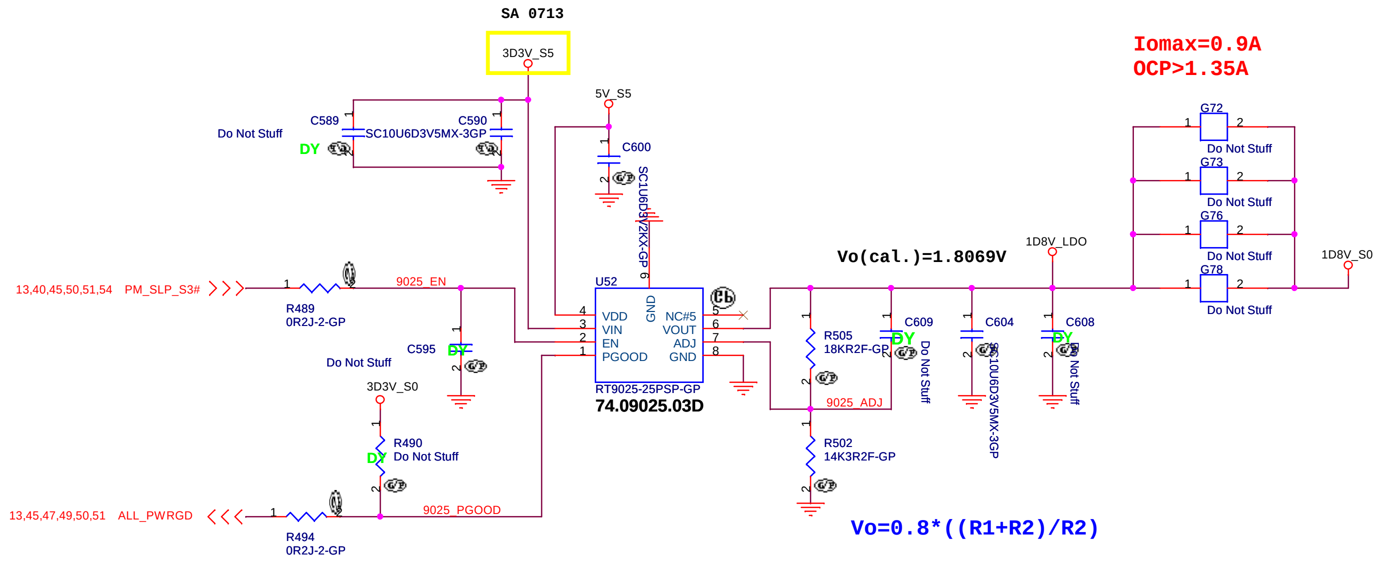
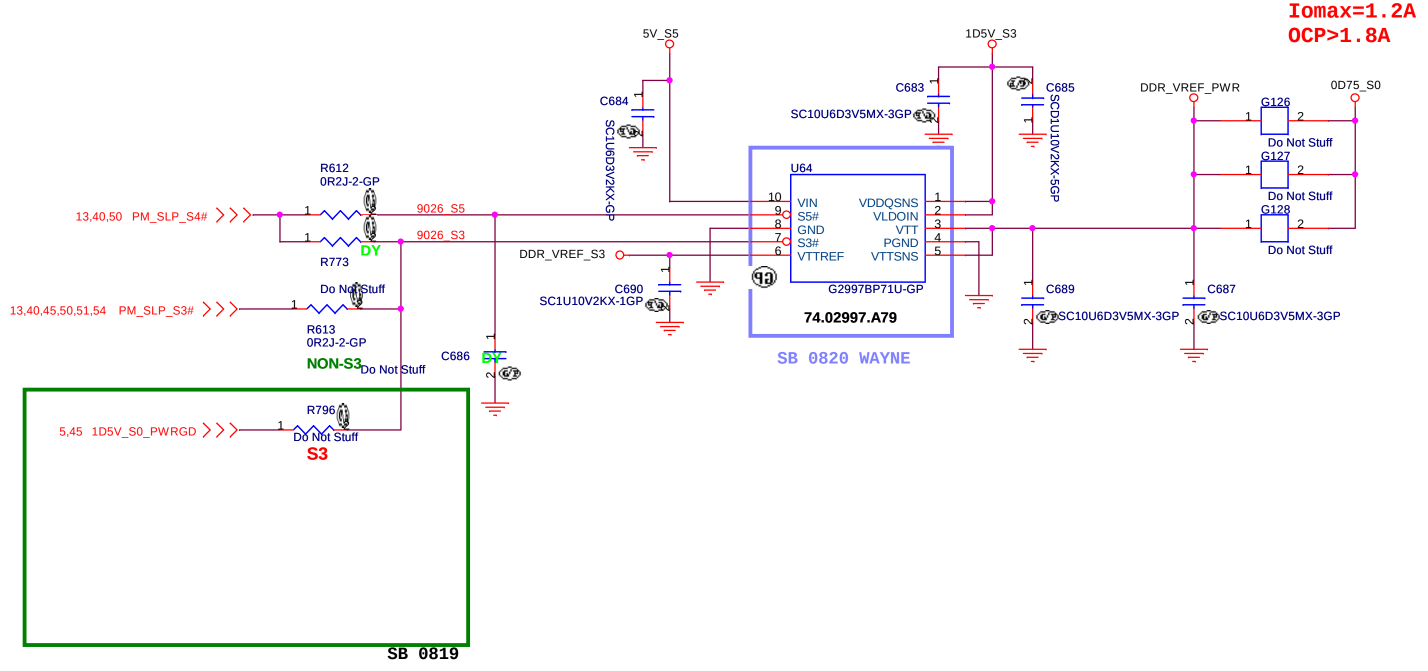
RT9025 for 1D8V_S0



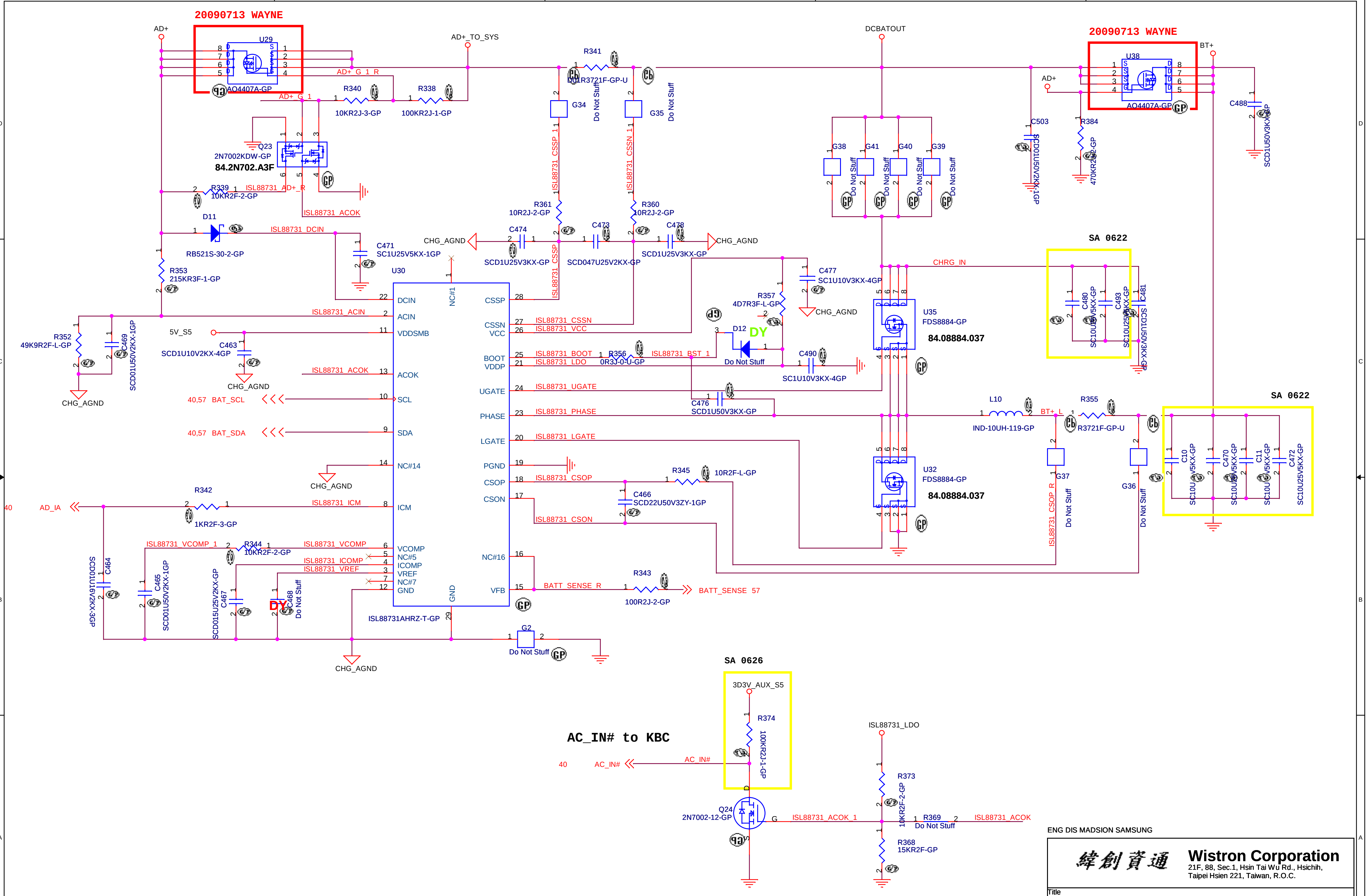
RT9026 for 0D75V_S3



ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
RT9025_1D8V/RT9026_0D75		
Size	Document Number JV50-CP	Rev SA
Date: Thursday, September 03, 2009	Sheet 52 of 57	



ENG DIS MADSION SAMSUNG

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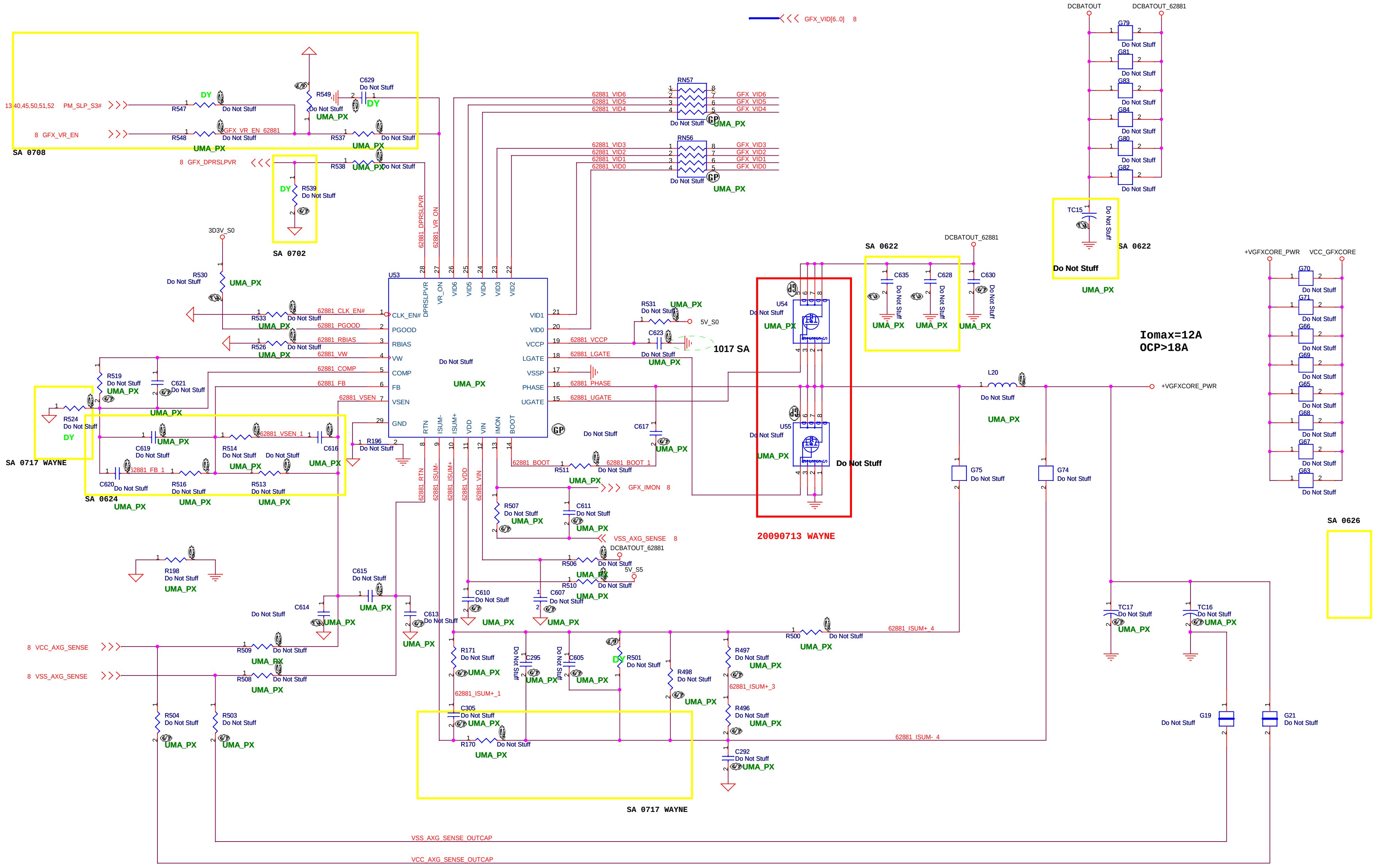
Taipei Hsien 221, Taiwan, R.O.C.

Title
ISL88731A CHARGER

Size | Document Number **JV50-CP** | Rev **SA**

Date: Thursday, September 03, 2009 | Sheet 53 of 57



ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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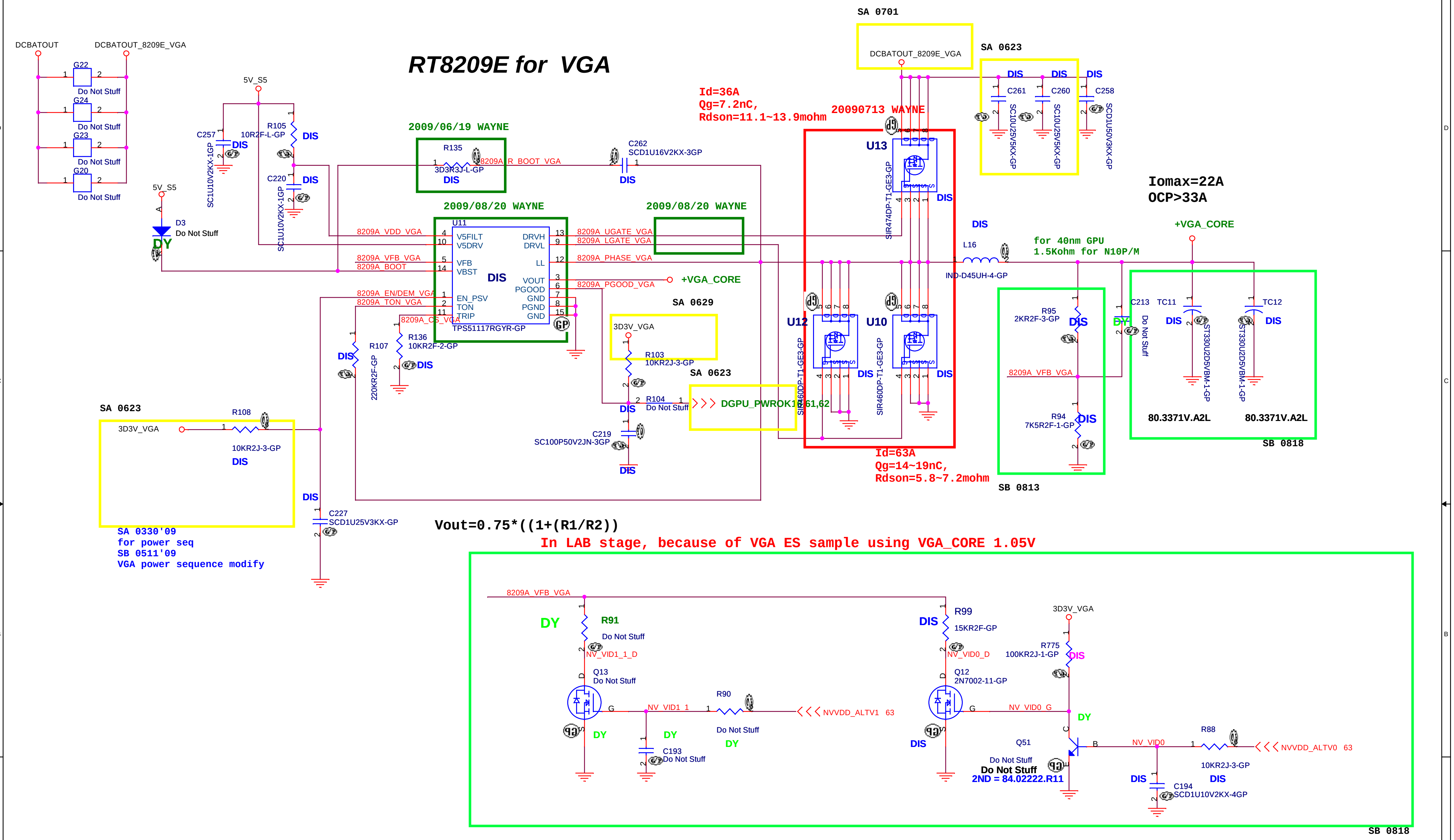
Title
ISL62881_+VCC_GFXCORE

Size C
Document Number
JV50-CP
Rev **SB**

Date: Thursday, September 03, 2009 Sheet 54 of 45



Vout=0.75*((1+(R1/R2))

In LAB stage, because of VGA ES sample using VGA_CORE 1.05V

	I/O	Inter Pull Low	GPIO TABLE	
NVVDD_ALTV0	O	YES	GPU VOLTAGE GPU VOLTAGE	L: 1.05V H: 0.95V

ENG DIS MADSION SAMSUNG

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Taipei Hsien 221, Taiwan, R.O.C.

Title
RT8209E VGA CORE

Size A3
Document Number
JV50-CP
Rev

Date: Thursday, September 03, 2009
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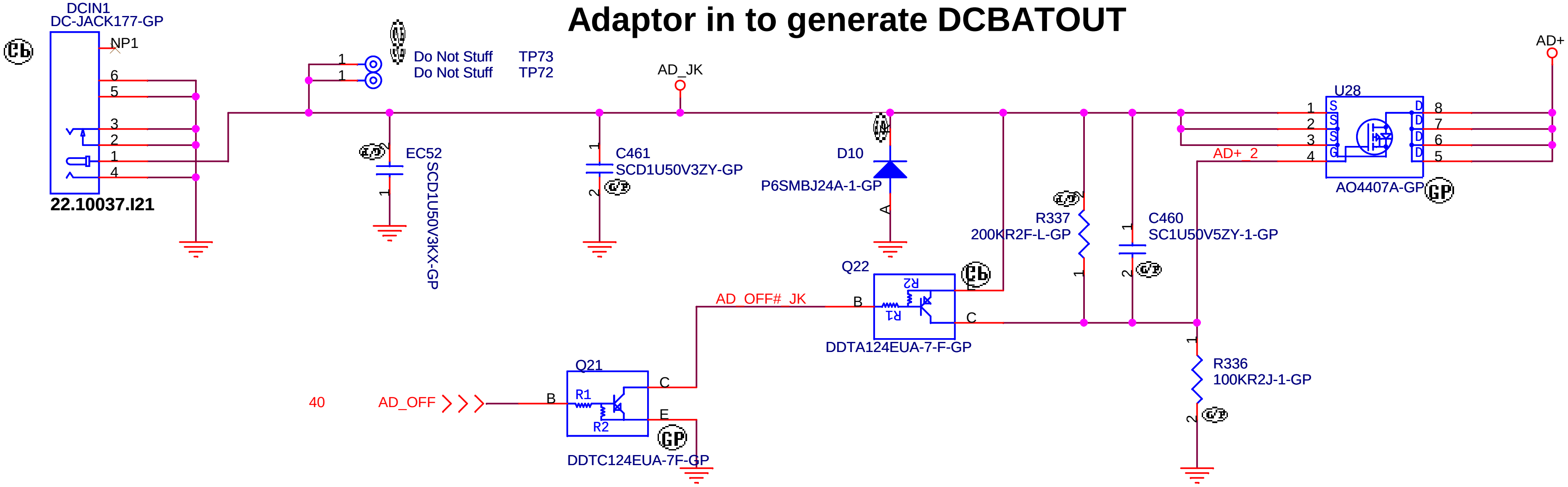
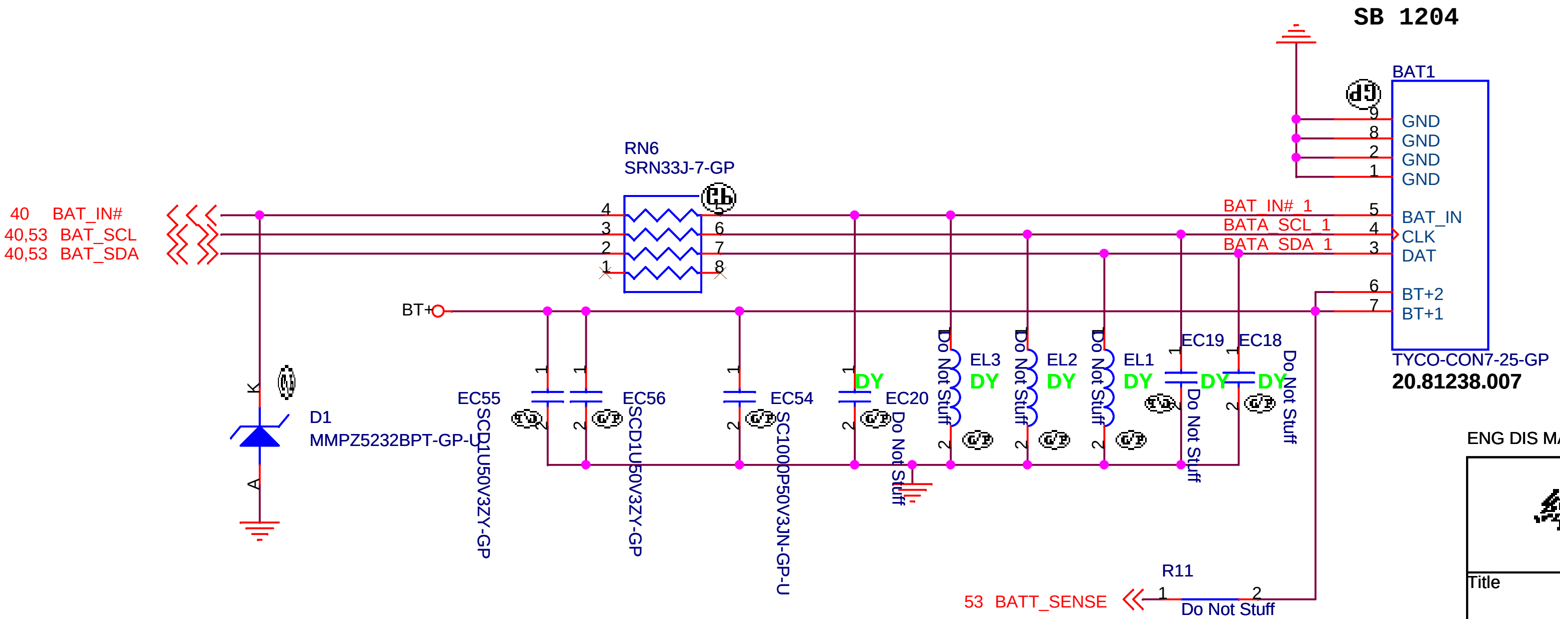
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



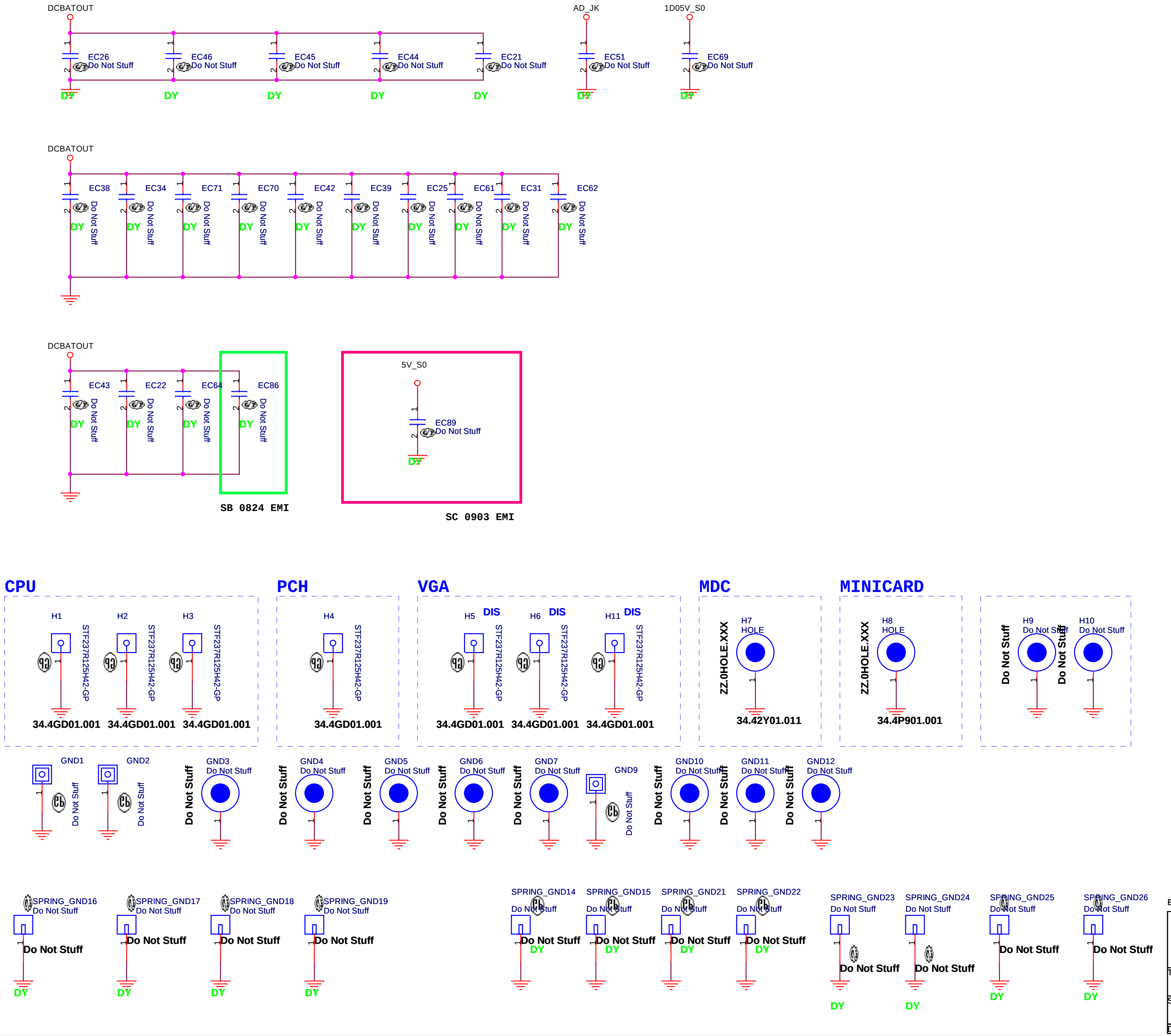
ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
AD/BATT CONN

Size
Document Number
JV50-CP
Rev
SA

Date: Thursday, September 03, 2009 Sheet 57 of 61



ENG DIS MADSION SAMSUNG

緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
EMI/Spring/Boss

Size	Document Number	Rev
	JV50-CP	SA

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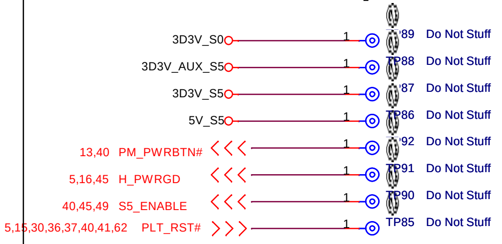
Check test point



Test Point放在Dimm Door打開可量測處

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
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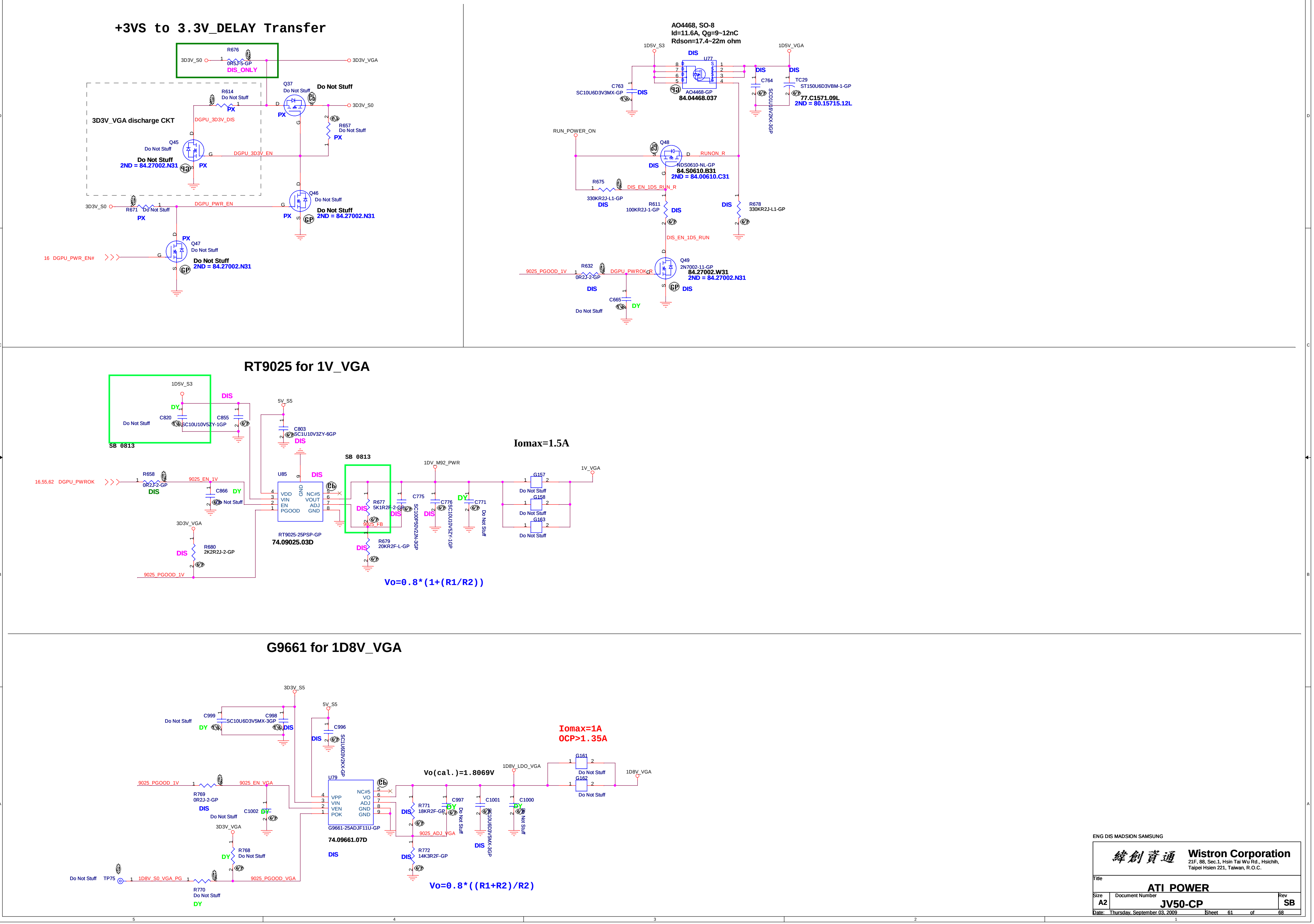
Taipei Hsien 221, Taiwan, R.O.C.

Title
AFTE TP

Size	Document Number	Rev
	JV50-CP	**SA**

Date: Thursday, September 03, 2009 Sheet 59 of 57



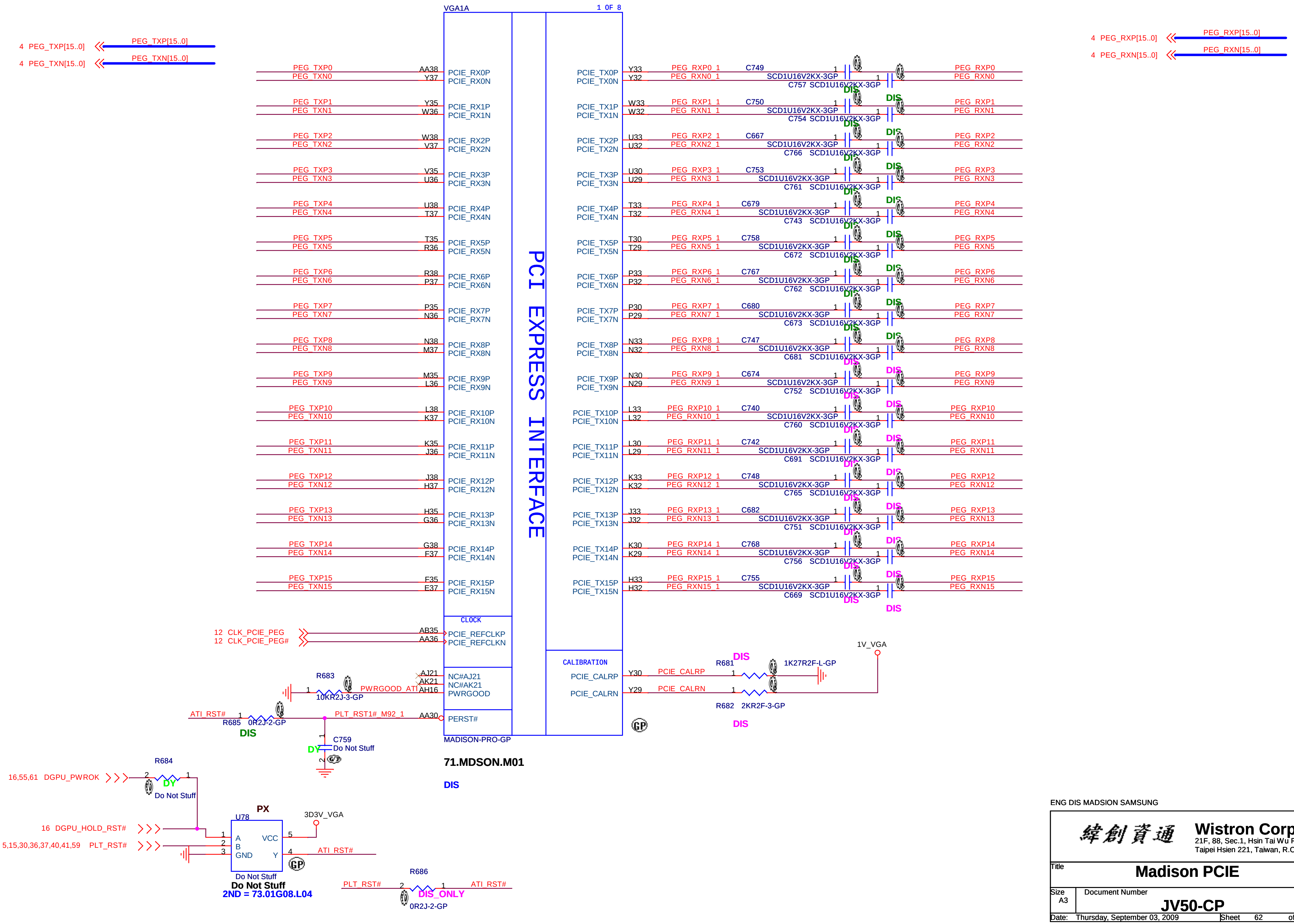
ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
ATI_POWER

Size A2 Document Number **JV50-CP** Rev **SB**

Date: Thursday, September 03, 2009 Sheet 61 of 68



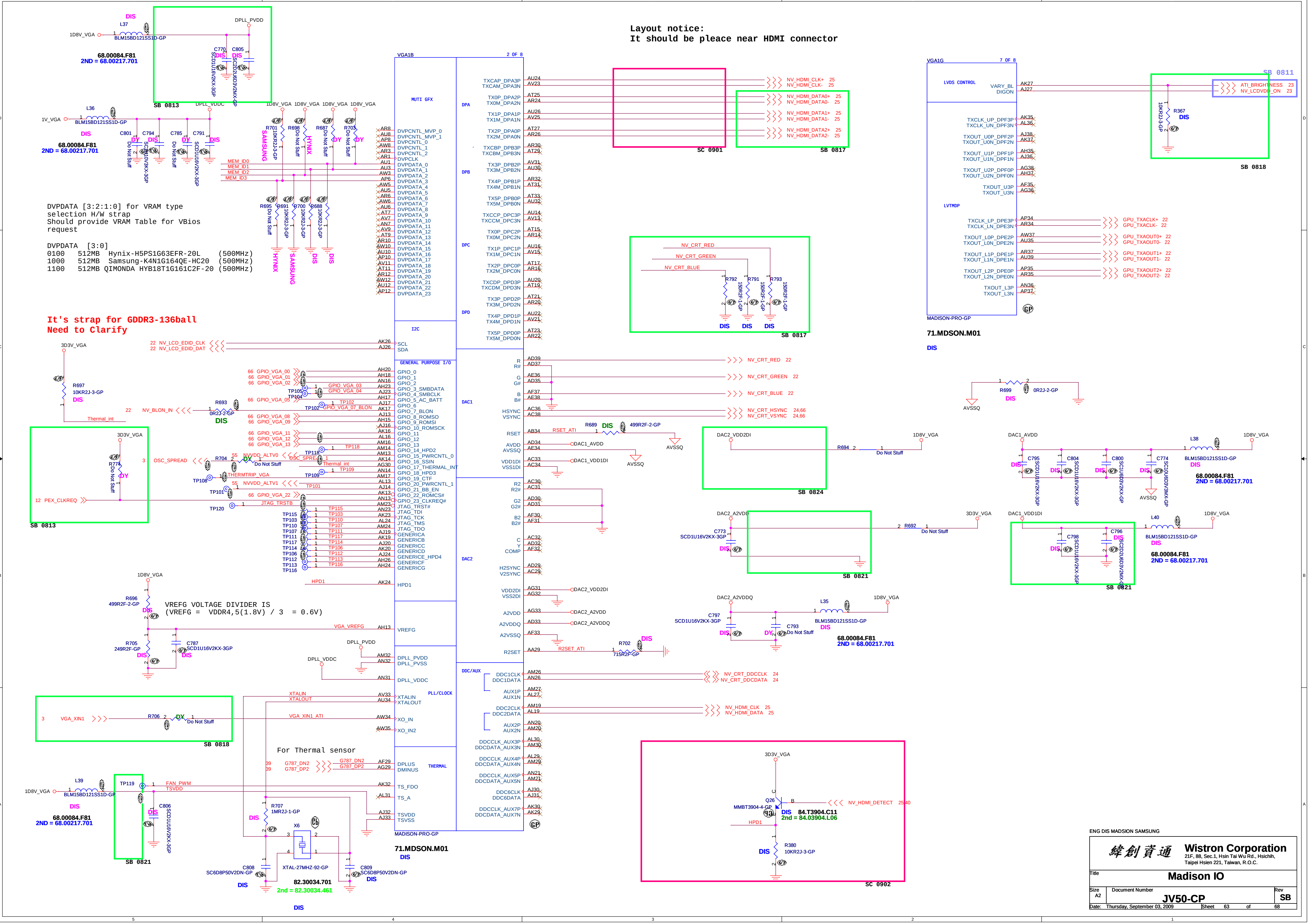
ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Madison PCIE**

Size A3 | Document Number **JV50-CP** | Rev **SB**

Date: Thursday, September 03, 2009 | Sheet 62 of 68



Layout notice:
It should be pleace near HDMI connector

DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request

DVPDATA	[3:0]		
0100	512MB	Hynix-H5PS1G63EFR-20L	(500MHz)
1000	512MB	Samsung-K4N1G164QE-HC20	(500MHz)
1100	512MB	QIMONDA HYB18T1G161C2F-20	(500MHz)

It's strap for GDDR3-136ball
Need to Clarify

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

For Thermal sensor

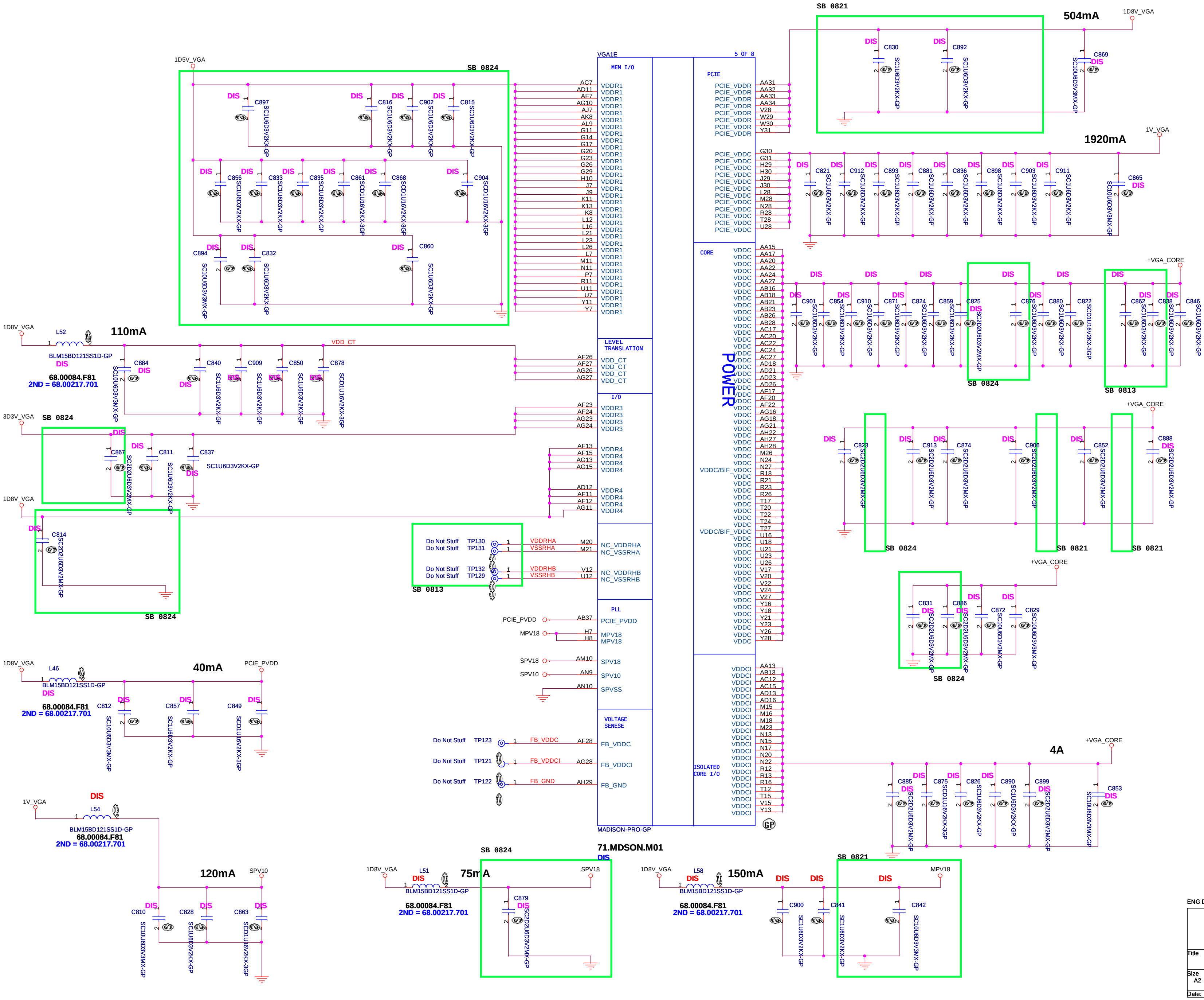
ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Madison IO**

Size: A2 | Document Number: **JV50-CP** | Rev: **SB**

Date: Thursday, September 03, 2009 | Sheet 63 of 68



ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Madison POWER**

Size A2
Document Number **JV50-CP**
Rev **SB**
Date: Wednesday, August 26, 2009
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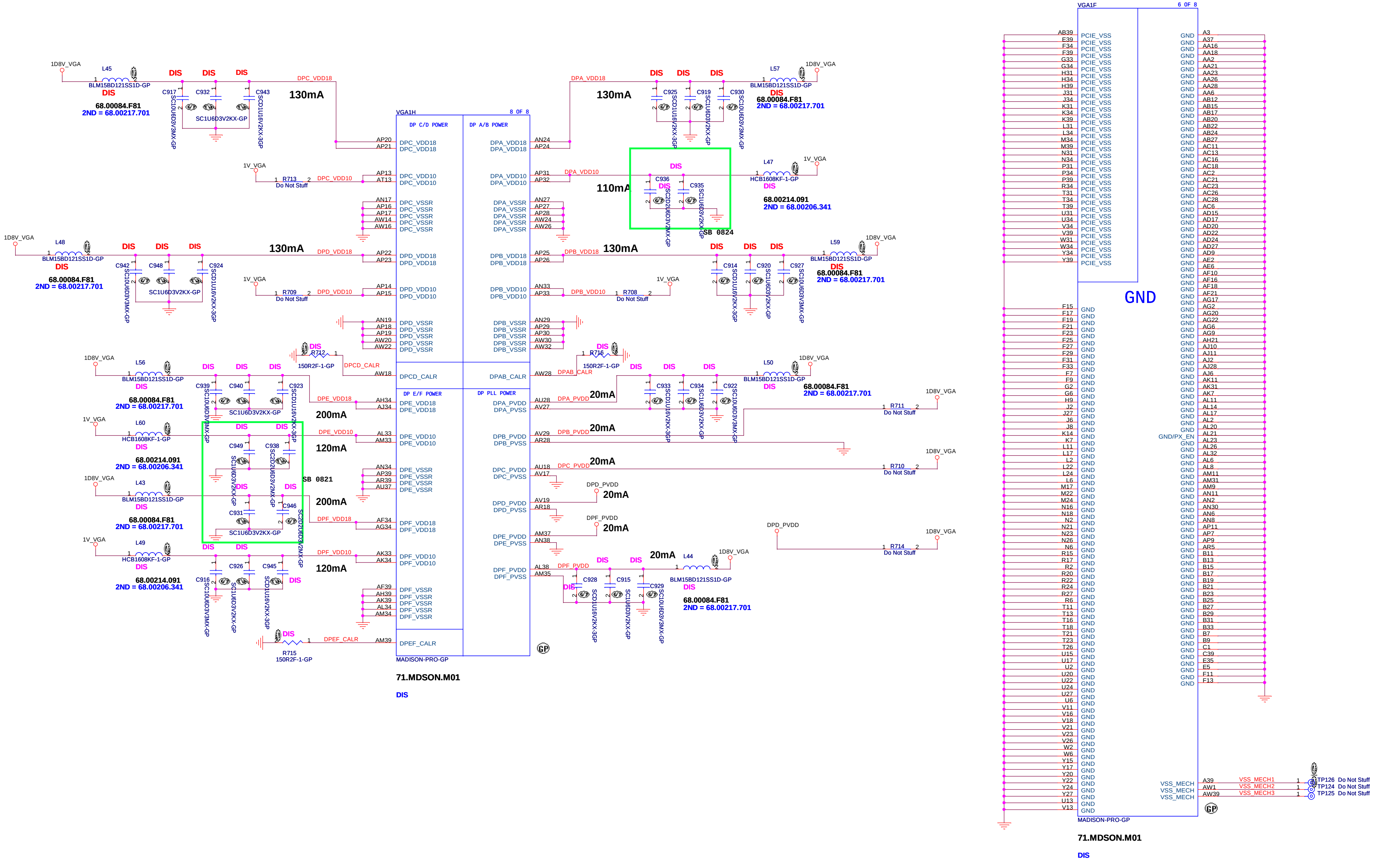


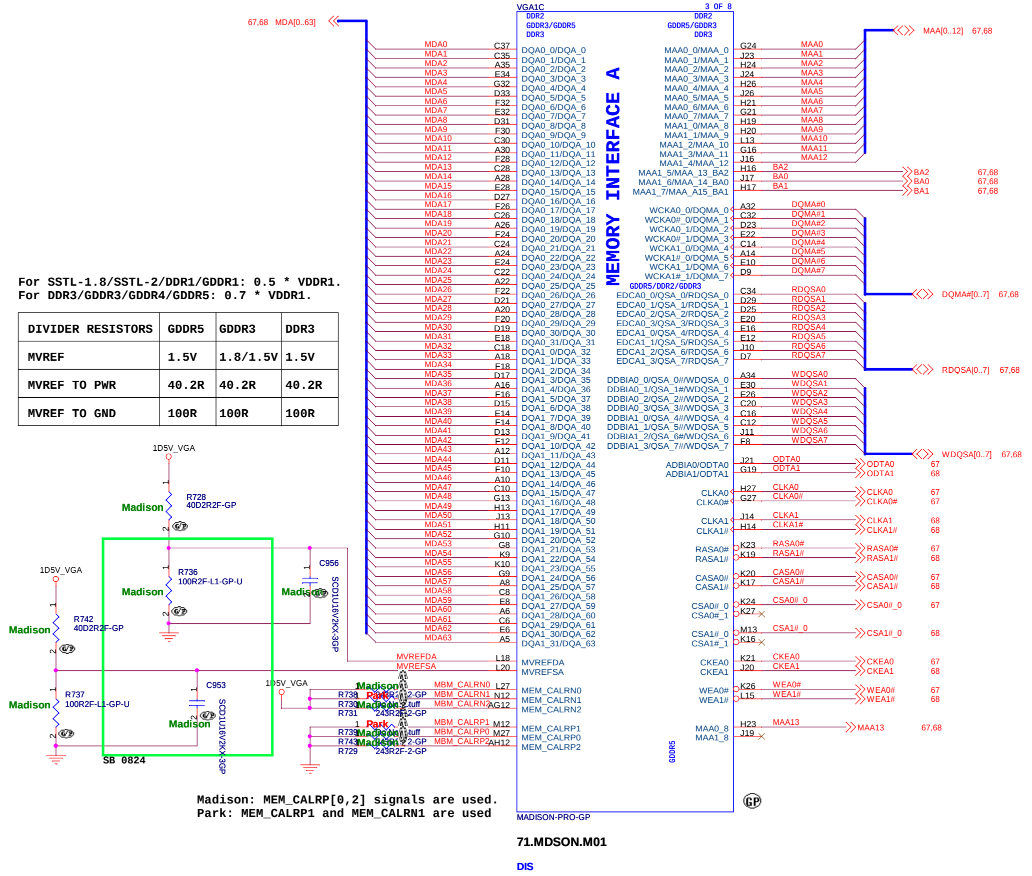
ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DP POWER_GND**

Size: A2
Document Number: **JV50-CP**
Rev: **SB**

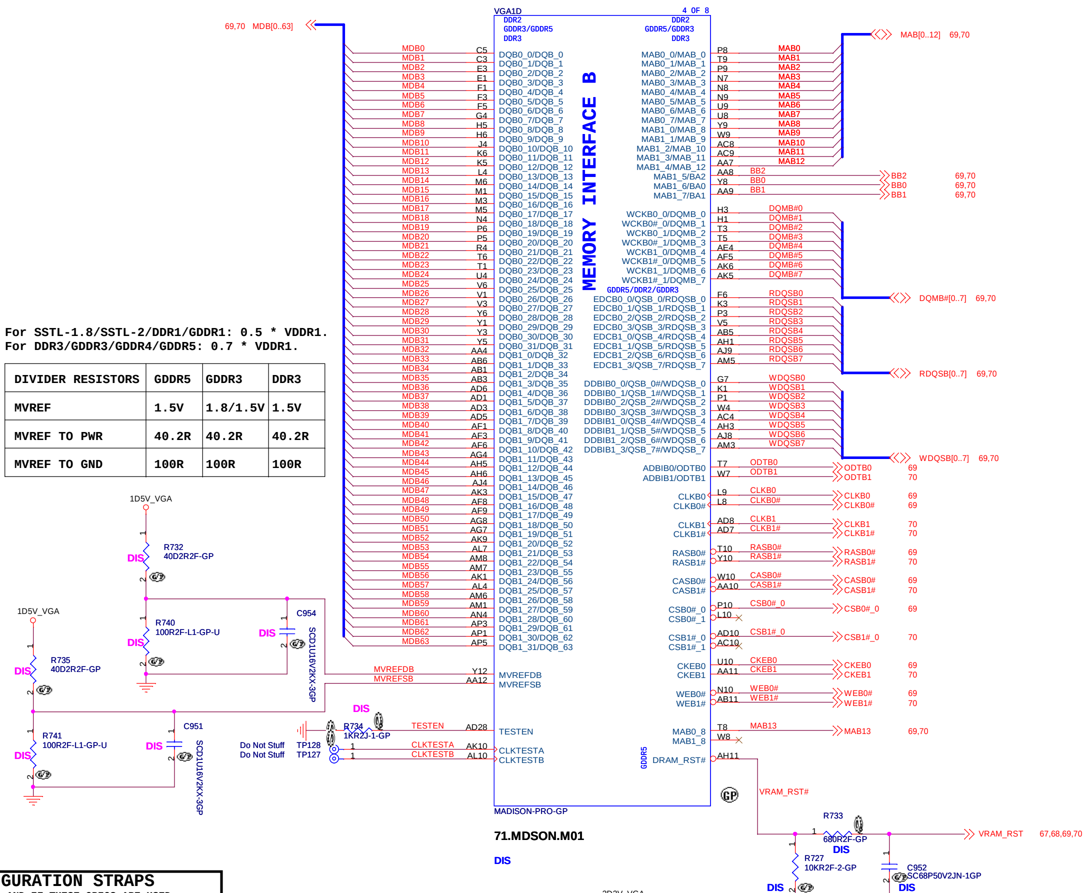
Date: Wednesday, August 26, 2009
Sheet 65 of 68



For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

Madison: MEM_CALRP[0,2] signals are used.
Park: MEM_CALRP1 and MEM_CALRN1 are used



For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

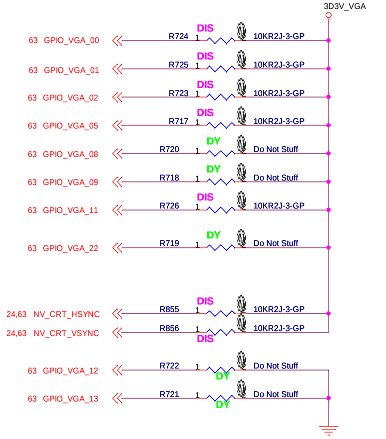
STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED,
THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB 256MB 64MB 32MB 512MB 1GB 2GB 4GB	x000 x001 x010 x x x x x	ST Microelectronics	M25P05A M25P10A M25P20 M25P40 M25P80	0100 0101 0101 0101 0101
		Chingis (formerly PMC)	Pm25LV512A Pm25LV010A	0100 0101



Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
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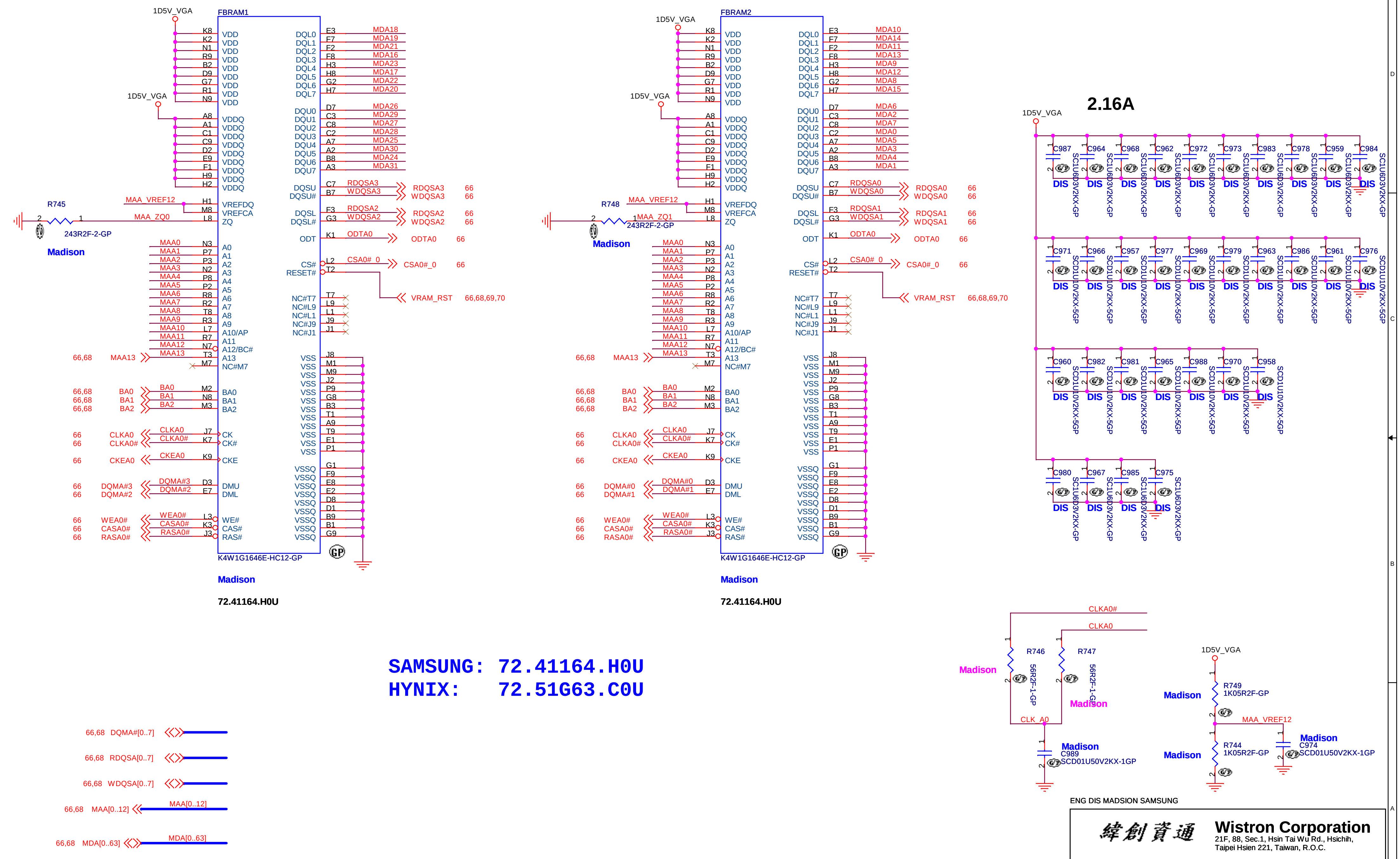
Title **Madison Memory / Straps**

Size A2 Document Number **JV50-CP** Rev **SB**

Date: Thursday, September 03, 2009 Sheet 66 of 68

DDR3



SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM(1/4)

Size	Document Number	Rev
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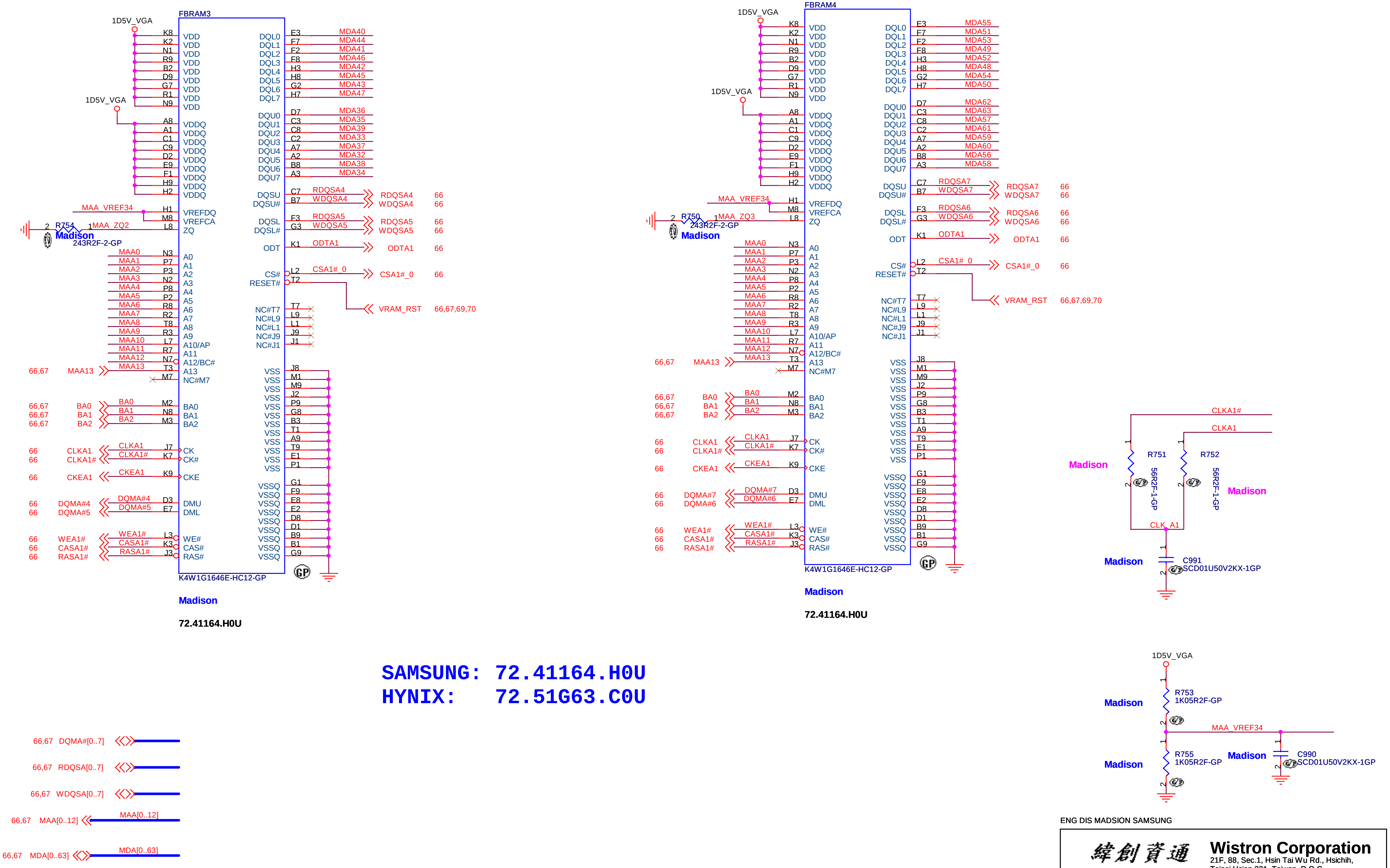
Date: Thursday, September 03, 2009 Sheet 67 of 68

DDR3



SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

緯創資通 **Wistron Corporation**
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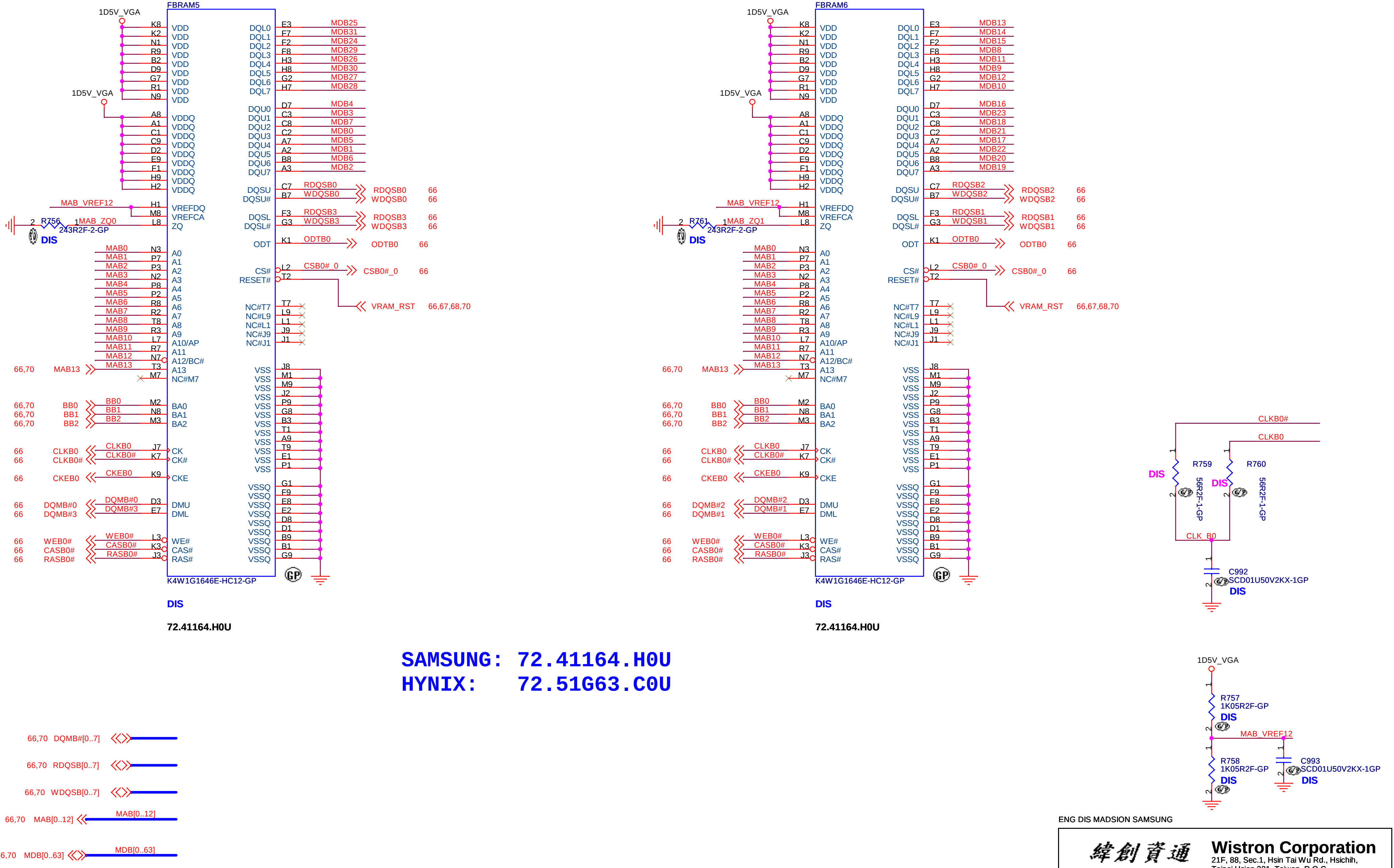
Title	VRAM(2/4)	
Size A3	Document Number JV50-CP	Rev SB
Date: Thursday, September 03, 2009	Sheet 68 of 68	

DDR3



SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
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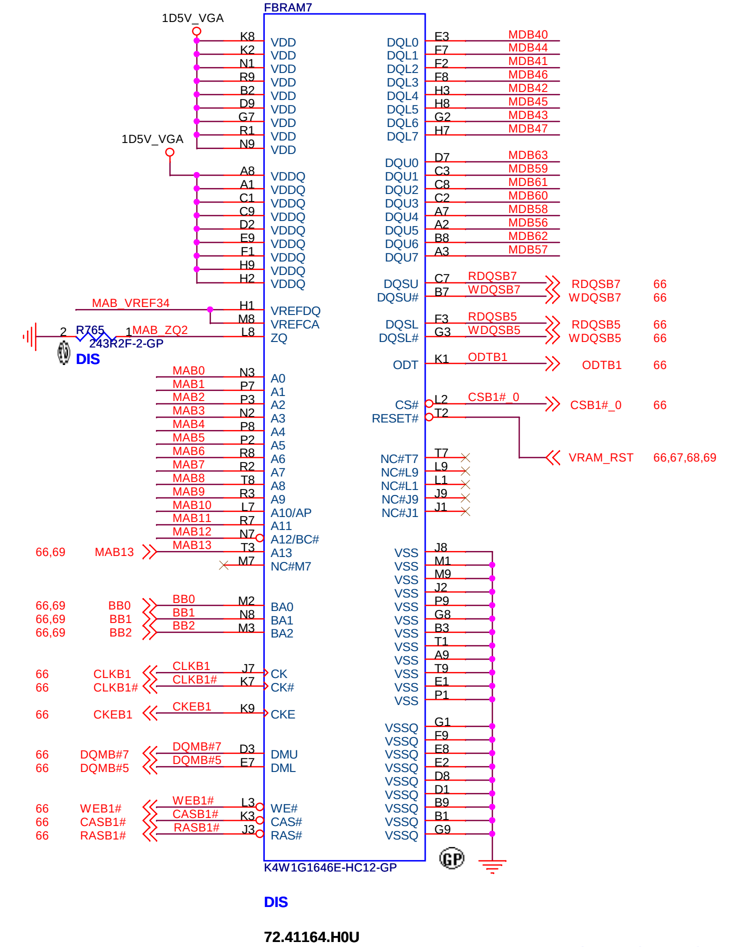
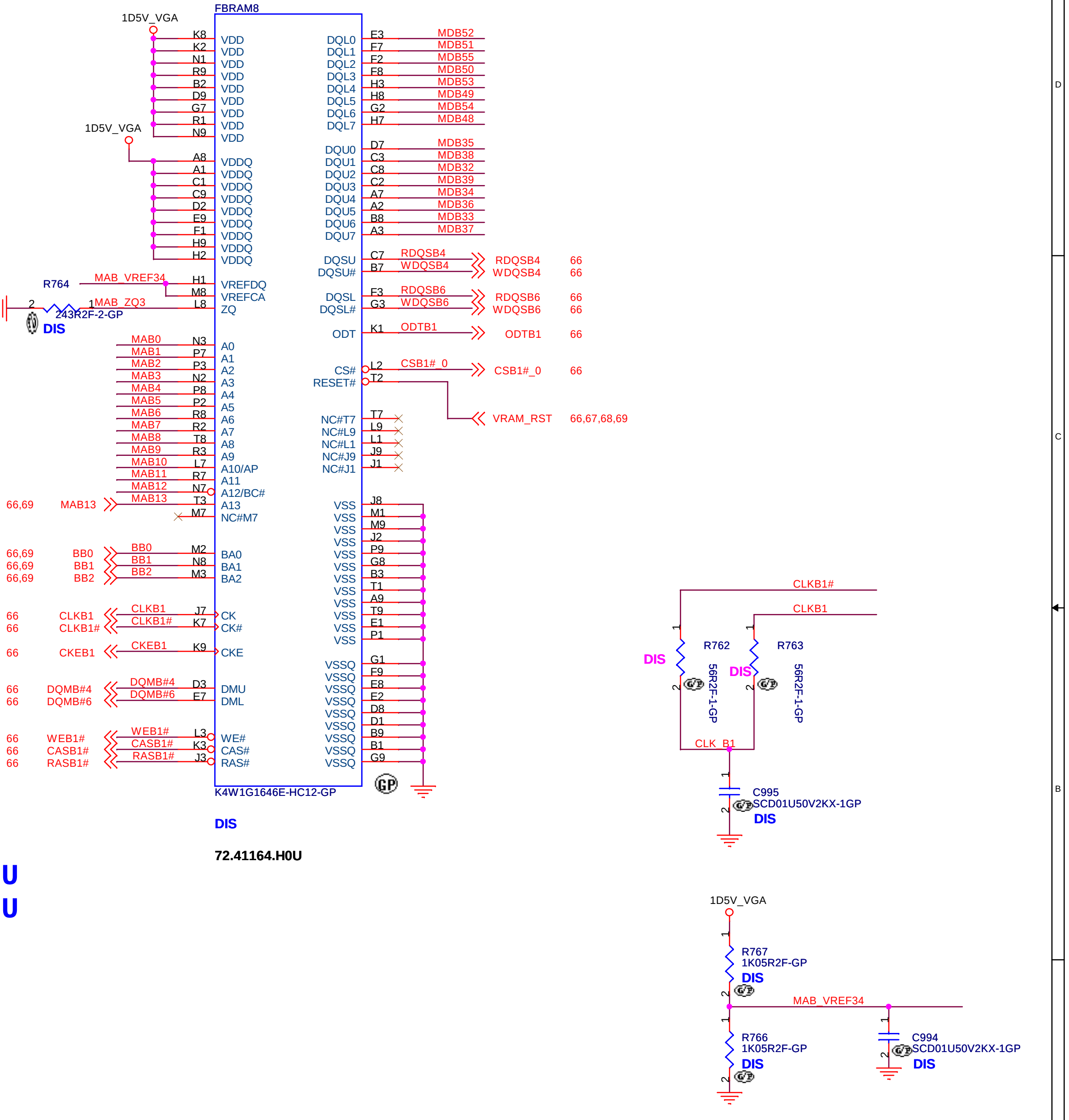
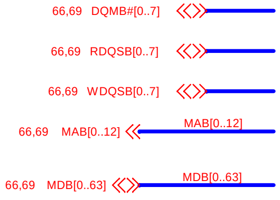
Title	*VRAM(3/4)*	
Size A3	Document Number JV50-CP	Rev SB
Date: Thursday, September 03, 2009	Sheet 69 of 68	

DDR3





SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
VRAM(4/4)

Size	Document Number	Rev
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D D

C C

B B

A A

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title
Modify History

Size	Document Number	Rev
	JV50-CP	**SA**

Date: Tuesday, August 18, 2009 Sheet 71 of 57