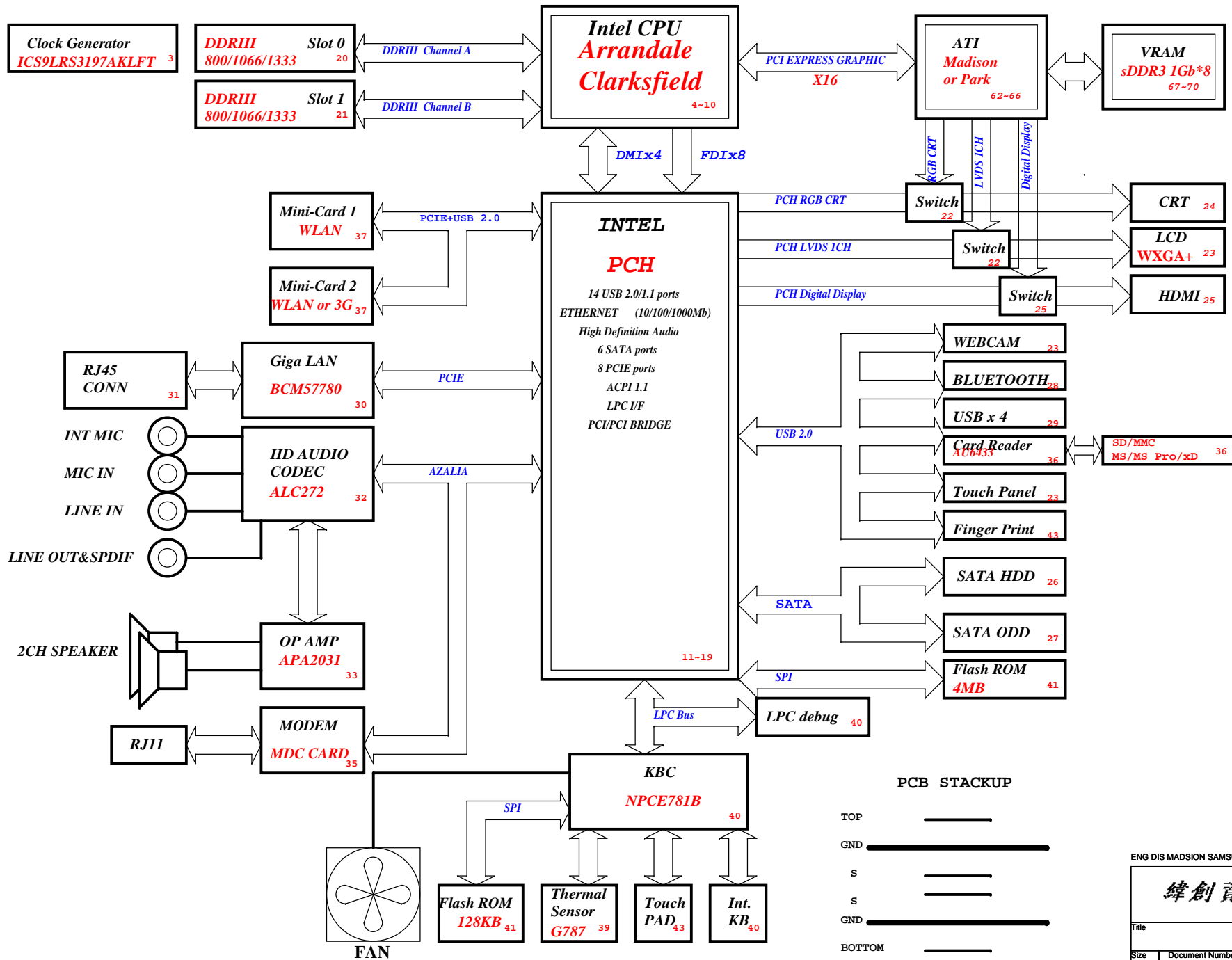


# JV50-CP Block Diagram

Project code: 91.4GD01.001

PCB P/N : 48.4GD01.0SB

REVISION : SB 09285



CPU DC/DC ISL62882	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 47,48
SYSTEM DC/DC TPS51123	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 49
SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 50
SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 50
SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 51
RT9025	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0 50
G2997	
INPUTS	OUTPUTS
1D5V_S3	0D75_S0 52
SYSTEM DC/DC ISL62881	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 54
SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	+VGA_CORE 55
CHARGER ISL88731A	
INPUTS	OUTPUTS
DCBATOUT	BT+ 53

## PCB STACKUP



ENG DIS MADISON SAMSUNG

緯創資通 **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size A3 Document Number **JV50-CP** Rev **SA**

Date: Thursday, August 27, 2009 Sheet 1 of 57

# PCH Strapping

Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> <b>Default Mode:</b> Internal weak Pull-down. <b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	<b>Default Mode:</b> Internal pull-up. <b>Low (0) = Top Block Swap Mode</b> (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	<b>High (1) = Integrated VRM is enabled</b> <b>Low (0) = Integrated VRM is disabled</b>
GNT0#, GNT1#	<b>Default (SPI):</b> Left both GNT0# and GNT1# floating. No pull up required. <b>Boot from PCI:</b> Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. <b>Boot from LPC:</b> Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	<b>Default - Internal pull-up.</b> <b>Low (0)=</b> Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	<b>Default:</b> Do not pull low. <b>Disable ME in Manufacturing Mode:</b> Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	<b>Enable iTPM:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable iTPM:</b> Left floating, no pull-down required.
NV_ALE	<b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable Danbury:</b> Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	<b>Low (0):</b> Flash Descriptor Security will be overridden. <b>High (1) :</b> Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	<b>Default = Do not connect (floating)</b> High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

# Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	<b>Embedded DisplayPort Presence</b>	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	<b>PCI-Express Static Lane Reversal</b>	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	<b>PCI-Express Configuration Select</b>	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	<b>Reserved - Temporarily used for early Clarksfield samples.</b>	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.0K Ohm/5% resistor <b>Note:</b> Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

## USB Table

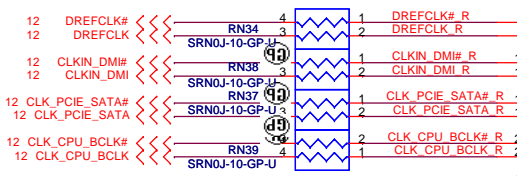
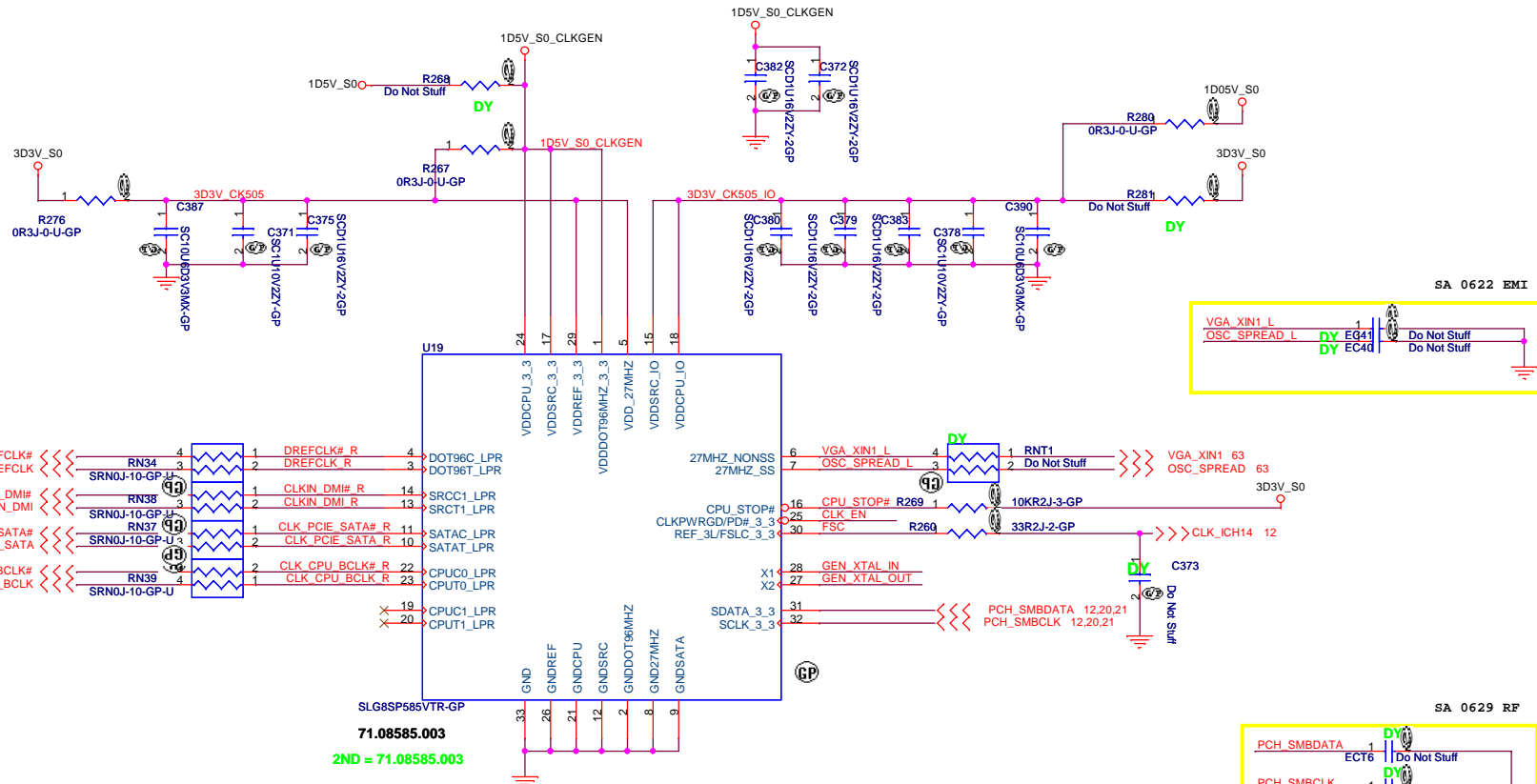
Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1(HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

## PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

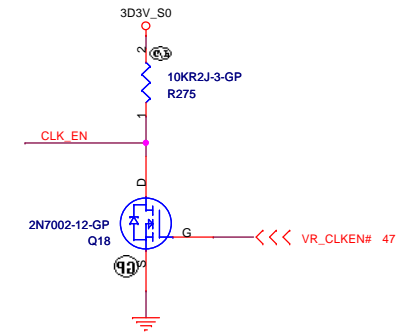
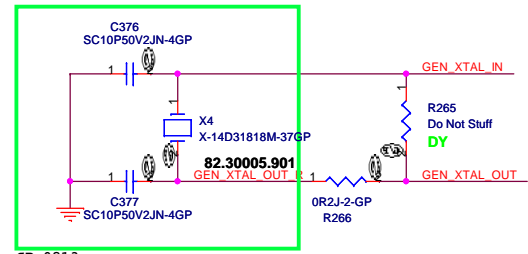
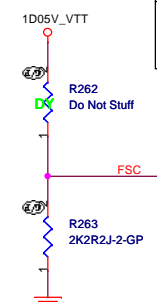
ENG DIS MADISON SAMSUNG

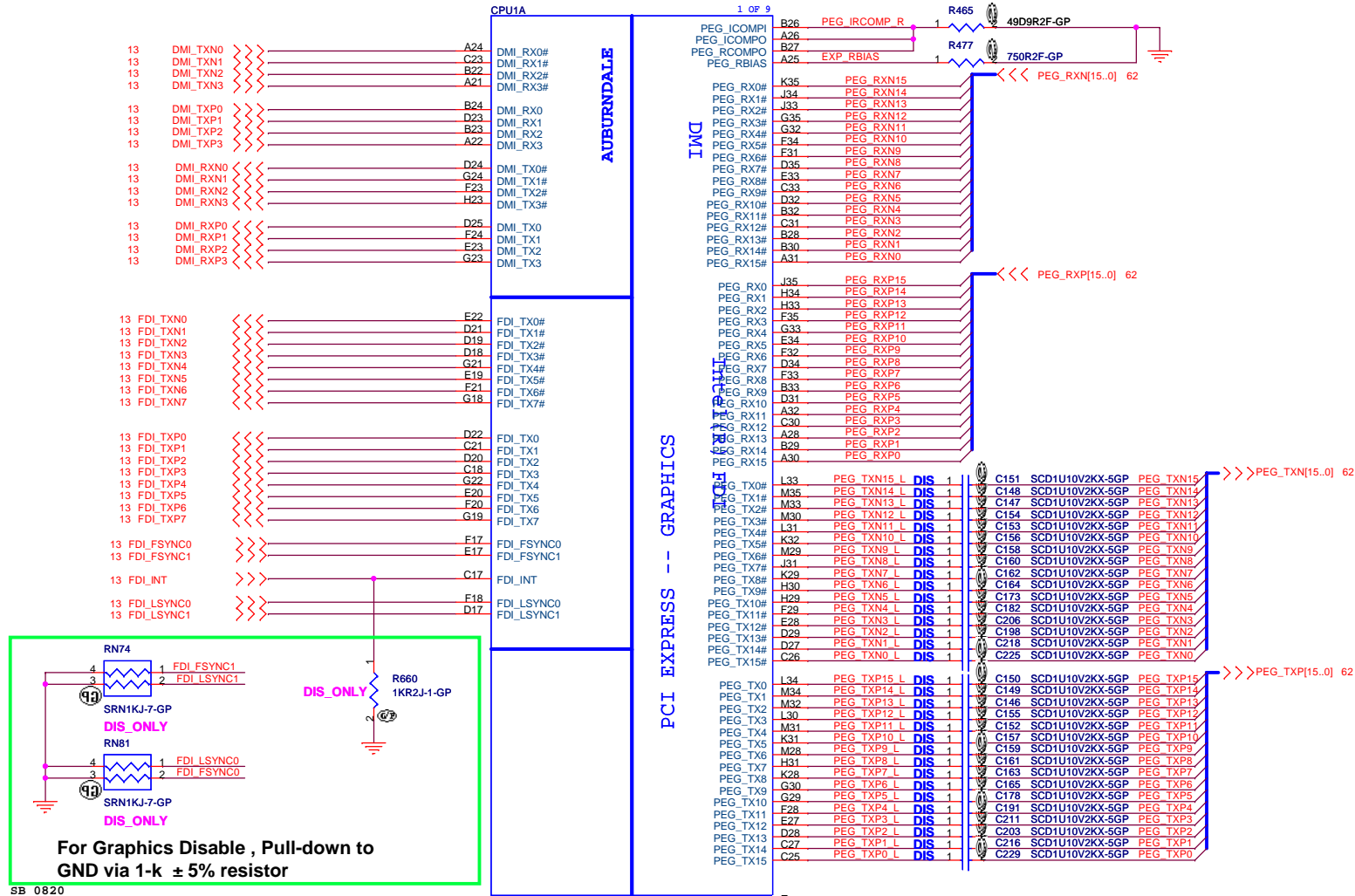
<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Table of Content</b>			
Title			
Size A3	Document Number	Rev	
	<b>JV50-CP</b>	<b>SA</b>	
Date: Tuesday, August 18, 2009	Sheet 2	of	57



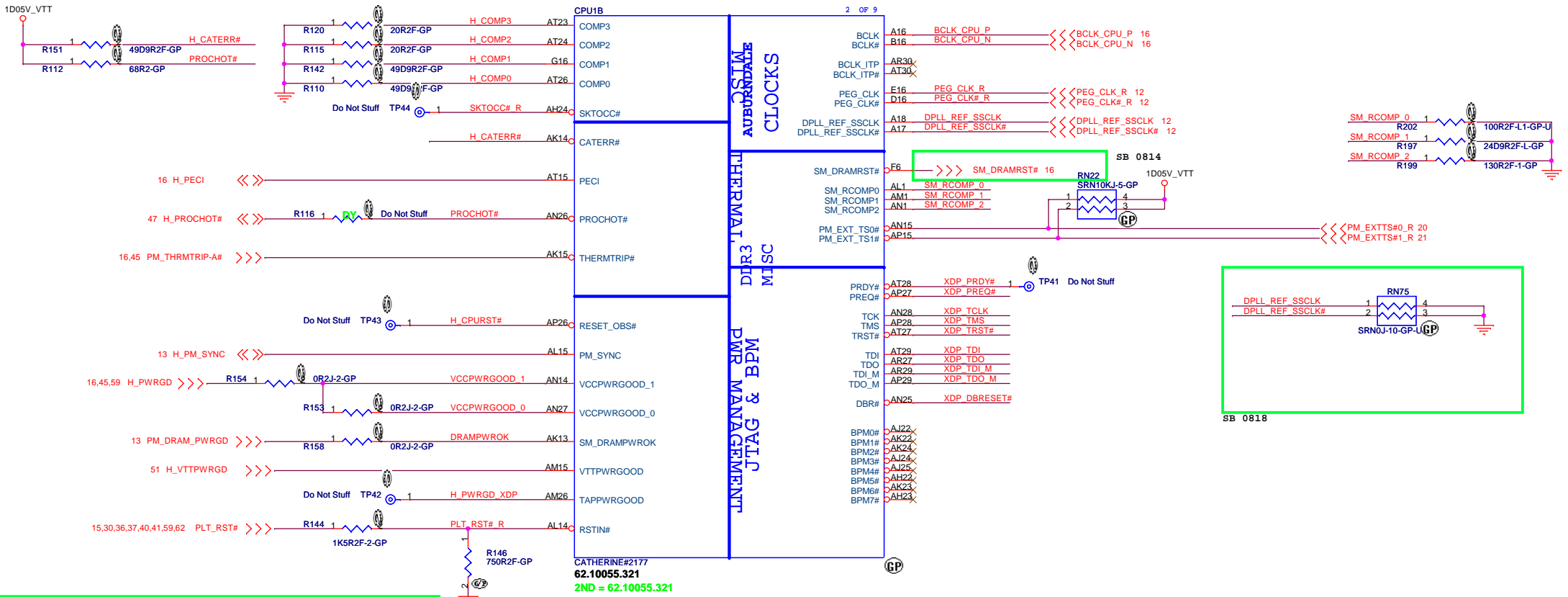
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71.08585.003  
2ND = 71.08585.003

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SPEED	133MHz (Default)	100MHz

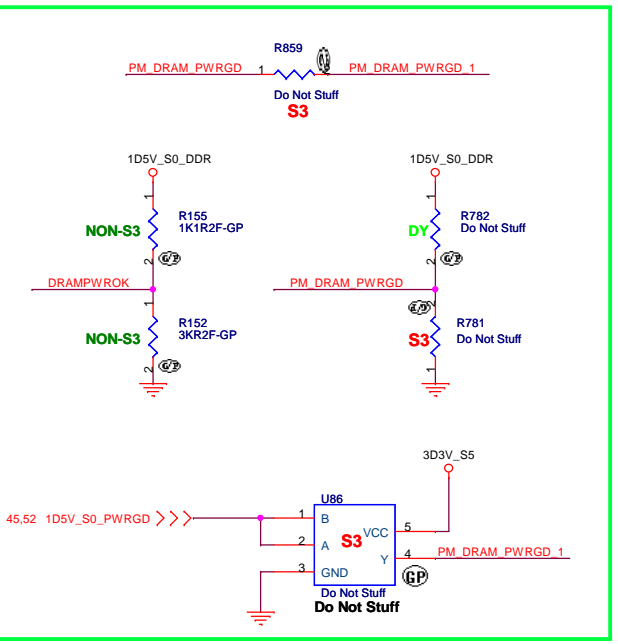




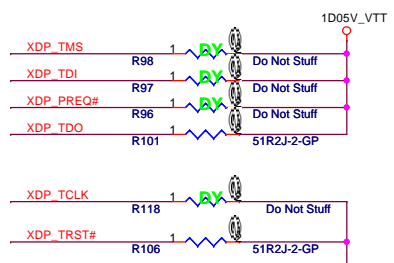
ENG DIS MADISON SAMSUNG



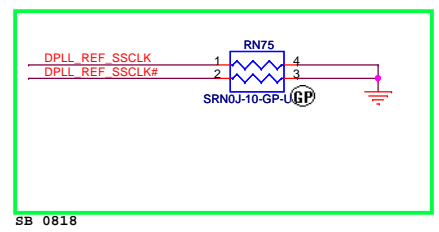
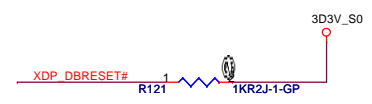
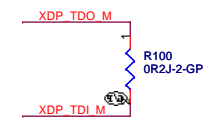
CATHERINE#2177  
**62.10055.321**  
 2ND = 62.10055.321



SB 0814



**CPU JTAG**



SB 0814

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**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (2/7)**

Size A3 Document Number **JV50-CP** Rev **SA**

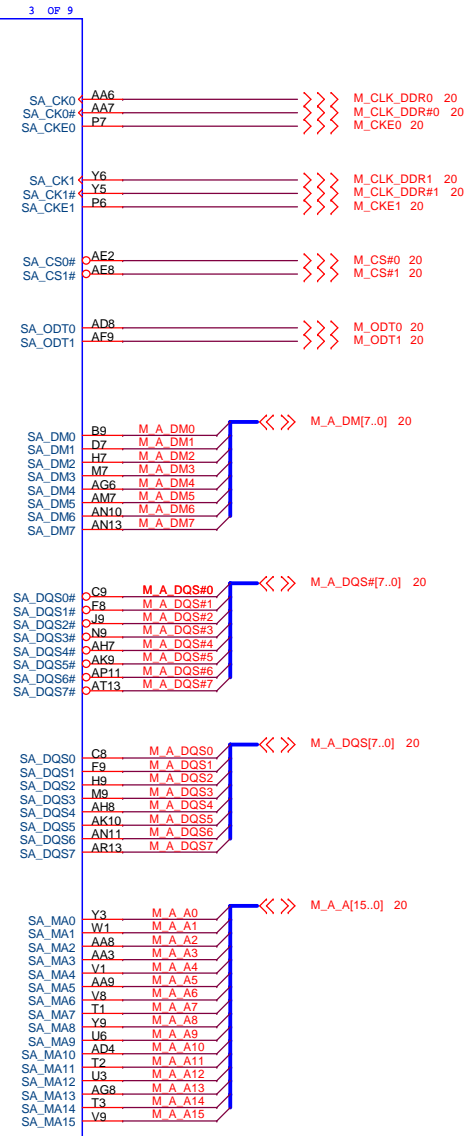
Date: Thursday, September 03, 2009 Sheet 5 of 57

20 M\_A\_DQ[63..0] <<>

M A DQ0	A10	SA_DQ0
M A DQ1	C10	SA_DQ1
M A DQ2	C7	SA_DQ2
M A DQ3	AZ	SA_DQ3
M A DQ4	B10	SA_DQ4
M A DQ5	D10	SA_DQ5
M A DQ6	E10	SA_DQ6
M A DQ7	A8	SA_DQ7
M A DQ8	D8	SA_DQ8
M A DQ9	F8	SA_DQ9
M A DQ10	E6	SA_DQ10
M A DQ11	F7	SA_DQ11
M A DQ12	E9	SA_DQ12
M A DQ13	B7	SA_DQ13
M A DQ14	E7	SA_DQ14
M A DQ15	C6	SA_DQ15
M A DQ16	H10	SA_DQ16
M A DQ17	G8	SA_DQ17
M A DQ18	K7	SA_DQ18
M A DQ19	J8	SA_DQ19
M A DQ20	G7	SA_DQ20
M A DQ21	G10	SA_DQ21
M A DQ22	J7	SA_DQ22
M A DQ23	J10	SA_DQ23
M A DQ24	L7	SA_DQ24
M A DQ25	M6	SA_DQ25
M A DQ26	M8	SA_DQ26
M A DQ27	L9	SA_DQ27
M A DQ28	K8	SA_DQ28
M A DQ29	K6	SA_DQ29
M A DQ30	N8	SA_DQ30
M A DQ31	P9	SA_DQ31
M A DQ32	AH5	SA_DQ32
M A DQ33	AF5	SA_DQ33
M A DQ34	AK6	SA_DQ34
M A DQ35	AK7	SA_DQ35
M A DQ36	AF6	SA_DQ36
M A DQ37	AG5	SA_DQ37
M A DQ38	AJ7	SA_DQ38
M A DQ39	AJ6	SA_DQ39
M A DQ40	AJ10	SA_DQ40
M A DQ41	AJ9	SA_DQ41
M A DQ42	AL10	SA_DQ42
M A DQ43	AK12	SA_DQ43
M A DQ44	AK8	SA_DQ44
M A DQ45	AL7	SA_DQ45
M A DQ46	AK11	SA_DQ46
M A DQ47	AL8	SA_DQ47
M A DQ48	AN8	SA_DQ48
M A DQ49	AM10	SA_DQ49
M A DQ50	AR11	SA_DQ50
M A DQ51	AL11	SA_DQ51
M A DQ52	AM9	SA_DQ52
M A DQ53	AN9	SA_DQ53
M A DQ54	AT11	SA_DQ54
M A DQ55	AP12	SA_DQ55
M A DQ56	AM12	SA_DQ56
M A DQ57	AN12	SA_DQ57
M A DQ58	AM13	SA_DQ58
M A DQ59	AT14	SA_DQ59
M A DQ60	AT12	SA_DQ60
M A DQ61	AL13	SA_DQ61
M A DQ62	AR14	SA_DQ62
M A DQ63	AP14	SA_DQ63

AUBURDALE

DDR SYSTEM MEMORY A



20 M\_A\_BS0 <<>  
20 M\_A\_BS1 <<>  
20 M\_A\_BS2 <<>

20 M\_A\_CAS# <<>  
20 M\_A\_RAS# <<>  
20 M\_A\_WE# <<>

CATHERINE#2177

2ND = 62.10055.321

62.10055.321



21 M\_B\_DQ[63..0] <<>

M B DQ0	B5	SB_DQ0
M B DQ1	A5	SB_DQ1
M B DQ2	C3	SB_DQ2
M B DQ3	B3	SB_DQ3
M B DQ4	E4	SB_DQ4
M B DQ5	A6	SB_DQ5
M B DQ6	A4	SB_DQ6
M B DQ7	C4	SB_DQ7
M B DQ8	D1	SB_DQ8
M B DQ9	D2	SB_DQ9
M B DQ10	F2	SB_DQ10
M B DQ11	F1	SB_DQ11
M B DQ12	C2	SB_DQ12
M B DQ13	F5	SB_DQ13
M B DQ14	F3	SB_DQ14
M B DQ15	G4	SB_DQ15
M B DQ16	H6	SB_DQ16
M B DQ17	G2	SB_DQ17
M B DQ18	J6	SB_DQ18
M B DQ19	J3	SB_DQ19
M B DQ20	G1	SB_DQ20
M B DQ21	G5	SB_DQ21
M B DQ22	J2	SB_DQ22
M B DQ23	J1	SB_DQ23
M B DQ24	J5	SB_DQ24
M B DQ25	L3	SB_DQ25
M B DQ26	L2	SB_DQ26
M B DQ27	M1	SB_DQ27
M B DQ28	K5	SB_DQ28
M B DQ29	K4	SB_DQ29
M B DQ30	M4	SB_DQ30
M B DQ31	N5	SB_DQ31
M B DQ32	AF3	SB_DQ32
M B DQ33	AG1	SB_DQ33
M B DQ34	AJ3	SB_DQ34
M B DQ35	AK1	SB_DQ35
M B DQ36	AG4	SB_DQ36
M B DQ37	AG3	SB_DQ37
M B DQ38	AJ4	SB_DQ38
M B DQ39	AH4	SB_DQ39
M B DQ40	AK3	SB_DQ40
M B DQ41	AK4	SB_DQ41
M B DQ42	AM6	SB_DQ42
M B DQ43	AN2	SB_DQ43
M B DQ44	AK5	SB_DQ44
M B DQ45	AK2	SB_DQ45
M B DQ46	AM4	SB_DQ46
M B DQ47	AM3	SB_DQ47
M B DQ48	AP3	SB_DQ48
M B DQ49	AN5	SB_DQ49
M B DQ50	AT4	SB_DQ50
M B DQ51	AN6	SB_DQ51
M B DQ52	AN4	SB_DQ52
M B DQ53	AN3	SB_DQ53
M B DQ54	AT5	SB_DQ54
M B DQ55	AT6	SB_DQ55
M B DQ56	AN7	SB_DQ56
M B DQ57	AP6	SB_DQ57
M B DQ58	AP8	SB_DQ58
M B DQ59	AT9	SB_DQ59
M B DQ60	AT7	SB_DQ60
M B DQ61	AP9	SB_DQ61
M B DQ62	AR10	SB_DQ62
M B DQ63	AT10	SB_DQ63

21 M\_B\_BS0 <<>  
21 M\_B\_BS1 <<>  
21 M\_B\_BS2 <<>

21 M\_B\_CAS# <<>  
21 M\_B\_RAS# <<>  
21 M\_B\_WE# <<>

CATHERINE#2177

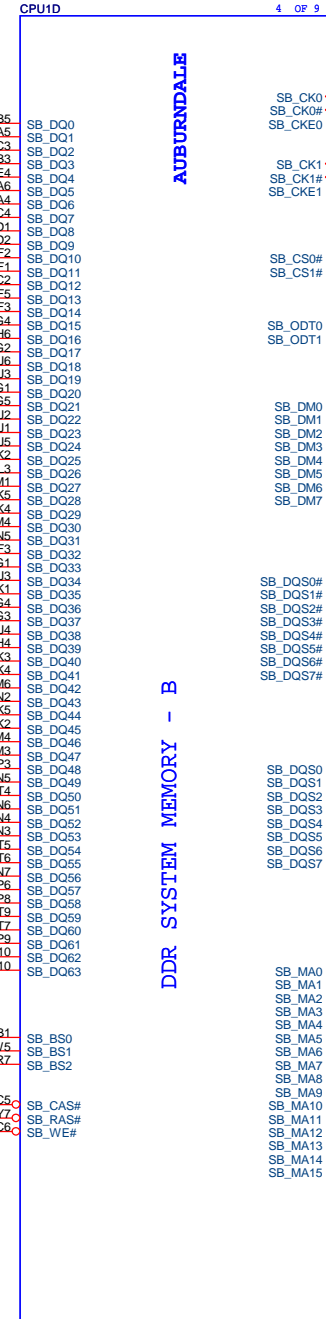
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62.10055.321

4 OF 9

AUBURDALE

DDR SYSTEM MEMORY - B

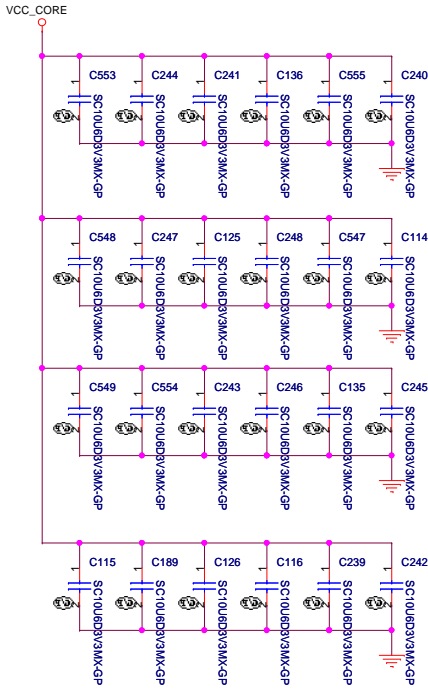


CATHERINE#2177

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緯創資通 Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU (3/7)		
Size	Document Number	Rev
A3	JV50-CP	SA
Date:	Thursday, September 03, 2009	Sheet 6 of 57



**PROCESSOR CORE POWER**

VCC\_CORE  
**52A**

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AG25 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
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- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
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- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- V35 VCC
- V34 VCC
- V33 VCC
- V32 VCC
- V31 VCC
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- V29 VCC
- V28 VCC
- V27 VCC
- V26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
- R34 VCC
- R33 VCC
- R32 VCC
- R31 VCC
- R30 VCC
- R29 VCC
- R28 VCC
- R27 VCC
- P35 VCC
- P34 VCC
- P33 VCC
- P32 VCC
- P31 VCC
- P30 VCC
- P29 VCC
- P28 VCC
- P27 VCC
- P26 VCC

**AUBURNDALE**

**1.1V RAIL POWER**

**CPU CORE SUPPLY**

**POWER**

**CPU VIDS**

**SENSE LINES**

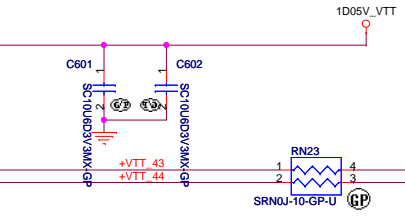
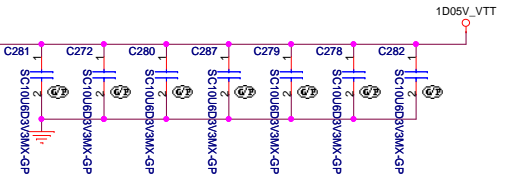
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- VTT0 AH11
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- VTT0 J13
- VTT0 H14
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- VTT0 G14
- VTT0 G13
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- VTT0 G11
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- VTT0 E11
- VTT0 E12
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- VTT0 D12
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- VTT0 C14
- VTT0 C13
- VTT0 C12
- VTT0 C11
- VTT0 B14
- VTT0 B12
- VTT0 A14
- VTT0 A13
- VTT0 A12
- VTT0 A11

- VTT0 AF10
- VTT0 AE10
- VTT0 AC10
- VTT0 AB10
- VTT0 Y10
- VTT0 W10
- VTT0 U10
- VTT0 T10
- VTT0 J12
- VTT0 J11
- VTT0 J16
- VTT0 J15

- PSI# AN33 >>> PSI# 47
- AK35 H\_VID0 >>> H\_VID[6..0] 47
- AK33 H\_VID1 >>>
- AK34 H\_VID2 >>>
- AL35 H\_VID3 >>>
- AL33 H\_VID4 >>>
- AM33 H\_VID5 >>>
- AM35 H\_VID6 >>>
- AM34 >>> PM\_DPRSLPVR 47

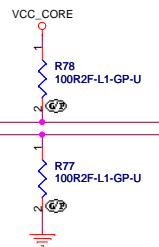
- G15 H\_VTTVID1 TP45 Do Not Stuff
- Clarkfield H\_VTTVID1 = Low, VTT = 1.1V
- Arrandale H\_VTTVID1 = High, VTT = 1.05V

- AN35 <<< IMVP\_MON 47
- AJ34 VCC\_SENSE >>>
- AJ35 VSS\_SENSE >>>
- B15 VTT\_SENSE TP46 Do Not Stuff >>>
- A15 TP\_VSS\_SENSE\_VTT >>>



The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarkfield VTT=1.1V

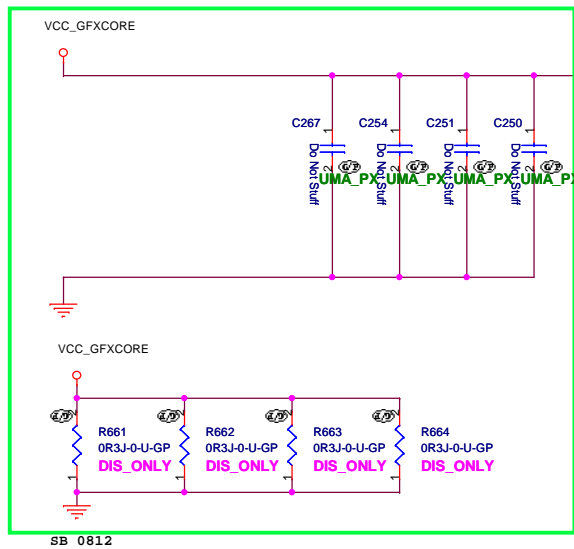


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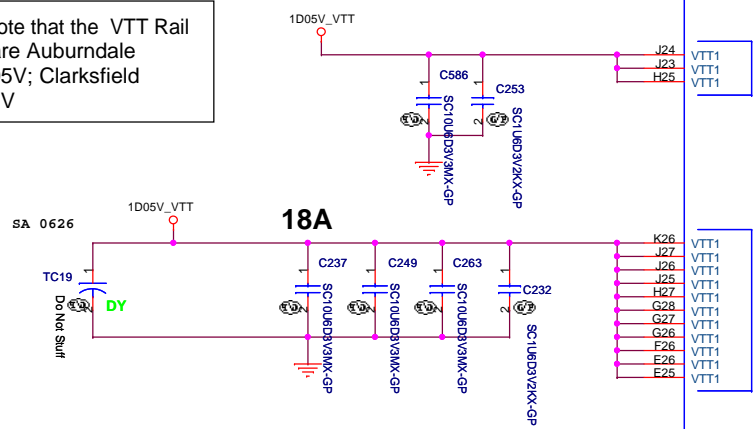
ENG DIS MADSION SAMSUNG

<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsin 221, Taiwan, R.O.C.			
<b>CPU (4/7)</b>			
Title	Document Number	Rev	SA
	<b>JV50-CP</b>		
Date: Thursday, September 03, 2009	Sheet 7	of	57





Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V



- CPU1G
- AT21 VAXG1
  - AT19 VAXG2
  - AT18 VAXG3
  - AT16 VAXG4
  - AR19 VAXG5
  - AR18 VAXG6
  - AR17 VAXG7
  - AR16 VAXG8
  - AP19 VAXG9
  - AP18 VAXG10
  - AP16 VAXG11
  - AN19 VAXG12
  - AN18 VAXG13
  - AN17 VAXG14
  - AN16 VAXG15
  - AM19 VAXG16
  - AM18 VAXG17
  - AM17 VAXG18
  - AM16 VAXG19
  - AL19 VAXG20
  - AL18 VAXG21
  - AL17 VAXG22
  - AL16 VAXG23
  - AK19 VAXG24
  - AK18 VAXG25
  - AK17 VAXG26
  - AK16 VAXG27
  - AK15 VAXG28
  - AJ19 VAXG29
  - AJ18 VAXG30
  - AJ17 VAXG31
  - AH19 VAXG32
  - AH18 VAXG33
  - AH17 VAXG34
  - AH16 VAXG35
  - AH15 VAXG36

**AUBURDALE**

**GRAPHICS**

**POWER**

**PEG & DMI**

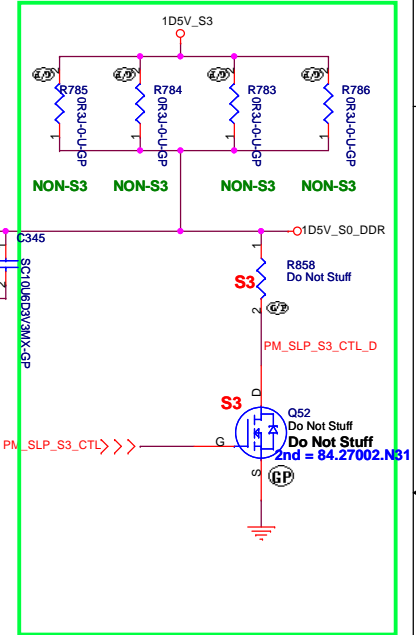
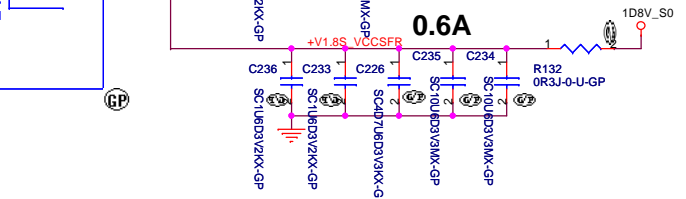
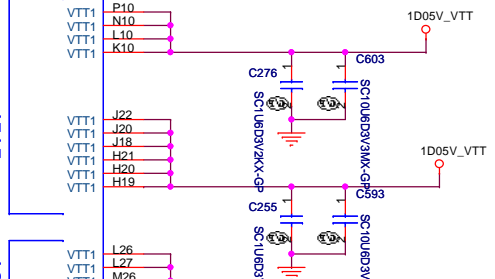
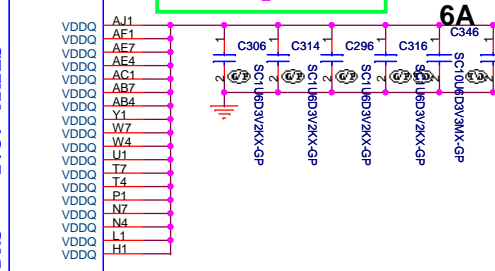
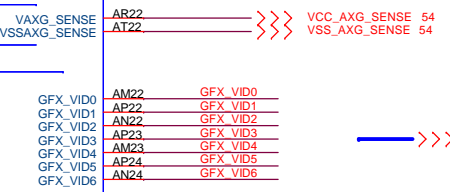
**SENSE LINES**

**GRAPHICS VIDS**

**DDR3 - 1.5V RAILS**

**1.1V**

**1.8V**

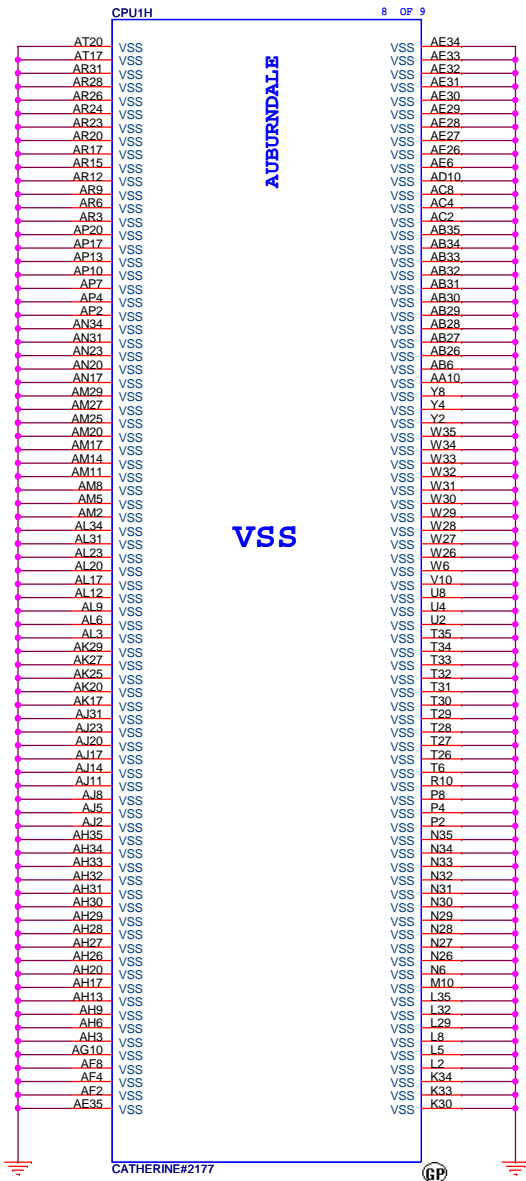


CATHERINE#2177  
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62.10055.321

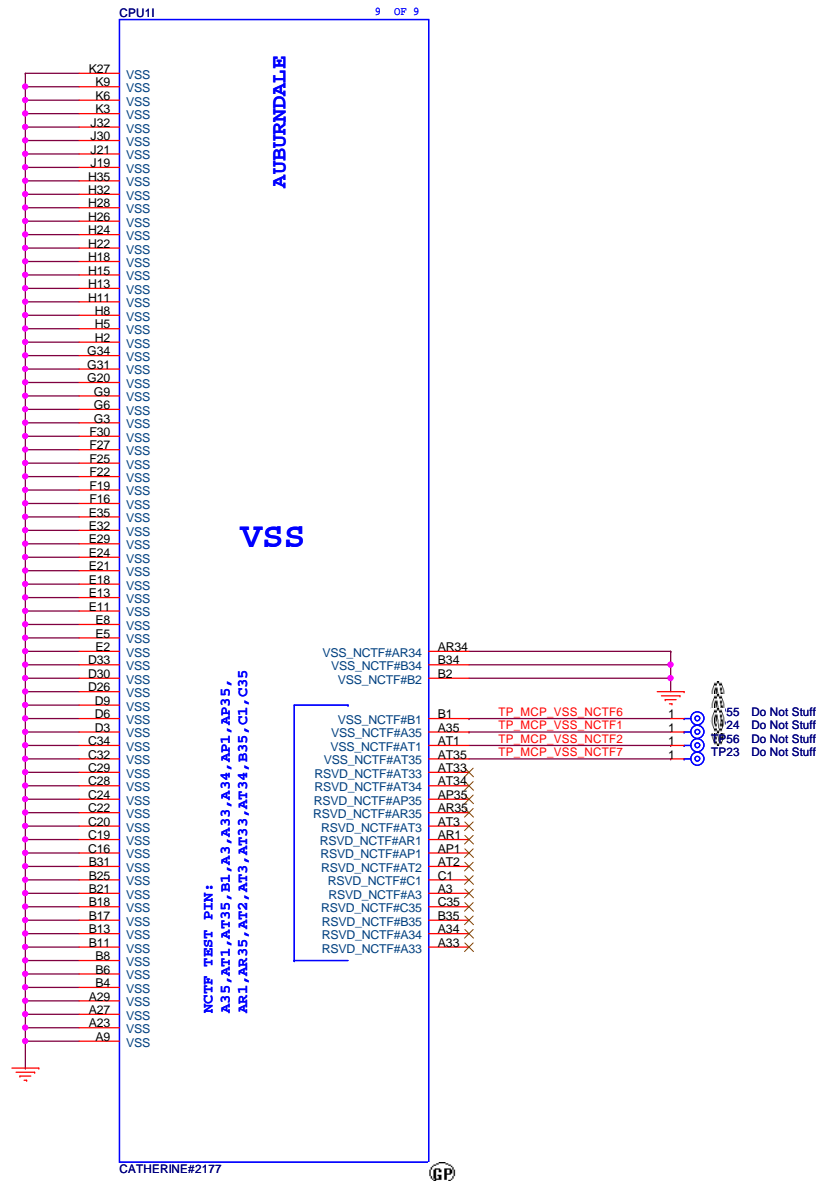
ENG DIS MADSION SAMSUNG

<b>緯創資通 Wistron Corporation</b>		
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>CPU (5/7)</b>		
Size A3	Document Number <b>JV50-CP</b>	Rev <b>SA</b>
Date: Thursday, September 03, 2009	Sheet 8 of 57	



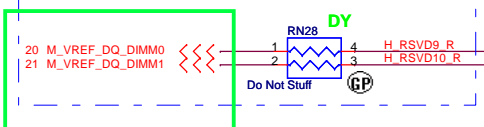


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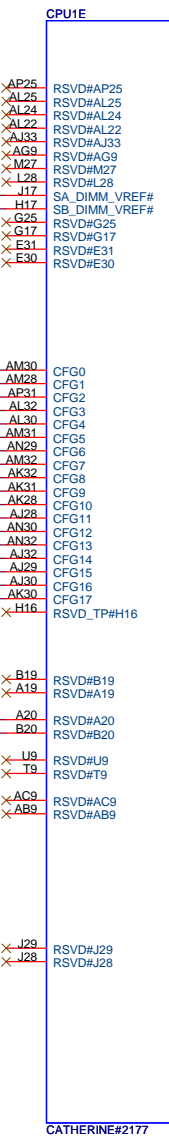
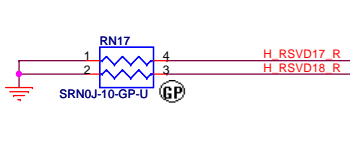
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### SO-DIMM VREFDQ (M3) Circuit for Clarkfield Processor



SB 0817

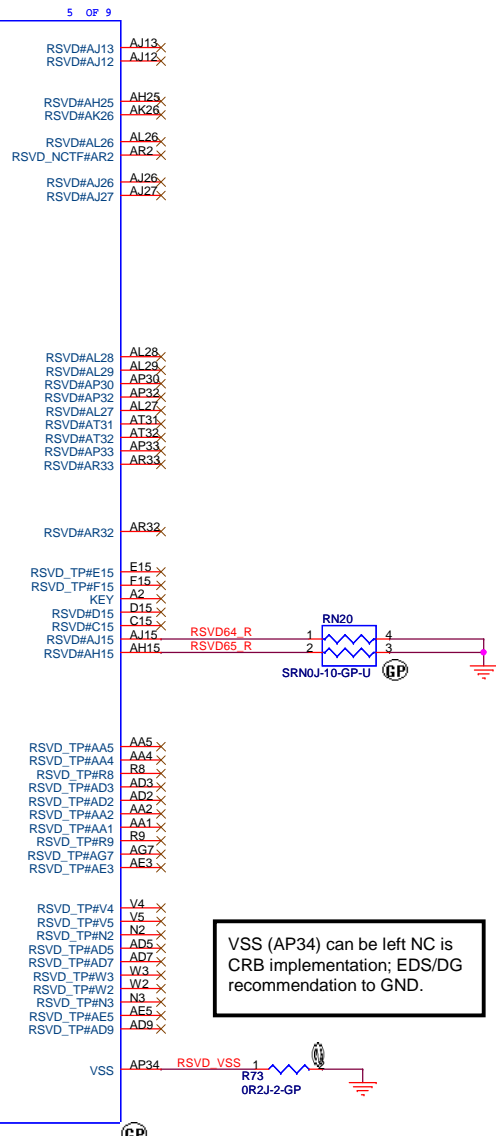
- Do Not Stuff TP38
- Do Not Stuff TP29
- Do Not Stuff TP32
- Do Not Stuff TP34
- Do Not Stuff TP30
- Do Not Stuff TP33
- Do Not Stuff TP39
- Do Not Stuff TP40
- Do Not Stuff TP31
- Do Not Stuff TP28
- Do Not Stuff TP27
- Do Not Stuff TP36
- Do Not Stuff TP37
- Do Not Stuff TP35



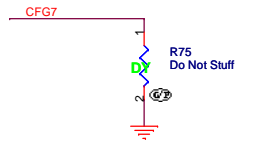
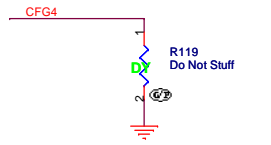
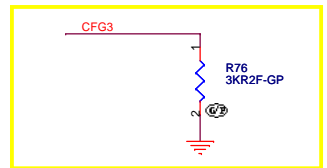
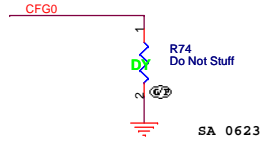
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62.10055.321

AUBURDALE

RESERVED



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

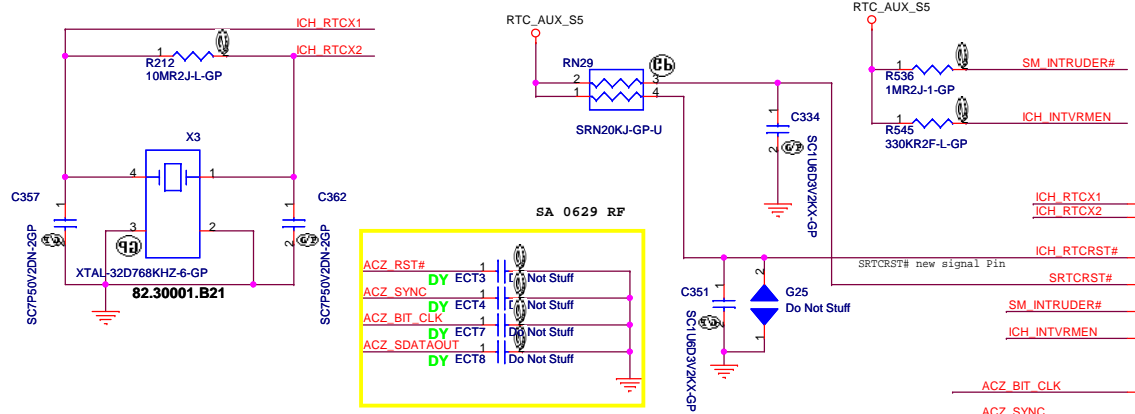
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarkfield samples.	
CFG7	Clarkfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.  Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

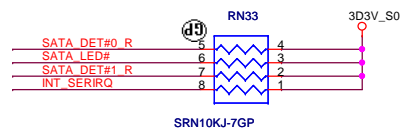
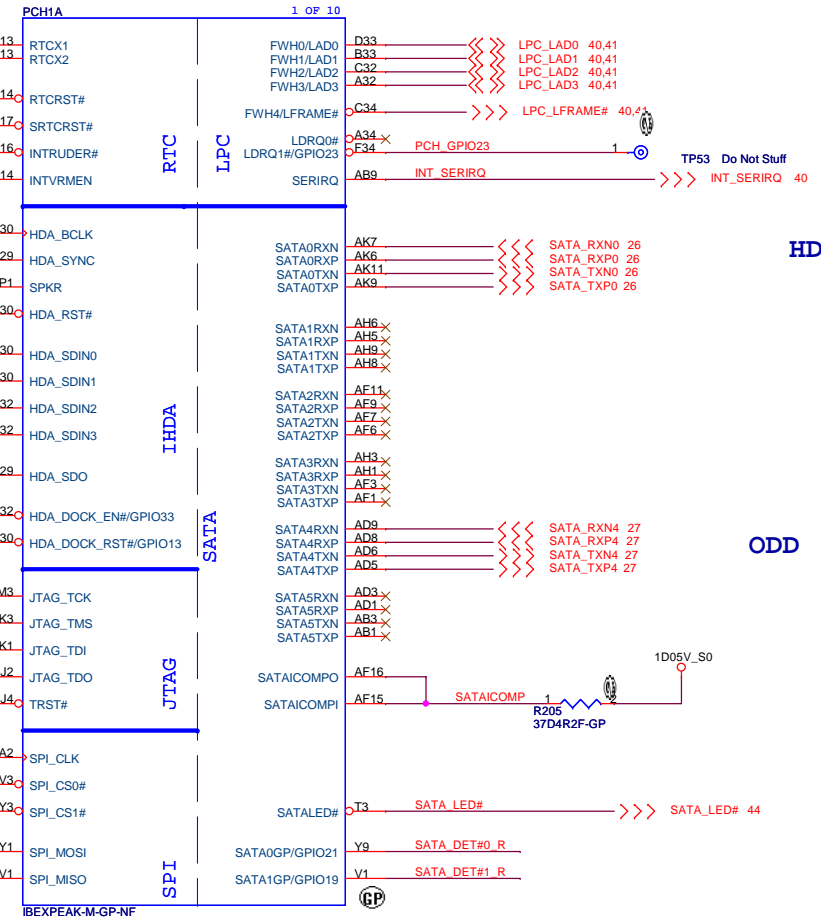
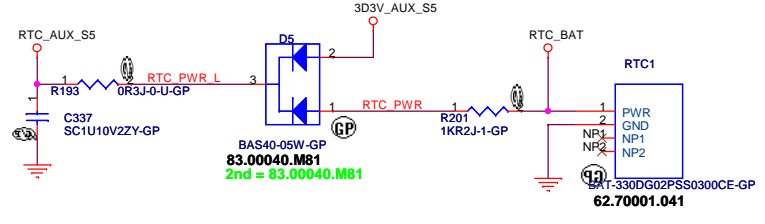
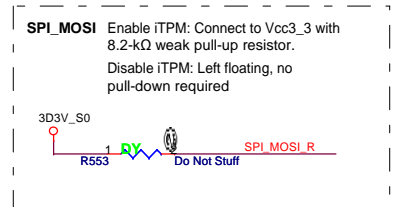
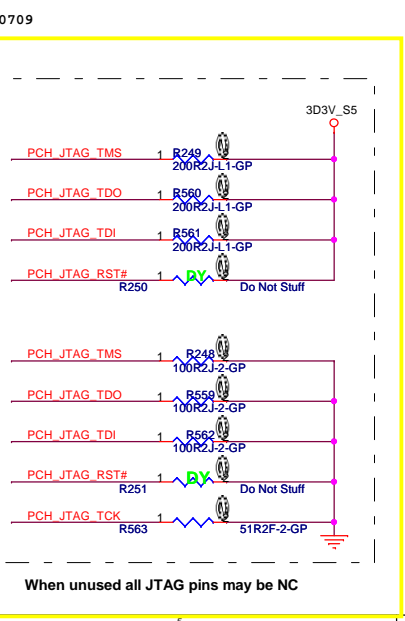
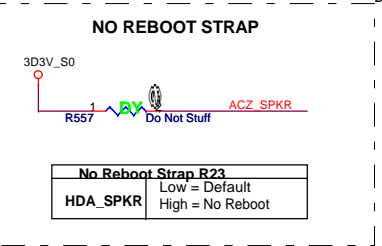
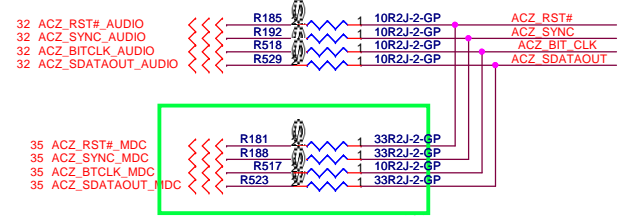
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<b>CPU (7/7)</b>	
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INTVRMEN- Integrated SUS  
1.1V VRM Enable  
High - Enable internal VRs

Integrated VccSua1_05,VccSua1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable



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Title: PCH (1/9)

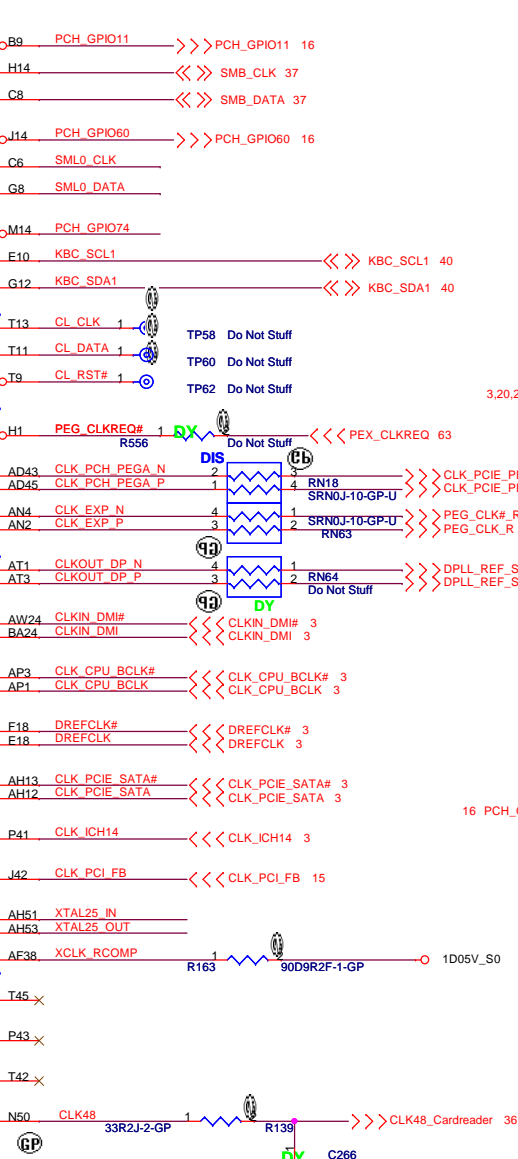
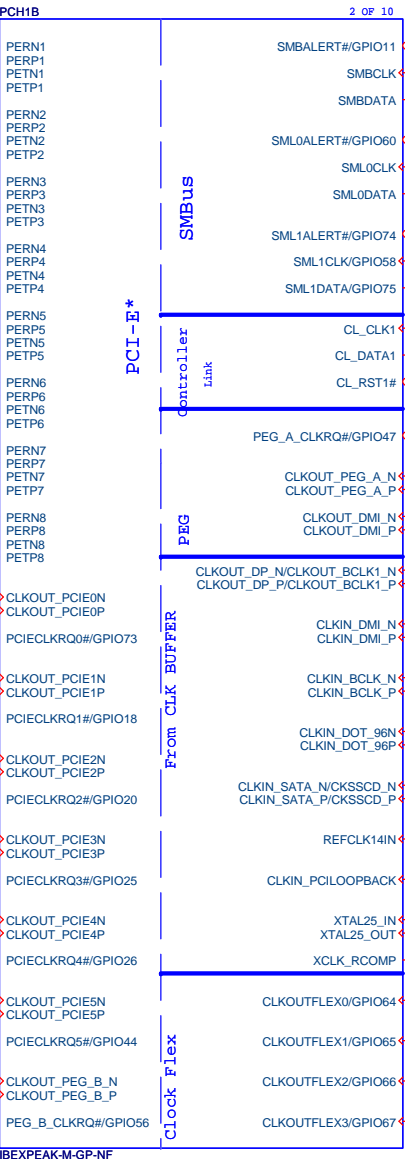
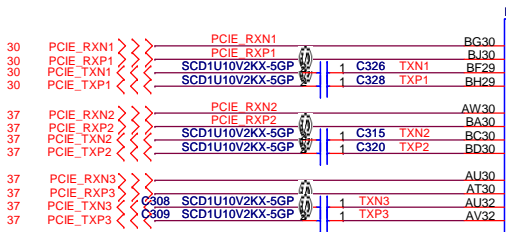
Size: A3 Document Number: JV50-CP Rev: SA

Date: Thursday, September 03, 2009 Sheet 11 of 57

LAN

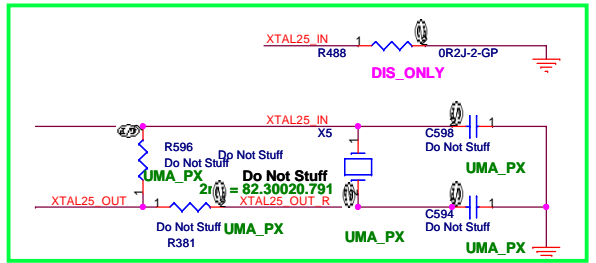
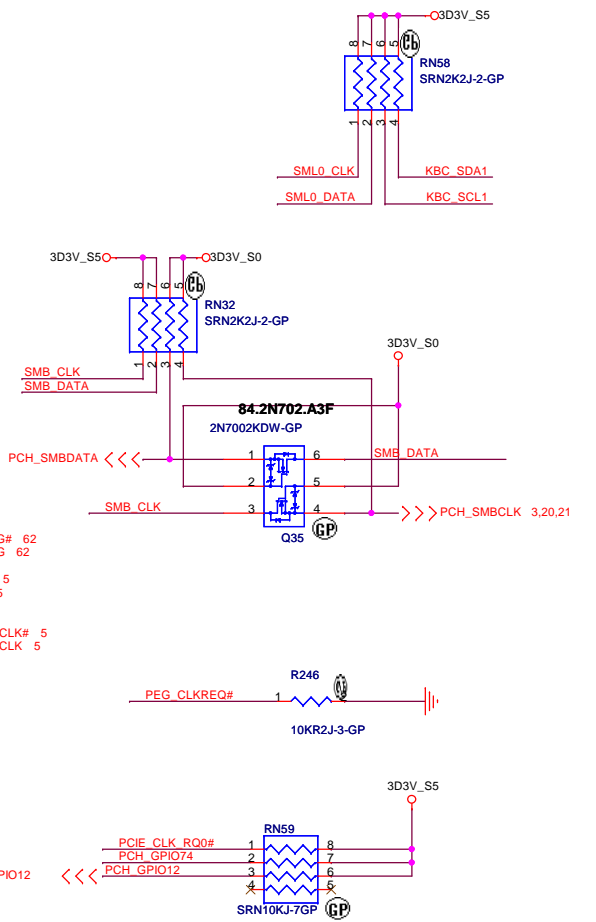
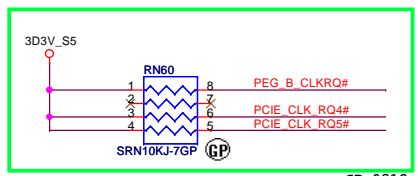
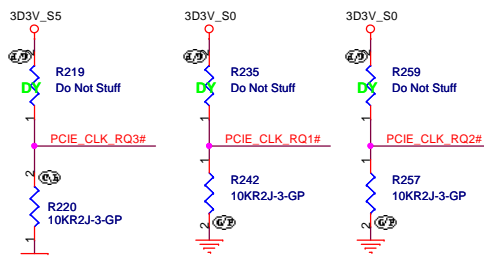
MINICARD1

MINICARD2



PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).



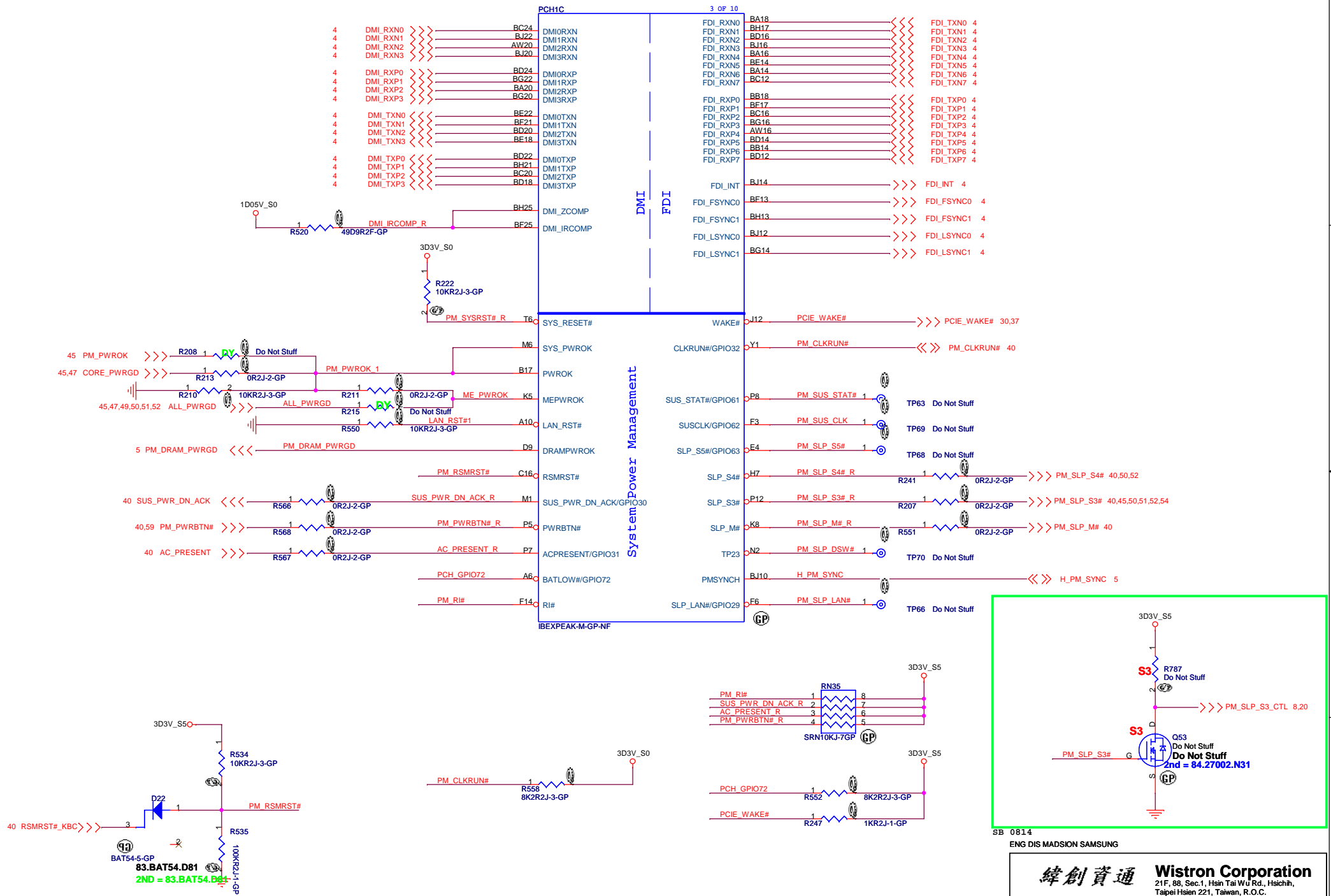
ENG DIS MADISON SAMSUNG

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Title: PCH (2/9)

Size A3 Document Number: JV50-CP Rev SA

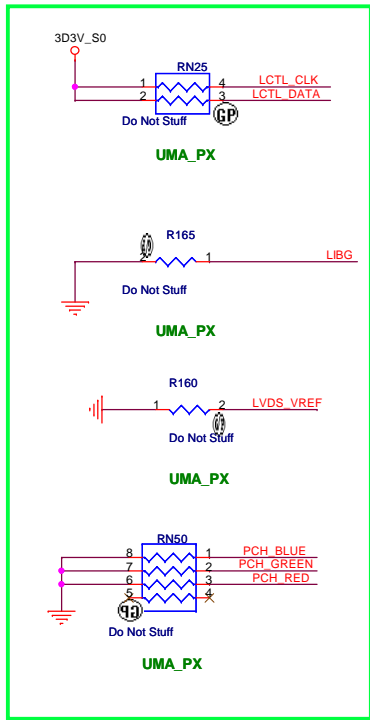
Date: Thursday, September 03, 2009 Sheet 12 of 57



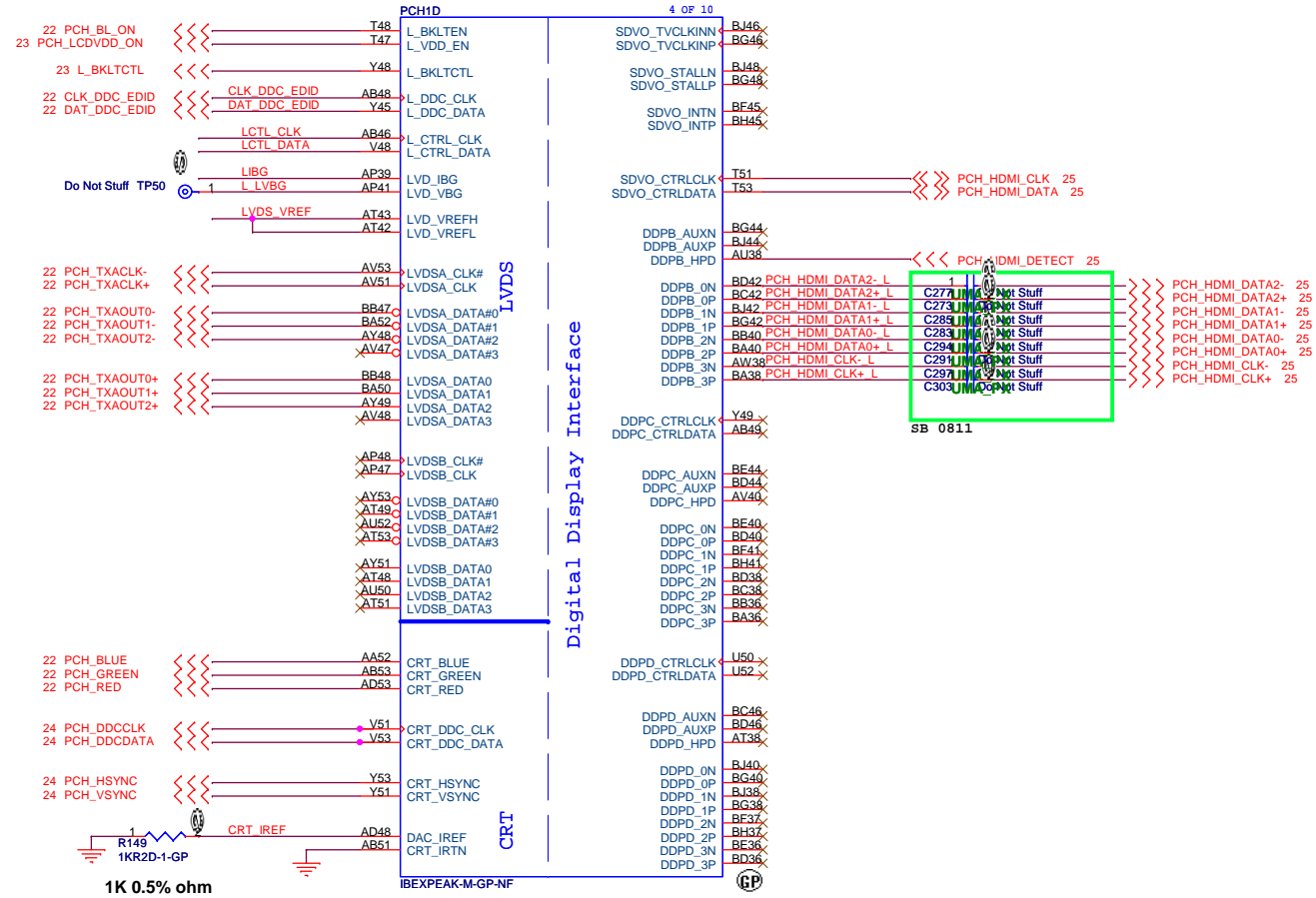
SB 0814

ENG DIS MADISON SAMSUNG

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<b>PCH (3/9)</b>	
Title Size A3 Date: Thursday, September 03, 2009	Document Number <b>JV50-CP</b> Sheet 13 of 57
Rev <b>SA</b>	

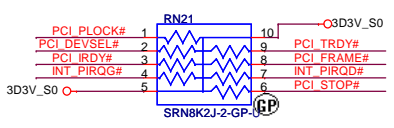


SB 0811

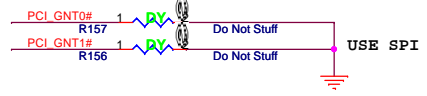
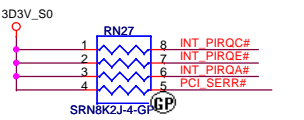
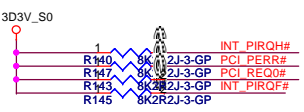
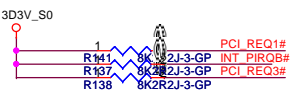


ENG DIS MADISON SAMSUNG

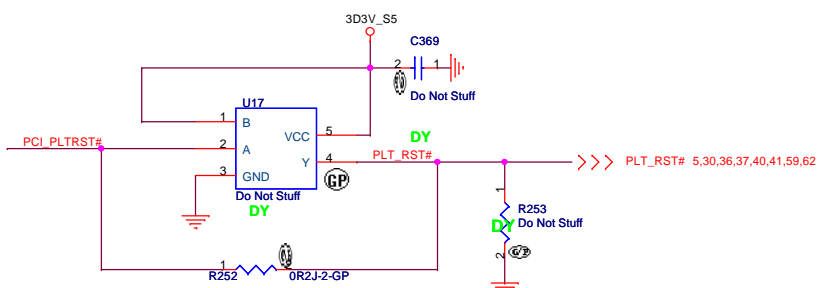
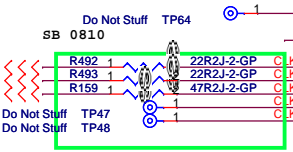
<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
<b>PCH (4/9)</b>	
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These pins are left as NC, because the function is disable.



BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI



- H40 AD0
- N34 AD1
- C44 AD2
- A38 AD3
- C36 AD4
- J34 AD5
- A40 AD6
- D45 AD7
- E36 AD8
- H48 AD9
- E40 AD10
- C40 AD11
- M48 AD12
- M45 AD13
- F53 AD14
- M40 AD15
- M43 AD16
- J36 AD17
- K48 AD18
- F40 AD19
- C42 AD20
- K46 AD21
- M51 AD22
- J52 AD23
- K51 AD24
- L34 AD25
- F42 AD26
- J40 AD27
- G46 AD28
- F44 AD29
- M47 AD30
- H36 AD31
- J50 C/BE#
- G42 C/BE1#
- H47 C/BE2#
- G34 C/BE3#
- G38 PIRQA#
- H51 PIRQB#
- B37 PIRQC#
- A44 PIRQD#
- F51 REQ0#
- A46 REQ1#/GPIO50
- E45 REQ2#/GPIO52
- M53 REQ3#/GPIO54
- F48 GNT0#
- K46 GNT1#/GPIO53
- F38 GNT2#/GPIO51
- H53 GNT3#/GPIO55
- B41 PIRQE#/GPIO2
- K53 PIRQF#/GPIO3
- A36 PIRQG#/GPIO4
- A48 PIRQH#/GPIO5
- K6 PCIRST#
- E44 SERR#
- E50 PERR#
- A42 PCI IRDY#
- H44 PCI DEVSEL#
- F46 PCI FRAME#
- C46 PCI PLOCK#
- D49 PCI STOP#
- C48 PCI TRDY#
- M7 ICH PME#
- D5 PCI PLTRST#
- N52 CLKOUT\_PC10
- P53 CLKOUT\_PC11
- P46 CLKOUT\_PC12
- P51 CLKOUT\_PC13
- P48 CLKOUT\_PC14

- NV\_CE#0 AY9
- NV\_CE#1 BD1
- NV\_CE#2 AP15
- NV\_CE#3 BDE
- NV\_DQ#0 AV9
- NV\_DQ#1 BGS
- NV\_DQ0/NV\_IO0 AP7
- NV\_DQ1/NV\_IO1 AP6
- NV\_DQ2/NV\_IO2 AT6
- NV\_DQ3/NV\_IO3 AT9
- NV\_DQ4/NV\_IO4 AV6
- NV\_DQ5/NV\_IO5 BB3
- NV\_DQ6/NV\_IO6 BB4
- NV\_DQ7/NV\_IO7 BA4
- NV\_DQ8/NV\_IO8 BE4
- NV\_DQ9/NV\_IO9 BB6
- NV\_DQ10/NV\_IO10 BD6
- NV\_DQ11/NV\_IO11 BC8
- NV\_DQ12/NV\_IO12 BJ8
- NV\_DQ13/NV\_IO13 BJ6
- NV\_DQ14/NV\_IO14 BG6
- NV\_DQ15/NV\_IO15
- NV\_ALE BD3
- NV\_CLE AY6
- NV\_RCOMP AU2
- NV\_RB# AV7
- NV\_WR#0\_RE# AY8
- NV\_WR#1\_RE# AY5
- NV\_WE#\_CK0 AV11
- NV\_WE#\_CK1 BE5
- USBPN H18
- USBPP J18
- USBP1N A18
- USBP1P C18
- USBP2N M20
- USBP2P J20
- USBP3N L20
- USBP3P F20
- USBP4N A20
- USBP4P G20
- USBP5N C20
- USBP5P M22
- USBP6N N22
- USBP6P B21
- USBP7N D21
- USBP7P H22
- USBP8N J22
- USBP8P E22
- USBP9N F22
- USBP9P A22
- USBP10N C22
- USBP10P G24
- USBP11N H24
- USBP11P L24
- USBP12N M24
- USBP12P A24
- USBP13N Q24
- USBP13P USBPN9 29
- USBPN10 29
- USBPN11 28
- USBPN12 28
- USBPN13 37
- USBPN14 37
- USBPN15 36
- USBPN16 36

These pins are left as NC, because the function is disable.

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

Danbury Technology:  
Disabled when Low.  
Enable when High.

USB

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1(HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

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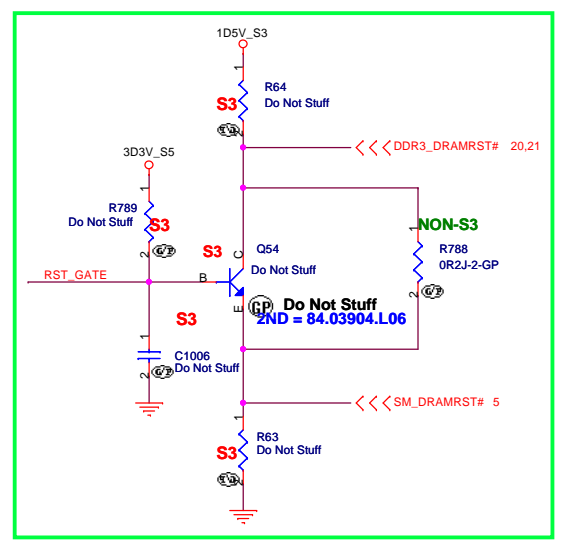
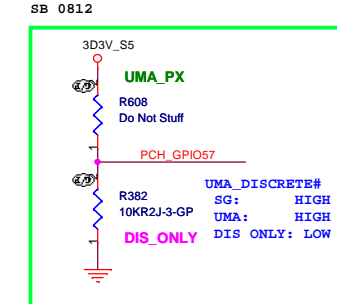
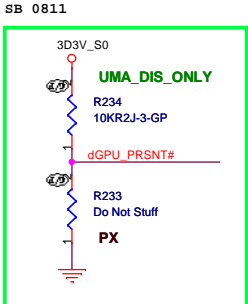
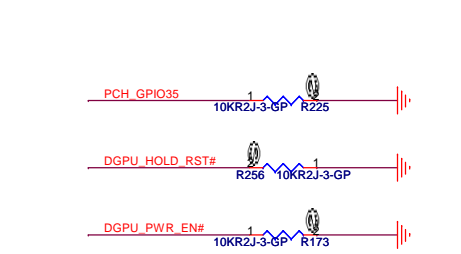
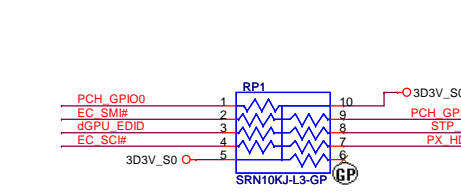
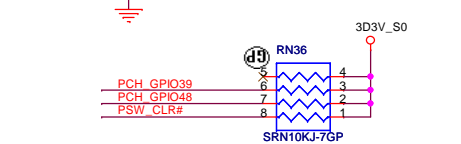
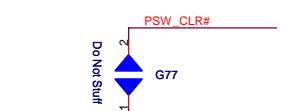
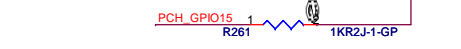
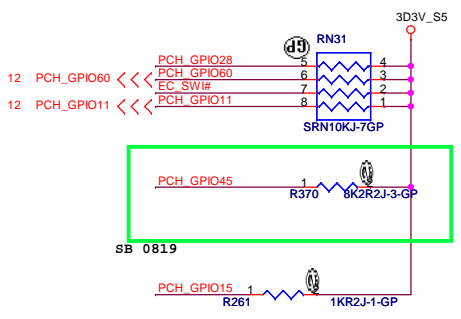
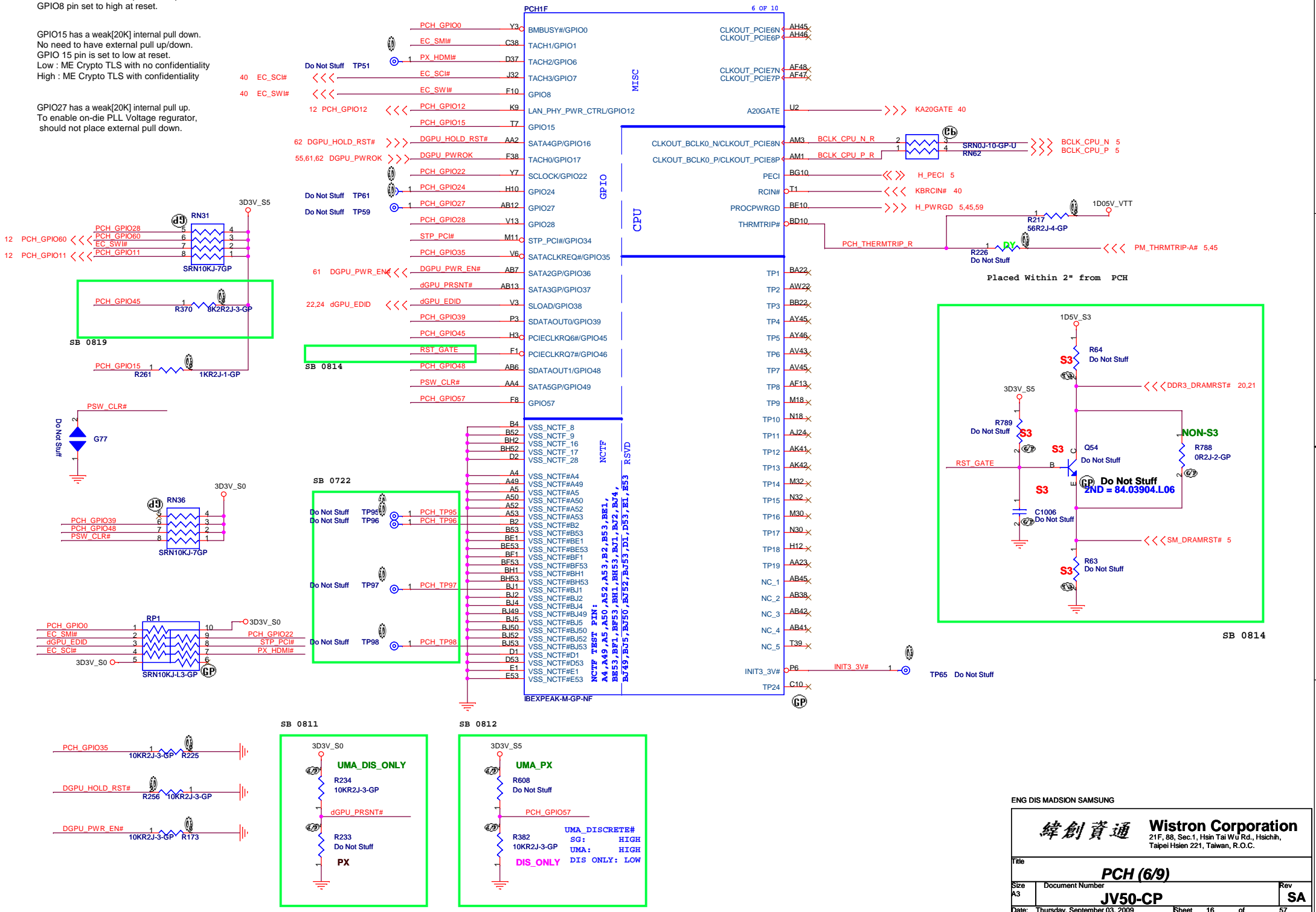
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GPIO8 has a weak[20K] internal pull up.  
No need to have external pull down/up.  
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.  
No need to have external pull up/down.  
GPIO 15 pin is set to low at reset.  
Low : ME Crypto TLS with no confidentiality  
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.  
To enable on-die PLL Voltage regulator,  
should not place external pull down.



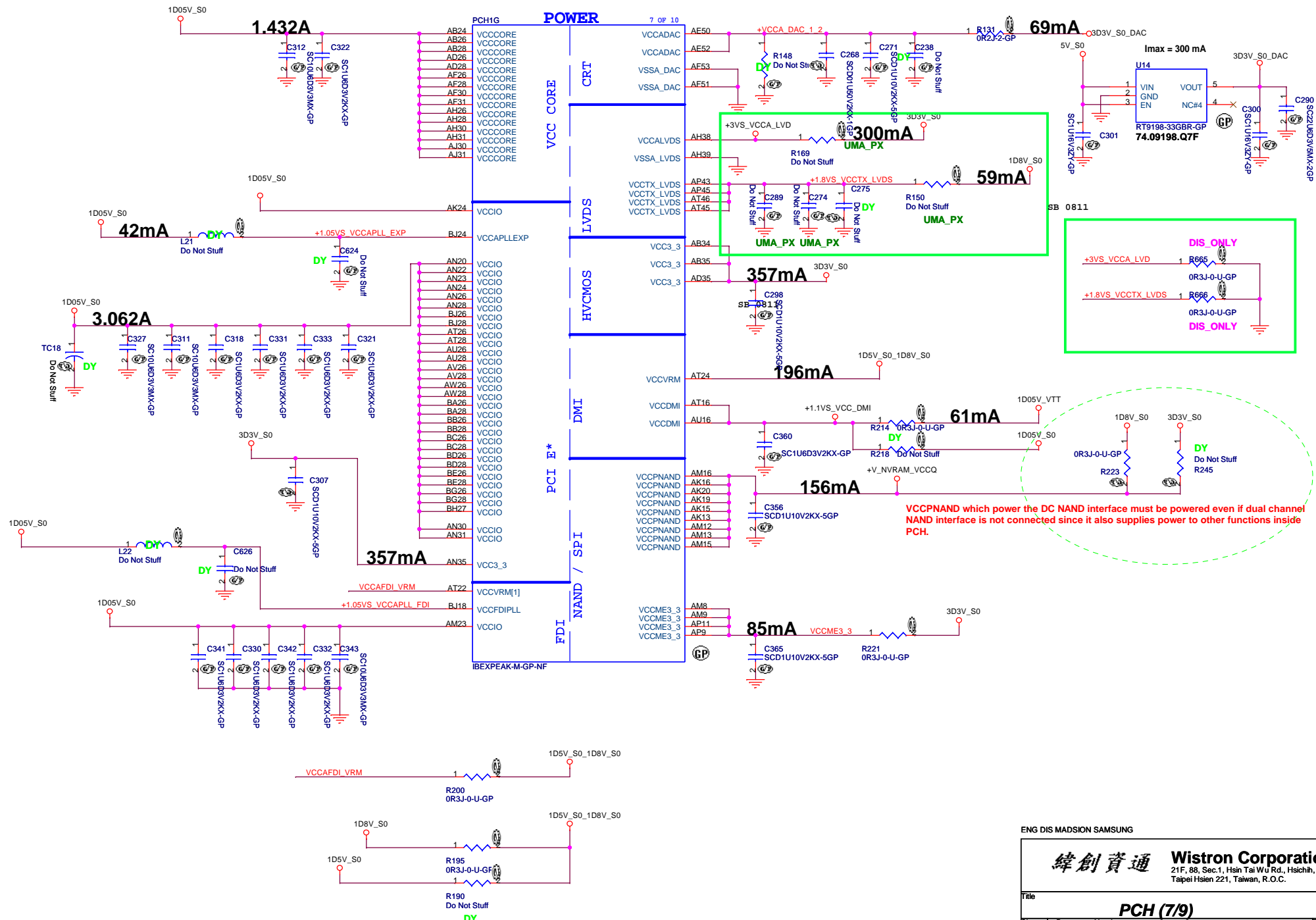
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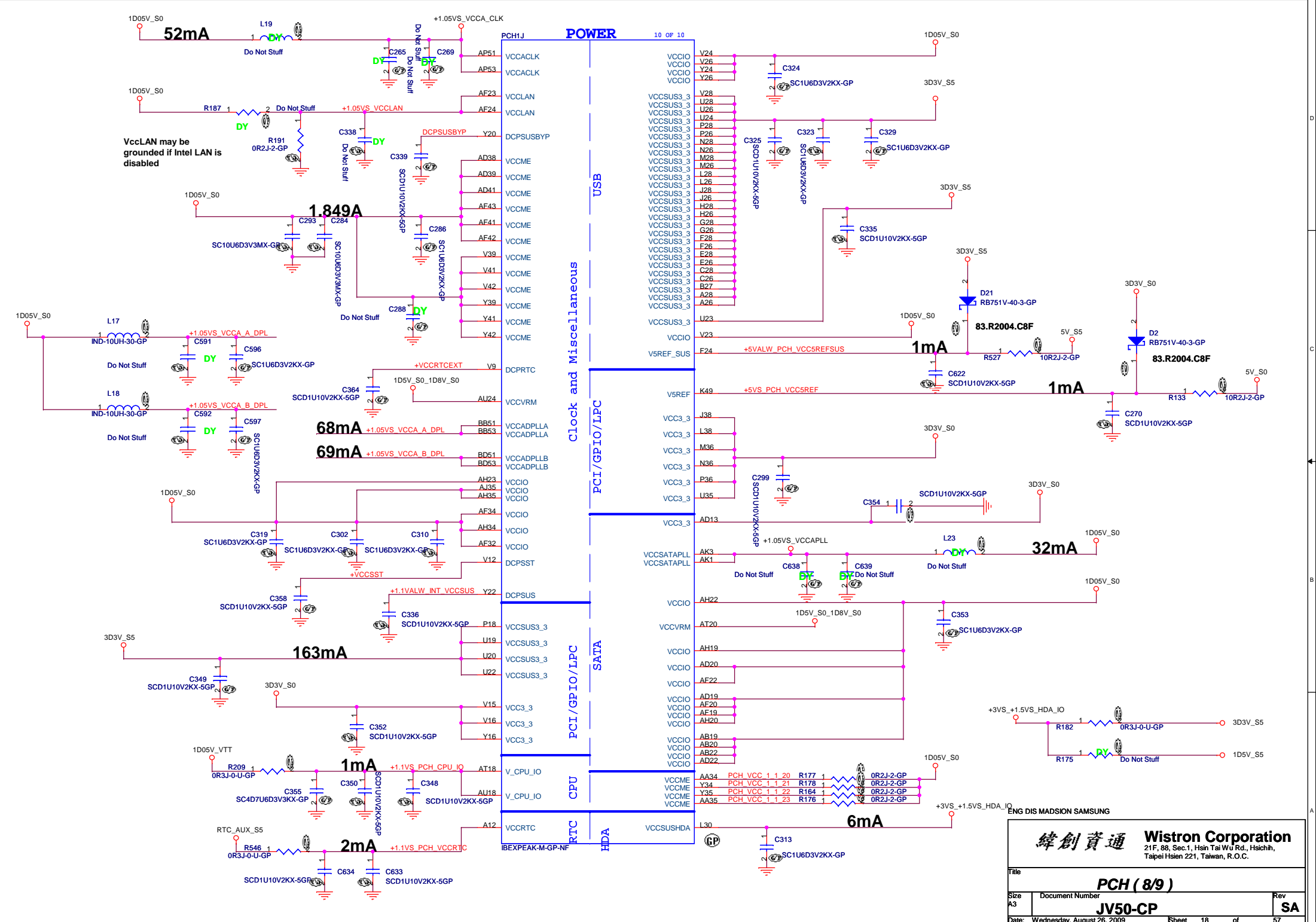
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Title: **PCH (6/9)**

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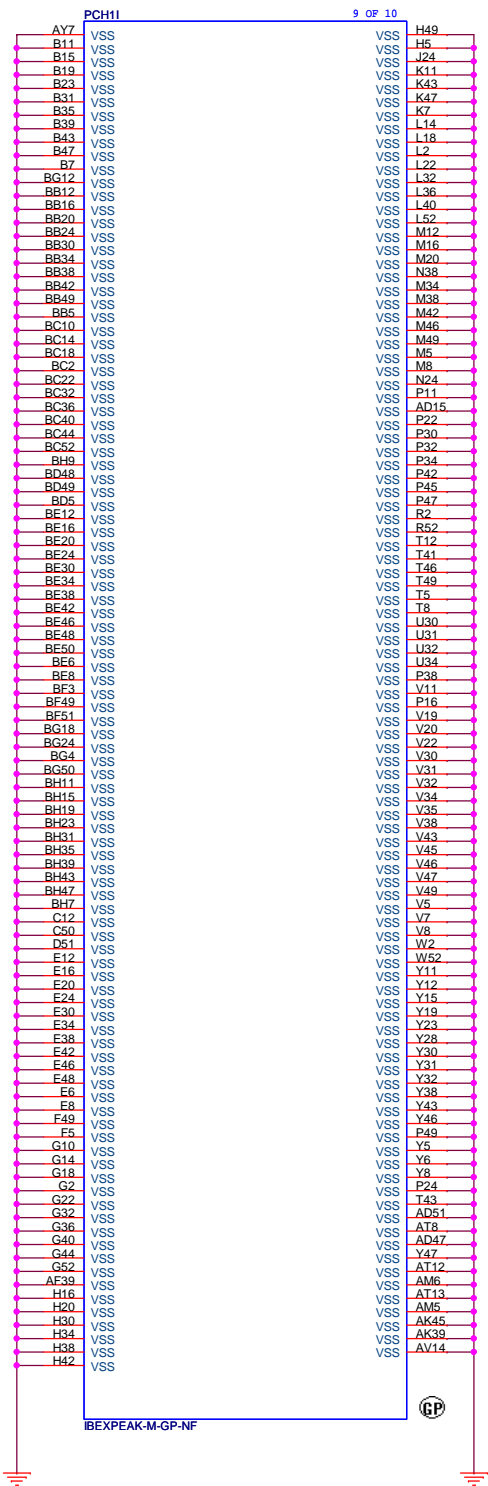
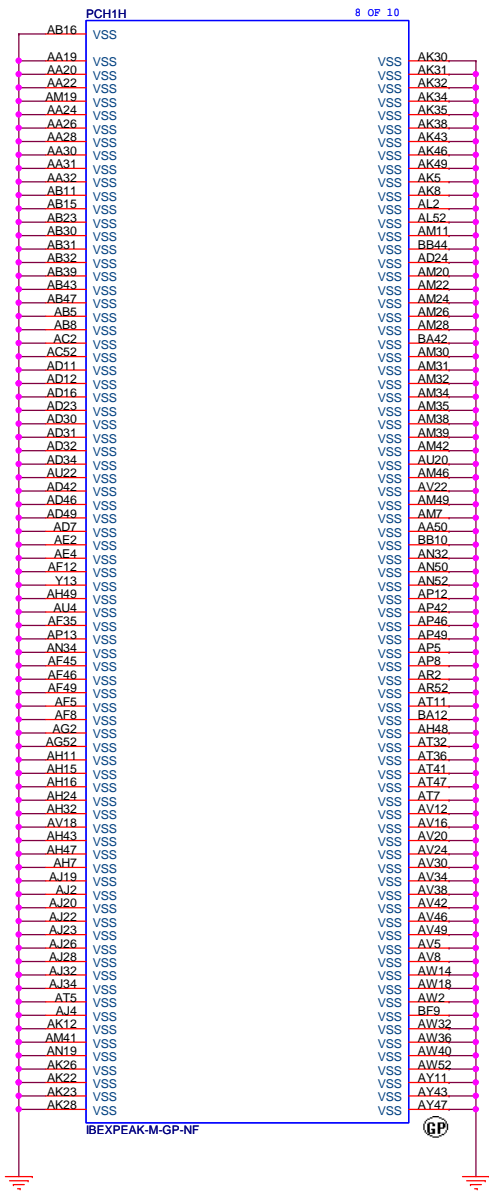


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Title: **PCH ( 8/9 )**

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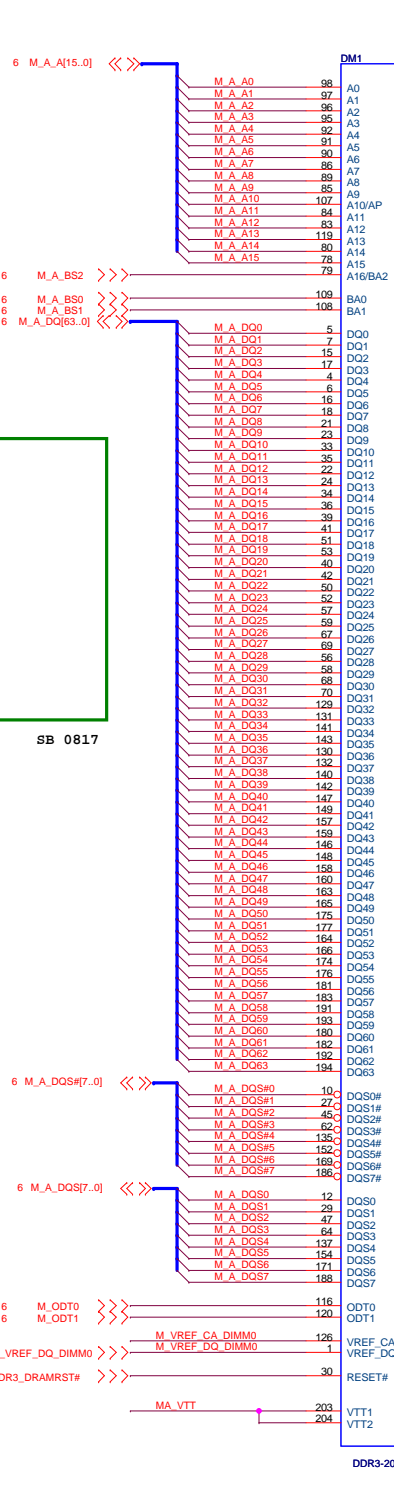
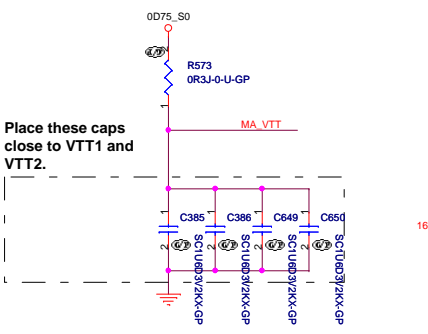
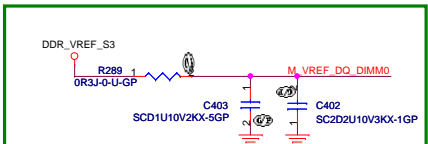
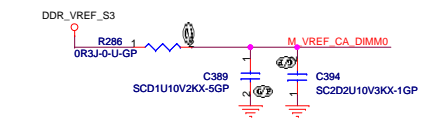
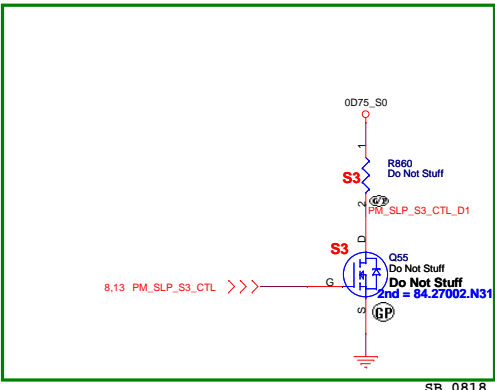


ENG DIS MADSON SAMSUNG

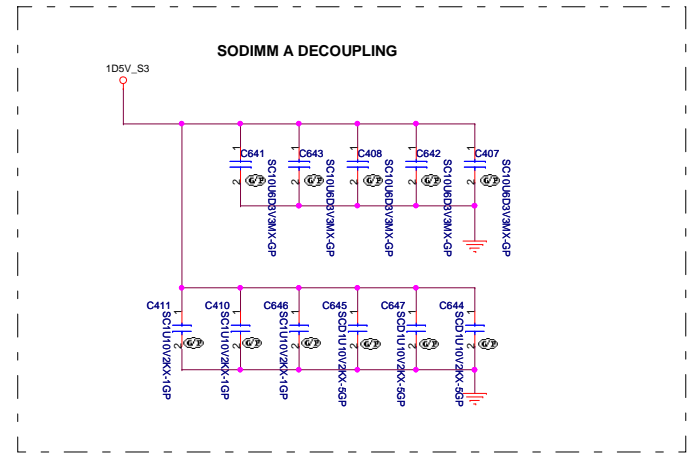
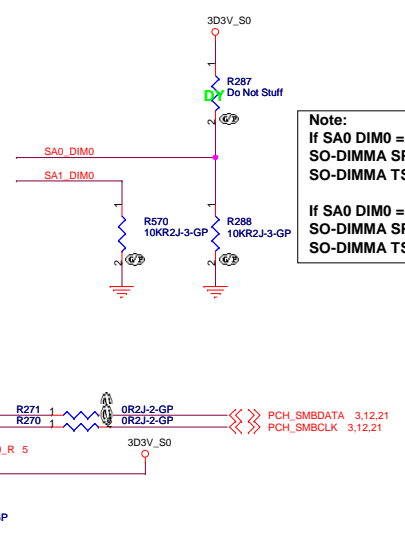
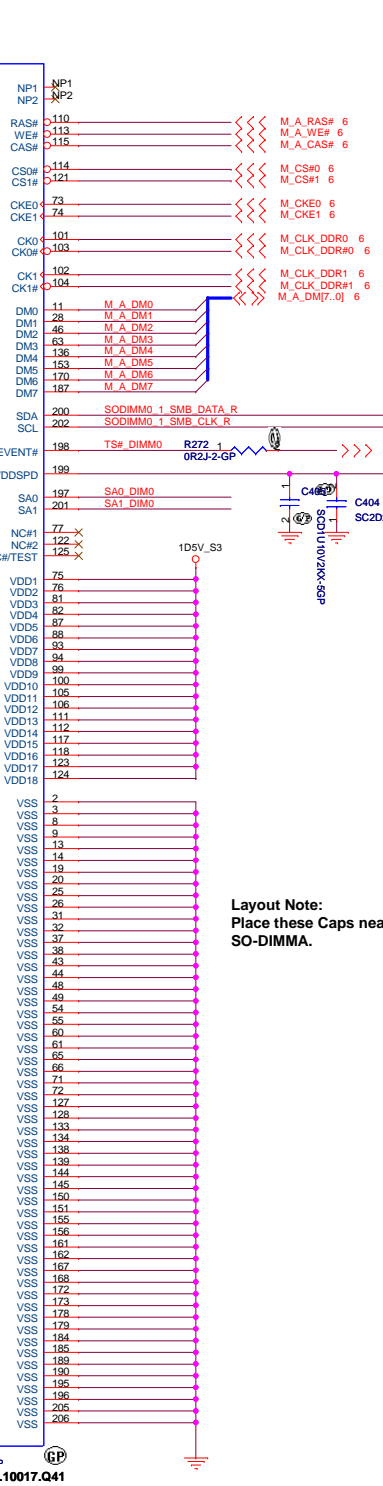
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (9/9)**

Size A3	Document Number <b>JV50-CP</b>	Rev <b>SA</b>
Date: Tuesday, August 18, 2009	Sheet 19	of 57



**REVERSE TYPE**

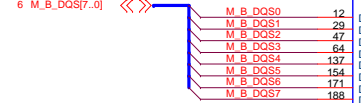
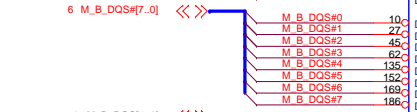
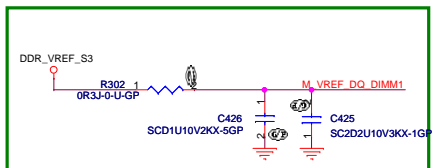
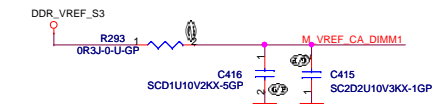


Layout Note:  
Place these Caps near SO-DIMMA.

H = 9.2mm 2ND = 62.10017.N61



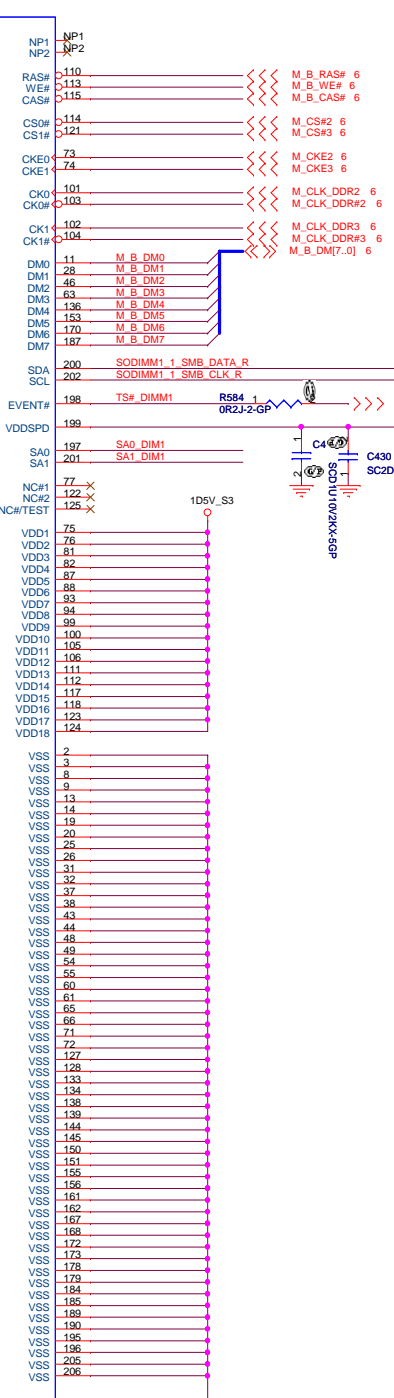
SB 0817



Place these caps close to VTT1 and VTT2.

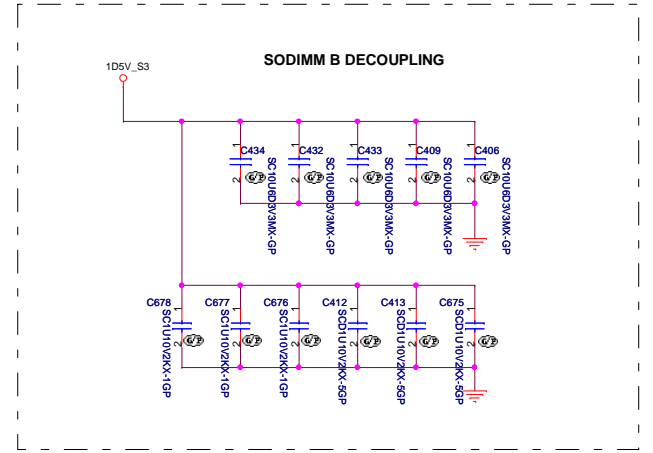
Note:  
SO-DIMMB SPD Address is 0x44  
SO-DIMMB TS Address is 0x34

# REVERSE TYPE



62.10017.P61 2ND = 62.10017.N41

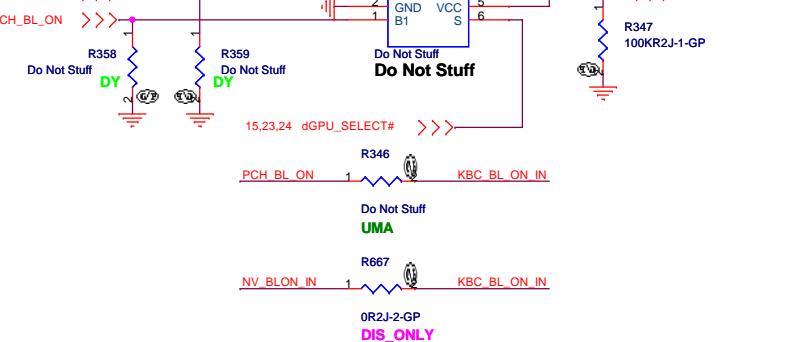
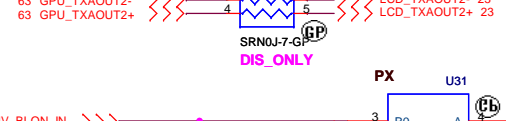
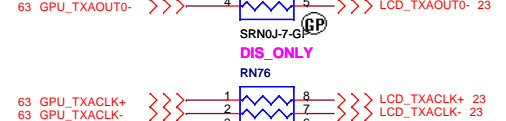
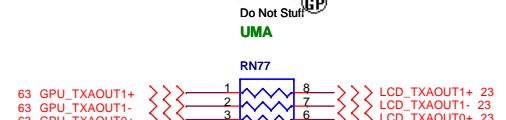
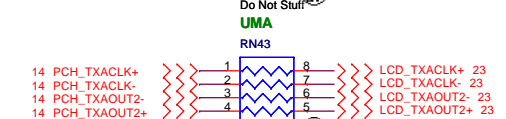
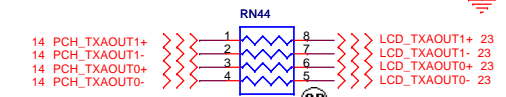
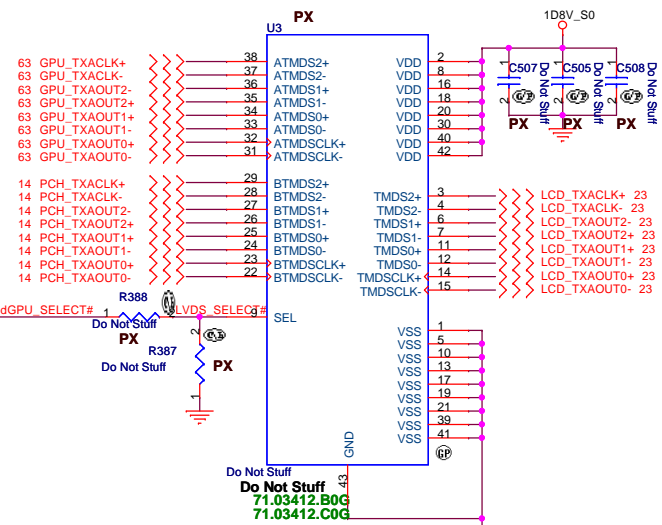
SO-DIMMB is placed farther from the Processor than SO-DIMMA



ENG DIS MADISON SAMSUNG

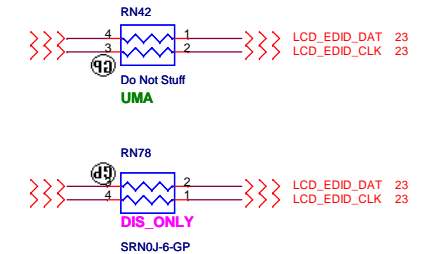
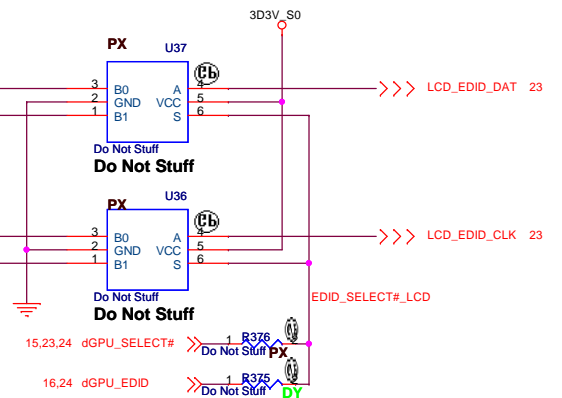
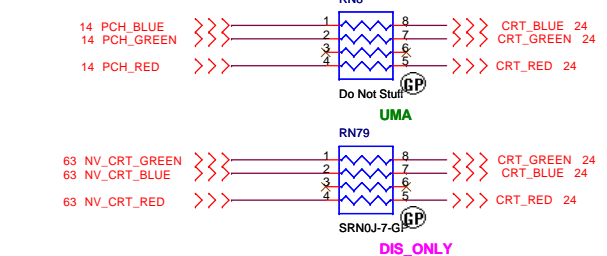
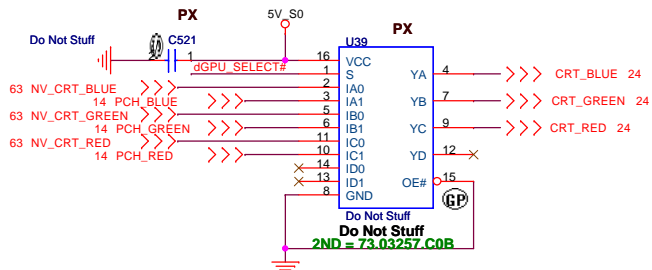
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Title: **DDRIII Socket DM2**  
 Size: Custom  
 Document Number: **JV50-CP**  
 Date: Thursday, September 03, 2009 Sheet 21 of 57



**FUNCTION TABLE**

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMSn+ TMDSn- = ATMSn- TMDSCLK+ = ATMSCLK+ TMDSCLK- = ATMSCLK- BTMSn+ = High Impedance BTMSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMSn+ TMDSn- = BTMSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMSn+ = High Impedance ATMSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-



$\bar{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

ENG DIS MADISON SAMSUNG

**緯創資通 Wistron Corporation**  
 21F, 86, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

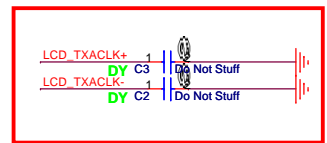
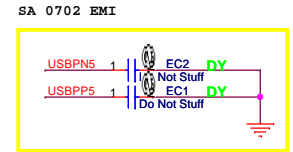
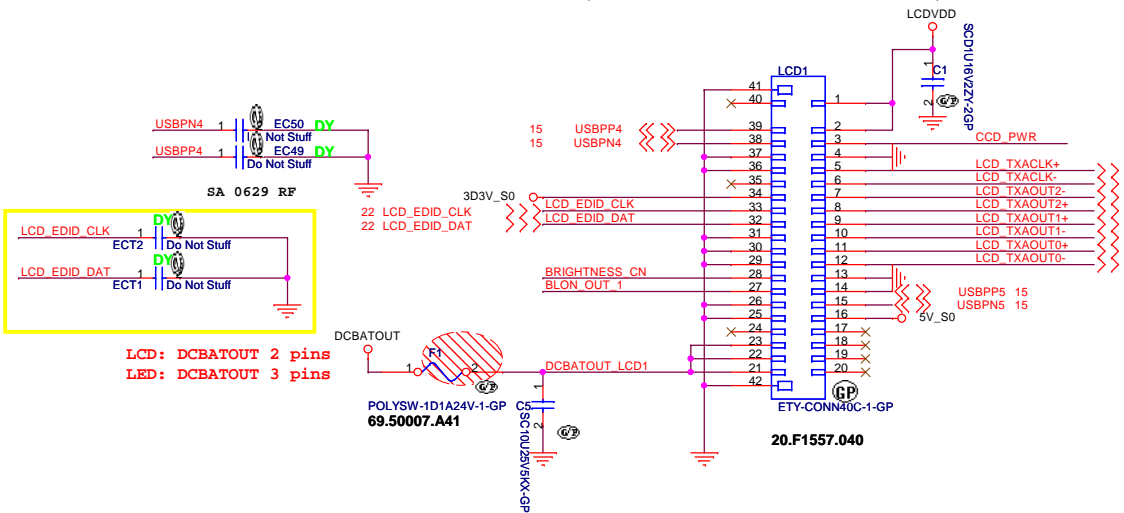
Title: **PX SWITCH**

Size A3 Document Number: **JV50-CP** Rev: **SA**

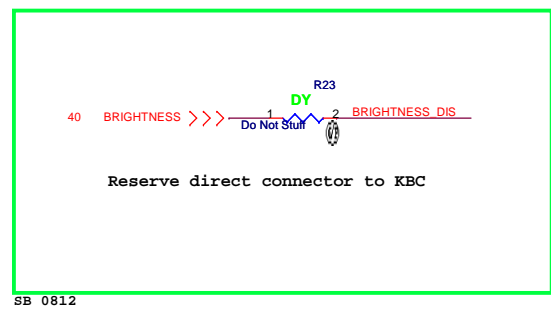
Date: Thursday, September 03, 2009 Sheet 22 of 57



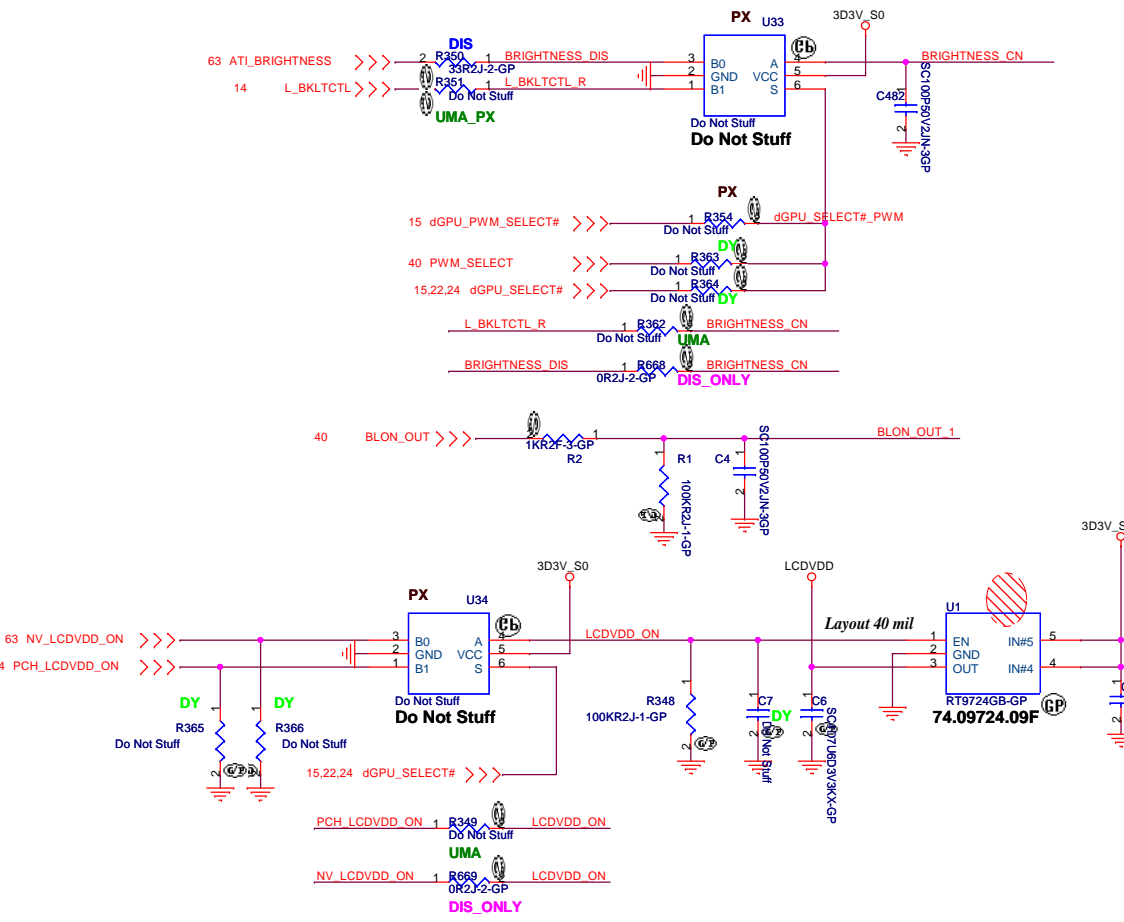
# LCD/INVERTER/CCD CONN



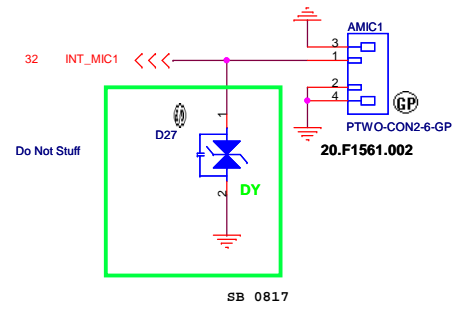
modify by RF



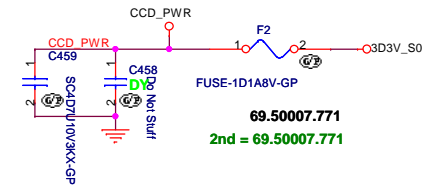
SB 0812



## Internal Mic



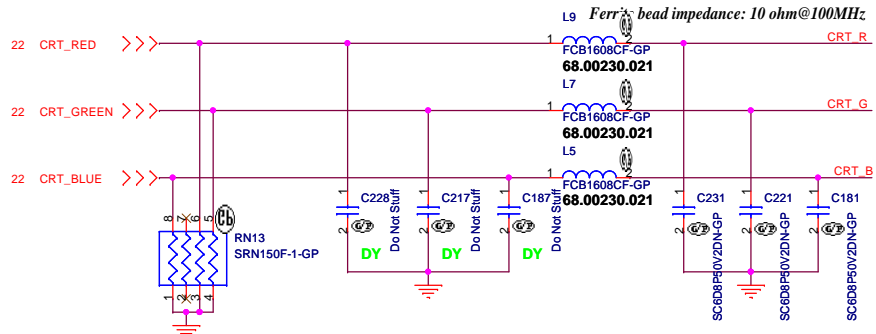
SB 0817



ENG DIS MADSION SAMSUNG

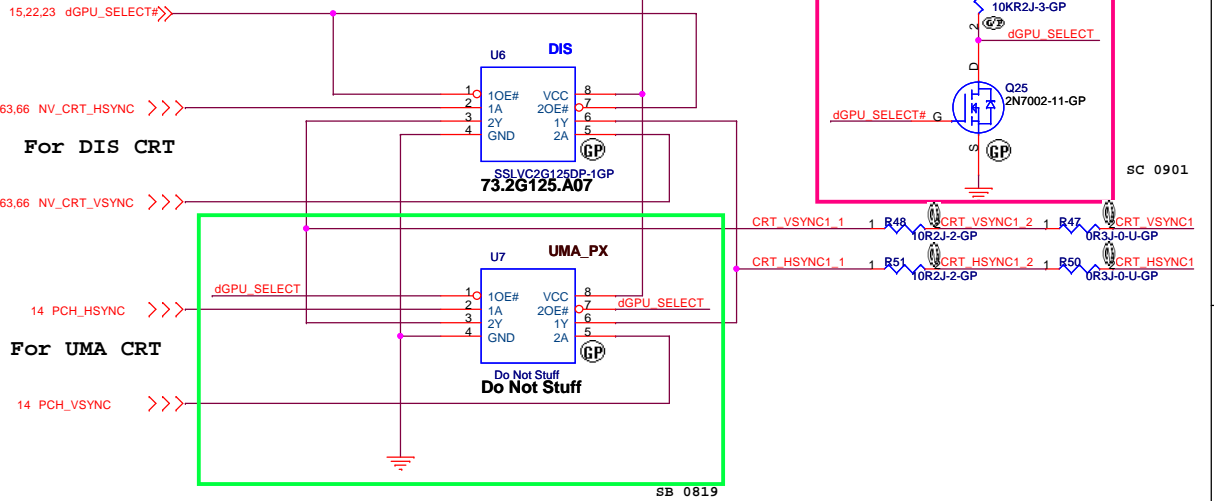
<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>LCD CONN</b>			
File	Document Number		Rev
	<b>JV50-CP</b>		SA
Date: Thursday, September 03, 2009	Sheet	23	of 61

Layout Note:  
Place these resistors  
close to the CRT-out  
connector

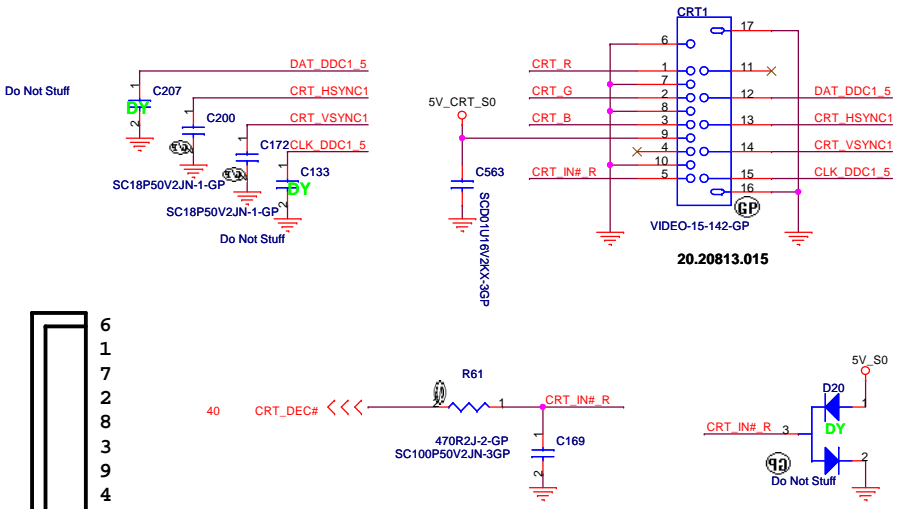


**Layout Note:**  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

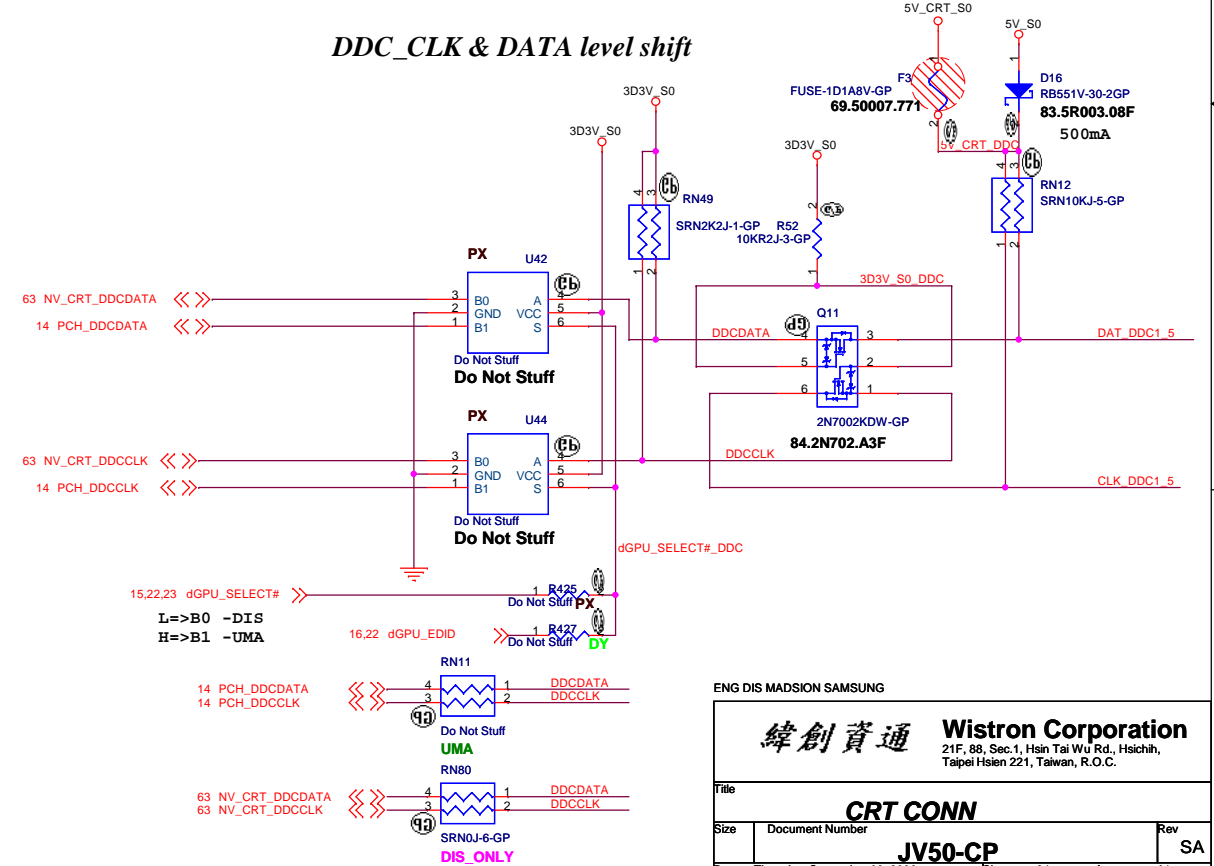
L=>B0 -DIS  
H=>B1 -UMA



### CRT I/F & CONNECTOR



### DDC\_CLK & DATA level shift



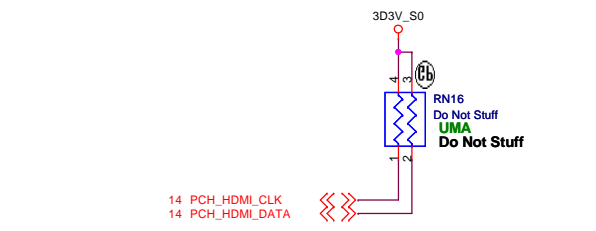
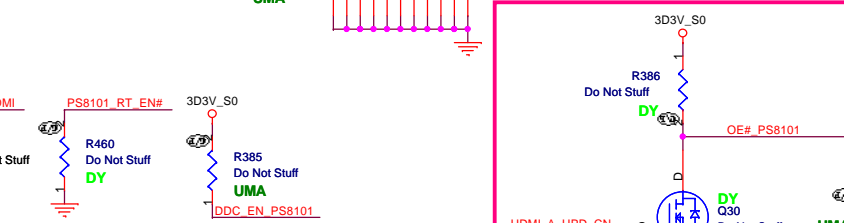
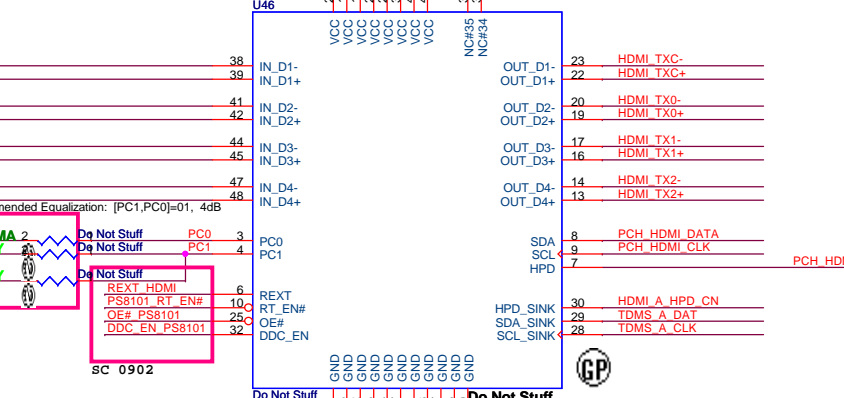
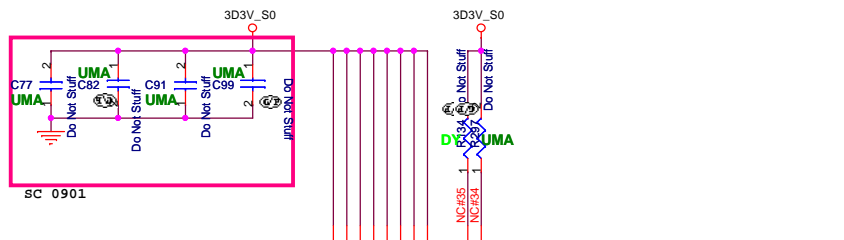
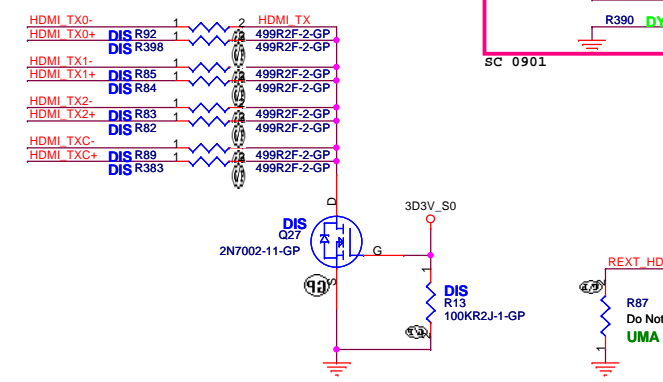
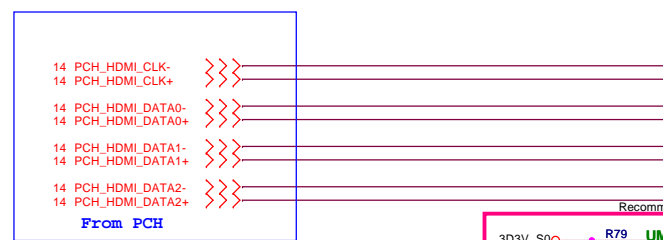
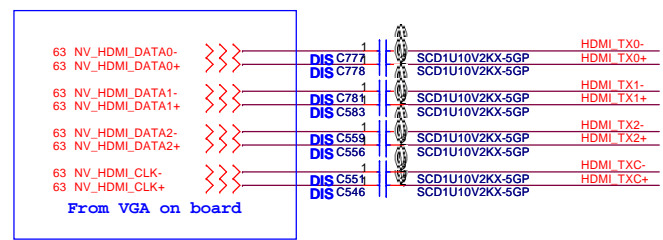
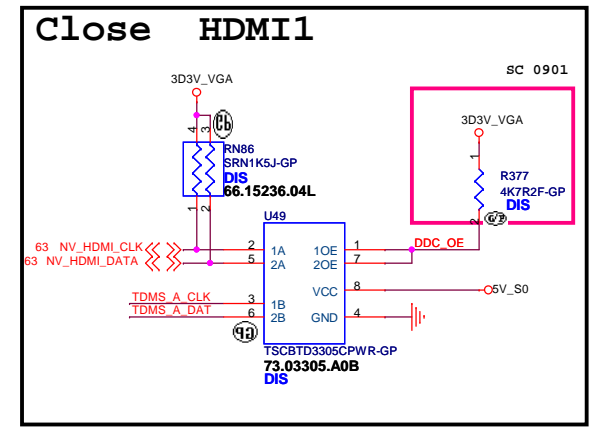
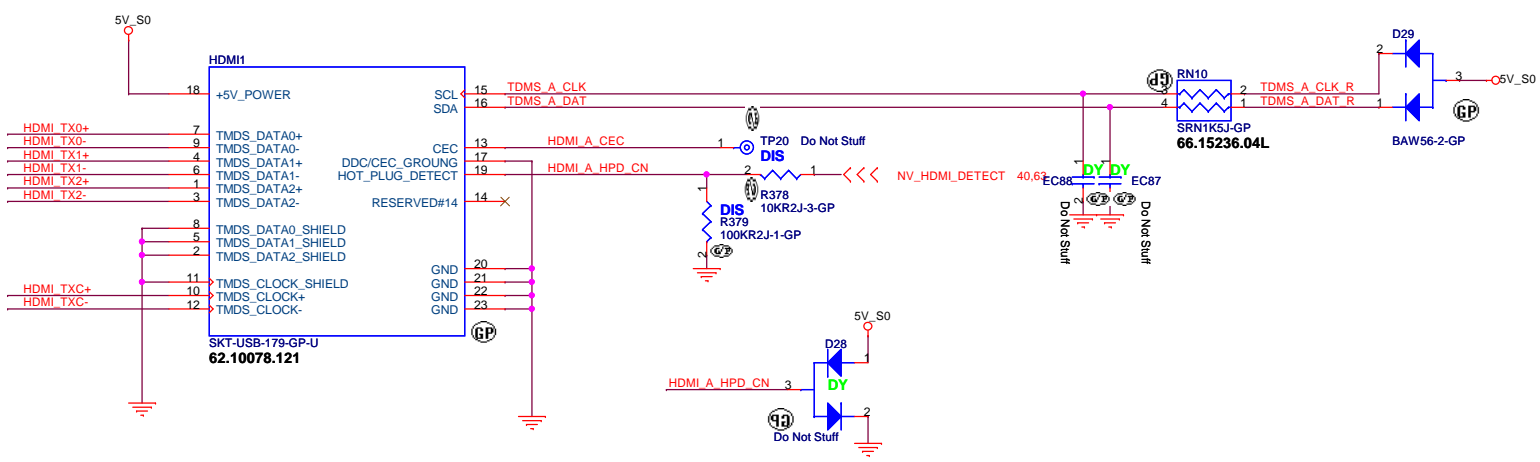
ENG DIS MADSION SAMSUNG

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Title: **CRT CONN**

Size: Document Number: **JV50-CP** Rev: SA

Date: Thursday, September 03, 2009 Sheet 24 of 61



ENG DIS MADSION SAMSUNG

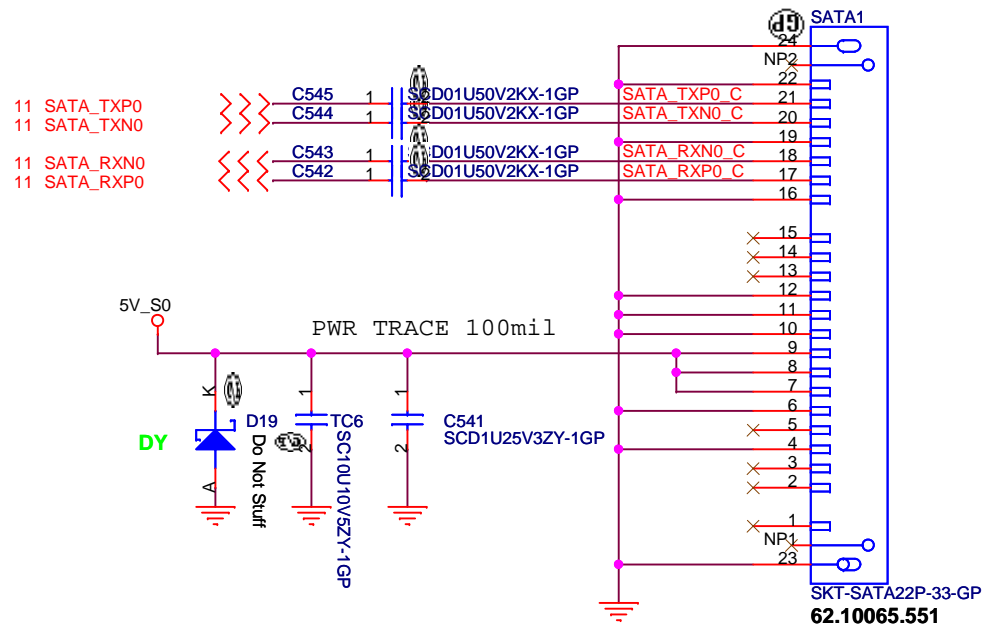
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI CONNECTOR**

Size: Document Number: **JV50-CP** Rev: SA

Date: Thursday, September 03, 2009 Sheet 25 of 57

# SATA Connector



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**緯創資通** **Wistron Corporation**  
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 Taipei Hsien 221, Taiwan, R.O.C.

Title

**HDD CONN**

Size Document Number

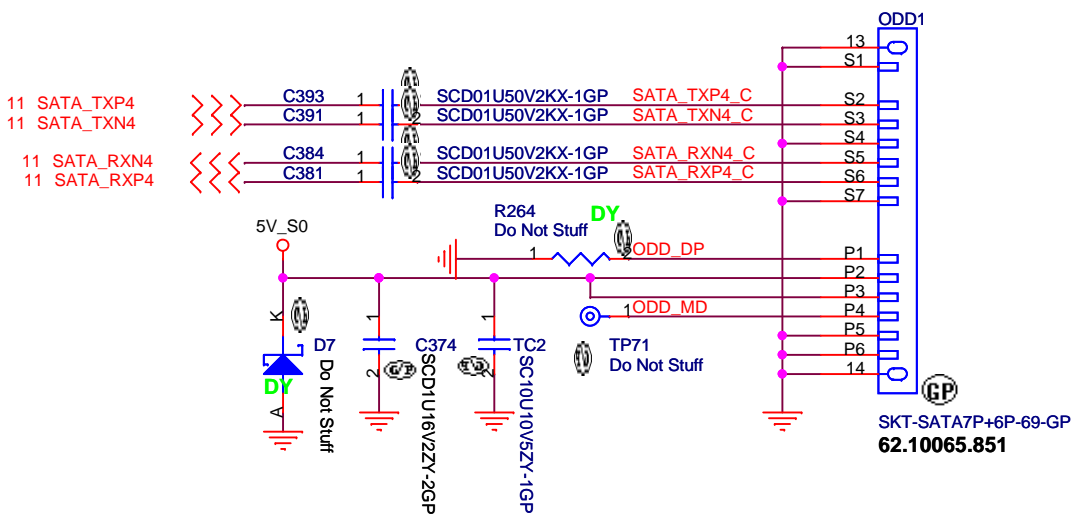
**JV50-CP**

Rev  
SA

Date: Thursday, September 03, 2009

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# ODD Connector

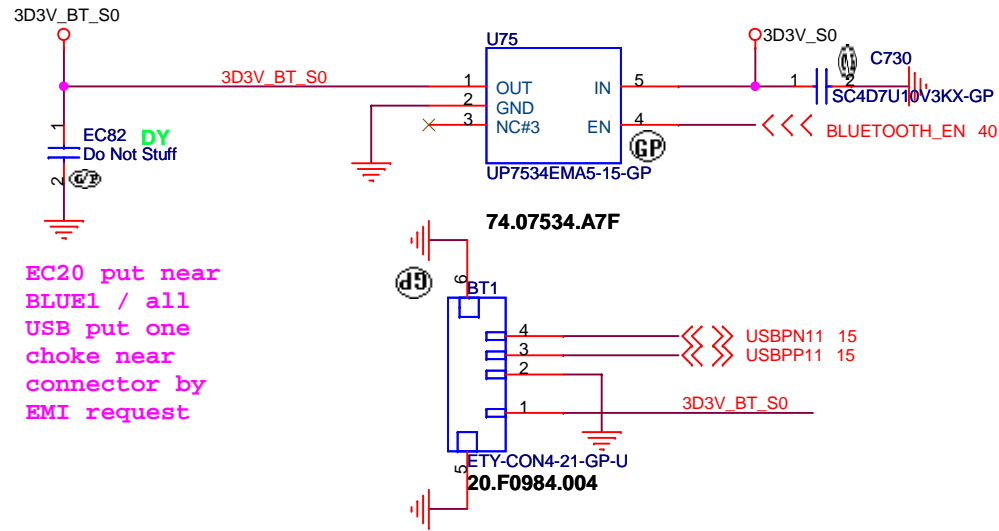


ENG DIS MADSION SAMSUNG

**緯創資通** **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title		
<b>ODD</b>		
Size	Document Number	Rev
	<b>JV50-CP</b>	<b>SA</b>
Date:	Thursday, September 03, 2009	Sheet 27 of 61

# BLUETOOTH MODULE



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緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**BLUETOOTH**

Size

Document Number

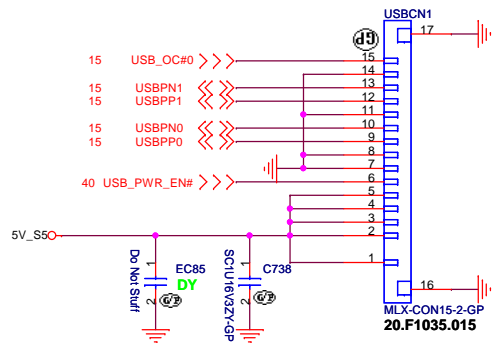
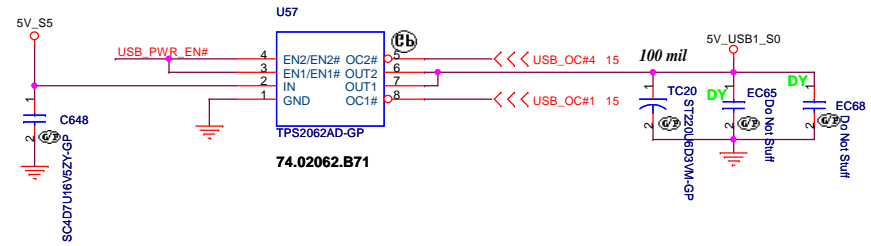
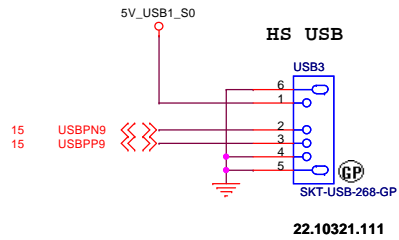
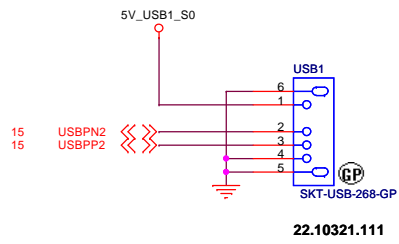
**JV50-CP**

Rev

SA

Date: Thursday, September 03, 2009

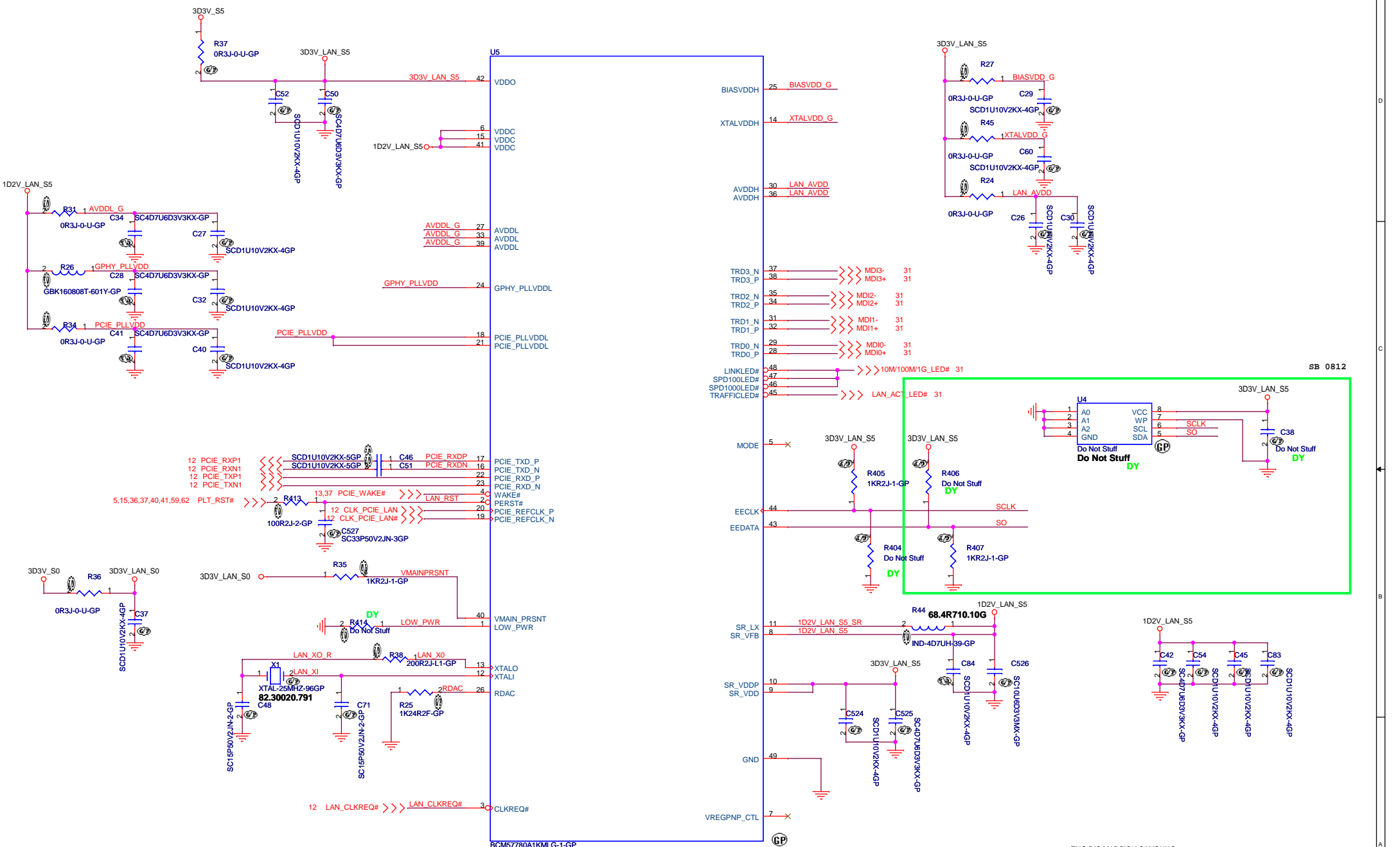
Sheet 28 of 61



ENG DIS MADSION SAMSUNG

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>USB CONN</b>			
Size	Document Number	Rev	SA
	<b>JV50-CP</b>		
Date:	Thursday, September 03, 2009	Sheet	29 of 61





71.57780.M04

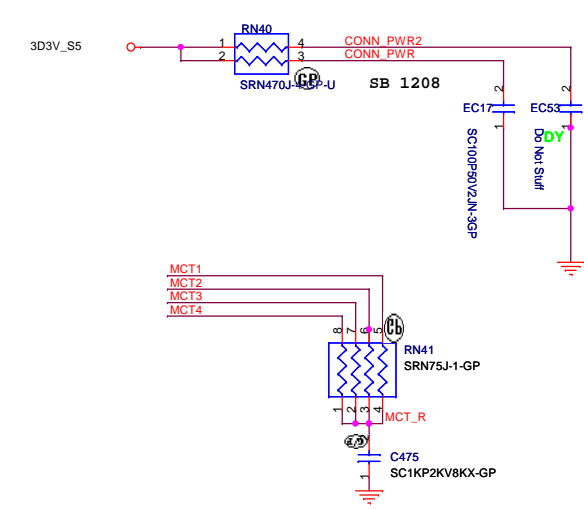
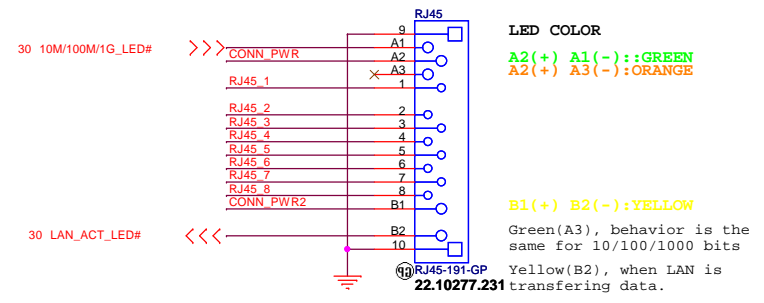
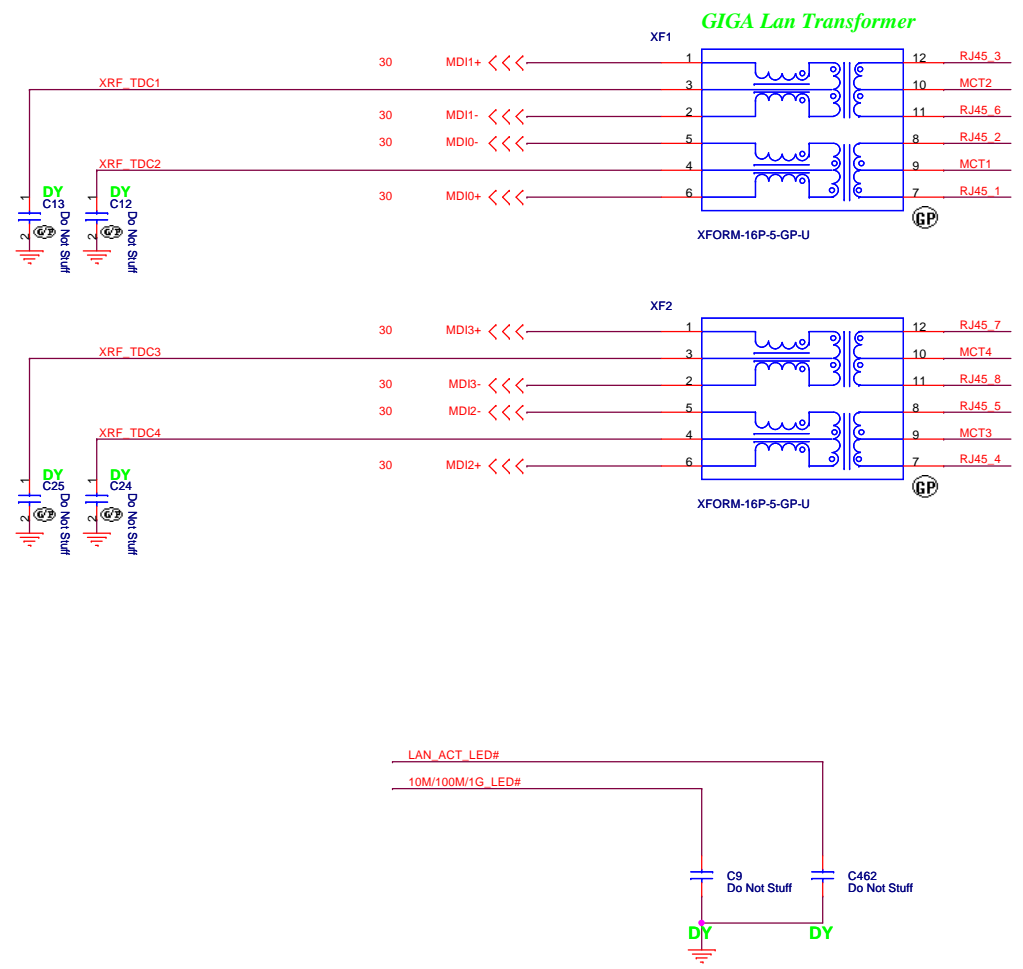
ENG DIS MADSION SAMSUNG

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>BCM57780</b>			
Size	Document Number		Rev
Custom	<b>JV50-CP</b>		<b>SA</b>
Date:	Thursday, September 03, 2009	Sheet 30	of 61

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

# LAN Connector

# LAN Connector

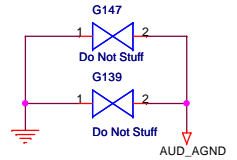
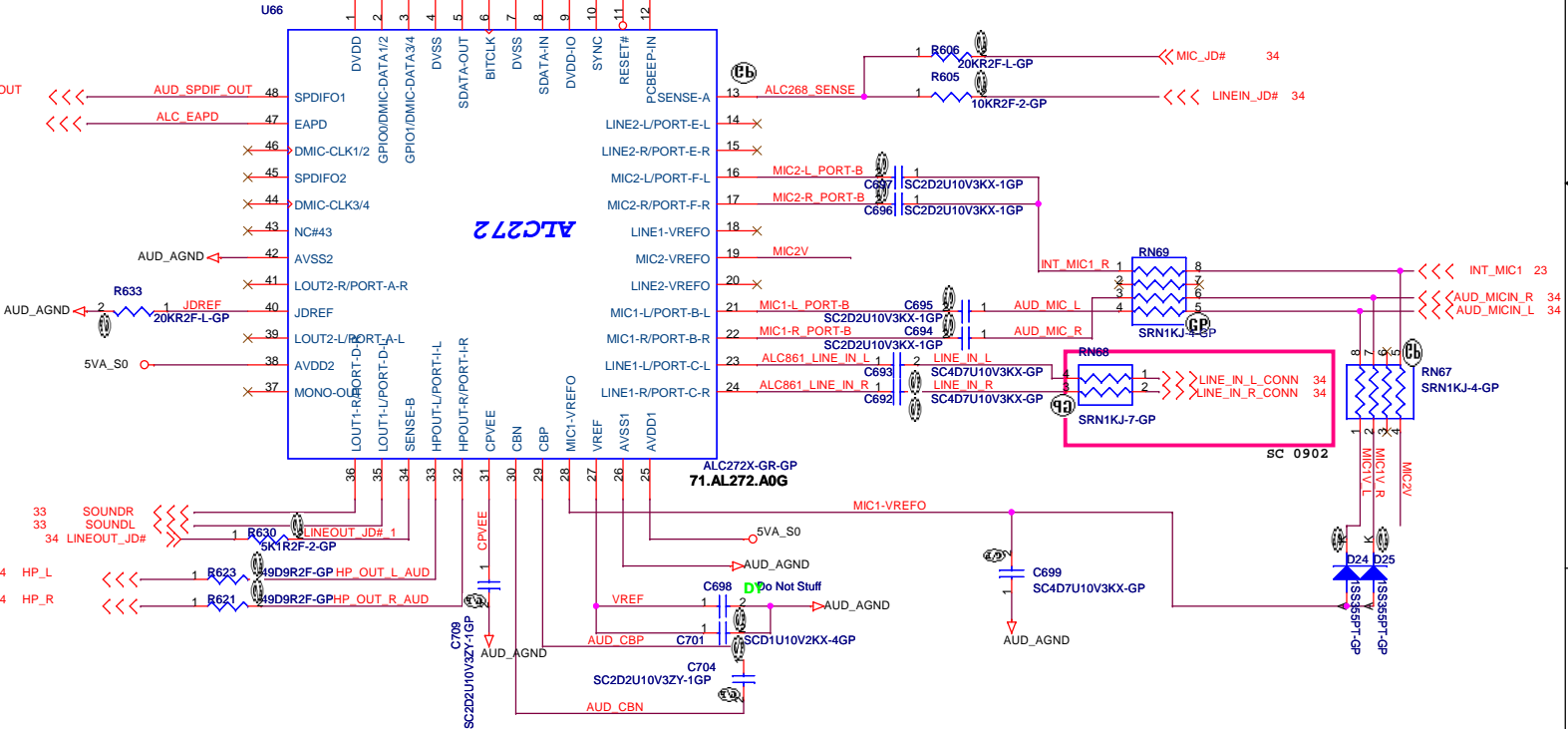
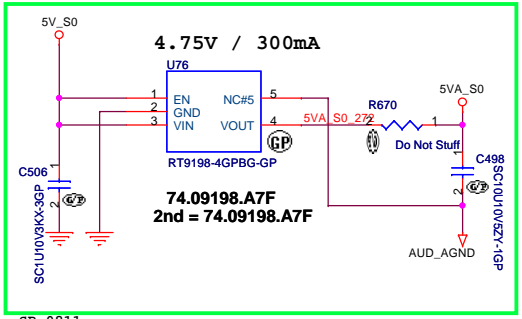
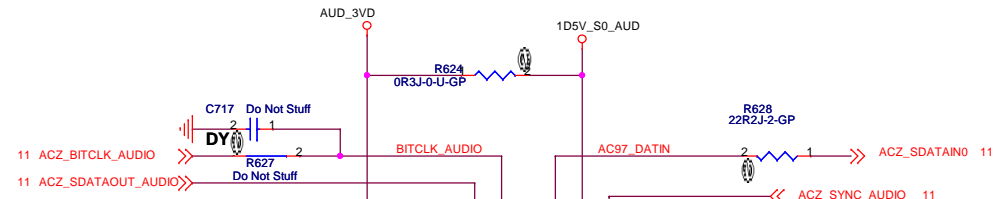
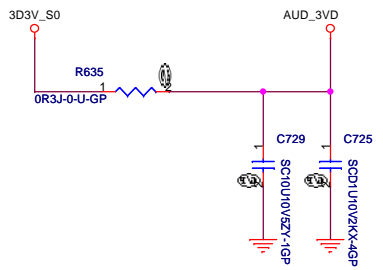
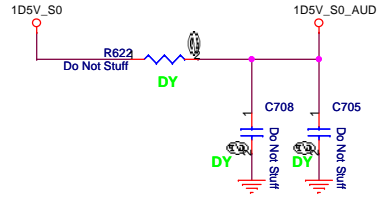
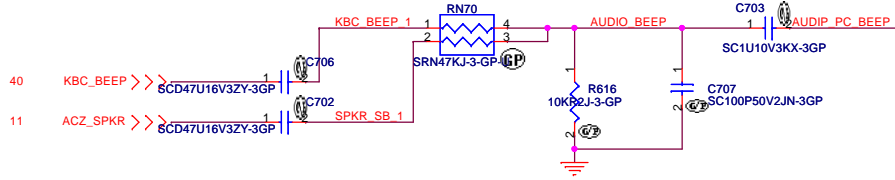


ENG DIS MADSION SAMSUNG

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Title: **LAN CONN**

Size A3	Document Number <b>JV50-CP</b>	Rev <b>SA</b>
Date: Thursday, September 03, 2009	Sheet 31 of 61	



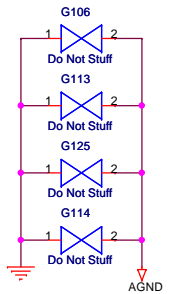
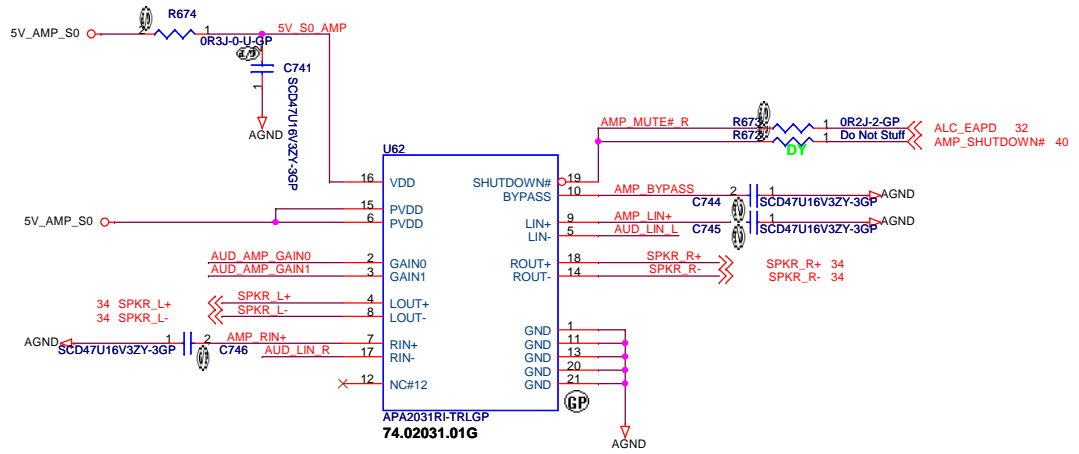
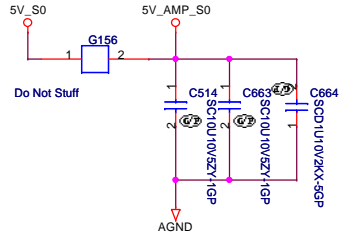
ENG DIS MADSION SAMSUNG

**緯創資通 Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

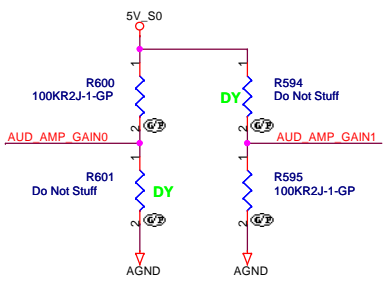
Title: **Azalia codec ALC272**

Size A3 | Document Number: **JV50-CP** | Rev: **SA**

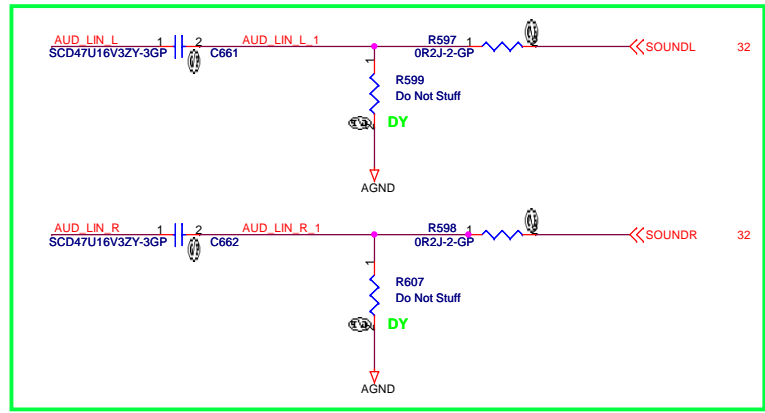
Date: Thursday, September 03, 2009 | Sheet 32 of 61



**GAIN SETTING**



GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



SB 0814

ENG DIS MADSION SAMSUNG

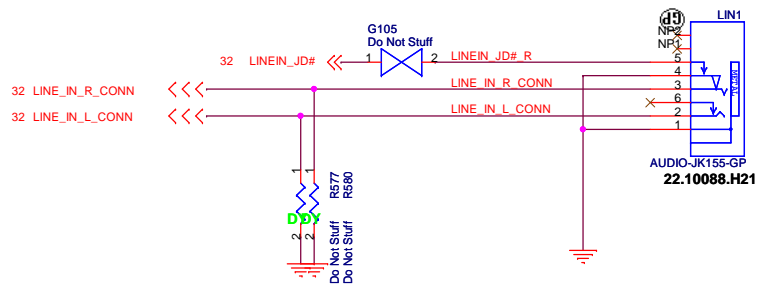
**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP**

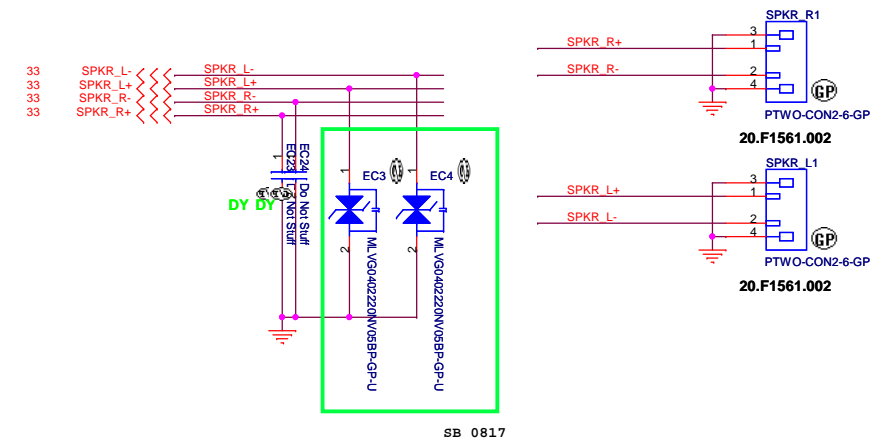
Size: Document Number **JV50-CP** Rev: **SA**

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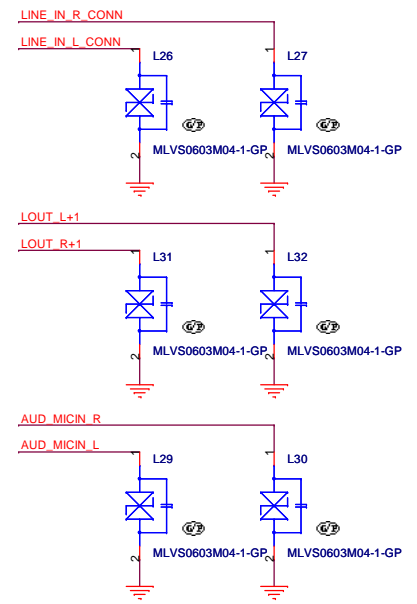
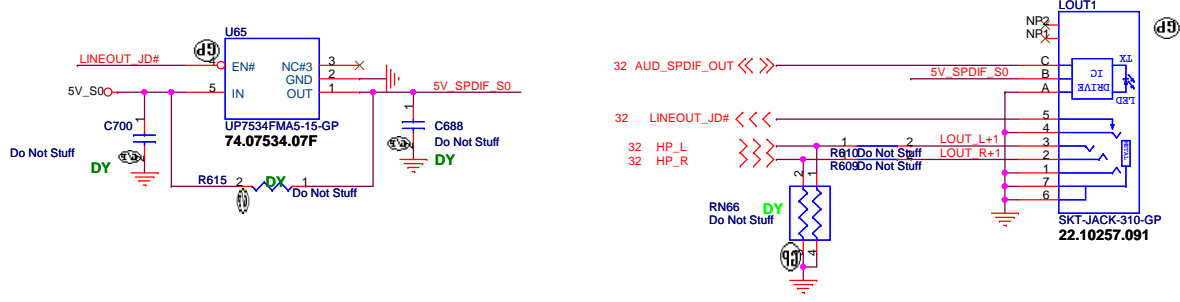
# LINE IN



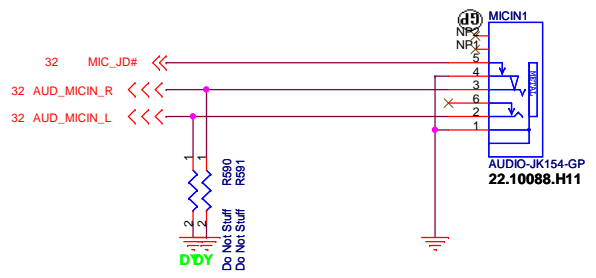
# Internal Speaker



# LINE OUT



# MIC IN



ENG DIS MADISON SAMSUNG

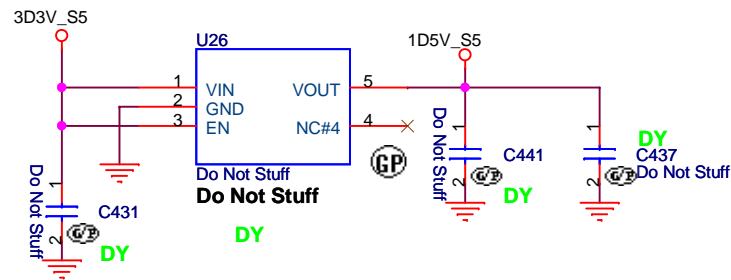
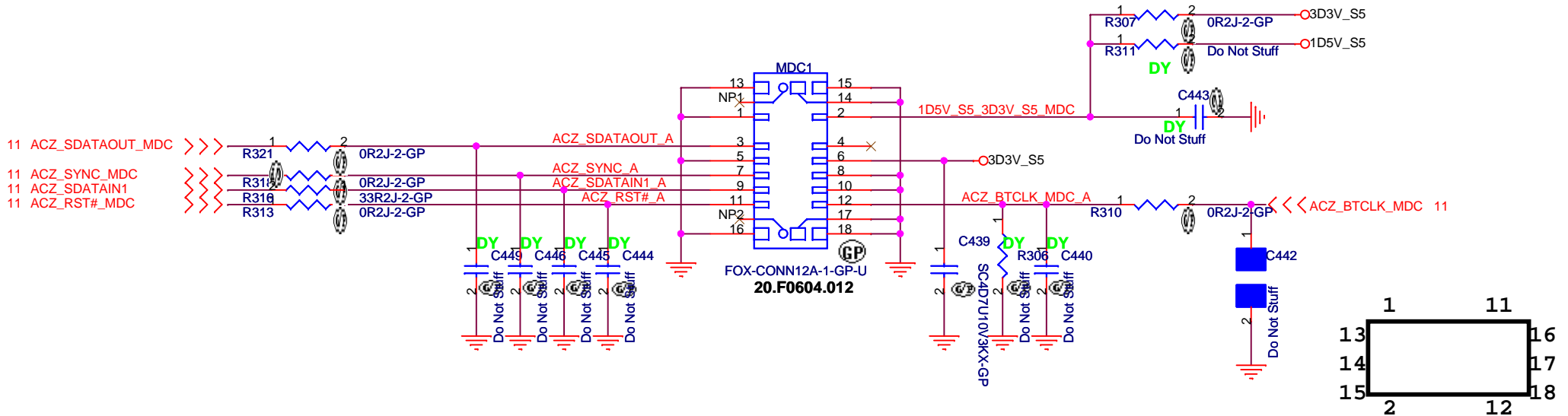
**緯創資通** **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO jack**

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# MDC 1.5 CONN



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緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**MDC**

Size

Document Number

**JV50-CP**

Rev

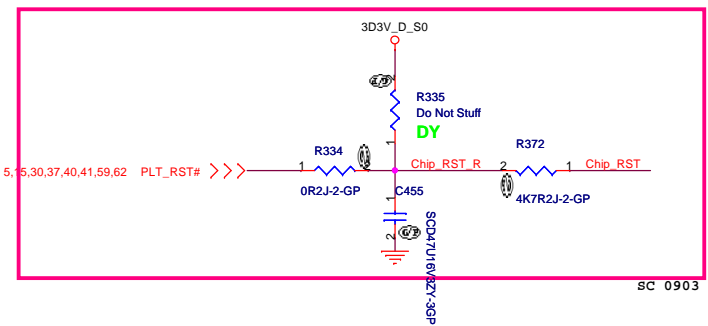
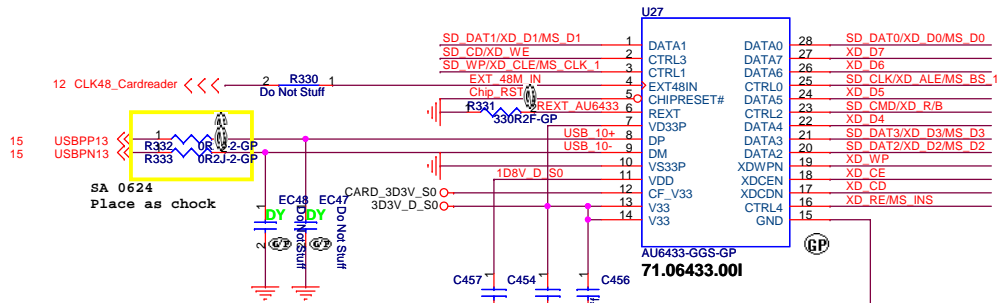
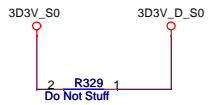
SA

Date: Thursday, September 03, 2009

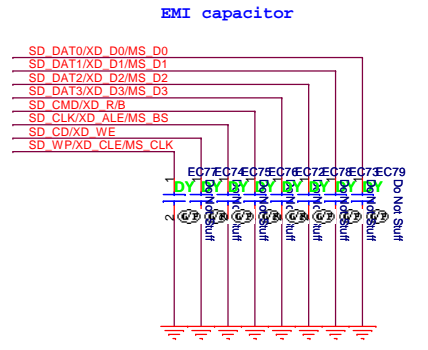
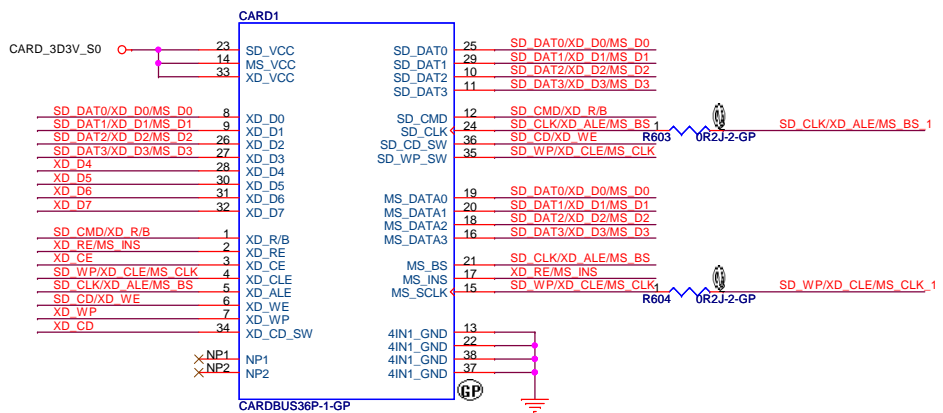
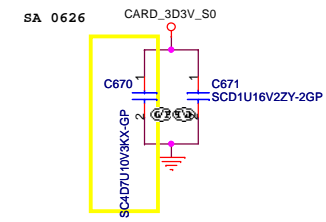
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### 5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



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**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Cardreader**

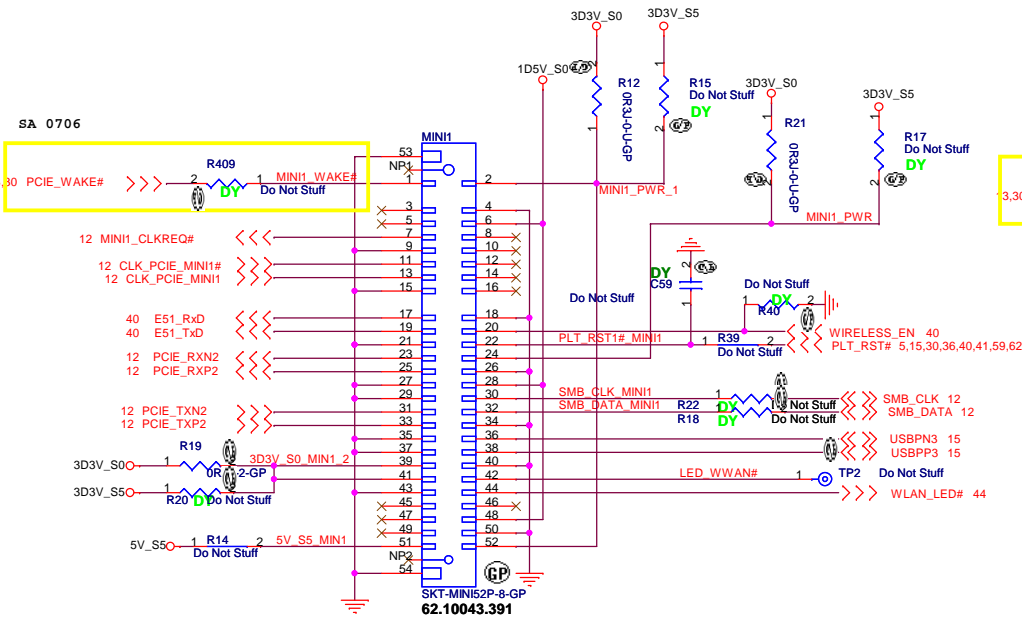
Size: Document Number **JV50-CP** Rev: SA

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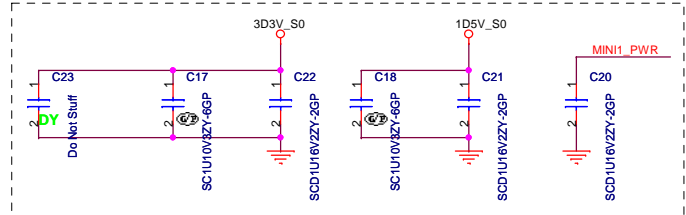


# Mini Card Connector(WLAN)

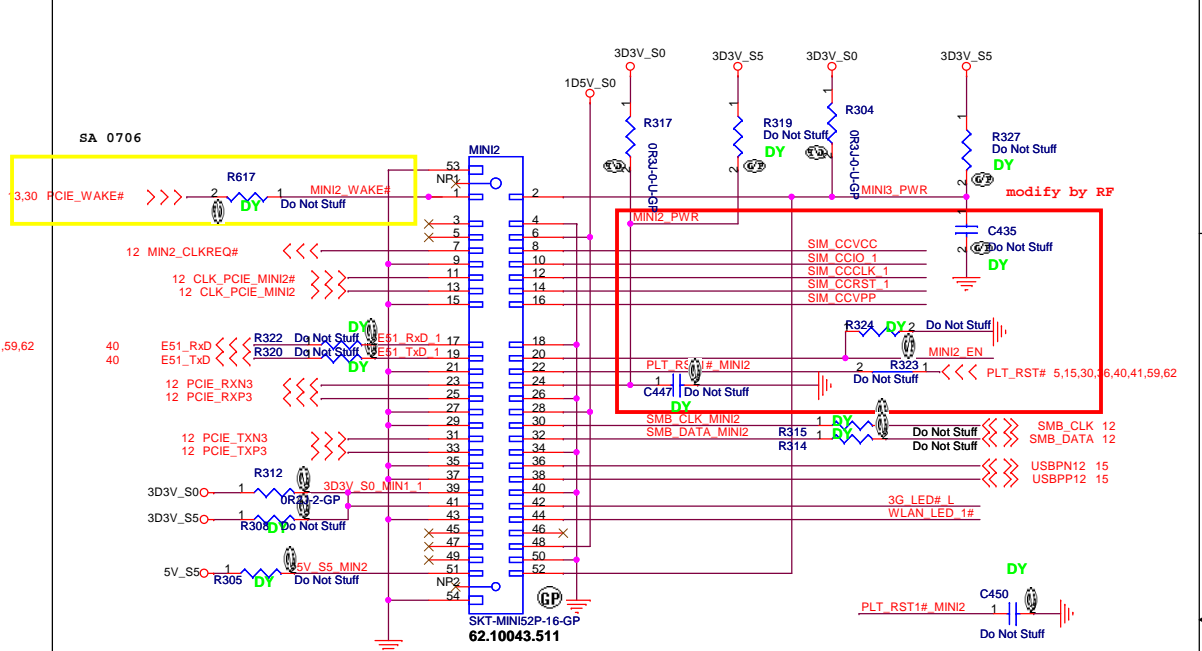
## Support debug-card



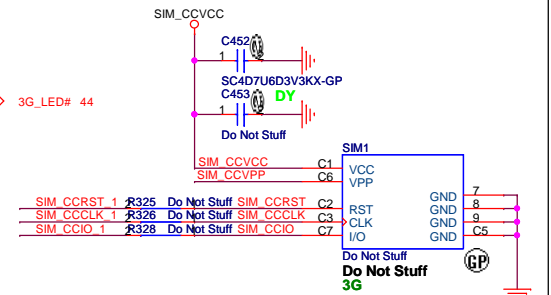
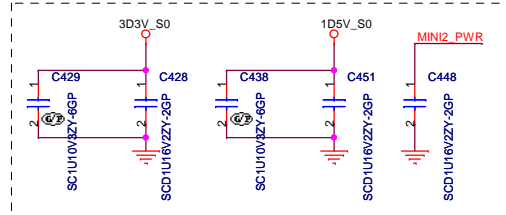
Place near MINI1



# Mini Card Connector(Robson2 and 3G)



Place near MINIC2



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**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

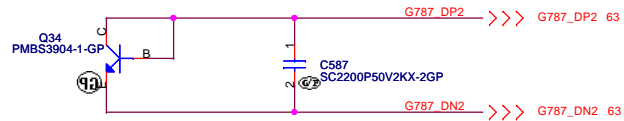
Title: **MINI CARD**

Size: A3 Document Number: **JV50-CP** Rev: **SA**

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for T8 thermal diode

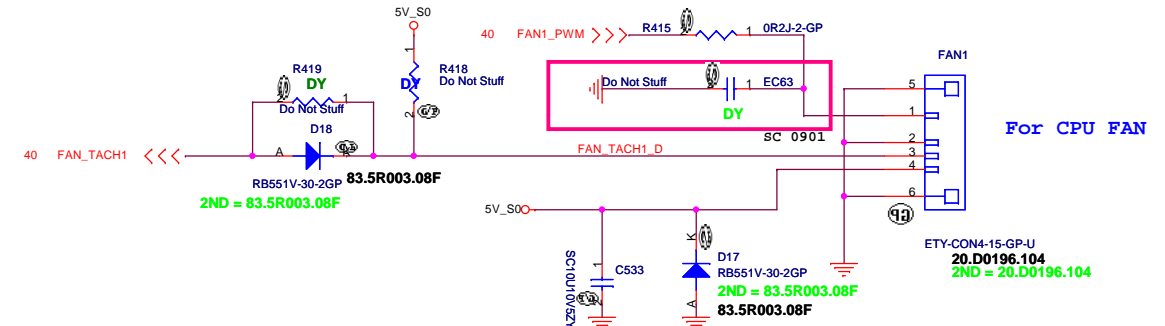
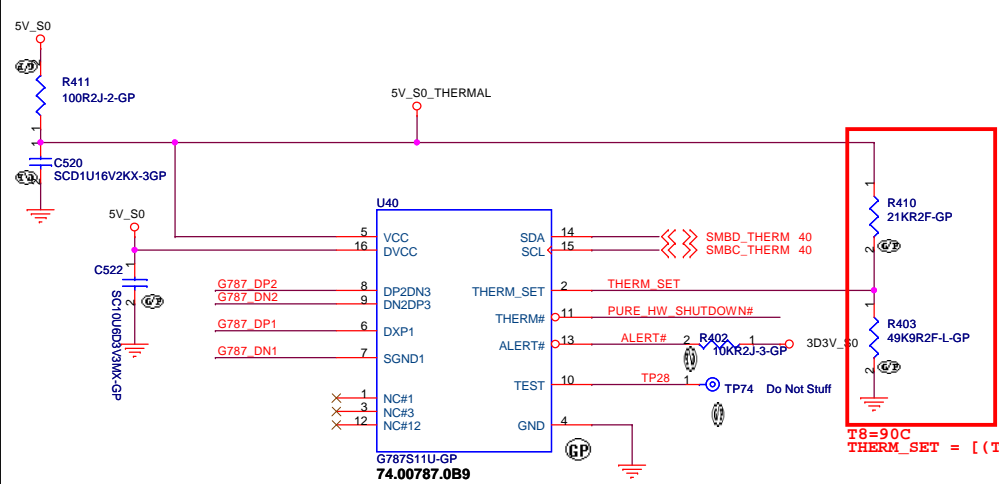
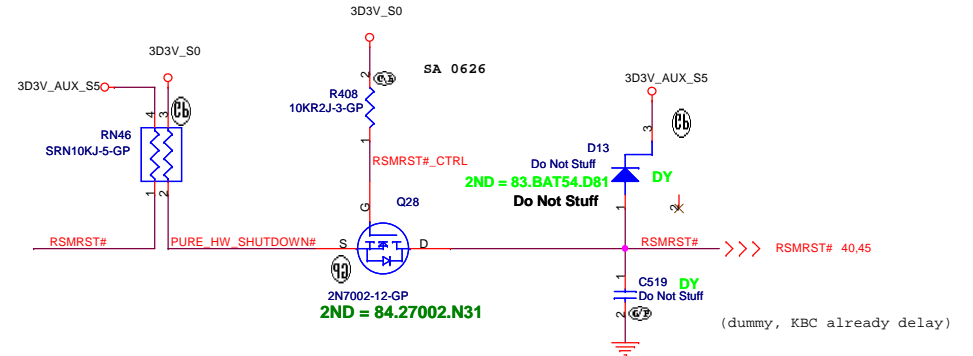
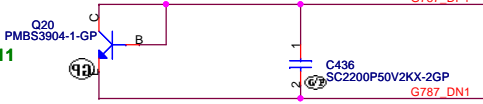
2nd = 84.03904.P11  
84.03904.L06



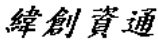
C82 & C561 CLOSE TO G787

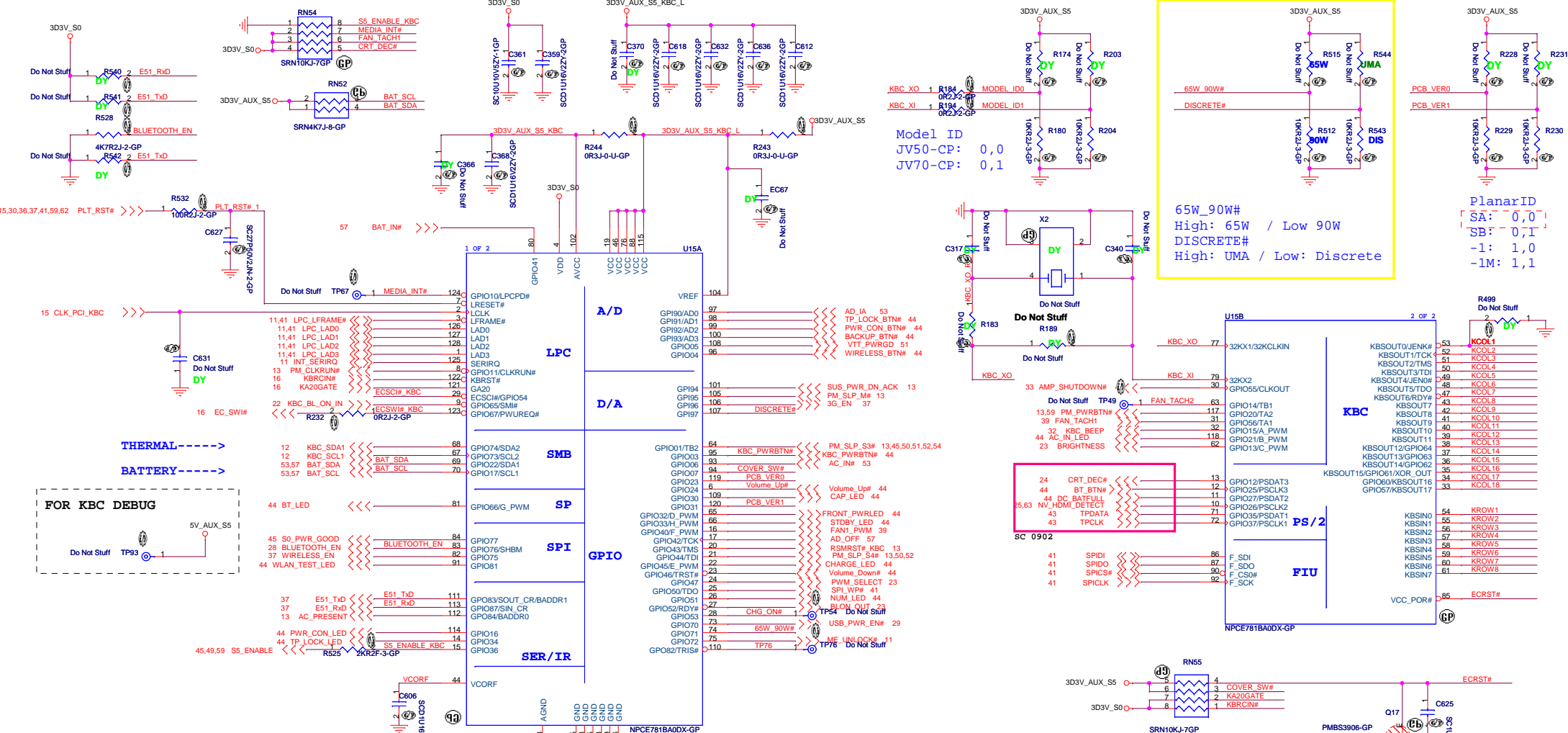
for system thermal diode

84.03904.L06  
2nd = 84.03904.P11

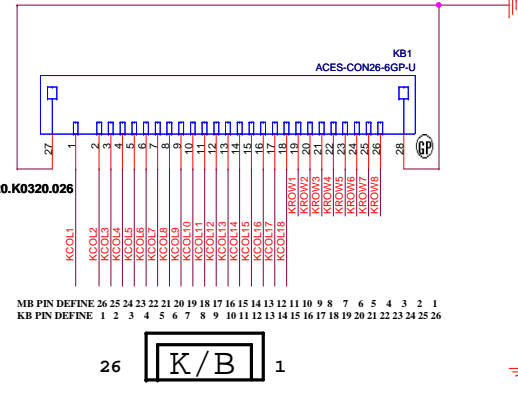


ENG DIS MADISON SAMSUNG

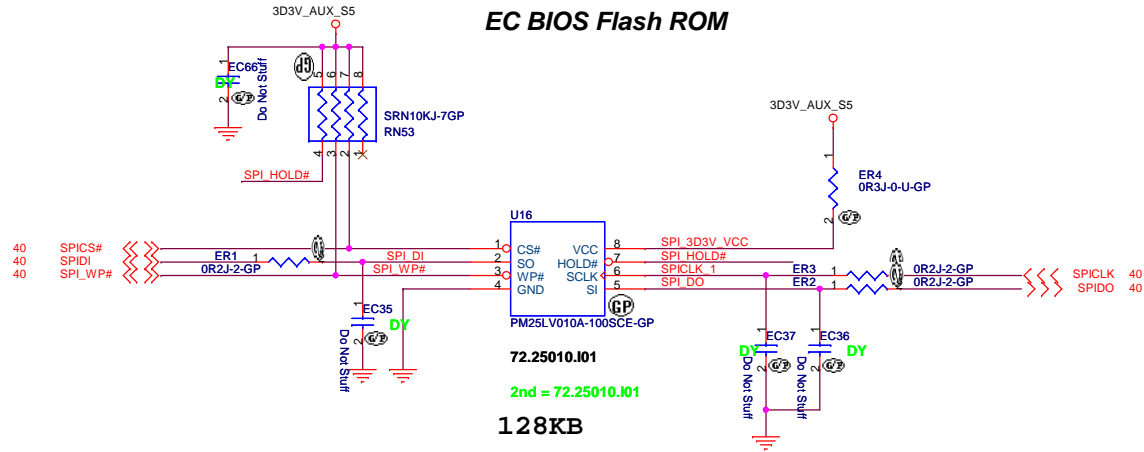
 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Thermal/Fan Connector</b>	
Size	Document Number
<b>JV50-CP</b>	
Date: Thursday, September 03, 2009	Rev SA



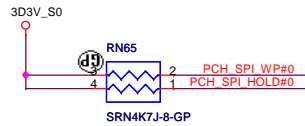
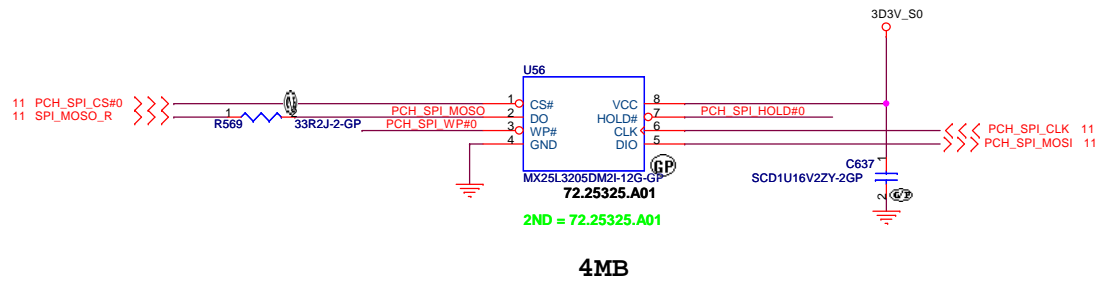
**Internal Keyboard Connector**



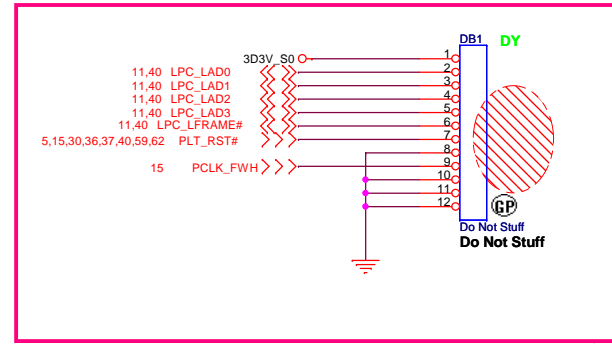
### EC BIOS Flash ROM



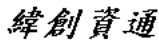
### System BIOS Flash ROM



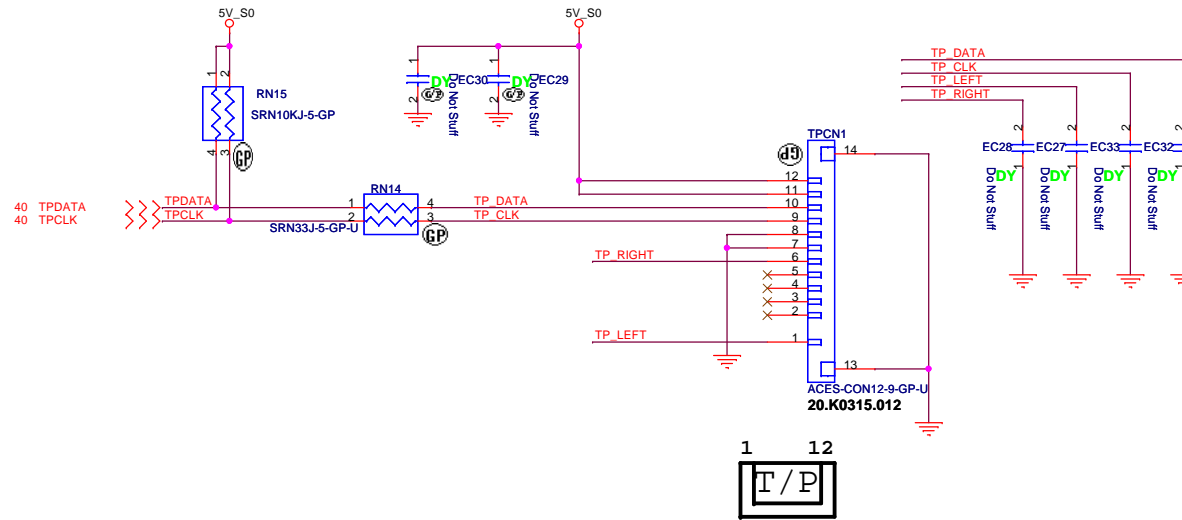
### GOLDEN FINGER FOR DEBUG BOARD



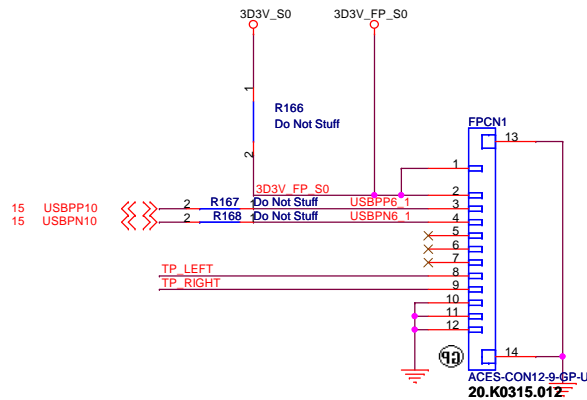
ENG DIS MADISON SAMSUNG

 <b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: <b>BIOS</b>	
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# TOUCH PAD



# Finger printer



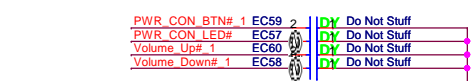
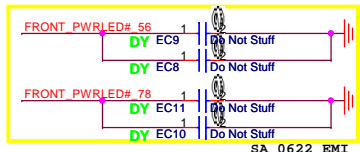
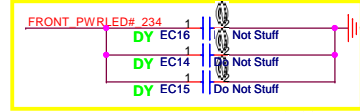
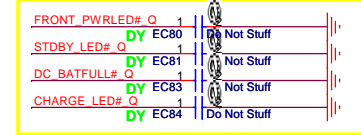
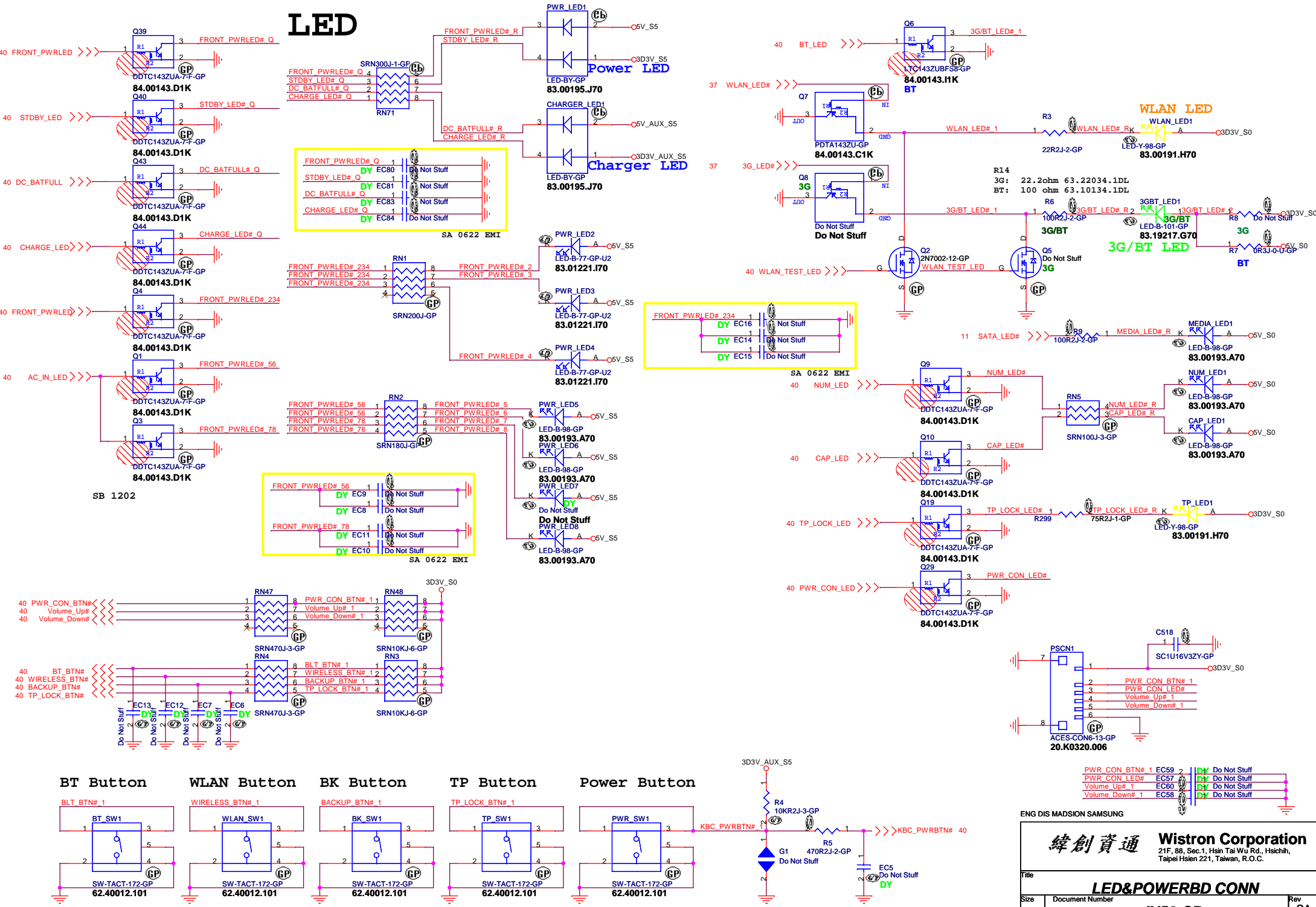
ENG DIS MADSION SAMSUNG

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Touch PAD and FP		
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# LED



ENG DIS MADISON SAMSUNG

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LED&POWERBD CONN**

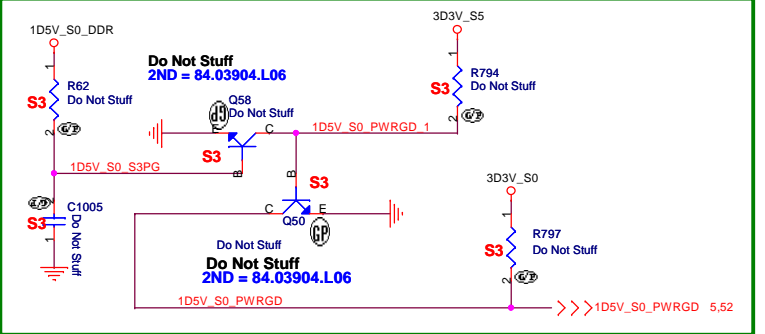
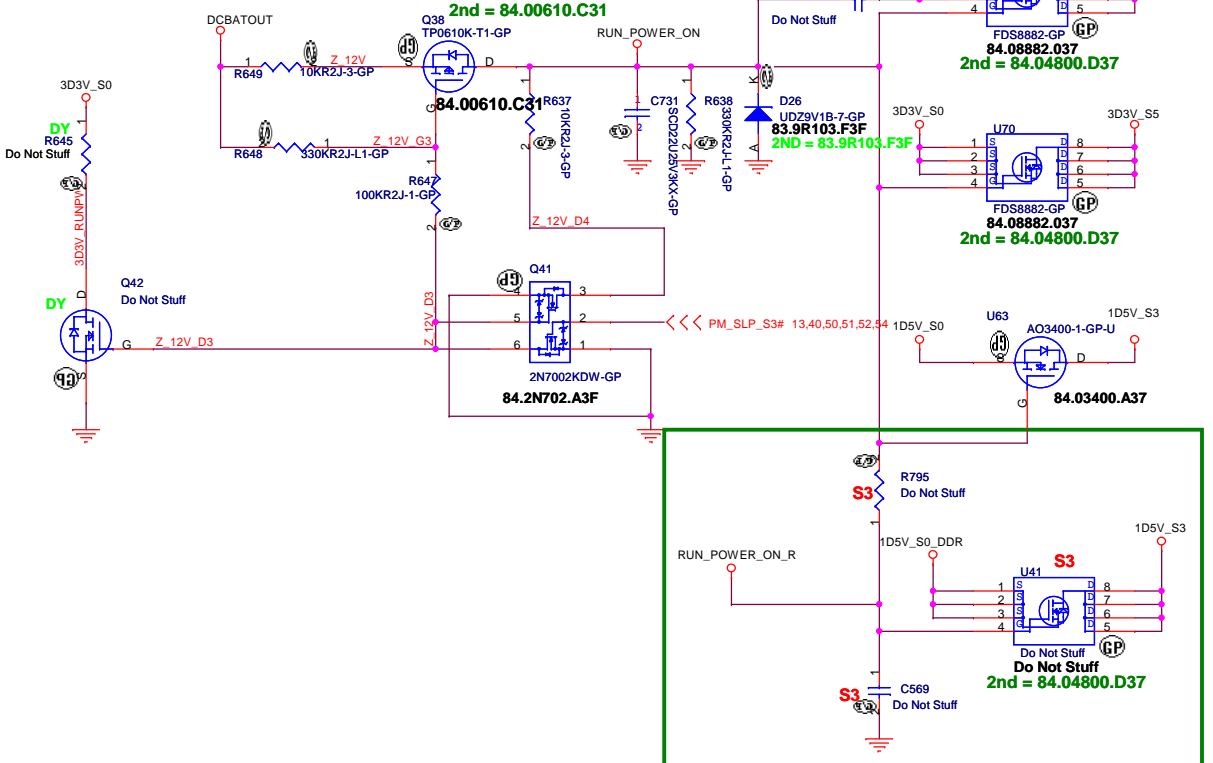
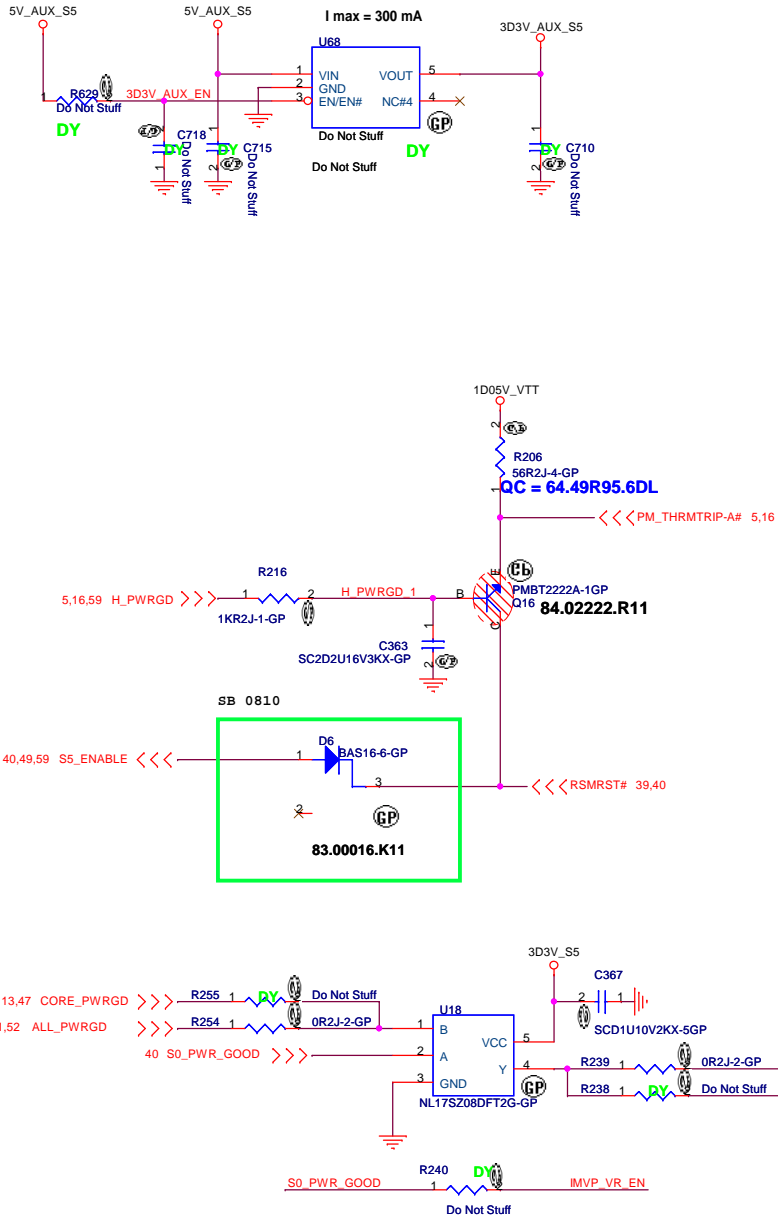
Size: Document Number: **JV50-CP** Rev: SA

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# Run Power

## Aux Power

3D3V\_AUX\_S5



ENG DIS MADISON SAMSUNG

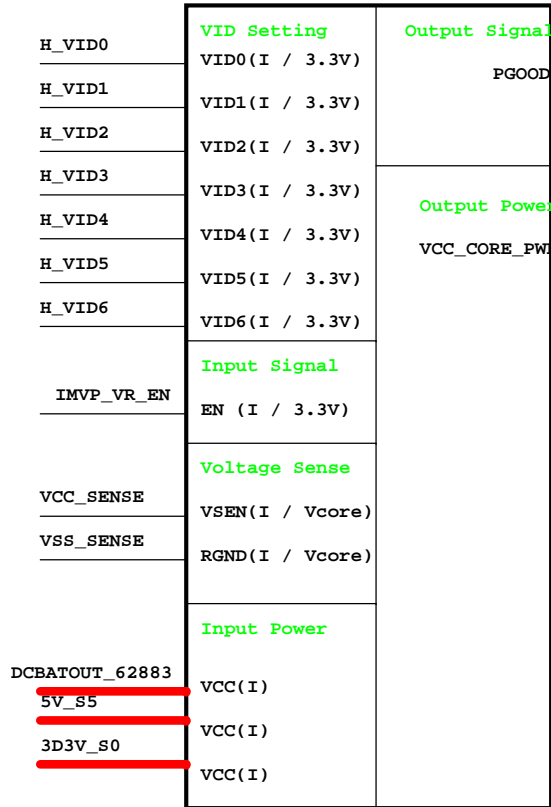
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN POWER and 3D3V AUX S5**

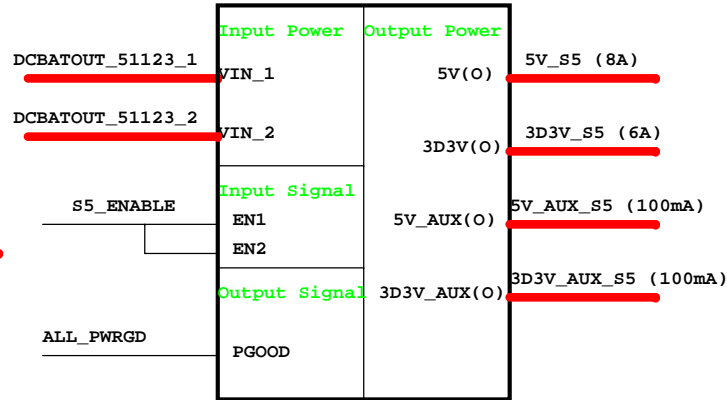
Size	Document Number	Rev
	<b>JV50-CP</b>	SA

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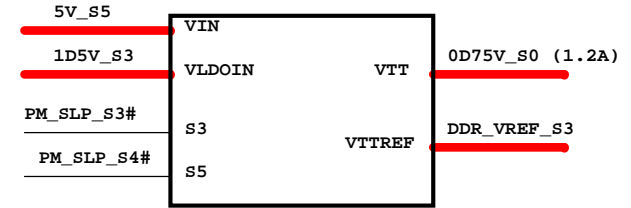
**ISL62883 VCC\_CORE**



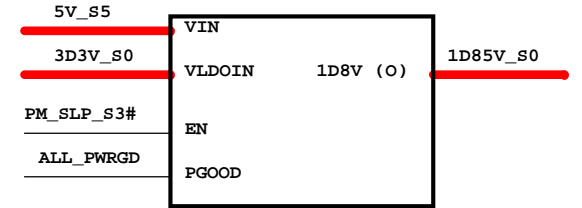
**TPS51123 5V/3D3V**



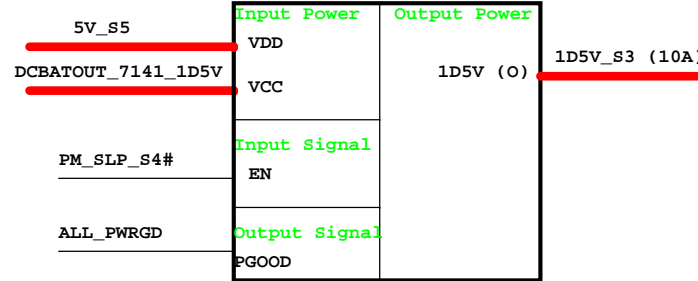
**RT9026 0D75V\_S0**



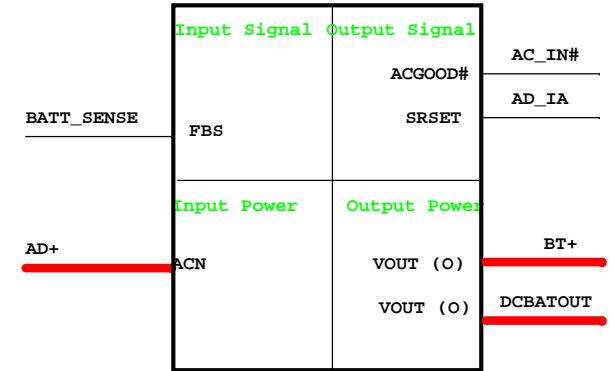
**RT9025 1D8V**



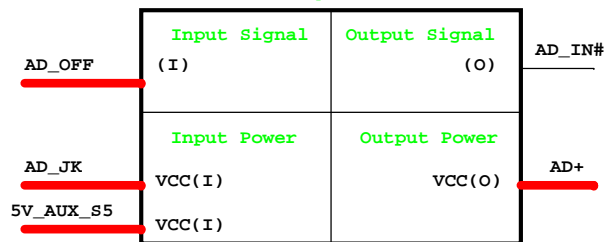
**RT9025 1D5V**



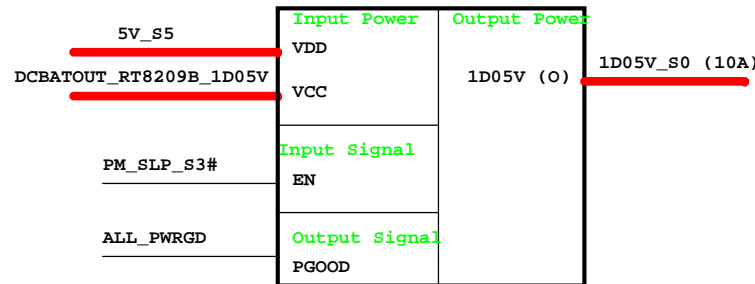
**Charger BQ24745**



**Adapter**



**RT8209B 1D05V**

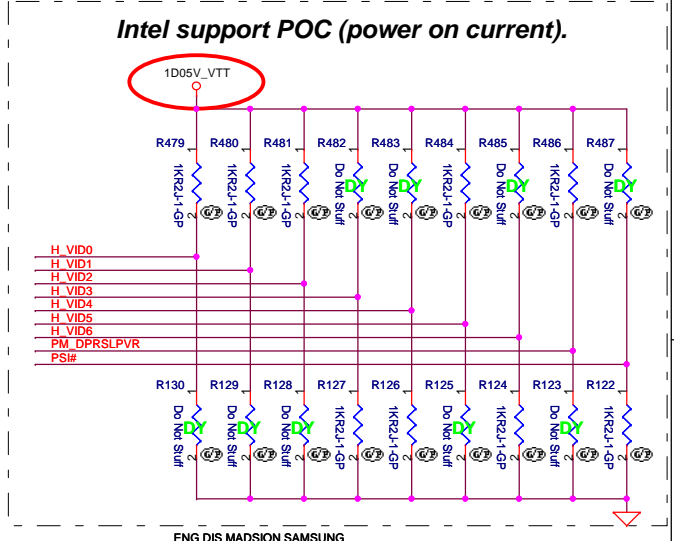
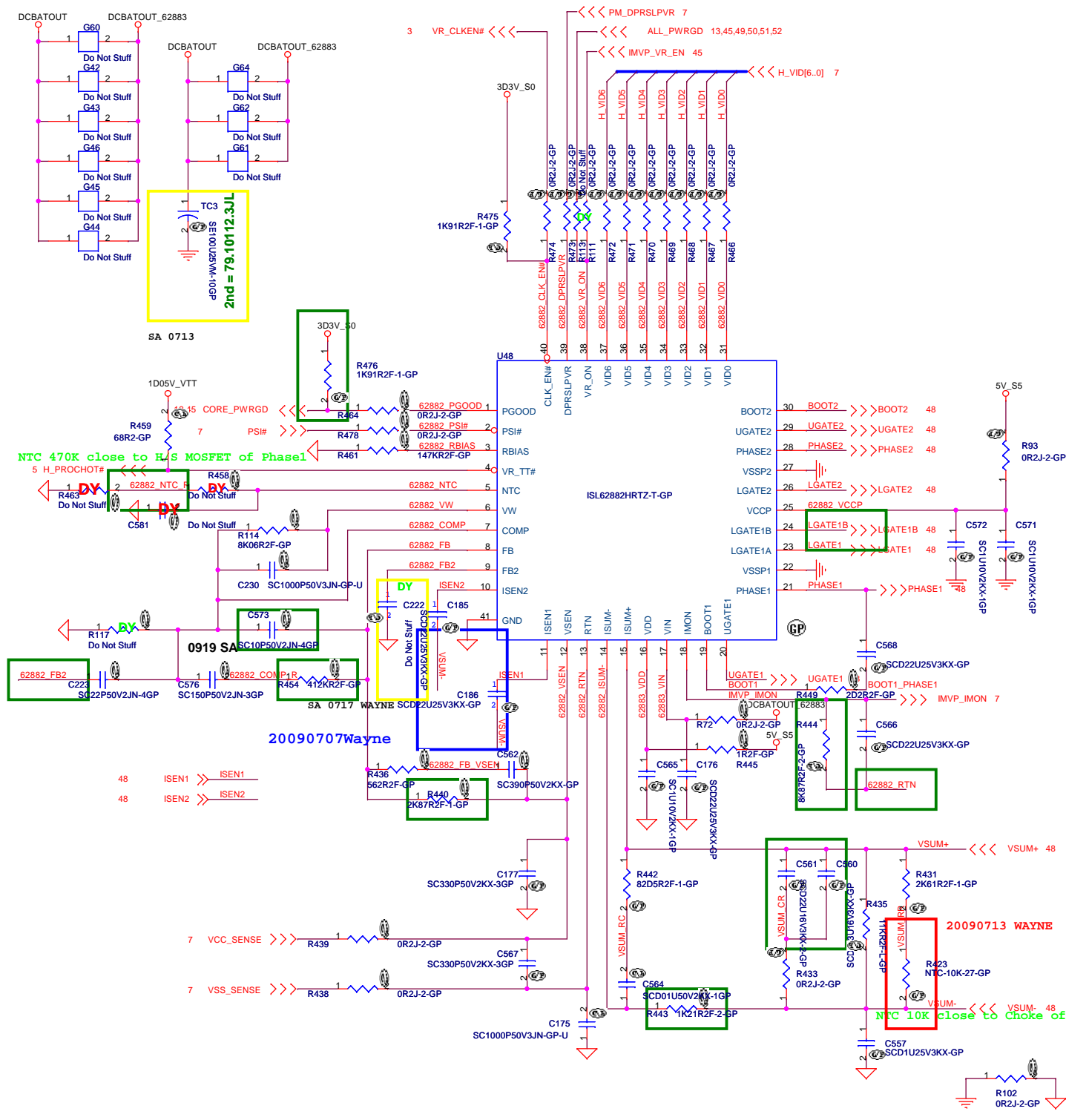


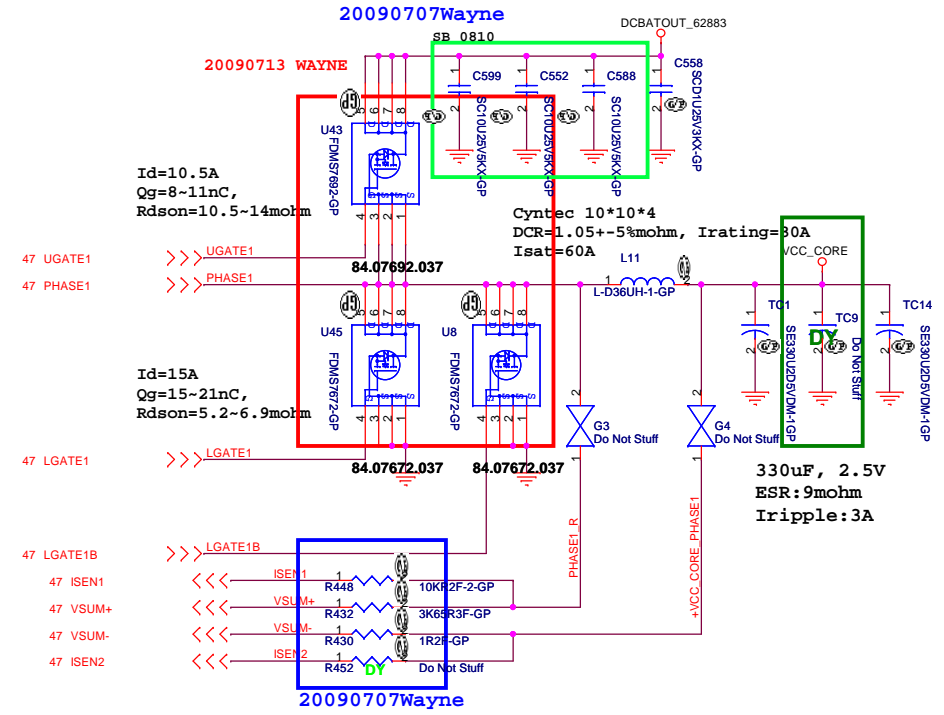
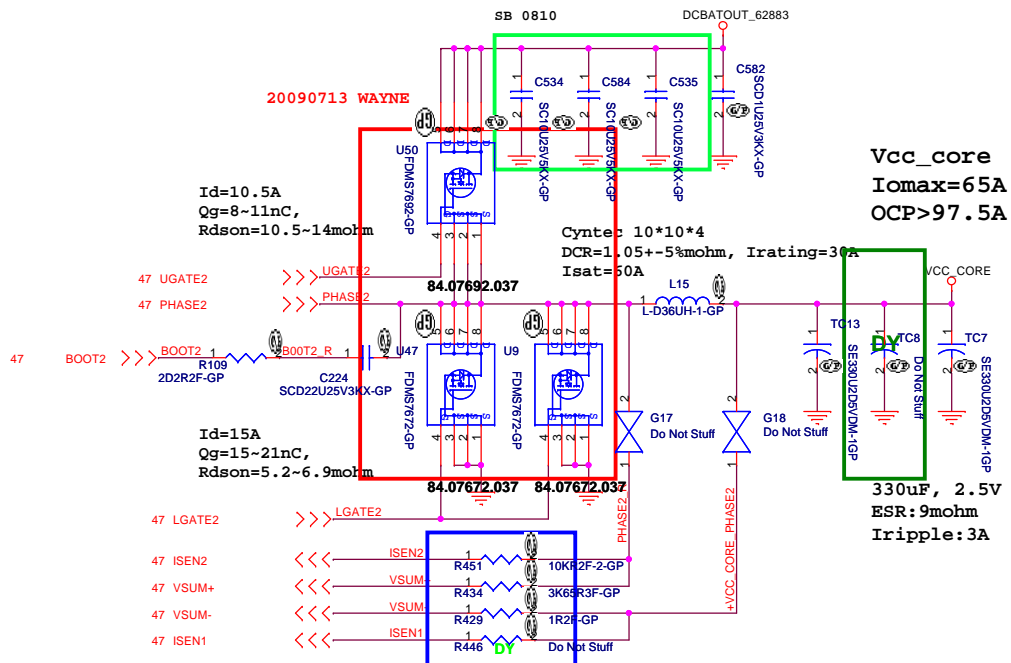
ENG DIS MADISON SAMSUNG

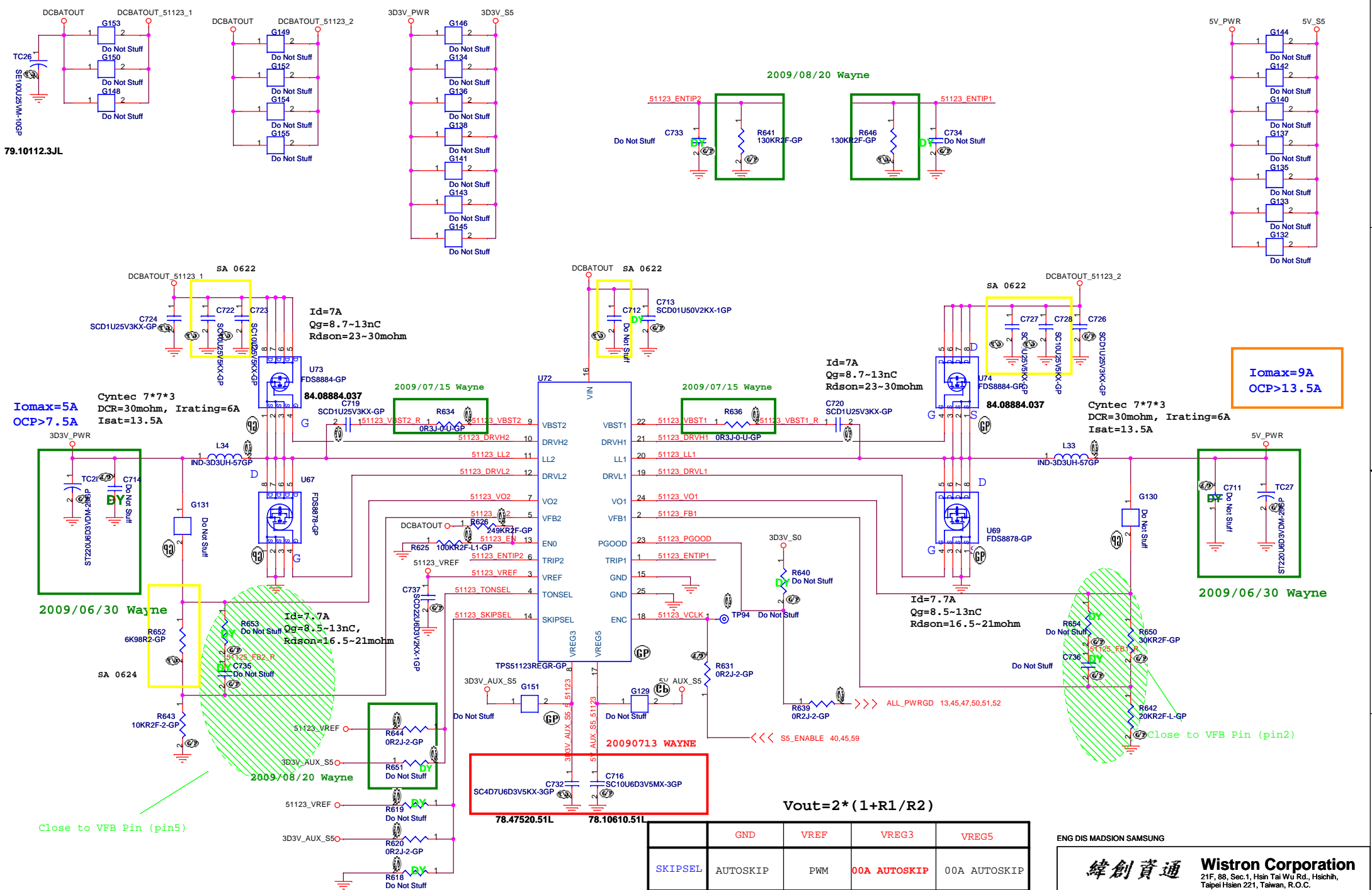
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai WJ Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title			Rev
<b>Power Block Diagram</b>			
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79.10112.3JL

2009/08/20 Wayne

Iomax=9A  
OCP>13.5A

2009/06/30 Wayne

2009/06/30 Wayne

2009/07/15 Wayne

2009/07/15 Wayne

2009/08/20 Wayne

20090713 WAYNE

$$V_{out} = 2 * (1 + R1/R2)$$

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

ENG DIS MADSION SAMSUNG

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

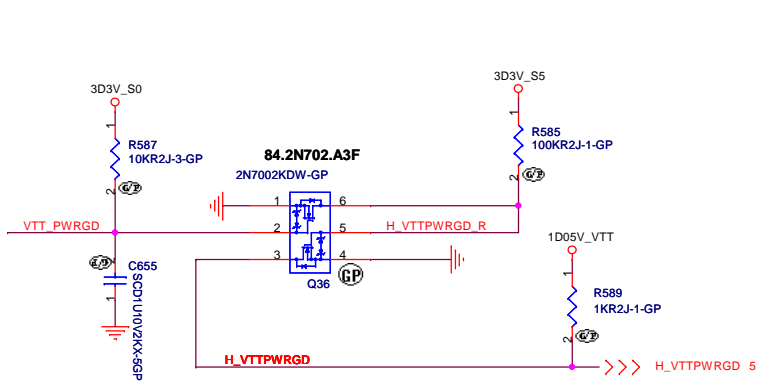
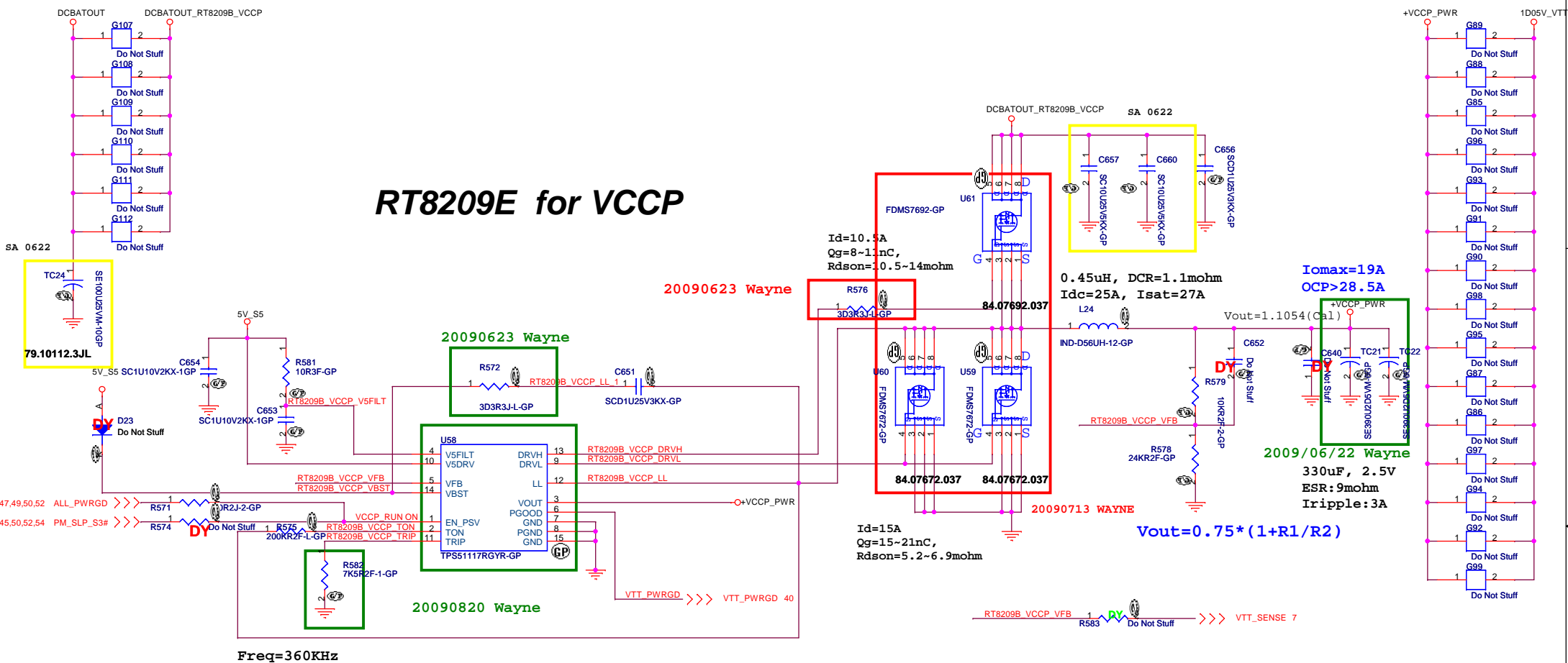
Title: **TPS51123 5V/3D3V**

Size: Document Number **JV50-CP** Rev: SA

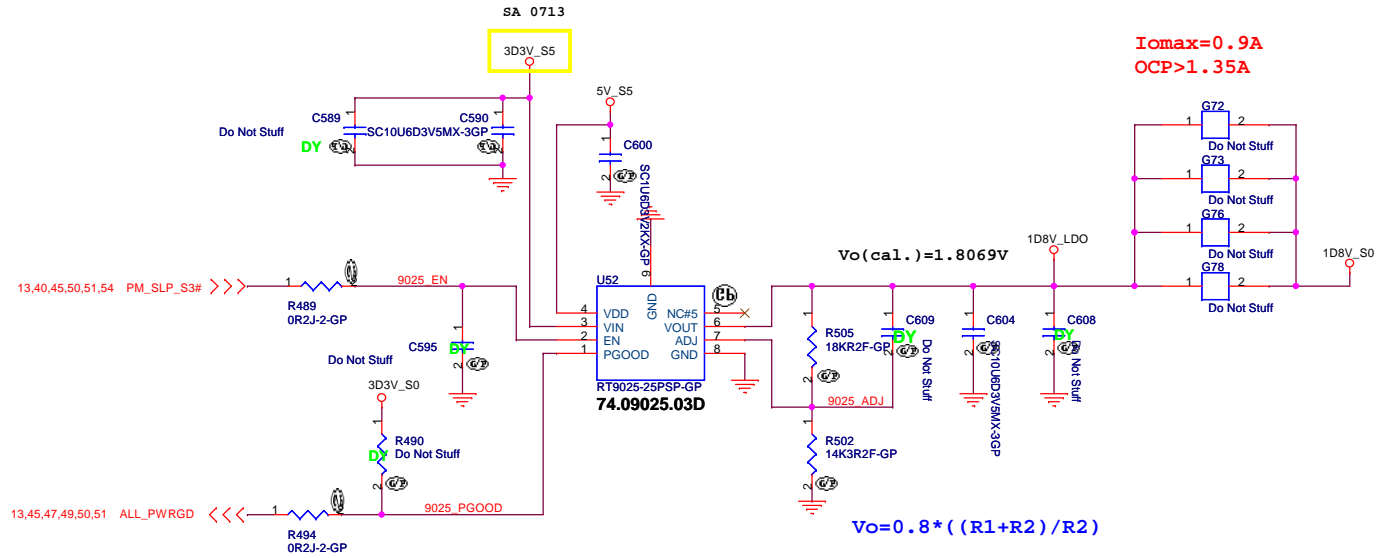
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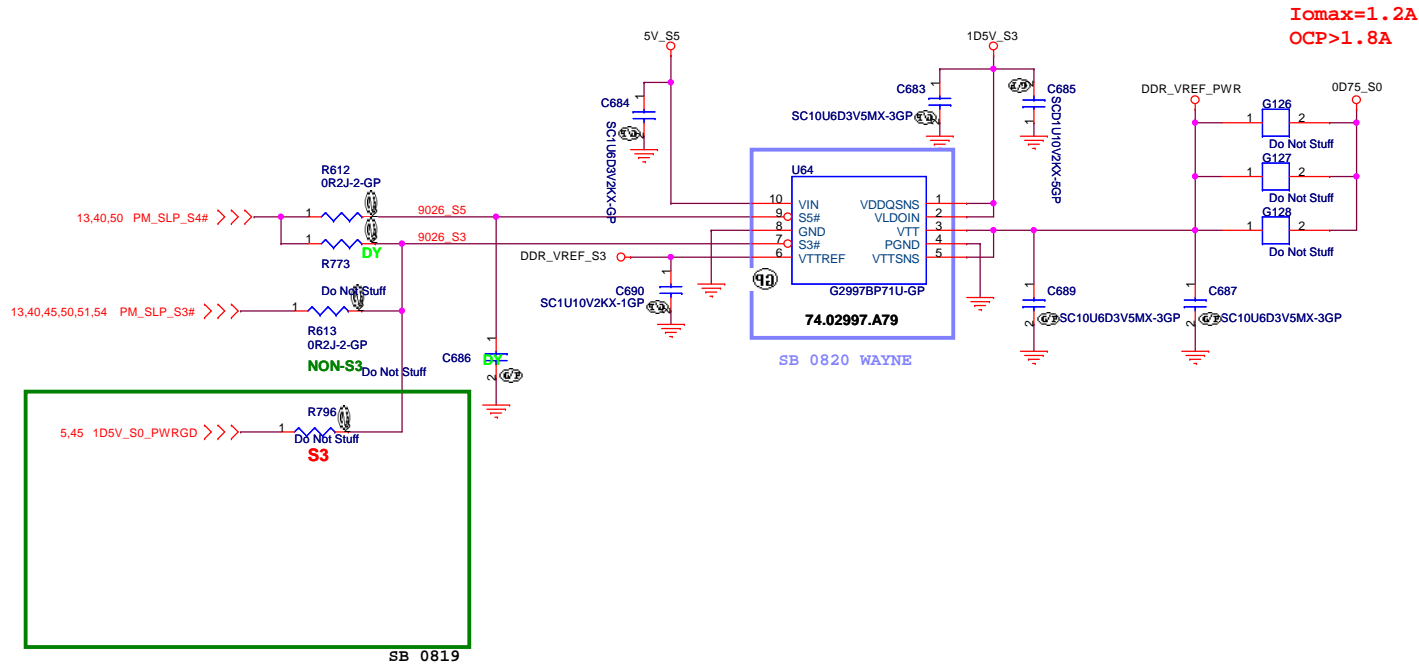
# RT8209E for VCCP



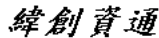
### RT9025 for 1D8V\_S0



### RT9026 for 0D75V\_S3

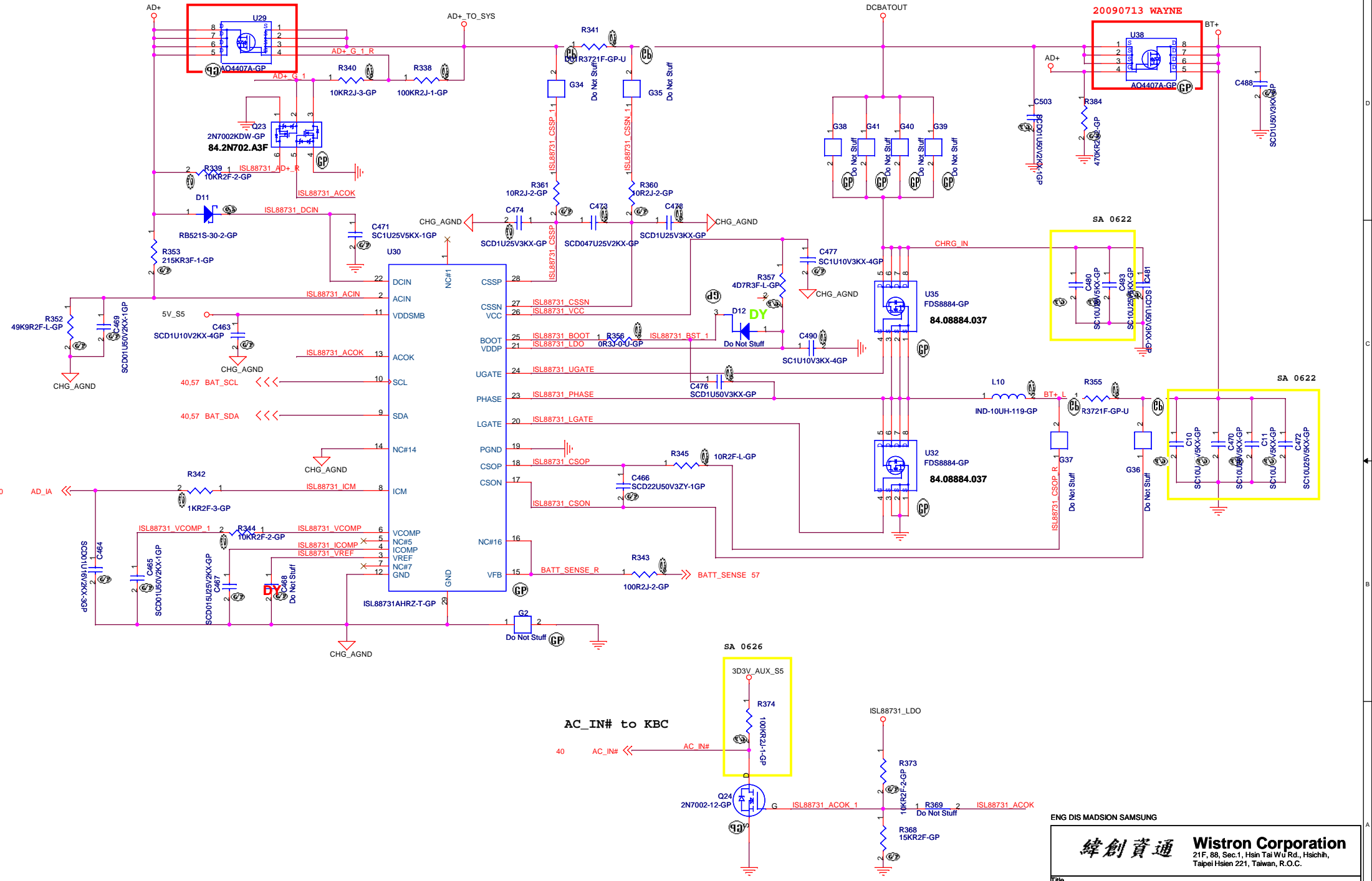


ENG DIS MADISON SAMSUNG

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>RT9025 1D8V/RT9026 0D75</b>	
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20090713 WAYNE

20090713 WAYNE



AC\_IN# to KBC

AC\_IN#

ENG DIS MADISON SAMSUNG

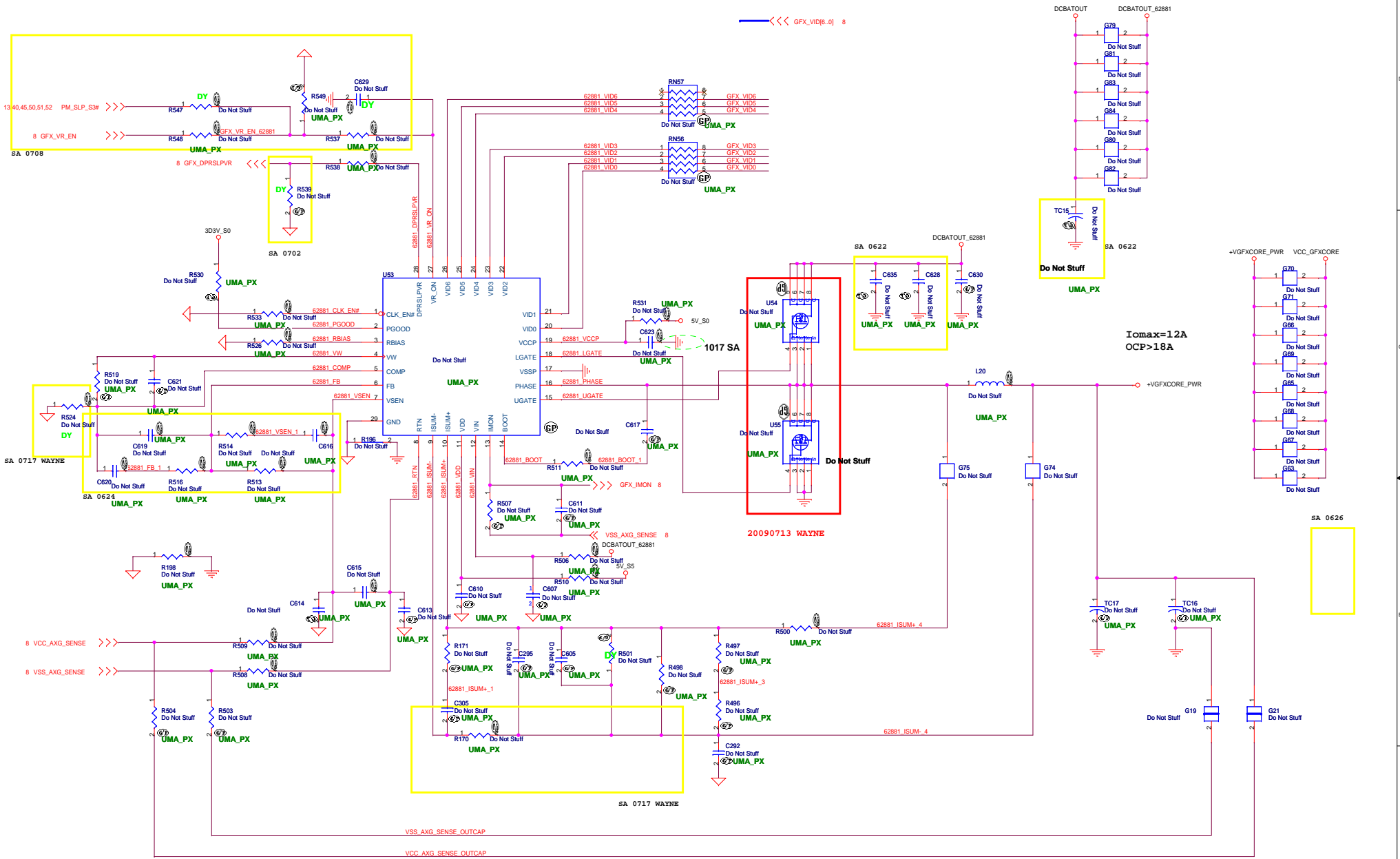
**緯創資通** **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL88731A CHARGER**

Size: Document Number

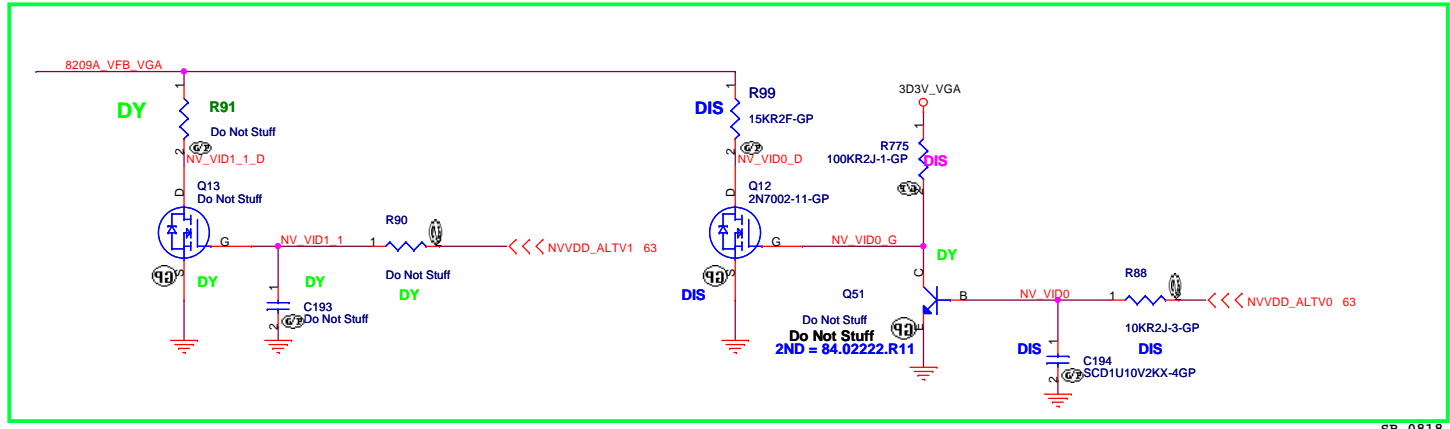
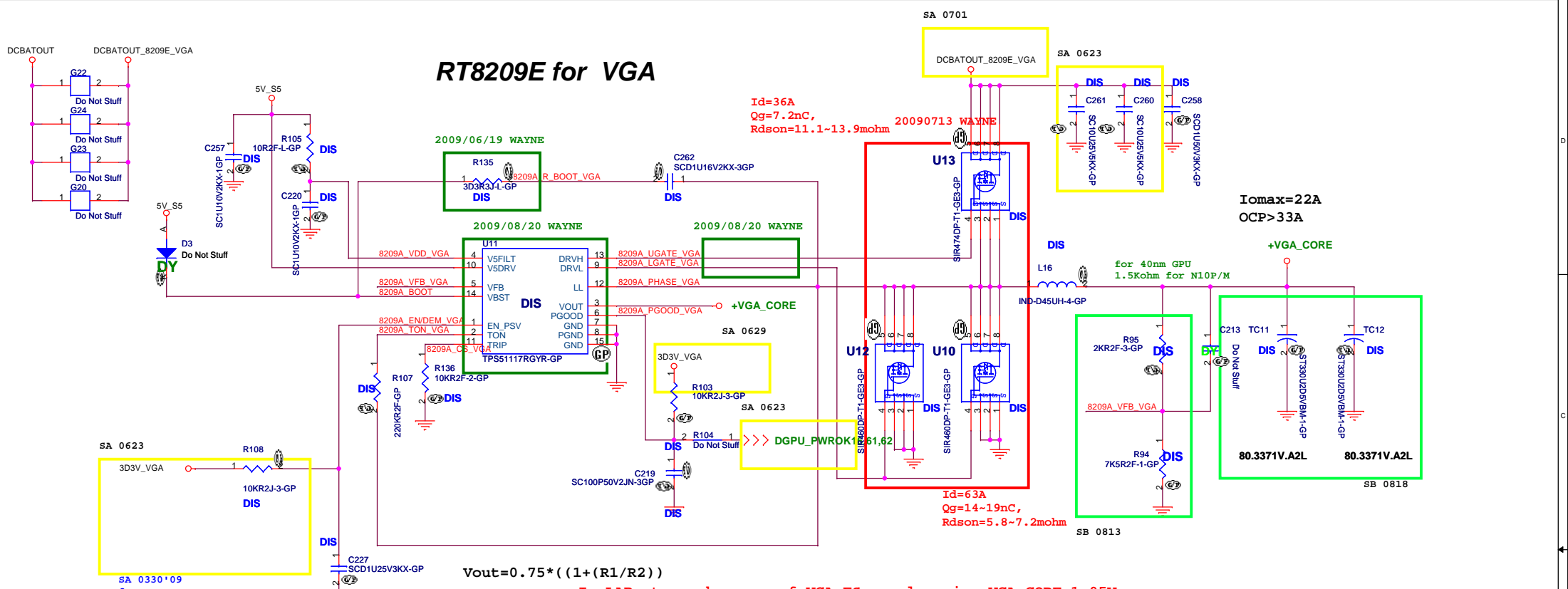
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# RT8209E for VGA



	I/O	Inter Pull Low	GPIO TABLE
NVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.05V GPU VOLTAGE H: 0.95V

ENG DIS MADSION SAMSUNG

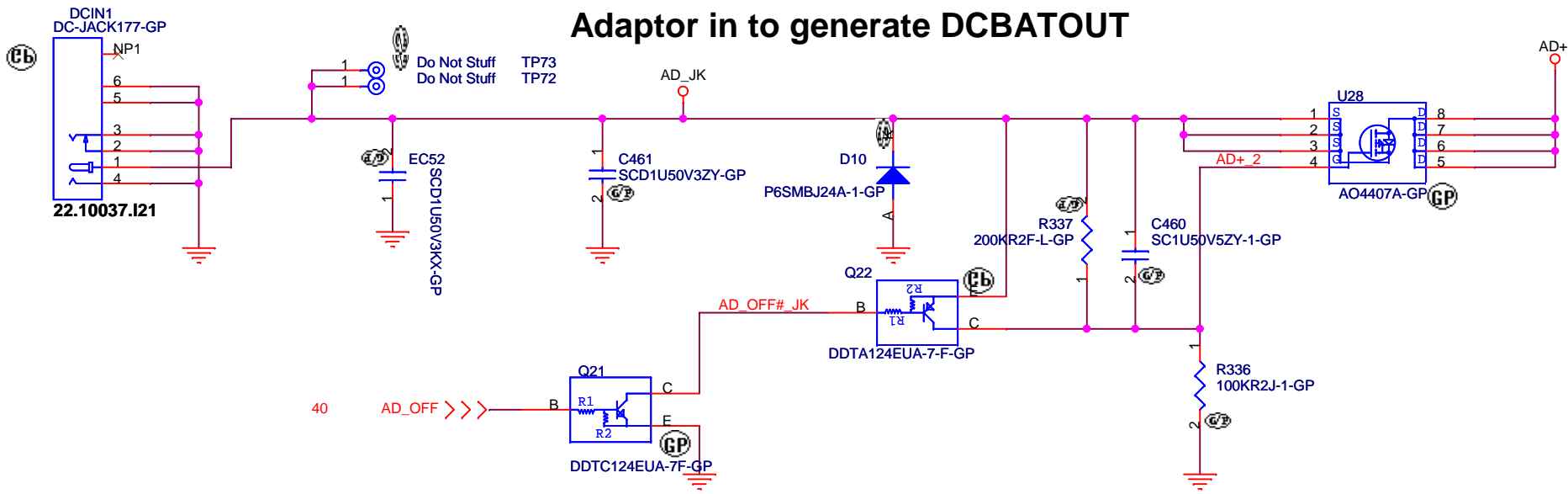
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8209E VGA CORE**

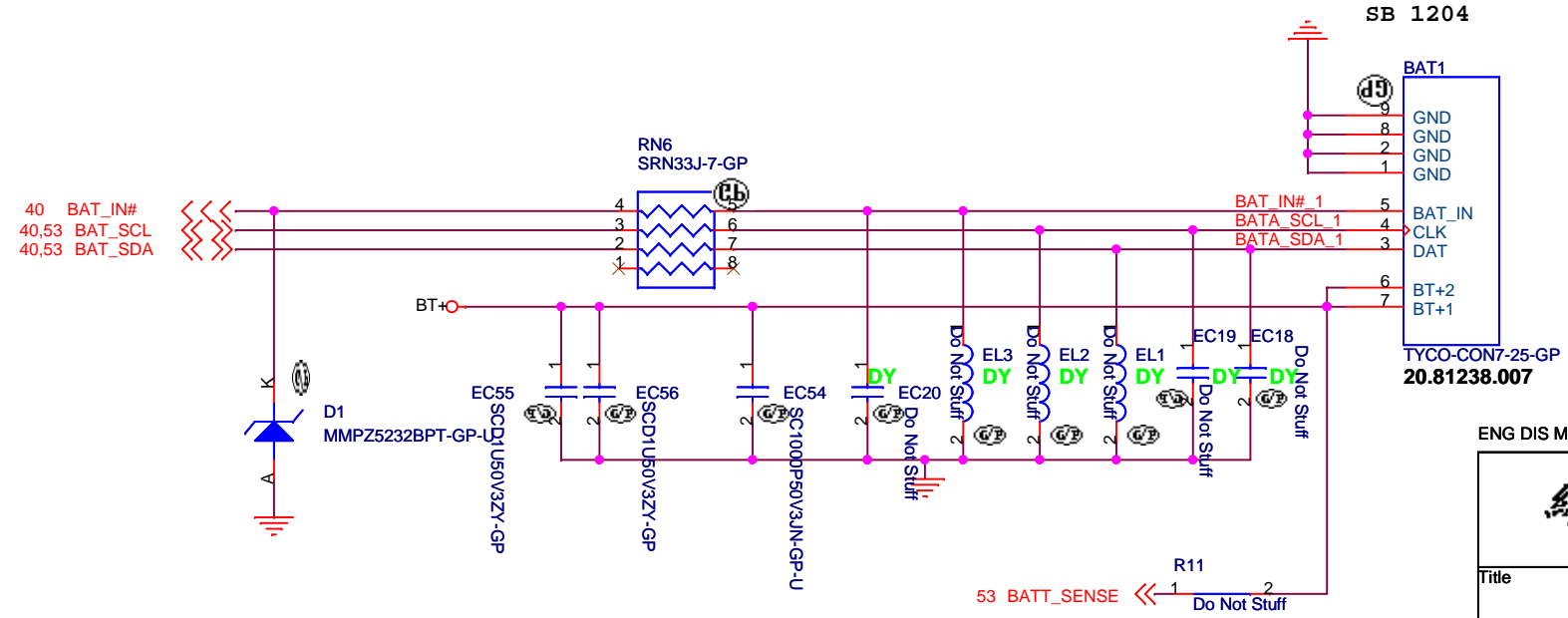
Size A3 Document Number: **JV50-CP** Rev: \_\_\_\_\_

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# Adaptor in to generate DCBATOUT



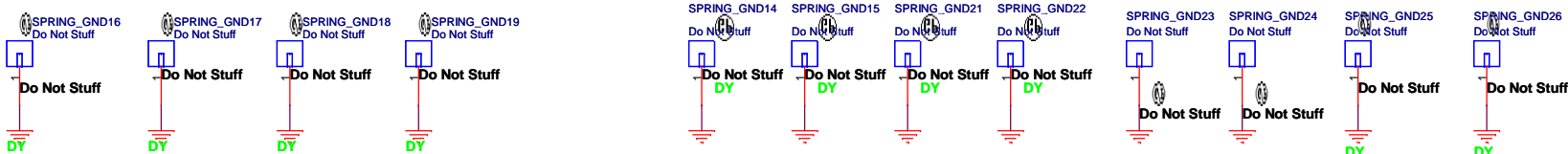
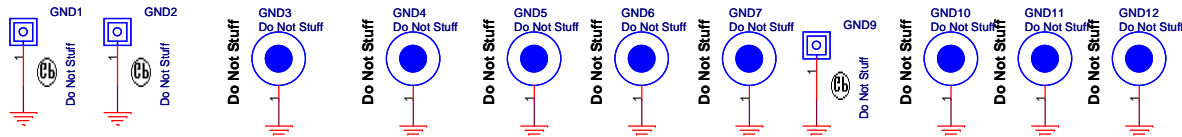
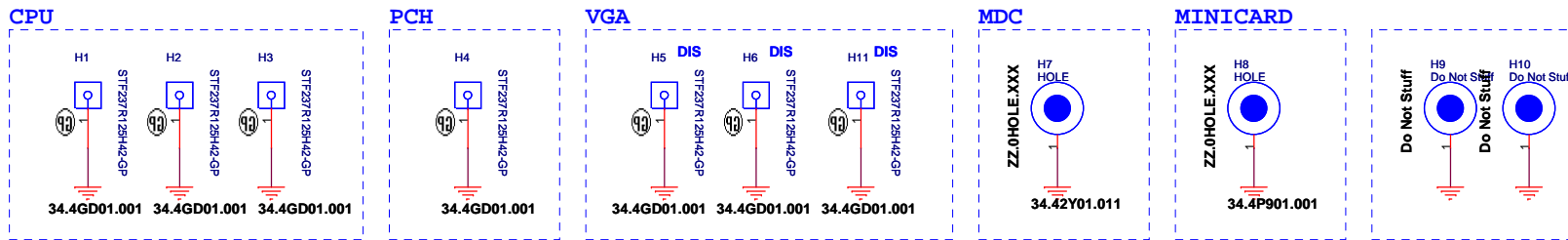
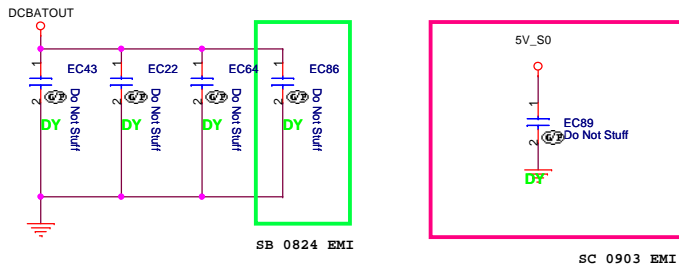
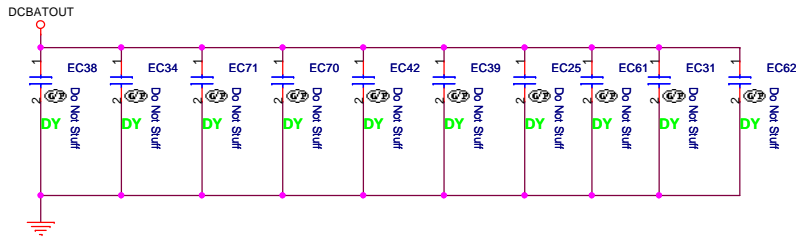
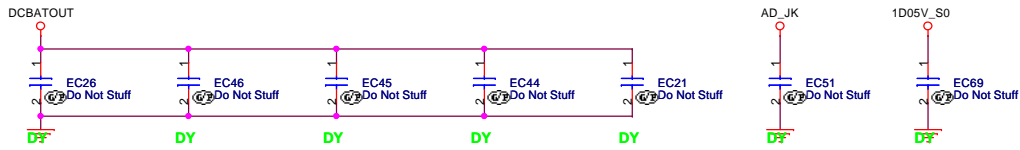
# BATTERY CONNECTOR



ENG DIS MADSION SAMSUNG

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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Title			
<b>AD/BATT CONN</b>			
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ENG DIS MADSION SAMSUNG

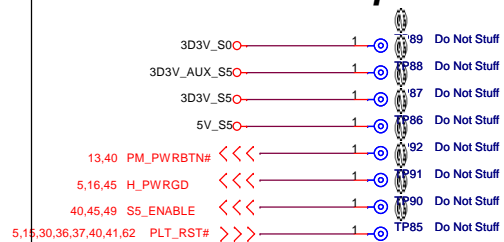
緯創資通 Wistron Corporation  
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Title: **EMI/Spring/Boss**

Size: Document Number: **JV50-CP** Rev: SA

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## Check test point



Test Point放在Dimm Door打開可量測處

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**AFTE TP**

Size

Document Number

**JV50-CP**

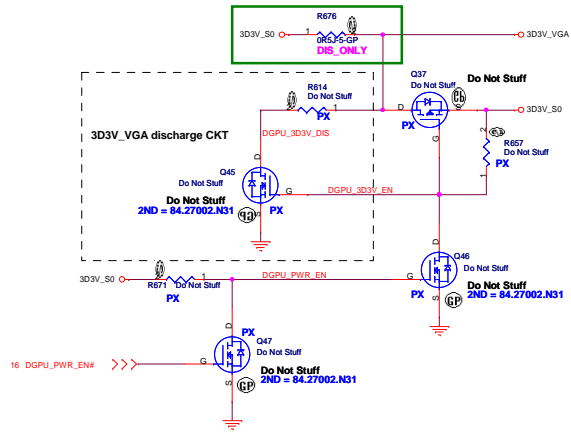
Rev

**SA**

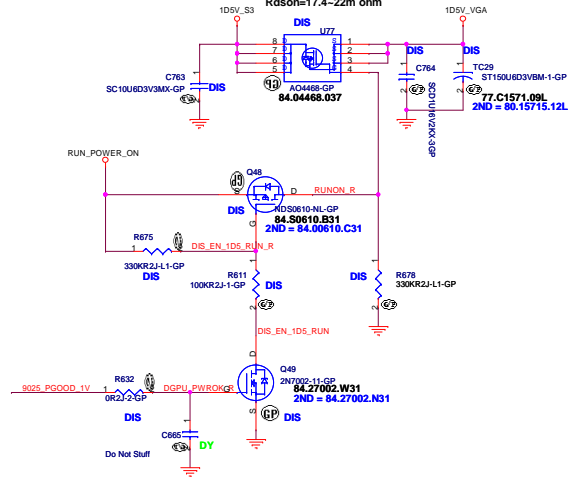
Date: Thursday, September 03, 2009

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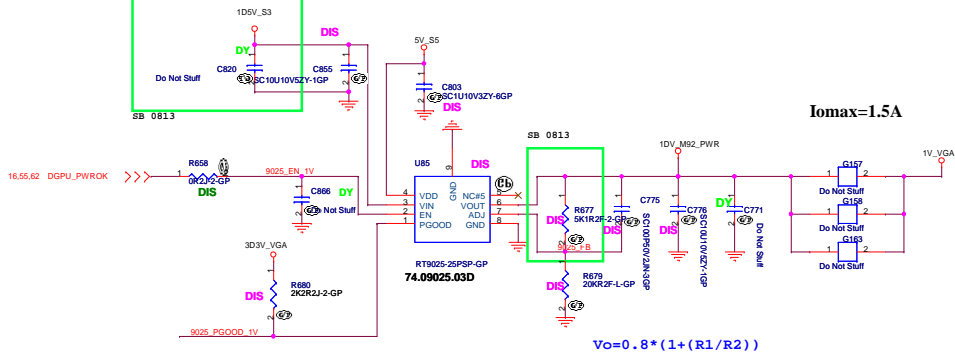
### +3VS to 3.3V\_DELAY Transfer



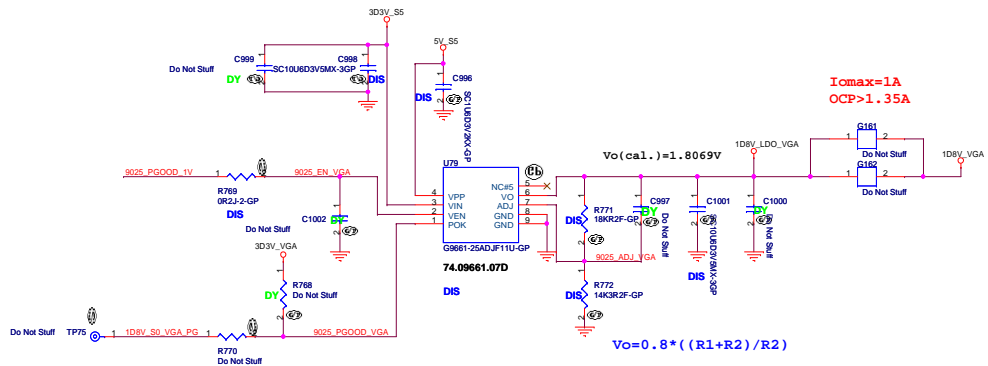
### AO4468, SO-8 Id=11.6A, Qg=9-12nC Rdson=17.4-22m ohm



### RT9025 for 1V\_VGA

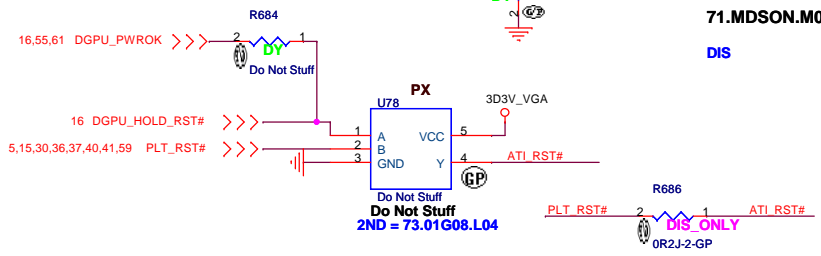
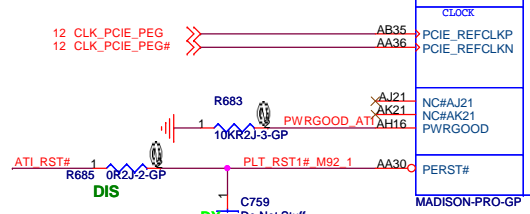
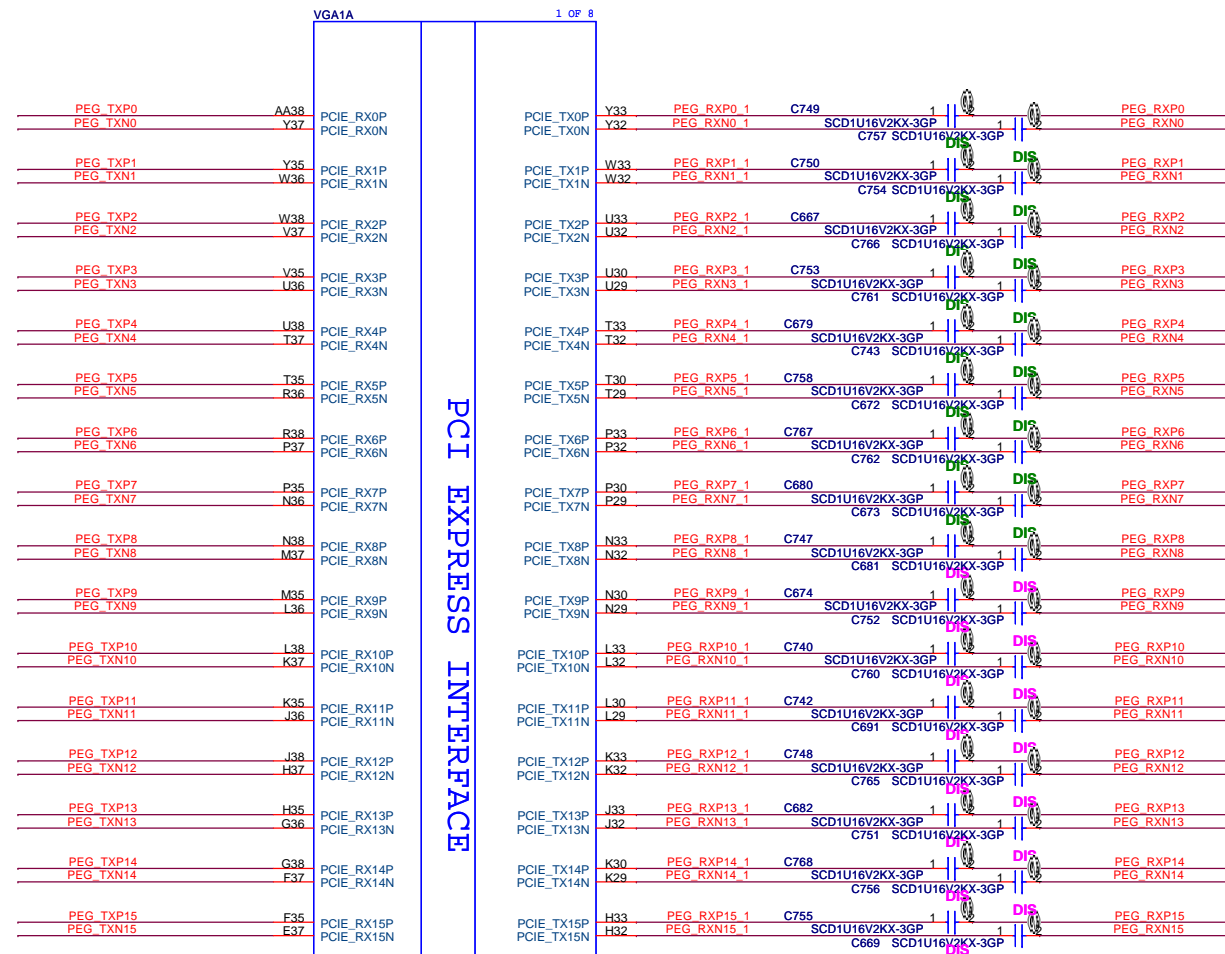


### G9661 for 1D8V\_VGA



4 PEG\_TXP[15..0] <<< PEG\_TXP[15..0]  
 4 PEG\_TXN[15..0] <<< PEG\_TXN[15..0]

4 PEG\_RXP[15..0] <<< PEG\_RXP[15..0]  
 4 PEG\_RXN[15..0] <<< PEG\_RXN[15..0]



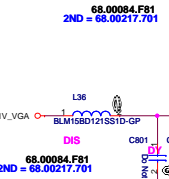
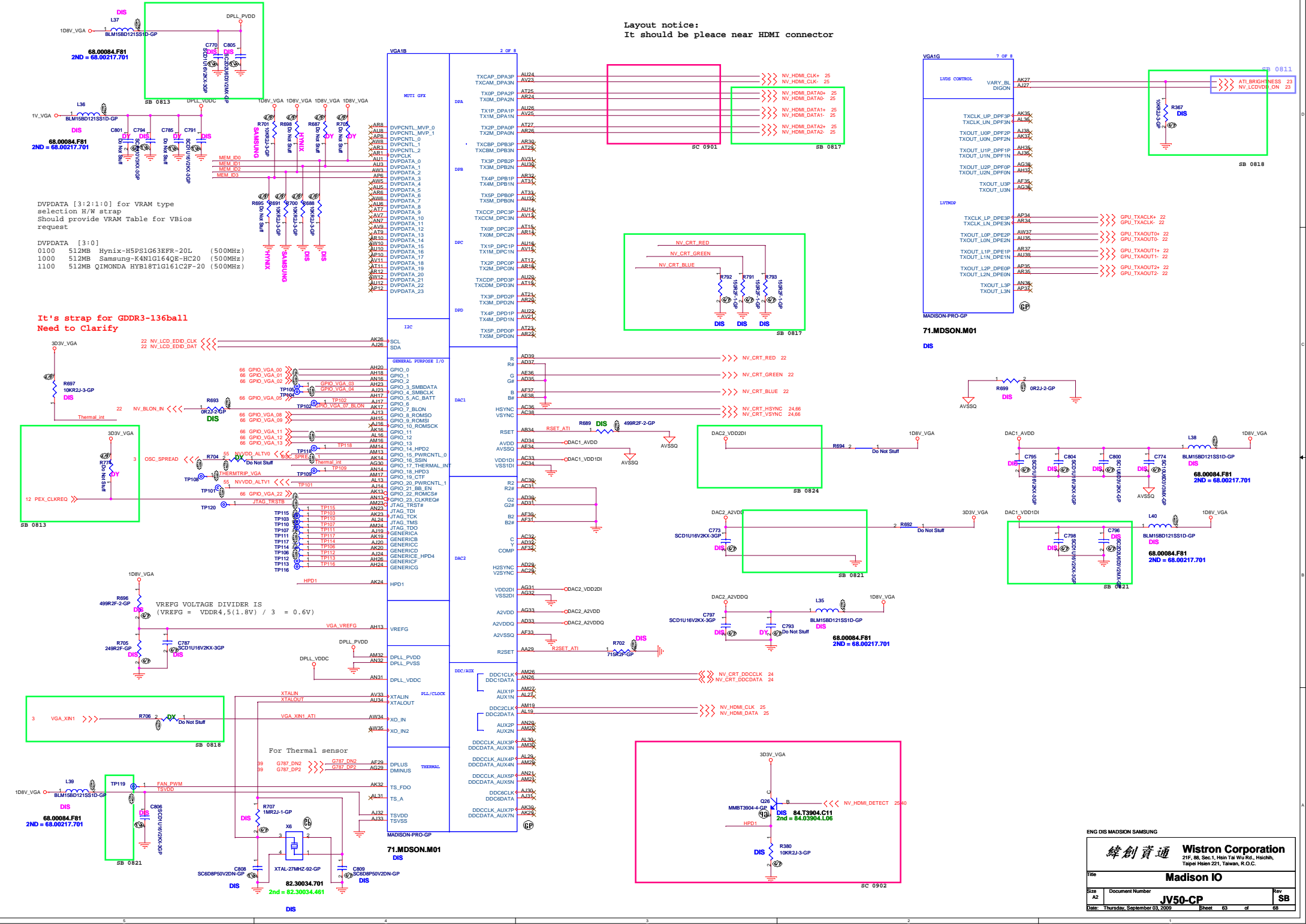
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File: **Madison PCIE**

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Layout note:  
It should be please near HDMI connector

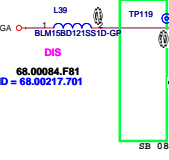
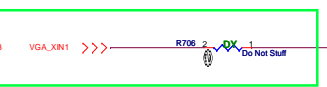
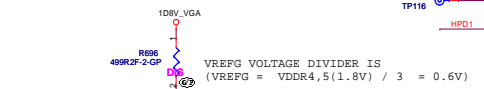
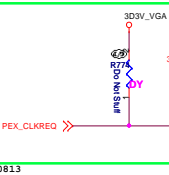


DVPDATA [3:2:1:0] for VRAM type selection H/W strap  
Should provide VRAM Table for Vbios request

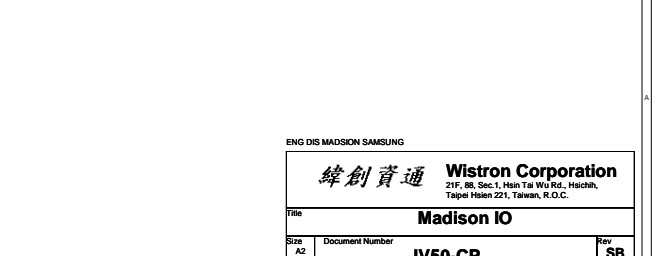
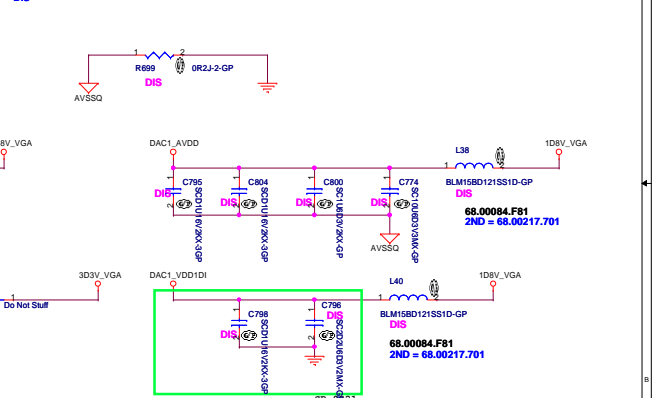
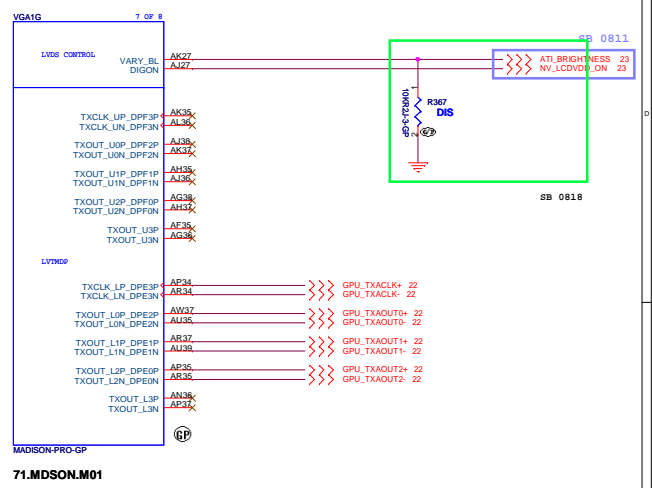
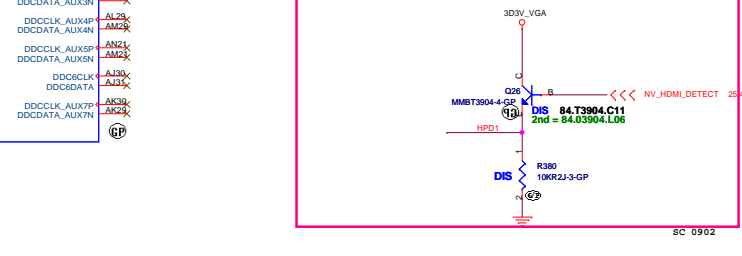
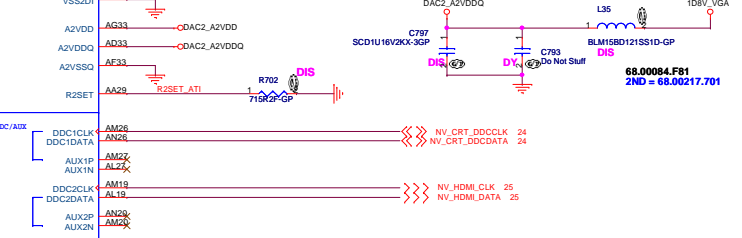
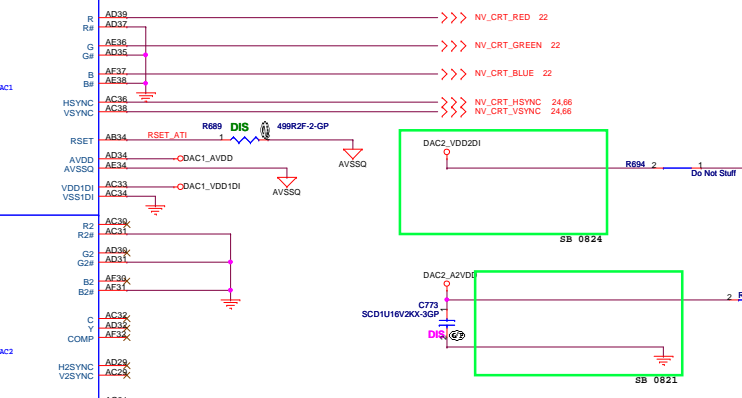
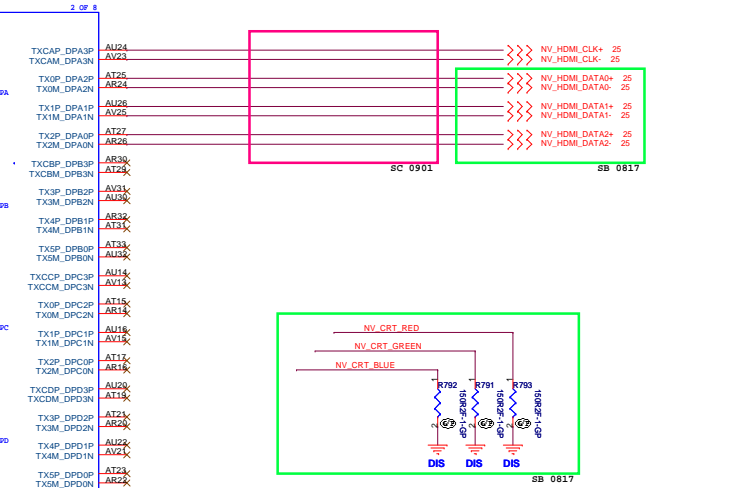
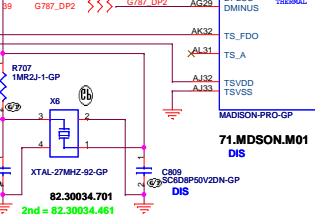
DVPDATA [3:0]

0100	512MB	Hynix-H5PS1G63EPR-20L	(500MHz)
1000	512MB	Samsung-K4N1G164QE-HC20	(500MHz)
1100	512MB	QIMONDA-HY818T1G161C2P-20	(500MHz)

It's strap for GDDR3-136ball  
Need to Clarify

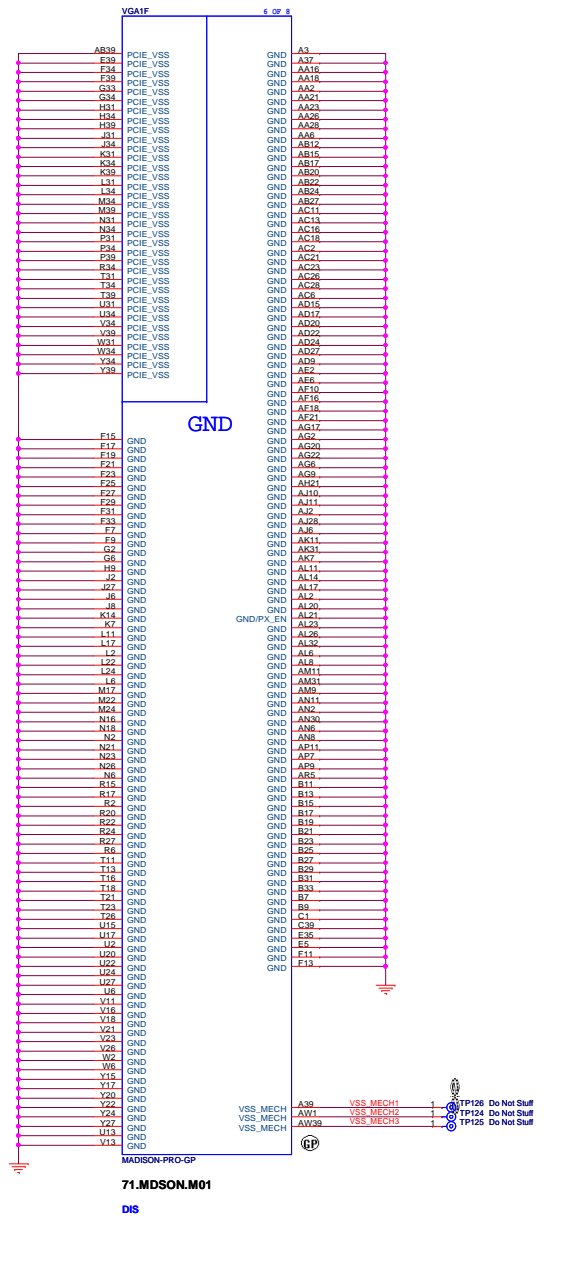
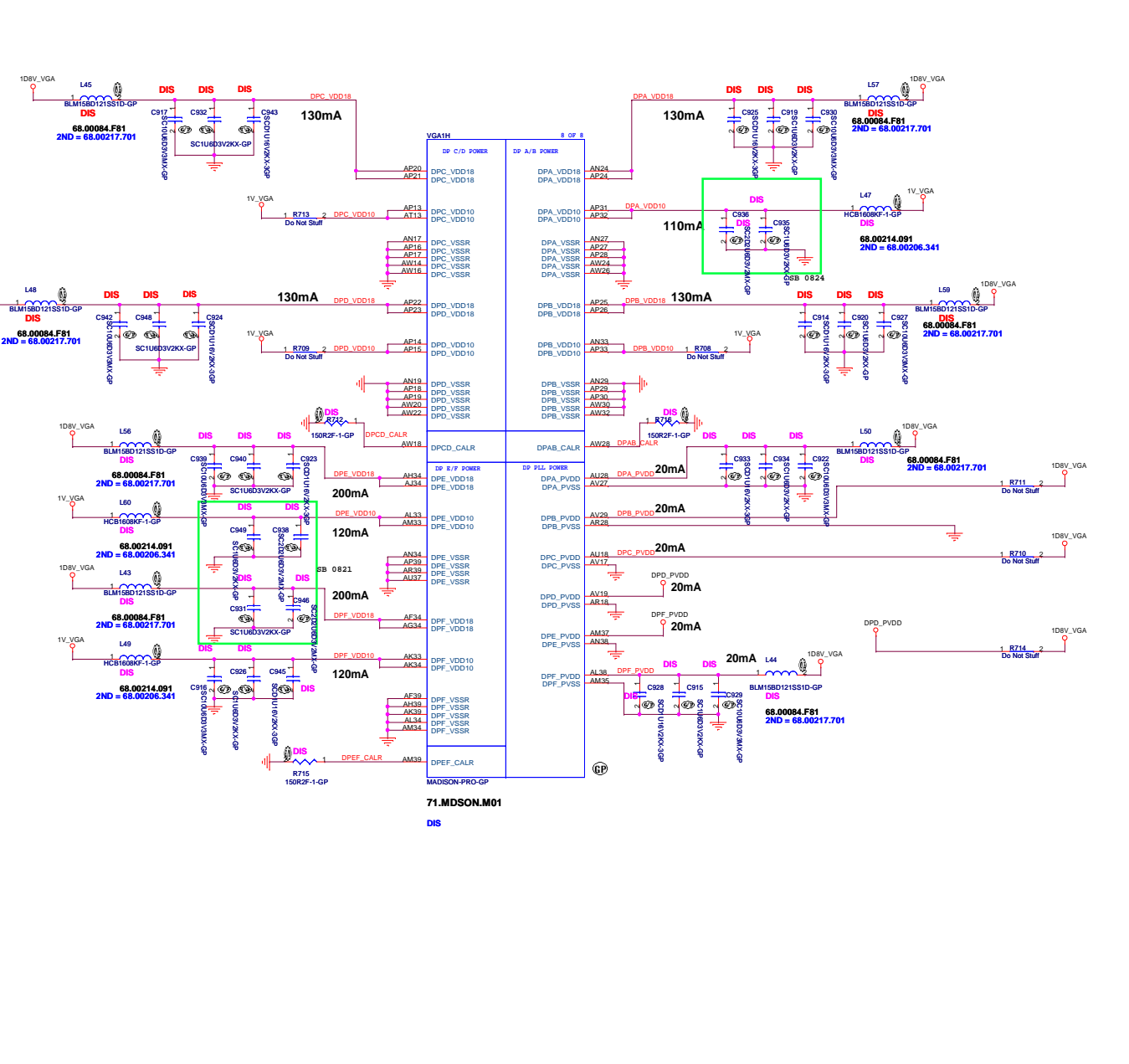


For Thermal sensor



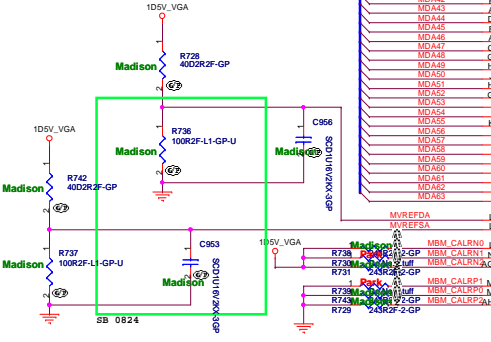






For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 \* VDDRL1.  
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 \* VDDRL1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R



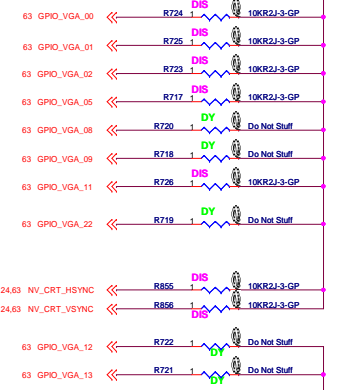
Madison: MEM\_CALRP[0,2] signals are used.  
Park: MEM\_CALRP1 and MEM\_CALRN1 are used

71.MDSOM.01

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS
TX_PWRS_ENB (Internal PD)	GPIO0	PCIe Full Tx Output Swing Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	x
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	x
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size	x x x
RSVD	V2SYNCS		0
RSVD	H2SYNCS		0
AUD[1] (Internal PD)	VGA_HSYNCS	AUD[1:0] 00: No audio function 01: Audio for DisplayPort and HDMI (if adapter is detected) 10: Audio for DisplayPort only 11: Audio for both DisplayPort and HDMI	x x x x

AMD RESERVED CONFIGURATION STRAPS  
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1	
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number
128MB	x000	ST	M25P05A
256MB	x001	ST	M25P10A
64MB	x010	ST	M25P20
32MB	x	ST	M25P40
512MB	x	ST	M25P80
1GB	x	Chingis (formerly PMC)	Pm25LV512A
2GB	x	Chingis (formerly PMC)	Pm25LV010A
4GB	x	Chingis (formerly PMC)	Pm25LV010A



71.MDSOM.01



Designator	For M97-M2	For Mannheim
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

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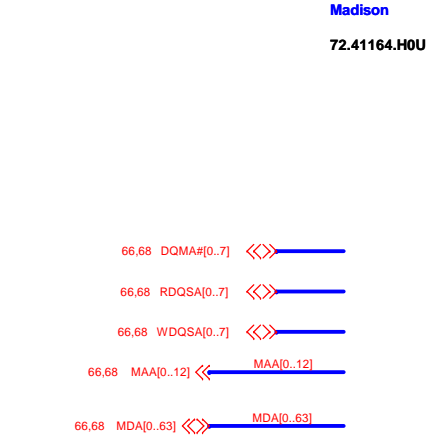
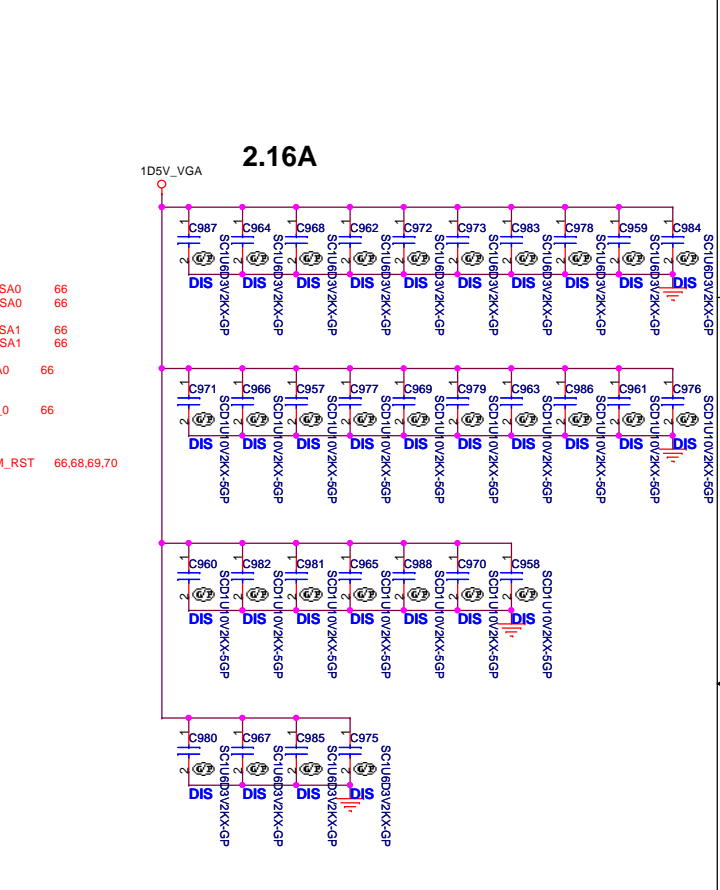
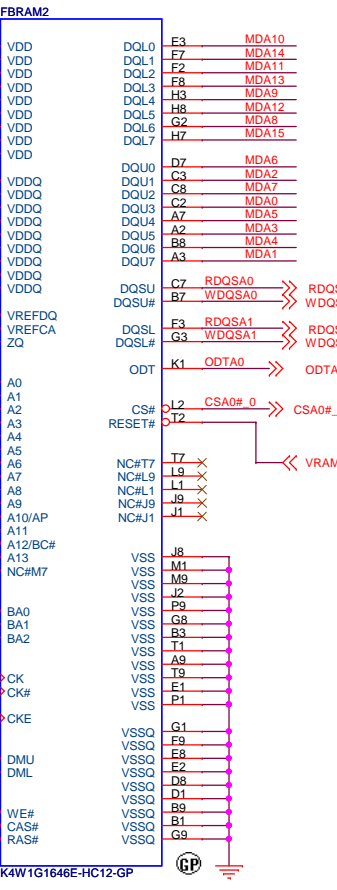
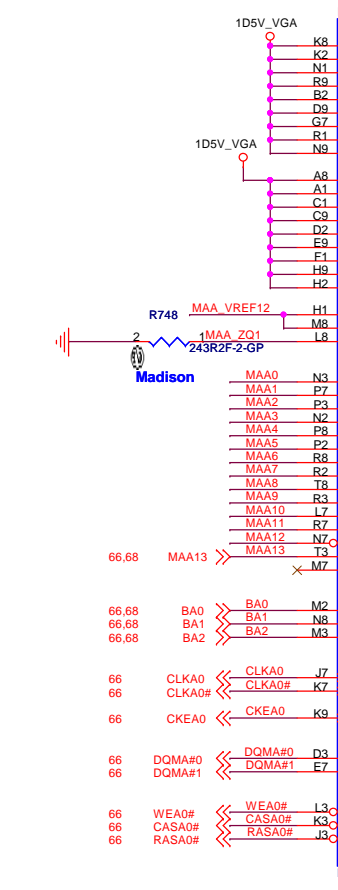
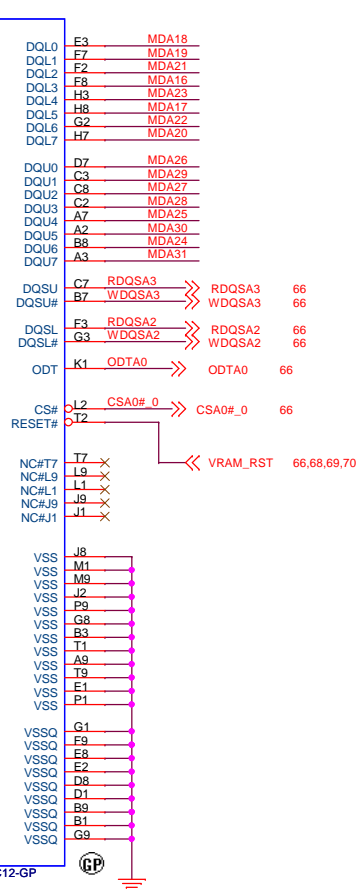
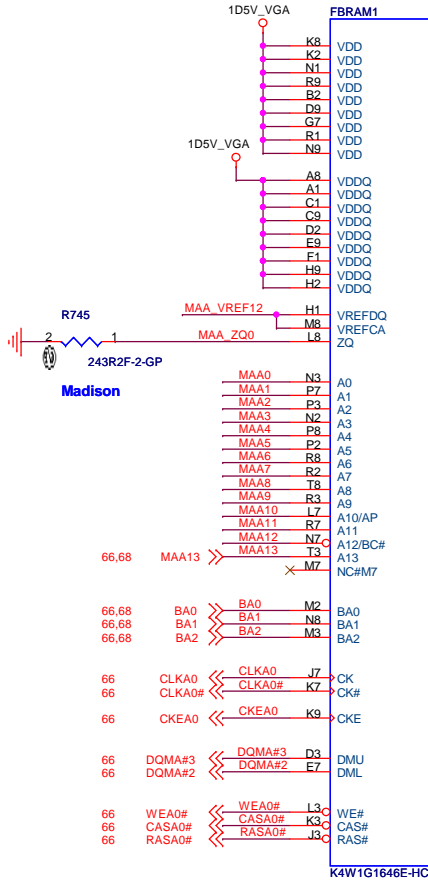
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Rev: SB

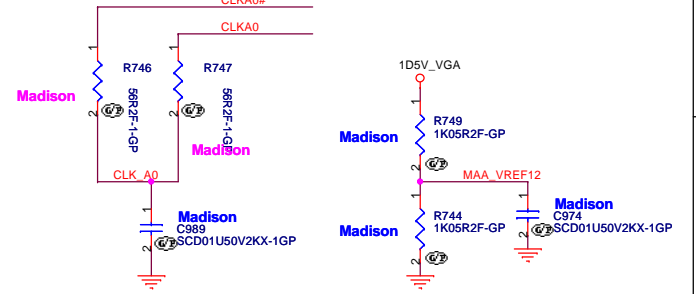
Document Number: JVS0-CP

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# DDR3



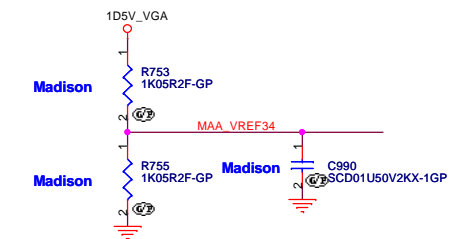
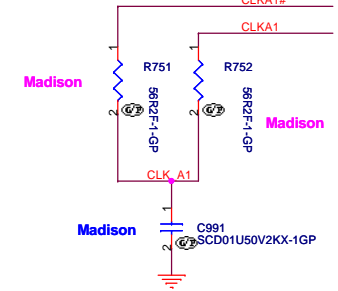
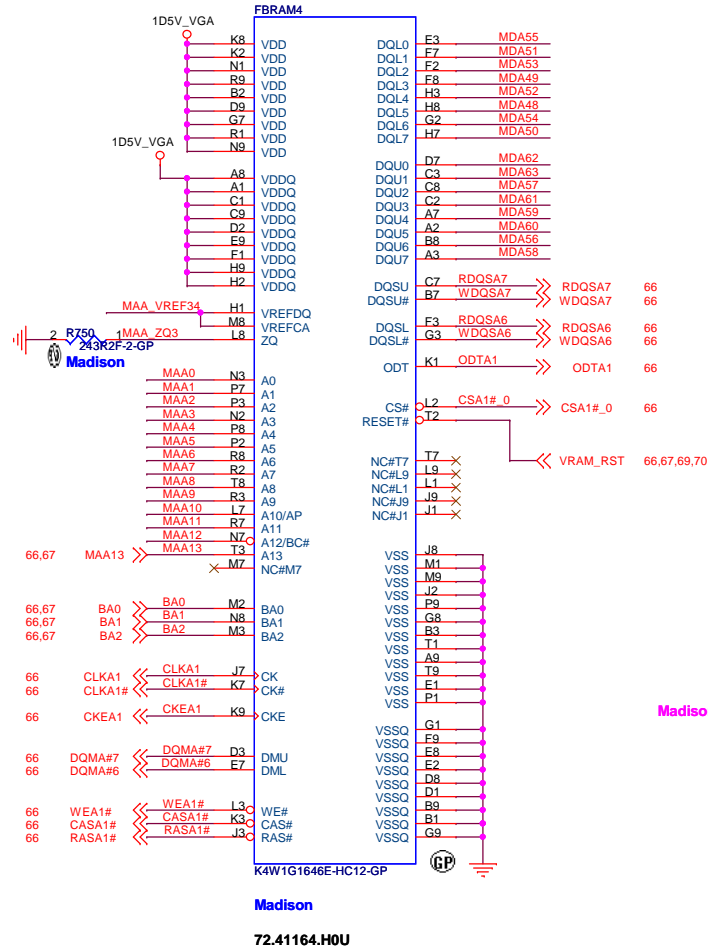
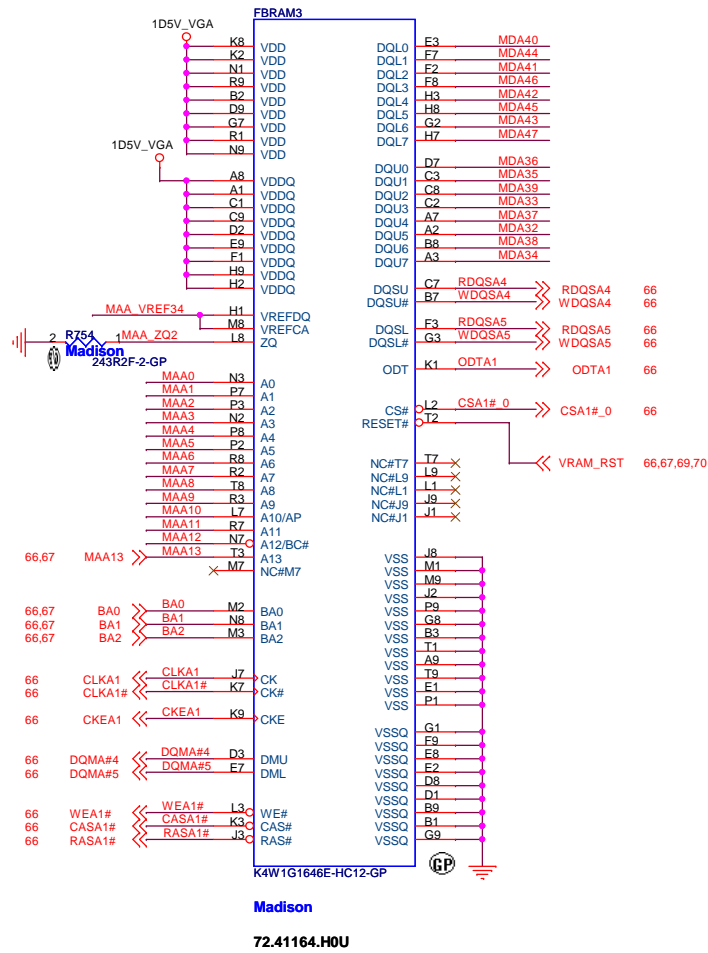
**SAMSUNG: 72.41164.H0U**  
**HYNIX: 72.51G63.C0U**



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Title	<b>VRAM(1/4)</b>	
Size A3	Document Number	Rev SB
<b>JV50-CP</b>		
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# DDR3



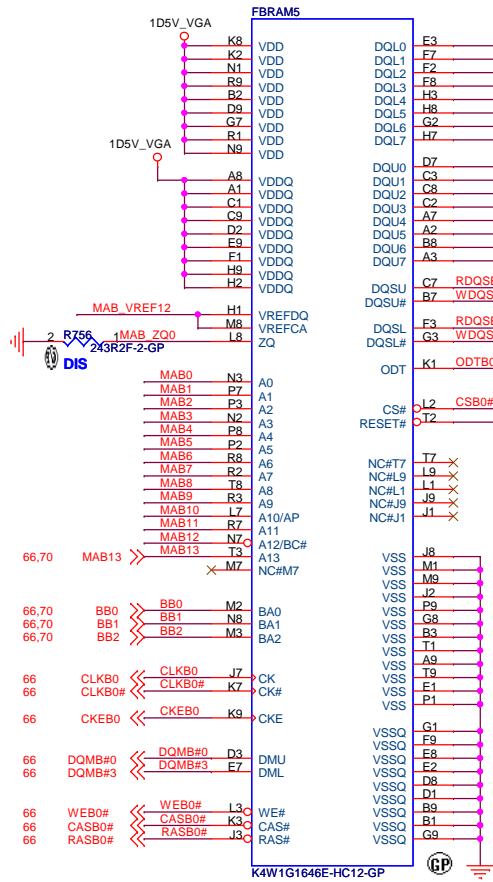
- 66,67 DQMA#[0..7] <<>>
- 66,67 RDQSA#[0..7] <<>>
- 66,67 WDQSA#[0..7] <<>>
- 66,67 MAA[0..12] << MAA[0..12]
- 66,67 MDA[0..63] <<>> MDA[0..63]

**SAMSUNG: 72.41164.H0U**  
**HYNIX: 72.51G63.C0U**

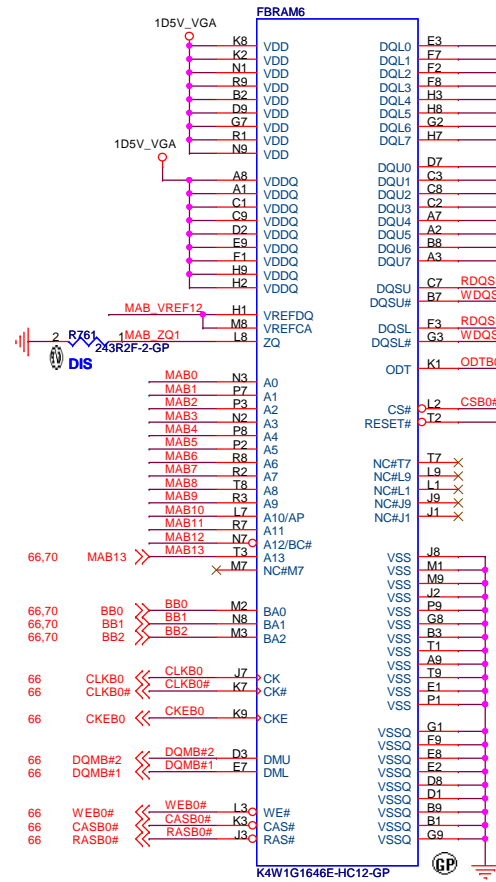
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<b>VRAM(2/4)</b>		
Title	Document Number	Rev
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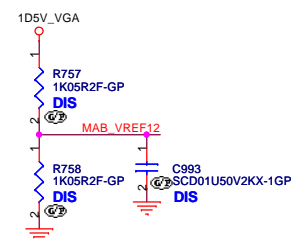
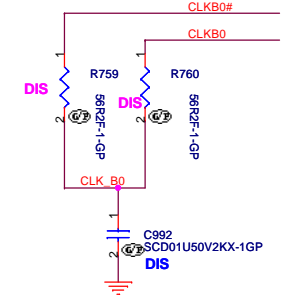
# DDR3



DIS  
72.41164.H0U



DIS  
72.41164.H0U



SAMSUNG: 72.41164.H0U  
HYNIX: 72.51G63.C0U

- 66,70 DQMB[0..7] <<< >>>
- 66,70 RDQS[0..7] <<< >>>
- 66,70 WDQS[0..7] <<< >>>
- 66,70 MAB[0..12] <<< MAB[0..12]
- 66,70 MDB[0..63] <<< MDB[0..63]

ENG DIS MADISON SAMSUNG

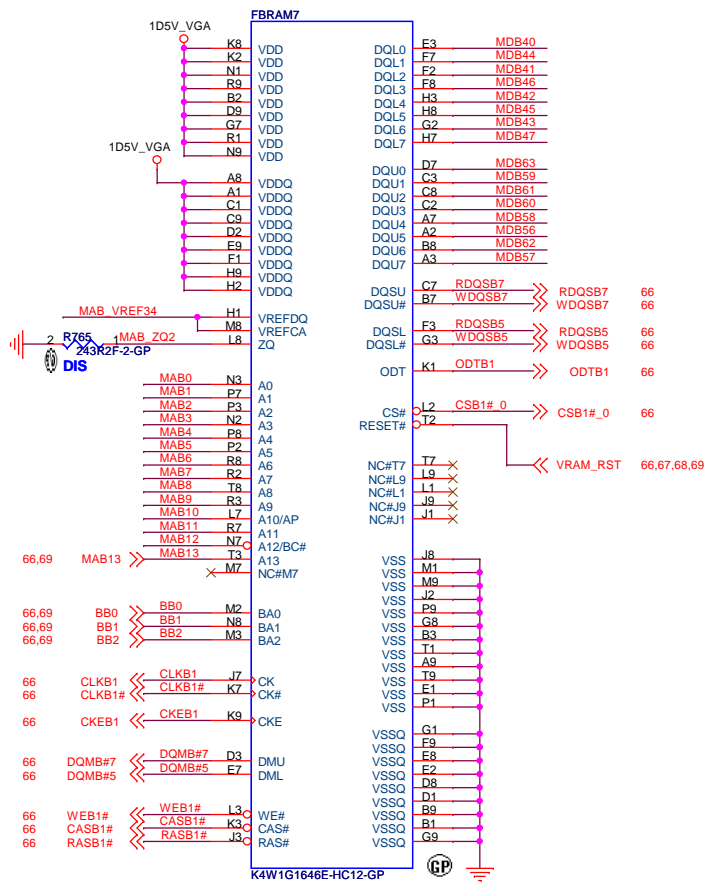
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM(3/4)**

Size: A3 Document Number: **JV50-CP** Rev: **SB**

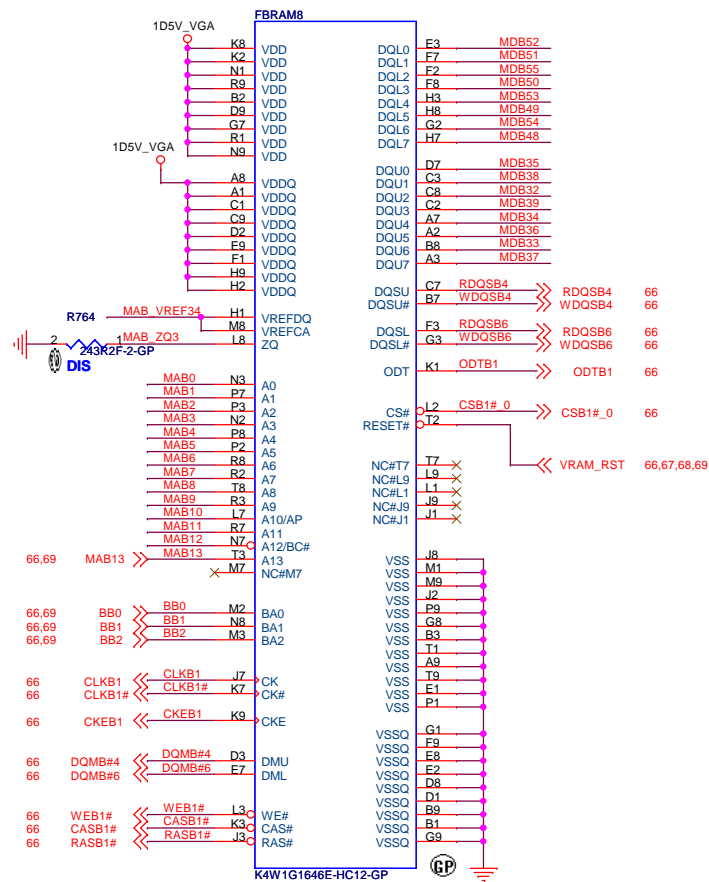
Date: Thursday, September 03, 2009 Sheet 69 of 68

# DDR3

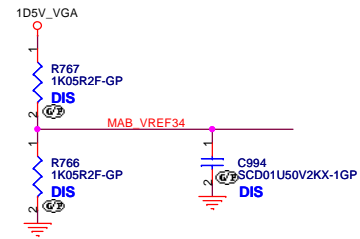
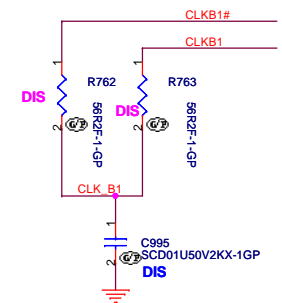


DIS  
72.41164.H0U

SAMSUNG: 72.41164.H0U  
HYNIX: 72.51G63.C0U



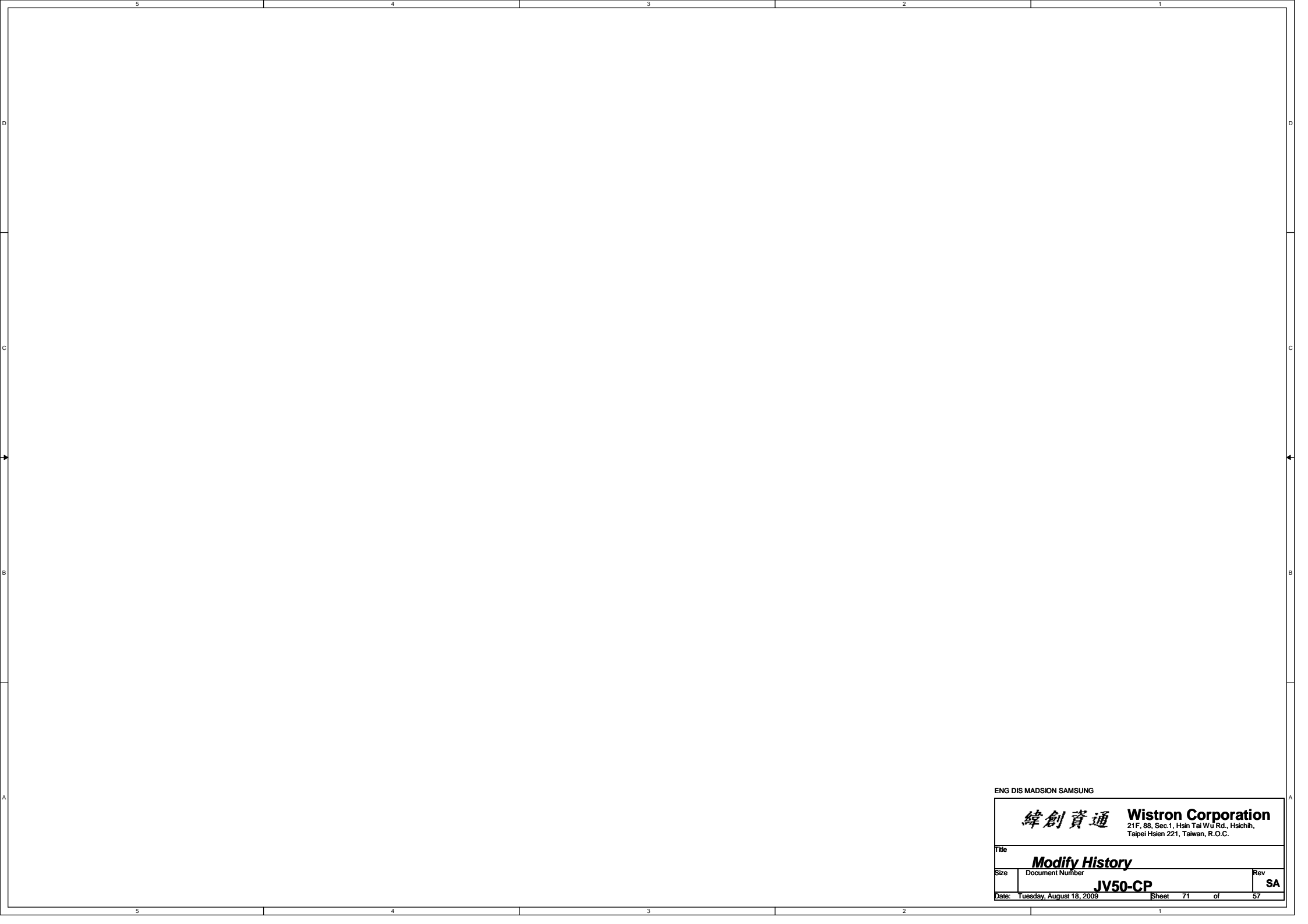
DIS  
72.41164.H0U



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Title		
<b>VRAM(4/4)</b>		
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Title

**Modify History**

Size

Document Number

**JV50-CP**

Rev

**SA**

Date: Tuesday, August 18, 2009

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