ACER_SJM31

MAIN BOARD

2009.05.04

Monday, May 04, 2009	2009-ECO-006989	A
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE= VER:

FILE NAME: XXXX-XXXXXX-XX

P/N XXXXXXXXXXX

INVENTEC

TITLE ACER_SJM31

SIZE	CODE	DOC.NUMBER	REV
C	CS	D-CS-1310A22752-0-ALG	B

SHEET 1 of 36

1. Schematic Page Description :

Montevina Schematic Ver : A02

1. Title
2. Schematic Page DESCR
3. Block Diagram
4. Annotations
5. Schematic Modify
6. Timing Diagram
7. Power Block Diagram
8. Adaptor in/Charge
9. 5VLA/5VA/3VA
10. 3VS/5VS/1.5V (DDR3)
11. 1.05VS/1.5S/1.8V/1.5VA
12. Power Latch/1.5VS/SCREW HOLE
13. CPU Core Power
14. GPU Core Power
15. Penryn Processor(1/2)
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17. CPU Thermal
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20. Cantiga DDRII(3/6)
21. Cantiga Power(4/6)
22. Cantiga Power(5/6)
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24. Clock Generator
25. DDR3 SDRAM SO-DIMM0
26. DDR3 SDRAM SO-DIMM1
27. ICH9M CPU/IDE/SATA(1/4)
28. ICH9M PCI/PCIE/DMI/USB(2/4)
29. ICH9M GPIO(3/4)
30. ICH9M Power/GND(4/4)
31. LCD CNN/SATA/3G/WLAN
32. KBC ITE8512F
33. IO CN 1/3
34. IO CN 2/3
35. IO CN 3/3
36. Audio Codec

INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
Schematic Page

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	A

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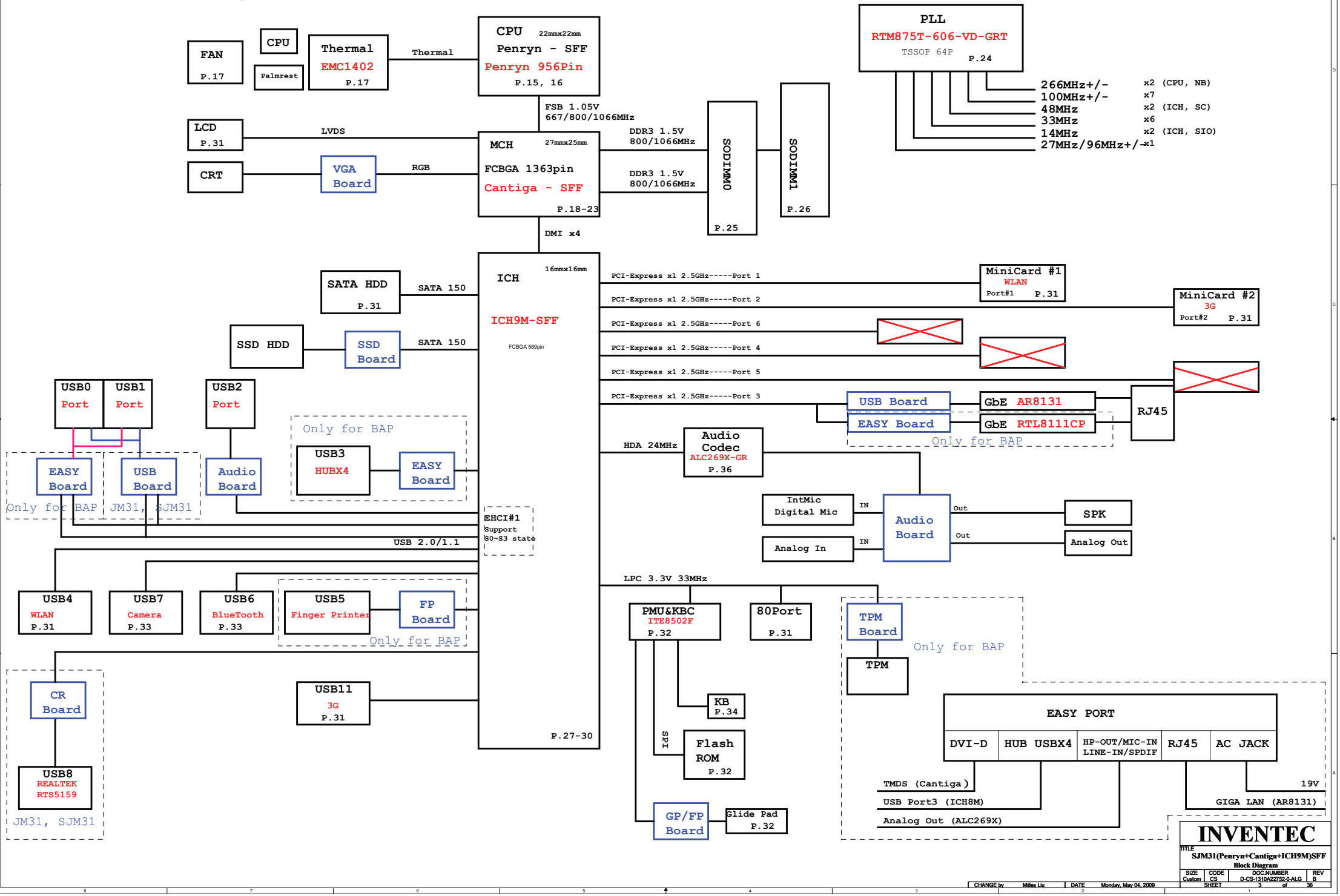
CHANGE by Miles Liu DATE Monday, May 04, 2009

3. Block Diagram :



INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

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4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9m by SLP_S3#_3R
+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Ground Plane
Layer 3	Stripline Layer
Layer 4	Power Plane
Layer 5	Stripline Layer
Layer 6	Stripline Layer
Layer 7	Ground Plane
Layer 8	Solder Side,Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn SFF HFM:	1.3319V~1.4375V~1.4591V	18A
	LFM:	0.9221V~0.9625V~0.9739V	
1.05VS	Penryn SFF : AGTL+ termination	1V~1.05V~1.10V	4.5A
	Cantiga GS: Core	0.997V~1.05V~1.102V	8.7A
	Cantiga GS: PCIE	0.9975V~1.05V~1.1025V	1.78A
	Cantiga GS:Core+IMEL+HSIO	0.9975V~1.05V~1.1025V	2.898A
	Cantiga GS:VCC_GMCH	0.997V~1.05V~1.102V	10.154A
	Cantiga GS:VCCA_SM_CK and NCTF	0.997V~1.05V~1.102V	37.95mA
	Cantiga GS:VCC_DMI	0.997V~1.05V~1.102V	456mA
	Cantiga GS:VCCA_SM	0.997V~1.05V~1.102V	747.5mA
	Cantiga GS:VTT	0.997V~1.05V~1.102V	852mA
	ICH9M:VCC1_05	0.997V~1.05V~1.102V	1.634A
	ICH9M:DMI	0.997V~1.05V~1.102V	48mA
	ICH9M:CPU_IO	0.997V~1.05V~1.102V	2mA
1.5VS	Penryn SFF PLL	1.425V~1.5V~1.575V	130mA
	Cantiga GS: QDAC	1.425V~1.5V~1.575V	0.5mA
	Cantiga GS: LVDS	1.71V~1.8V~1.89V	60.31mA
	Cantiga GS: TVDAC	1.425V~1.5V~1.575V	35mA
	Cantiga GS: Various PLLS analog supply	1.425V~1.5V~1.575V	485mA
	Cantiga GS: VCC_SM_CK	1.425V~1.5V~1.575V	149.5mA
	Cantiga GS: VCC_SM	1.425V~1.5V~1.575V	3.1625A
	ICH9M:PCIE_ICH	1.425V~1.5V~1.575V	646mA
	ICH9M:SATA_ICH	1.425V~1.5V~1.575V	1.342A
	ICH9M:VCC_GLAN	1.425V~1.5V~1.575V	80mA
	Mini Card:		
	Express Card:	1.425V~1.5V~1.575V	650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V~1.5V~1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	:DDRIII Terminator:	0.7125V~0.75V~0.7875V	1.0A
3VS	Cantiga GS: HV CMOS	3.135V~3.3V~3.465V	105.3mA
	Cantiga GS: VCCS_TVDAC	3.135V~3.3V~3.465V	78mA
	ICH9M:VCC3_3	3.135V~3.3V~3.465V	308mA
	ICH9M:VCCGLAN3_3	3.135V~3.3V~3.465V	1mA
	Thermal Sensor:	3.0V~3.3V~3.6V	5mA
	Mini Card: UMTS		
	Express Card:	3.135V~3.3V~3.465V	1.3A
	CLK Generator: ICS9LPRS365BKLFT	3.135V~3.3V~3.465V	500mA
	Mini Card: WirelessLan		
	Bluetooth:	3.0V~3.3V~3.6V	
	Super I/O: IT8305E		
	Azalia Codec: ALC262		
	Azalia MDC:		
1.8VS	DVI	3.0V~3.3V~3.6V	120mA
3VA	ICH9M: RTC	2V~3.3V~3.465V	6uA
	ICH9M:VCCSUS3_3	3.135V~3.3V~3.465V	212mA
	ICH9M:VCCCL3_3	3.135V~3.3V~3.465V	73mA
	ICH9M:VCCLAN3_3	3.135V~3.3V~3.465V	78mA
	LCD:	3.0V~3.3V~3.6V	2A
	Lan:AR8131	3.0V~3.3V~3.6V	1A
	Azalia MDC:		
	Flash ROM: BIOS	3.0V~3.3V~3.6V	
5VS	Cardreader: RTS5159	3.0V~3.3V~3.6V	
	Azalia Codec: ALC269	3.0V~3.3V~3.6V	
	HDD: SATA	4.75V~5.0V~5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA
	~~ODD: SATA~~	~~4.75V~5.0V~5.25V~~	~~Max: 1.5A ; R/W: 900mA ; STDBY: 45mA~~
	~~Audio AMP: G1432~~		
	Inverter:		
	WebCam	4.75V~5.0V~5.25V	1A
5VA	USB: x 2 ports	5VA	2A
	USB	5VA	1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V~3.3V~3.6V	300mA

CHANGE by: Miles Liu | DATE: Monday, May 04, 2009

INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
ANNOTATIONS

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

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6.Schematic modify Item and History :

2009.0108

1. ADD USB P3 for Docking, USB P5 for Finger printer,
   Modify CN5 -----P28
2. Modify CN20 to 50pin-------P33
3. Move PWR_SWIN# from CN14 to CN20
4. ADD TPM module------P34

2009.0109

1. ADD DOCK_USB_EN, DOCK_CRT_IN#-----P32,33

2009.0112

1. Change power item: R490,R291,BAT CNN TH PIN

AX1 to A01 change list

1. Change AD_ON circiut for Green adaptor PC. (Page 12)
2. Change thermal shut down control by PM_ICH_PWROK from ALL_SYSPWRGD. (Page 17)
3. Add PCIE I/F to 3G mini card connector for support EM772 (Page24, Page28, Page31)

A01 to A02 change list (JM31 A02, SJM31 A01)

1. Add EC_3VLA soft start circuit --- Change R480 to NU, Add Q28, R378,R738,C374,R299,Q118,R739,C376 (Page 9)
2. Add 3VA porotect diode --- Add D35 (Page 9)
3. For green adaptor --- Change C419 from 0.1uf to 4.7uF , Add Q120, R744,R742,R743 (Page 8, 12)
4. For power consumption --- Change Q37,Q50,Q51 from 6015B0090401 to 6015B0082201, Change Q54,Q38,Q48 from 6015B0086301 to 6015B0089301.(Page 8, 10, 11)
5. Change R29,R30,R31,R32,R33,R34,R35 from 0 Ohm to short pad.(Page 13)
6. For safty ---- Change R231 from 0 Ohm to 330 Ohm, R226 from 665 Ohm to 330 Ohm. (Page 27)
7. For 3G leakage ---- Delete R220,R211 (Page 29)
8. Delete reverse HW timing circuit. ---- Delete U7,D13,R237,C376,U9,U8,D9,R222,C327 (Page 29, 32)

A02 for SJM31 change list

1. R513 change to 470 for SJM31 TP lock LED

INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
Schematic Modify

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

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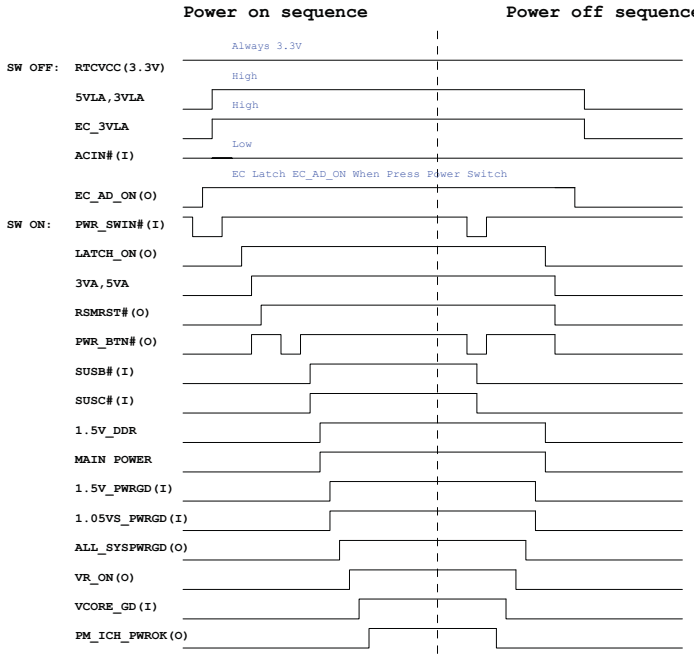
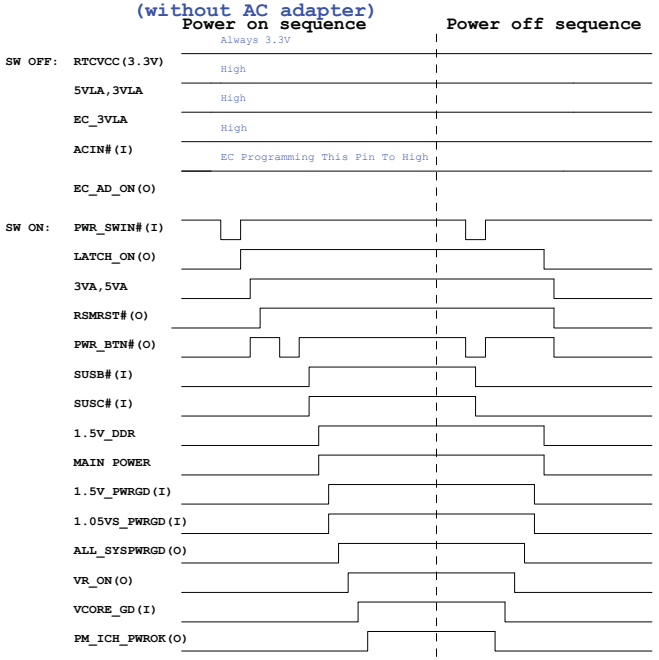
SYSTEM POWER ON/OFF SEQUENCE

Drawing : Wendy, Huang

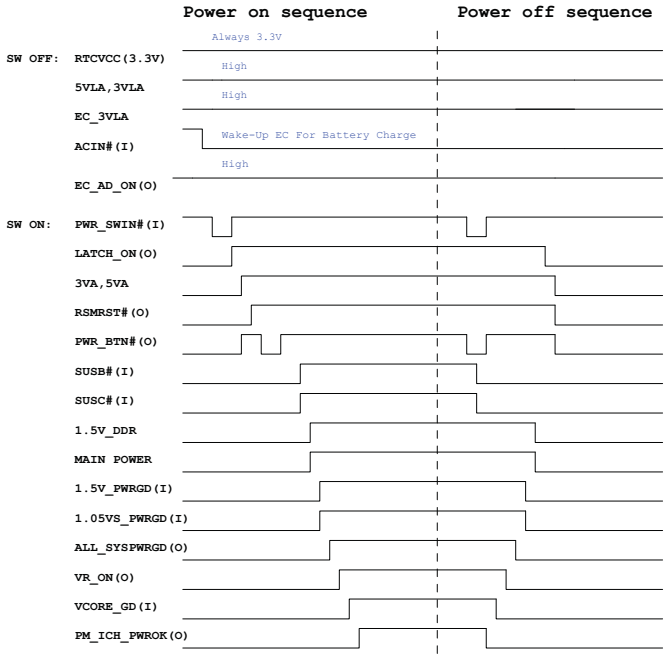
Power on/off sequence AC insert (without Battery Pack)



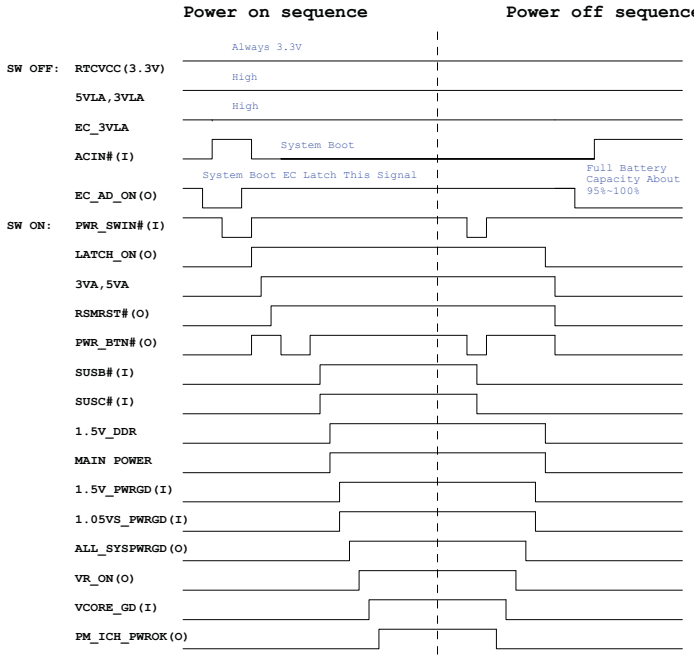
Power on/off sequence Battery insert (without AC adapter)



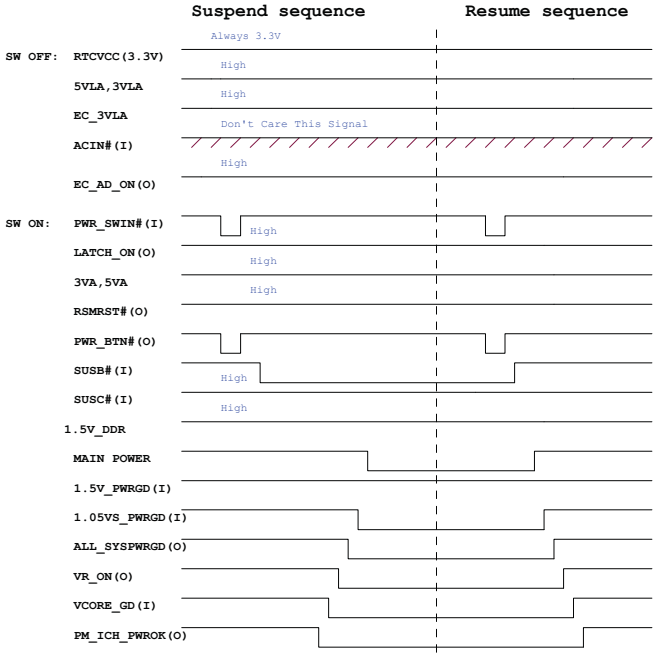
Power on/off sequence AC insert(with charge over 95%)



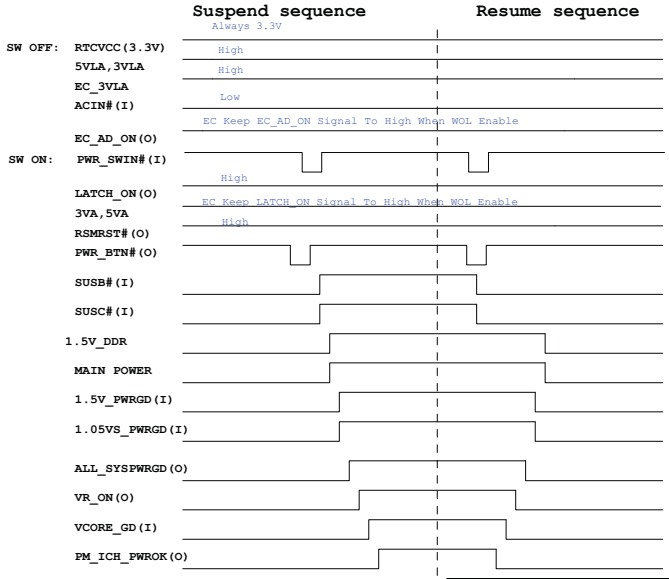
Power on/off sequence AC insert(without charge over 95%)



Suspend And Resume Sequence (S3)



Power on/off sequence after windows shoutdown (WOL enable)



INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
Time Diagram

SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

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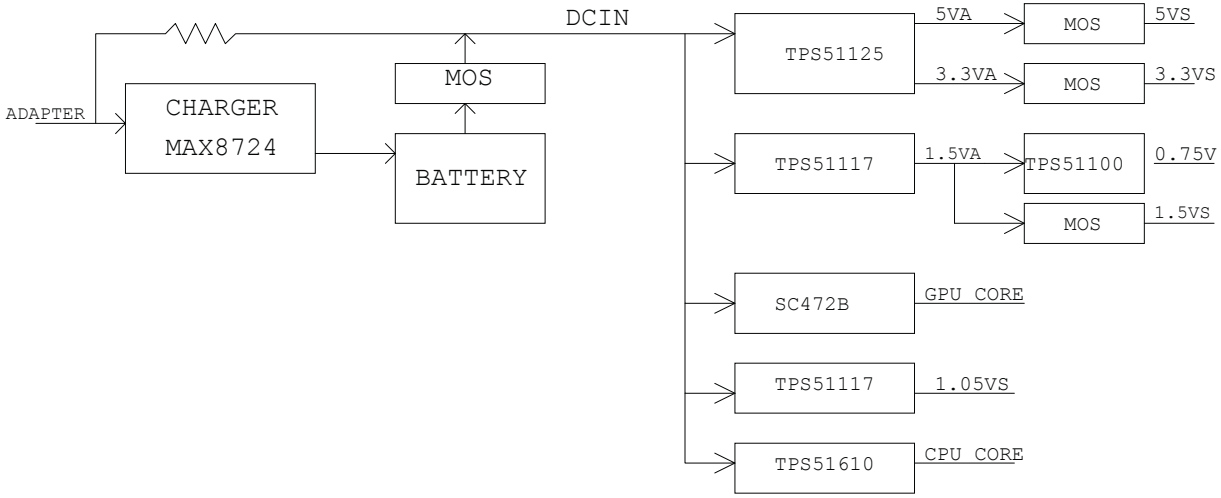
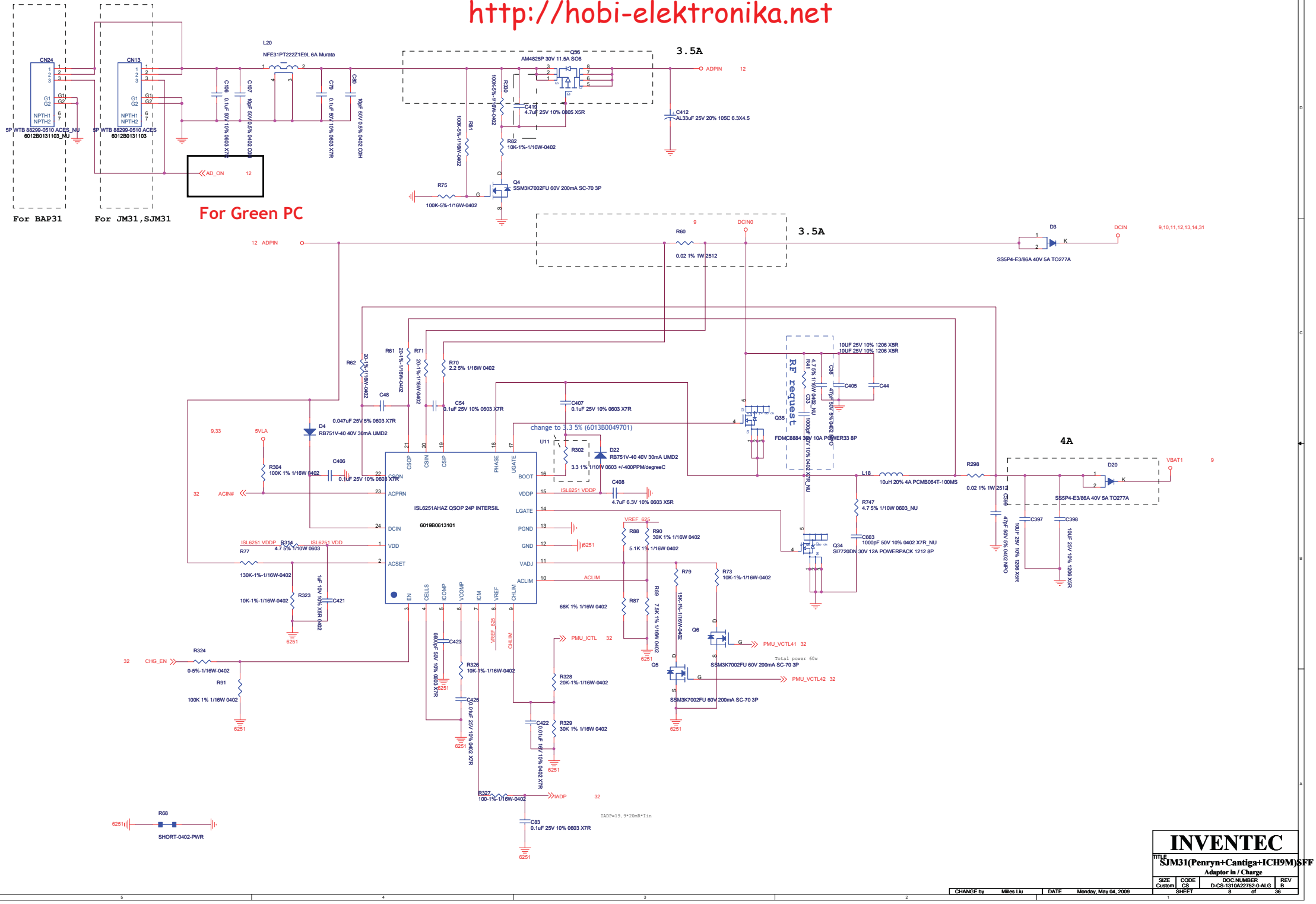
Power Block Diagram :



INVENTEC			
TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF Power Block Diagram			
SIZE: C	CODE: CS	DOC.NUMBER: D-CS-1310A22752-0-ALG	REV: B
CHANGE by: Miles Liu	DATE: Monday, May 04, 2009	SHEET: 7 of 36	



CHANGE by	Miles Liu	DATE	Monday, May 04, 2009

INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
Adaptor in / Charge

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

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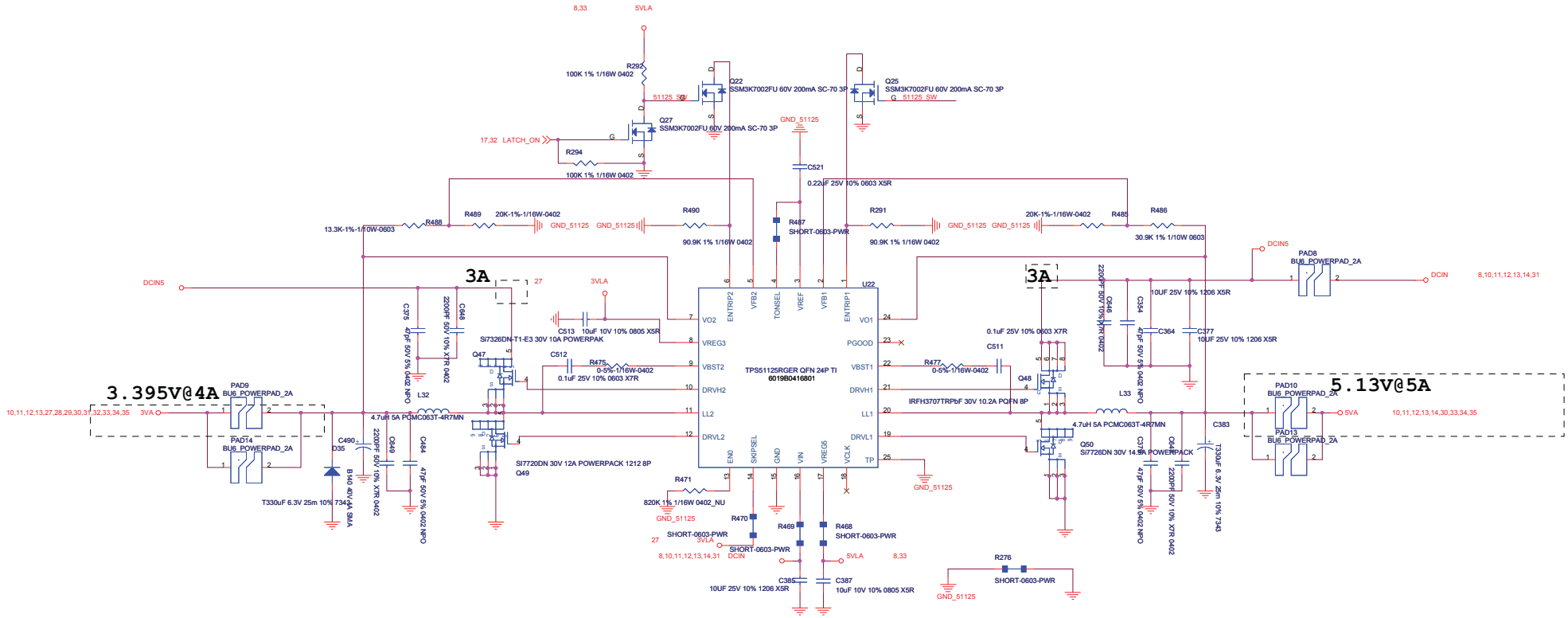
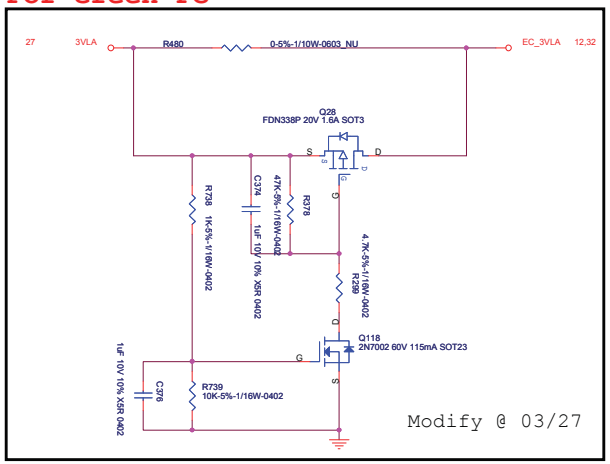
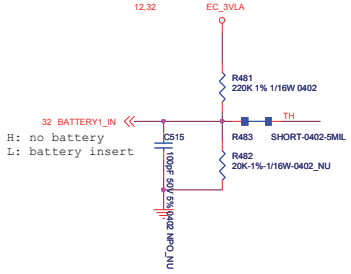
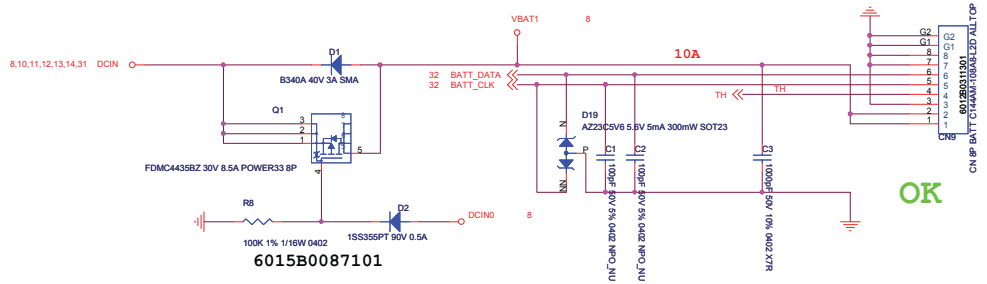


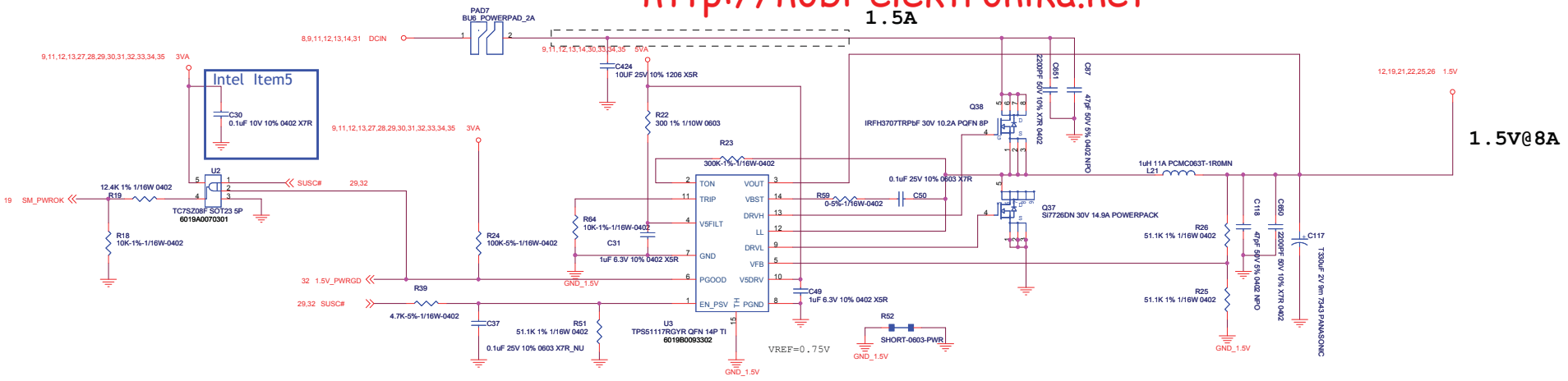
For Green PC

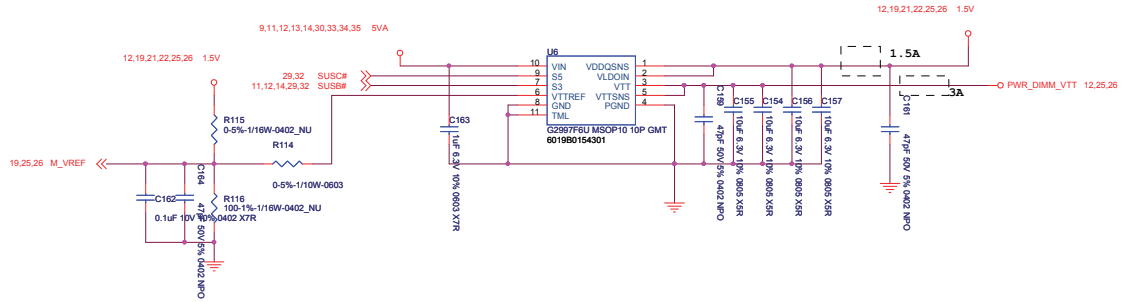




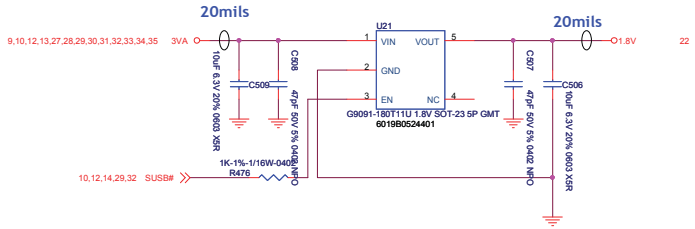


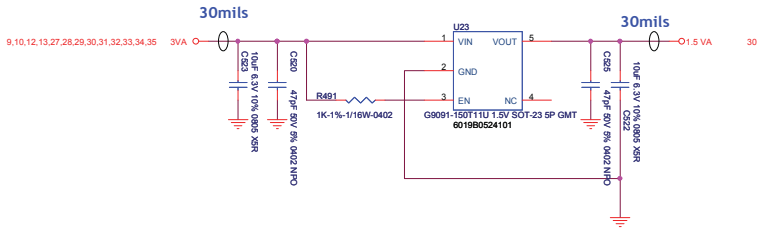
INVENTEC			
TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF 5VLA/5VA/3VLA/3VA			
SIZE: Custom	CODE: CS	DOC.NUMBER: D-CS-1310A22752-0-ALG	REV: B
CHANGE by: Miles Liu	DATE: Monday, May 04, 2009	SHEET: 9 of 36	

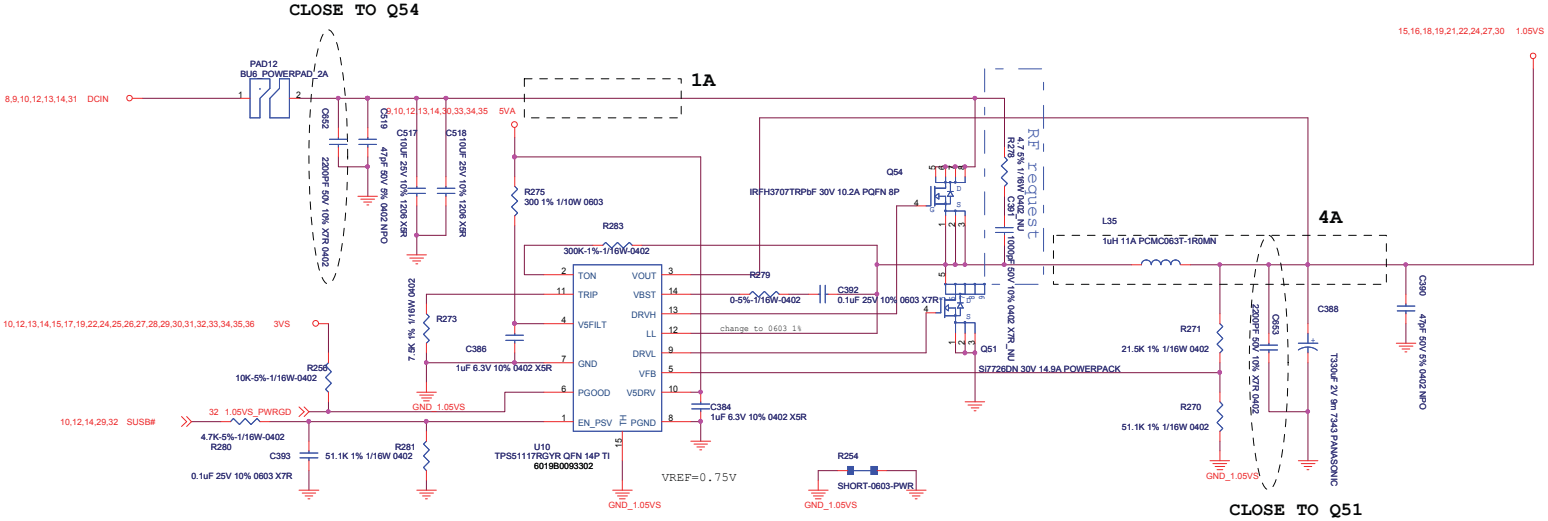




INVENTEC			
TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF 3VS/5VS/1.5V (DDR3)			
SIZE: Custom	CODE: CS	DOC.NUMBER: D-CS-1310A22752-0-ALG	REV: B
CHANGE by: Miles Liu	DATE: Monday, May 04, 2009	SHEET: 10 of 36	







CHANGE by	Miles Liu	DATE	Monday, May 04, 2009

INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
1.05VS/1.5S/1.8V/1.5VA

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

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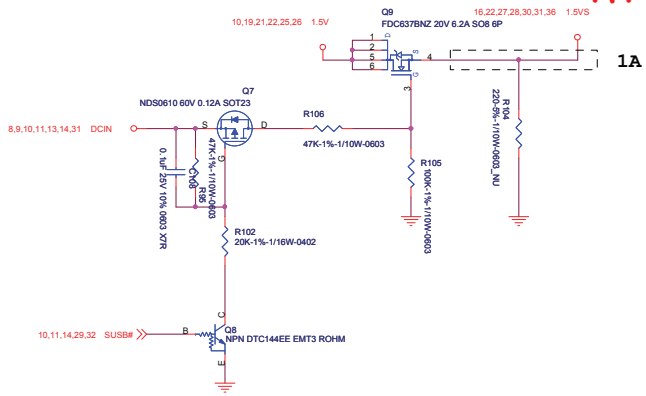
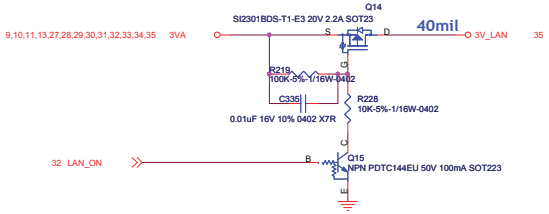
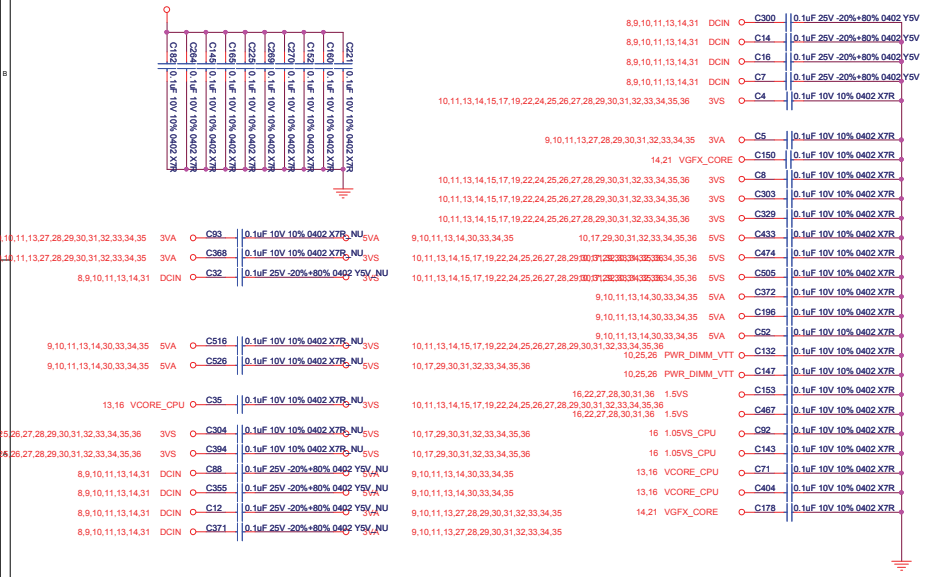
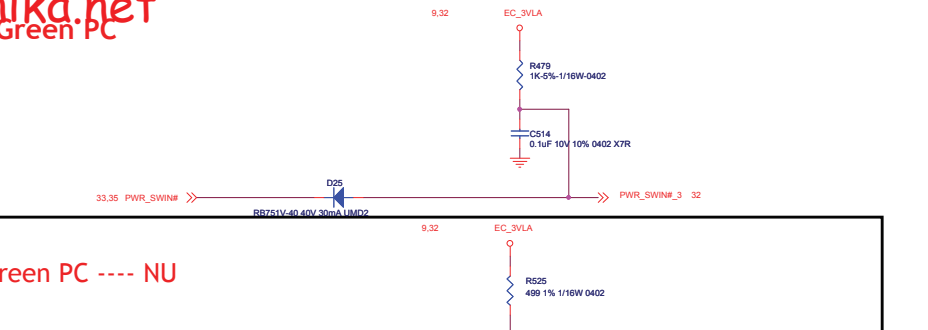
1.5VS

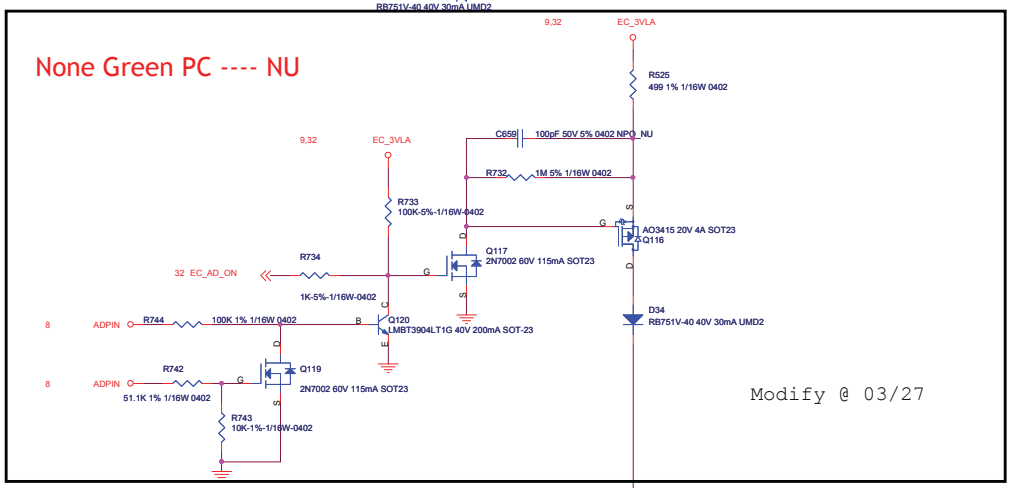


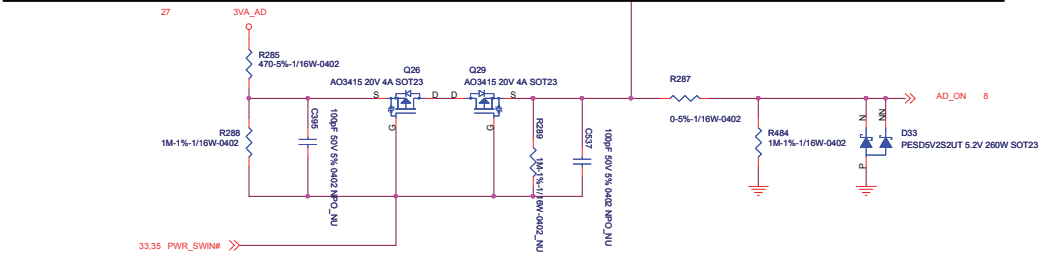


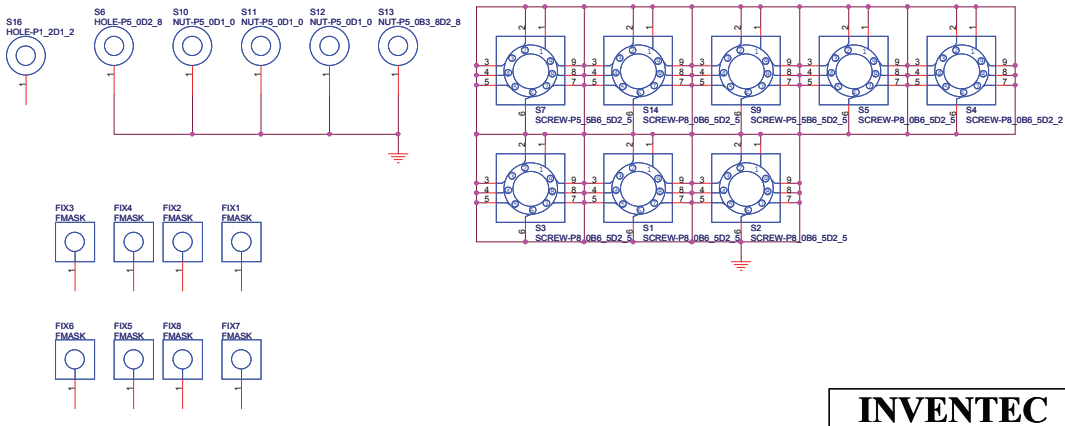
EMI Cap









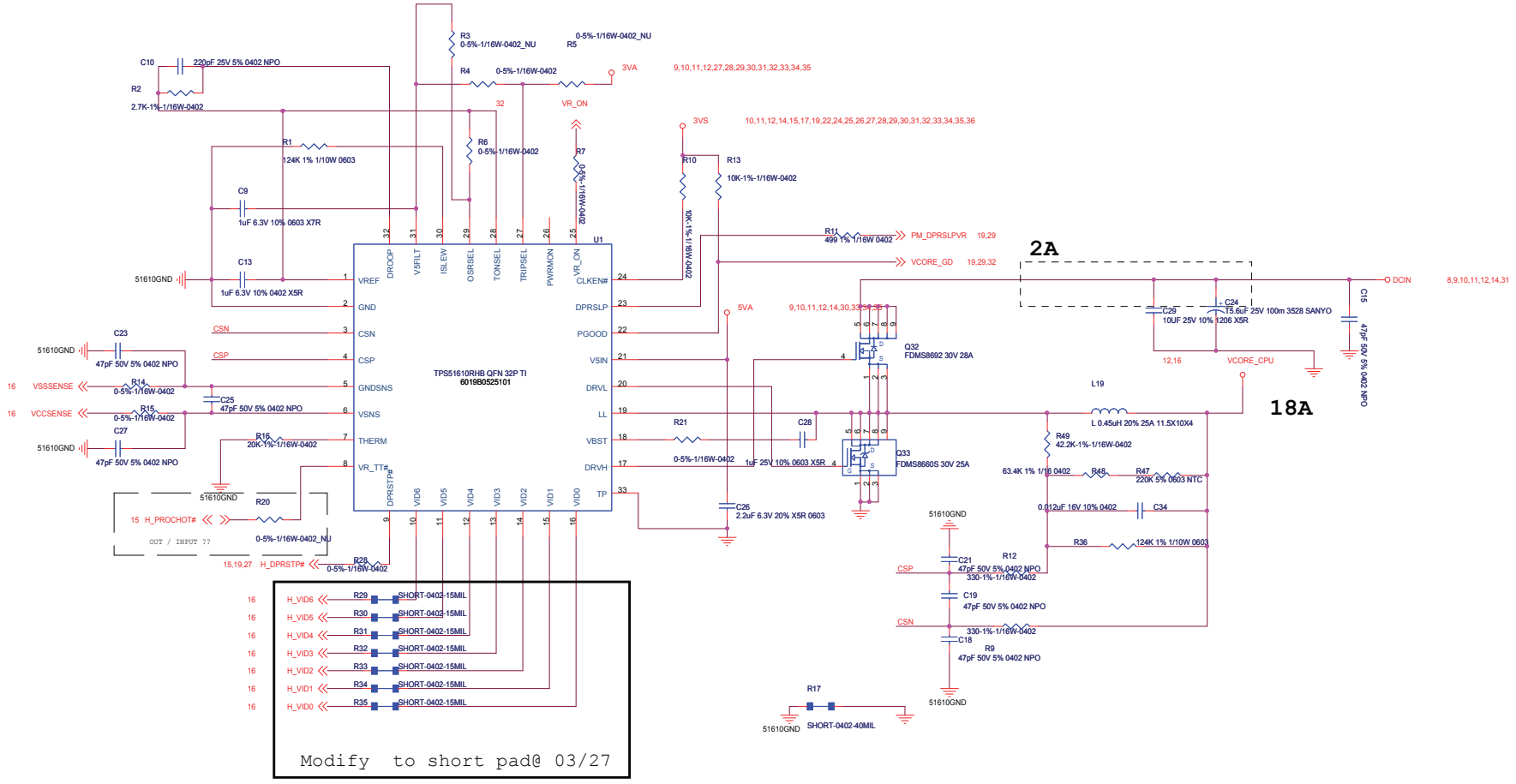


CHANGE by	Miles Liu	DATE	Monday, May 04, 2009	SHEET	12 of 36

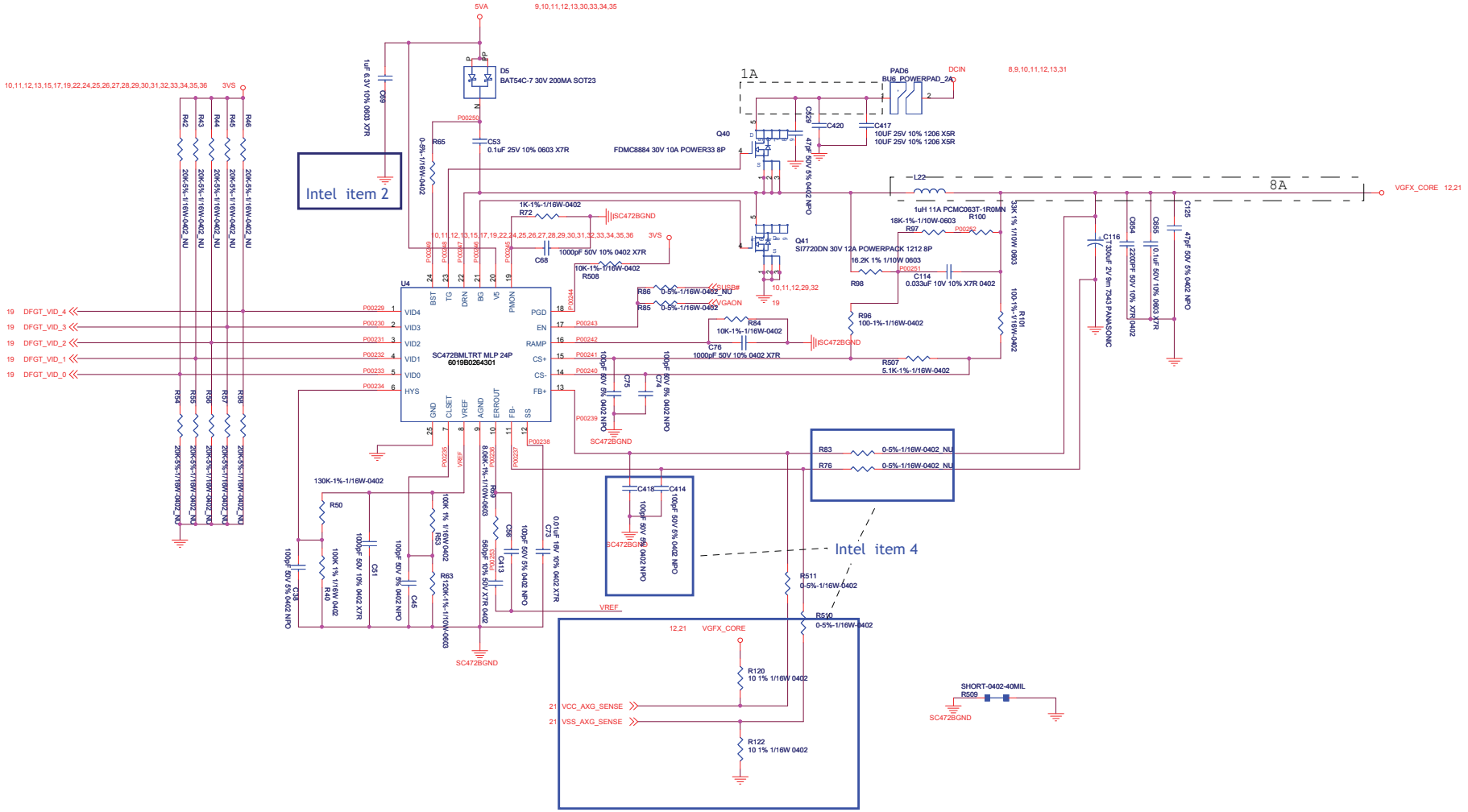
INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
Power on latch

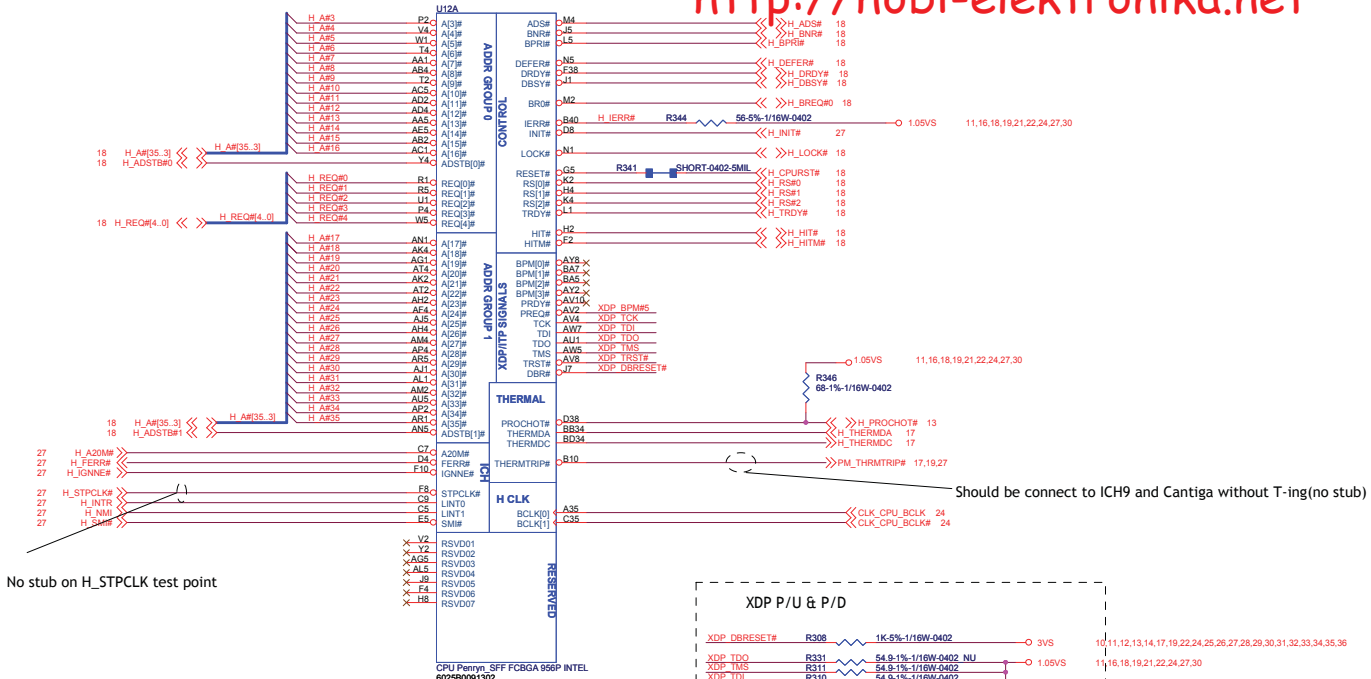
SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

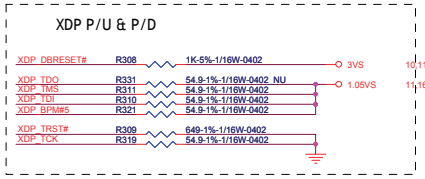


INVENTEC			
TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF CPU Core Power			
SIZE: C	CODE: CS	DOC.NUMBER: D-CS-1310A2Z752-0-ALG	REV: B
CHANGE by: Milles Liu	DATE: Monday, May 04, 2009	SHEET: 13 of 36	

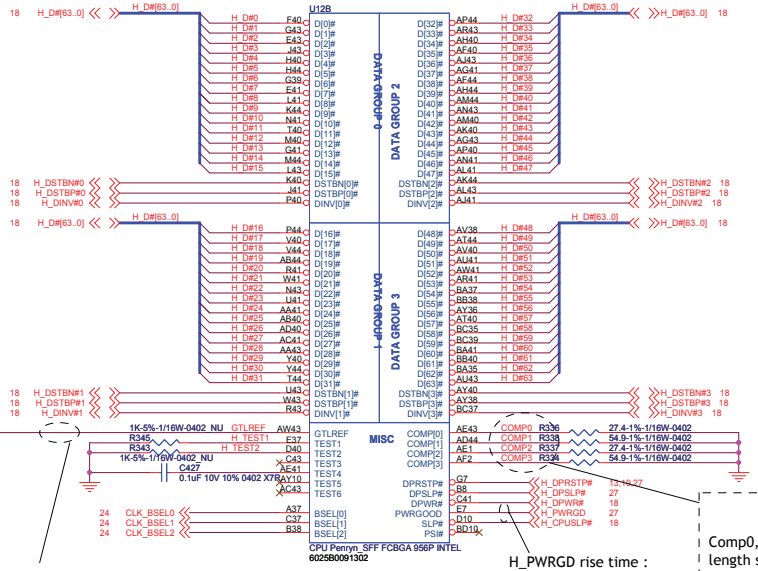


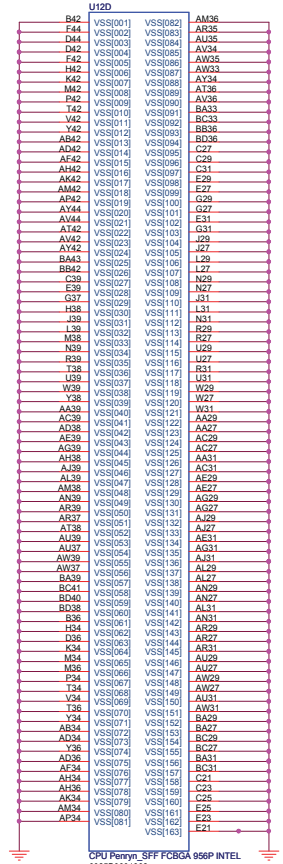
INVENTEC			
TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF GPU CORE			
SIZE: Custom	CODE: CS	DOC.NUMBER: D-CS-1310A22752-0-ALG	REV: B
CHANGE by: Miles Liu	DATE: Monday, May 04, 2009	SHEET: 14 of 36	

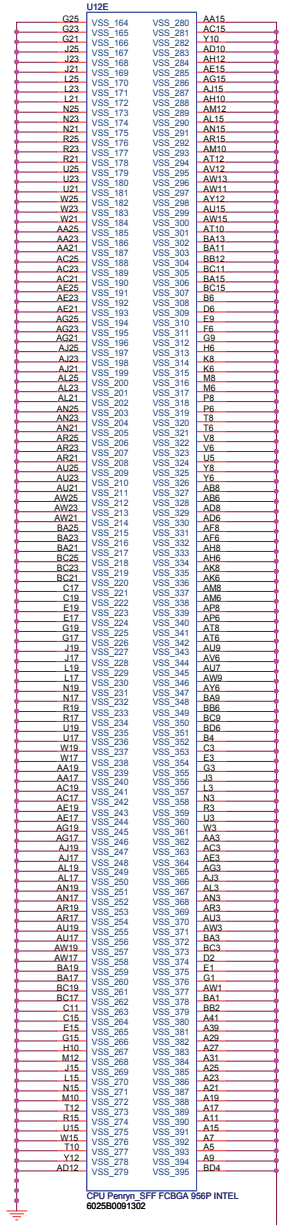




A#[32-39], APM#[0-1]:Leave escape routing on for future functionality





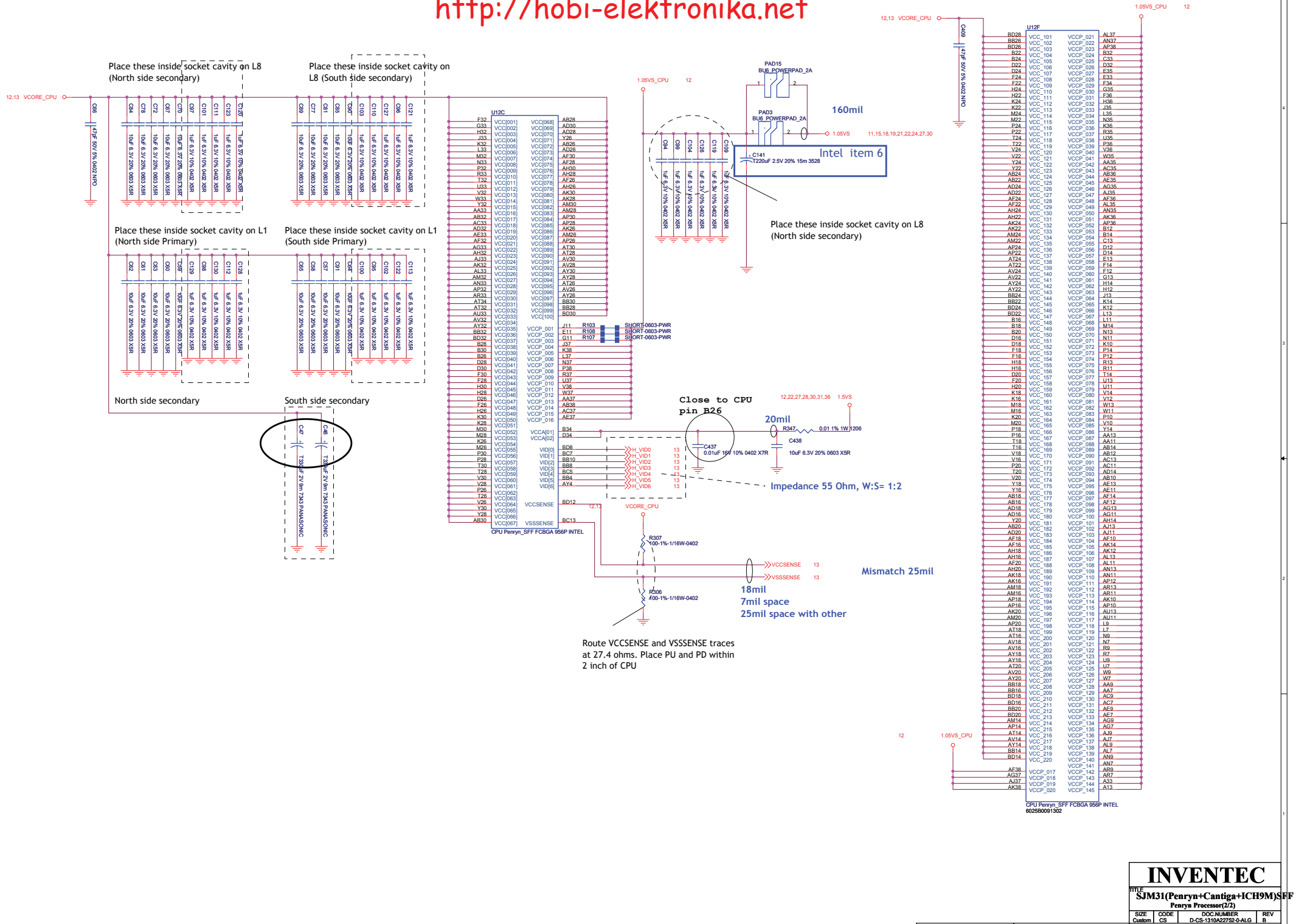


INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
Penryn Processor(1/2)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

CHANGE by: Miles Liu | DATE: Monday, May 04, 2009 | SHEET 15 of 36



CHANGE by	Miles Liu	DATE	Monday, May 04, 2009

INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
Penryn Processor(2/2)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

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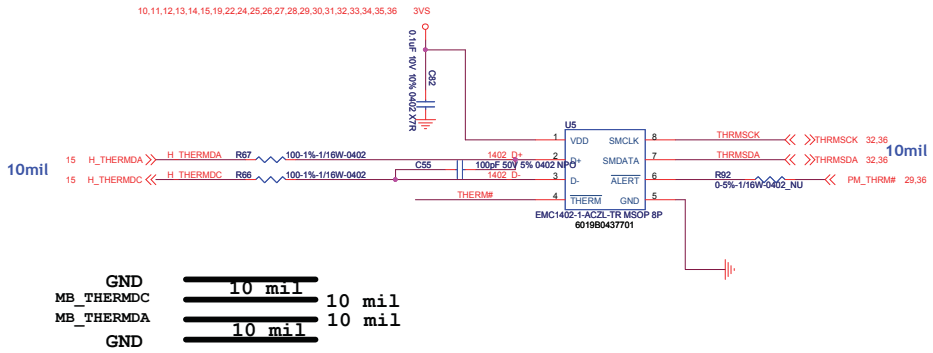
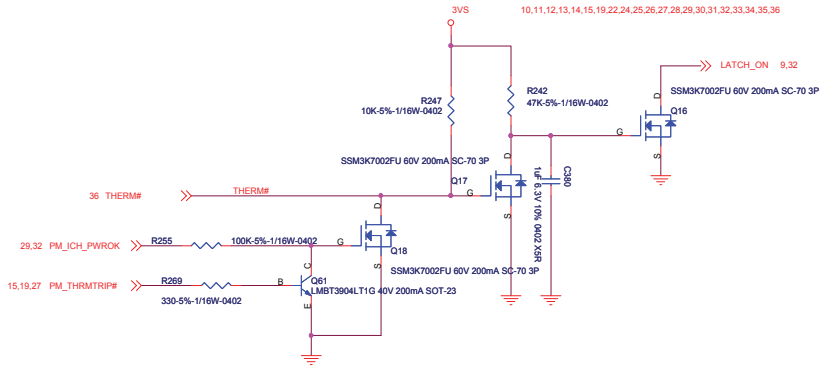
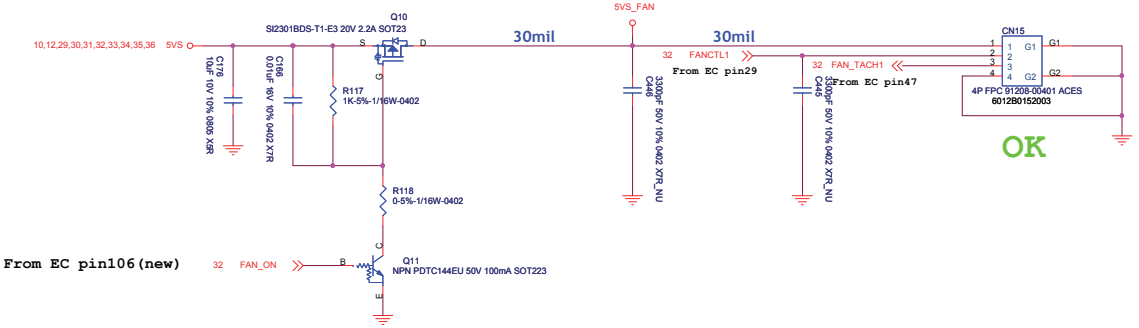
THERMAL SENSOR





Fan control

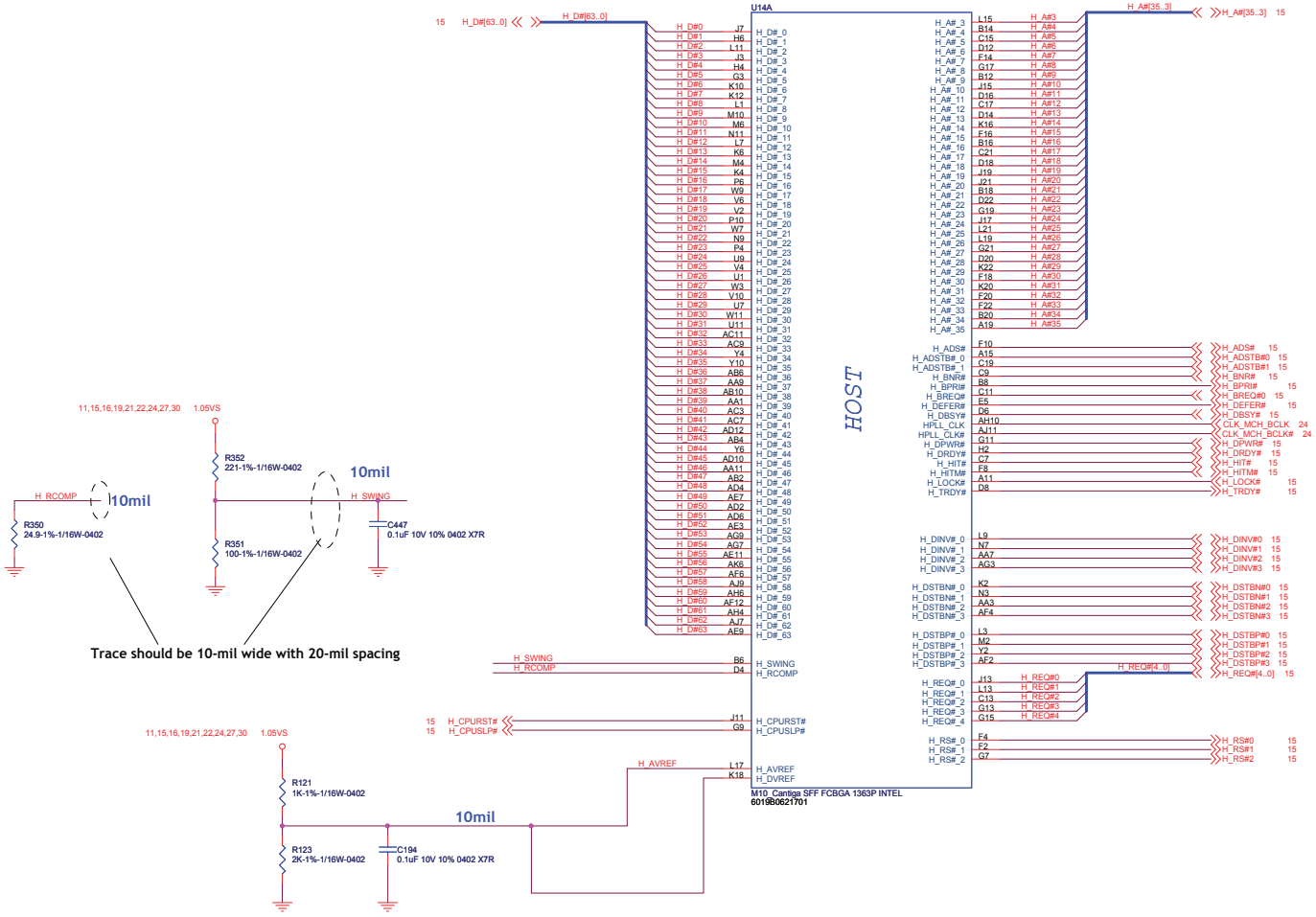


CHANGE by	Miles Liu	DATE	Monday, May 04, 2009

INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
CPU Thermal

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B
SHEET	17	of	36



CHANGE by	Milles Liu	DATE	Monday, May 04, 2009

INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
Cantiga Host(1/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

SHEET 18 of 36

Route M_OCDCMOP 0&1 as short as possible

Place 150ohm termination resistor close to GMCH

As close as possible to GMCH and Minimum spacing of 20 mils away from any toggle signals

When the display is completely white , the RGB voltage is between 665mV to 770mV by VESA Spec

If meet , CRT_IREF resistor value is optimal

INTEL SPEC : 75nF ~ 200nF

Cantiga Strapping:

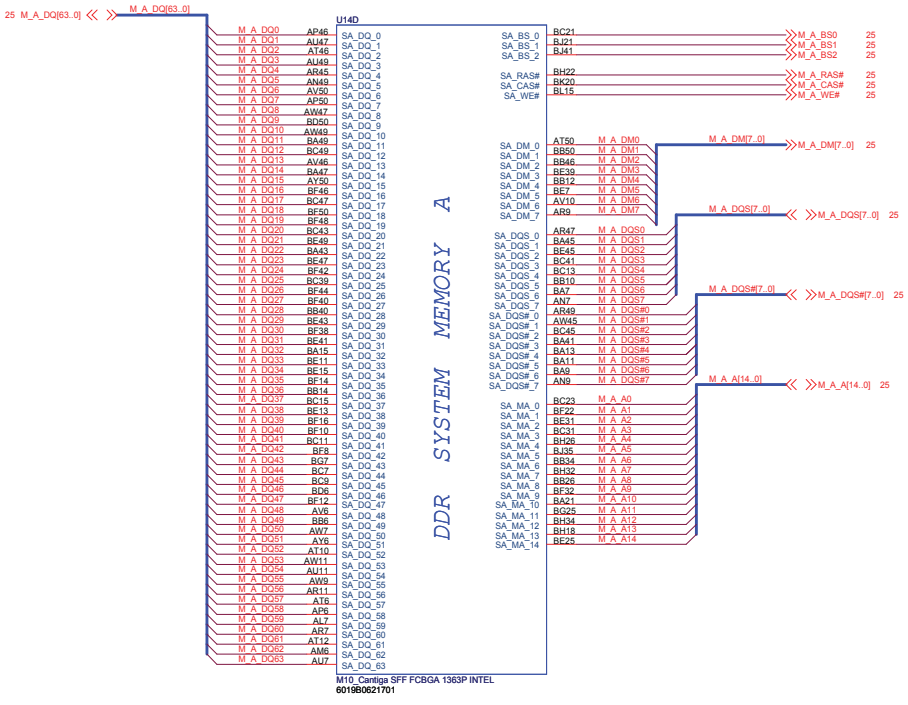
	Low	High
MCH_CFG5	DMIx2	DMIX4
MCH_CFG6(iTPM Host I/F)	Enable	Disable(default)
MCH_CFG7(TLS confidentiality)	With	With no(default)
MCH_CFG9 (PCIE Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG10 (PCIE loopback)	Enable	Disable(default)
MCH_CFG12 (ALLZ)	Enable	Disable(default)
MCH_CFG13(XOR)	Enable	Disable(default)
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only SDVO or PCIE x1 is operation	Only SDVO or PCIE x1 with PEG port

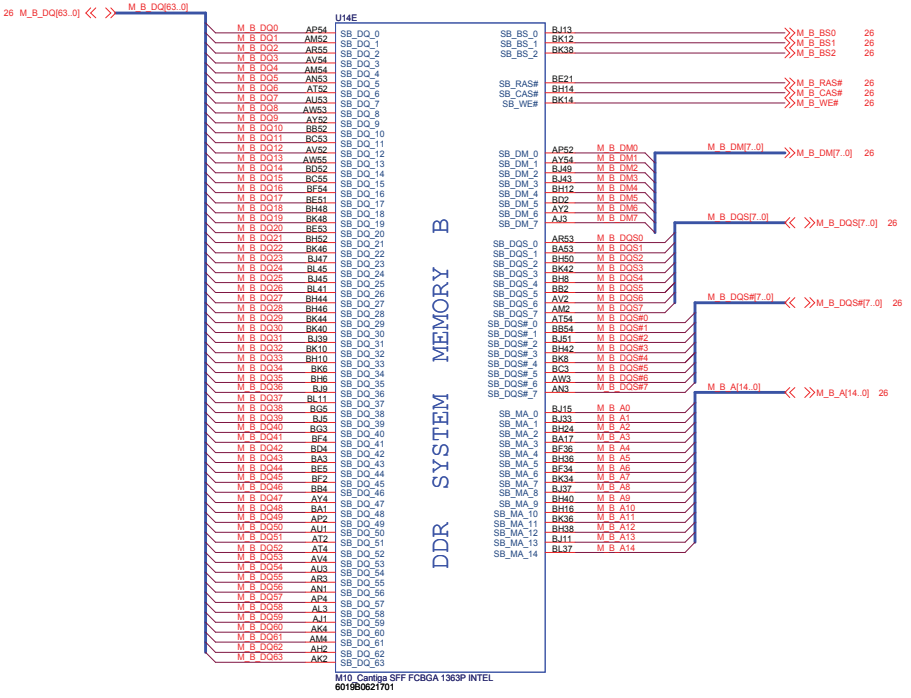
INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
Cantiga DMI/Graph2/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

CHANGE by: Milles Liu | DATE: Monday, May 04, 2009 | SHEET 19 of 36



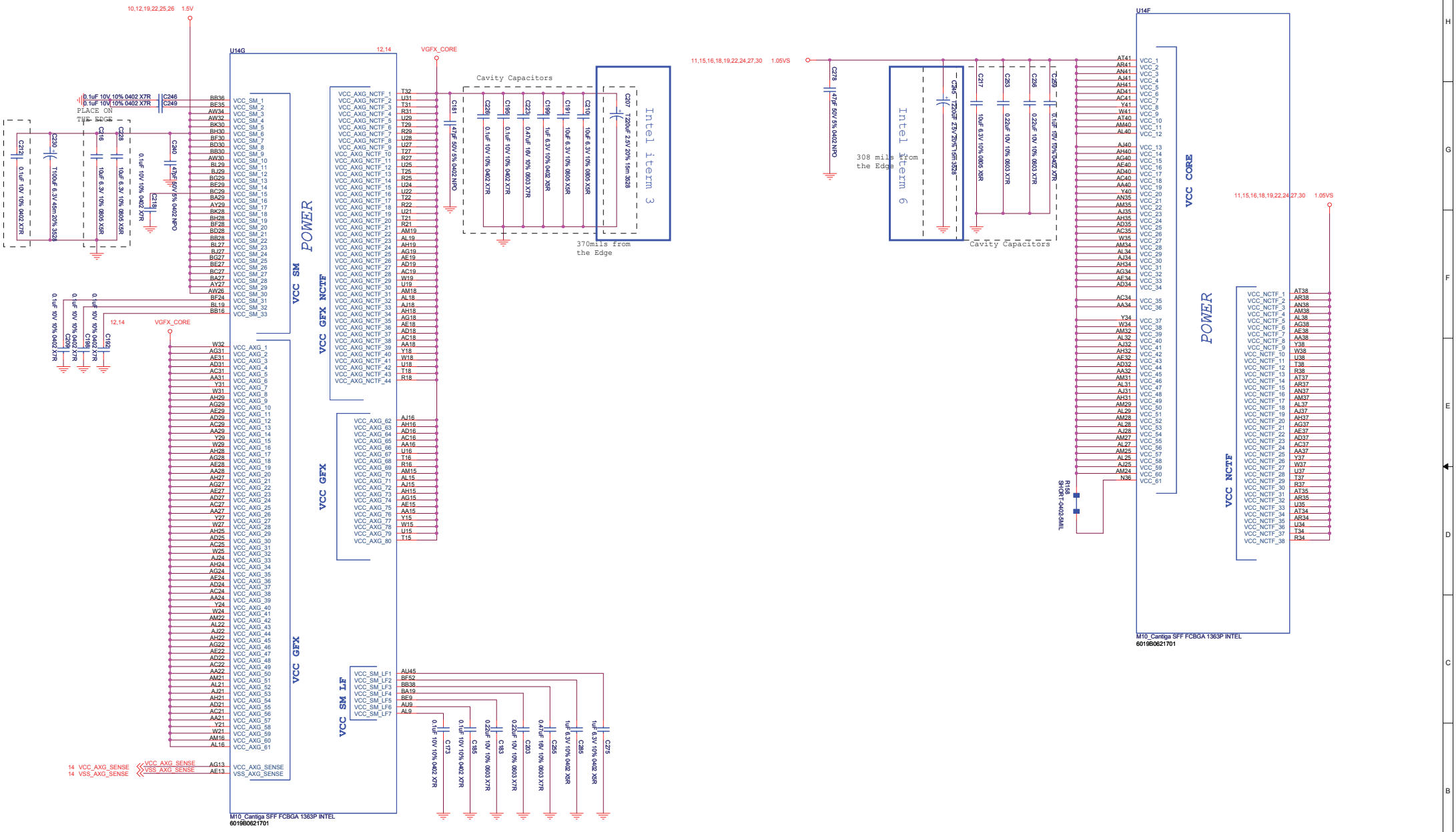


INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
Cantiga DDR3(3/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

CHANGE by: Milles Liu | DATE: Monday, May 04, 2009 | SHEET 20 of 36



INVENTEC				
TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF				
Cantiga Power(4/6)				
SIZE: Custom	CODE: CS	DOC.NUMBER: D-CS-1310A22752-0-ALG	REV: B	
CHANGE by: Milles Liu	DATE: Monday, May 04, 2009	SHEET: 21 of 36		

0.1uf caps in 1.5VDDM_xPLL need to be located as edge caps within 200mils

30mil

11,15,16,18,19,21,24,27,30 1.05VS

L9 100ohm 25% 2A 0.1ohm 0603 — (40mA) — 10mil — 1.05VS_DPLLA
C277 10uF 6.3V 10% 0805 X5R
C271 0.1uF 10V 10% 0402 X7R

L10 100ohm 25% 2A 0.1ohm 0603 — (40mA) — 10mil — 1.05VS_DPLLB
C288 10uF 6.3V 10% 0805 X5R
C289 0.1uF 10V 10% 0402 X7R

L2 100ohm 25% 2A 0.1ohm 0603 — (45mA) — 10mil — 1.05VS_HPLL
C177 4.7uF 6.3V 10% 0603 X5R
C169 0.1uF 10V 10% 0402 X7R

L28 100ohm 25% 2A 0.1ohm 0603 — (45mA) — 10mil — 1.05VS_MPLL
C441 10uF 6.3V 10% 0805 X5R
C439 0.1uF 10V 10% 0402 X7R

L7 100ohm 25% 2A 0.1ohm 0603 — 10mil — 1.05VS_PEGPLL
C283 10uF 6.3V 10% 0805 X5R
C282 0.1uF 10V 10% 0402 X7R

12,16,27,28,30,31,36 1.5VS
R124 100 1% 1/10W 0603 — (24mA) — 10mil — 1.5VS_TVDAC
C201 0.1uF 10V 10% 0402 X7R
C206 0.01uF 16V 10% 0402 X7R

Caps used in 1.5VDDM_TVDAC and 1.5VDDM_QTVDAC should be within 250mils of edge

180ohm 25% 1.5A 0603(FBM-11-160808-181A15T)
L6 — 10mil — 1.5VS_QDAC
C243 0.1uF 10V 10% 0402 X7R
C238 0.01uF 16V 10% 0402 X7R

3VS 10,11,12,13,14,15,17,19,24,25,26,27,28,29,30,31,32,33,34,35,36
R134 0-5%-1/10W-0603 — (120mA) — 10mil — VCCS_TVDACA
C224 0.1uF 10V 10% 0402 X7R
C231 0.01uF 16V 10% 0402 X7R

3VDDM_TVDAC should be within 250mils of edge

Vout
R1 Vout=Vref(1+R2/R1)+Iadj*R2
R2=R1(Vout/Vref-1)
FB 1117 Vref=1.250V,Iadj=55uA
R2
GND

180ohm 25% 1.5A 0603(FBM-11-160808-181A15T)
3VS L5 — 20mil
C219 0.01uF 16V 10% 0402 X7R
C229 0.1uF 10V 10% 0402 X7R
20mil
C244 0.01uF 16V 10% 0402 X7R
C239 0.1uF 10V 10% 0402 X7R

10,11,12,13,14,15,17,19,24,25,26,27,28,29,30,31,32,33,34,35,36

U14H

CRT: VCCA_CRT_DAC J31; VCCA_DAC_BG L31; VSSA_DAC_BG M33
PLL: 1.05VS_DPLLA J45 VCCA_DPLLA; 1.05VS_DPLLB L49 VCCA_DPLLB; 1.05VS_HPLL AF10 VCCA_HPLL; 1.05VS_MPLL AE1 VCCA_MPLL
LVDS: 1.8V_TXLVDS U43 VCCA_LVDS1; U41 VCCA_LVDS2; V44 VSSA_LVDS
C260 1000pF 50V 10% 0402 X7R
C262 0.1uF 10V 10% 0402 X7R
12,16,27,28,30,31,36 1.5VS AJ43 VCCA_PEG_BG
PEG: 1.05VS_PEGPLL AG43 VCCA_PEG_PLL
POWER
11,15,16,18,19,21,24,27,30 1.05VS
C197 10uF 6.3V 10% 0805 X5R
C198 4.7uF 6.3V 10% 0603 X5R
C205 10uF 6.3V 10% 0805 X5R
C196 1uF 6.3V 10% 0402 X5R
SM: VCCA_SM_1 AW24; VCCA_SM_2 AU24; VCCA_SM_3 AW22; VCCA_SM_4 AU22; VCCA_SM_5 AU21; VCCA_SM_6 AW20; VCCA_SM_7 AU19; VCCA_SM_8 AW18; VCCA_SM_9 AU18; VCCA_SM_10 AW16; VCCA_SM_11 AU16; VCCA_SM_12 AT16; VCCA_SM_13 AR16; VCCA_SM_14 AU15; VCCA_SM_15 AT15; VCCA_SM_16 AR15; VCCA_SM_17 AW14
SM: VCCA_SM_NCTF_1 AT24; VCCA_SM_NCTF_2 AR24; VCCA_SM_NCTF_3 AT22; VCCA_SM_NCTF_4 AR22; VCCA_SM_NCTF_5 AT21; VCCA_SM_NCTF_6 AR21; VCCA_SM_NCTF_7 AT19; VCCA_SM_NCTF_8 AR19; VCCA_SM_NCTF_9 AT18; VCCA_SM_NCTF_10 AR18

11,15,16,18,19,21,24,27,30 1.05VS
C222 10uF 6.3V 10% 0805 X5R
C227 4.7uF 6.3V 10% 0603 X5R
C215 0.1uF 10V 10% 0402 X7R
SM: VCCA_SM_CK_4 AU27; VCCA_SM_CK_3 AU28; VCCA_SM_CK_2 AU29; VCCA_SM_CK_1 AU31
SM: VCCA_SM_CK_NCTF_1 AT31; VCCA_SM_CK_NCTF_2 AR31; VCCA_SM_CK_NCTF_3 AT29; VCCA_SM_CK_NCTF_4 AR29; VCCA_SM_CK_NCTF_5 AT28; VCCA_SM_CK_NCTF_6 AR28; VCCA_SM_CK_NCTF_7 AT27; VCCA_SM_CK_NCTF_8 AR27

11,15,16,18,19,21,24,27,30 1.05VS
0.1uF 10V 10% 0402 X7R
C258
1.05VS_PEGPLL
0.1uF 10V 10% 0402 X7R
C261
VCCD_HPLL AH12; VCCD_PEG_PLL AE43; VCCD_LVDS_1 M46; VCCD_LVDS_2 L45

11 1.8V
C274 1uF 6.3V 10% 0402 X5R

M10_Cantiga SFF FCBGA 1363P INTEL
6019B0621701

3VS 10,11,12,13,14,15,17,19,24,25,26,27,28,29,30,31,32,33,34,35,36
R360 10-5%-1/10W-0603
D23 1SS355PT 90V 0.5A
1.05VS 11,15,16,18,19,21,24,27,30
R361 SHORT-0402-15MIL
20mil
C456 0.1uF 10V 10% 0402 X7R
3VS_HV

11,15,16,18,19,21,24,27,30 1.05VS
C444 4.7uF 6.3V 10% 0603 X5R
C443 4.7uF 6.3V 10% 0603 X5R
C442 2.2uF 6.3V 20% X5R 0603
C440 0.47uF 16V 10% 0603 X7R
PLACE ON THE EDGE
C158 100uF 6.3V 45m 20% 3528_NU

VTT: VTT_1 R13; VTT_2 T12; VTT_3 R11; VTT_4 T10; VTT_5 R9; VTT_6 T8; VTT_7 R7; VTT_8 T6; VTT_9 R5; VTT_10 T4; VTT_11 R3; VTT_12 T2; VTT_13 R1

TV: VCCA_TV_DAC K30 — 10mil — VCCS_TVDACA

HDA: VCC_HDA A31 — 1.5VS 12,16,27,28,30,31,36
0.1uF 10V 10% 0402 X7R
C454

TV/CRT: VCCD_QDAC N34 — 1.5VS_QDAC; VCCD_TVDAC N32 — 1.5VS_TVDAC

AXF: VCC_AXF_1 M25; VCC_AXF_2 N24; VCC_AXF_3 M23
30mil
1uF 6.3V 10% 0402 X5R
C211
C202 10uF 6.3V 10% 0805 X5R_NU
1.05VS 11,15,16,18,19,21,24,27,30

SM CK: VCC_SM_CK_1 BK24; VCC_SM_CK_2 BL23; VCC_SM_CK_3 BL22; VCC_SM_CK_4 BK22
30mil
0.1uF 10V 10% 0402 X7R
C204
C200 10uF 6.3V 10% 0805 X5R
L3 100ohm 25% 2A 0.1ohm 0603
1.5V 10,12,19,21,25,26

HV: VCC_TX_LVDS T41; VCC_HV_1 C33; VCC_HV_2 A33
1000pF 50V 10% 0402 X7R
1.8V_TXLVDS
L8 120ohm 25% 200mA 0603(BLM11A121S)
1.8V 11
10mil
C256
C252 22uF 6.3V 20% 0805 X5R_NU
3VS_HV

PEG: VCC_PEG_1 AB44; VCC_PEG_2 Y44; VCC_PEG_3 AC43; VCC_PEG_4 AA43
30mil
10uF 6.3V 10% 0805 X5R
C281
C279 T100uF 6.3V 45m 20% 3528_NU
1.05VS 11,15,16,18,19,21,24,27,30

DMI: VCC_DMI_1 AM44; VCC_DMI_2 AN43; VCC_DMI_3 AL43
20mil
C276
C280 0.1uF 10V 10% 0402 X7R

VTTLF: VTTLF1 K14; VTTLF2 Y12; VTTLF3 P2
VTTLF_CAP1
VTTLF_CAP2
VTTLF_CAP3
C175 0.47uF 16V 10% 0603 X7R
C188 0.47uF 16V 10% 0603 X7R
C189 0.47uF 16V 10% 0603 X7R
10uF 6.3V 10% 0805 X5R

CHANGE by	Milles Liu	DATE	Monday, May 04, 2009

INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
Cantiga Power(5/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

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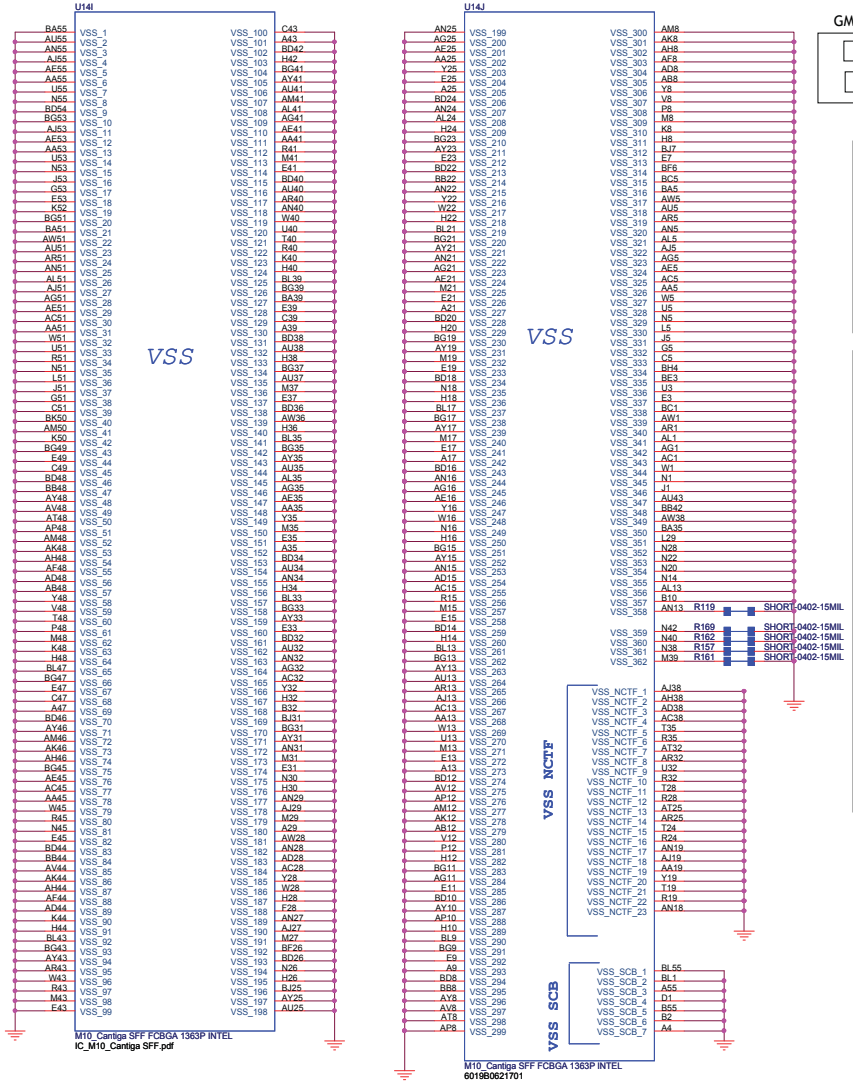
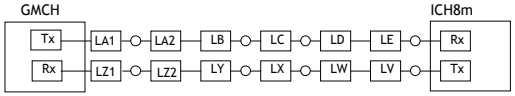


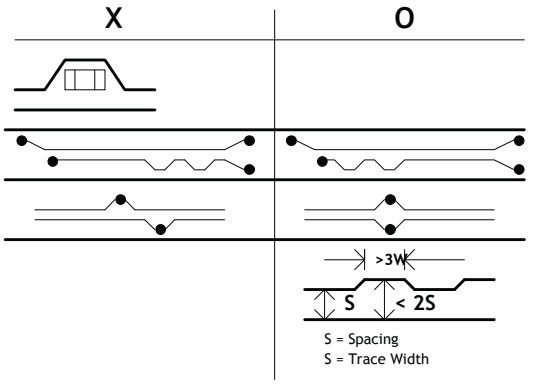
DMI Routing Guideline



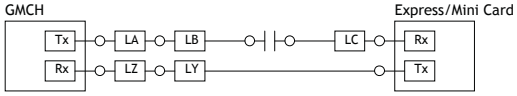
Breakout/in LA/LZ	Main Route LB/LY		Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Didderential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 250 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



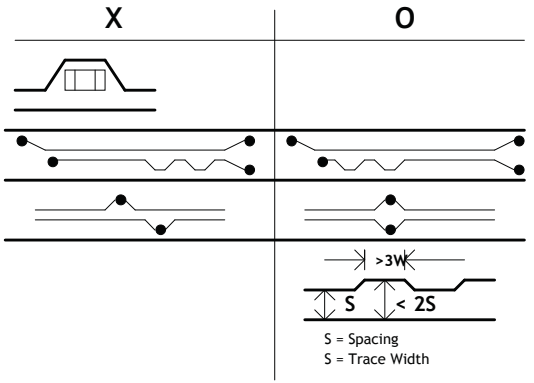
PCIE Routing Guideline



Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



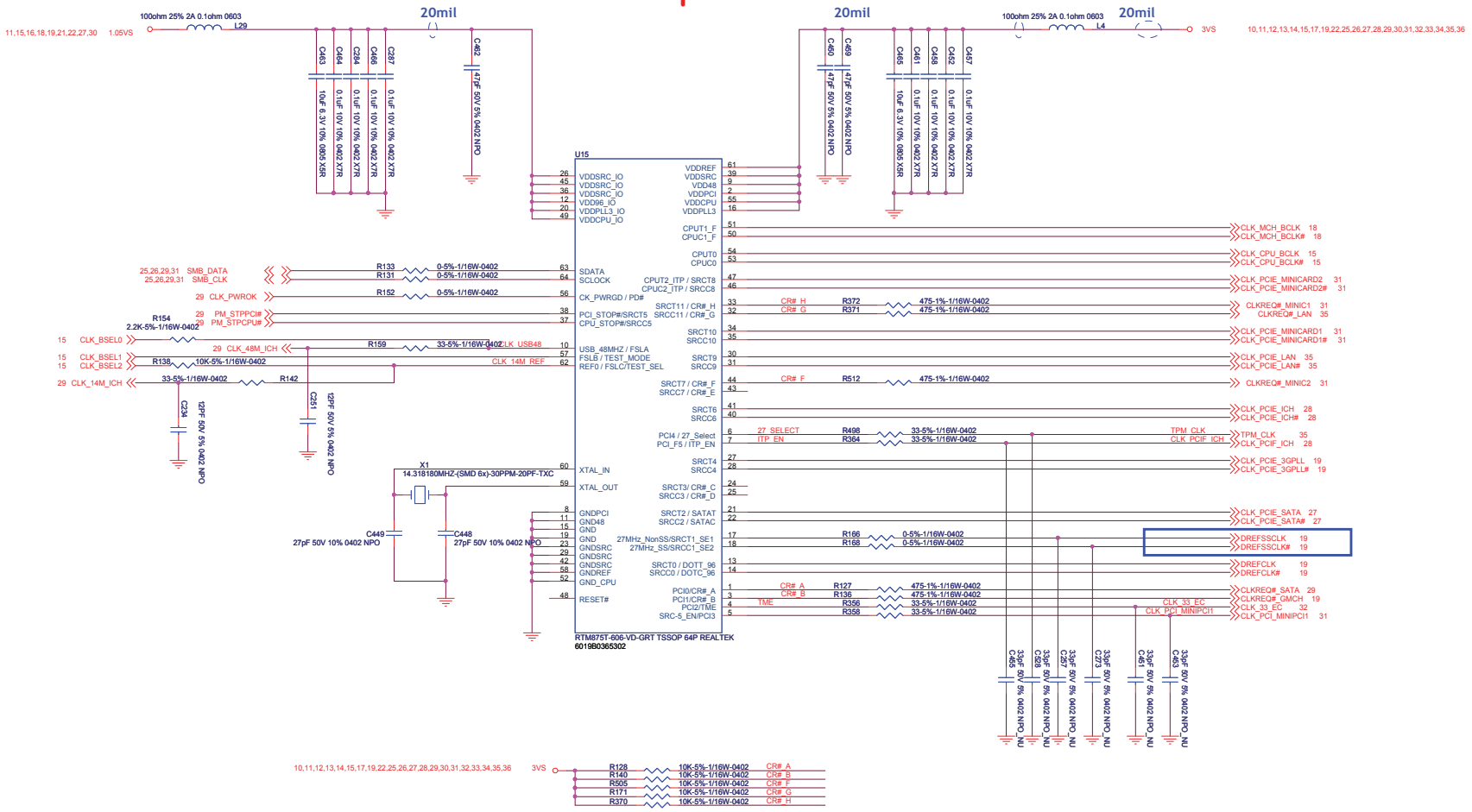
INVENTEC

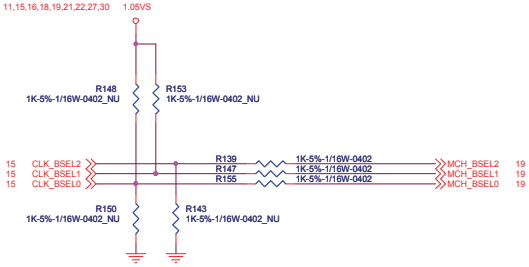
TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
Cantiga Ground(6/6)

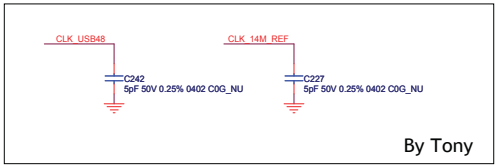
SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

SHEET 23 of 36

CHANGE by Miles Liu | DATE Monday, May 04, 2009

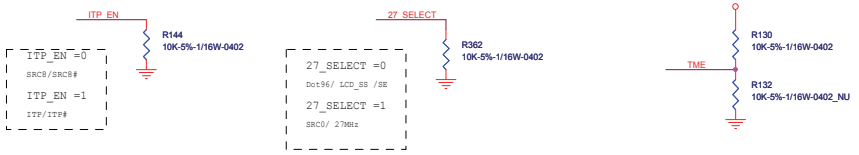






CR#_A:	Byte 5 bit 6=0--->SRC0 bit 6=1--->SRC2	BIT 7=1 (Enable)
CR#_C:	Byte 5 bit 2=0--->SRC0 bit 2=1--->SRC2	BIT 3=1 (Enable)
CR#_B:	Byte 5 bit 4=0--->SRC1 bit 4=1--->SRC4	BIT 5=1 (Enable)
CR#_D:	Byte 5 bit 0=0--->SRC1 bit 0=1--->SRC4	BIT 1=1 (Enable)
CR#_E:	SRC6 (Byte 6)	BIT 7=1 (Enable)
CR#_F:	SRC8 (Byte 6)	BIT 6=1 (Enable)
CR#_G:	SRC9 (Byte 6)	BIT 5=1 (Enable)
CR#_H:	SRC10 (Byte 6)	BIT 4=1 (Enable)

FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200
0	0	0	1067	266 *



CHANGE by	Miles Liu	DATE	Monday, May 04, 2009

INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
Clock Generator

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

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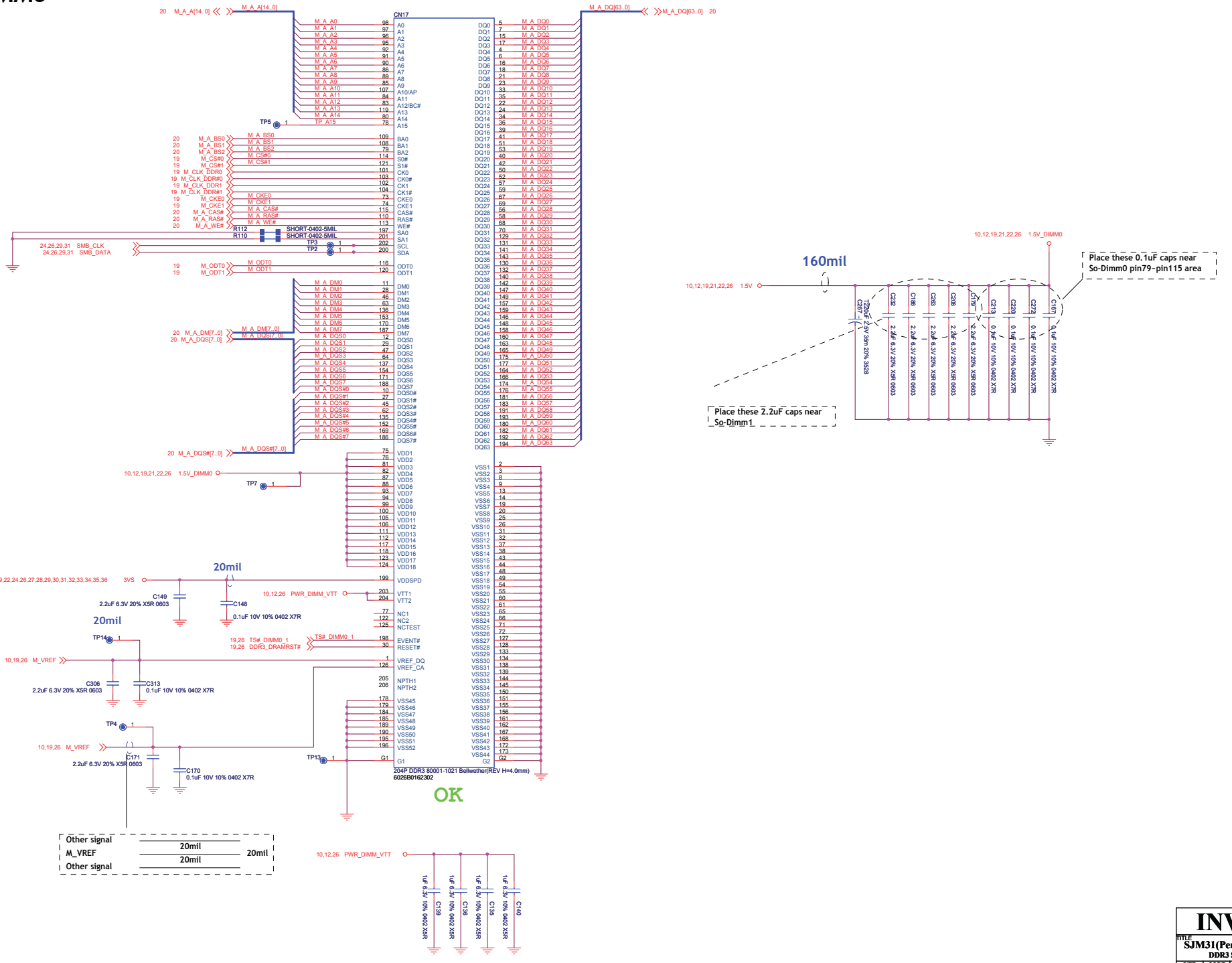
SO-DIMM0



CHANGE by	Miles Liu	DATE	Monday, May 04, 2009

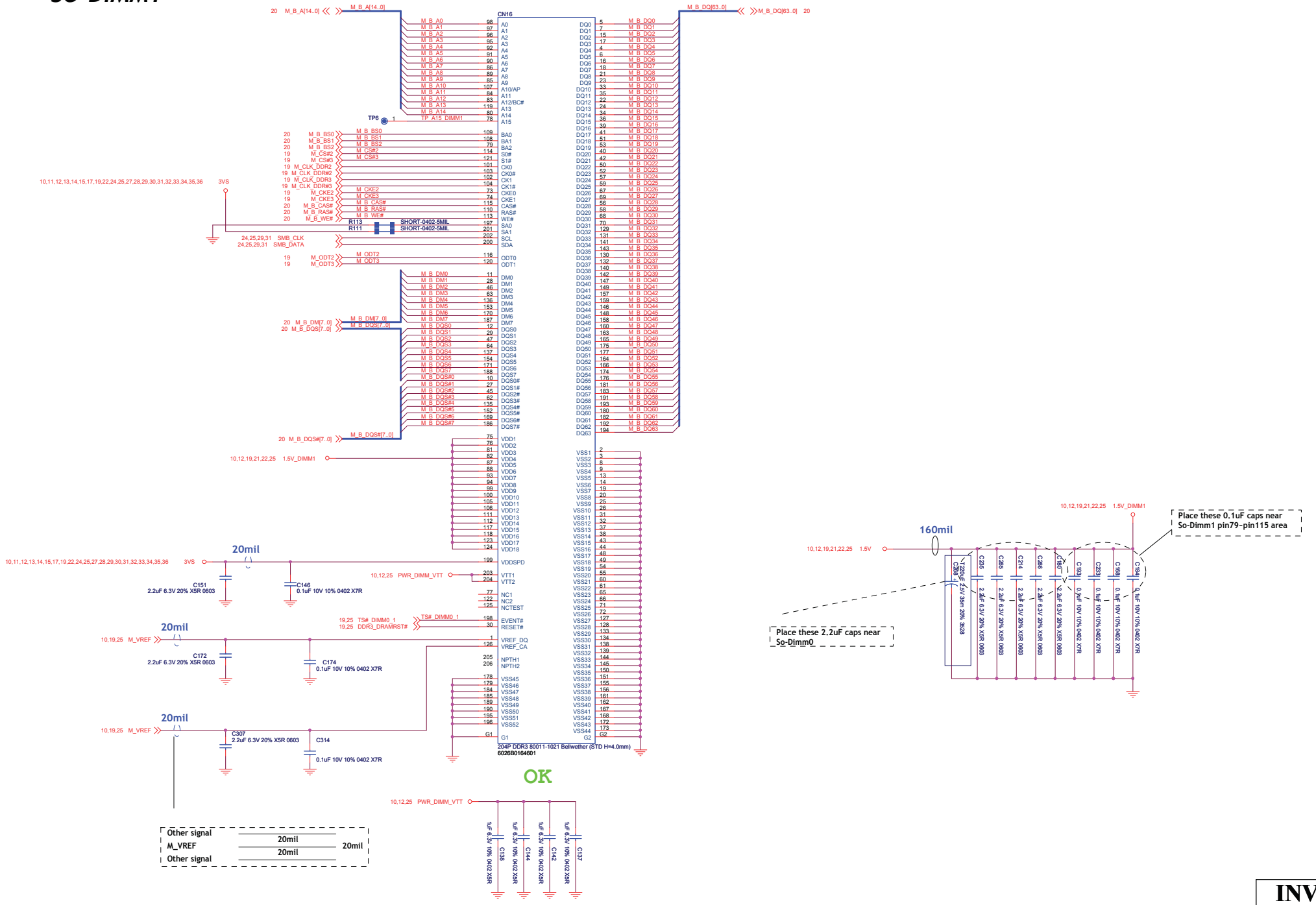
INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
DDR3 SDRAM SO-DIMM0

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

SHEET 25 of 36

SO-DIMM1



INVENTEC			
TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF DDR3 SDRAM SO-DIMM1			
SIZE: Custom	CODE: CS	DOC.NUMBER: D-CS-1310A22752-0-ALG	REV: B
CHANGE by: Miles Liu	DATE: Monday, May 04, 2009	SHEET: 26 of 36	

RTC Circuit

1. RC delay time should be in the range of 18~25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

1. The ICH7m requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended

For JM31,SJM31 For BAP31

For Green PC

BATT1

123

CABLE,ROUND,3POS,75mm,I,RTC_NU

6027B0066801

RTC Battery Life :

220mAh(220000uAh) / 6uA = 4.2 year

Place all series resistors 0.6 to 2.6 inches from the ICH9

Needs to be placed within 2" of ICH9m

Must be placed within 2" of 24.9 ohm w/o stub

Distance between the ICH9-M and cap on the "P" signal should be identical distance between the ICH9-M and cap on the "N" signal for same pair.

Placed within 500mils of ICH9m ball

ICH8m internal VR enable strap

	Enable	Disable
INTVRMEN	1(Default)	0

Internal VRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05

Short pins AG1 and AG2 at the package

ACZ_SDATAOUT strap functionality base on RSVD9 strap

XOR chain entrance (RSVD9 pulled low)

PCIE port config bit 1(RSVD9 not pulled low)

Stuff for XOR chain testing

XOR Chain Entrance Strap - to be updated		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

By Tony

CHANGE by	Miles Liu	DATE	Monday, May 04, 2009

INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF

ICH9M CPU/IDE/SATA(1/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

SHEET 27 of 36

PCIE AC coupling caps need to be within 250mils of the driver

WLAN
3G
LAN

U18D

PCI-Express
Direct Media Interface
SPI
USB

M10_ICH9M_SFF FCBGA 569P INTEL
6019B0621801

STUFF for iTPM enable

R194 1K-5%-1/16W-0402_NU

R206 24.9-1%-1/16W-0402

10mil

Place within 500mils of ICH

Place within 500mils of ICH
5/5 mils spacing on microstrip

U16
W25X32VSSIG SOIC 8P Winbon_NU
6019B0499501_NU

By Tony

U18B

PCI

Interrupt I/F

M10_ICH9M_SFF FCBGA 569P INTEL
6019B0621801

PCI Pull up

Buffer to reduce loading on PLT_RST#

PCI_GNT#3	No stuff : by default Stuff : For A16 swap override

PCI_GNT#0	SPI_CS1#	
1	1	LPC
1	0	PCI
0	1	SPI

Check BIOS type

INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
ICH9M PCI/PCIE/DMI/USB(2/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

CHANGE by: Milles Liu | DATE: Monday, May 04, 2009 | SHEET 28 of 36

SUSCLK duty cycle can be between 30% and 70%

RSMRST# should go high no sooner than 10ms after both Vccsus3_3 and Vccsus1_5 have reached their nominal voltage

Rise edge : 1~2us
ICH9m Spec : less 50us

ICH9m strap

ACZ_SPKR	No stuff : by default Stuff : For NO reboot

Default is OPEN
Add 0ohm for BIOS Recovery

PMU P/U

BIOS ID setting

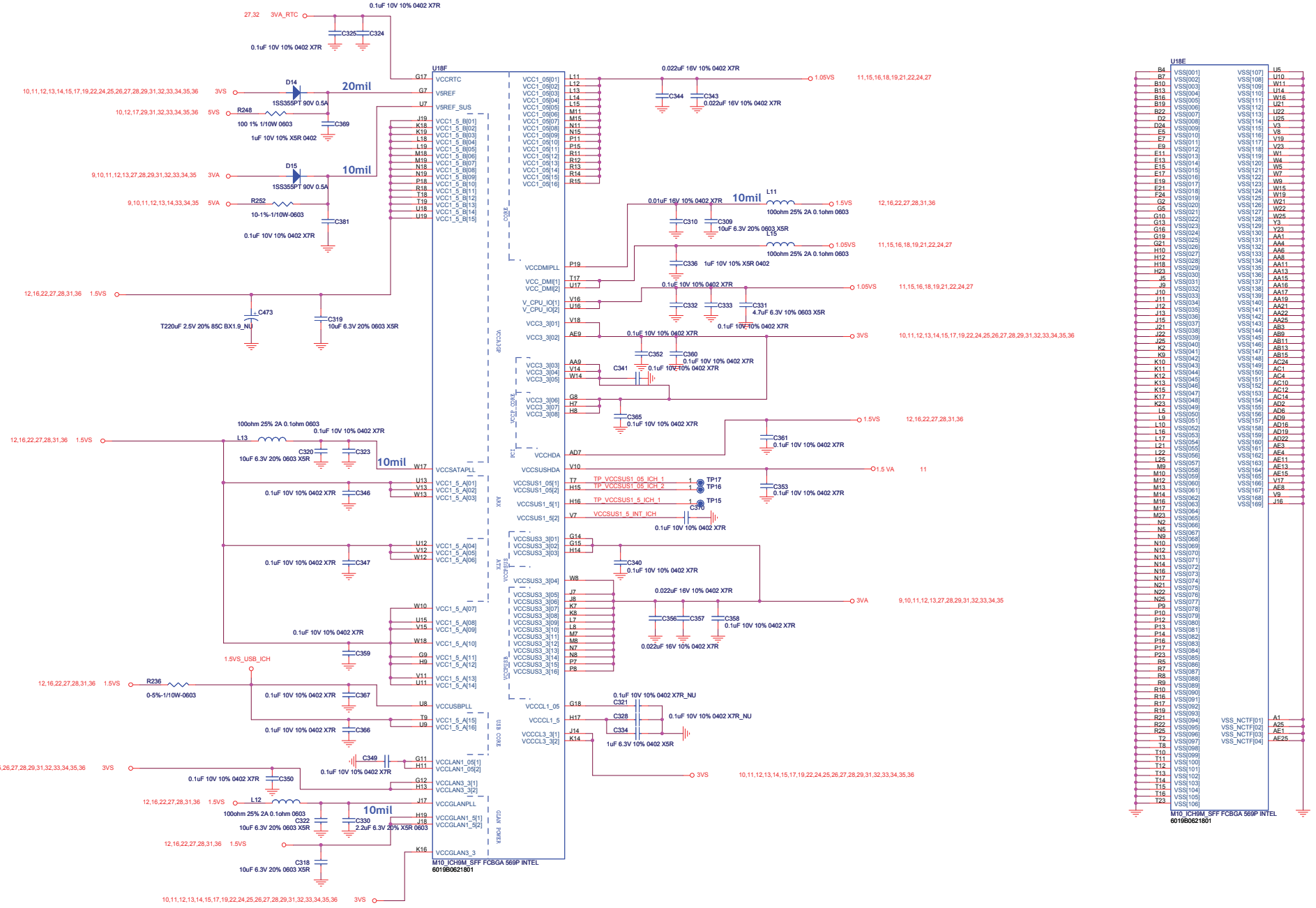
Project	MB_ID3 GPIO 39	MB_ID2 GPIO 1	MB_ID1 GPIO 7	MB_ID0 GPIO 17
JM31 (UMA)	1	1	1	1
SJM31 (UMA)	1	1	1	0
BAP31 (UMA)	1	1	0	1
	1	1	0	0
	1	0	1	1
	1	0	1	0
	1	0	0	1
	1	0	0	0
	0	1	1	1
	0	1	1	0
	0	1	0	1
	0	1	0	0
	0	0	1	1
	0	0	1	0
	0	0	0	1
	0	0	0	0

INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
ICH9M GPIO(3/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B
		SHEET 29 of 36	

CHANGE by: Miles Liu | DATE: Monday, May 04, 2009



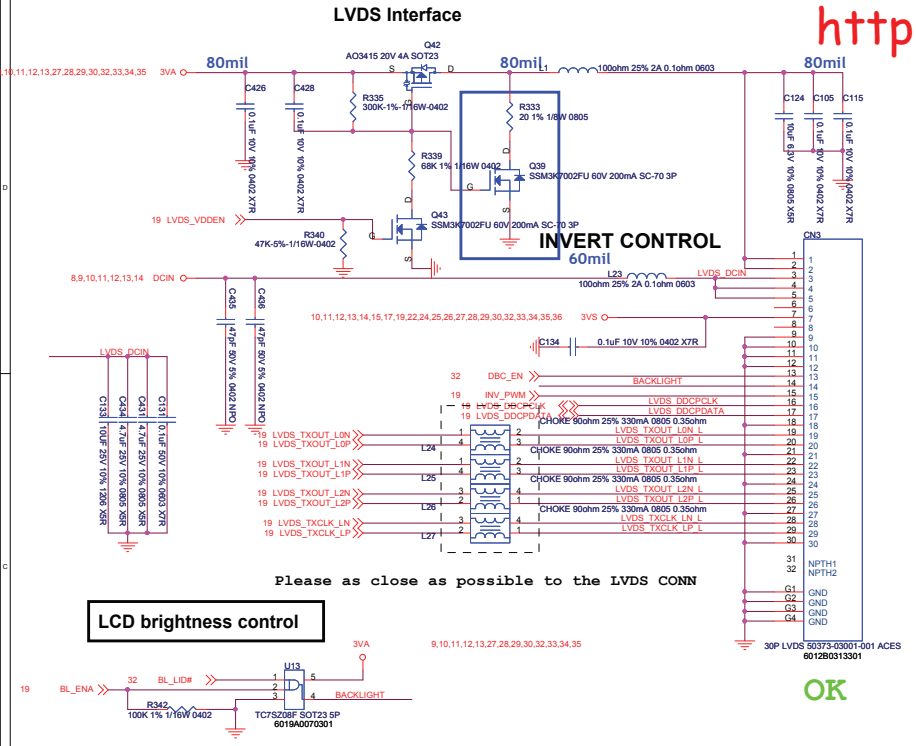
CHANGE by	Miles Liu	DATE	Monday, May 04, 2009

INVENTEC

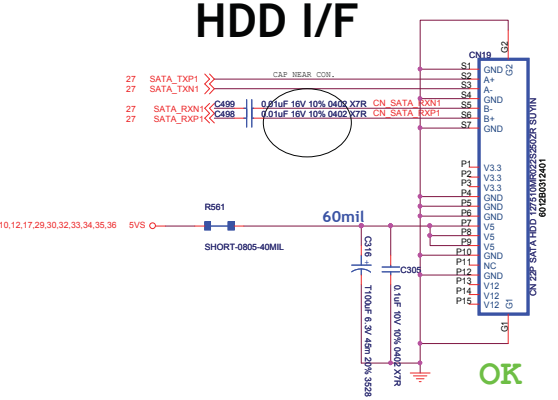
TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
ICH9M Power/GND(4/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B
		SHEET 30 of 36	

LVDS Interface

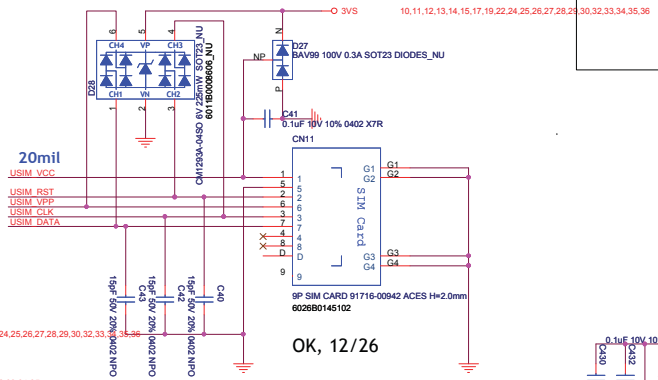


HDD I/F

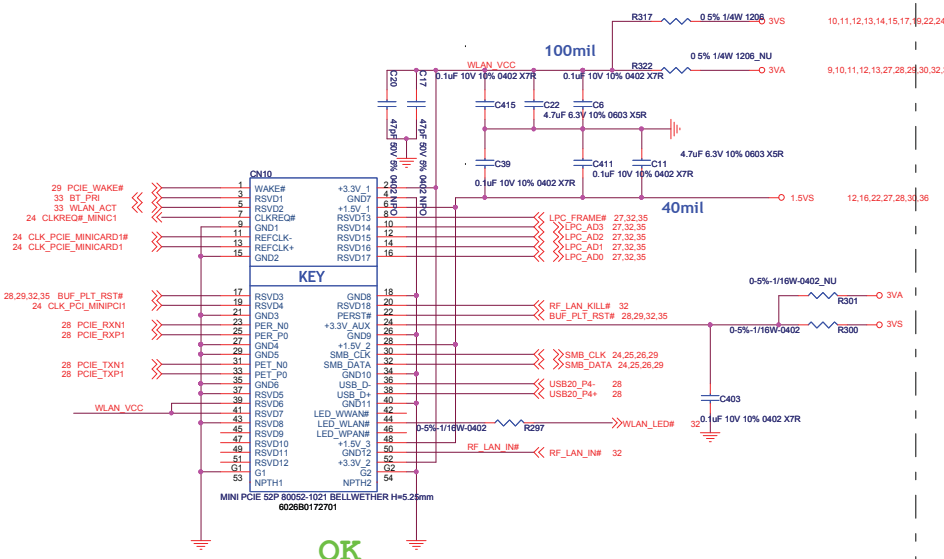


SIM CARD slot

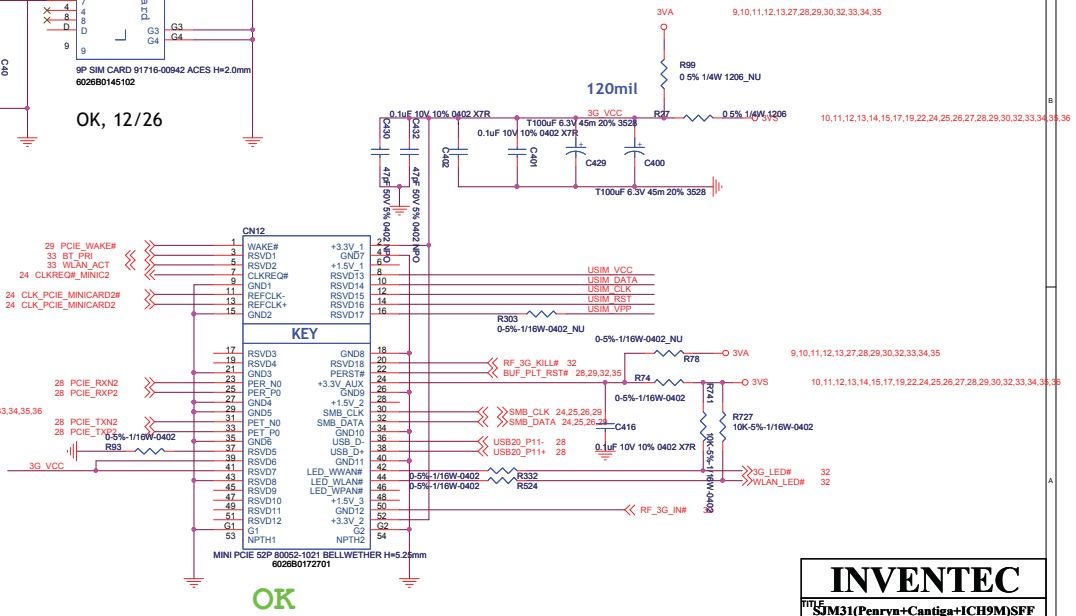
On Chip 5V to 3.3V regulator. No external regulator required
On-Chip power MOSFETs for supplying flash media card power.



PCIE Mini Card(WLAN)



PCIE Mini Card for 3G



CHANGE by	Miles Liu	DATE	Monday, May 04, 2009

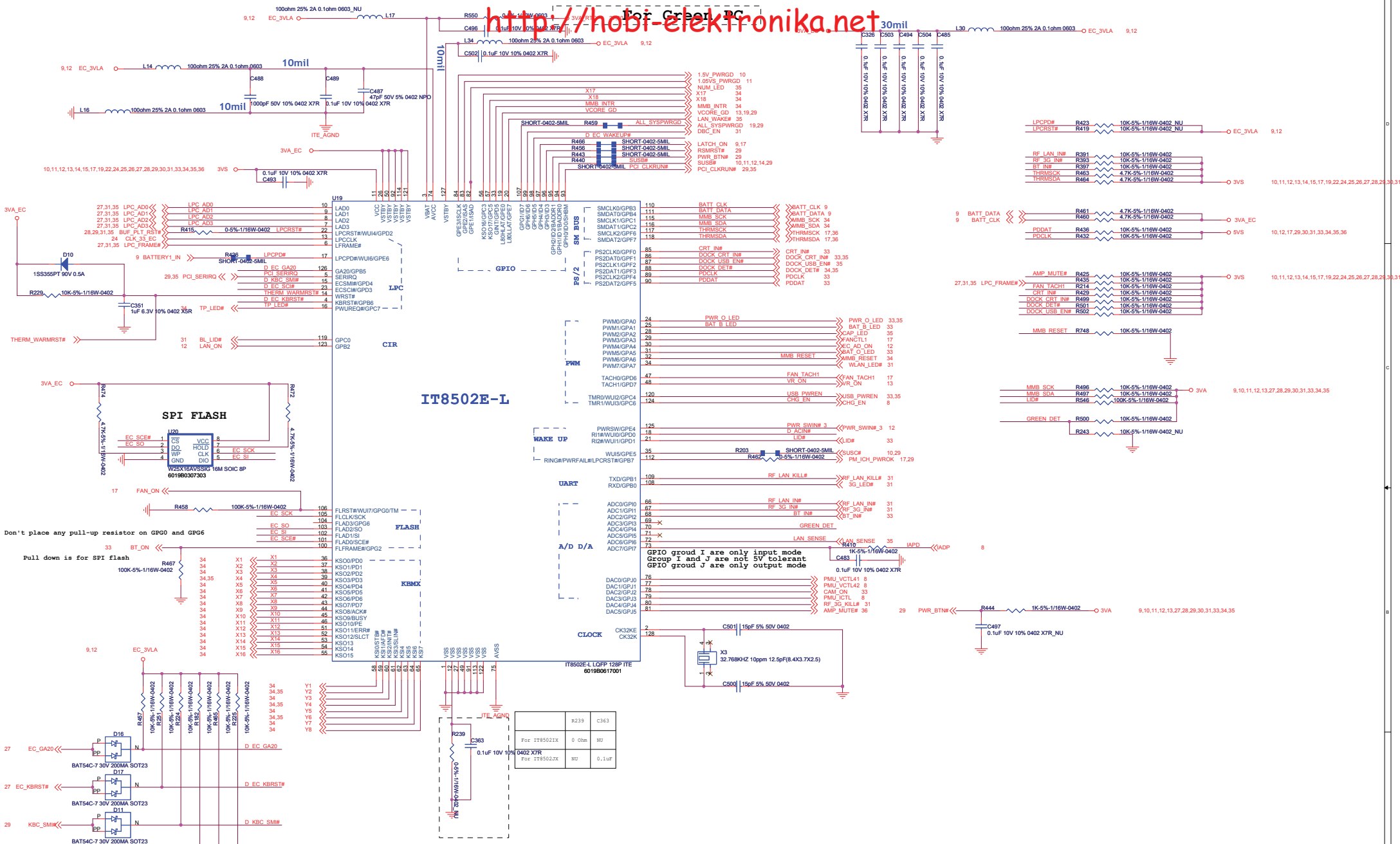
INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
LCD CNN & WLAN & 3G

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

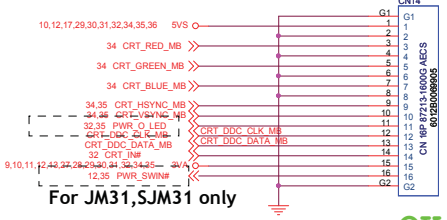
SHEET 31 of 36

for Green PC



VGA Board CN

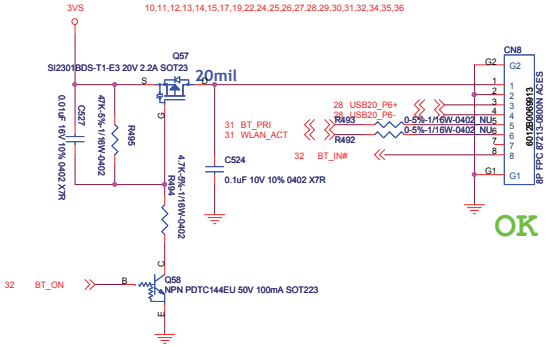
(CRT+ PWR SW)



For JM31,SJM31 only

OK

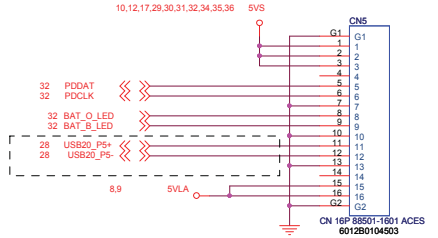
Bluetooth CON.



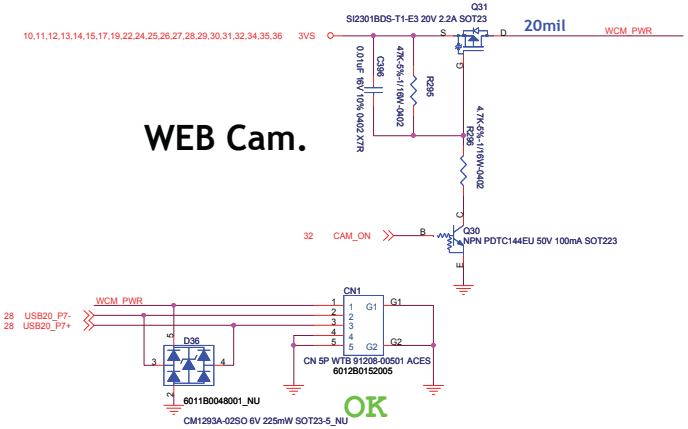
OK

GLIDE PAD Board

For BAP31 only



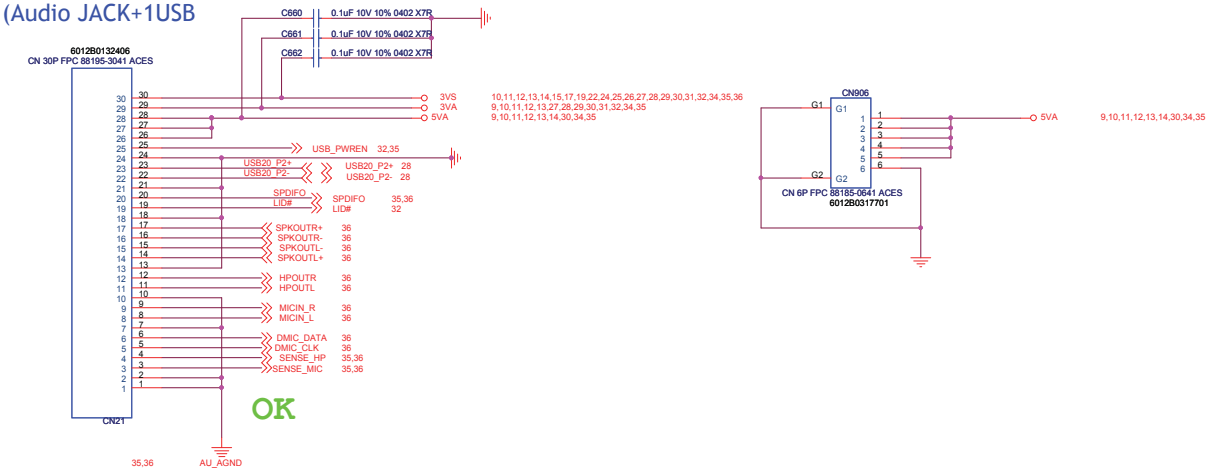
WEB Cam.



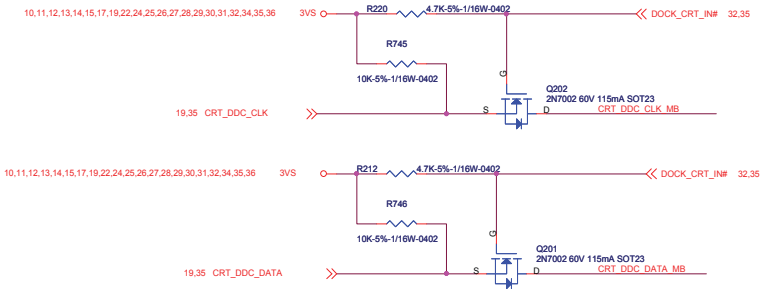
OK

AUDIO Board CN

(Audio JACK+1USB

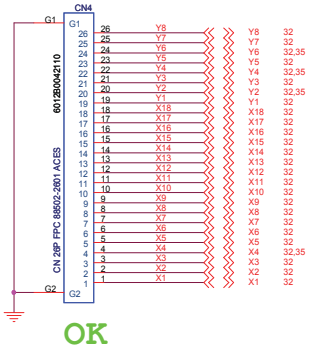


OK

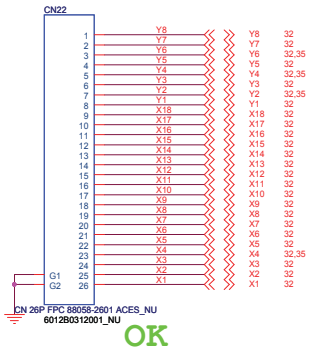


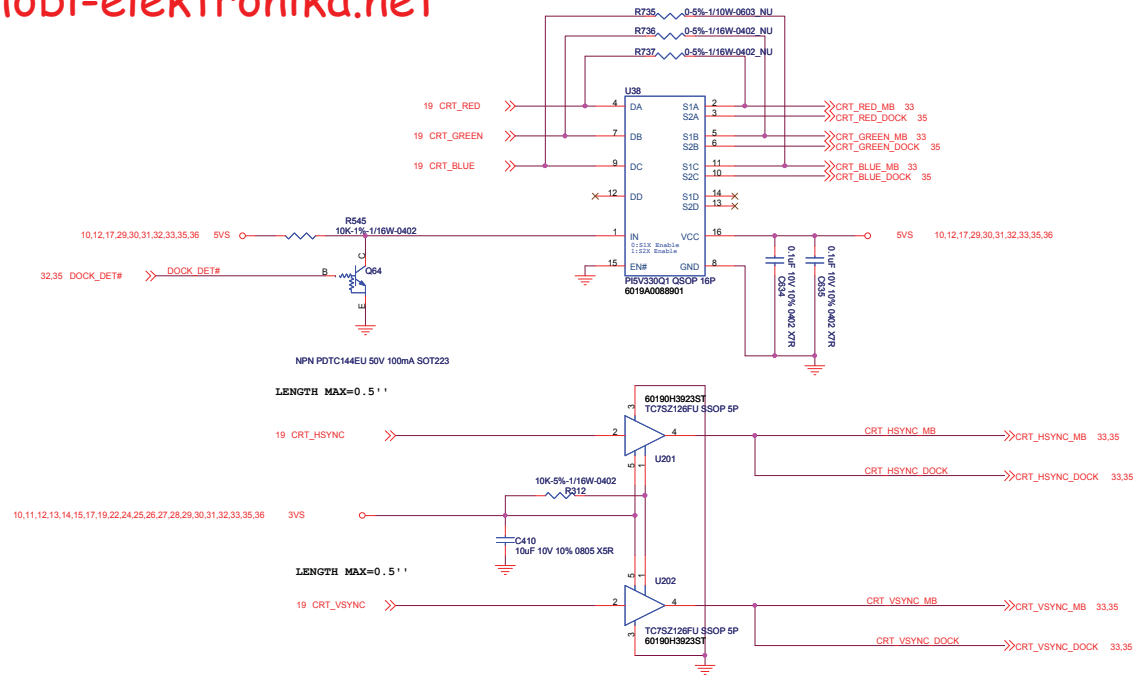
INVENTEC			
TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF Daughter Connector			
SIZE: Custom	CODE: CS	DOC NUMBER: D-CS-1310A22752-0-ALG	REV: B
CHANGE by: Miles Liu	DATE: Monday, May 04, 2009	SHEET: 33 of 36	

To K/B(For JM31,BAP31)



To K/B (For SJM31)



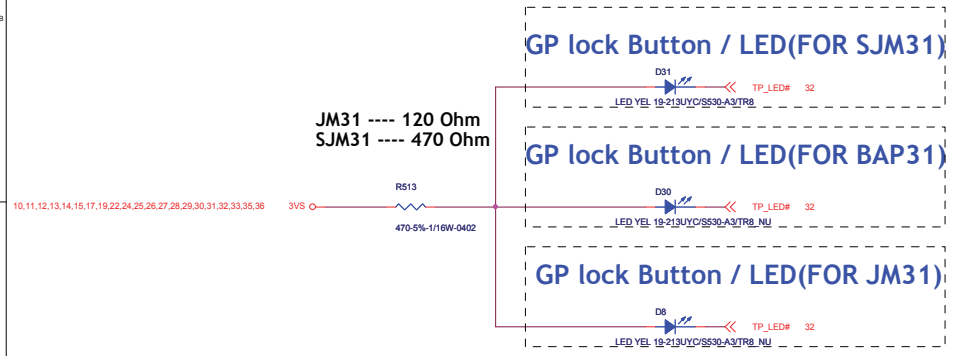


GP lock Button / LED(FOR SJM31)

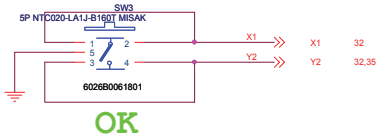
GP lock Button / LED(FOR BAP31)

GP lock Button / LED(FOR JM31)

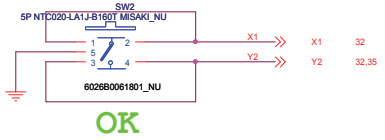
JM31 ---- 120 Ohm
SJM31 ---- 470 Ohm



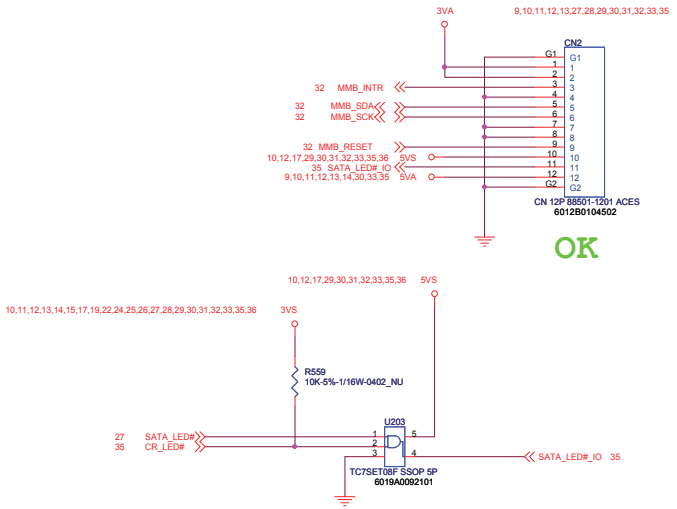
SW (FOR SJM31)



SW (FOR JM31,BAP31)



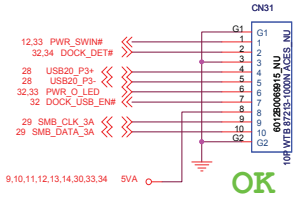
SW Sensor BOARD(For JM31,SJM31)



INVENTEC			
TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF BDP			
SIZE: Custom	CODE: CS	DOC NUMBER: D-CS-1310A22752-0-ALG	REV: B
CHANGE by: Milles Liu	DATE: Monday, May 04, 2009	SHEET: 34 of 36	

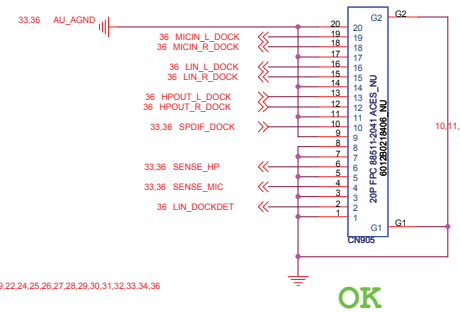
For BAP31(EASY/B)

MB(USB) TO EASY/B



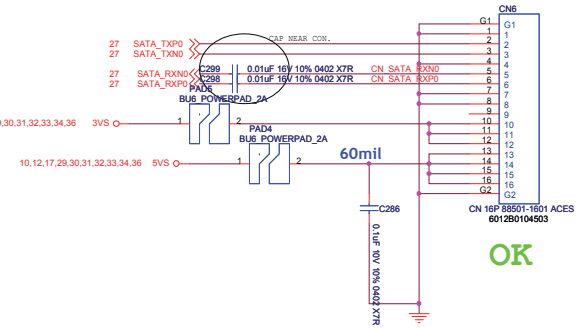
OK

MB(AUDIO) TO EASY/B(For BAP31)



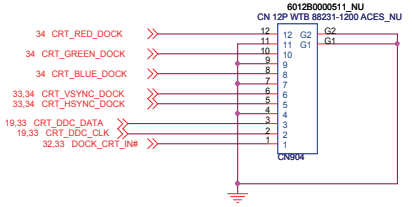
OK

SSD I/F

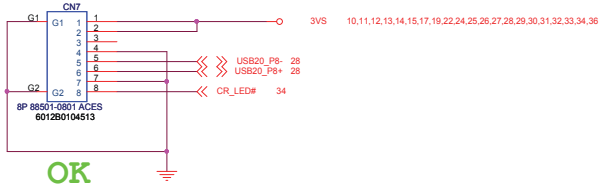


OK

MB(RGB) TO EASY/B

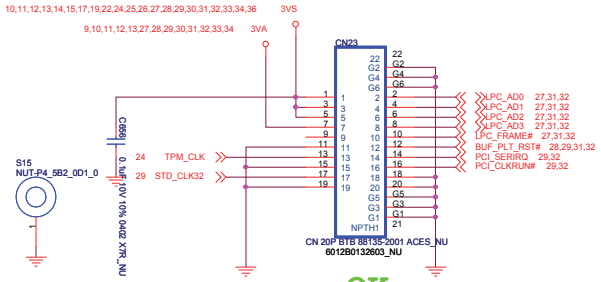


Card Reader BOARD CN



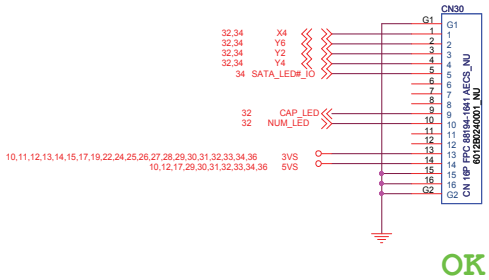
OK

TPM CN



OK

SW/B CN



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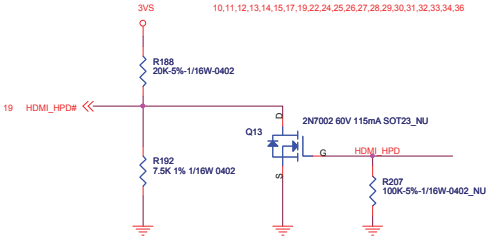
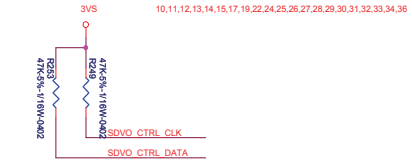
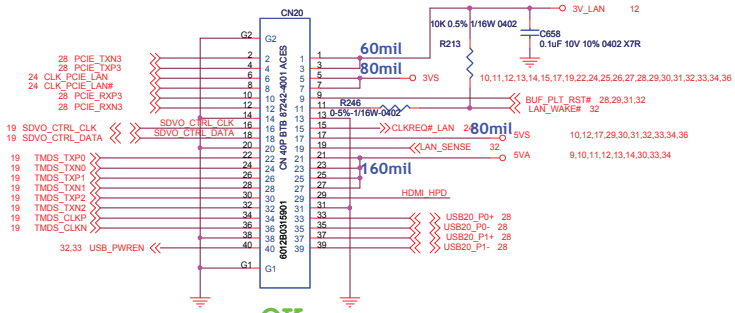




USB Board CN

(LAN+HDMI+2USB)



OK

CHANGE by	Milles Liu	DATE	Monday, May 04, 2009

INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF BDP

SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

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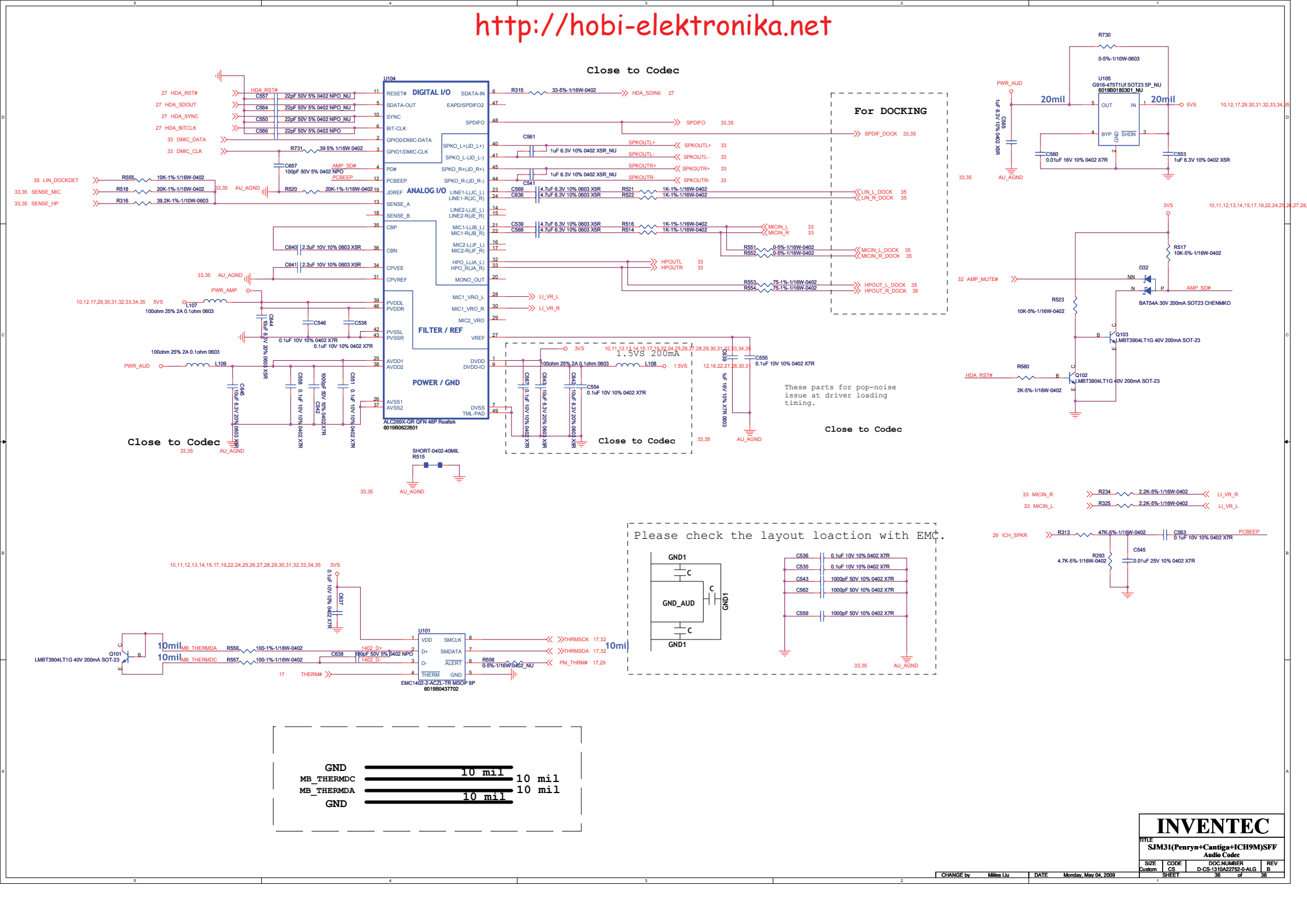

CHANGE by	Milles Liu	DATE	Monday, May 04, 2009

INVENTEC

TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF
Audio Codec

SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

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