JV71-MV DDR3 Madison Block Diagram

Project code: 91.4FX01.001
PCB P/N : 48.4FX01.01M
REVISION : 09924 -1

PCB STACKUP

TOP		L1
GND		L2
S		L3
S		L4
GND		L5
BOTTOM		L6

CLK GEN. ICS9LPRS365B 3

Mobile CPU Penryn 4, 5

SMSC EMC2102 34

HOST BUS 667/800/1066MHz@1.05V

VRAM 64MbX16X8 1024M

DDR3 1066 MHz 16,17

DDR3 1066 MHz 16,17

Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
6,7,8,9,10,11

PCIex16

VGA Madison / M96 52~57

HDMI 20

LCD 18

CRT 19

X4 DMI 400MHz

C-Link0

ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
4 SATA
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
12,13,14,15

USB

CardBus RTS5159 31

MS/MS Pro/xD /MMC/SD

LAN Giga LAN BCM5784 25

TXFM 26

RJ45 26

PCIe

Mini 1 Card Wire LAN 33

LPC BUS

LINE IN 29

Int MIC 18

MIC In 29

INT.SPKR 1.5W 29

LINE OUT 29

AZALIA

Codec ALC888S 27

OP AMP MAX9789A 30

MODEM MDC Card 30

RJ11

SATA

HDD SATA 21

SATA

ODD SATA 22

Mini USB Blue Tooth 23

Finger Printer 37

USB

Camera

USB 4 Port 24

KBC Winbond WPCE773 35

SPI

BIOS (2MB) 36

MEDIA KEY 38

Touch Pad 37

INT. KB 35

LPC DEBUG CONN. 36

SYSTEM DC/DC ISL62392 42

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC TPS51124 43

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9A) 1D5V_S3(12A)

RT9026 44

1D5V_S3	DDR_VREF_S3 (1.2A)

RT9018 44

1D5V_S3	1D1V_S0(2A)

TPS51117 45

DCBATOUT	FBVDD(4A)

CHARGER ISL88731A 47

INPUTS	OUTPUTS
DCBATOUT	BT+

CPU DC/DC ISL6266A 41

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 38A

VGA_CORE RT8202A 47

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 13A

GFXCORE ISL6263A 46

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (7A)

JV71-MV DDR3 Madison

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Title: BLOCK DIAGRAM

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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

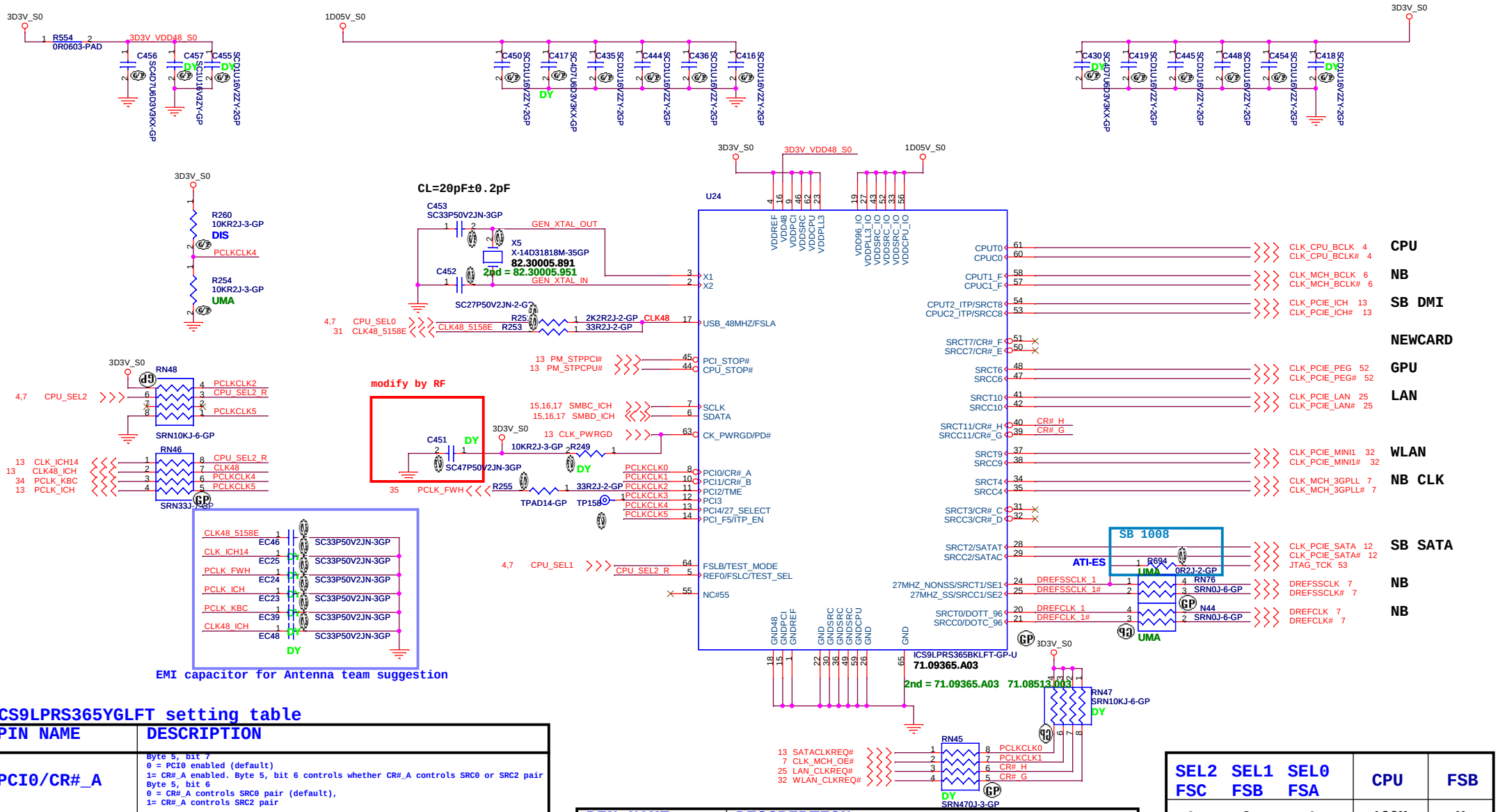
ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.



ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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Title: Clock Generator

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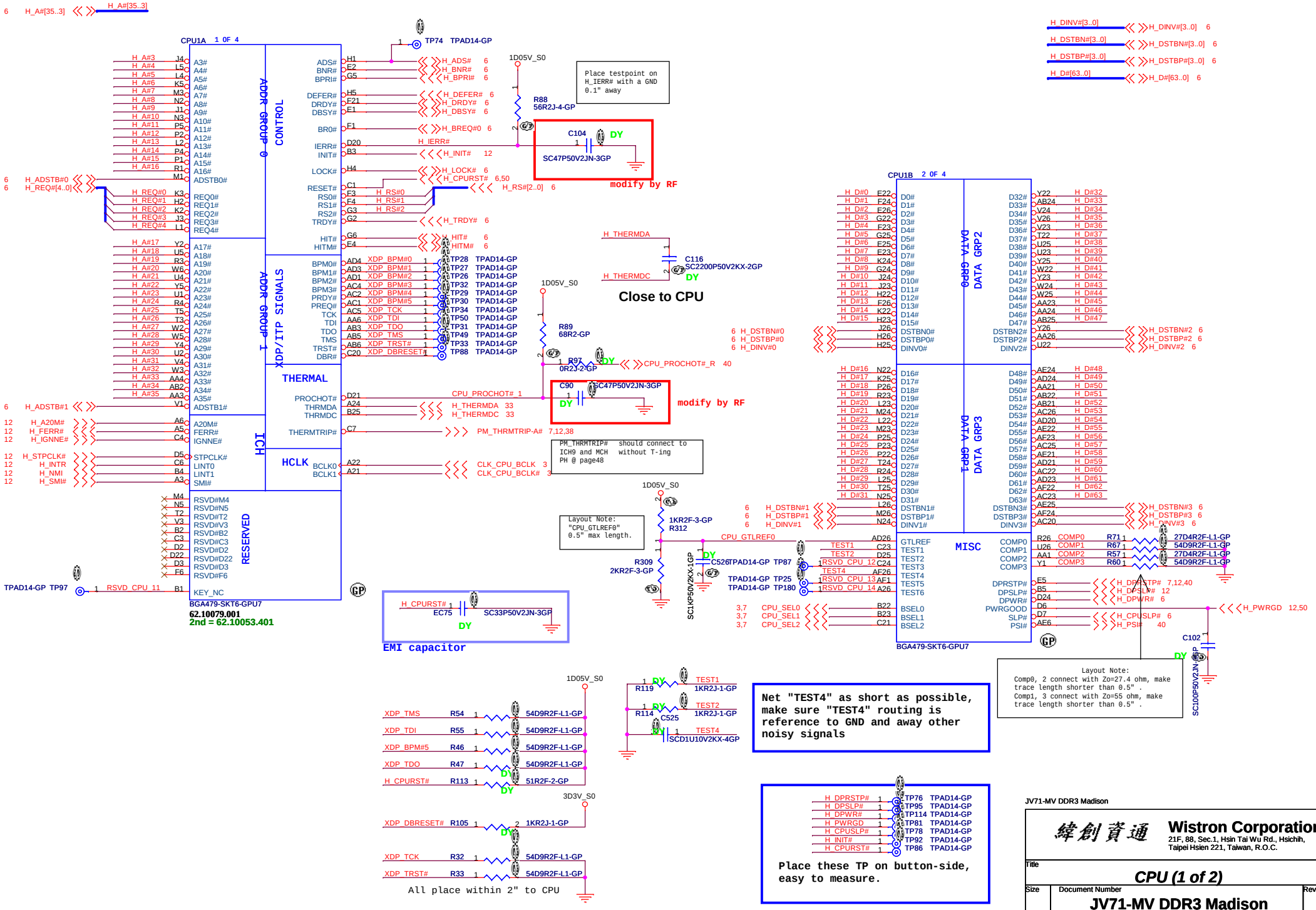
CPU1A 1 OF 4
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
BGA479-SKT6-GPU7
62.10079.001
2nd = 62.10053.401
CPU1B 2 OF 4
DATA GRP0
DATA GRP1
DATA GRP2
DATA GRP3
MISC
Close to CPU
modify by RF
EMI capacitor
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH PH @ page48
Layout Note: "CPU_GTLREF0" 0.5" max length.
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Place these TP on button-side, easy to measure.
All place within 2" to CPU
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
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CPU (1 of 2)
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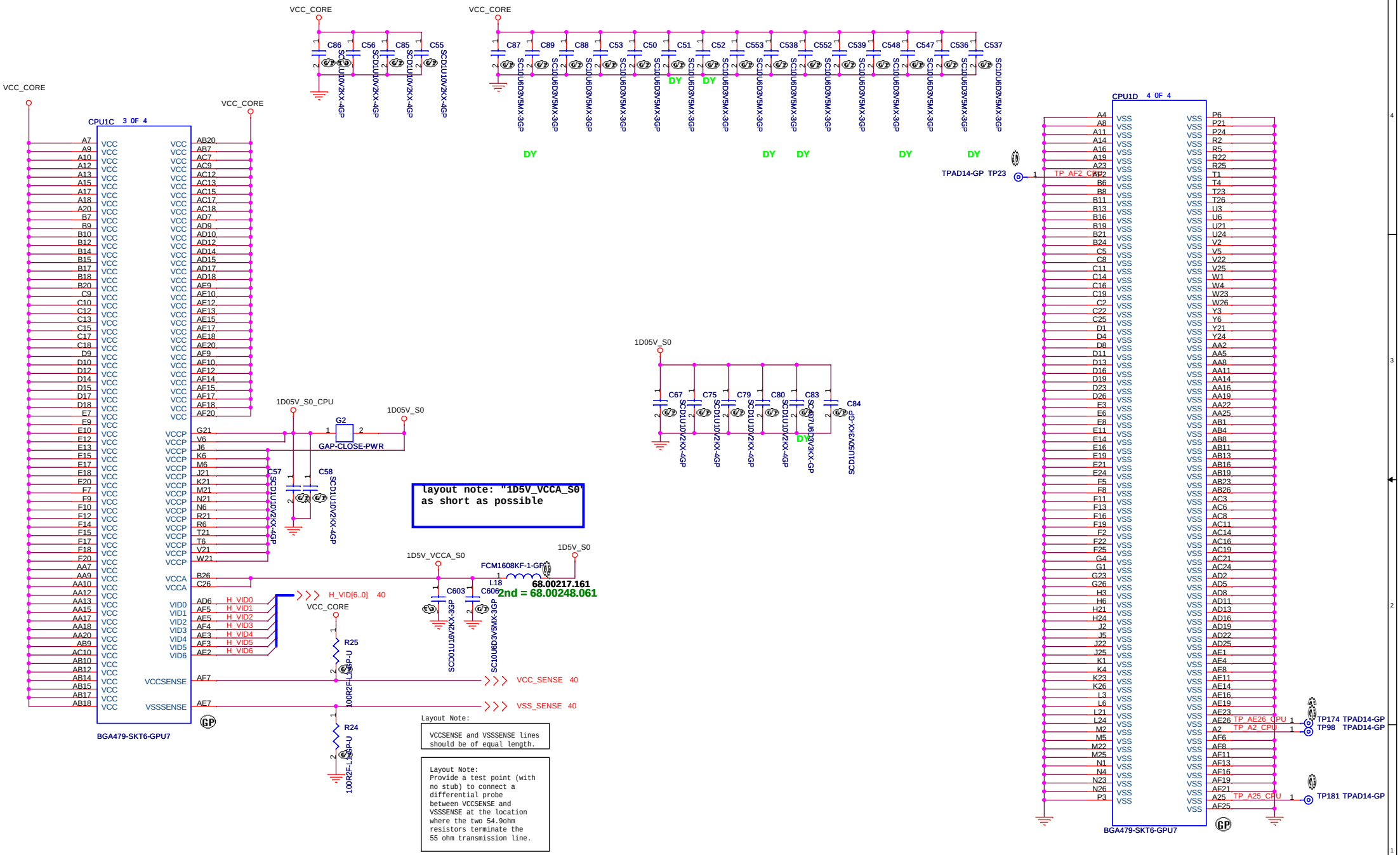

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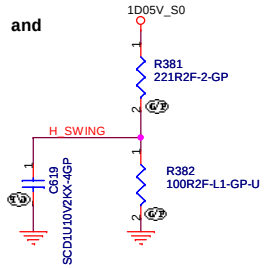
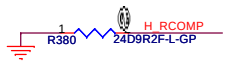
H_SWING routing Trace width and Spacing use 10 / 20 mil

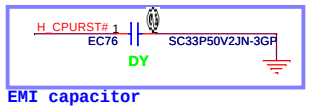
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



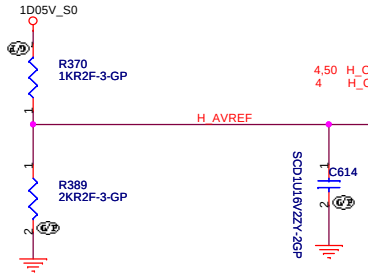
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



EMI capacitor



JV71-MV DDR3 Madison

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Close to GMCH as 500 mils.

modify by RF

FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm

CRT_IREF routing Trace width use 20 mil

for HDMI port C

FOR Cantiga:500 ohm
Teenah: 392 ohm

EMI capacitor

FOR UMA,change to 159 ohm (66.15156.08L)

FOR Discrete change RN to 0 ohm (66.R0036.A8L)

FOR UMA,change to 75 ohm (66.75036.08L)

layout take note

Remove RN88 & RN89

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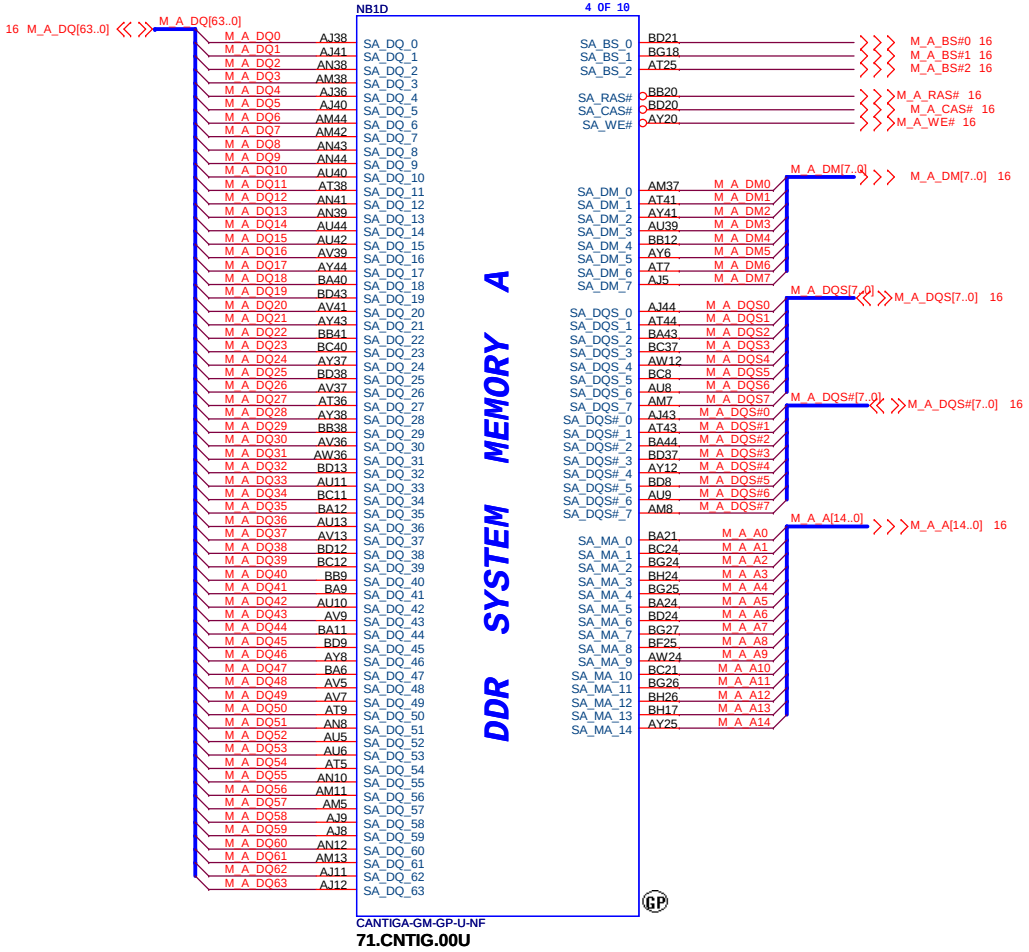

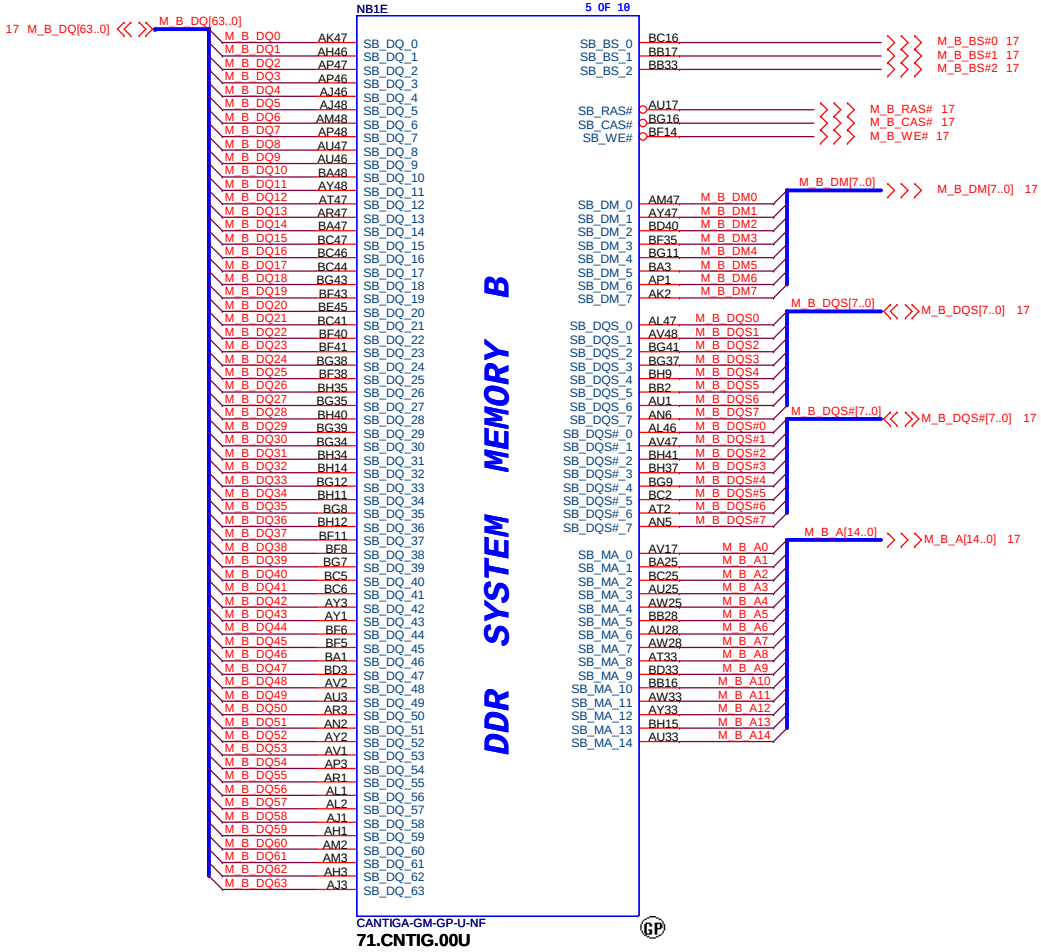

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Title: ***Cantiga (3 of 6)***

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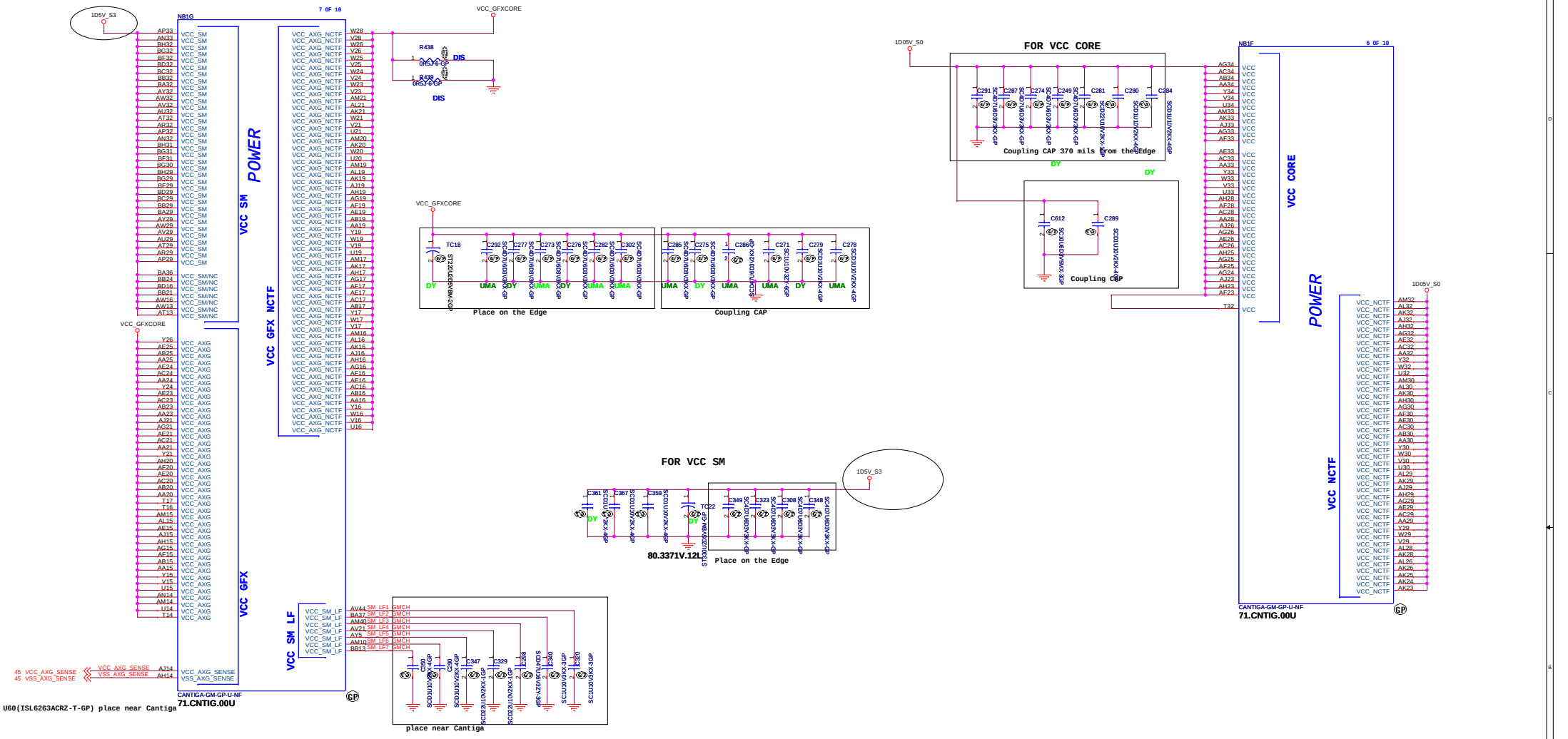

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Title: Cantiga (4 of 6)		
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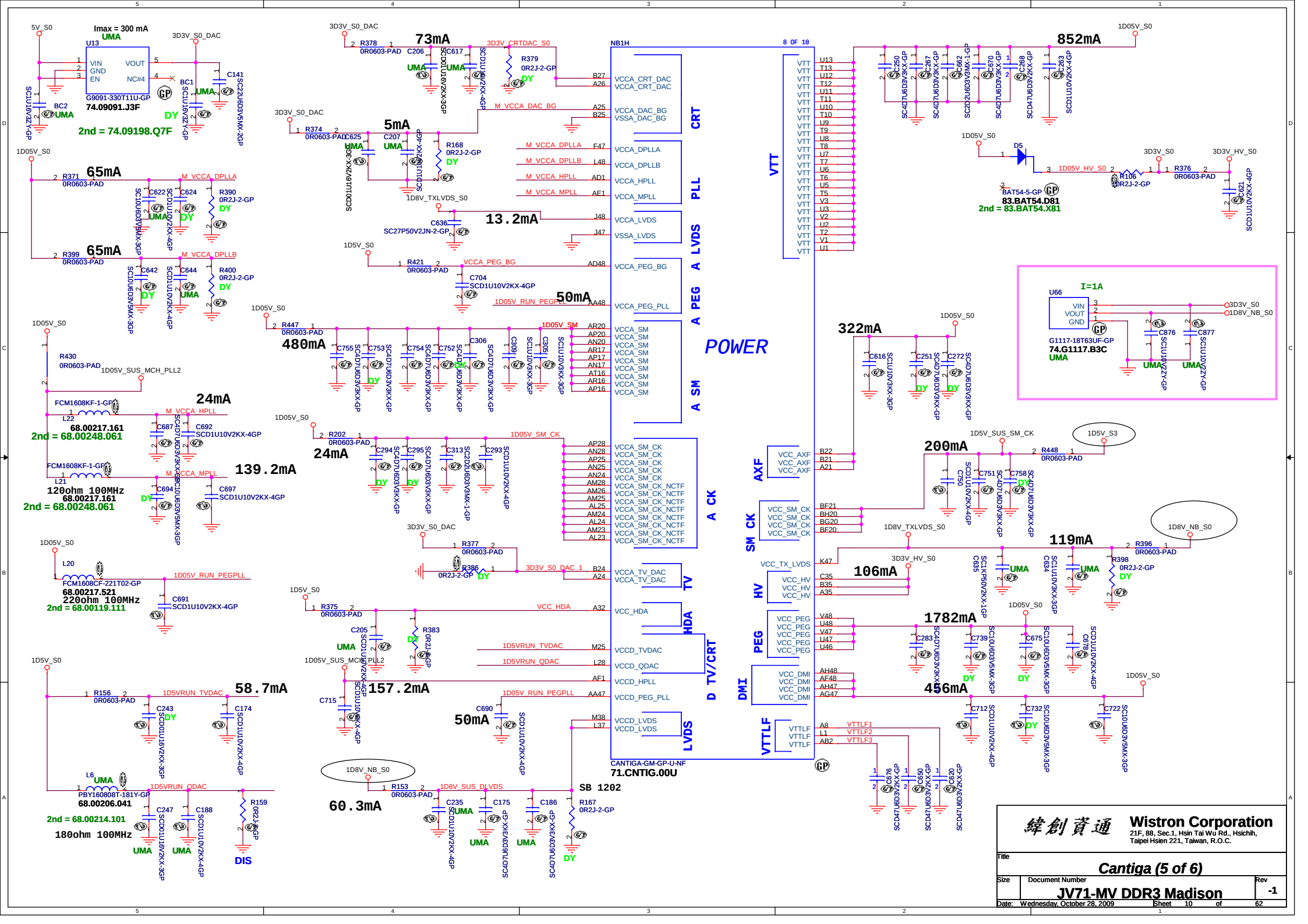
POWER
NB1H
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
Imax = 300 mA
UMA
G9091-330T11U-GP
74.09091.J3F
2nd = 74.09198.Q7F
73mA
5mA
65mA
65mA
13.2mA
50mA
480mA
24mA
139.2mA
58.7mA
157.2mA
50mA
60.3mA
852mA
322mA
200mA
119mA
106mA
1782mA
456mA
24mA
68.00217.161
2nd = 68.00248.061
120ohm 100MHz
68.00217.161
2nd = 68.00248.061
68.00217.521
220ohm 100MHz
2nd = 68.00119.111
68.00206.041
2nd = 68.00214.101
180ohm 100MHz
DIS
SB 1202
I=1A
G1117-18T63UF-GP
74.G1117.B3C
BAT54-5-GP
83.BAT54.D81
2nd = 83.BAT54.X81
CRT
PLL
A LVDS
A PEG
A SM
A CK
AXF
SM CK
HV
PEG
DMI
D TV/CRT
HDA
TV
LVDS
VTT
VTTLF
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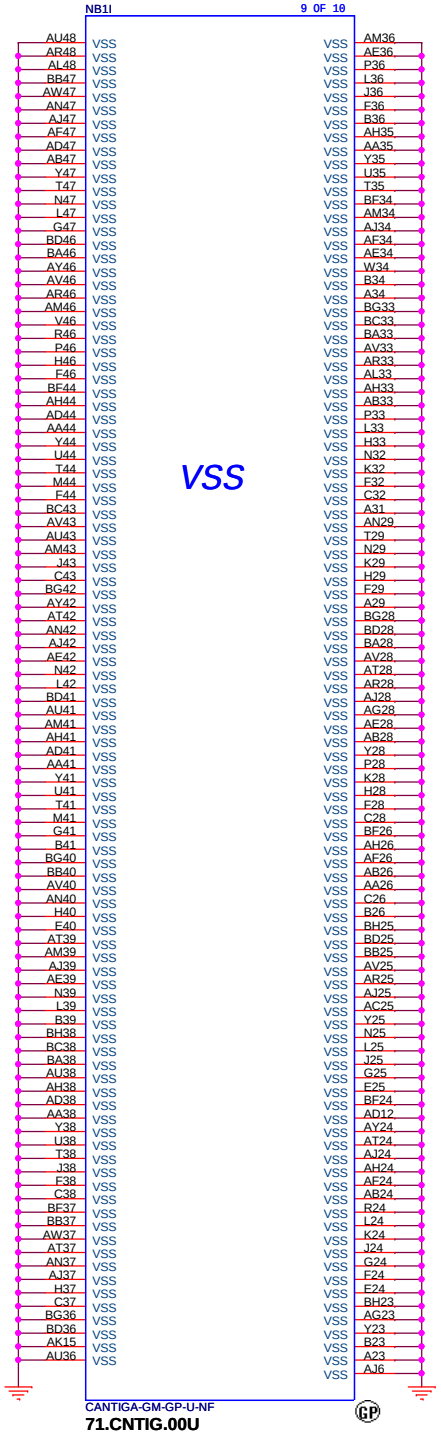

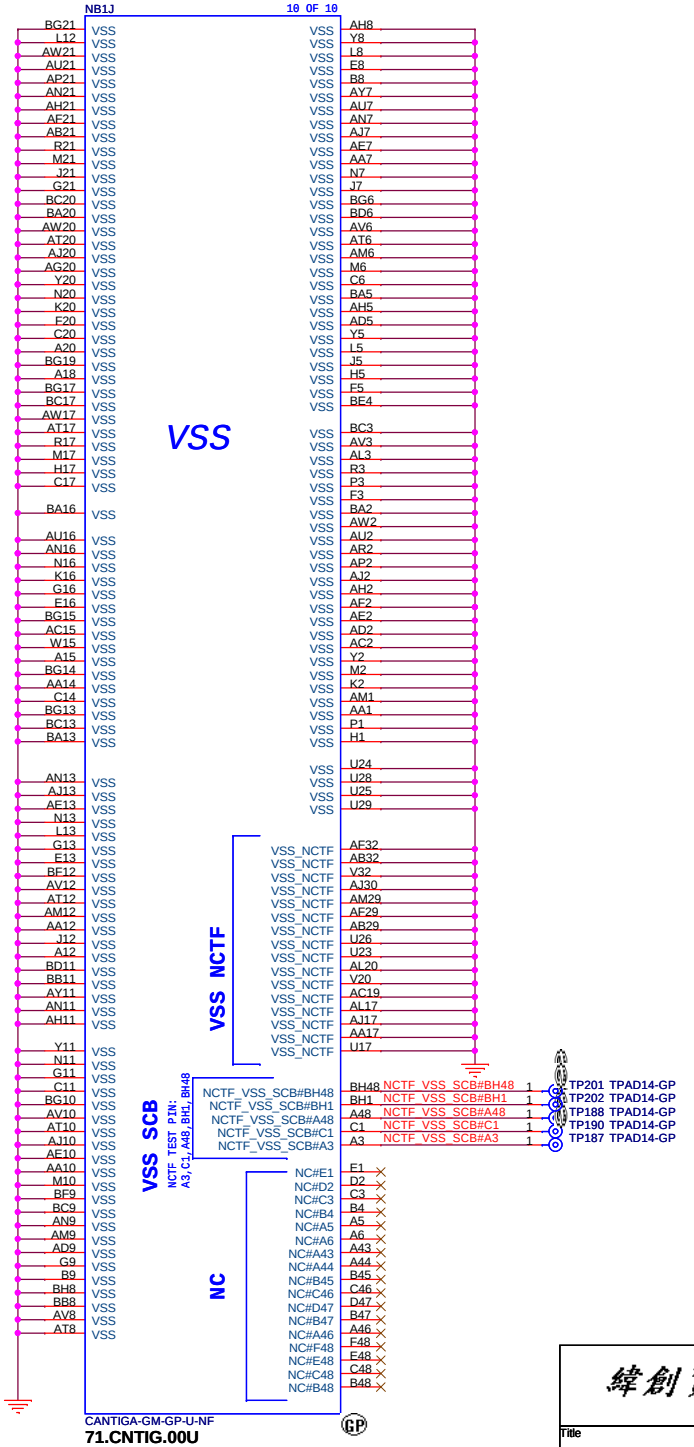

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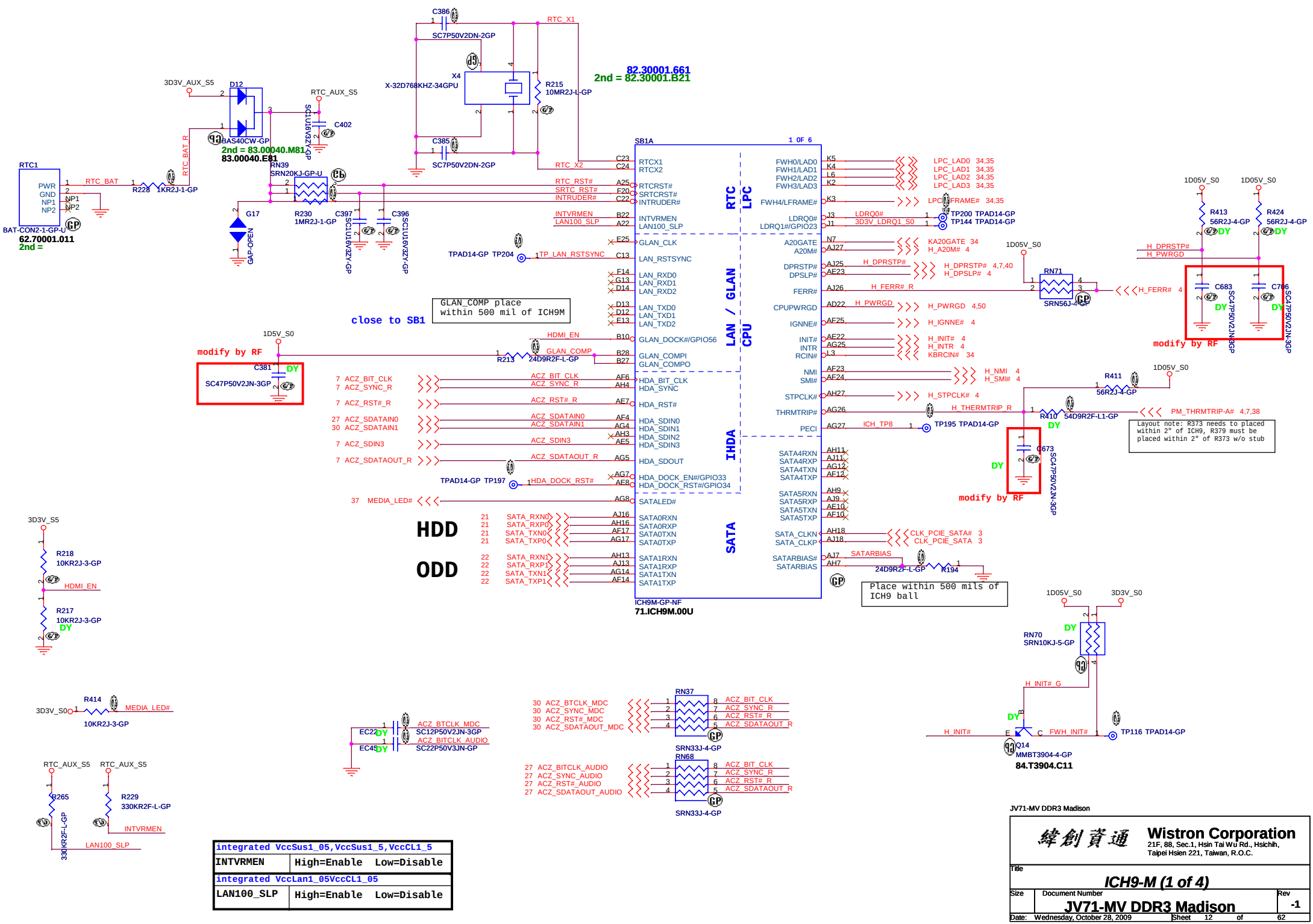
82.30001.661
2nd = 82.30001.B21
SB1A
1 OF 6
RTC
LPC
GLAN
LAN / GLAN
CPU
IHDA
SATA
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
ICH9M-GP-NF
71.ICH9M.00U
RTC_X1
RTC_X2
X4
X-32D768KHZ-34GPU
C386
C385
SC7P50V2DN-2GP
R215
10MR2J-L-GP
C23
C24
RTC_RST#
SRTC_RST#
INTRUDER#
INTVRMEN
LAN100_SLP
TPAD14-GP TP204
TP_LAN_RSTSYNC
C13
HDMI_EN
GLAN_COMP
R213
24D9R2F-L-GP
close to SB1
GLAN_COMP place within 500 mil of ICH9M
modify by RF
1D05V_S0
C381
SC47P50V2JN-3GP
DY
ACZ_BIT_CLK
ACZ_SYNC_R
ACZ_RST#_R
ACZ_SDATAIN0
ACZ_SDATAIN1
ACZ_SDIN3
ACZ_SDATAOUT_R
TPAD14-GP TP197
HDA_DOCK_RST#
MEDIA_LED#
HDD
ODD
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
LPC_LAD0 34,35
LPC_LAD1 34,35
LPC_LAD2 34,35
LPC_LAD3 34,35
LPC_FRAME# 34,35
LDRQ0#
3D3V_LDRQ1_S0
TP200 TPAD14-GP
TP144 TPAD14-GP
KA20GATE 34
H_A20M# 4
H_DPRSTP# 4,7,40
H_DPSLP# 4
H_FERR# 4
H_PWRGD 4,50
H_IGNNE# 4
H_INIT# 4
H_INTR 4
KBRCIN# 34
H_NMI 4
H_SMI# 4
H_STPCLK# 4
H_THERMTRIP_R
TP195 TPAD14-GP
ICH_TP8
CLK_PCIE_SATA# 3
CLK_PCIE_SATA 3
SATARBIAS
24D9R2F-L-GP
R194
Place within 500 mils of ICH9 ball
RN71
SRN56J-4-GP
R413
R424
56R2J-4-GP
C683
C706
SC47P50V2JN-3GP
R411
R410
54D9R2F-L1-GP
PM_THRMTRIP-A# 4,7,38
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
C673
RTC1
BAT-CON2-1-GP-U
62.70001.011
2nd =
RTC_BAT
R228
1KR2J-1-GP
RTC_BAT_R
D12
BAS40CW-GP
2nd = 83.00040.M81
83.00040.E81
3D3V_AUX_S5
RTC_AUX_S5
C402
SC1U16V2ZY-GP
RN39
SRN20KJ-GP-U
R230
1MR2J-1-GP
C397
C396
SC1U16V3ZY-GP
G17
GAP-OPEN
R218
10KR2J-3-GP
R217
10KR2J-3-GP
3D3V_S5
R414
10KR2J-3-GP
MEDIA_LED#
3D3V_S0
RN70
SRN10KJ-5-GP
H_INIT#_G
H_INIT#
Q14
MMBT3904-4-GP
84.T3904.C11
TP116 TPAD14-GP
FWH_INIT#
RN37
SRN33J-4-GP
RN68
SRN33J-4-GP
ACZ_BTCLK_MDC
ACZ_SYNC_MDC
ACZ_RST#_MDC
ACZ_SDATAOUT_MDC
ACZ_BTCLK_AUDIO
ACZ_SYNC_AUDIO
ACZ_RST#_AUDIO
ACZ_SDATAOUT_AUDIO
EC22
EC45
SC12P50V2JN-3GP
SC22P50V3JN-GP
R265
33KR2F-L-GP
R229
330KR2F-L-GP
INTVRMEN
LAN100_SLP
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN
High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP
High=Enable Low=Disable
JV71-MV DDR3 Madison
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4)
Size
Document Number
JV71-MV DDR3 Madison
Rev
-1
Date: Wednesday, October 28, 2009
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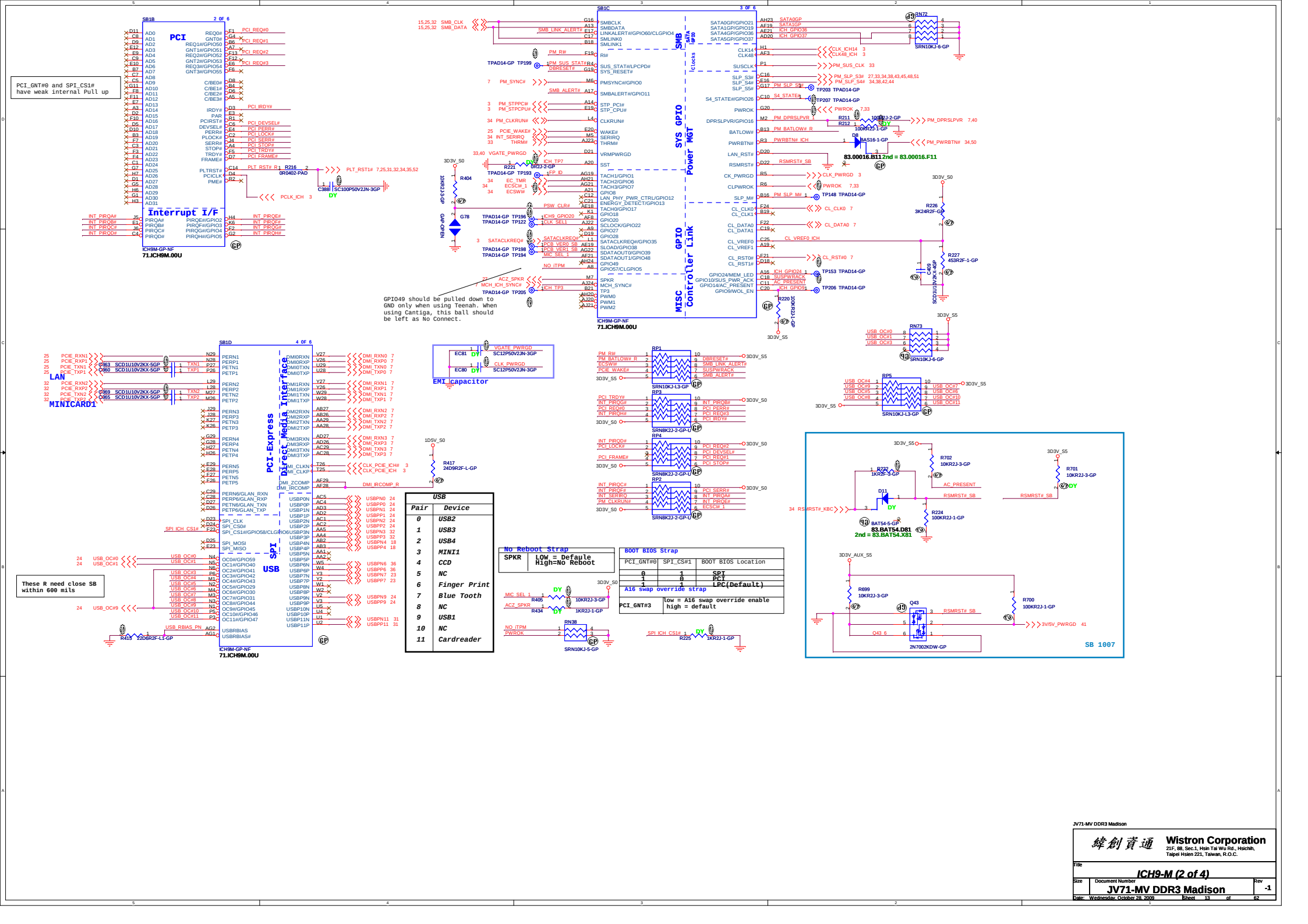
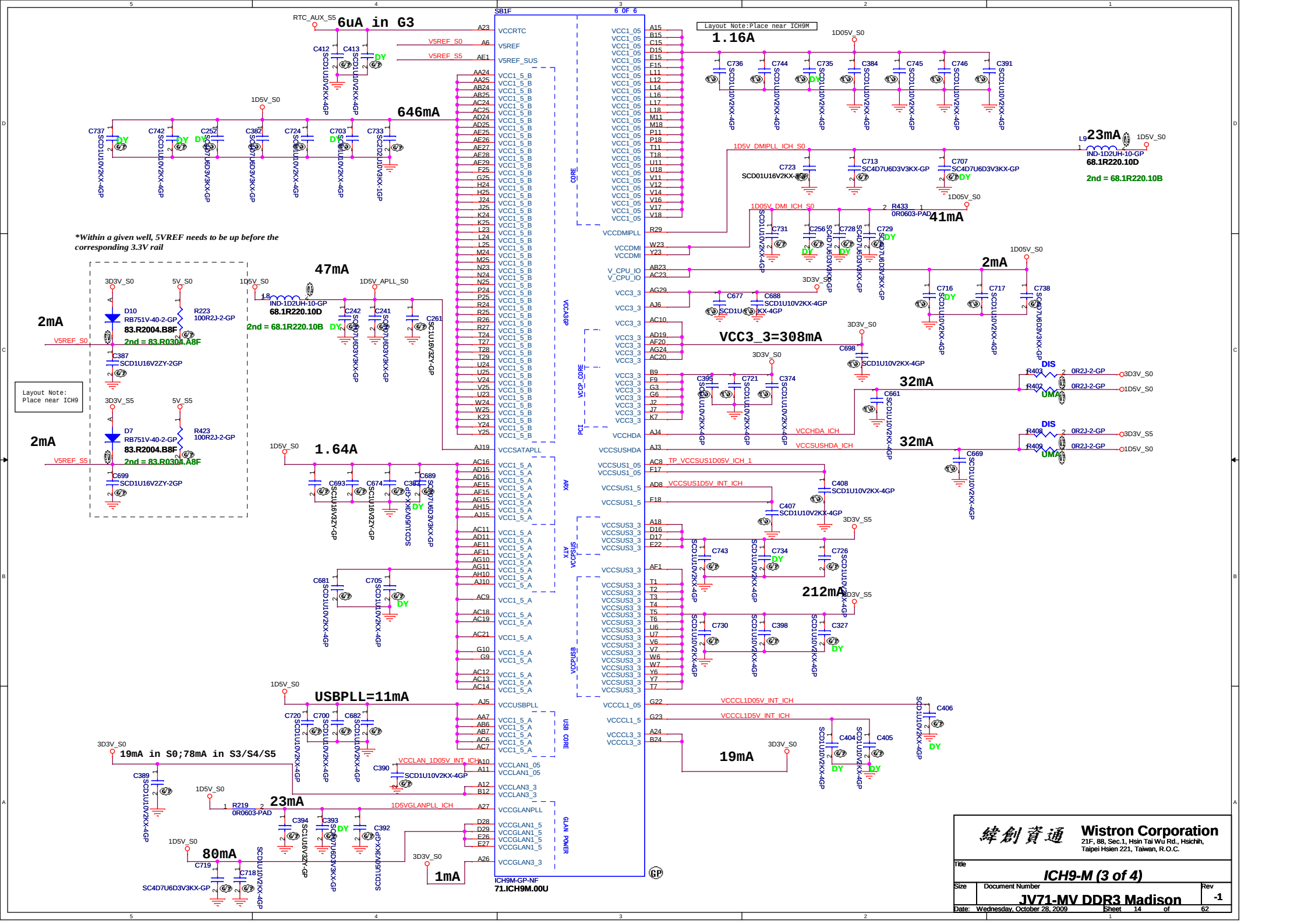

PCI_GNT#0 and SPI_CS1# have weak internal Pull up
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
SB1B
2 OF 6
SB1C
3 OF 6
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
SB1D
4 OF 6
PCI-Express
Direct Media Interface
SPI
USB
LAN
MINICARD1
EMI capacitor
These R need close SB within 600 mils
USB
Pair
Device
0
USB2
1
USB3
2
USB4
3
MINI1
4
CCD
5
NC
6
Finger Print
7
Blue Tooth
8
NC
9
USB1
10
NC
11
Cardreader
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
BOOT BIOS Strap
PCI_GNT#0
SPI_CS#1
BOOT BIOS Location
0
1
SPI
1
0
PCI
1
1
LPC(Default)
A16 swap override strap
PCI_GNT#3
low = A16 swap override enable
high = default
2nd = 83.BAT54.X81
83.BAT54.D81
SB 1007
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
JV71-MV DDR3 Madison
ICH9-M (2 of 4)
JV71-MV DDR3 Madison
-1
Wednesday, October 28, 2009
13
62


6uA in G3
646mA
1.16A
23mA
41mA
2mA
47mA
1.64A
VCC3_3=308mA
32mA
212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
80mA
1mA
19mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
ICH9M-GP-NF
71.ICH9M.00U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
JV71-MV DDR3 Madison
Rev -1
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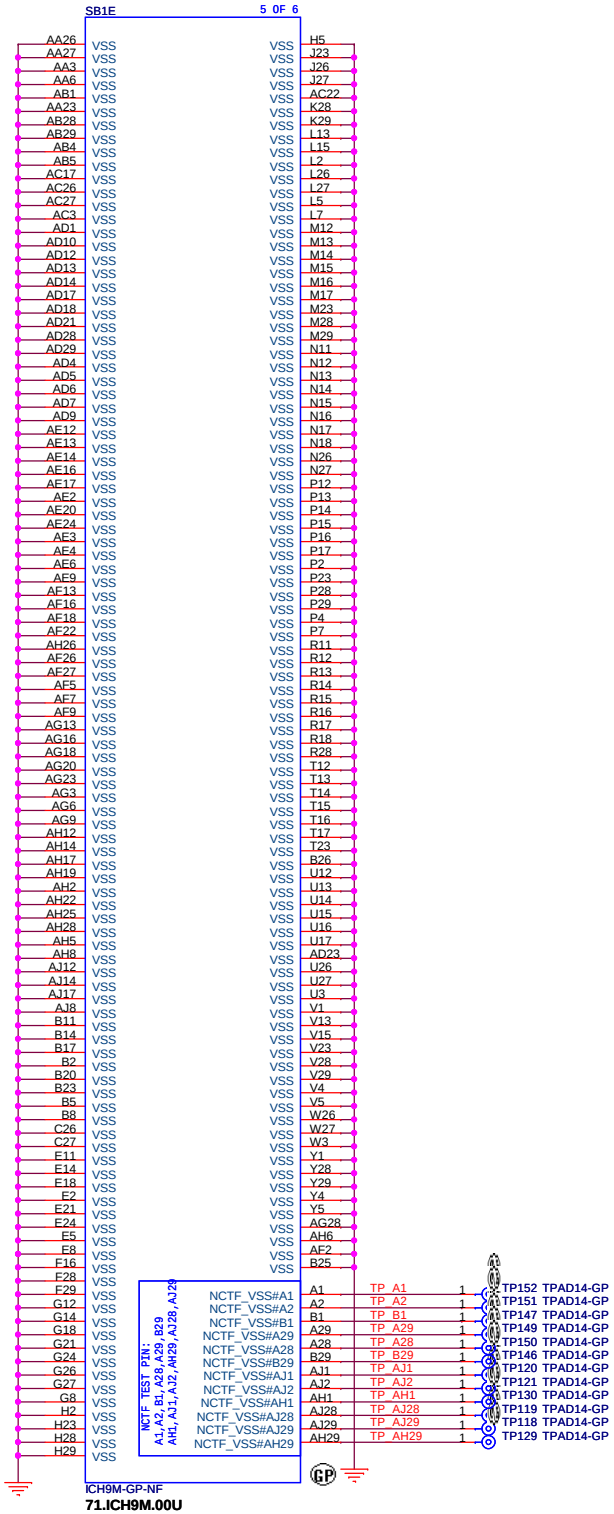

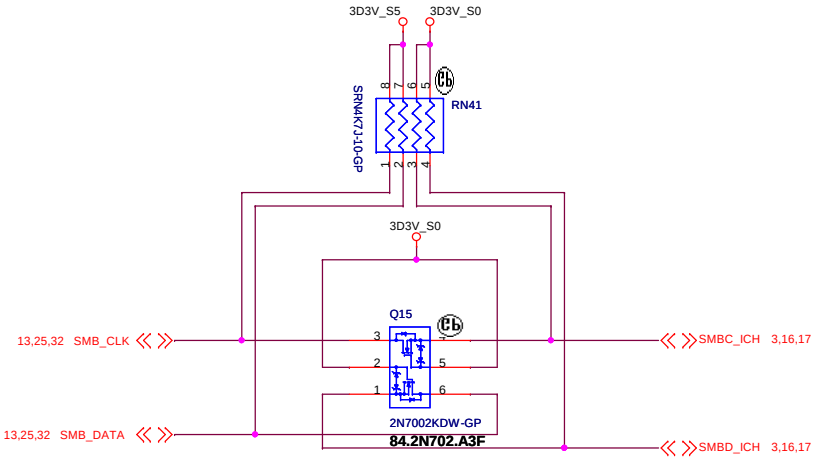

SMBUS

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Title: ***ICH9-M (4 of 4)***

Size | Document Number: **JV71-MV DDR3 Madison** | Rev: -1

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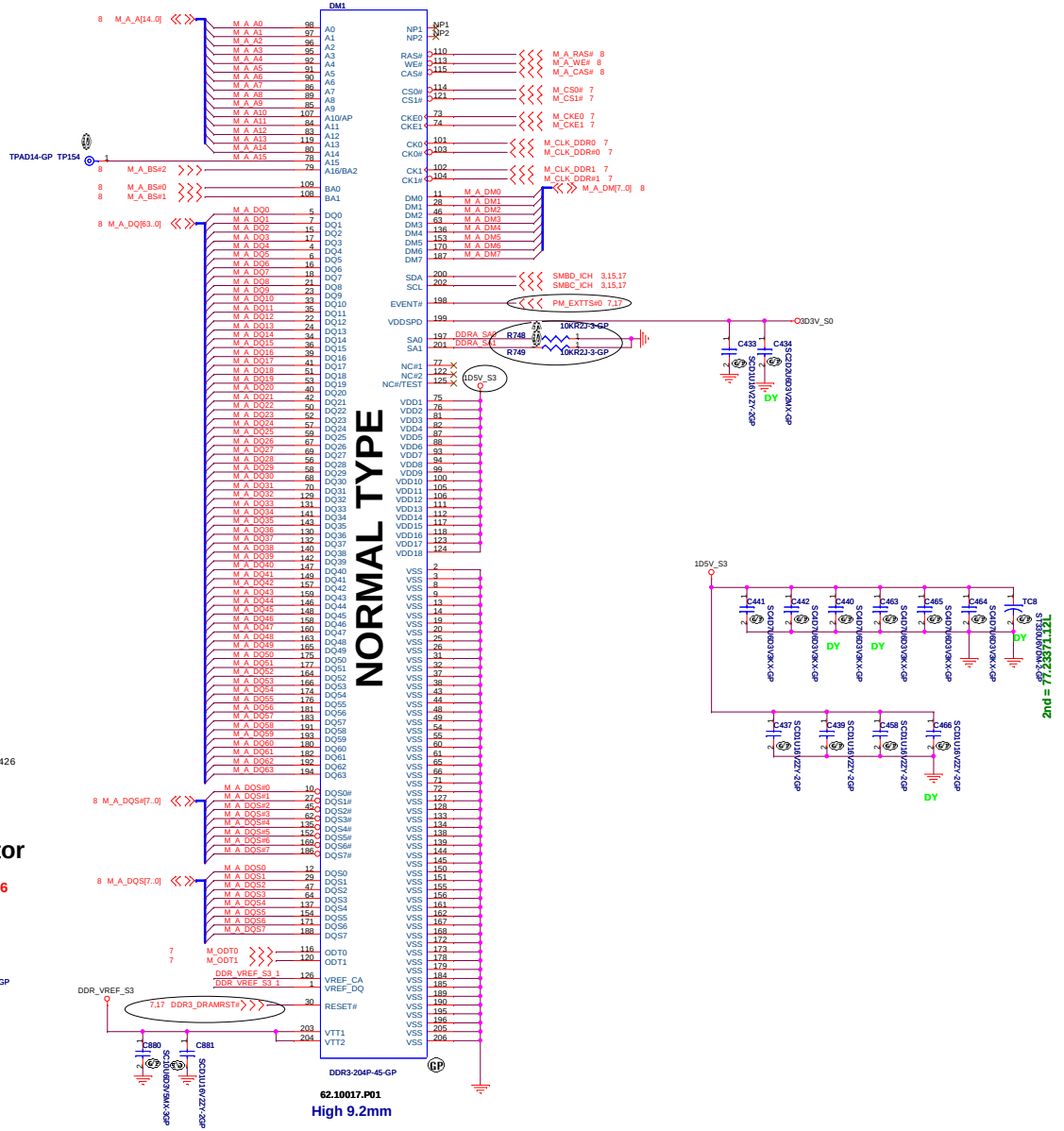
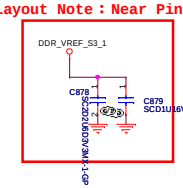
DDR3 SOCKET_1



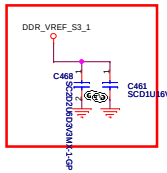
0818 delete pull-up resistor(RN88~RN94),C400,C426

Decoupling Capacitor

Layout Note : Near Pin 126



Layout Note : Near Pin 1



0818 add the net(DDR3_DRAMRST#)
0818 modify the net(DDR_VREF_S3_1)

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Title	*DDR3 Socket*	
Size	Document Number: JV71-MV DDR3 Madison	Rev: -1
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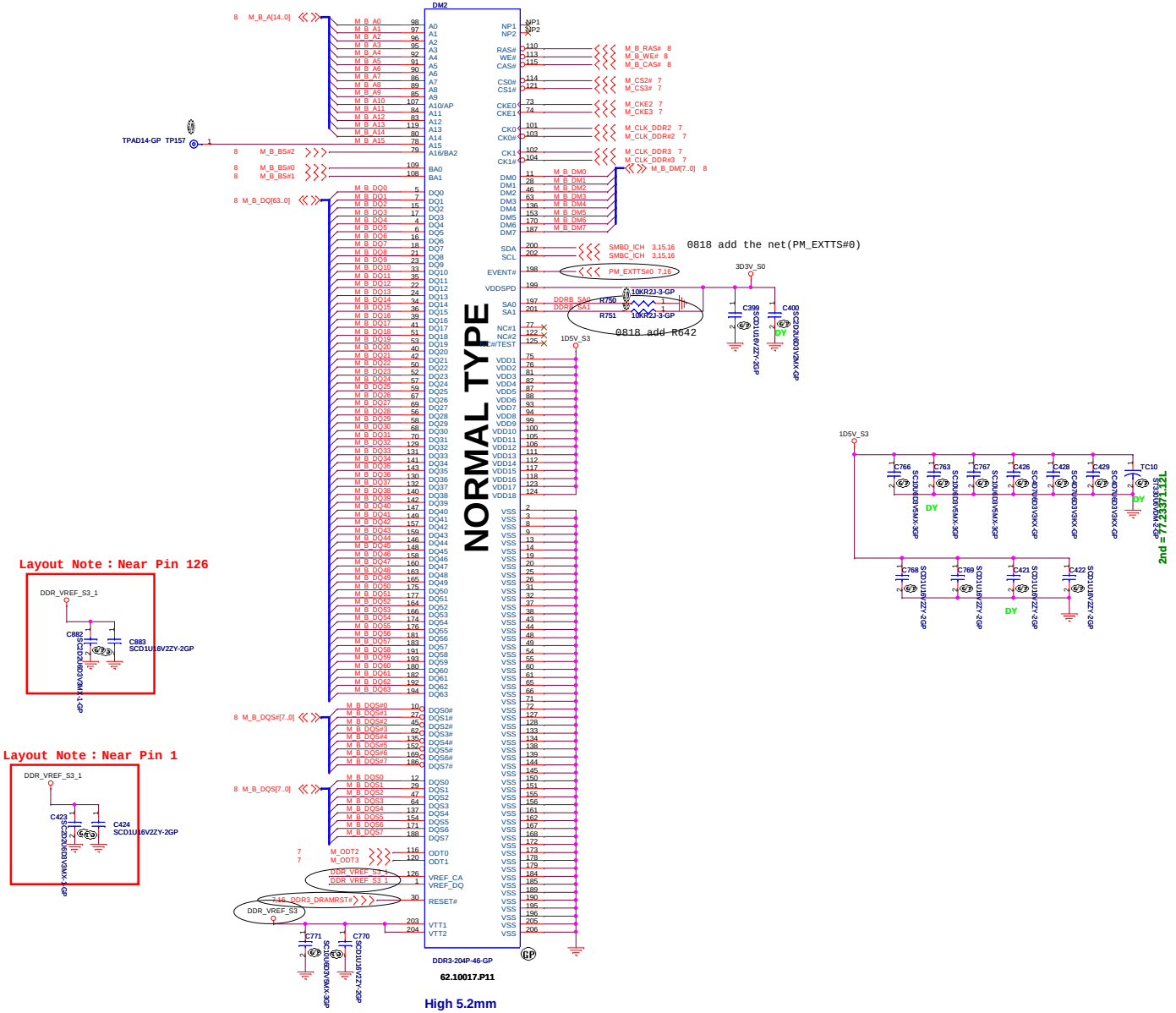
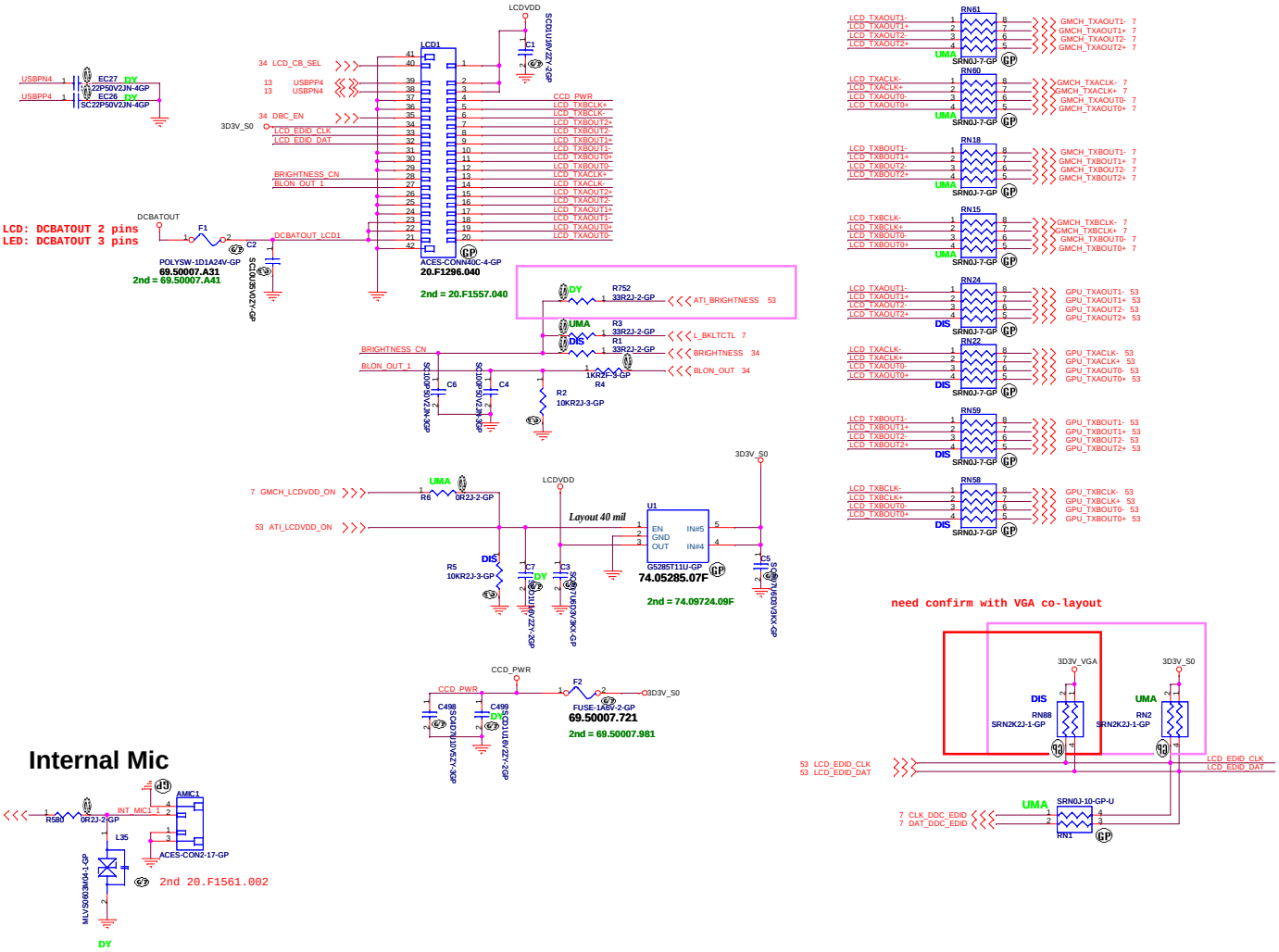
DDR3 SOCKET_2



0818 add the net(DDR3_DRAMRST#)
0818 modify the net(DDR_VREF_S3_1)
0824 modify DM2 pin 203,204 to (DDR_VREF_S3)

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DDR3 Socket2	
Size	Document Number: JV71-MV DDR3 Madison	Rev: -1
Date: Wednesday, October 28, 2009	Sheet 17 of 62	

LCD/INVERTER/CCD CONN



need confirm with VGA co-layout

Internal Mic

JV71-MV DDR3 Madison

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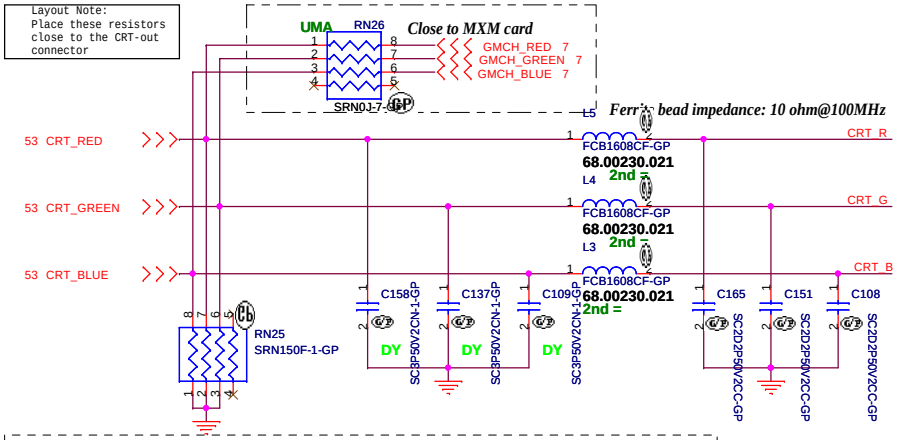
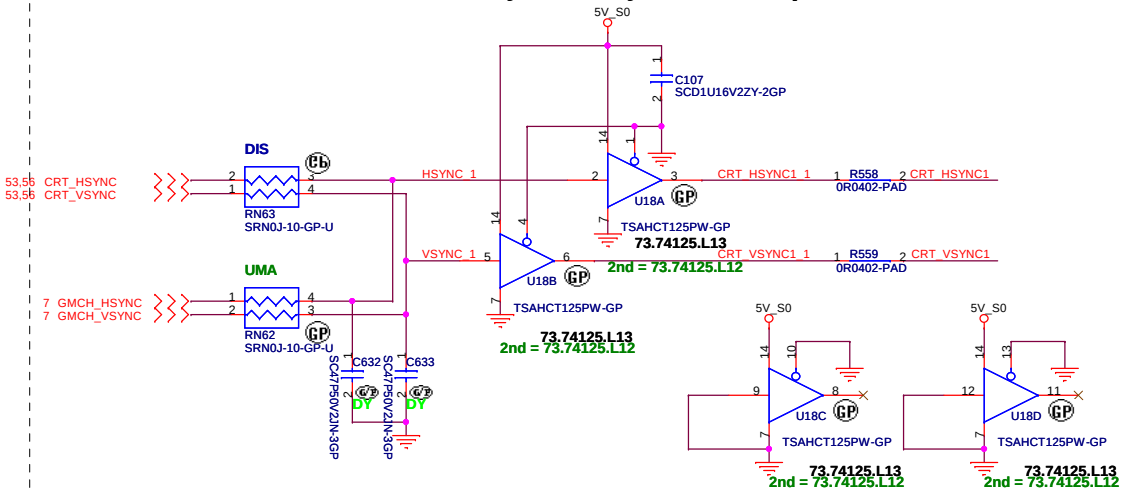
Title	***LCD CONN***
Size	Document Number: **JV71-MV DDR3 Madison** — Rev: -1
Date: Wednesday, October 28, 2009	Sheet 18 of 62

Layout Note:
Place these resistors close to the CRT-out connector

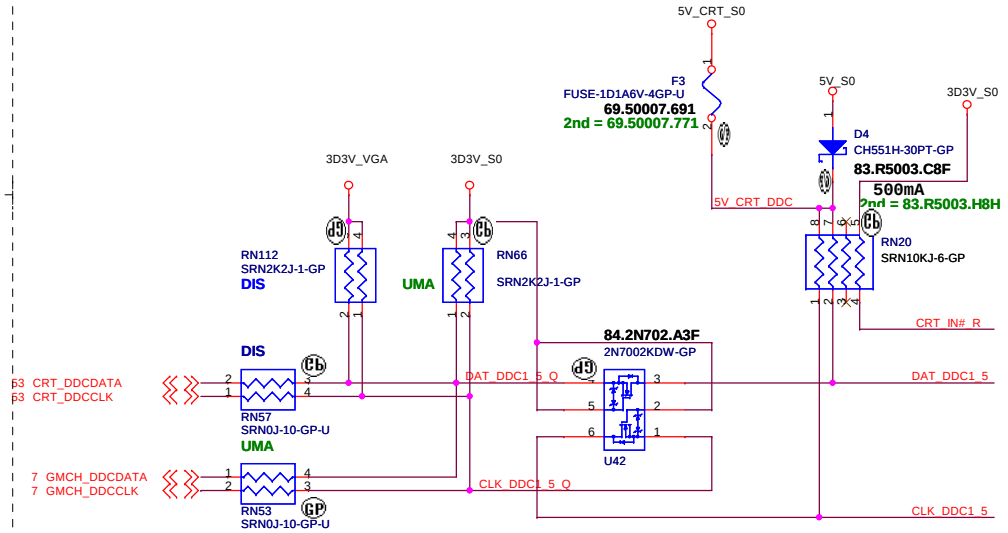


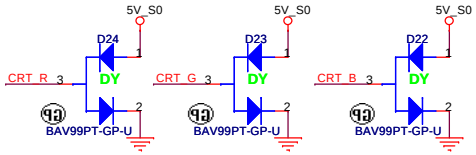
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

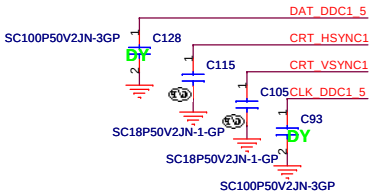


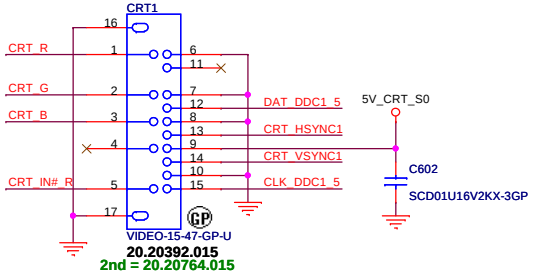
DDC_CLK & DATA level shift

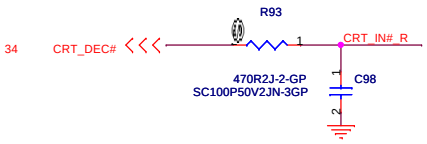


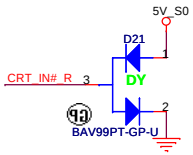


CRT I/F & CONNECTOR









6 1 7 2 8 3 9 4 10 5

JV71-MV DDR3 Madison

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Title: **CRT CONN**

Size	Document Number	Rev
	JV71-MV DDR3 Madison	-1

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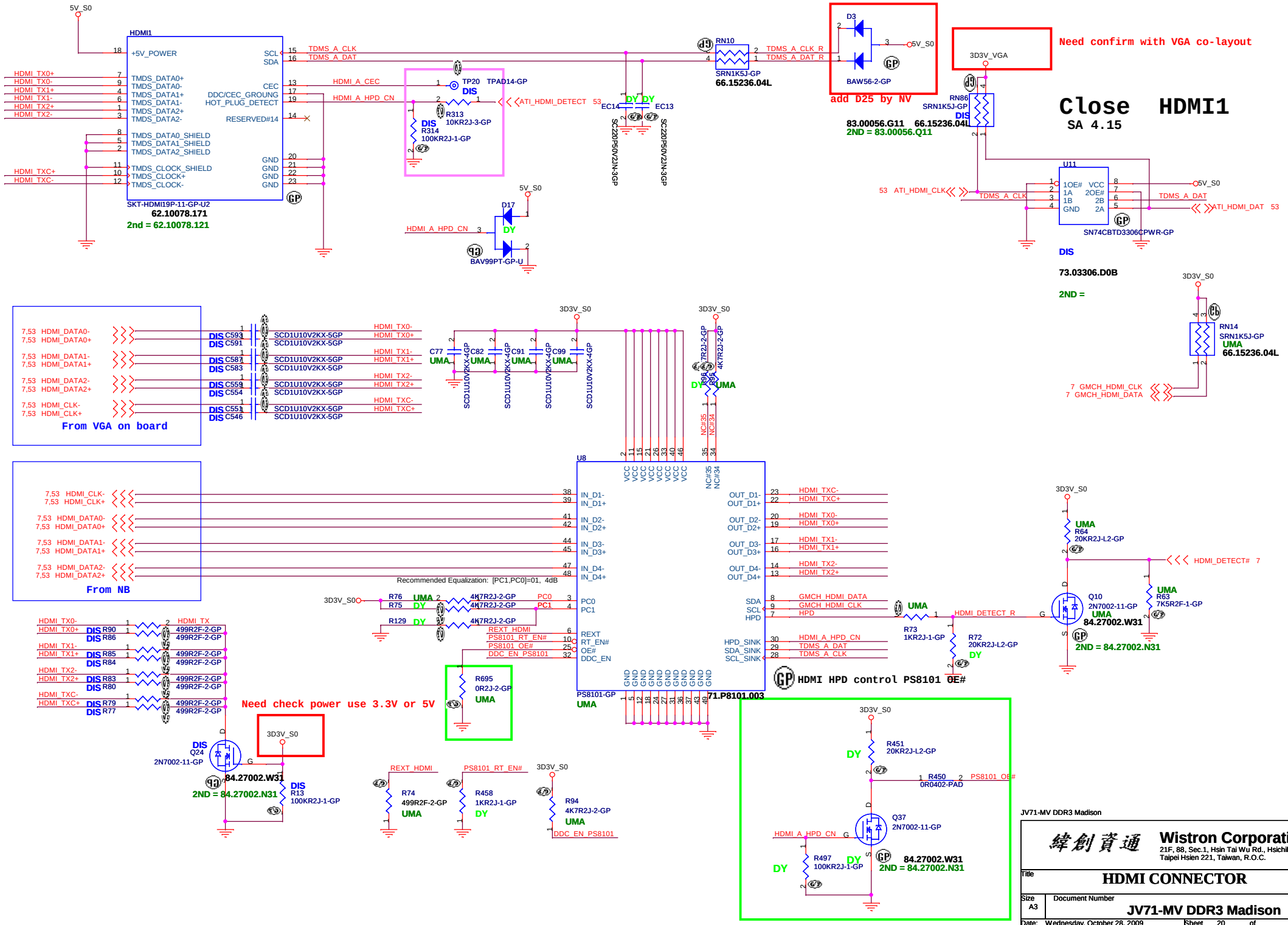
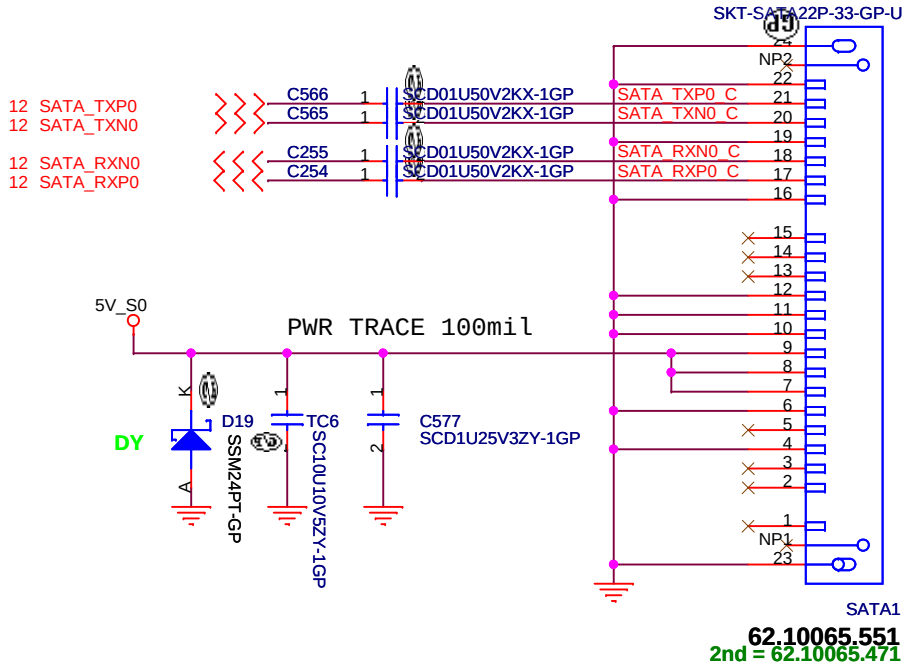

HDMI1
SKT-HDMI19P-11-GP-U2
62.10078.171
2nd = 62.10078.121
Need confirm with VGA co-layout
Close HDMI1
SA 4.15
add D25 by NV
83.00056.G11 66.15236.04L
2ND = 83.00056.Q11
SN74CBTD3306CPWR-GP
DIS
73.03306.D0B
2ND =
From VGA on board
From NB
Recommended Equalization: [PC1,PC0]=01, 4dB
PS8101-GP
71.P8101.003
HDMI HPD control PS8101 OE#
Need check power use 3.3V or 5V
2ND = 84.27002.N31
JV71-MV DDR3 Madison
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
HDMI CONNECTOR
JV71-MV DDR3 Madison
Wednesday, October 28, 2009

SATA Connector



JV71-MV DDR3 Madison

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Title	***HDD CONN***	
Size	Document Number: **JV71-MV DDR3 Madison**	Rev: **-1**
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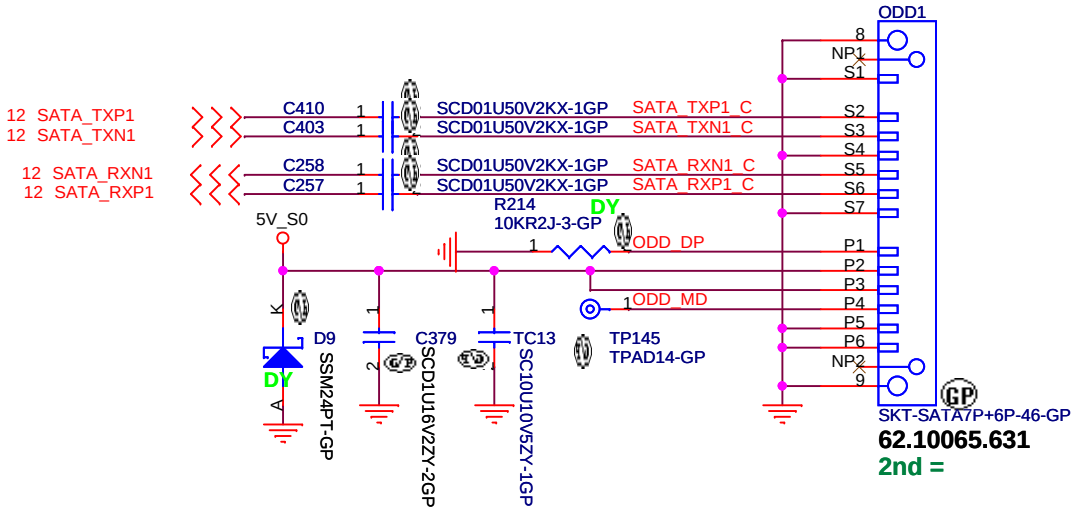
ODD Connector



JV71-MV DDR3 Madison

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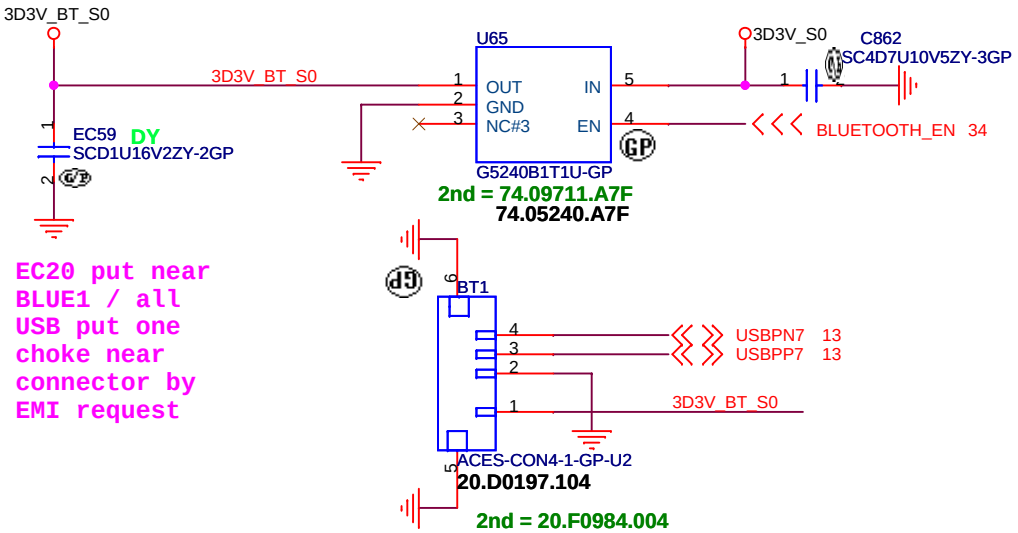
Title	***ODD***	
Size	Document Number **JV71-MV DDR3 Madison**	Rev **-1**
Date: Wednesday, October 28, 2009	Sheet 22 of 62	

BLUETOOTH MODULE



JV71-MV DDR3 Madison

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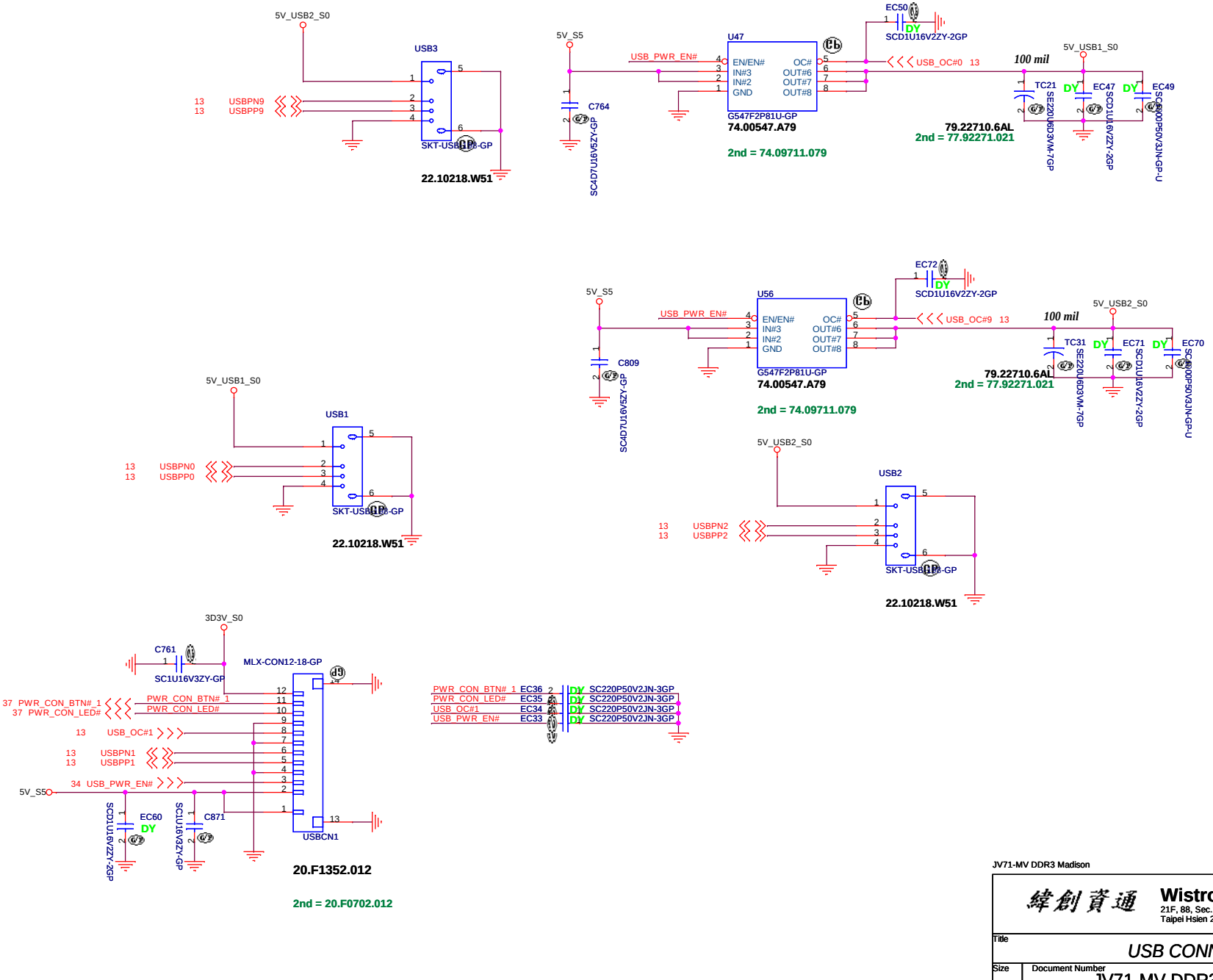
Title: ***BLUETOOTH***		
Size	Document Number: **JV71-MV DDR3 Madison**	Rev: **-1**
Date: Wednesday, October 28, 2009	Sheet 23 of 62	



JV71-MV DDR3 Madison

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Title	*USB CONN*	
Size	Document Number: JV71-MV DDR3 Madison	Rev: -1
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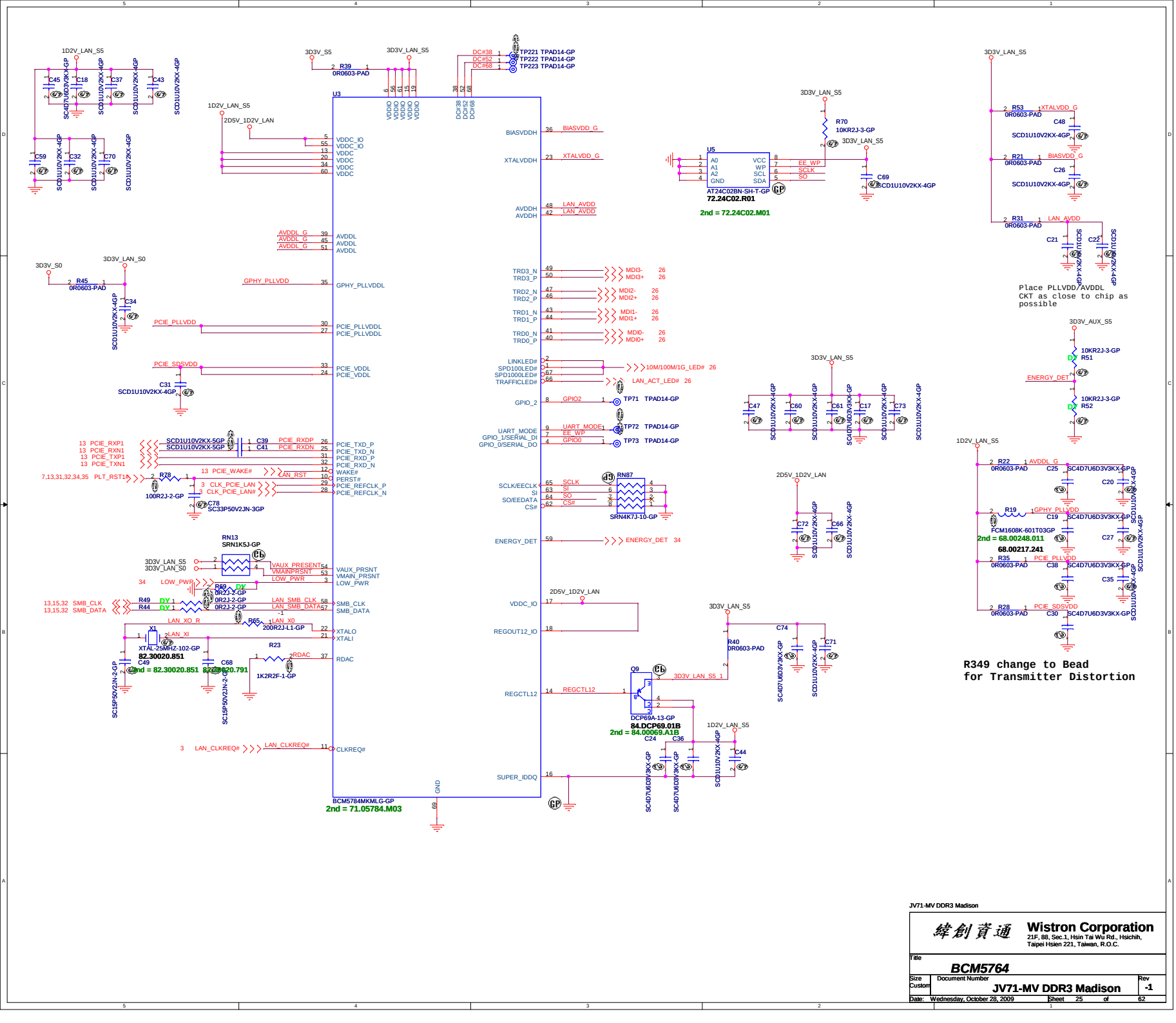
U3
BCM5784MKMLG-GP
2nd = 71.05784.M03
U5
AT24C02BN-SH-T-GP
72.24C02.R01
2nd = 72.24C02.M01
X1
XTAL-25MHZ-102-GP
82.30020.851
2nd = 82.30020.851 82.30020.791
Q9
DCP69A-13-GP
84.DCP69.01B
2nd = 84.00069.A1B
RN13
SRN1K5J-GP
RN87
SRN4K7J-10-GP
Place PLLVDD/AVDDL CKT as close to chip as possible
R349 change to Bead for Transmitter Distortion
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
BCM5764
JV71-MV DDR3 Madison
Rev -1
Wednesday, October 28, 2009
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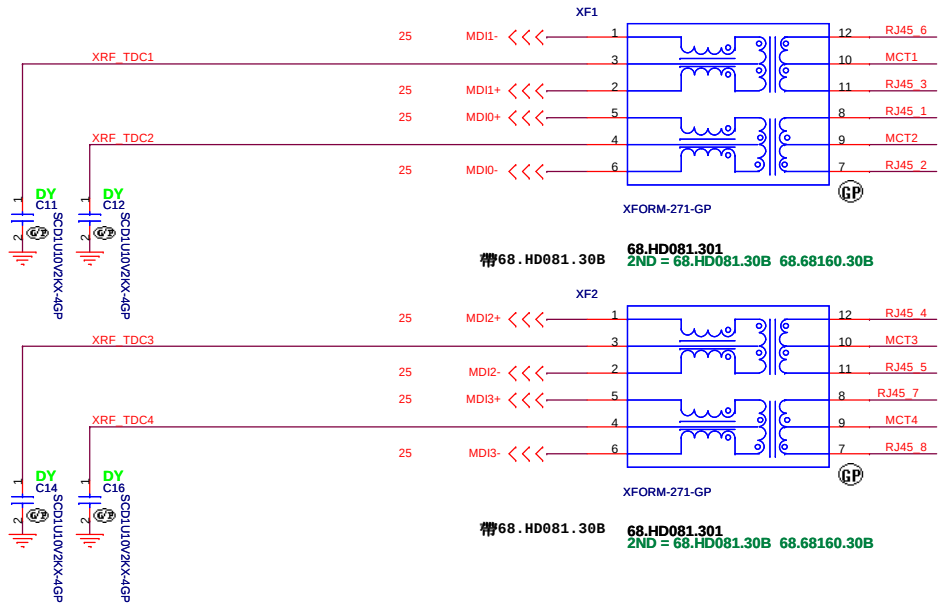
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector

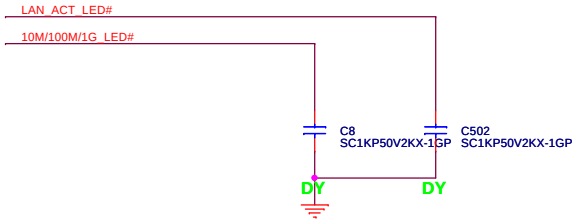
LAN Connector

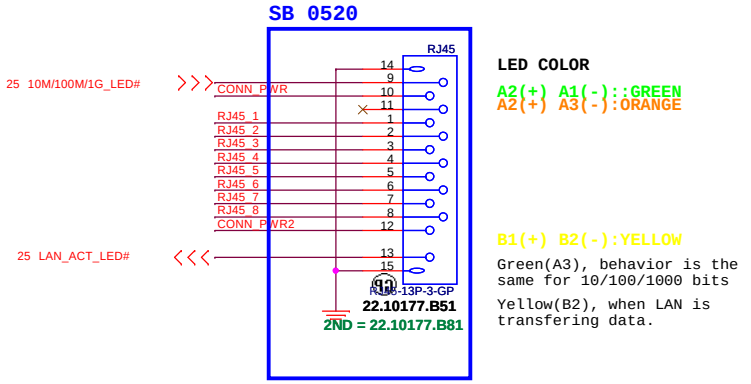
GIGA Lan Transformer

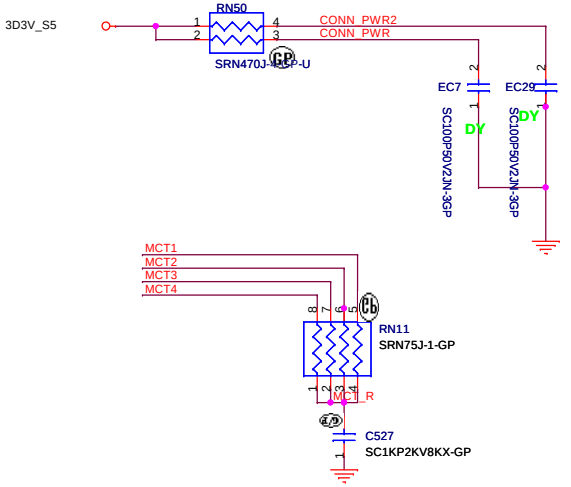


帶68.HD081.30B 68.HD081.301
2ND = 68.HD081.30B 68.68160.30B

帶68.HD081.30B 68.HD081.301
2ND = 68.HD081.30B 68.68160.30B







JV71-MV DDR3 Madison

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN CONN	
Size A3	Document Number JV71-MV DDR3 Madison	Rev -1
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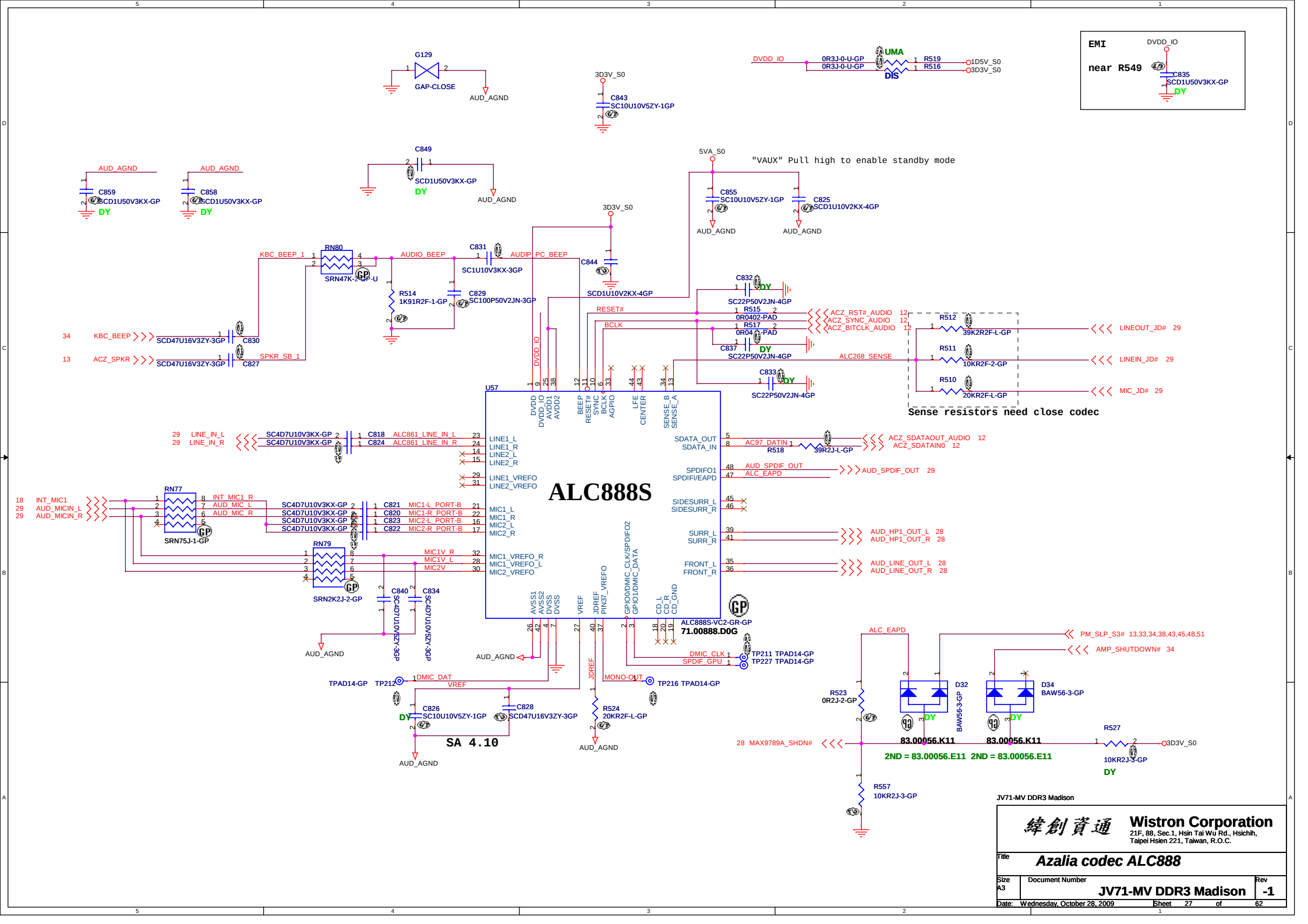
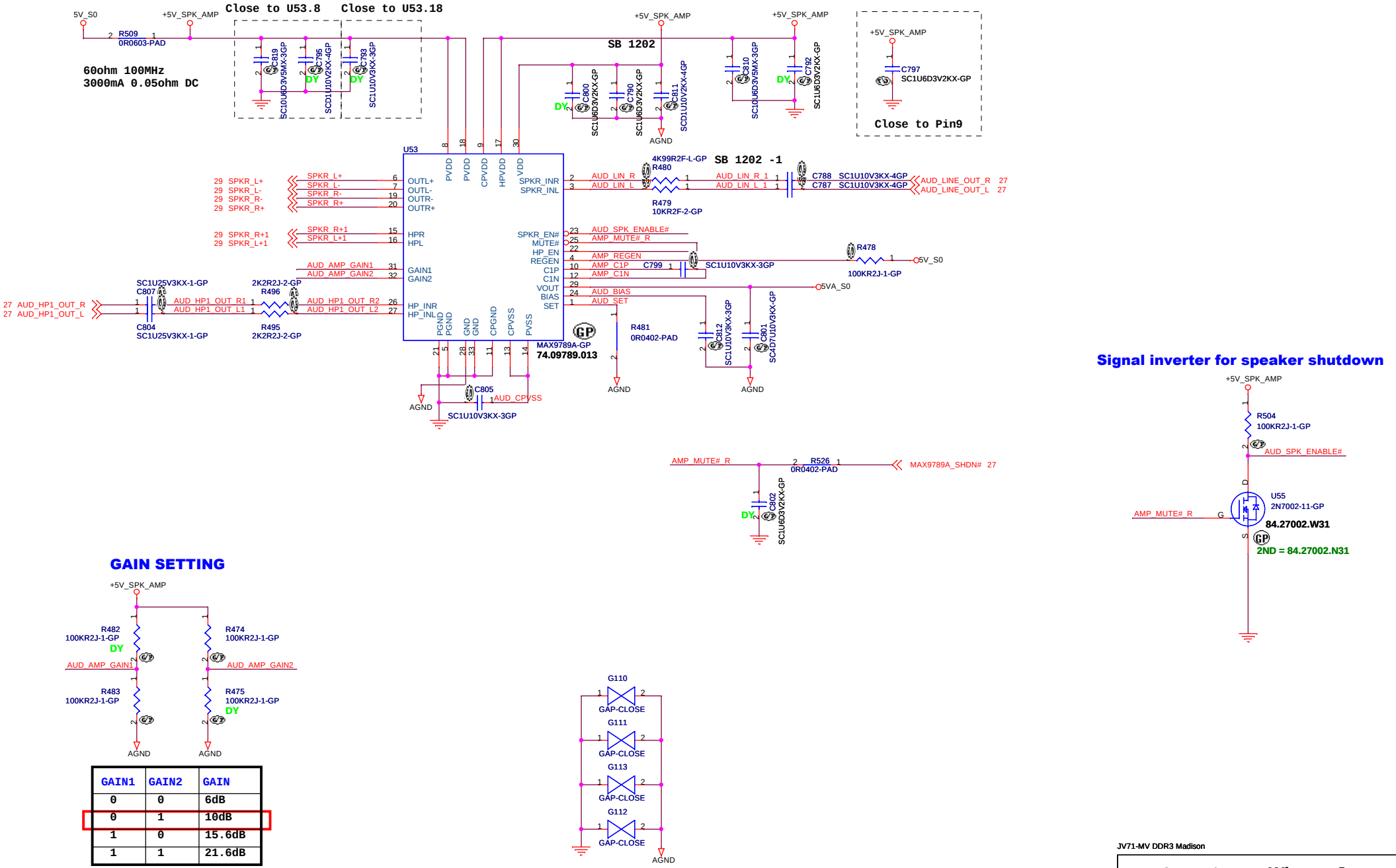

EMI
near R549
DVDD_IO
C835
SCD1U50V3KX-GP
DY
G129
GAP-CLOSE
AUD_AGND
DVDD_IO
0R3J-0-U-GP
0R3J-0-U-GP
UMA
DIS
R519
R516
1D5V_S0
3D3V_S0
3D3V_S0
C843
SC10U10V5ZY-1GP
C849
SCD1U50V3KX-GP
DY
AUD_AGND
AUD_AGND
C859
SCD1U50V3KX-GP
DY
AUD_AGND
C858
SCD1U50V3KX-GP
DY
5VA_S0
"VAUX" Pull high to enable standby mode
C855
SC10U10V5ZY-1GP
C825
SCD1U10V2KX-4GP
AUD_AGND
AUD_AGND
3D3V_S0
KBC_BEEP_1
RN80
SRN47K-2-GP-U
AUDIO_BEEP
C831
SC1U10V3KX-3GP
AUDIP_PC_BEEP
C844
SCD1U10V2KX-4GP
R514
1K91R2F-1-GP
C829
SC100P50V2JN-3GP
C832
DY
SC22P50V2JN-4GP
RESET#
BCLK
R515
0R0402-PAD
R517
0R0402-PAD
ACZ_RST#_AUDIO
ACZ_SYNC_AUDIO
ACZ_BITCLK_AUDIO
34 KBC_BEEP
SCD47U16V3ZY-3GP
C830
13 ACZ_SPKR
SCD47U16V3ZY-3GP
C827
SPKR_SB_1
C837
DY
SC22P50V2JN-4GP
ALC268_SENSE
C833
DY
SC22P50V2JN-4GP
R512
39K2R2F-L-GP
R511
10KR2F-2-GP
R510
20KR2F-L-GP
LINEOUT_JD#
LINEIN_JD#
MIC_JD#
Sense resistors need close codec
U57
ALC888S
DVDD
DVDD_IO
AVDD1
AVDD2
BEEP
RESET#
SYNC
BCLK
AGPIO
LFE
CENTER
SENSE_B
SENSE_A
29 LINE_IN_L
29 LINE_IN_R
SC4D7U10V3KX-GP
C818
C824
ALC861_LINE_IN_L
ALC861_LINE_IN_R
LINE1_L
LINE1_R
LINE2_L
LINE2_R
LINE1_VREFO
LINE2_VREFO
SDATA_OUT
SDATA_IN
AC97_DATIN
R518
39R2J-L-GP
ACZ_SDATAOUT_AUDIO
ACZ_SDATAIN0
SPDIFO1
SPDIFI/EAPD
AUD_SPDIF_OUT
ALC_EAPD
AUD_SPDIF_OUT
SIDESURR_L
SIDESURR_R
SURR_L
SURR_R
AUD_HP1_OUT_L
AUD_HP1_OUT_R
FRONT_L
FRONT_R
AUD_LINE_OUT_L
AUD_LINE_OUT_R
18 INT_MIC1
29 AUD_MICIN_L
29 AUD_MICIN_R
RN77
SRN75J-1-GP
INT_MIC1_R
AUD_MIC_L
AUD_MIC_R
SC4D7U10V3KX-GP
C821
C820
C823
C822
MIC1-L_PORT-B
MIC1-R_PORT-B
MIC2-L_PORT-B
MIC2-R_PORT-B
MIC1_L
MIC1_R
MIC2_L
MIC2_R
RN79
SRN2K2J-2-GP
MIC1V_R
MIC1V_L
MIC2V
MIC1_VREFO_R
MIC1_VREFO_L
MIC2_VREFO
C840
C834
SC4D7U10V2ZY-3GP
SC4D7U10V2ZY-3GP
AUD_AGND
AUD_AGND
AVSS1
AVSS2
DVSS
DVSS
VREF
JDREF
PIN37_VREFO
GPIO0/DMIC_CLK/SPDIFO2
GPIO1/DMIC_DATA
CD_L
CD_R
CD_GND
ALC888S-VC2-GR-GP
71.00888.D0G
DMIC_CLK
SPDIF_GPU
TP211 TPAD14-GP
TP227 TPAD14-GP
TPAD14-GP TP212
1DMIC_DAT
VREF
JDREF
MONO-OUT
TP216 TPAD14-GP
C826
DY
SC10U10V5ZY-1GP
C828
SCD47U16V3ZY-3GP
R524
20KR2F-L-GP
SA 4.10
AUD_AGND
AUD_AGND
ALC_EAPD
PM_SLP_S3# 13,33,34,38,43,45,48,51
AMP_SHUTDOWN# 34
R523
0R2J-2-GP
D32
BAW56-3-GP
D34
BAW56-3-GP
DY
DY
83.00056.K11
83.00056.K11
2ND = 83.00056.E11
2ND = 83.00056.E11
28 MAX9789A_SHDN#
R527
10KR2J-3-GP
3D3V_S0
DY
R557
10KR2J-3-GP
JV71-MV DDR3 Madison
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Azalia codec ALC888
Size
A3
Document Number
JV71-MV DDR3 Madison
Rev
-1
Date: Wednesday, October 28, 2009
Sheet 27 of 62



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

JV71-MV DDR3 Madison

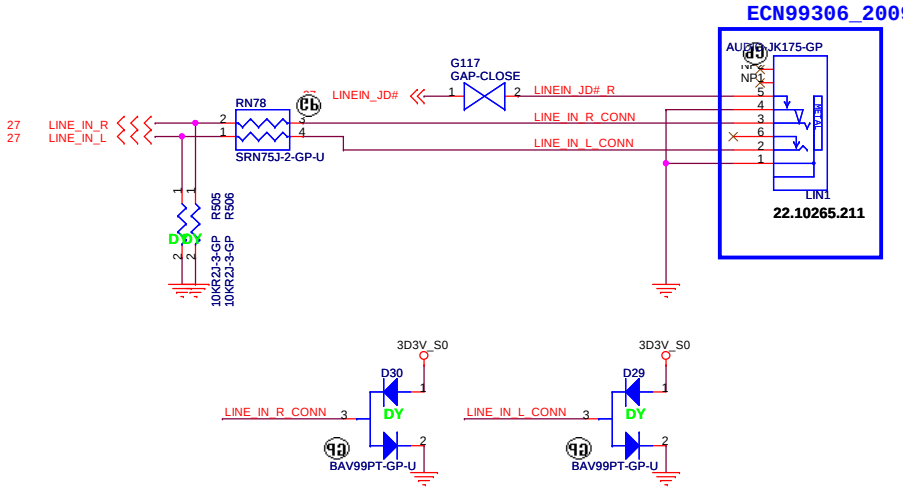
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP

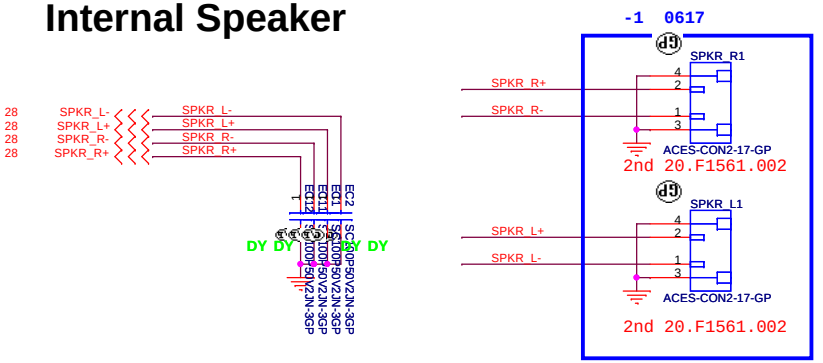
Size | Document Number: JV71-MV DDR3 Madison | Rev: -1

Date: Wednesday, October 28, 2009 | Sheet 28 of 62

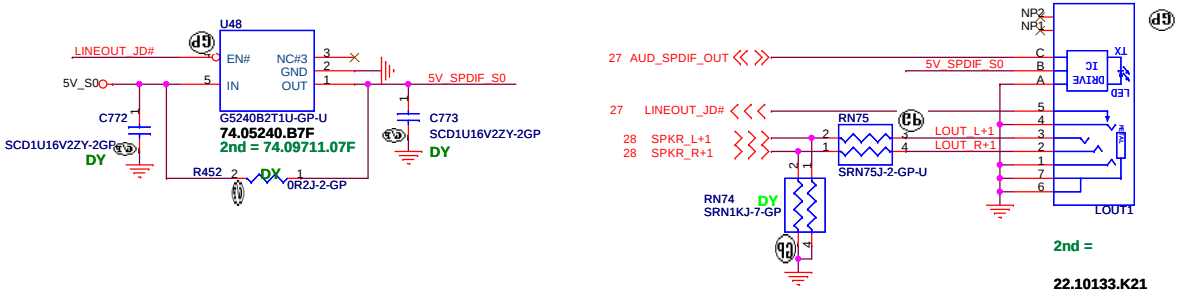
LINE IN

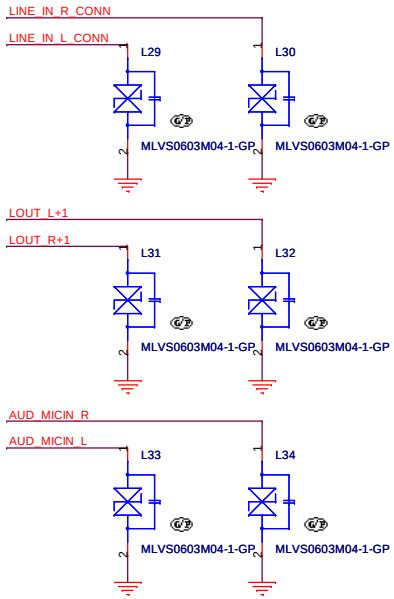


Internal Speaker

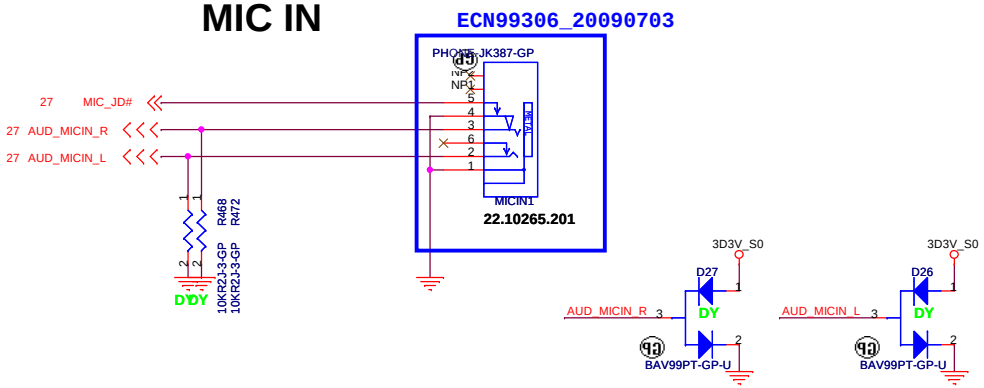


LINE OUT





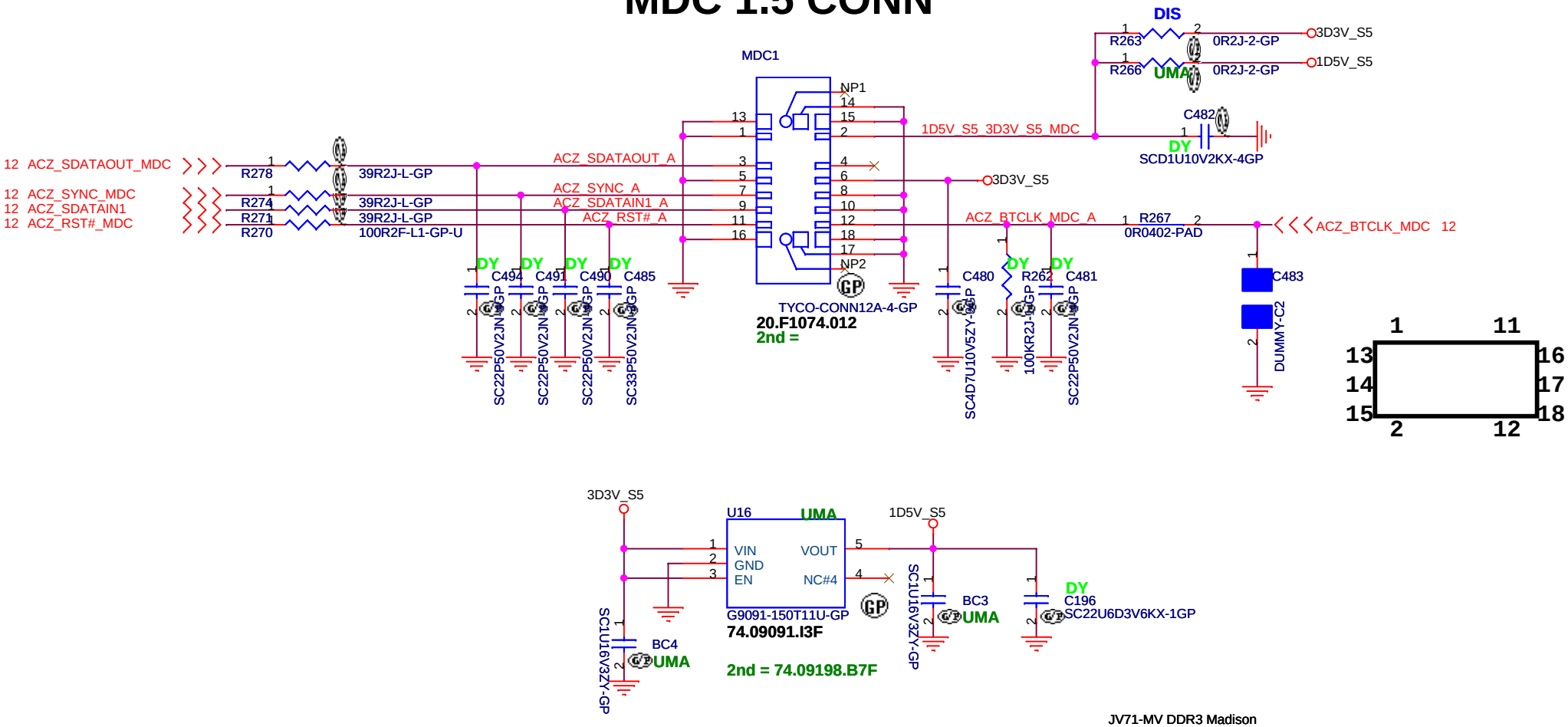
MIC IN



JV71-MV DDR3 Madison

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*AUDIO jack*	
Size	Document Number JV71-MV DDR3 Madison	Rev -1
Date: Wednesday, October 28, 2009	Sheet 29 of 62	

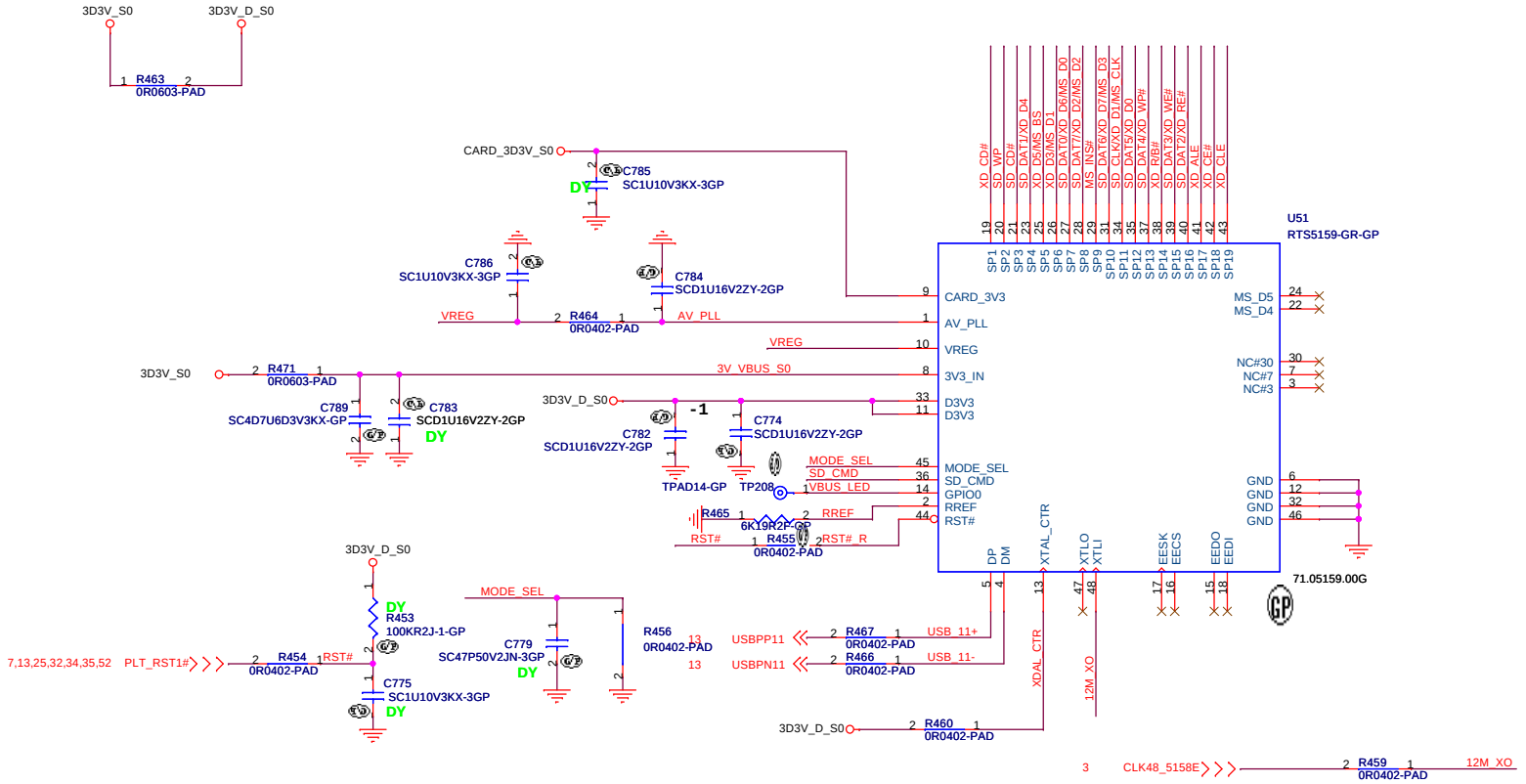
MDC 1.5 CONN



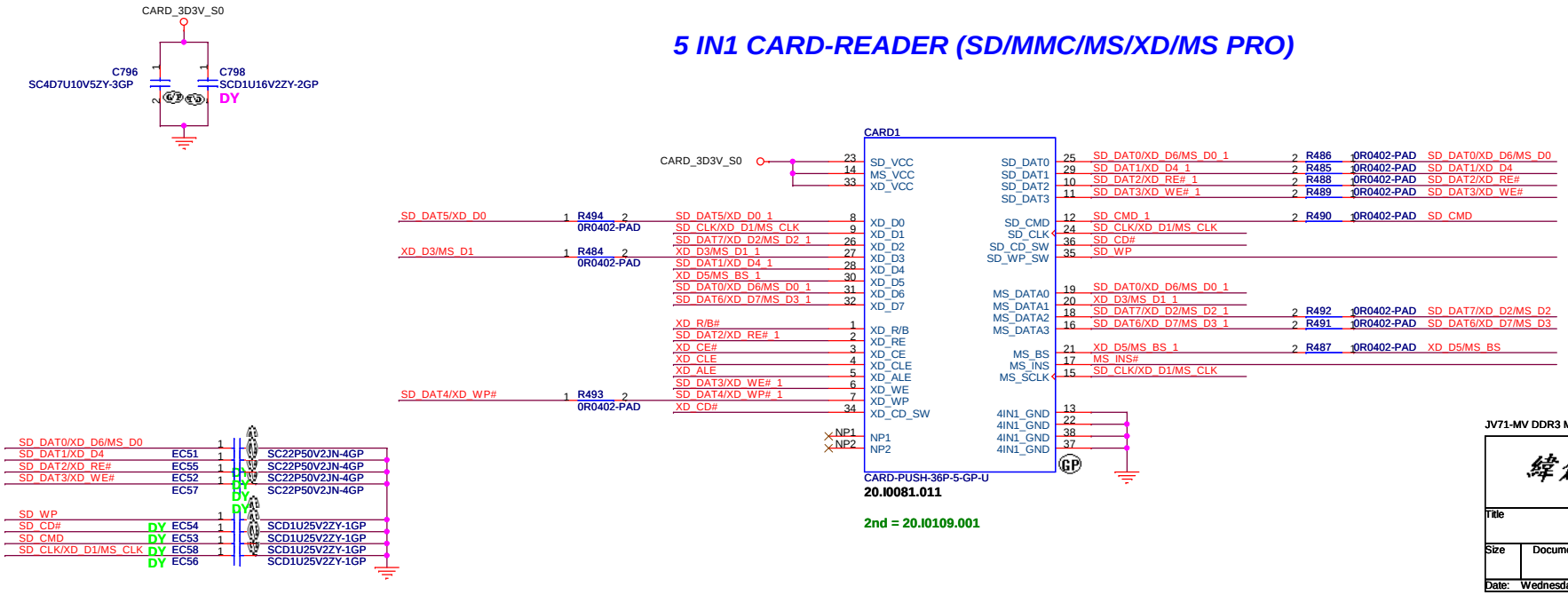
JV71-MV DDR3 Madison

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MDC	
Size	Document Number: JV71-MV DDR3 Madison	Rev: -1
Date: Wednesday, October 28, 2009	Sheet 30 of 62	



5 IN1 CARD-READER (SD/MMC/MS/XD/MS PRO)

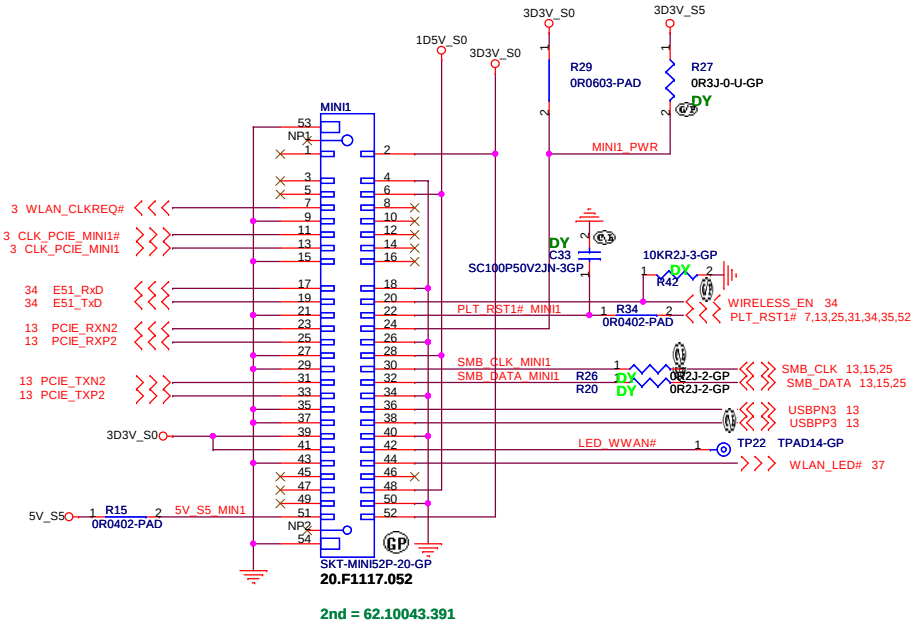


JV71-MV DDR3 Madison

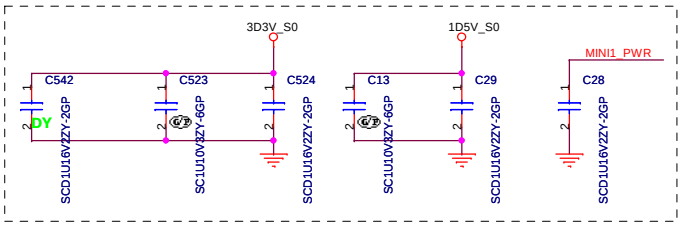
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Cardreader RTS5159*	
Size	Document Number: JV71-MV DDR3 Madison	Rev: -1
Date: Wednesday, October 28, 2009	Sheet 31 of 62	

Mini Card Connector(WLAN)
Support debug-card



Place near MINI1



Mini Card Connector

JV71-MV DDR3 Madison

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD**

Size	Document Number	Rev
A3	JV71-MV DDR3 Madison	-1

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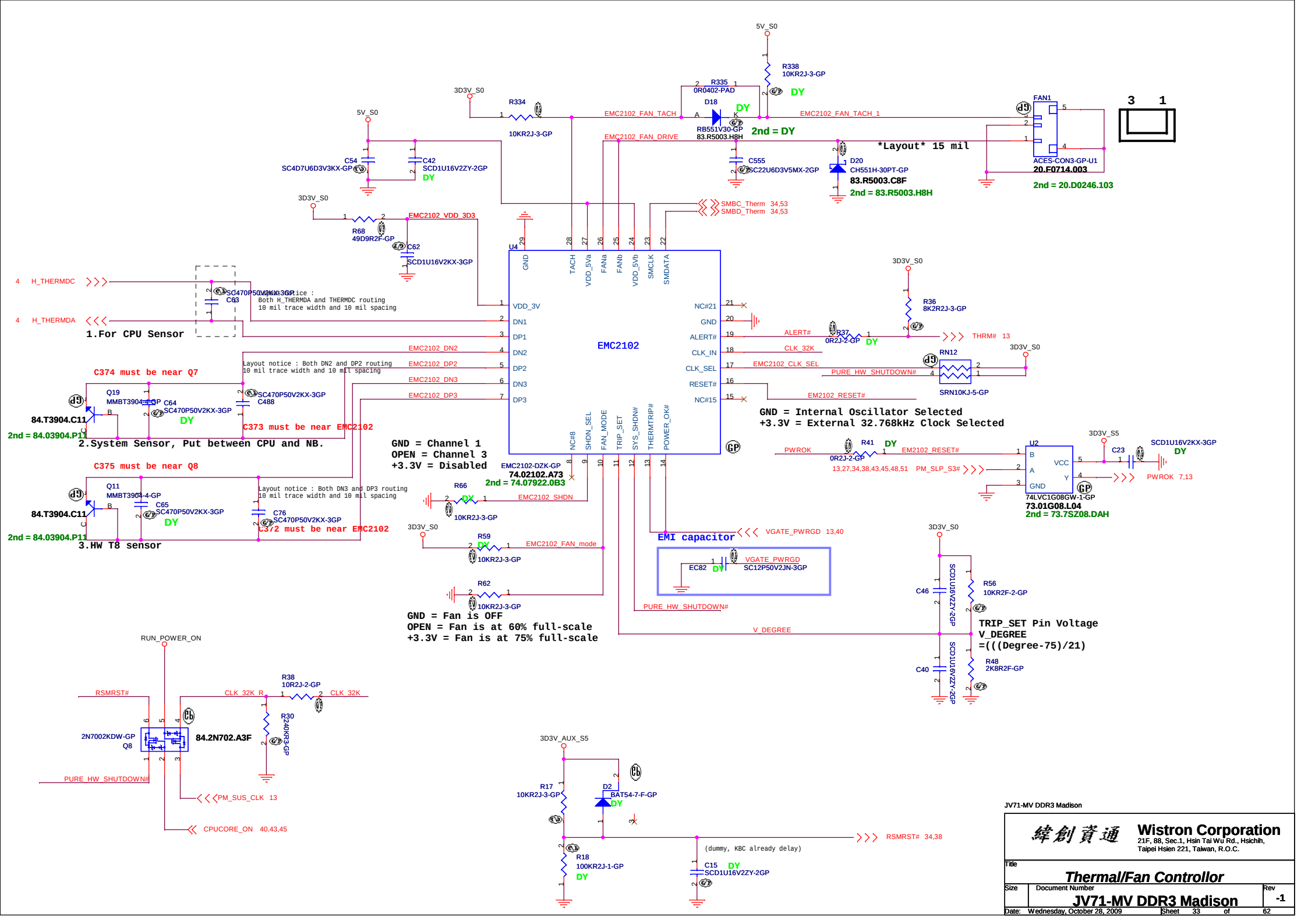

JV71-MV DDR3 Madison

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

Size	Document Number	Rev
	JV71-MV DDR3 Madison	-1

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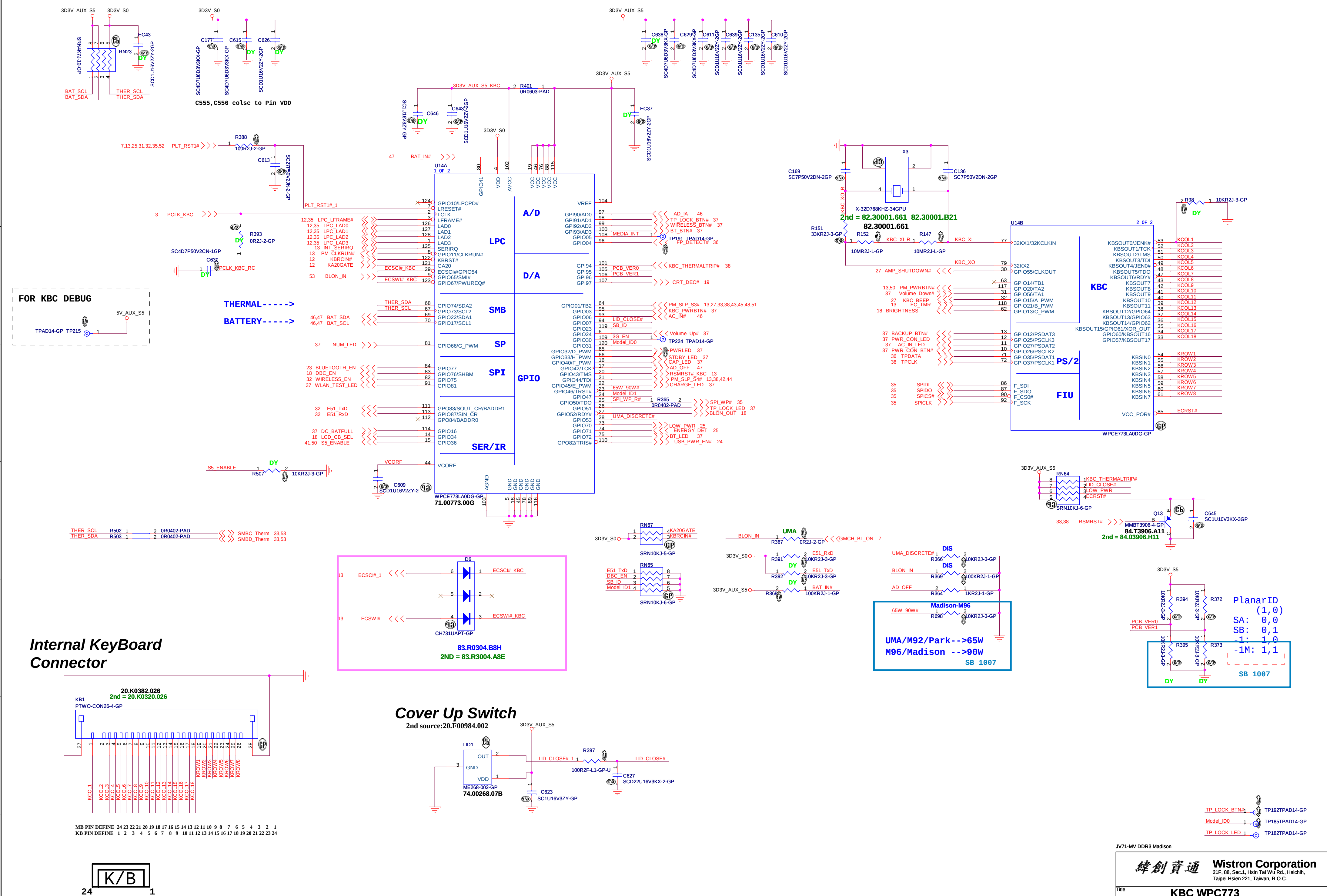
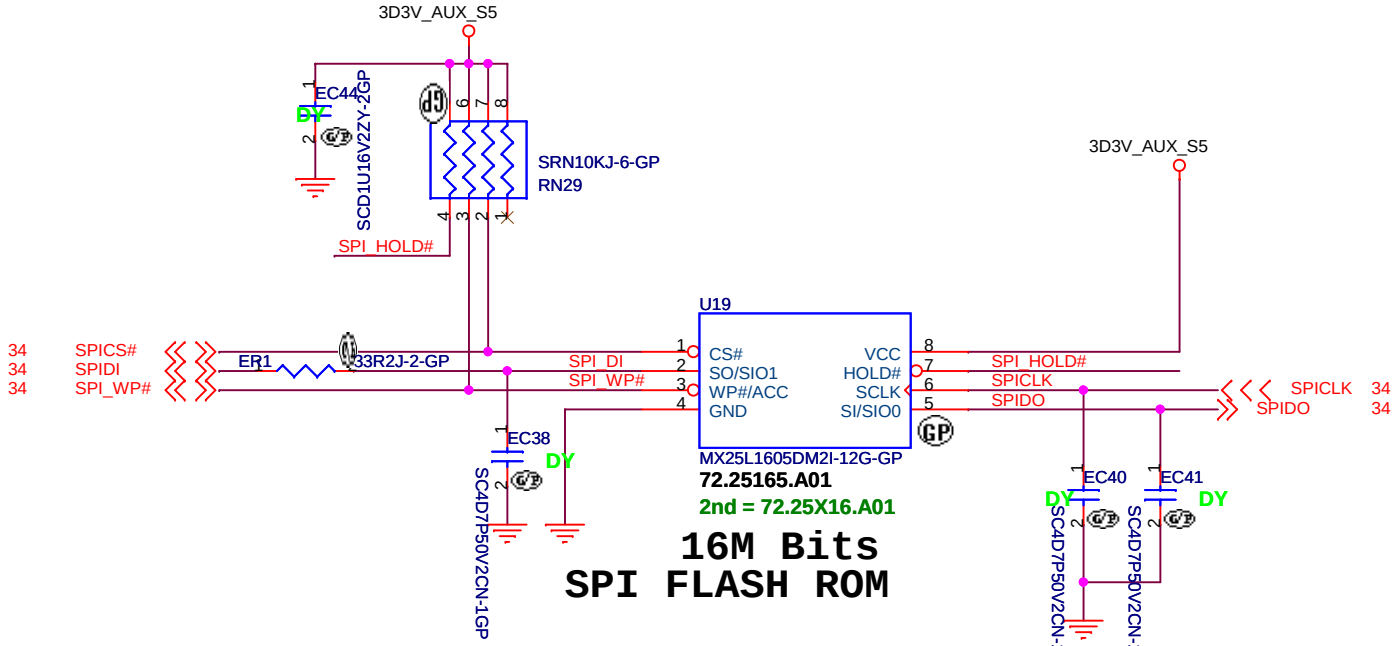


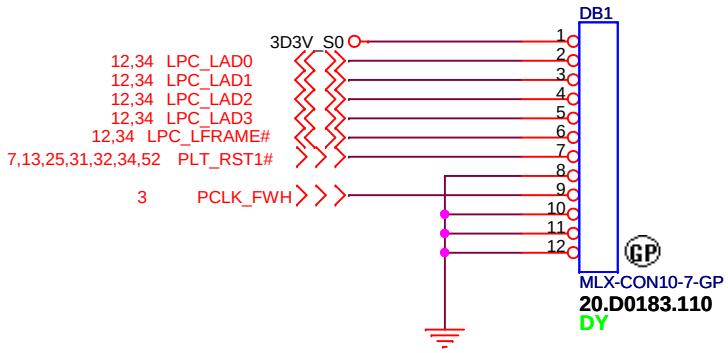
JV71-MV DDR3 Madison

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	KBC WPC773	
Size A2	Document Number JV71-MV DDR3 Madison	Rev -1
Date: Wednesday, October 28, 2009	Sheet 34 of 62	



GOLDEN FINGER FOR DEBUG BOARD



JV71-MV DDR3 Madison

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BIOS***	
Size	Document Number **JV71-MV DDR3 Madison**	Rev -1
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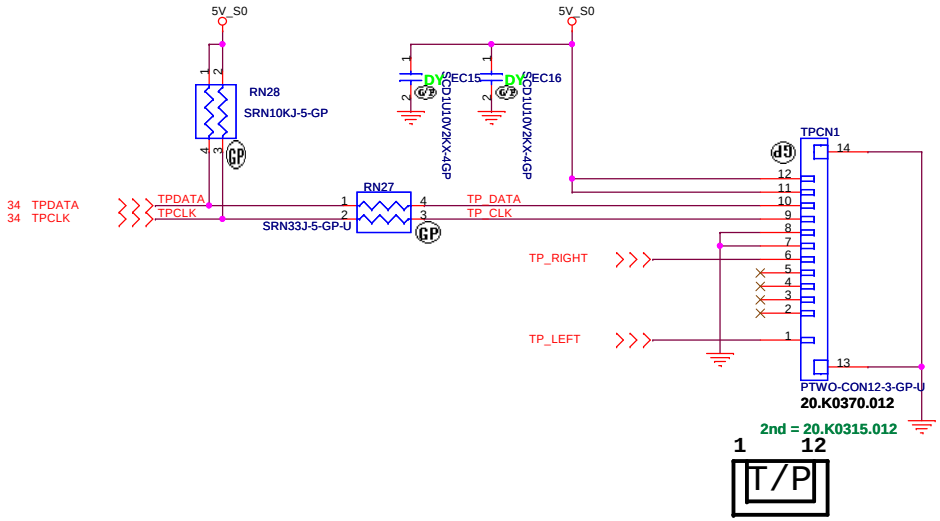
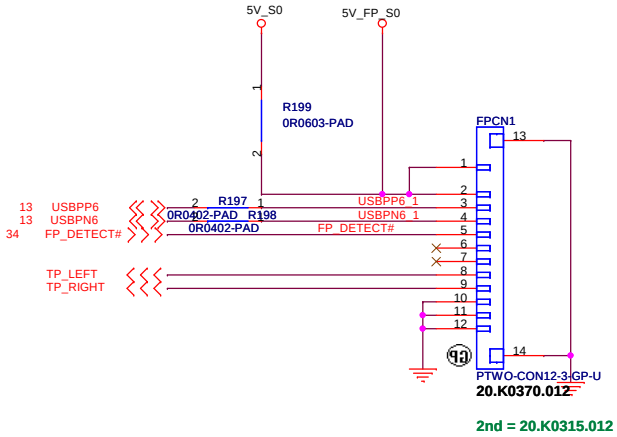
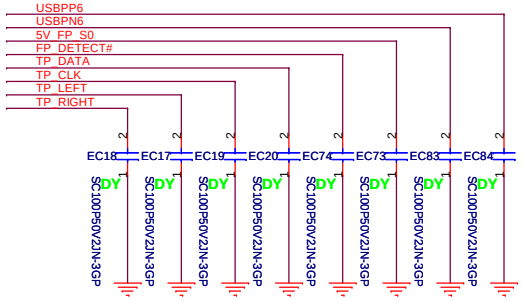
TOUCH PAD



Finger printer





JV71-MV DDR3 Madison

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Touch PAD and FP
Size / Document Number	JV71-MV DDR3 Madison
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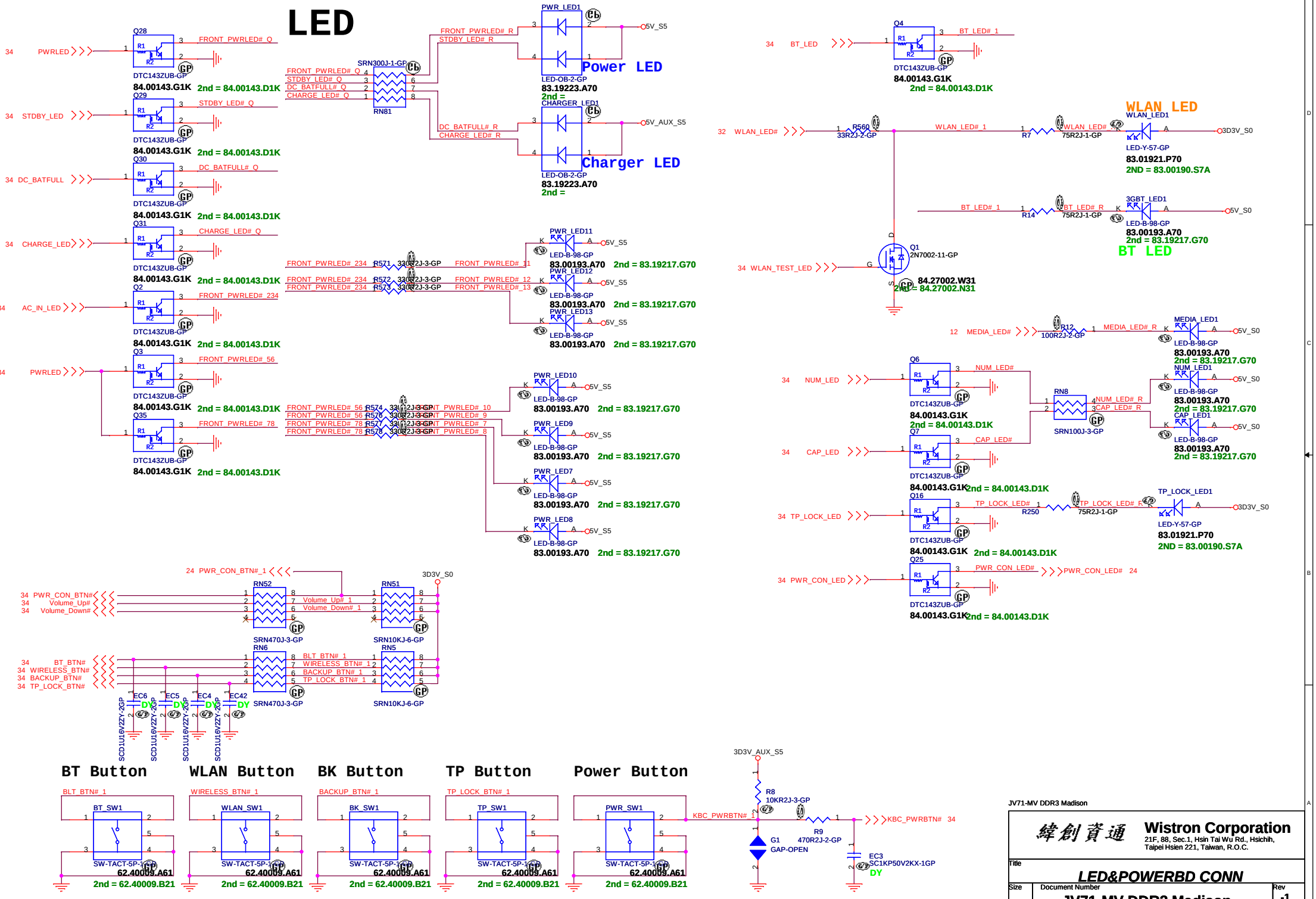
LED


Power LED
Charger LED
WLAN LED
BT LED
Q28
Q29
Q30
Q31
Q2
Q3
Q35
Q4
Q1
Q6
Q7
Q16
Q25
PWR_LED1
CHARGER_LED1
PWR_LED11
PWR_LED12
PWR_LED13
PWR_LED10
PWR_LED9
PWR_LED7
PWR_LED8
WLAN_LED1
3GBT_LED1
MEDIA_LED1
NUM_LED1
CAP_LED1
TP_LOCK_LED1
RN52
RN51
RN6
RN5
RN8
BT Button
WLAN Button
BK Button
TP Button
Power Button
BT_SW1
WLAN_SW1
BK_SW1
TP_SW1
PWR_SW1
R8
R9
G1
EC3
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
JV71-MV DDR3 Madison
LED&POWERBD CONN
Size
Document Number
JV71-MV DDR3 Madison
Rev
-1
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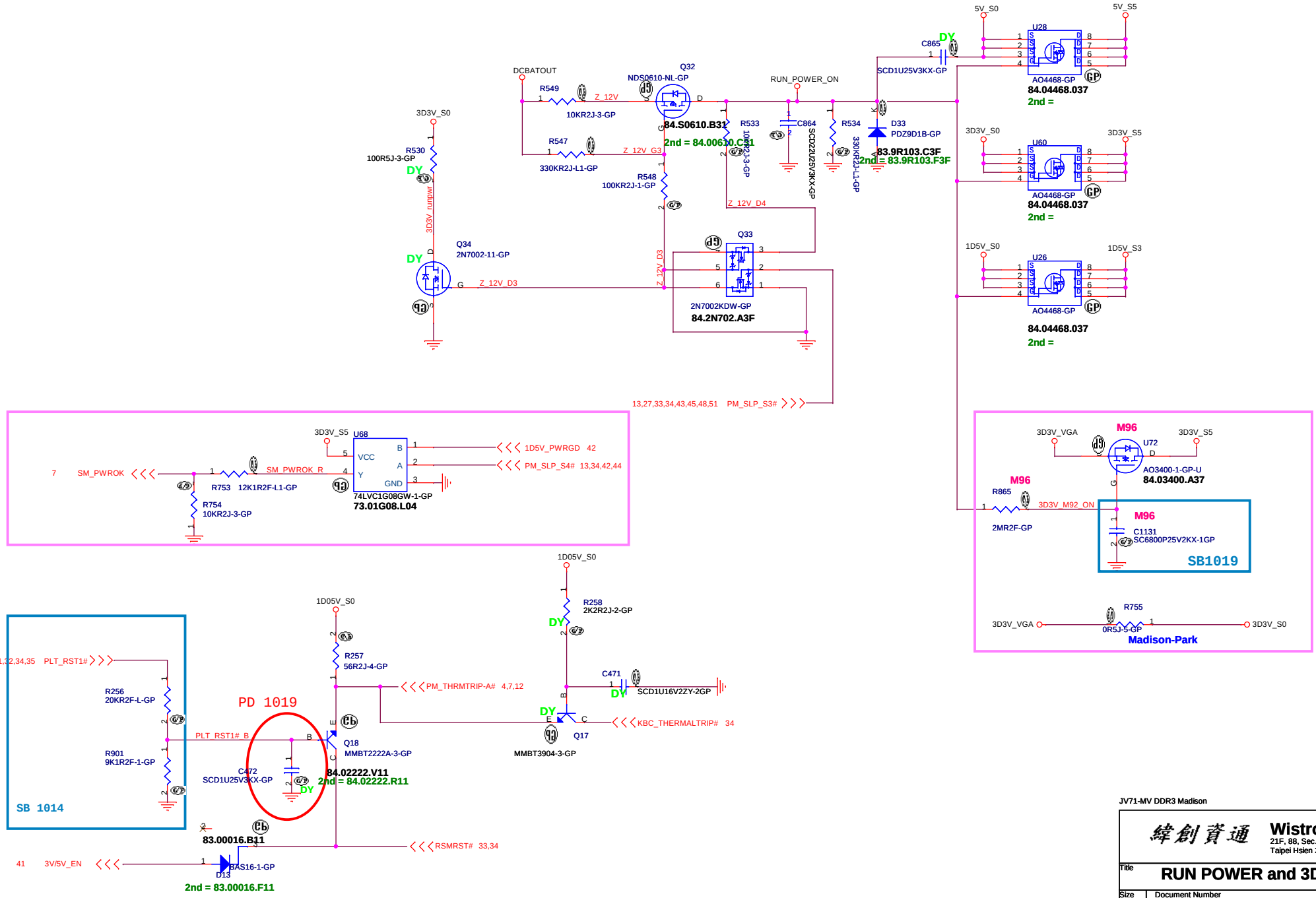
Run Power



JV71-MV DDR3 Madison

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

Size	Document Number	Rev
	JV71-MV DDR3 Madison	-1

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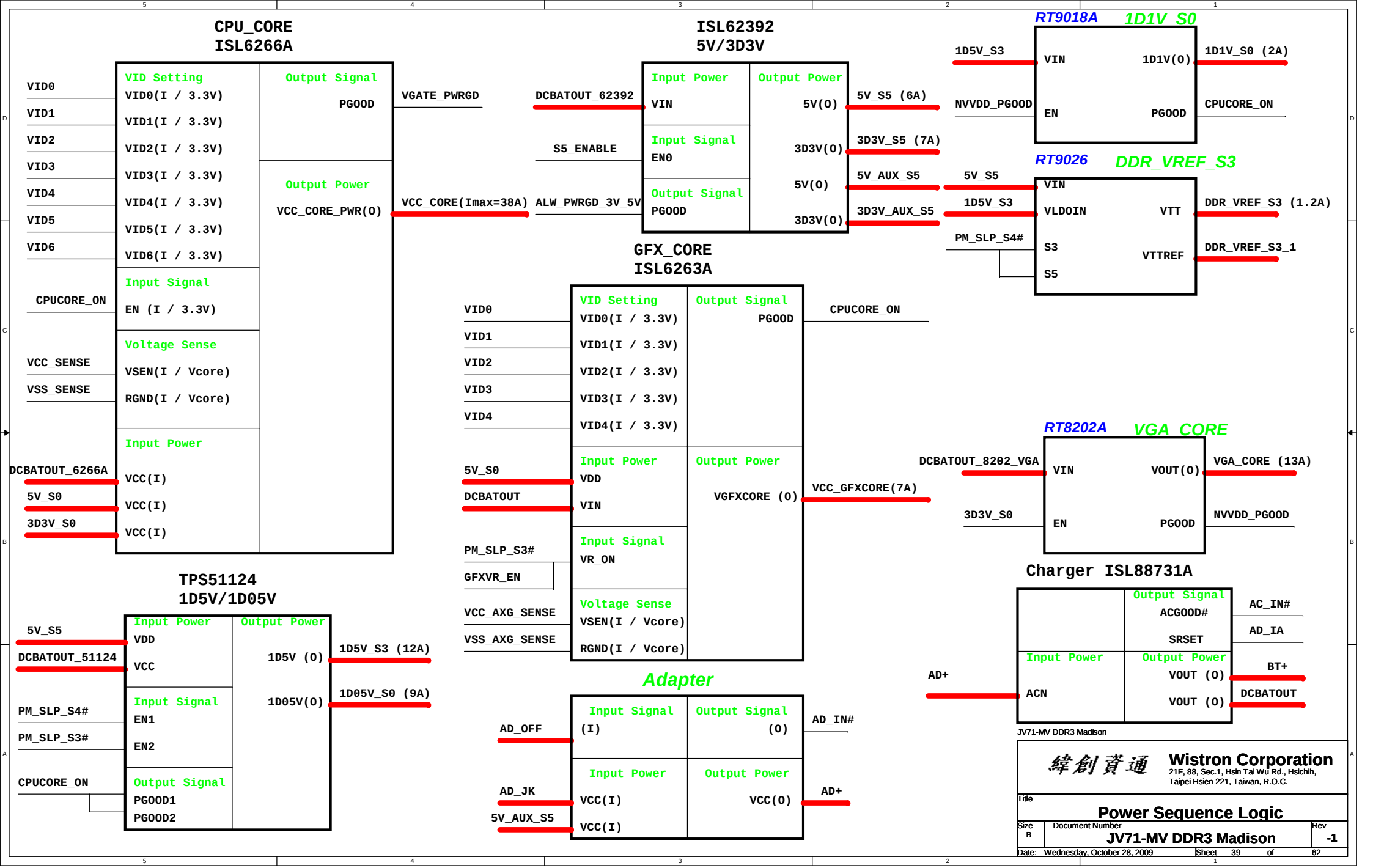
CPU_CORE
ISL6266A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)
Input Signal
EN (I / 3.3V)
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)
Output Signal
PGOOD
Output Power
VCC_CORE_PWR(O)
VID0
VID1
VID2
VID3
VID4
VID5
VID6
CPUCORE_ON
VCC_SENSE
VSS_SENSE
DCBATOUT_6266A
5V_S0
3D3V_S0
VGATE_PWRGD
VCC_CORE(Imax=38A)
ISL62392
5V/3D3V
Input Power
VIN
Input Signal
EN0
Output Signal
PGOOD
Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)
DCBATOUT_62392
S5_ENABLE
ALW_PWRGD_3V_5V
5V_S5 (6A)
3D3V_S5 (7A)
5V_AUX_S5
3D3V_AUX_S5
RT9018A
1D1V_S0
VIN
EN
1D1V(O)
PGOOD
1D5V_S3
NVVDD_PGOOD
1D1V_S0 (2A)
CPUCORE_ON
RT9026
DDR_VREF_S3
VIN
VLDOIN
S3
S5
VTT
VTTREF
5V_S5
1D5V_S3
PM_SLP_S4#
DDR_VREF_S3 (1.2A)
DDR_VREF_S3_1
GFX_CORE
ISL6263A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
Input Power
VDD
VIN
Input Signal
VR_ON
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Output Signal
PGOOD
Output Power
VGFXCORE (O)
VID0
VID1
VID2
VID3
VID4
5V_S0
DCBATOUT
PM_SLP_S3#
GFXVR_EN
VCC_AXG_SENSE
VSS_AXG_SENSE
CPUCORE_ON
VCC_GFXCORE(7A)
RT8202A
VGA_CORE
VIN
EN
VOUT(O)
PGOOD
DCBATOUT_8202_VGA
3D3V_S0
VGA_CORE (13A)
NVVDD_PGOOD
TPS51124
1D5V/1D05V
Input Power
VDD
VCC
Input Signal
EN1
EN2
Output Signal
PGOOD1
PGOOD2
Output Power
1D5V (O)
1D05V(O)
5V_S5
DCBATOUT_51124
PM_SLP_S4#
PM_SLP_S3#
CPUCORE_ON
1D5V_S3 (12A)
1D05V_S0 (9A)
Adapter
Input Signal
(I)
Input Power
VCC(I)
VCC(I)
Output Signal
(O)
Output Power
VCC(O)
AD_OFF
AD_JK
5V_AUX_S5
AD_IN#
AD+
Charger ISL88731A
Output Signal
ACGOOD#
SRSET
Input Power
ACN
Output Power
VOUT (O)
VOUT (O)
AD+
AC_IN#
AD_IA
BT+
DCBATOUT
JV71-MV DDR3 Madison
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power Sequence Logic
Size
B
Document Number
JV71-MV DDR3 Madison
Rev
-1
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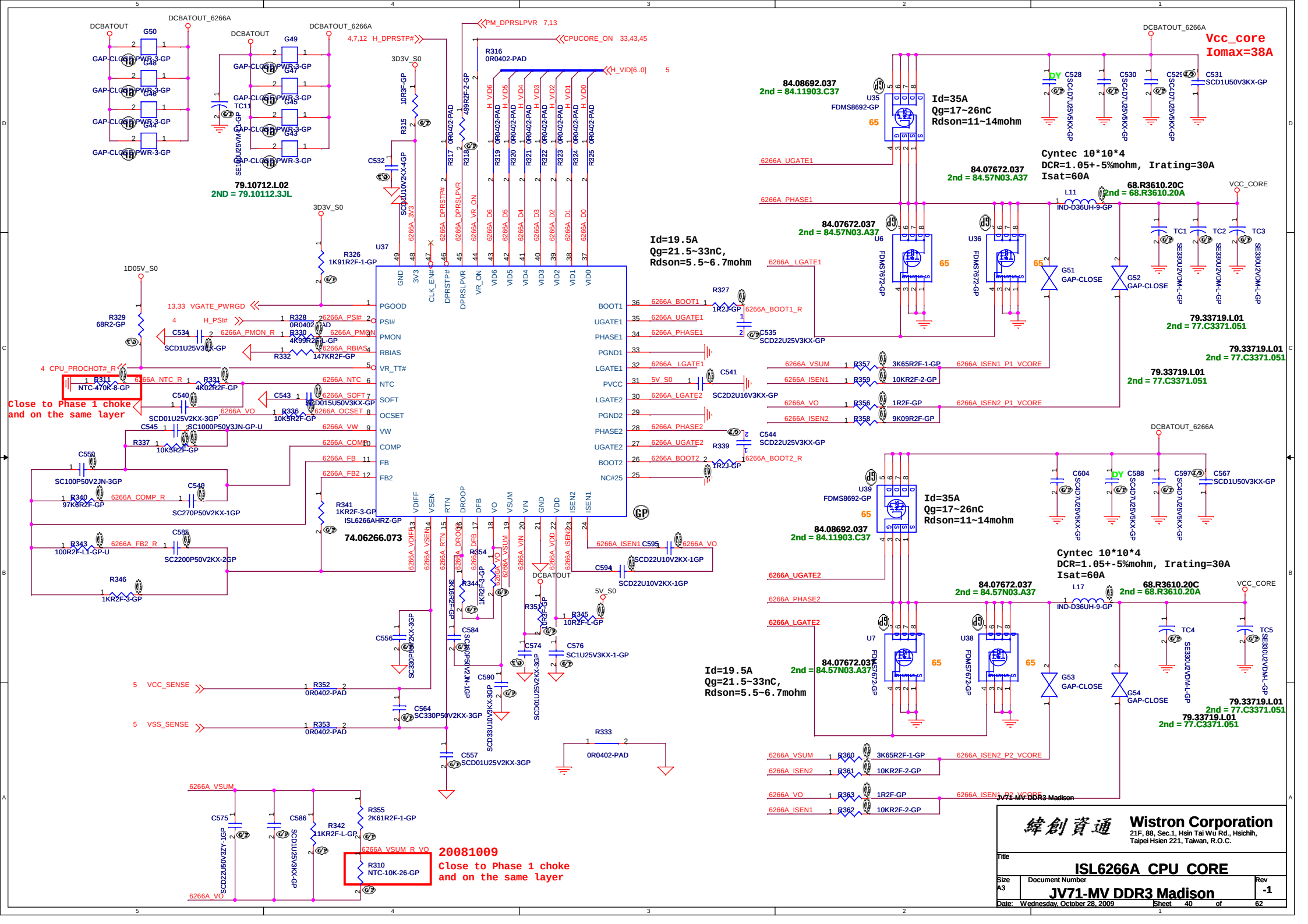
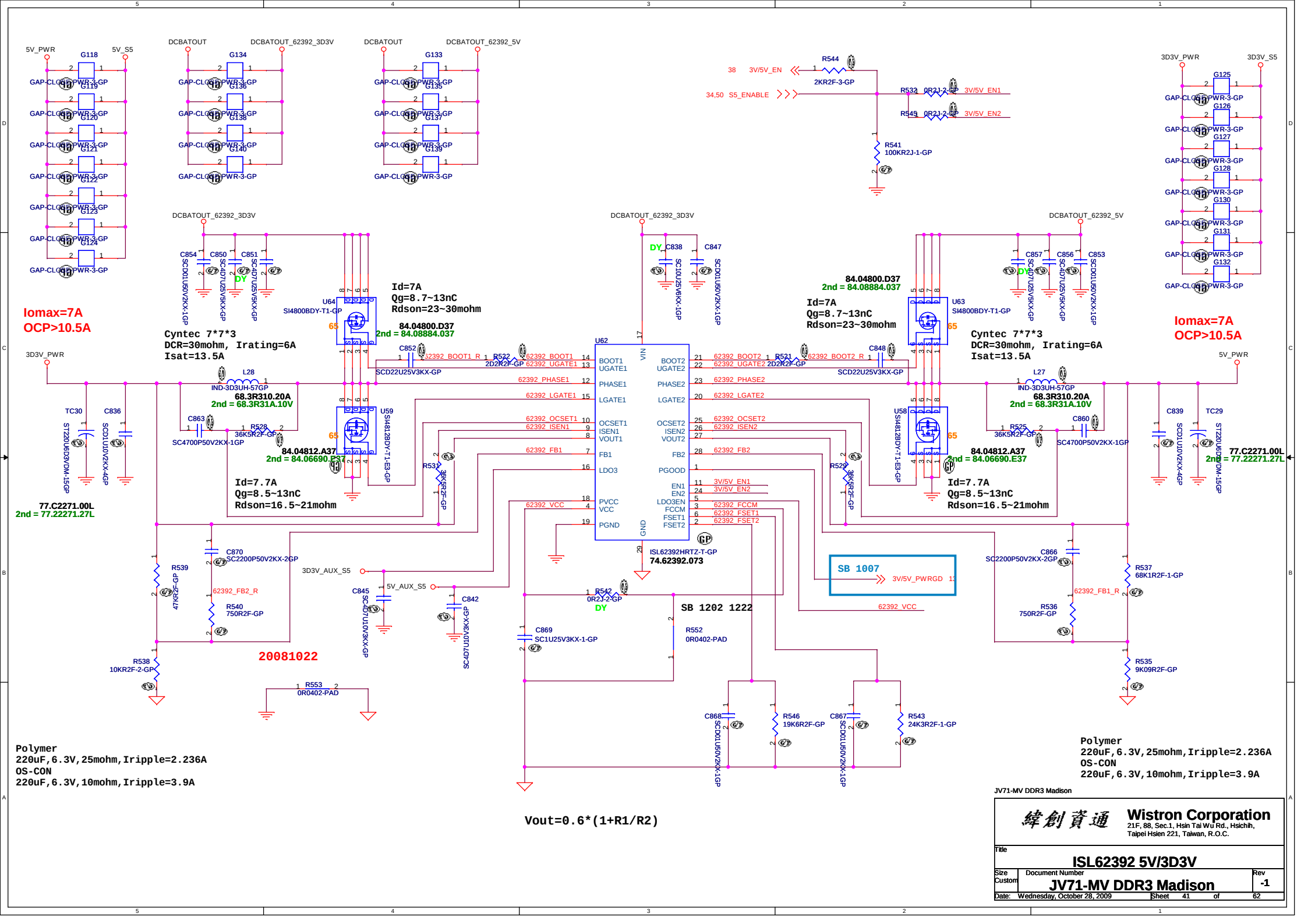
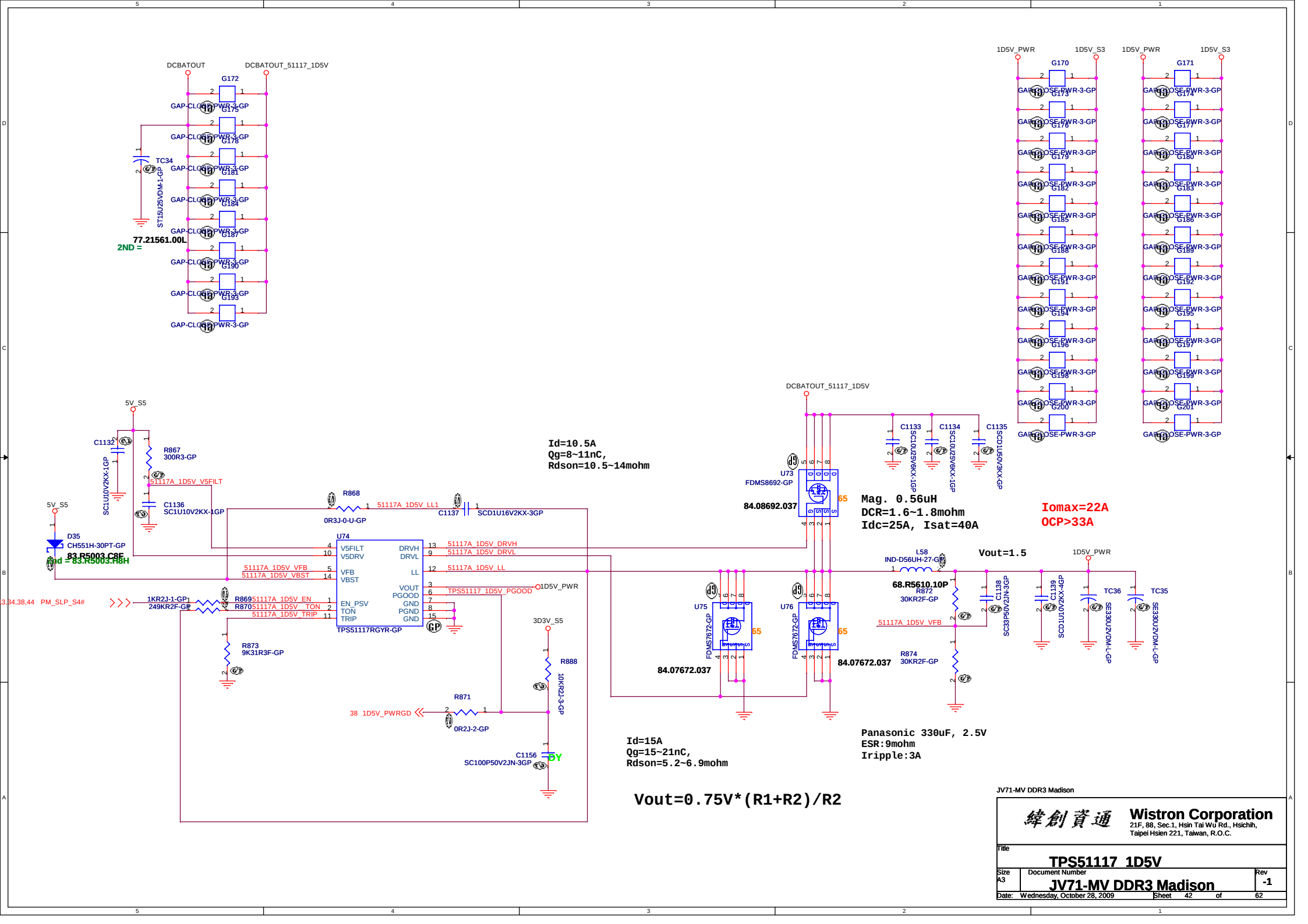
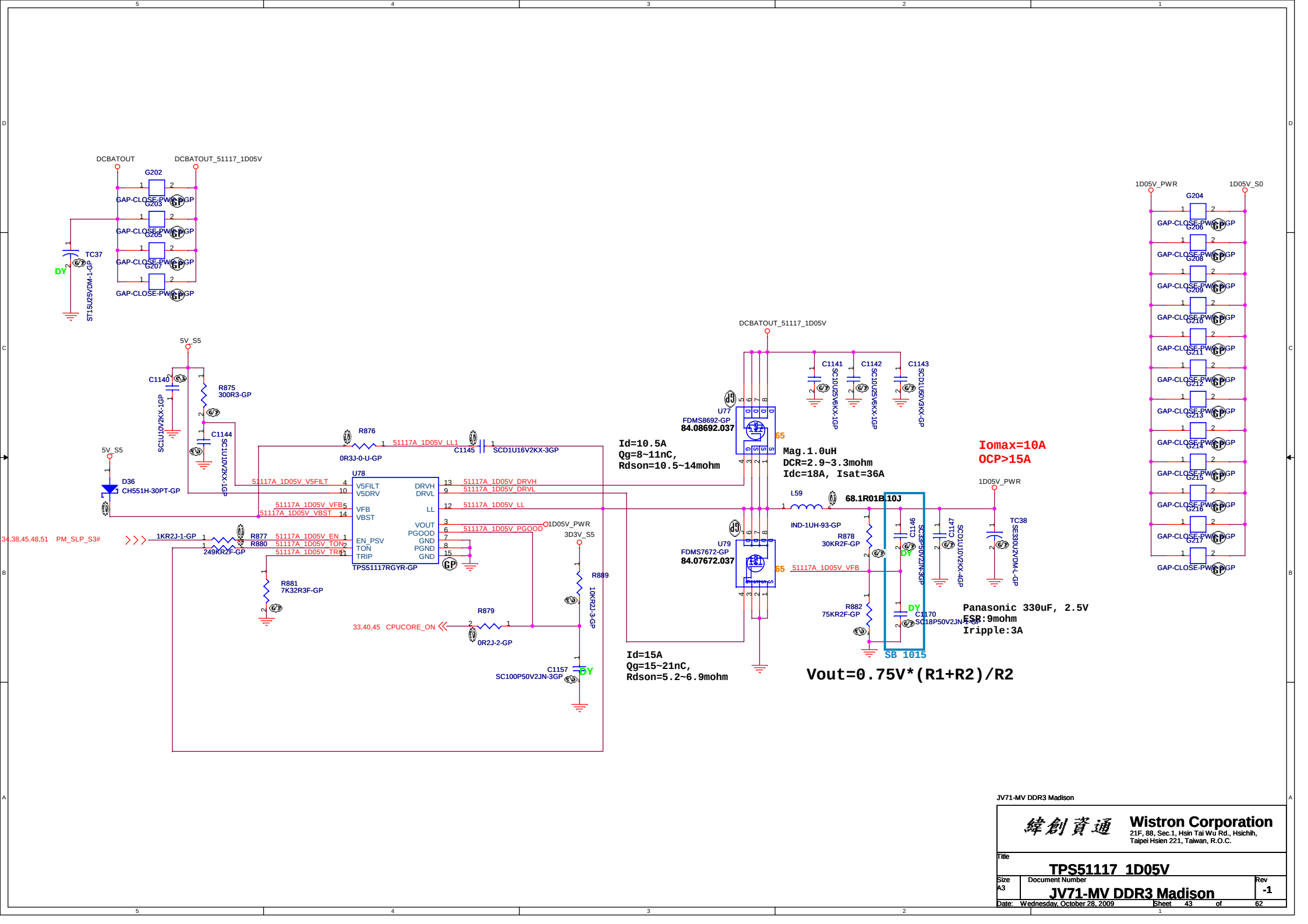
Sheet 39 of 62


Vcc_core
Iomax=38A
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
ISL6266AHRZ-GP
74.06266.073
Close to Phase 1 choke
and on the same layer
20081009
Close to Phase 1 choke
and on the same layer
JV71-MV DDR3 Madison
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6266A_CPU_CORE
JV71-MV DDR3 Madison
Wednesday, October 28, 2009


5V_PWR
5V_S5
DCBATOUT
DCBATOUT_62392_3D3V
DCBATOUT_62392_5V
3D3V_PWR
3D3V_S5
G118
G119
G120
G121
G122
G123
G124
G134
G135
G136
G137
G138
G139
G140
G133
G125
G126
G127
G128
G130
G131
G132
GAP-CLOSE-PWR-3-GP
R544
2KR2F-3-GP
38 3V/5V_EN
34,50 S5_ENABLE
R532 0R2J-2-GP 3V/5V_EN1
R545 0R2J-2-GP 3V/5V_EN2
R541
100KR2J-1-GP
Iomax=7A
OCP>10.5A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
84.04800.D37
2nd = 84.08884.037
U64
SI4800BDY-T1-GP
U63
U62
U59
U58
SI4812BDY-T1-E3-GP
ISL62392HRTZ-T-GP
74.62392.073
L28
L27
IND-3D3UH-57GP
68.3R310.20A
2nd = 68.3R31A.10V
84.04812.A37
2nd = 84.06690.E37
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
77.C2271.00L
2nd = 77.22271.27L
TC30
TC29
C836
C839
C863
C860
R528
36K5R2F-GP
R525
R531
R529
C852
C848
R522
R521
62392_BOOT1_R
62392_BOOT2_R
62392_BOOT1
62392_BOOT2
62392_UGATE1
62392_UGATE2
62392_PHASE1
62392_PHASE2
62392_LGATE1
62392_LGATE2
62392_OCSET1
62392_OCSET2
62392_ISEN1
62392_ISEN2
62392_FB1
62392_FB2
62392_VCC
62392_FCCM
62392_FSET1
62392_FSET2
3V/5V_EN1
3V/5V_EN2
BOOT1
UGATE1
PHASE1
LGATE1
OCSET1
ISEN1
VOUT1
FB1
LDO3
PVCC
VCC
PGND
BOOT2
UGATE2
PHASE2
LGATE2
OCSET2
ISEN2
VOUT2
FB2
PGOOD
EN1
EN2
LDO3EN
FCCM
FSET1
FSET2
VIN
GND
SB 1007
3V/5V_PWRGD
SB 1202 1222
R542
0R2J-2-GP
DY
R552
0R0402-PAD
R553
0R0402-PAD
C869
SC1U25V3KX-1-GP
C868
C867
R546
19K6R2F-GP
R543
24K3R2F-1-GP
SCD01U50V2KX-1GP
C870
SC2200P50V2KX-2GP
R539
47KR2F-GP
R540
750R2F-GP
R538
10KR2F-2-GP
62392_FB2_R
3D3V_AUX_S5
5V_AUX_S5
C845
C842
SC4D7U10V3KX-GP
20081022
C866
R537
68K1R2F-1-GP
R536
750R2F-GP
R535
9K09R2F-GP
62392_FB1_R
C857
C856
C853
C838
C847
C854
C850
C851
SCD01U50V2KX-1GP
SC4D7U25V5KX-GP
SC10U25V6KX-1GP
SCD22U25V3KX-GP
SC4700P50V2KX-1GP
SC4D7U10V3KX-4GP
SCD1U10V2KX-4GP
ST220U6D3VDM-15GP
Polymer
220uF,6.3V,25mohm,Iripple=2.236A
OS-CON
220uF,6.3V,10mohm,Iripple=3.9A
Vout=0.6*(1+R1/R2)
JV71-MV DDR3 Madison
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62392 5V/3D3V
Size
Custom
Document Number
JV71-MV DDR3 Madison
Rev
-1
Date: Wednesday, October 28, 2009
Sheet 41 of 62


DCBATOUT
DCBATOUT_51117_1D5V
G172
GAP-CLOSE-PWR-3-GP
TC34
ST15U25VDM-1-GP
77.21561.00L
2ND =
1D5V_PWR
1D5V_S3
G170
G171
5V_S5
C1132
SC1U10V2KX-1GP
R867
300R3-GP
51117A_1D5V_V5FILT
C1136
SC1U10V2KX-1GP
D35
CH551H-30PT-GP
83.R5003.C8F
2nd = 83.R5003.H8H
R868
0R3J-0-U-GP
51117A_1D5V_LL1
C1137
SCD1U16V2KX-3GP
U74
V5FILT
V5DRV
VFB
VBST
EN_PSV
TON
TRIP
DRVH
DRVL
LL
VOUT
PGOOD
GND
PGND
GND
TPS51117RGYR-GP
51117A_1D5V_DRVH
51117A_1D5V_DRVL
51117A_1D5V_LL
TPS51117_1D5V_PGOOD
1D5V_PWR
51117A_1D5V_VFB
51117A_1D5V_VBST
51117A_1D5V_EN
51117A_1D5V_TON
51117A_1D5V_TRIP
1KR2J-1-GP
249KR2F-GP
R869
R870
R873
9K31R3F-GP
3D3V_S5
R888
10KR2J-3-GP
R871
0R2J-2-GP
38 1D5V_PWRGD
C1156
SC100P50V2JN-3GP
Id=10.5A
Qg=8~11nC,
Rdson=10.5~14mohm
DCBATOUT_51117_1D5V
U73
FDMS8692-GP
84.08692.037
C1133
C1134
C1135
SCD1U25V9KX-1GP
SCD1U25V9KX-3GP
Mag. 0.56uH
DCR=1.6~1.8mohm
Idc=25A, Isat=40A
Iomax=22A
OCP>33A
U75
U76
FDMS7672-GP
84.07672.037
L58
IND-D56UH-27-GP
68.R5610.10P
Vout=1.5
R872
30KR2F-GP
R874
30KR2F-GP
C1138
SC33P50V2JN-3GP
C1139
SCD1U10V2KX-4GP
TC36
TC35
SE330U2VDM-L-GP
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
Panasonic 330uF, 2.5V
ESR:9mohm
Iripple:3A
Vout=0.75V*(R1+R2)/R2
JV71-MV DDR3 Madison
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51117 1D5V
Size
A3
Document Number
JV71-MV DDR3 Madison
Rev
-1
Date: Wednesday, October 28, 2009
Sheet 42 of 62



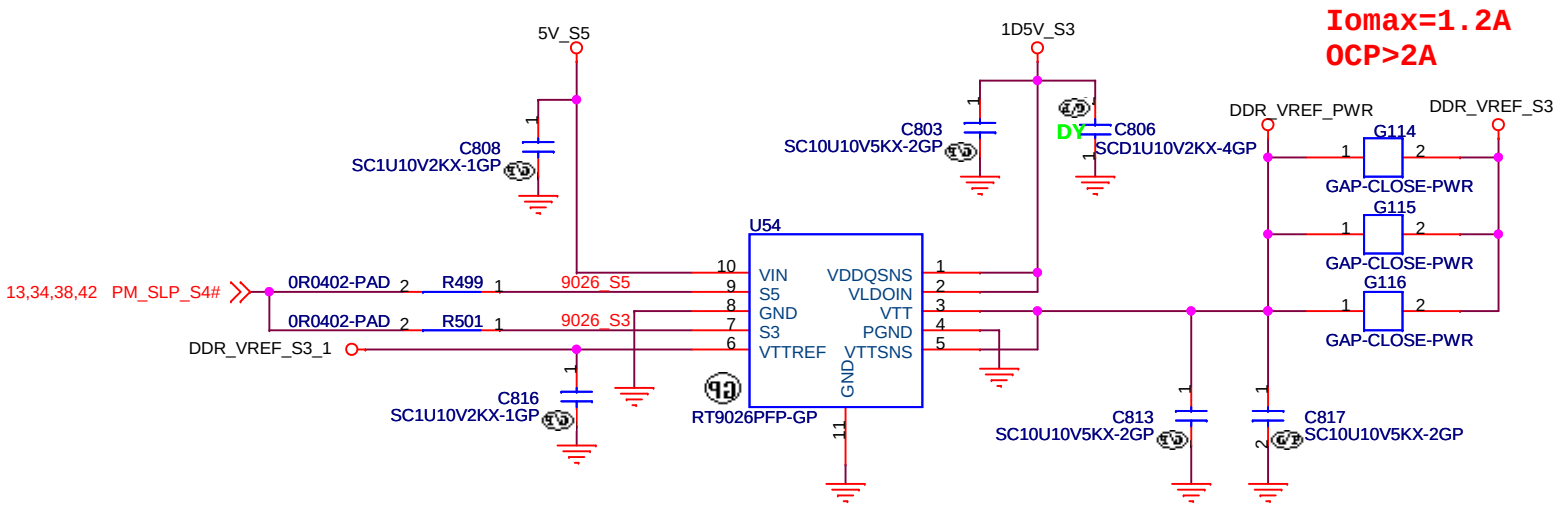
JV71-MV DDR3 Madison

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51117 1D05V**

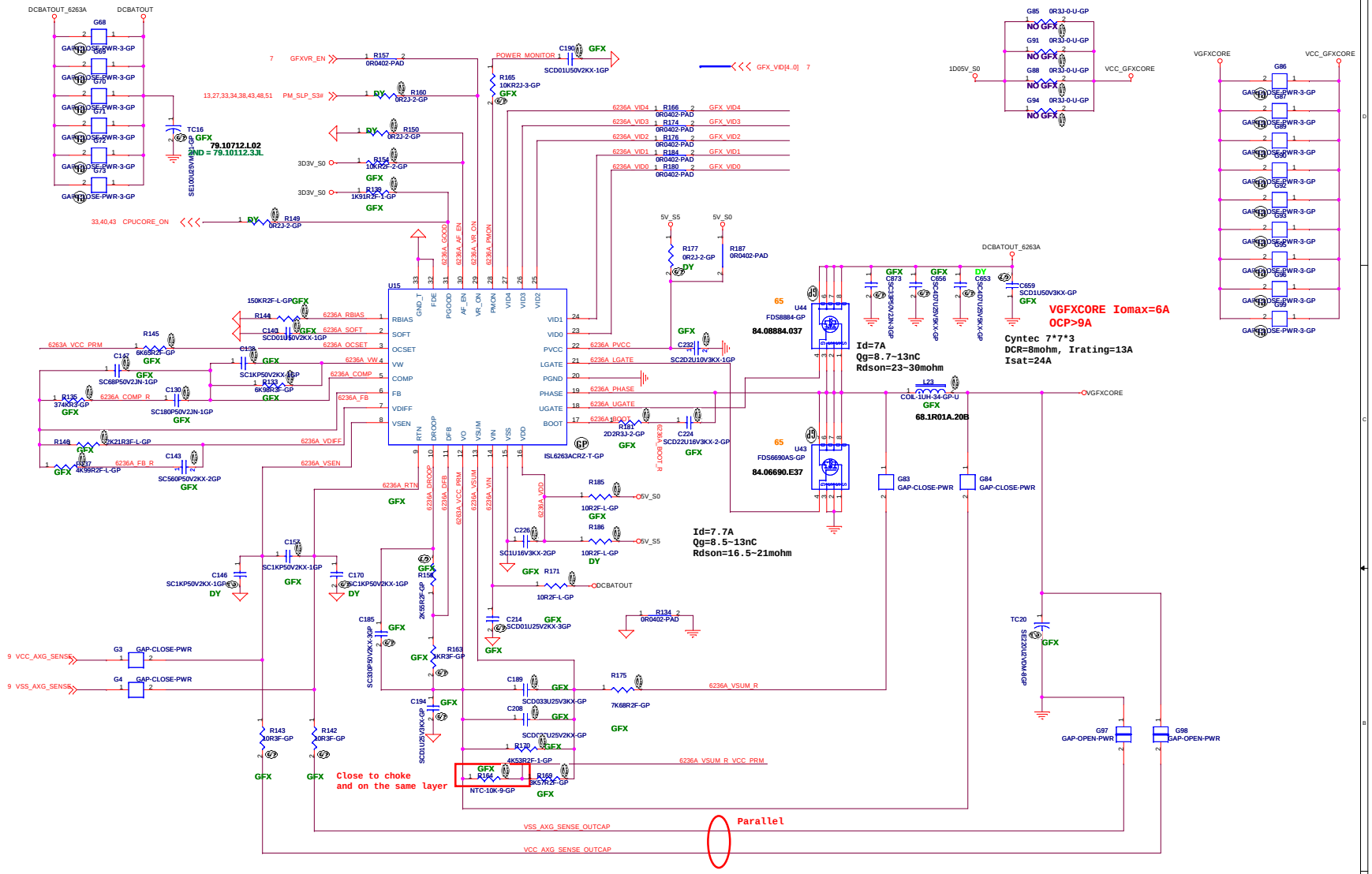
Size	Document Number	Rev
A3	JV71-MV DDR3 Madison	-1

Date: Wednesday, October 28, 2009 Sheet 43 of 62



JV71-MV DDR3 Madison

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 0D75V		
Size: A4	Document Number: JV71-MV DDR3 Madison	Rev: -1
Date: Wednesday, October 28, 2009	Sheet 44 of 62	



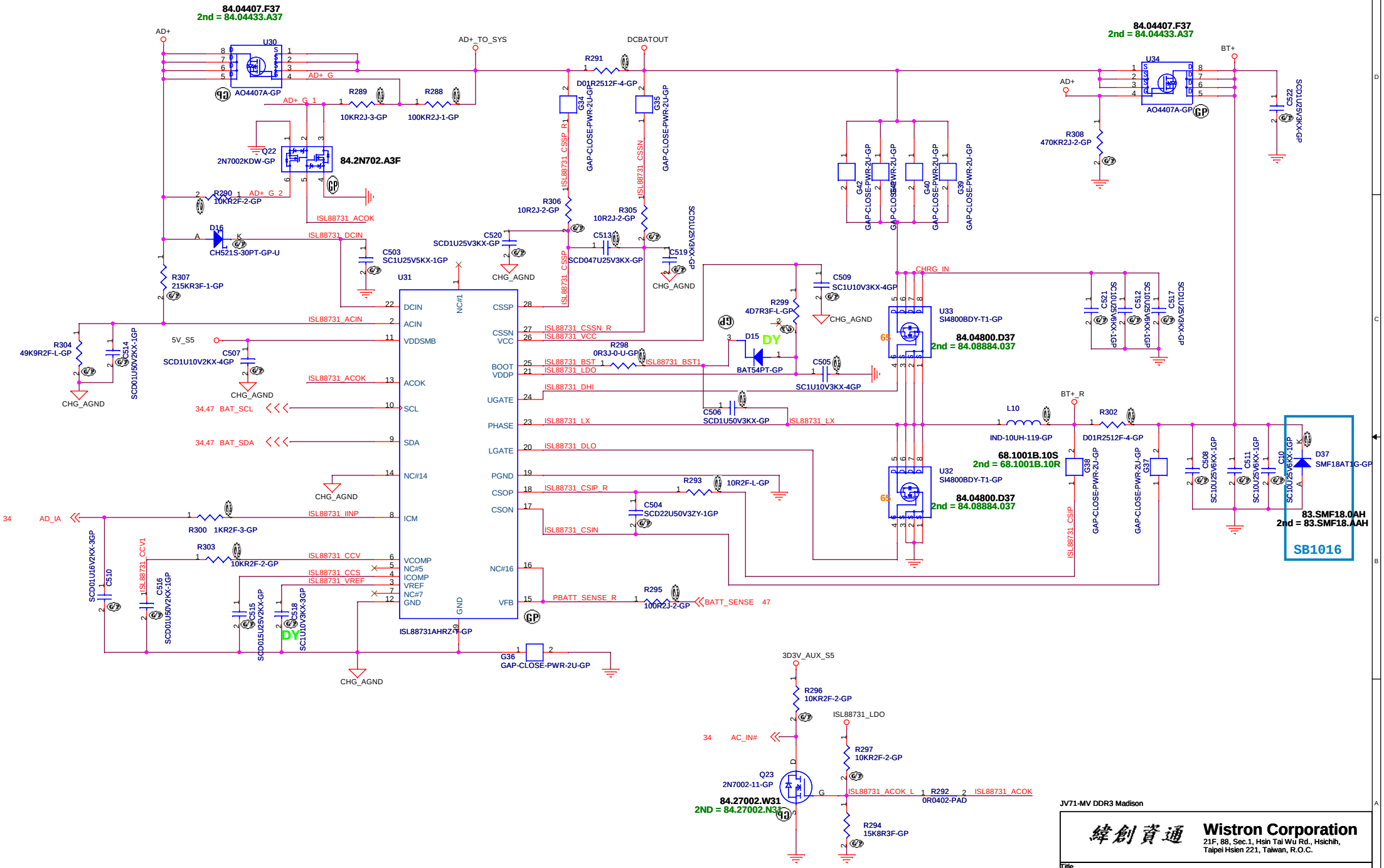
JV71-MV DDR3 Madison

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

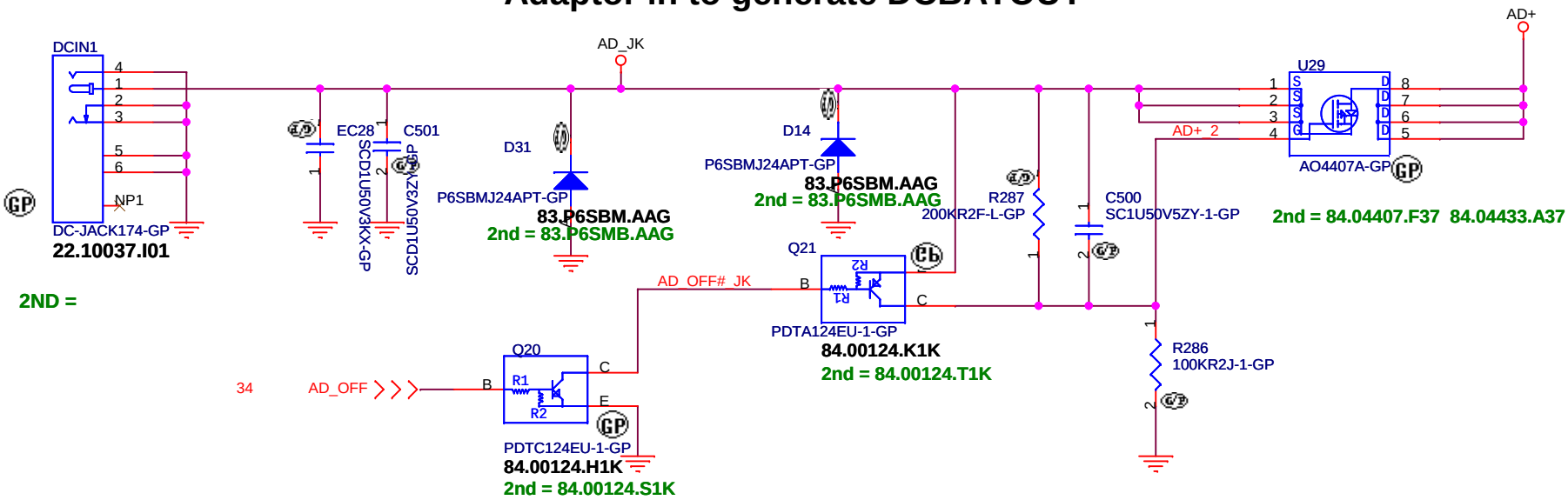
Title: ISL6263A_GFX CORE

Size	Document Number	Rev
Custom	JV71-MV DDR3 Madison	-1

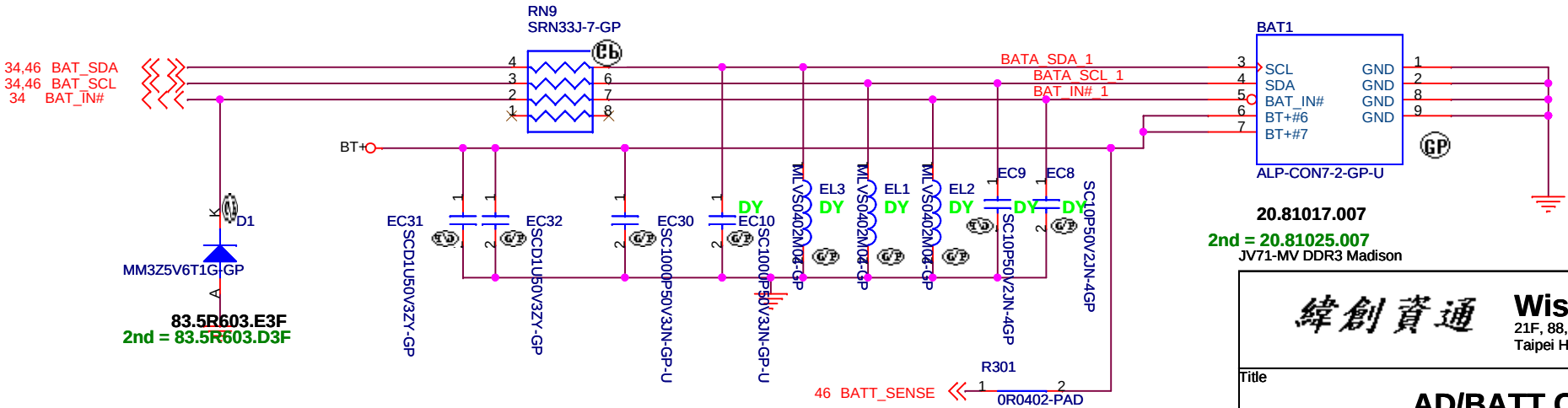
Date: Wednesday, October 28, 2009 Sheet 45 of 62


84.04407.F37
2nd = 84.04433.A37
AD+
U30
AO4407A-GP
AD+_TO_SYS
DCBATOUT
R291
D01R2512F-4-GP
R289
10KR2J-3-GP
R288
100KR2J-1-GP
Q22
2N7002KDW-GP
84.2N702.A3F
R290
10KR2F-2-GP
ISL88731_ACOK
D16
CH521S-30PT-GP-U
ISL88731_DCIN
C503
SC1U25V5KX-1GP
R307
215KR3F-1-GP
U31
ISL88731AHRZT-GP
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
NC#1
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
R306
10R2J-2-GP
R305
10R2J-2-GP
C520
SCD1U25V3KX-GP
C513
SCD047U25V3KX-GP
C519
SCD1U25V3KX-GP
CHG_AGND
ISL88731_CSSP_R1
ISL88731_CSSN
G34
G35
GAP-CLOSE-PWR-2U-GP
R304
49K9R2F-L-GP
C514
SCD01U50V2KX-1GP
5V_S5
C507
SCD1U10V2KX-4GP
ISL88731_ACIN
ISL88731_CSSN_R
ISL88731_VCC
ISL88731_BST
ISL88731_BST1
ISL88731_LDO
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
ISL88731_CSIP_R
ISL88731_CSIN
ISL88731_IINP
ISL88731_CCV
ISL88731_CCS
ISL88731_VREF
PBATT_SENSE_R
34,47 BAT_SCL
34,47 BAT_SDA
R298
0R3J-0-U-GP
R299
4D7R3F-L-GP
D15
BAT54PT-GP
DY
C509
SC1U10V3KX-4GP
C505
SC1U10V3KX-4GP
C506
SCD1U50V3KX-GP
R293
10R2F-L-GP
C504
SCD22U50V3ZY-1GP
R295
100R2J-2-GP
BATT_SENSE 47
34 AD_IA
R300 1KR2F-3-GP
R303
10KR2F-2-GP
C510
SCD01U16V2KX-3GP
C516
SCD01U50V2KX-1GP
C515
SCD015U25V2KX-GP
C518
SC1U10V3KX-3GP
G36
GAP-CLOSE-PWR-2U-GP
CHRG_IN
U33
SI4800BDY-T1-GP
U32
SI4800BDY-T1-GP
84.04800.D37
2nd = 84.08884.037
84.04400.D37
2nd = 84.08884.037
L10
IND-10UH-119-GP
68.1001B.10S
2nd = 68.1001B.10R
R302
D01R2512F-4-GP
BT+_R
BT+
U34
AO4407A-GP
R308
470KR2J-2-GP
C522
SCD1U25V3KX-GP
D37
SMF18AT1G-GP
83.SMF18.0AH
2nd = 83.SMF18.AAH
SB1016
C508
C511
C10
SC10U25V6KX-1GP
C521
C512
C517
SCD1U25V3KX-GP
SC10U25V6KX-1GP
3D3V_AUX_S5
R296
10KR2F-2-GP
ISL88731_LDO
34 AC_IN#
R297
10KR2F-2-GP
Q23
2N7002-11-GP
84.27002.W31
2ND = 84.27002.N31
ISL88731_ACOK_L
R292
0R0402-PAD
ISL88731_ACOK
R294
15K8R3F-GP
JV71-MV DDR3 Madison
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A Charger
Size
A3
Document Number
JV71-MV DDR3 Madison
Rev
-1
Date: Wednesday, October 28, 2009
Sheet 46 of 62

Adaptor in to generate DCBATOUT

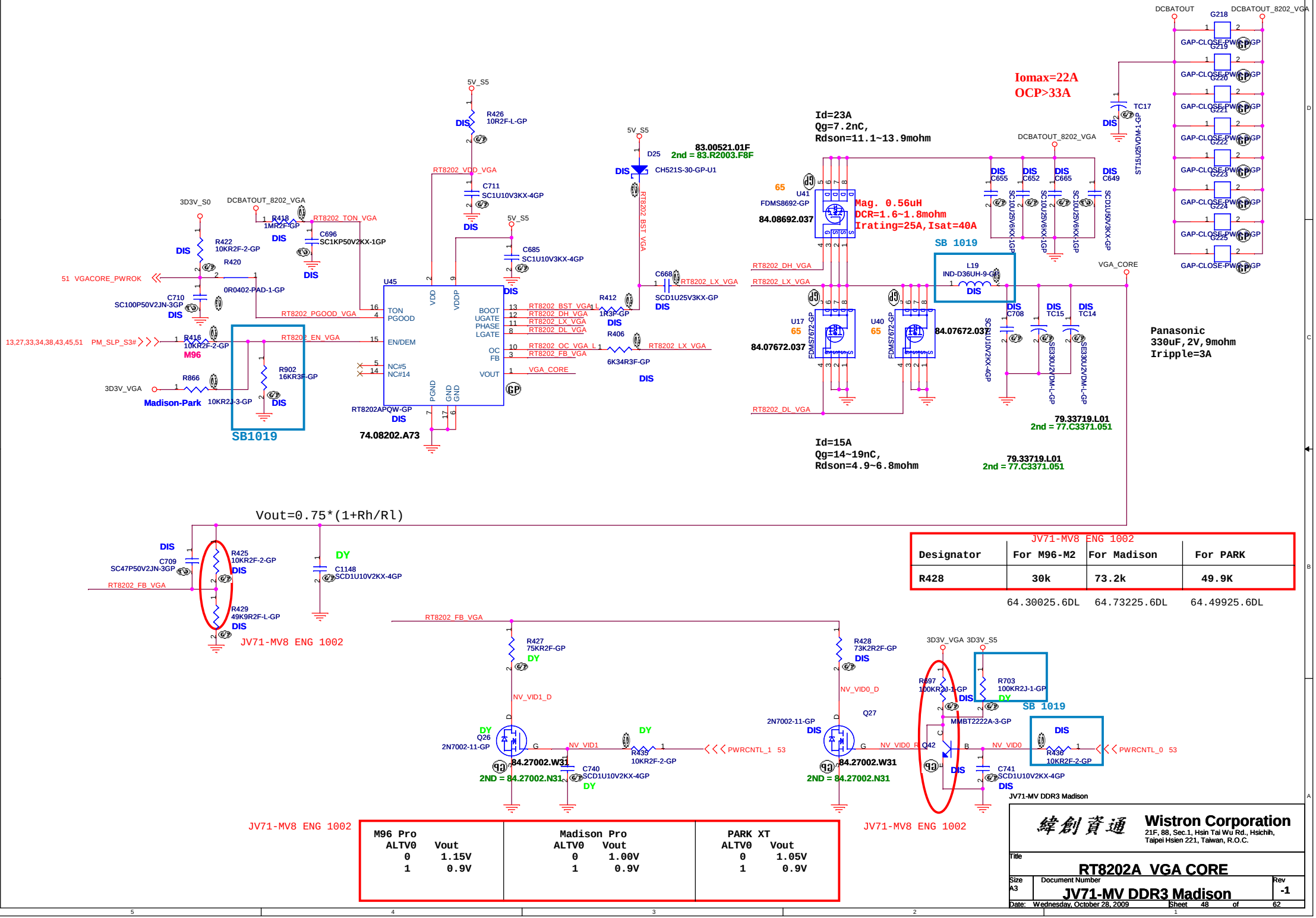


BATTERY CONNECTOR



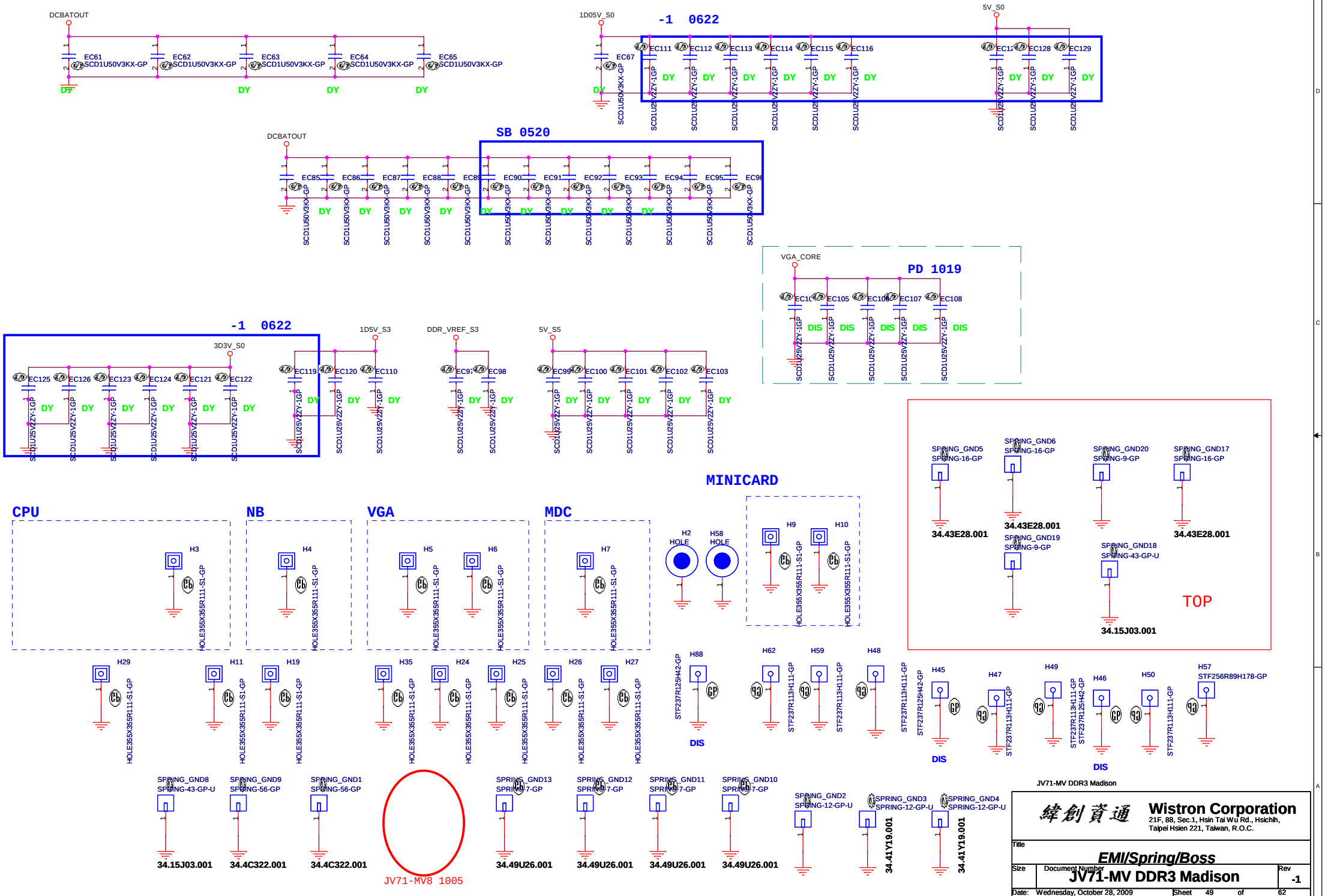
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size	Document Number: JV71-MV DDR3 Madison	Rev: -1
Date: Wednesday, October 28, 2009	Sheet 47 of 62	

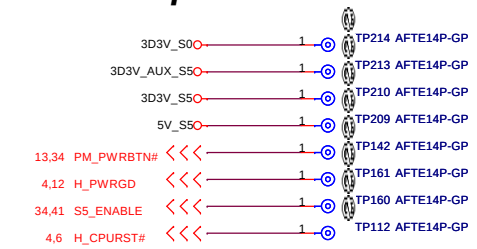


Designator	For M96-M2	For Madison	For PARK
R428	30k	73.2k	49.9K
	64.30025.6DL	64.73225.6DL	64.49925.6DL

M96 Pro		Madison Pro		PARK XT	
ALTV0	Vout	ALTV0	Vout	ALTV0	Vout
0	1.15V	0	1.00V	0	1.05V
1	0.9V	1	0.9V	1	0.9V


DCBATOUT
EC61 SCD1U50V3KX-GP
EC62 SCD1U50V3KX-GP
EC63 SCD1U50V3KX-GP
EC64 SCD1U50V3KX-GP
EC65 SCD1U50V3KX-GP
DY
1D05V_S0
-1 0622
EC67 SCD1U50V3KX-GP
EC111 EC112 EC113 EC114 EC115 EC116
5V_S0
EC127 EC128 EC129
SCD1U25V2ZY-1GP
SB 0520
EC85 EC86 EC87 EC88 EC89 EC90 EC91 EC92 EC93 EC94 EC95 EC96
SCD1U50V3KX-GP
VGA_CORE
PD 1019
EC104 EC105 EC106 EC107 EC108
DIS
-1 0622
3D3V_S0
EC125 EC126 EC123 EC124 EC121 EC122
1D5V_S3
EC119 EC120 EC110
DDR_VREF_S3
EC97 EC98
5V_S5
EC99 EC100 EC101 EC102 EC103
MINICARD
CPU
NB
VGA
MDC
H3 H4 H5 H6 H7
HOLE355X355R111-S1-GP
H2 HOLE
H58 HOLE
H9 H10
SPRING_GND5 SPRING-16-GP
34.43E28.001
SPRING_GND6 SPRING-16-GP
34.43E28.001
SPRING_GND20 SPRING-9-GP
SPRING_GND17 SPRING-16-GP
34.43E28.001
SPRING_GND19 SPRING-9-GP
SPRING_GND18 SPRING-43-GP-U
34.15J03.001
TOP
H29 H11 H19 H35 H24 H25 H26 H27
H88
STF237R125H42-GP
DIS
H62 H59 H48
STF237R113H111-GP
H45
STF237R125H42-GP
DIS
H47
H49
H46
STF237R113H111-GP
STF237R125H42-GP
DIS
H50
STF237R113H111-GP
H57
STF256R89H178-GP
SPRING_GND8 SPRING-43-GP-U
34.15J03.001
SPRING_GND9 SPRING-56-GP
34.4C322.001
SPRING_GND1 SPRING-56-GP
34.4C322.001
JV71-MV8 1005
SPRING_GND13 SPRING-7-GP
34.49U26.001
SPRING_GND12 SPRING-7-GP
34.49U26.001
SPRING_GND11 SPRING-7-GP
34.49U26.001
SPRING_GND10 SPRING-7-GP
34.49U26.001
SPRING_GND2 SPRING-12-GP-U
SPRING_GND3 SPRING-12-GP-U
34.41Y19.001
SPRING_GND4 SPRING-12-GP-U
34.41Y19.001
JV71-MV DDR3 Madison
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
Document Number
JV71-MV DDR3 Madison
Rev
-1
Date: Wednesday, October 28, 2009
Sheet 49 of 62

Check test point



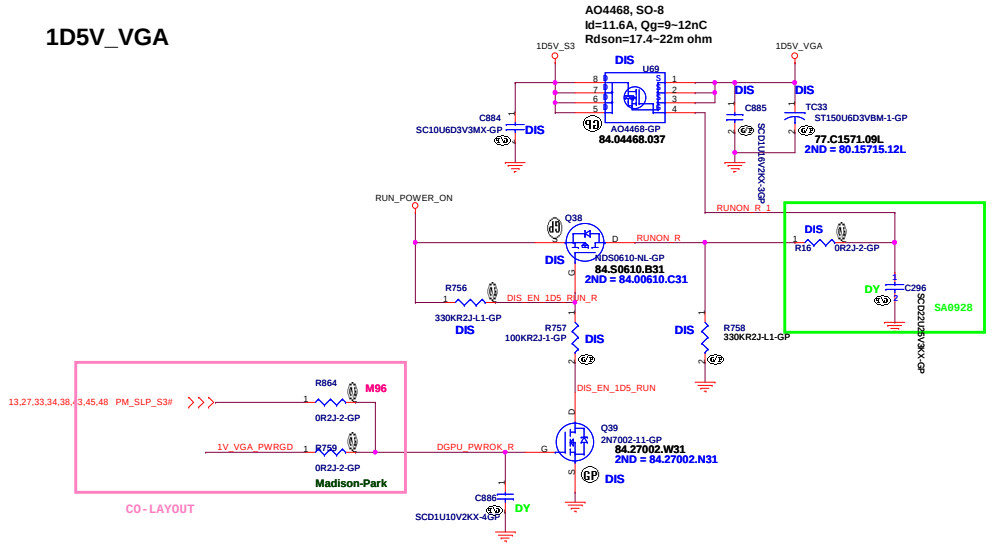
Test Point放在Dimm Door打開可量測處

JV71-MV DDR3 Madison

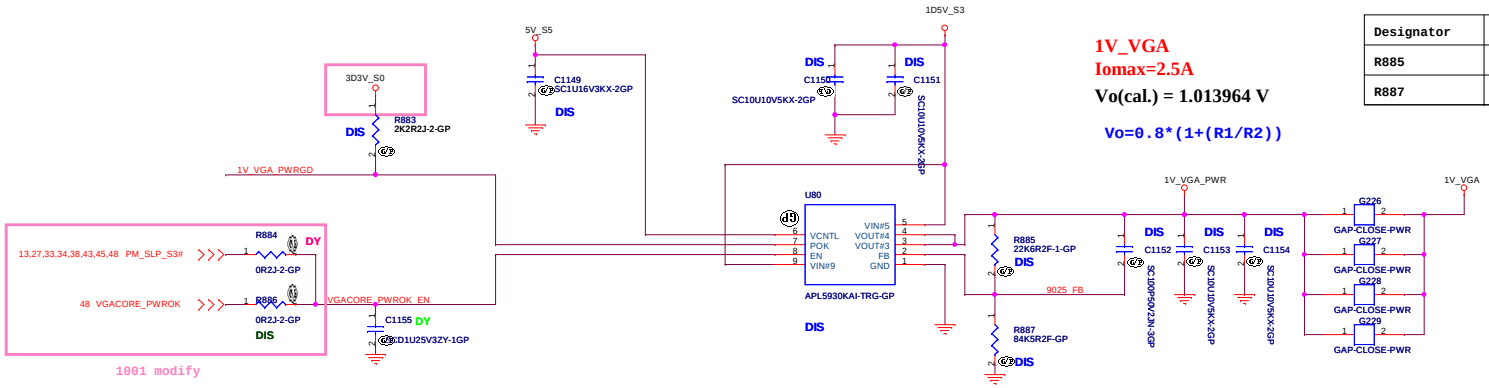
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

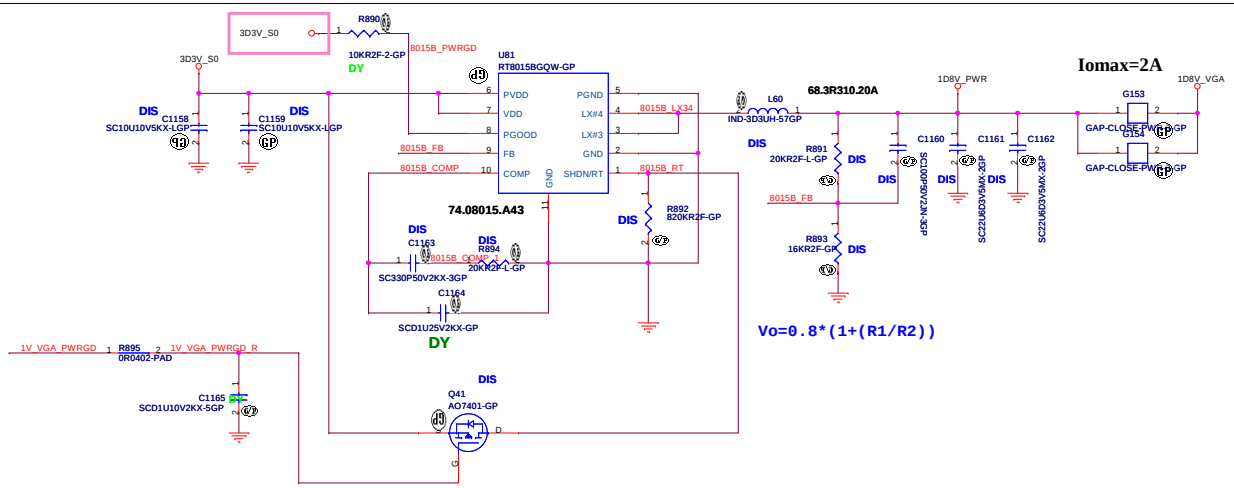
Title	***AFTE_TP***	
Size A3	Document Number **JV71-MV DDR3 Madison**	Rev **-1**
Date: Wednesday, October 28, 2009	Sheet 50 of 62	

1D5V_VGA



APL5930 for 1V_VGA





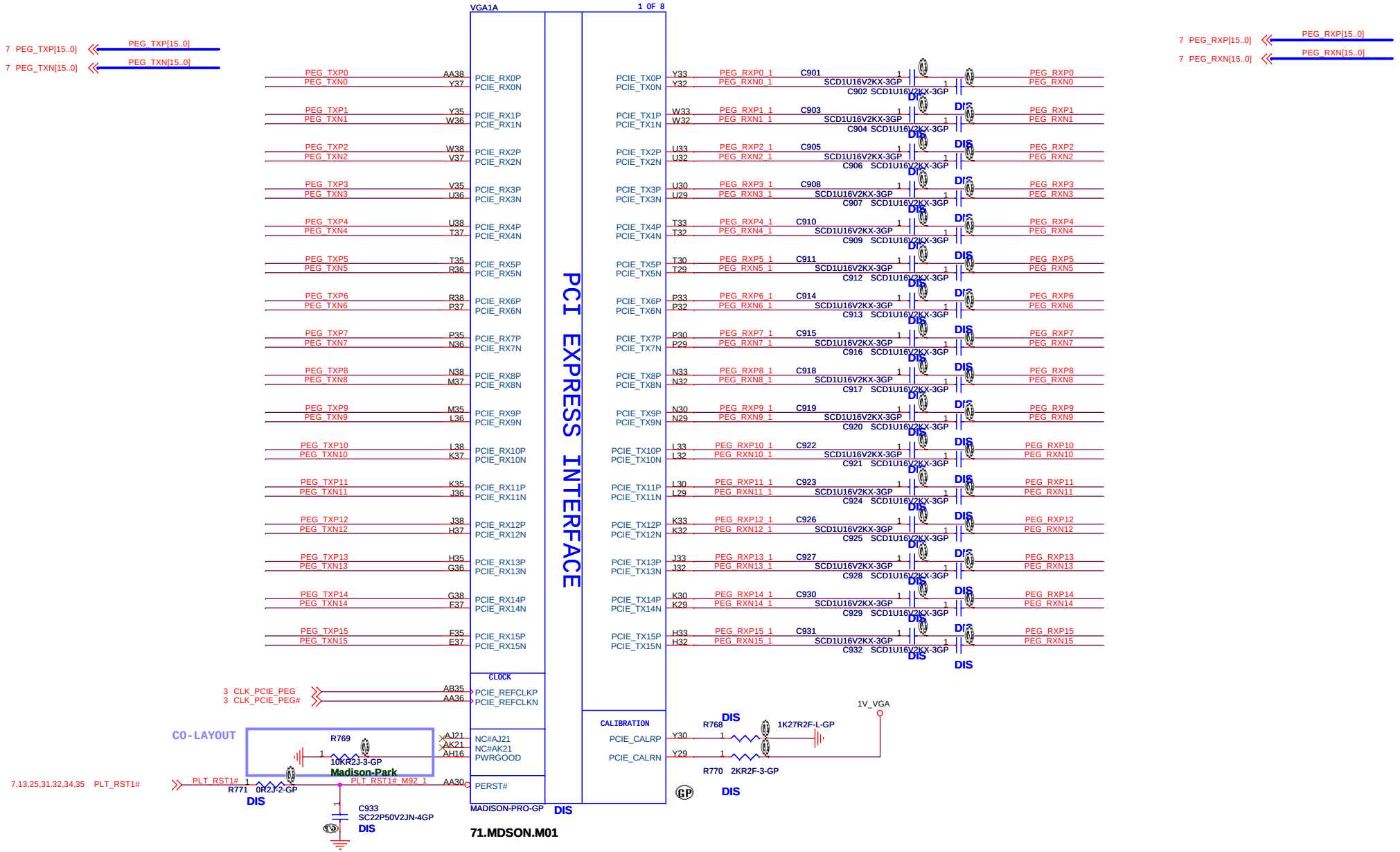
JV71-MV DDR3 Madison

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI POWER**

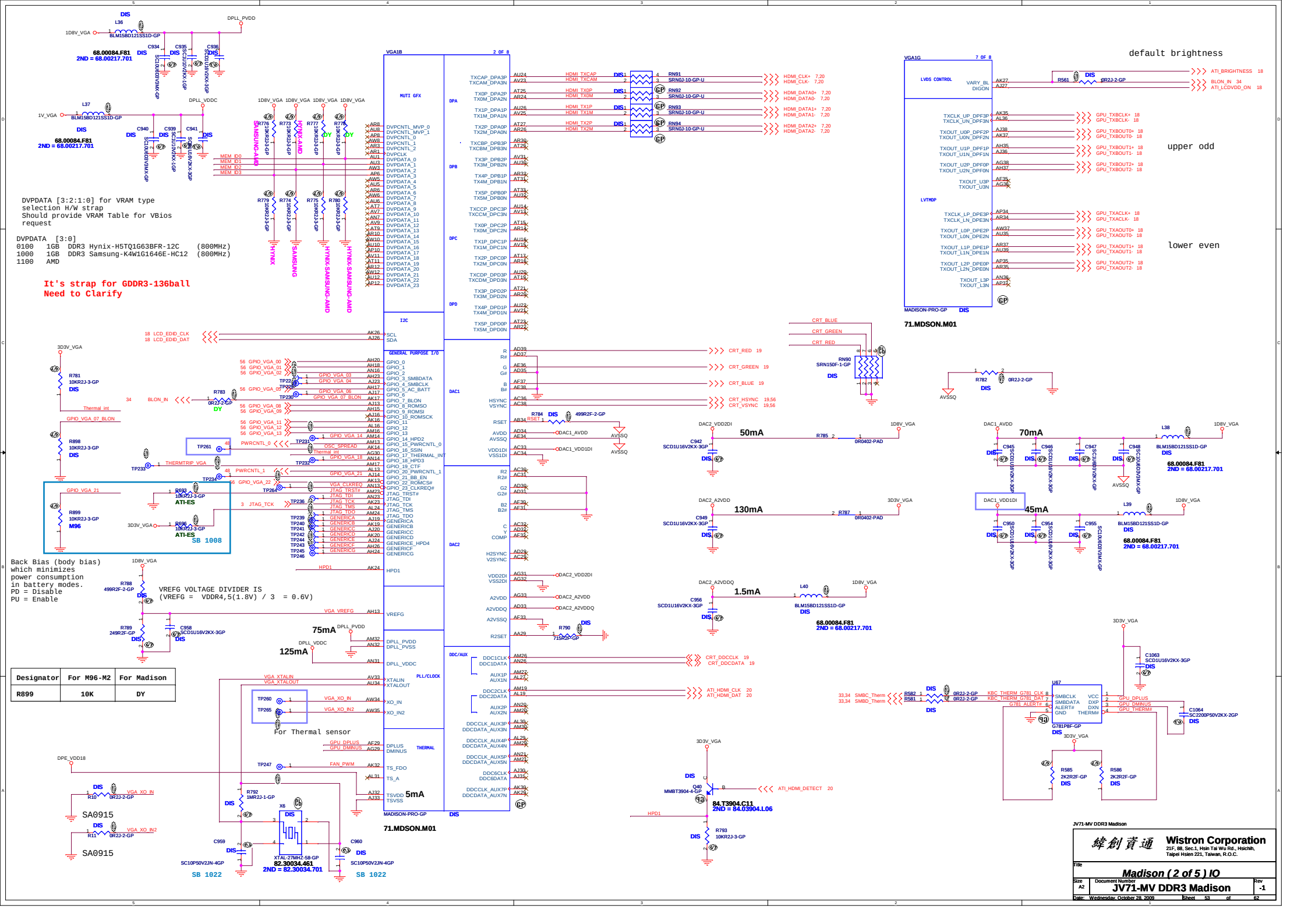
Size: Custom | Document Number: **JV71-MV DDR3 Madison** | Rev: -1

Date: Wednesday, October 28, 2009 | Sheet 51 of 62

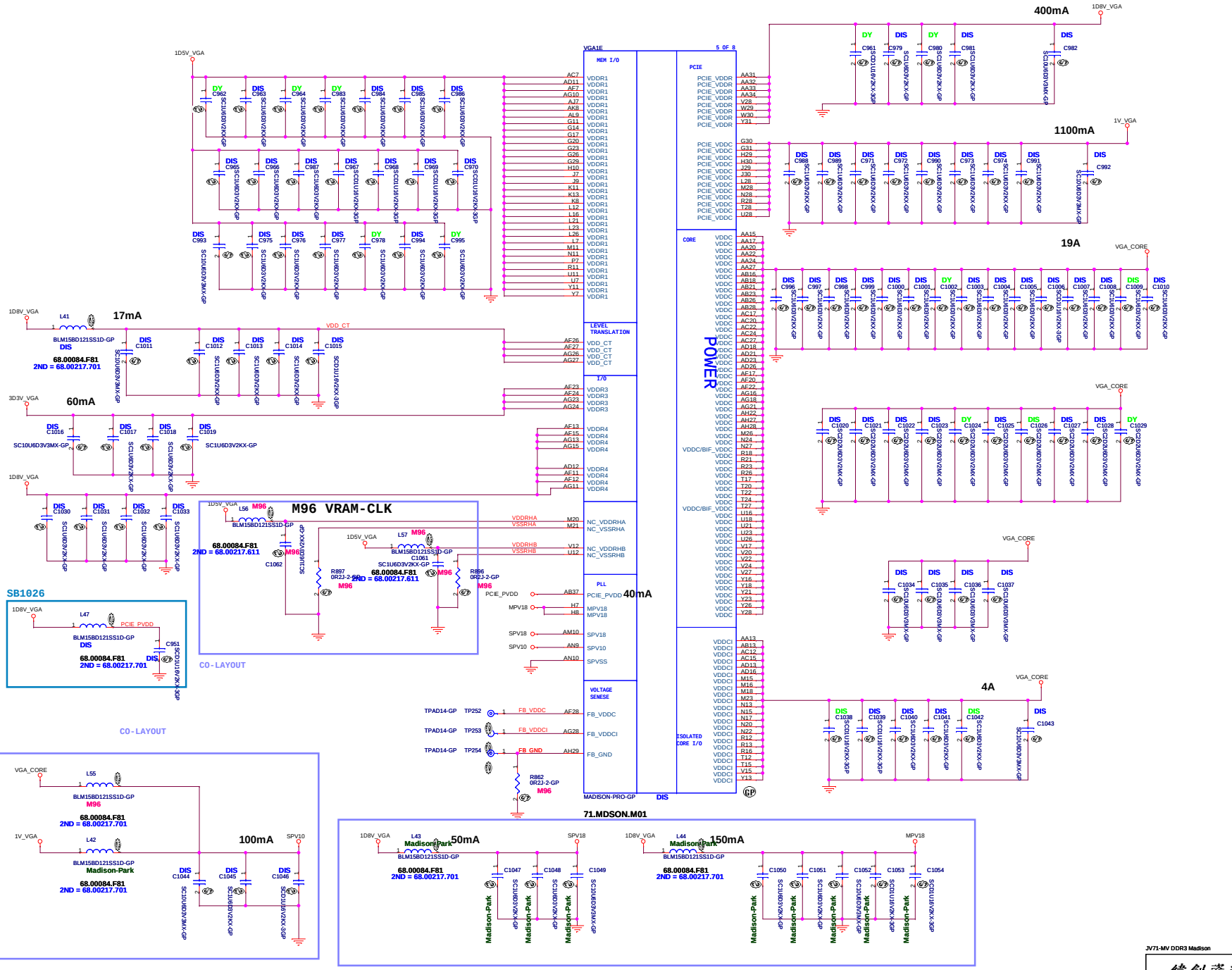


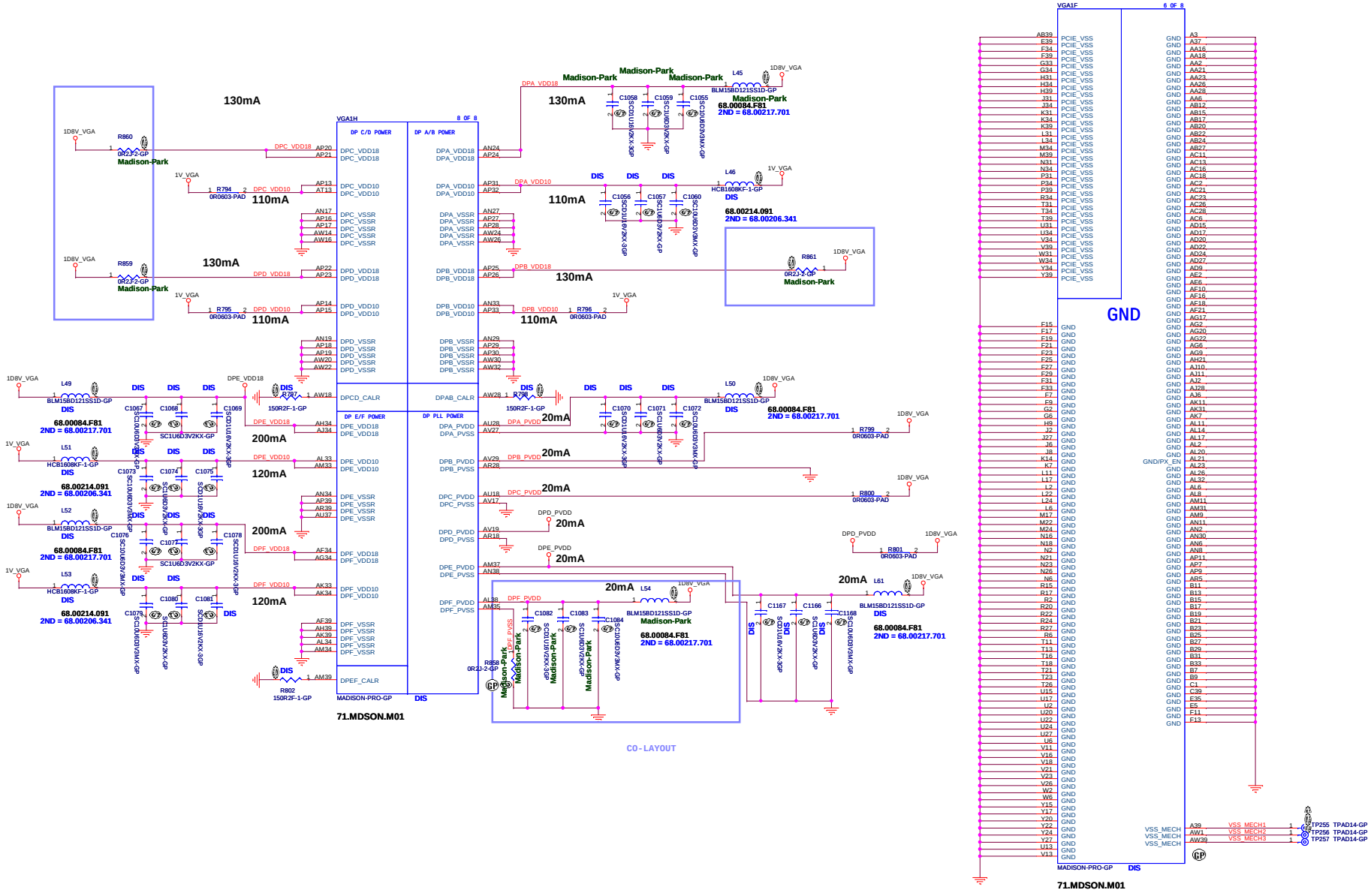
JV71-MV DDR3 Madison

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Madison (1 of 5) PCIE		
Size: A3	Document Number: JV71-MV DDR3 Madison	Rev: -1
Date: Wednesday, October 28, 2009	Sheet 52 of 62	



Designator	For M96-M2	For Madison
R899	10K	DY


400mA
1100mA
19A
17mA
60mA
40mA
100mA
50mA
150mA
4A
POWER
M96 VRAM-CLK
SB1026
CO-LAYOUT
CO-LAYOUT
VGA1E
MEM I/O
PCIE
CORE
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENESE
ISOLATED CORE I/O
MADISON-PRO-GP
DIS
71.MDSON.M01
68.00084.F81
2ND = 68.00217.701
Madison-Park
JV71-MV DDR3 Madison
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Madison (3 of 5) POWER
Size A2
Document Number JV71-MV DDR3 Madison
Rev -1
Date: Wednesday, October 28, 2009
Sheet 54 of 62



JV71-MV DDR3 Madison

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison (4 of 5) DP POWER

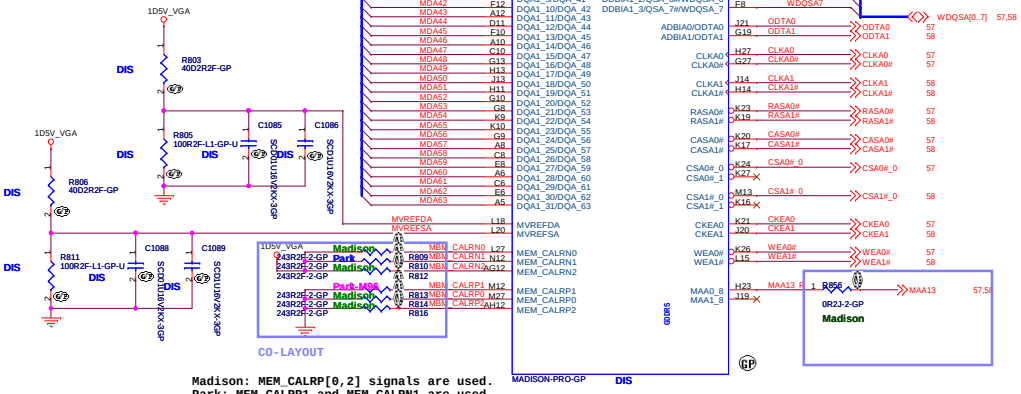
Size	Document Number	Rev
A2	JV71-MV DDR3 Madison	-1

Date: Wednesday, October 28, 2009 Sheet 55 of 62

Designator	For M96-M2	For Madison
R803/R806	100	40

For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R



Madison: MEM_CALRP[0,2] signals are used.
Park: MEM_CALRP1 and MEM_CALRN1 are used

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

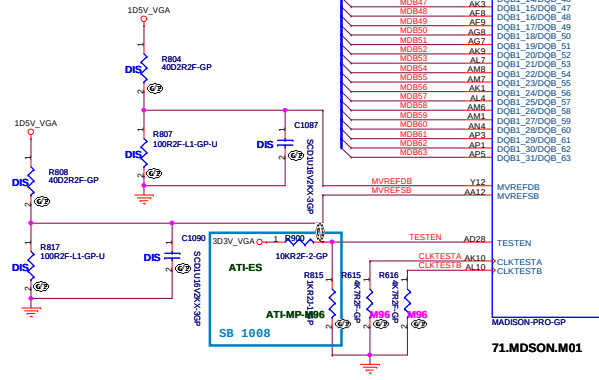
H2SYNC, GENERICC, GPIO2, GPIO1

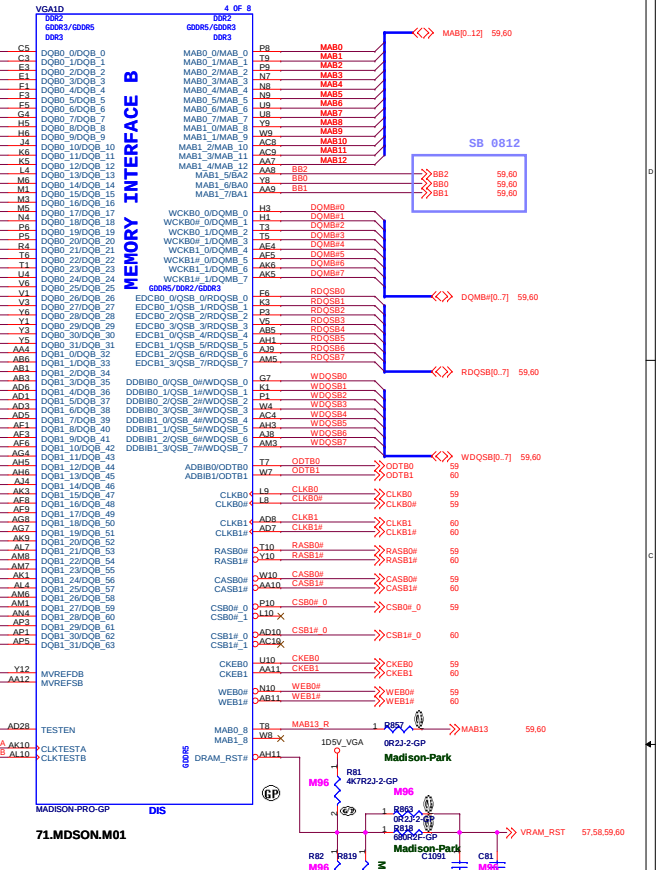
If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

Designator	For M96-M2	For Madison
R804/R808	100	40

For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

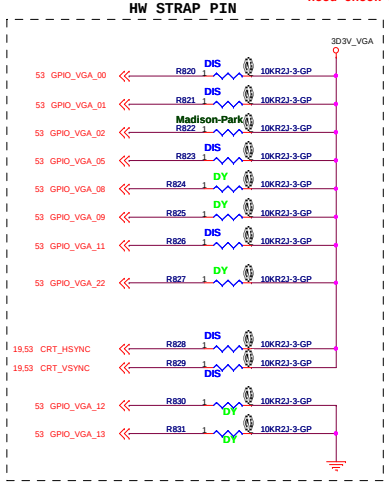
DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R





HW STRAP PIN

need check M9x schematic



JV71-MV DDR3 Madison

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison (5 of 5) MEMORY/ST

Size	Document Number	Rev
A2	JV71-MV DDR3 Madison	-1

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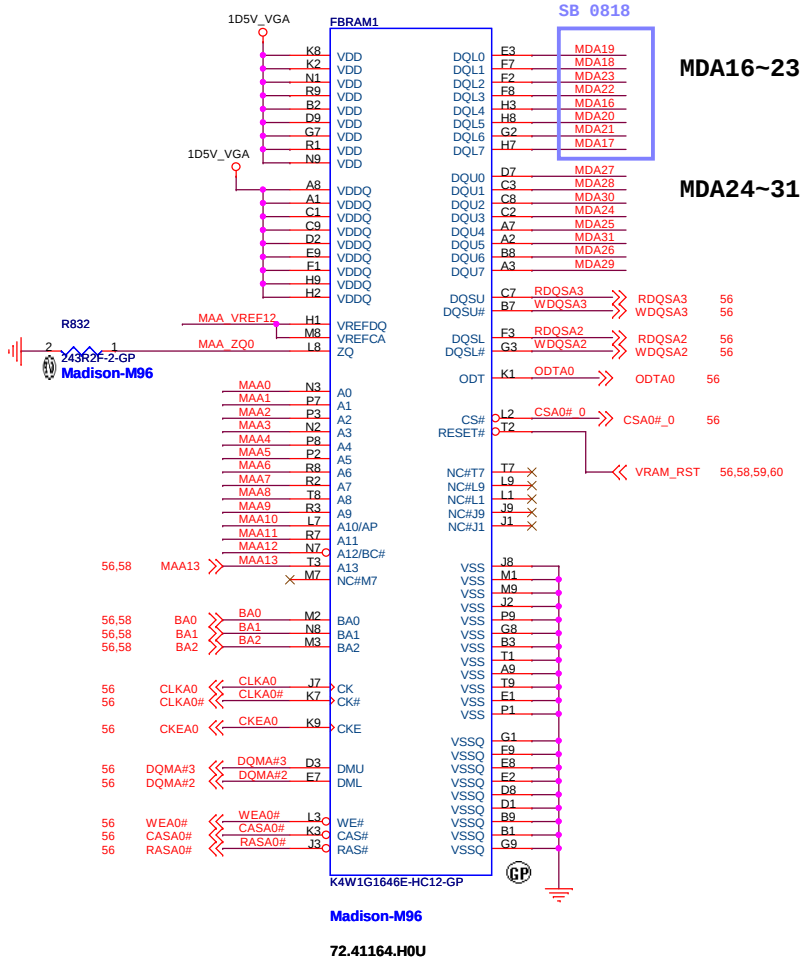
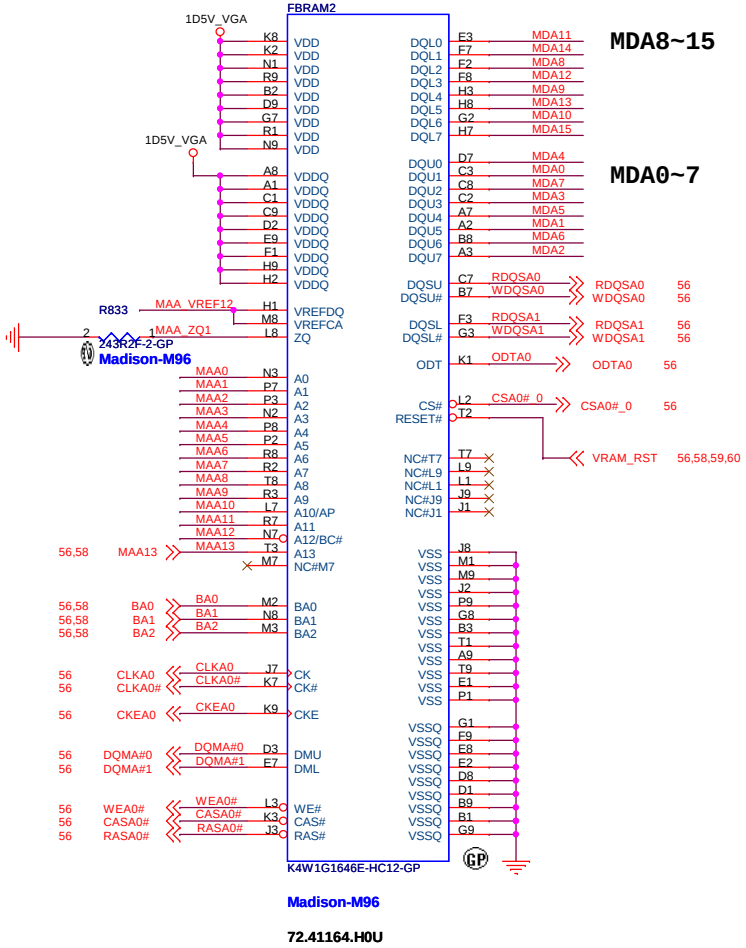
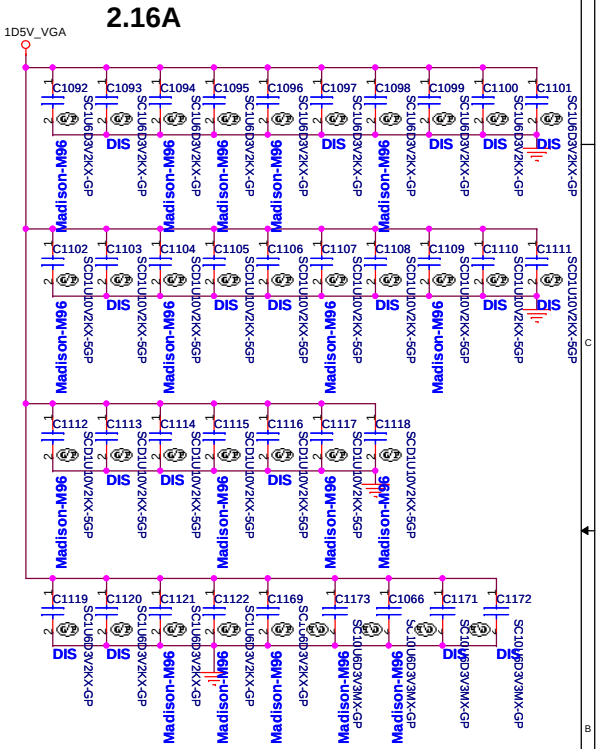
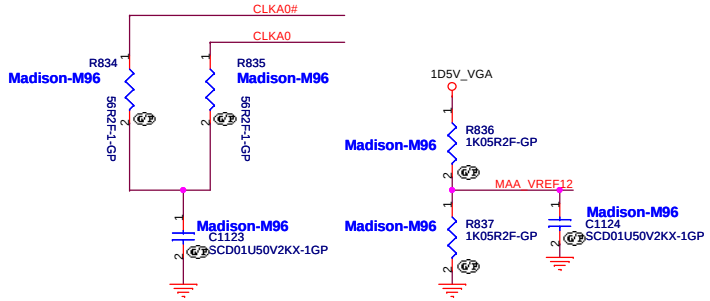
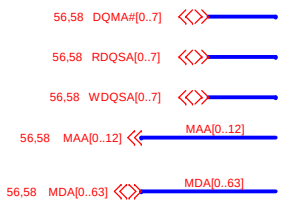
DDR3











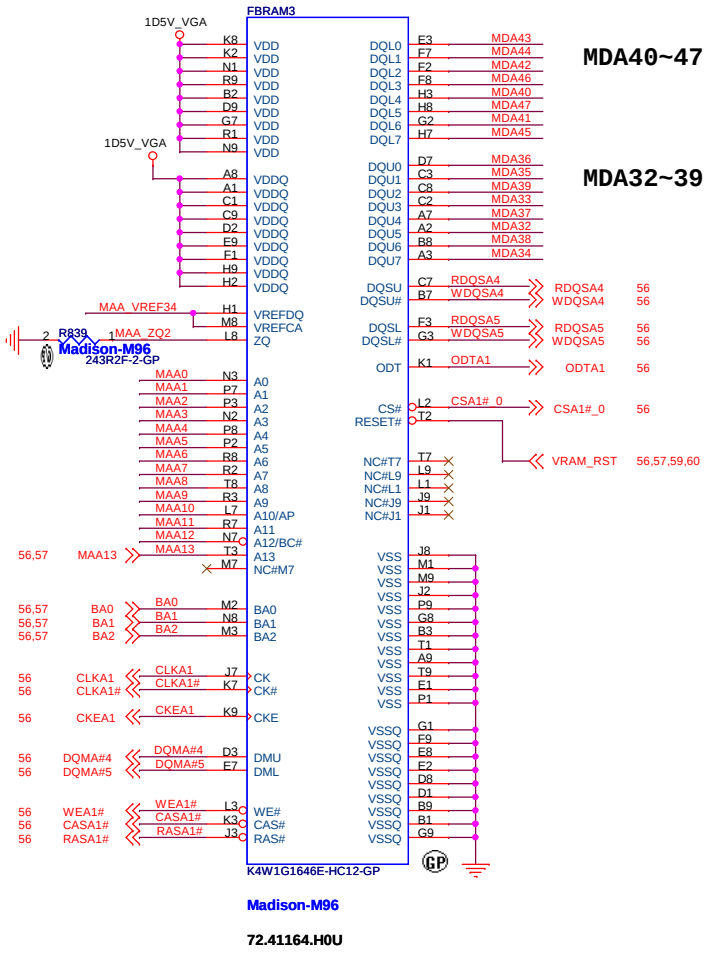
HYUNIX 1ST=72.51G63.C0U
SAMSUNG 2ND=72.41164.H0U
AMD 3RD=VR.1GB0T.002

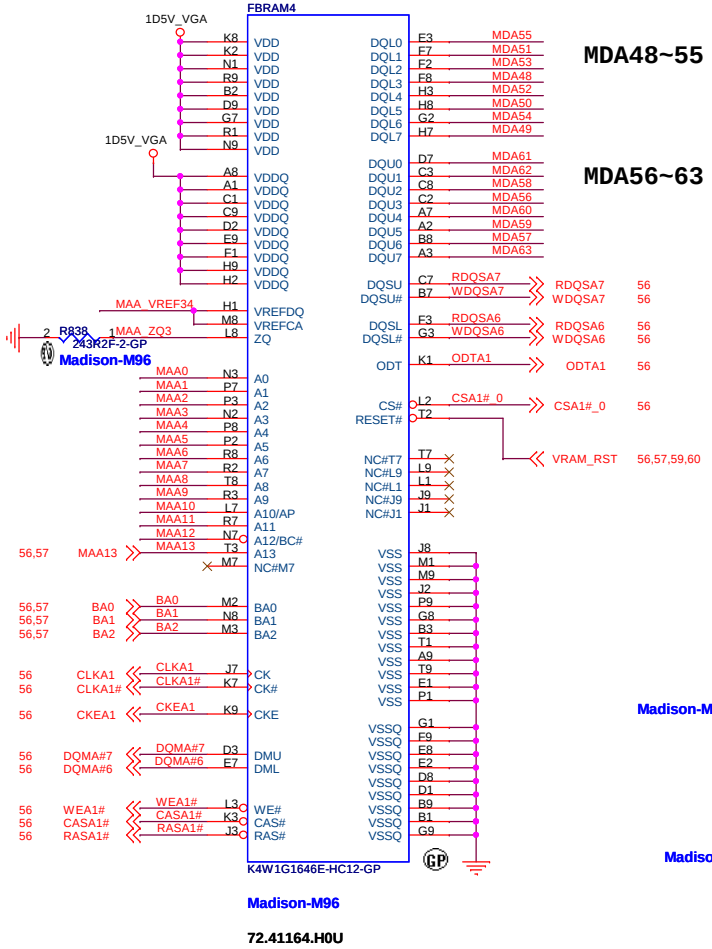
JV71-MV DDR3 Madison

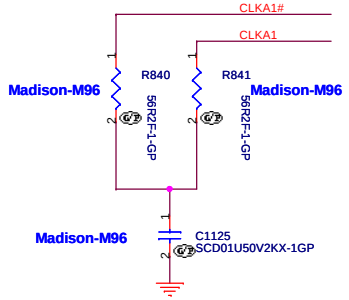
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

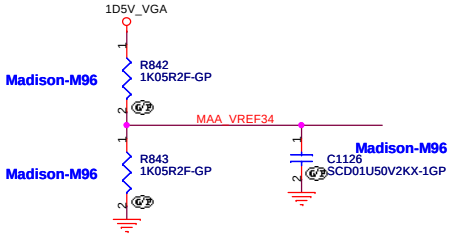
Title	***VRAM(1 of 4)***	
Size A3	Document Number **JV71-MV DDR3 Madison**	Rev -1
Date: Wednesday, October 28, 2009	Sheet 57 of 62	

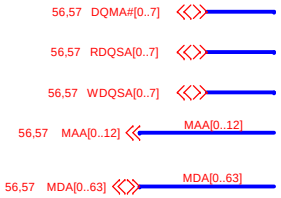
DDR3









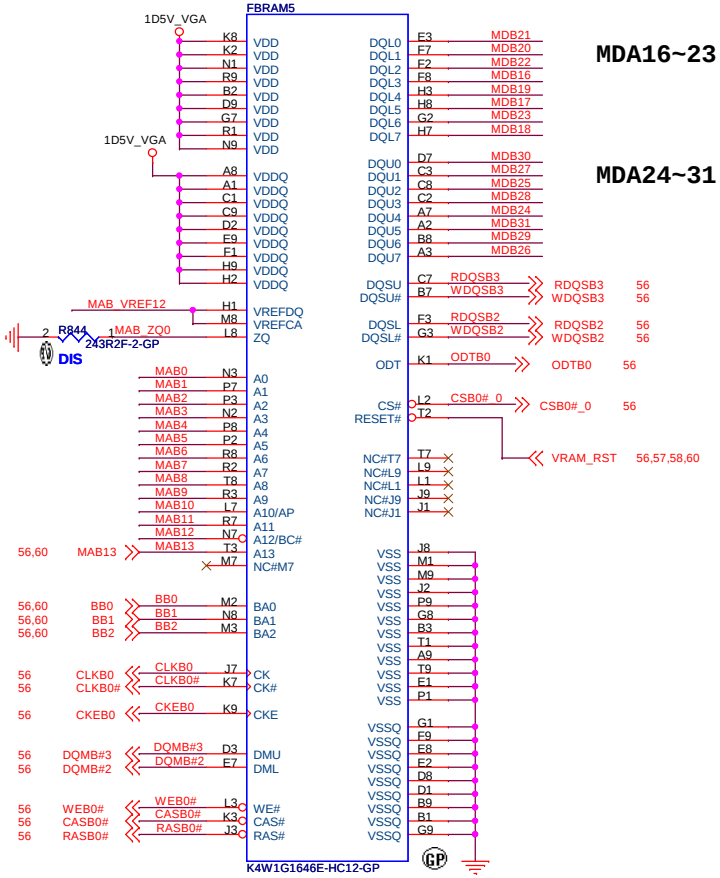


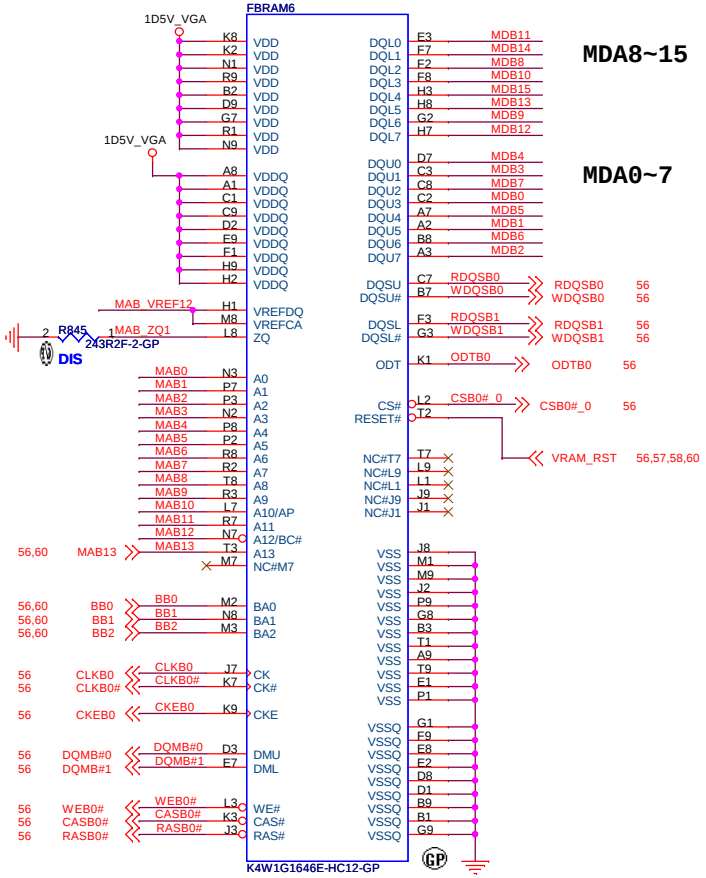
HYUNIX 1ST=72.51G63.C0U
SAMSUNG 2ND=72.41164.H0U
AMD 3RD=VR.1GB0T.002

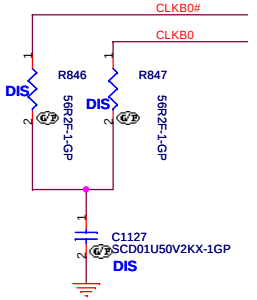
JV71-MV DDR3 Madison

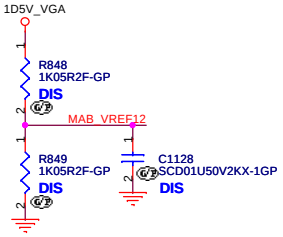
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *VRAM(2 fo 4)*		
Size: A3	Document Number: JV71-MV DDR3 Madison	Rev: -1
Date: Wednesday, October 28, 2009	Sheet 58 of 62	

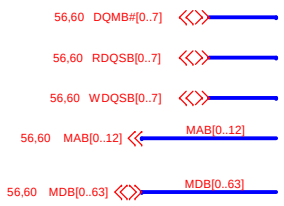
DDR3











HYUNIX 1ST=72.51G63.C0U
SAMSUNG 2ND=72.41164.H0U
AMD 3RD=VR.1GB0T.002

JV71-MV DDR3 Madison

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM(3 of 4)***

Size	Document Number	Rev
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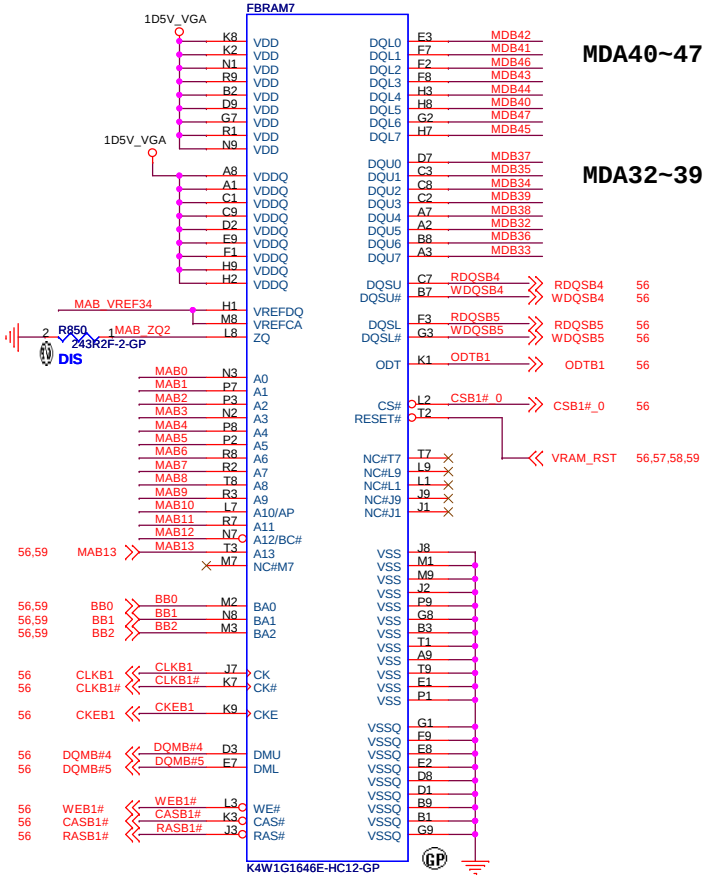
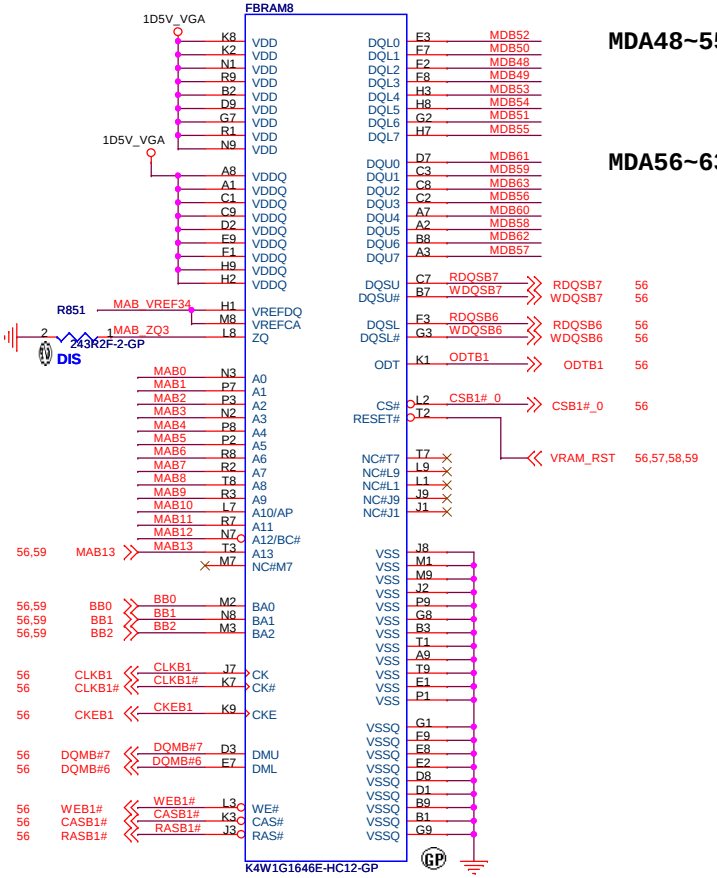
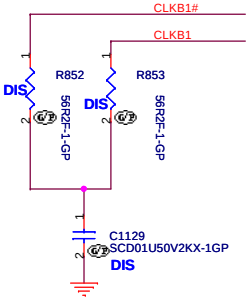
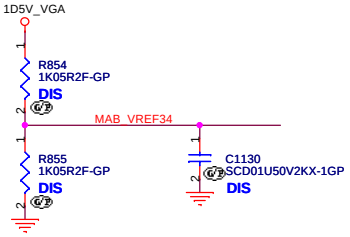
Date: Wednesday, October 28, 2009 Sheet 59 of 62

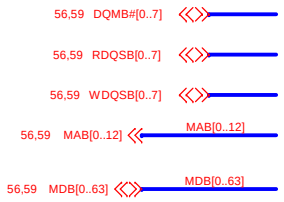
DDR3











HYUNIX 1ST=72.51G63.C0U
SAMSUNG 2ND=72.41164.H0U
AMD 3RD=VR.1GB0T.002

JV71-MV DDR3 Madison

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM(4 of 4)***

Size	Document Number	Rev
A3	**JV71-MV DDR3 Madison**	-1

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SA SB SC -1

JV71-MV DDR3 Madison

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HISTORY***

Size	Document Number	Rev
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Group Name	SKU A	SKU B	SKU C	SKU D
DY,ZZ,65	X	X	X	X
GFX	X	X	X	O
NOGFX	X	X	X	X
DIS	O	O	O	X
M96	O	X	X	X
Madison	X	O	X	X
Madison-M96	O	O	X	X
Madison-Park	X	O	O	X
Park	X	X	O	X
Park-M96	O	X	O	X
UMA	X	X	X	O
Hynix	X	O	O	X
Hynix-AMD	X	O	O	X
Hynix-Samsung-AMD	O	O	O	X
Samsung	O	X	X	X
Samsung-AMD	O	X	X	X
ATI-ES	X	O	O	X
ATI-MP-M96	O	X	X	X

65 Main	65 2nd
65.4FXZZ.024	65.4FXZZ.025
65.4FXZZ.026	65.4FXZZ.027
65.4FXZZ.028	65.4FXZZ.029
65.4FXZZ.032	65.4FXZZ.033

Group Name	SKU E	SKU F	SKU G	
DY,ZZ,65	X	X	X	
GFX	X	X	X	
NOGFX	X	X	X	
DIS	O	O	O	
M96	O	X	X	
Madison	X	O	X	
Madison-M96	O	O	X	
Madison-Park	X	O	O	
Park	X	X	O	
Park-M96	O	X	O	
UMA	X	X	X	
Hynix	O	X	X	
Hynix-AMD	O	X	X	
Hynix-Samsung-AMD	O	O	O	
Samsung	X	O	O	
Samsung-AMD	X	O	O	
ATI-ES	X	O	O	
ATI-MP-M96	O	X	X	

Part Name	SKU A PM45 M96 Samsung	SKU B PM45 Madison Hynix	SKU C PM45 Park Hynix	SKU D GM45 UMA
NB NB1	KI.G4501.002	KI.G4501.002	KI.G4501.002	KI.G4501.001
SB SB1	KI.80101.030	KI.80101.030	KI.80101.030	KI.80101.030
VGA VGA1	71.M96M2.M03	71.MDSON.M01	71.0PARK.M04	X
VRAM FBRAM1~4	VR.1GB0B.006	VR.1GB0G.004	X	X
VRAM FBRAM5~8	VR.1GB0B.006	VR.1GB0G.004	VR.1GB0G.004	X
1v_VGA/1.1v_VGA				
R885	64.78715.6DL	X	X	X
R887	64.20525.6DL	X	X	X
VGA_CORE R428	64.30025.6DL	64.73225.6DL	64.49925.6DL	X
RGB C165,151,108	X	X	X	78.6R874.1FL
TVDAC RN31	X	X	X	66.75036.08L
CRT RN30	X	X	X	66.15156.08L
TRANSFORMER XF1~2	68.HD081.30B	68.HD081.30B	68.HD081.30B	68.HD081.30B
MVREFDA R803	64.10005.6DL	X	X	X
MVREFSA R806	64.10005.6DL	X	X	X
MVREFDB R804	64.10005.6DL	X	X	X
MVREFSB R808	64.10005.6DL	X	X	X
90W/65W DCIN1	22.10037.I21	22.10037.I21	X	X
65BOM	65.4FXZZ.024	65.4FXZZ.024	65.4FXZZ.024	65.4FXZZ.032
	65.4FXZZ.026	65.4FXZZ.026	65.4FXZZ.026	65.4FXZZ.026
				65.4FXZZ.028

Part Name	SKU E PM45 M96 Hynix	SKU F PM45 Madison Samsung	SKU G PM45 Park Samsung	
NB NB1	KI.G4501.002	KI.G4501.002	KI.G4501.002	
SB SB1	KI.80101.030	KI.80101.030	KI.80101.030	
VGA VGA1	71.M96M2.M03	71.MDSON.M01	71.0PARK.M04	
VRAM FBRAM1~4	VR.1GB0G.004	VR.1GB0B.006	X	
VRAM FBRAM5~8	VR.1GB0G.004	VR.1GB0B.006	VR.1GB0B.006	
1v_VGA/1.1v_VGA				
R885	64.78715.6DL	X	X	
R887	64.20525.6DL	X	X	
VGA_CORE R428	64.30025.6DL	64.73225.6DL	64.49925.6DL	
TVDAC RN31	X	X	X	
CRT RN30	X	X	X	
TRANSFORMER XF1~2	68.HD081.30B	68.HD081.30B	68.HD081.30B	
MVREFDA R803	64.10005.6DL	X	X	
MVREFSA R806	64.10005.6DL	X	X	
MVREFDB R804	64.10005.6DL	X	X	
MVREFSB R808	64.10005.6DL	X	X	
90W/65W DCIN1	22.10037.I21	22.10037.I21	X	
65BOM	65.4FXZZ.024	65.4FXZZ.024	65.4FXZZ.024	
	65.4FXZZ.026	65.4FXZZ.026	65.4FXZZ.026	

LAB-Stage BOM temporary change list

SKU-A,B

Delete R428 64.15035.6DL

Delete Q27 84.27002.W31

Delete R436 63.10334.1DL

Delete C741 78.10423.5FL

Change R429 from 64.75025.6DL to 64.49925.6DL

SKU-C

Delete R428 64.15035.6DL

Delete Q27 84.27002.W31

Delete R436 63.10334.1DL

Delete C741 78.10423.5FL

Change R429 from 64.75025.6DL to 64.37425.6DL

SKU-B change for Power-Team 2nd source

Change U73 from 84.08692.037 to 84.01426.037

Change U75 from 84.07672.037 to 84.01712.037

Change U76 from 84.07672.037 to 84.01712.037

Change U77 from 84.08692.037 to 84.01426.037

Change U79 from 84.07672.037 to 84.01712.037

Change U41 from 84.08692.037 to 84.01426.037

Change U17 from 84.07672.037 to 84.01712.037

Change U40 from 84.07672.037 to 84.01712.037

Change TC35 from 79.33719.L01 to 77.C3371.051

Change TC36 from 79.33719.L01 to 77.C3371.051

Change TC38 from 79.33719.L01 to 77.C3371.051

Change TC14 from 79.33719.L01 to 77.C3371.051

Change TC15 from 79.33719.L01 to 77.C3371.051

Change L58 from 68.R5610.10P to 68.R5610.10D

Change L59 from 68.1R01B.10J to 68.1R01A.20A

Change L19 from 68.R5610.10P to 68.R5610.10D

JV71-MV DDR3 Madison

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HISTORY

Size	Document Number	Rev
A2	JV71-MV DDR3 Madison	-1

Date: Thursday, November 05, 2009 Sheet 62 of 62