

# Compal Confidential

## PEW52 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRII + ICH9M

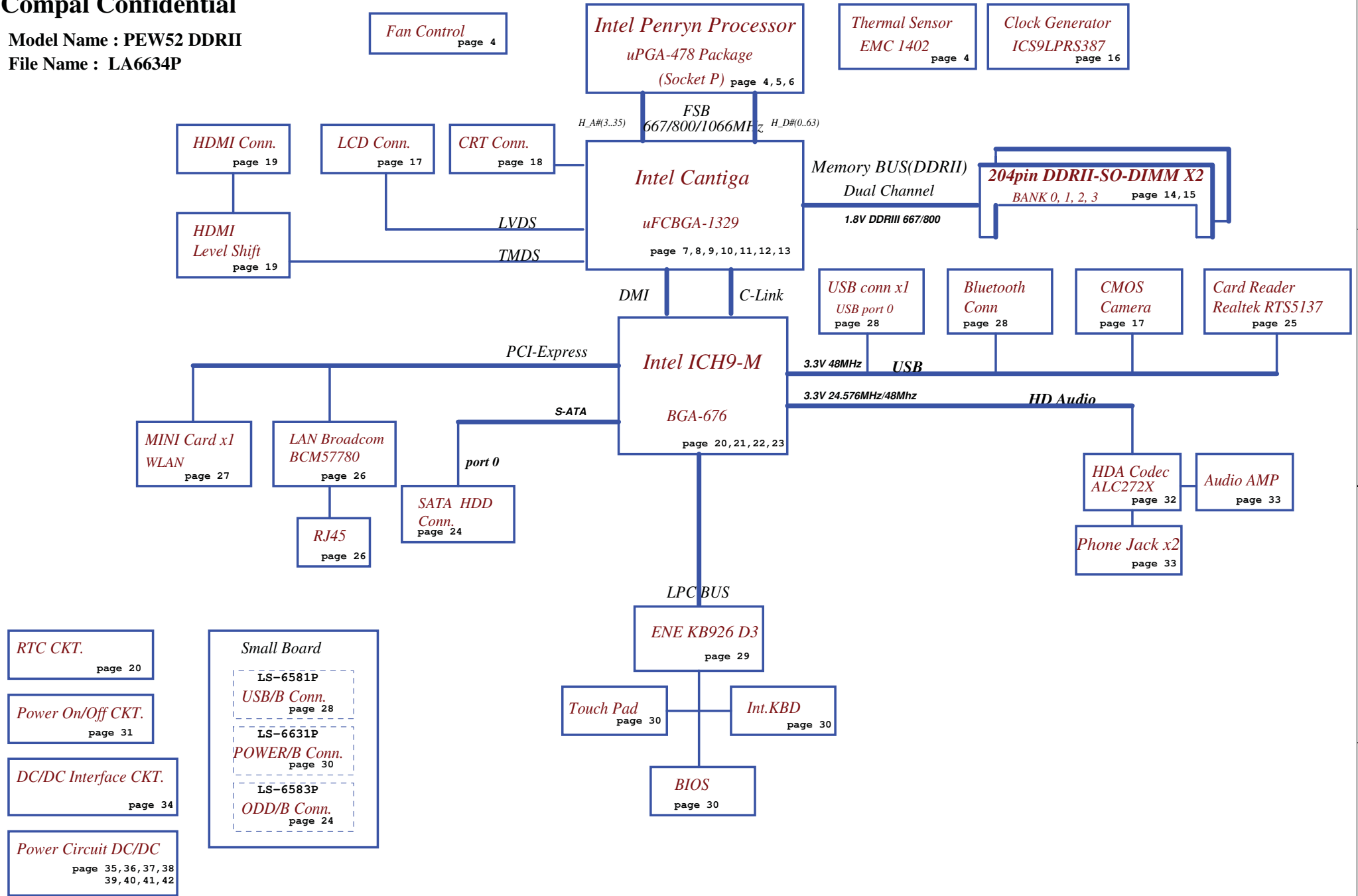
2010-08-06

REV: 0.1

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Model Name : PEW52 DDRII  
File Name : LA6634P



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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V power rail for DDR	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for LVDS	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	SMSC EMC1402	100 1100 b

## EC SM Bus2 address

## ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LVRS387, RTM890N)	1101 001Xb
DDR DIMM1	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

## BTO Option Table

BTO Item	BOM Structure
GM45 B3	GM@
GM40 A1	GLA1@
Bluetooth	BT@

## PCIE table

PCIE port1	
PCIE port2	Wireless Card
PCIE port3	PCIE LAN
PCIE port4	
PCIE port5	
PCIE port6	

## SATA table

SATA port0	HDD
SATA port1	ODD
SATA port2	
SATA port3	
SATA port4	
SATA port5	

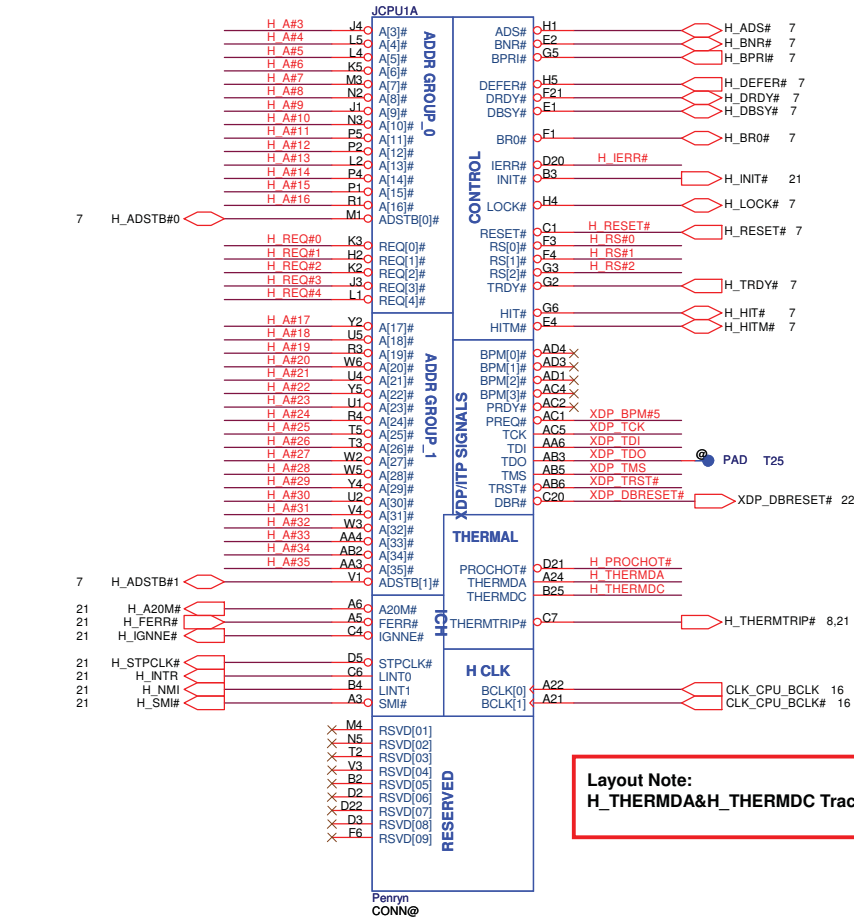
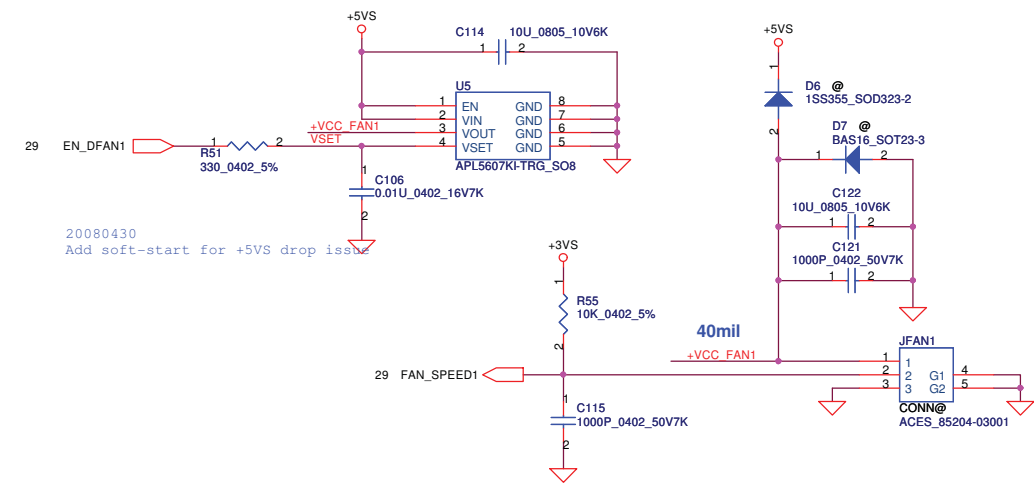
## USB table

EHCI1	UHCI1	Port0	MB USB Conn.
		Port1	USB/B Conn.
	UHCI2	Port2	
		Port3	CMOS Camera
		Port4	Card Reader
EHCI2	UHCI3	Port5	
		Port6	USB/B Conn.
	UHCI4	Port7	
		Port8	Blue Tooth
		Port9	
	UHCI5	Port10	Wireless Card
		Port11	

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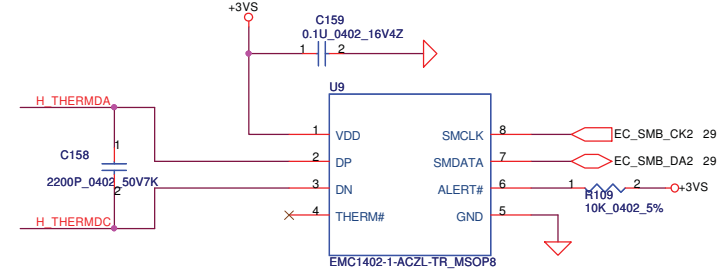
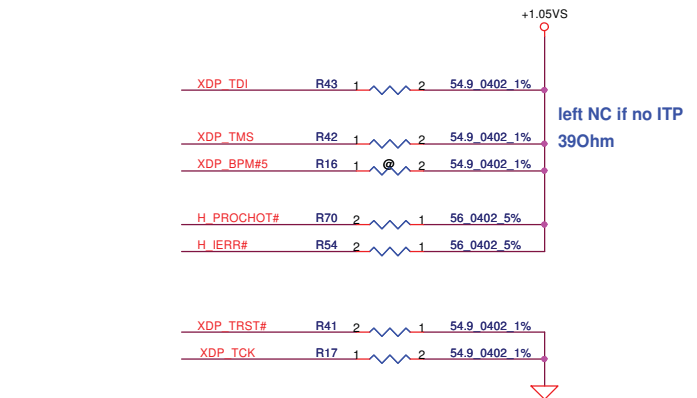
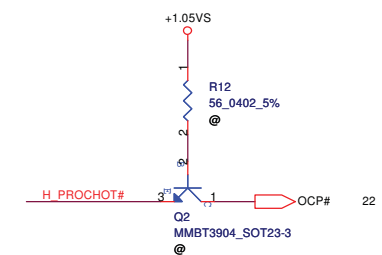
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- 7 H\_REQ#[0..4] H\_REQ#[0..4]
- 7 H\_RS#[0..2] H\_RS#[0..2]

### FAN1 Conn



**Layout Note:**  
H\_THERMDA&H\_THERMDC Trace / Space = 10 / 10 mil

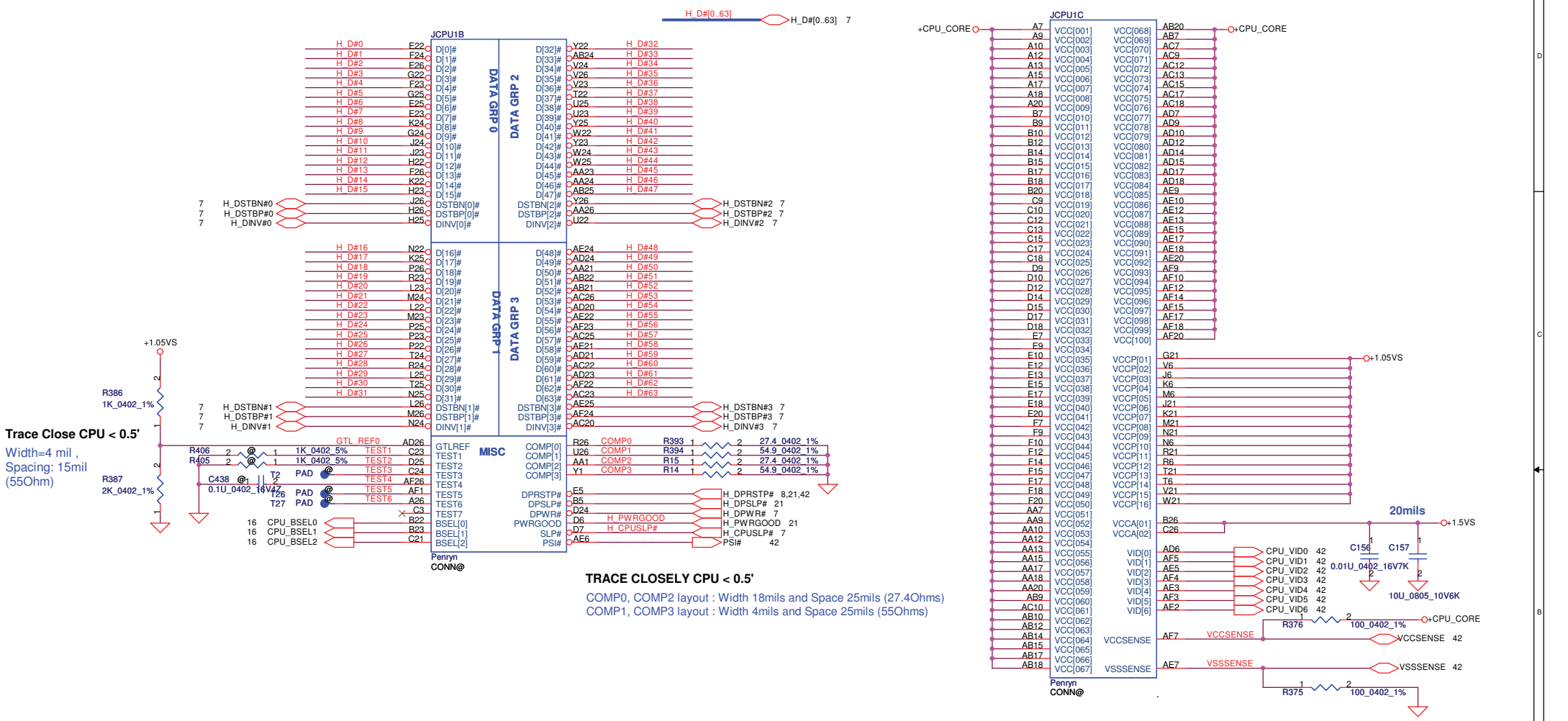
BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166



**PCB**

LA-6634P MB Rev0: DA60000JS00  
 LA-6634P MB Rev1: DA60000JS10  
 LA-6634P MB with Small Board Rev1:  
 PCB PEW72 LA-6631P LS-6631P/6581P/6583P

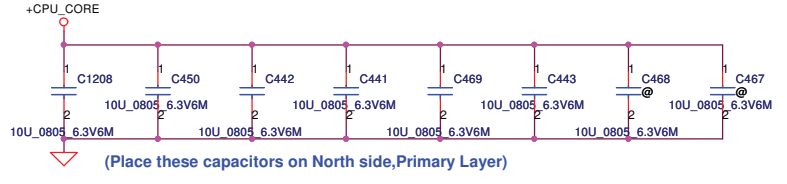
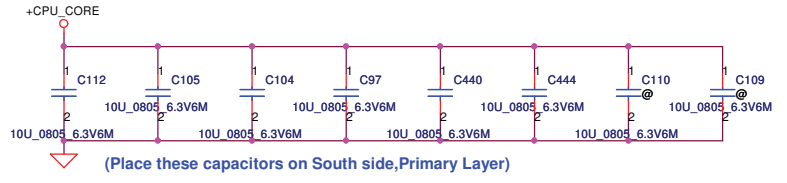
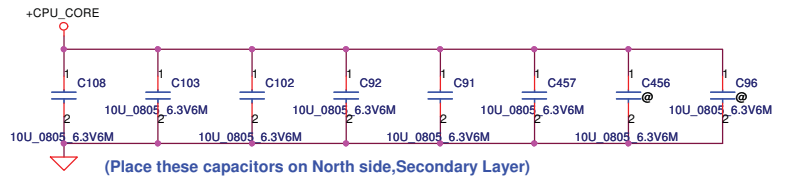
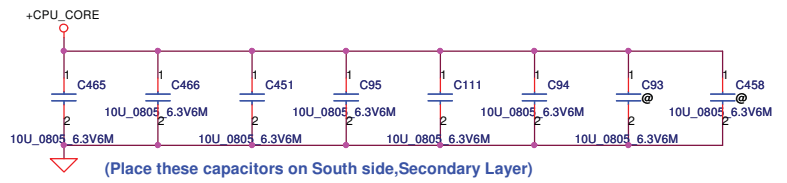
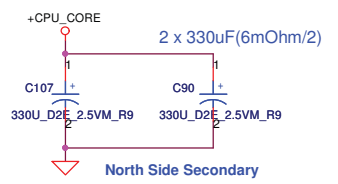
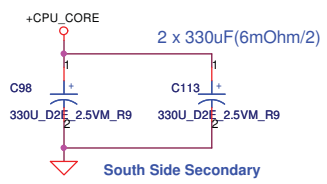
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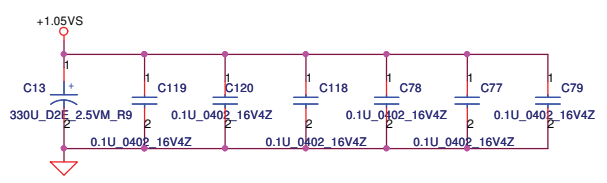
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JCPU1D		
A4	VSS 001	VSS 082
A8	VSS 002	VSS 083
A11	VSS 003	VSS 084
A14	VSS 004	VSS 085
A16	VSS 005	VSS 086
A19	VSS 006	VSS 087
A23	VSS 007	VSS 088
AF2	VSS 008	VSS 089
B6	VSS 009	VSS 090
B8	VSS 010	VSS 091
B11	VSS 011	VSS 092
B13	VSS 012	VSS 093
B16	VSS 013	VSS 094
B19	VSS 014	VSS 095
B21	VSS 015	VSS 096
B24	VSS 016	VSS 097
C5	VSS 017	VSS 098
C8	VSS 018	VSS 099
C11	VSS 019	VSS 100
C14	VSS 020	VSS 101
C16	VSS 021	VSS 102
C19	VSS 022	VSS 103
C2	VSS 023	VSS 104
C22	VSS 024	VSS 105
C25	VSS 025	VSS 106
D1	VSS 026	VSS 107
D4	VSS 027	VSS 108
D8	VSS 028	VSS 109
D11	VSS 029	VSS 110
D13	VSS 030	VSS 111
D16	VSS 031	VSS 112
D19	VSS 032	VSS 113
D23	VSS 033	VSS 114
D26	VSS 034	VSS 115
E3	VSS 035	VSS 116
E6	VSS 036	VSS 117
E8	VSS 037	VSS 118
E11	VSS 038	VSS 119
E14	VSS 039	VSS 120
E16	VSS 040	VSS 121
E19	VSS 041	VSS 122
E21	VSS 042	VSS 123
E24	VSS 043	VSS 124
F5	VSS 044	VSS 125
F8	VSS 045	VSS 126
F11	VSS 046	VSS 127
F13	VSS 047	VSS 128
F16	VSS 048	VSS 129
F19	VSS 049	VSS 130
F2	VSS 050	VSS 131
F22	VSS 051	VSS 132
F25	VSS 052	VSS 133
G4	VSS 053	VSS 134
G1	VSS 054	VSS 135
G23	VSS 055	VSS 136
G26	VSS 056	VSS 137
H3	VSS 057	VSS 138
H6	VSS 058	VSS 139
H21	VSS 059	VSS 140
H24	VSS 060	VSS 141
J2	VSS 061	VSS 142
J5	VSS 062	VSS 143
J22	VSS 063	VSS 144
J25	VSS 064	VSS 145
K1	VSS 065	VSS 146
K4	VSS 066	VSS 147
K23	VSS 067	VSS 148
K26	VSS 068	VSS 149
L3	VSS 069	VSS 150
L6	VSS 070	VSS 151
L21	VSS 071	VSS 152
L24	VSS 072	VSS 153
M2	VSS 073	VSS 154
M5	VSS 074	VSS 155
M22	VSS 075	VSS 156
M25	VSS 076	VSS 157
N1	VSS 077	VSS 158
N4	VSS 078	VSS 159
N23	VSS 079	VSS 160
N26	VSS 080	VSS 161
P3	VSS 081	VSS 162
		VSS 163
		AF25

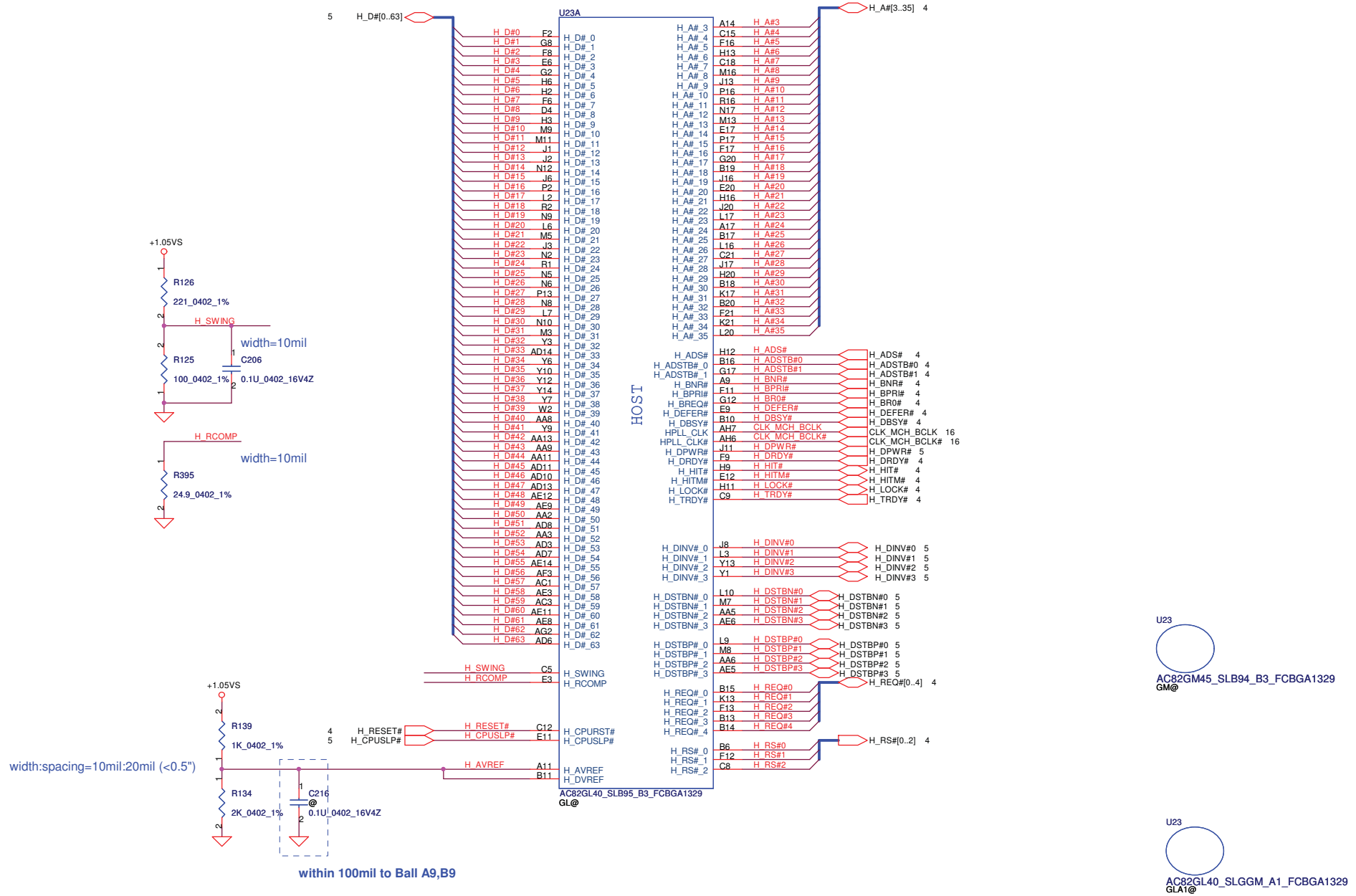
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CONN



+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



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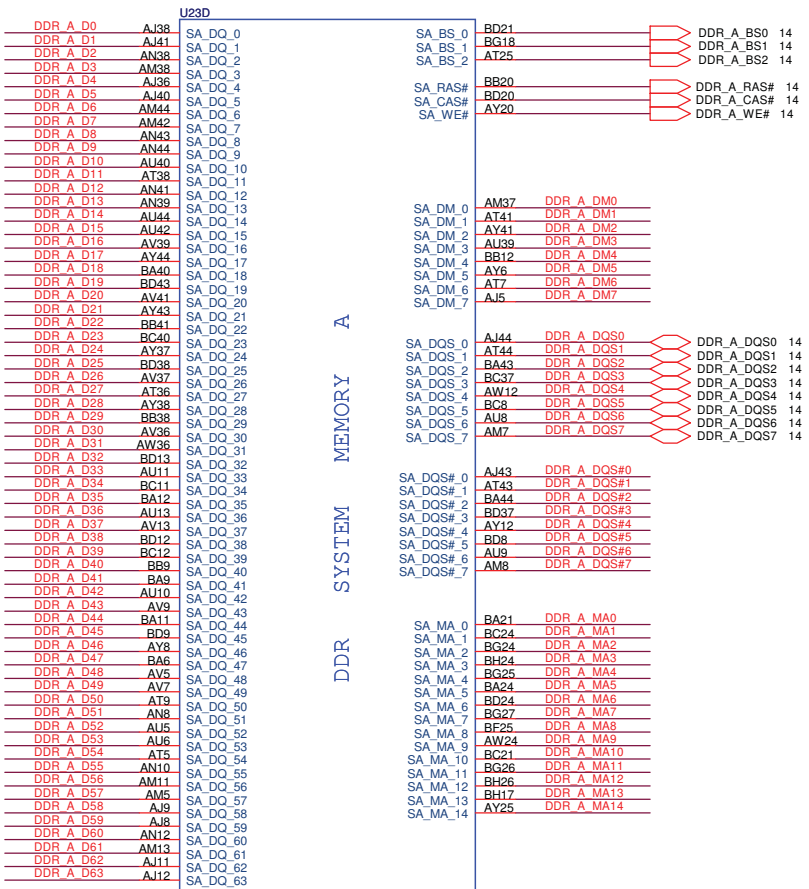


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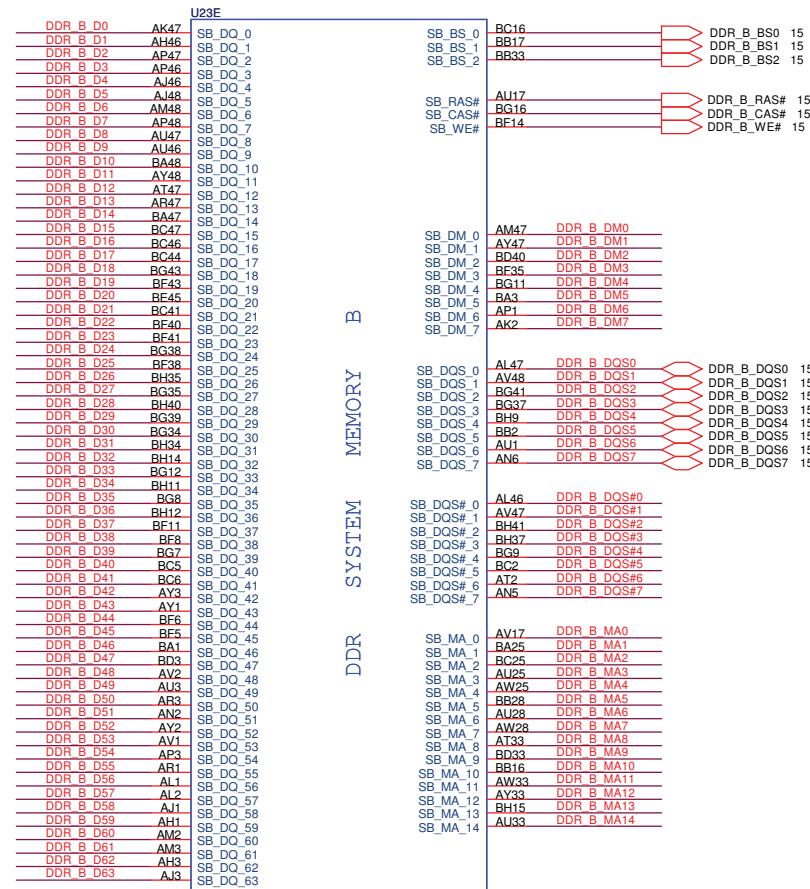






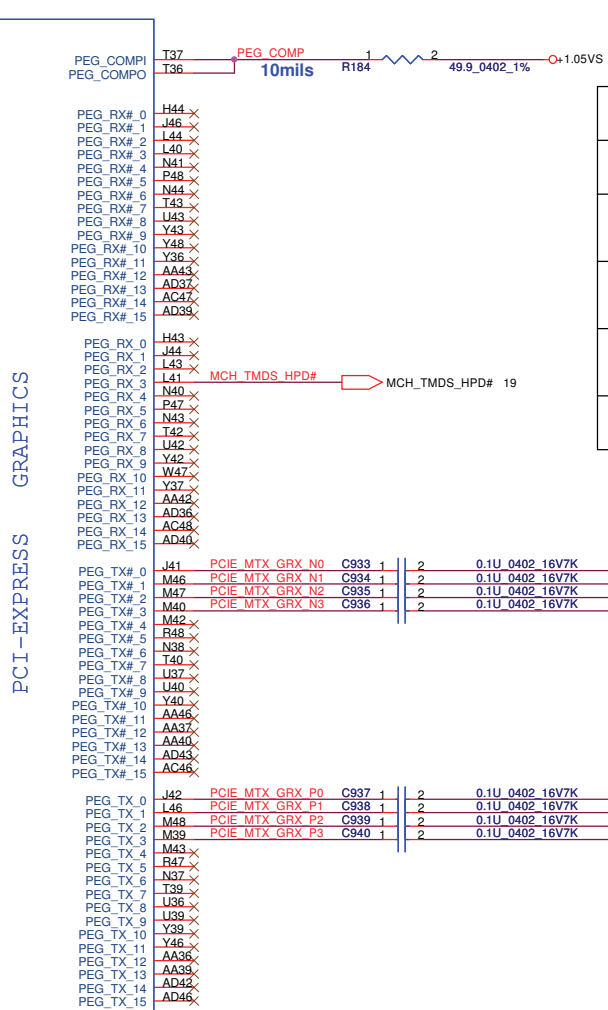
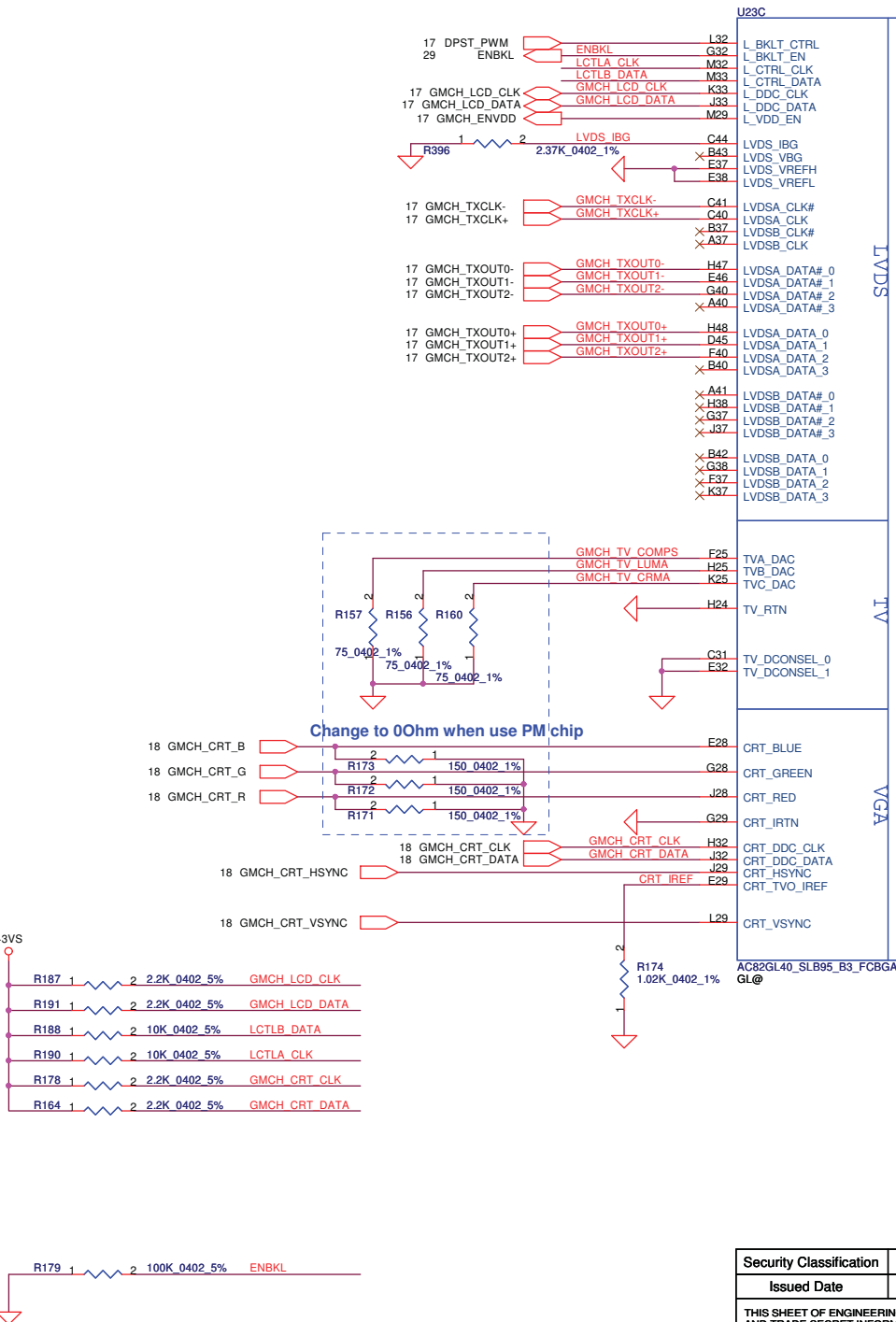


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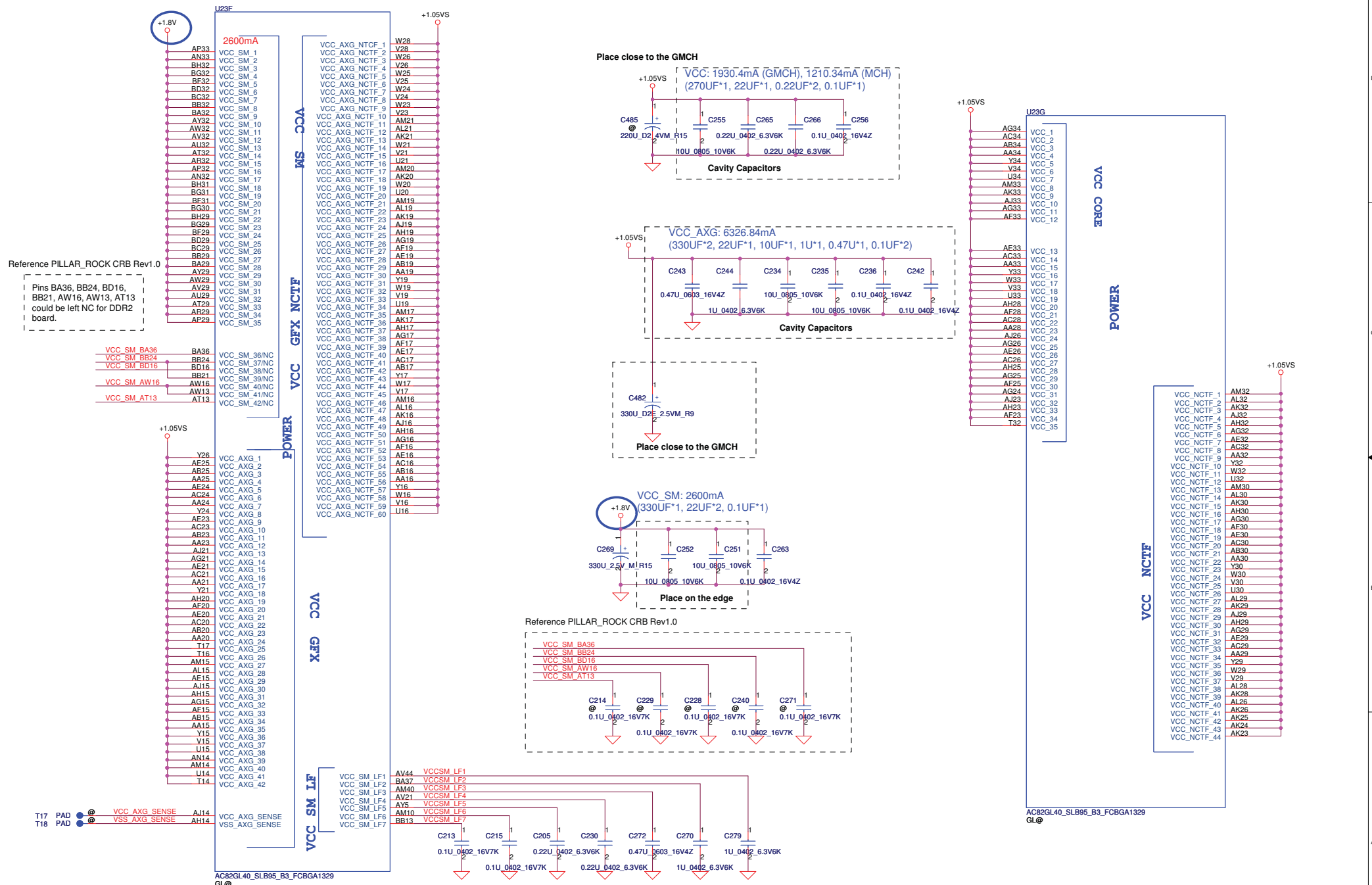
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### Intel Cantiga TMDs Pin Definition

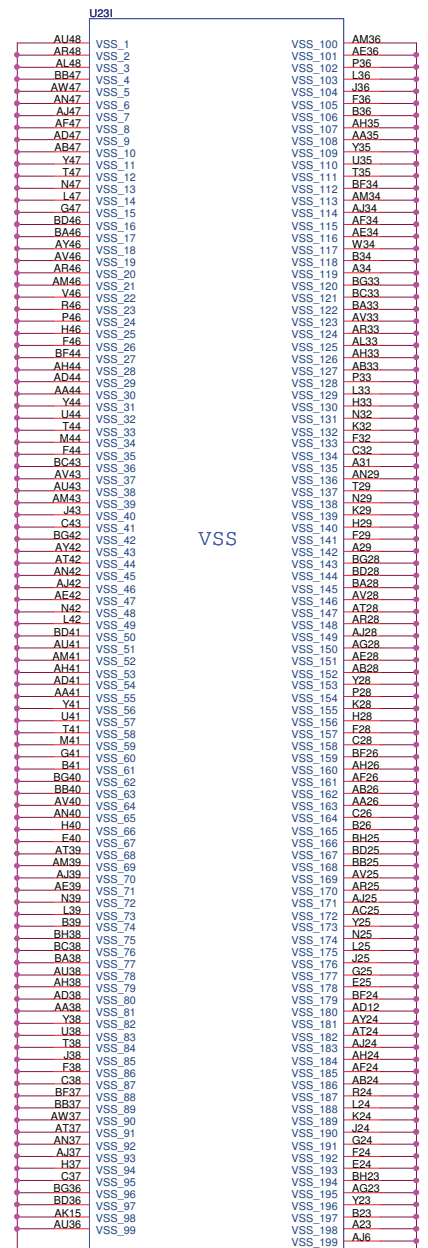
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TMDS_B_DATA1#	PEG_TXN_1
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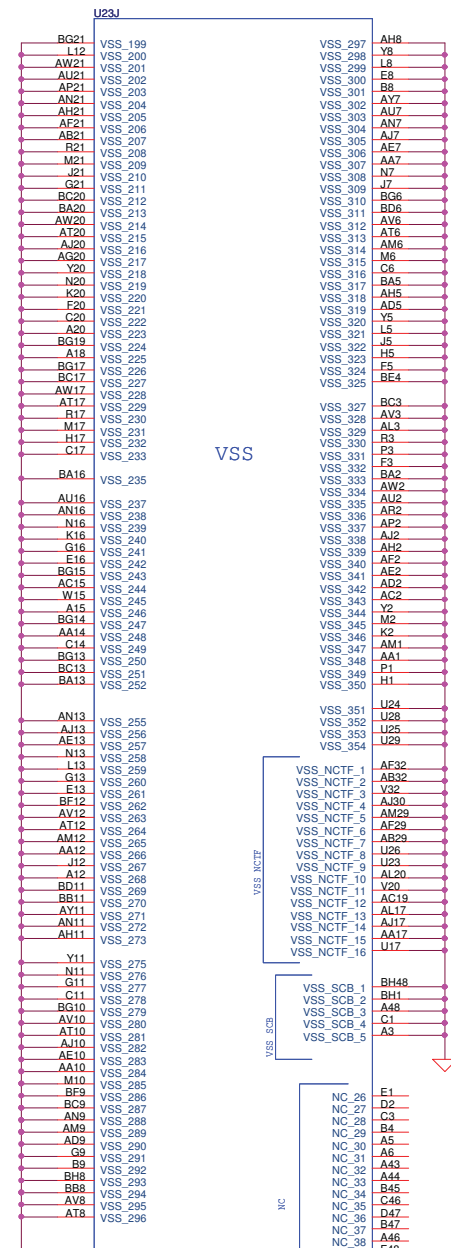
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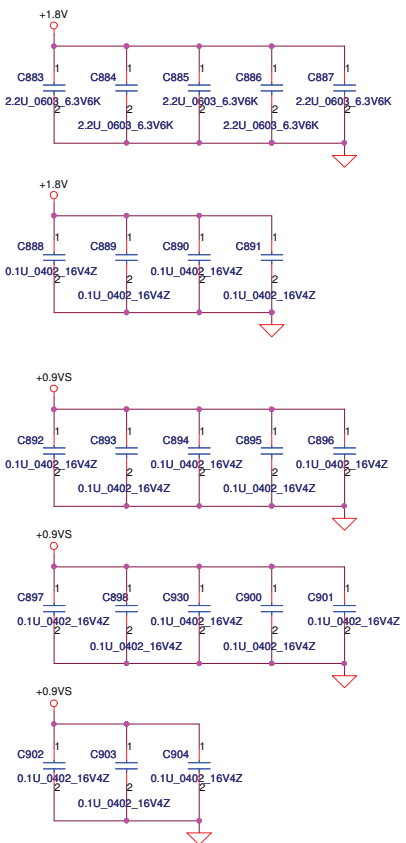
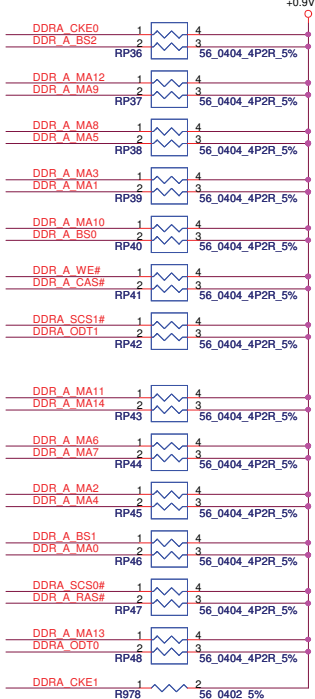
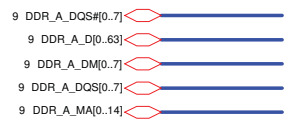
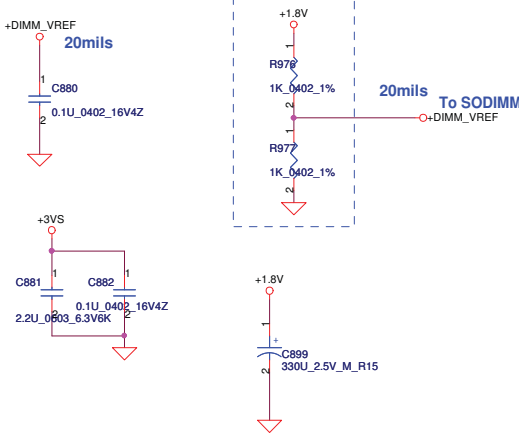
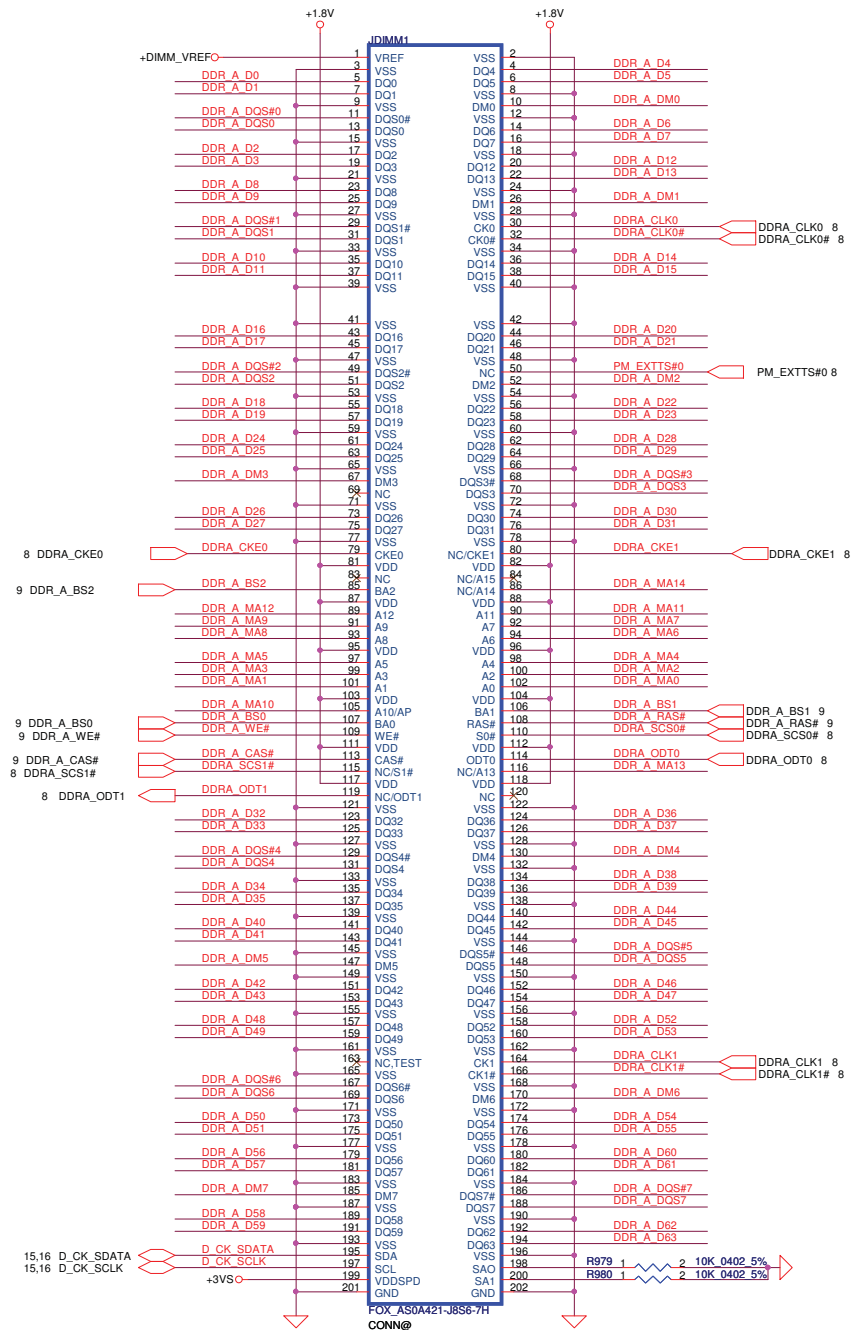


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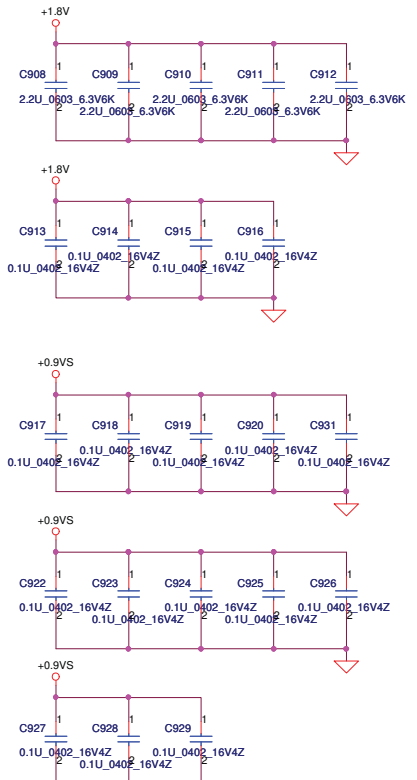
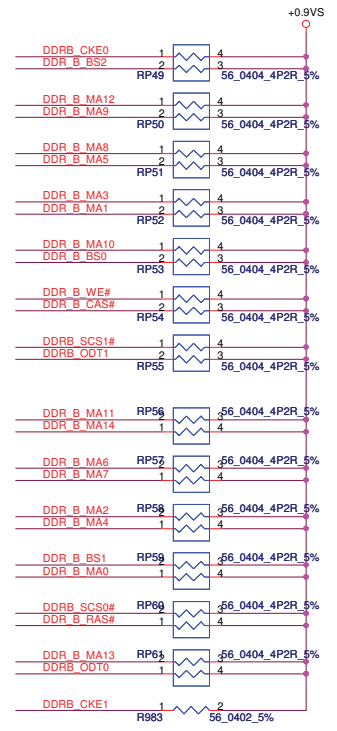
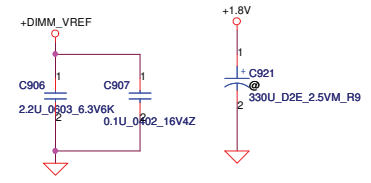
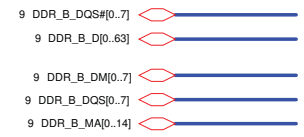
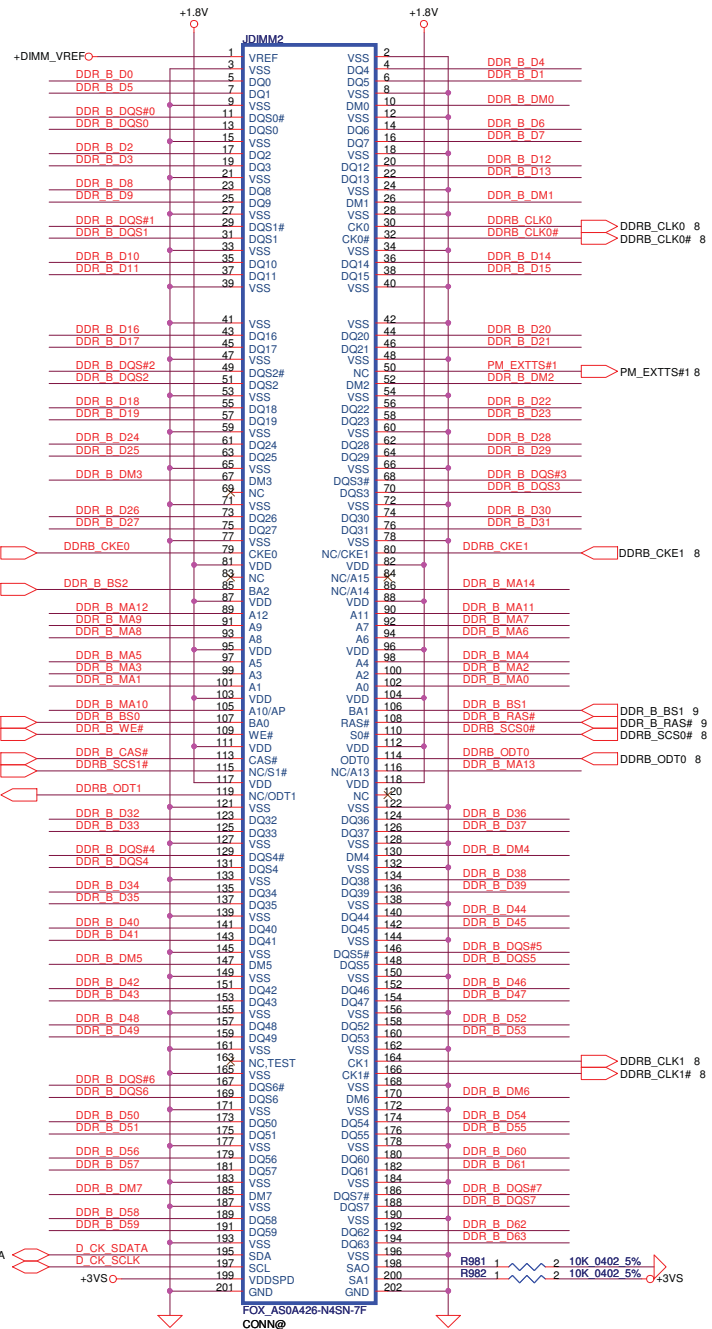
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Cantiga GMCH(7/7)-GND			
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**DIMM1 STD H:8mm (BOT)**

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Date:	Friday, August 06, 2010	Sheet	14	of	44	



**DIMM2 STD H:4mm (BOT)**

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Document Number	PEWS2 M/B Schematic		Rev 0.2
Date	Friday, August 06, 2010	Sheet	15 of 44

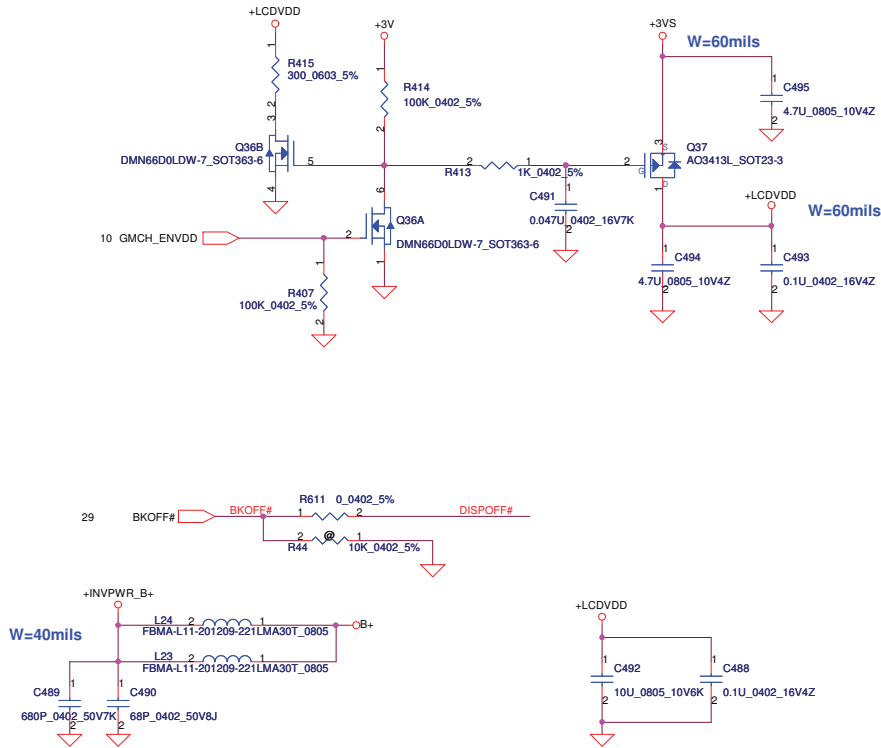
**Compal Electronics, Inc.**

**DDR2-SODIMM SLOT2**

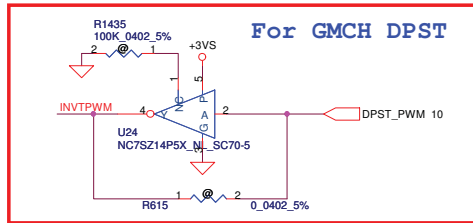
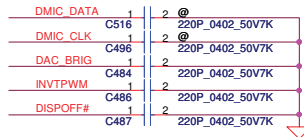
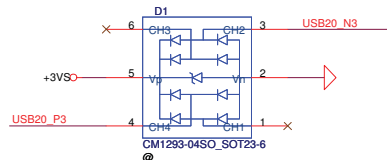
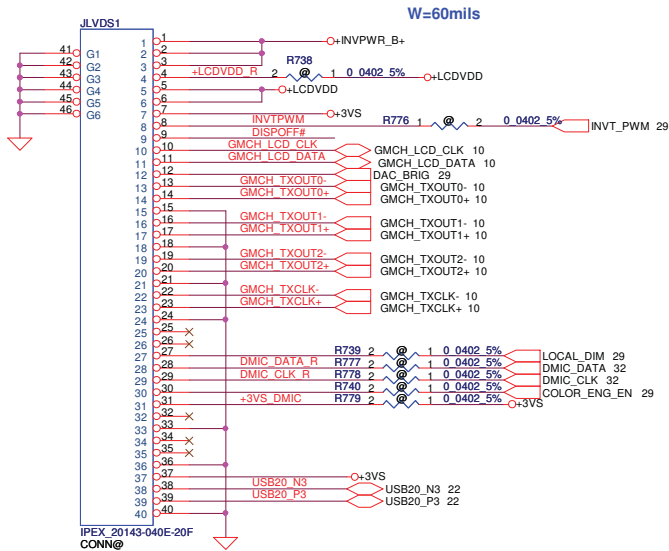




# LCD POWER CIRCUIT

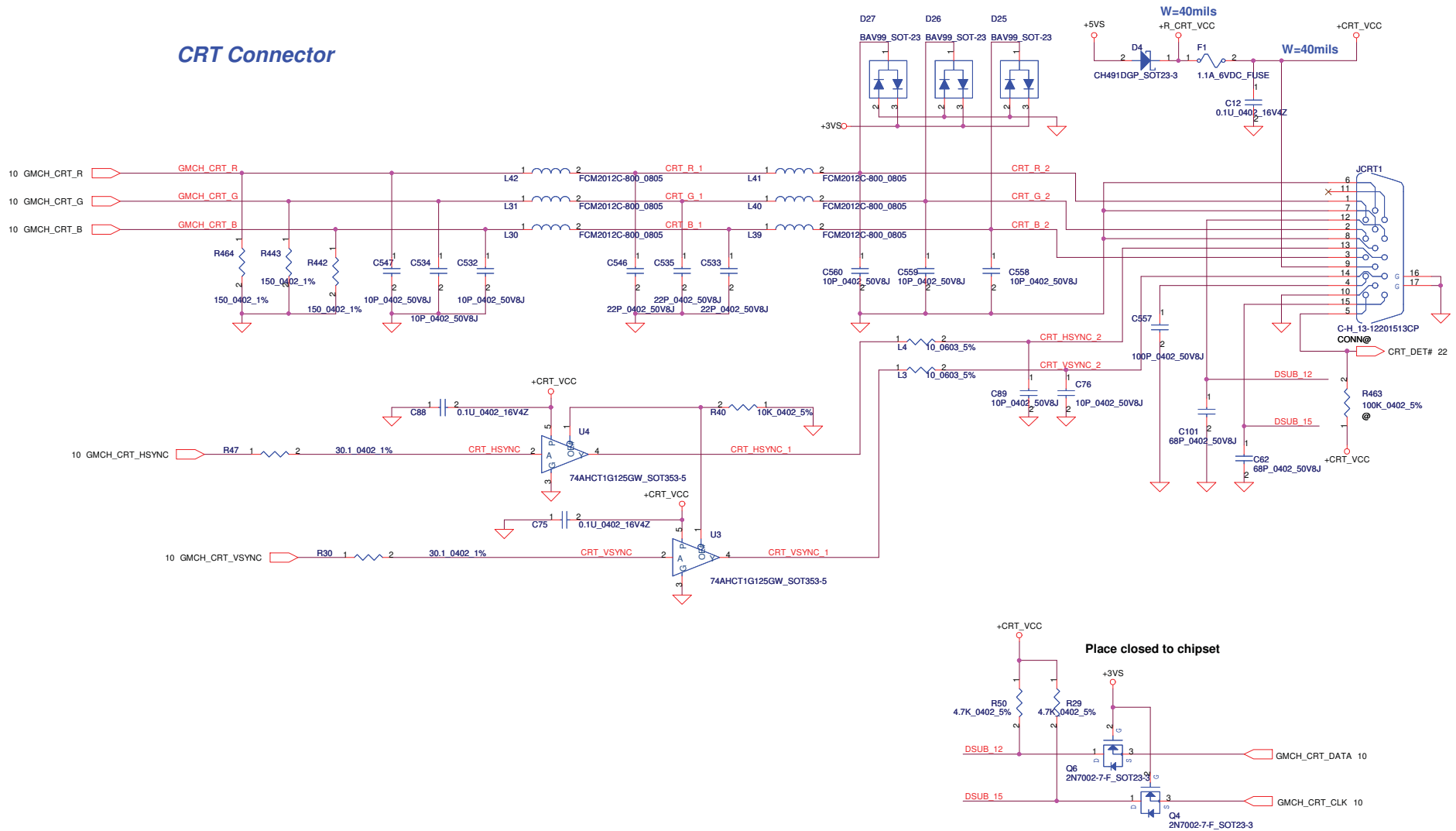


## LCD/PANEL BD. Conn.

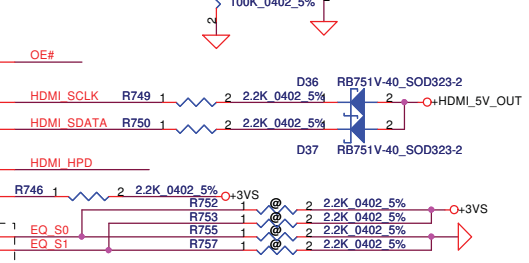
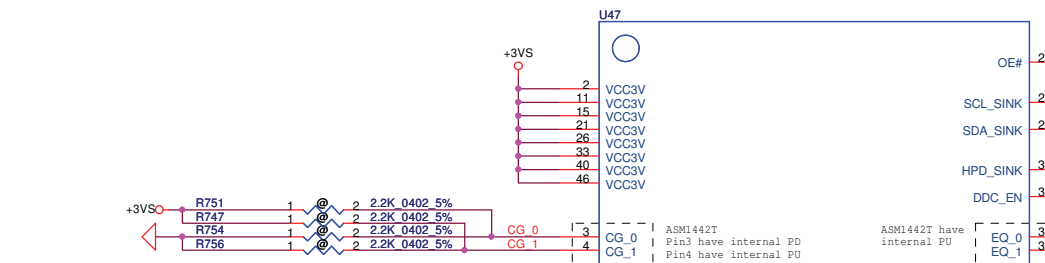
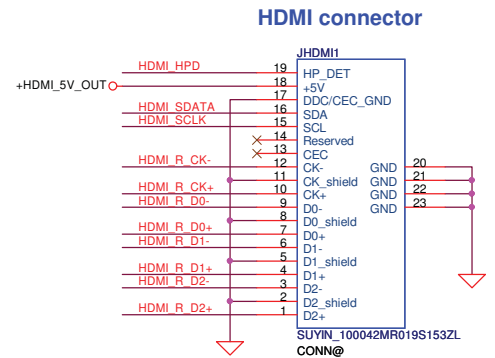
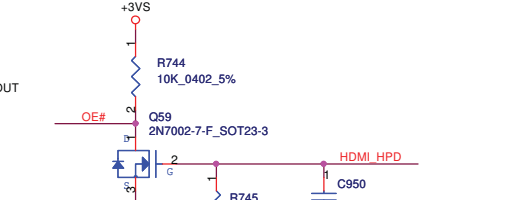
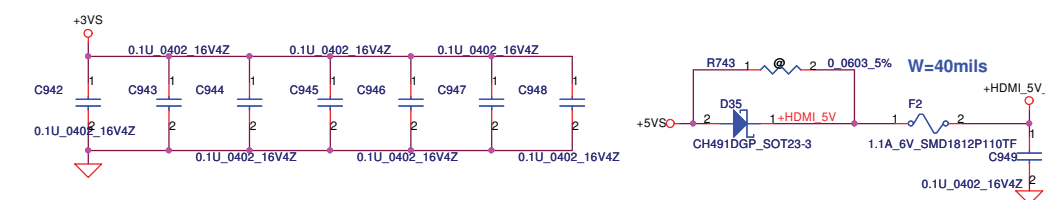


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				PEW52 M/B LA-6634P Schematic
				Rev 0.2
				Date: Friday, August 06, 2010   Sheet 17 of 44

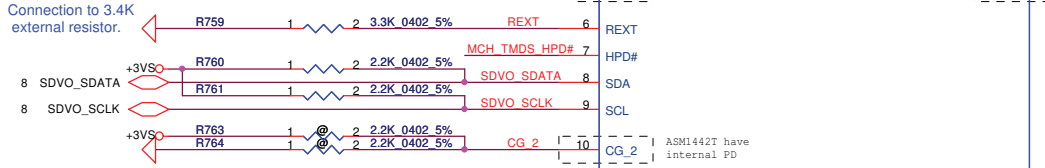
# CRT Connector



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				PEW52 M/B LA-6634P Schematic	0.2
				Date: Friday, August 06, 2010	Sheet 18 of 44

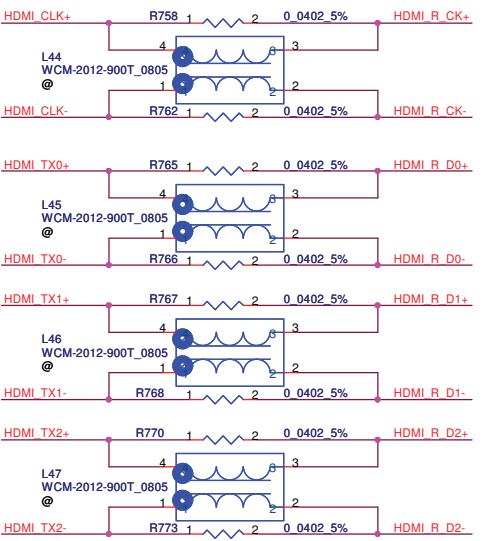
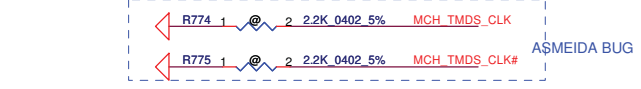
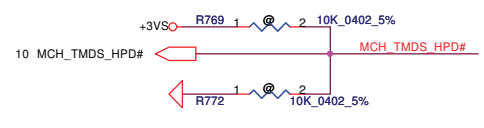
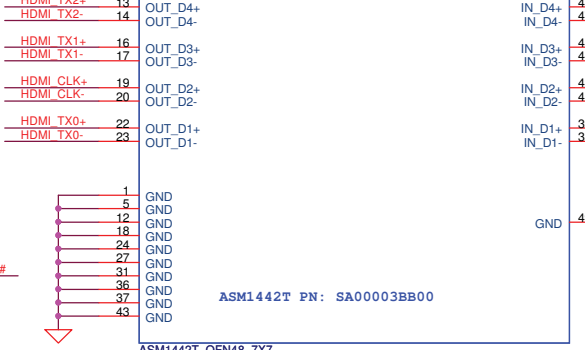


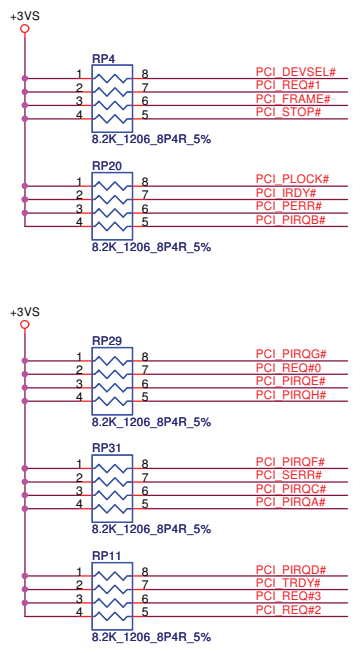
SM070001310 400ma 90ohm@100mhz DCR 0.3



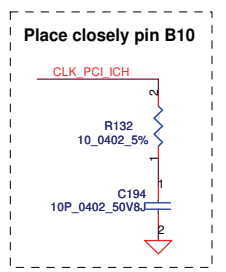
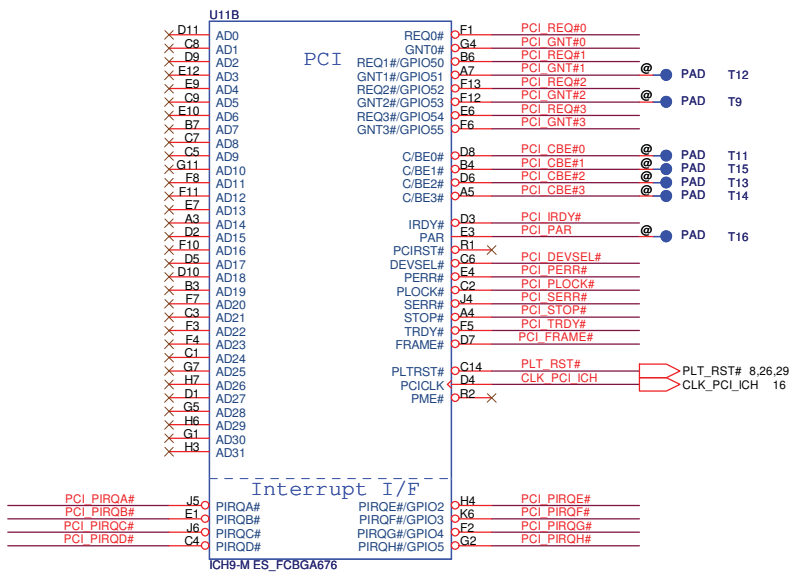
EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)

CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

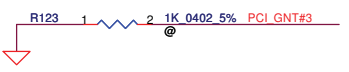




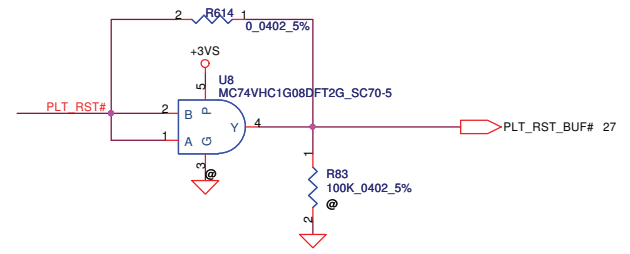
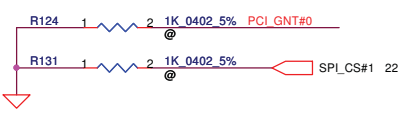
**DMI for ESI-compatible operation**  
**PCI\_GNT#1** Low= DMI for ESI-compatible operation  
 High= Default\* (Internal pull-up)

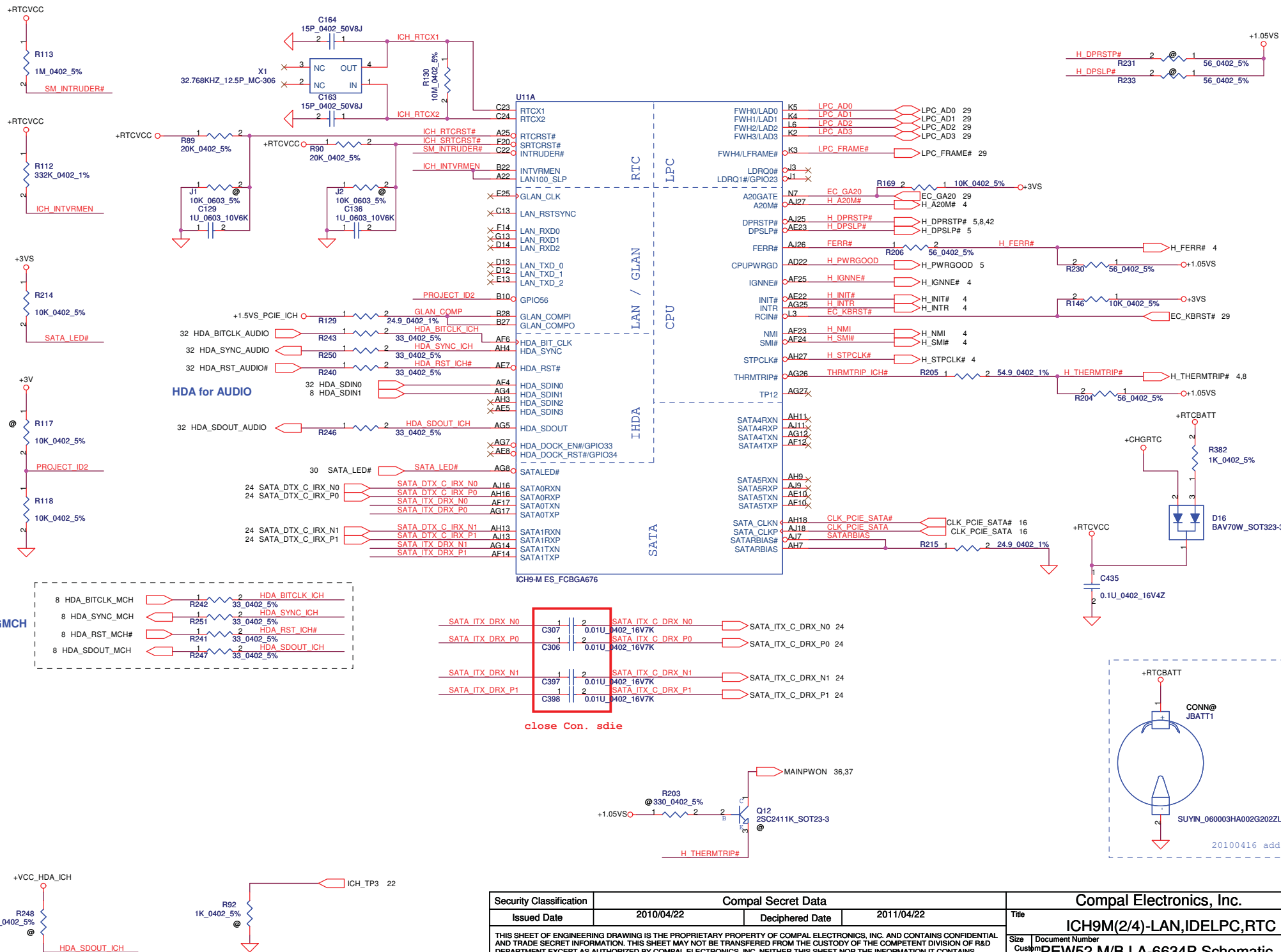


**A16 Swap Override Strap**  
**PCI\_GNT#3** Low= A16 swap override Enable  
 High= Default\*

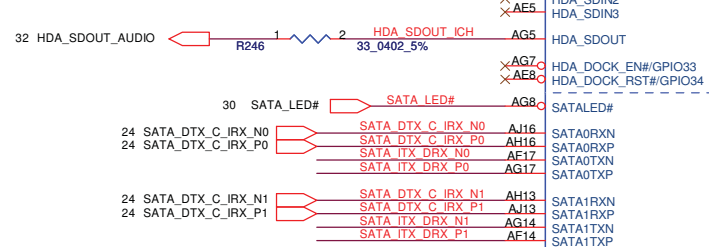


Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

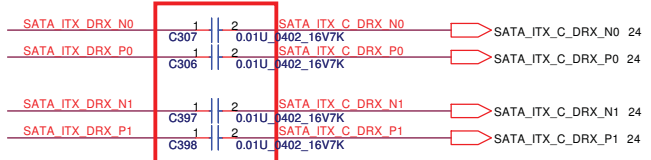
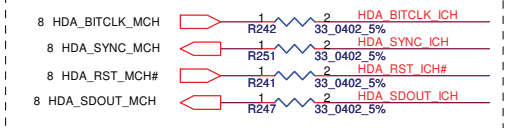




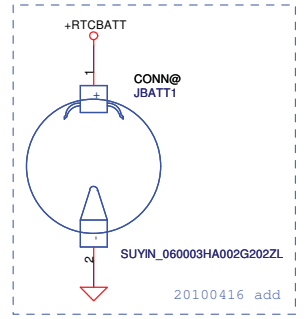
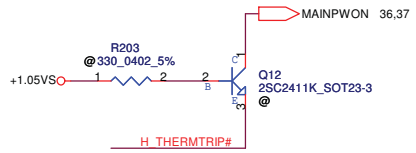
**HDA for AUDIO**



**HDA for GMCH**

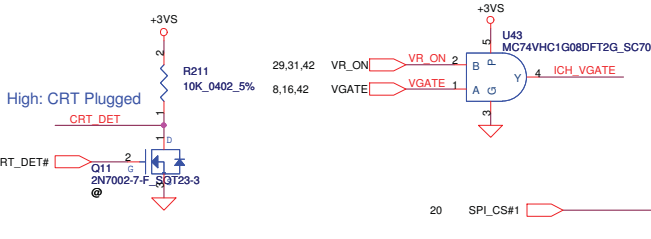
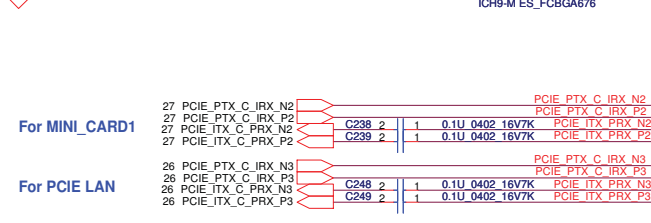
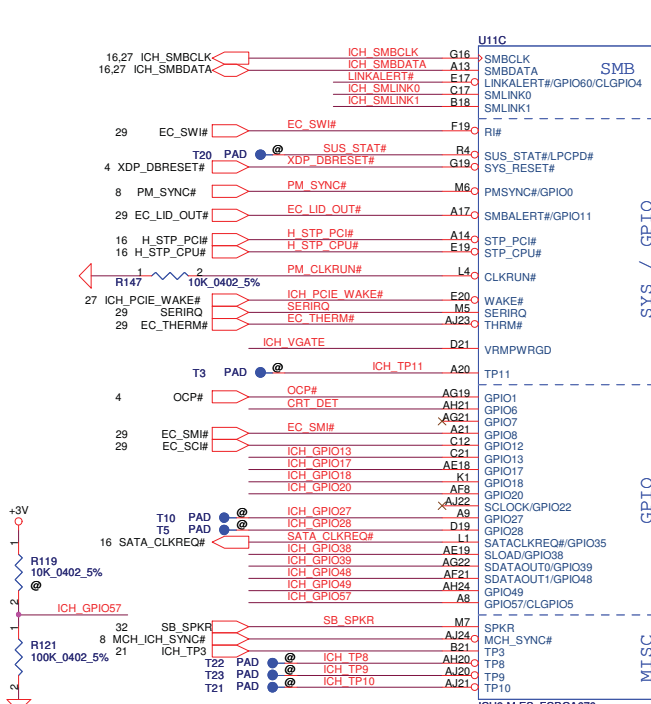
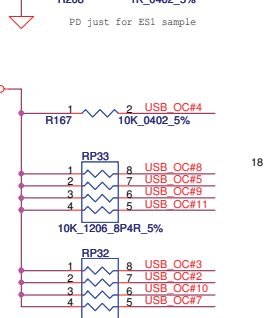
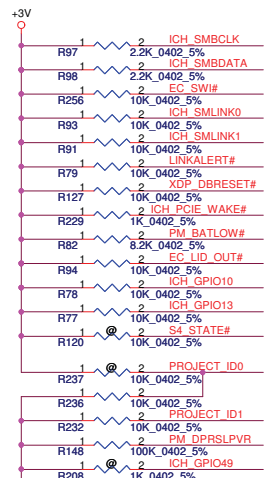
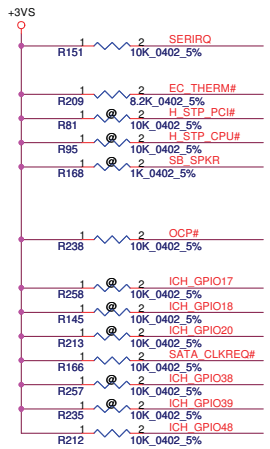


close Con. sdie

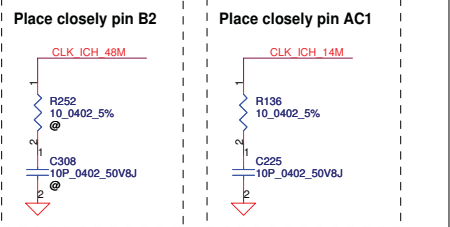
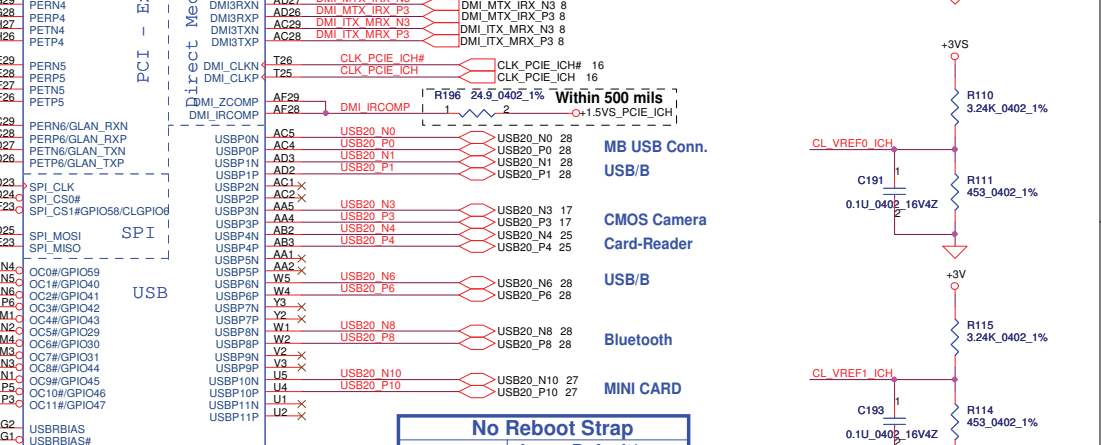
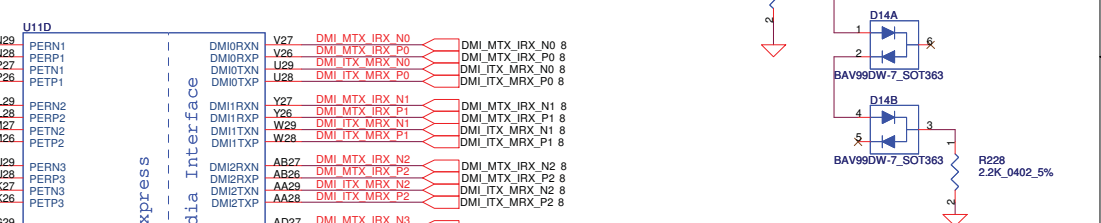
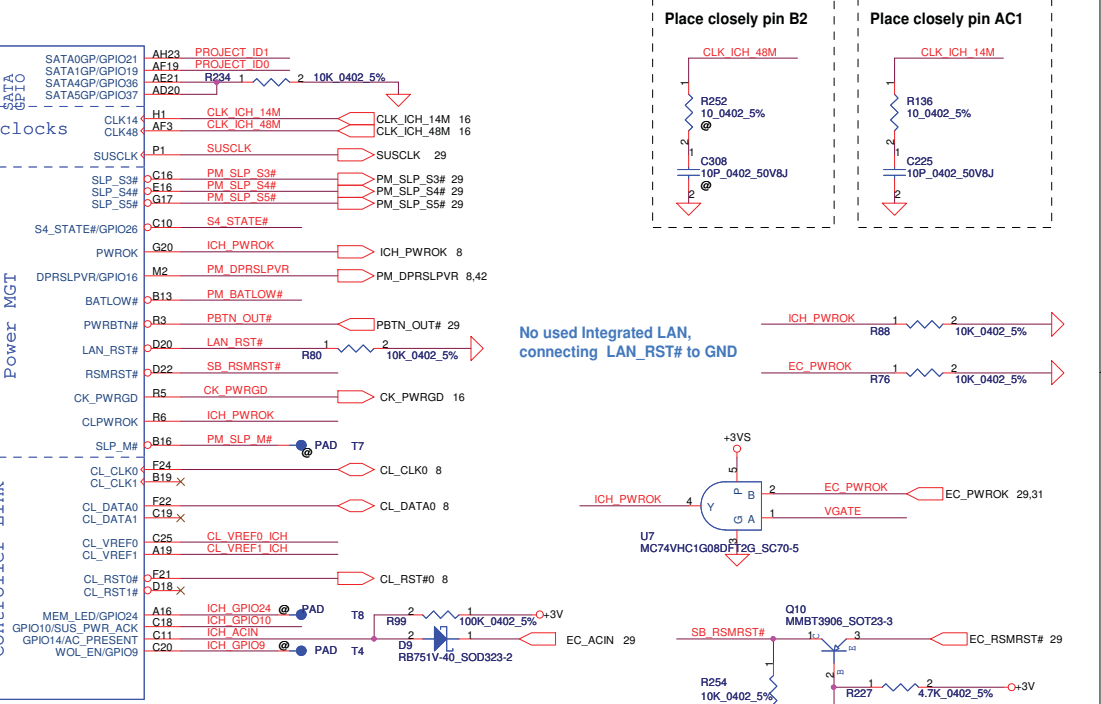


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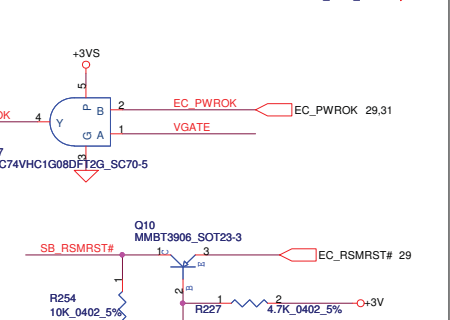




Project_ID0	Project_ID1	Project_ID2
0	0	0
1	0	0



No used Integrated LAN, connecting LAN\_RST# to GND



No Reboot Strap  
SB\_SPKR Low= Default\* High= "No Reboot"

Internal TPM Strap  
Low= Disable\* High= iTPM enable by MCH strap

DMI Termination Voltage  
Low= Desktop used High= Mobile\* (Internal pull-up)

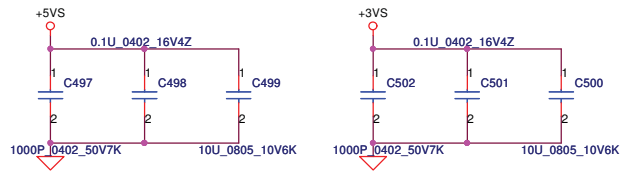
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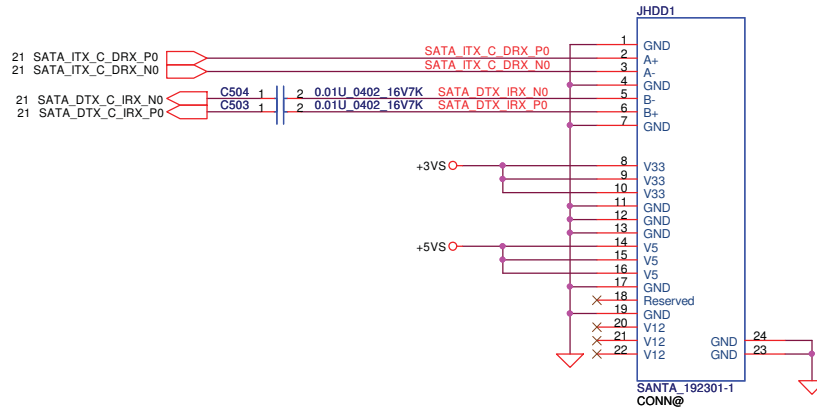
Compal Electronics, Inc.	
Title	ICH9M(3/4)-USB,GPIO,PCIE
Docment Number	PEW52 M/B LA-6634P Schematic
Date	Friday, August 06, 2010
Sheet	22 of 44



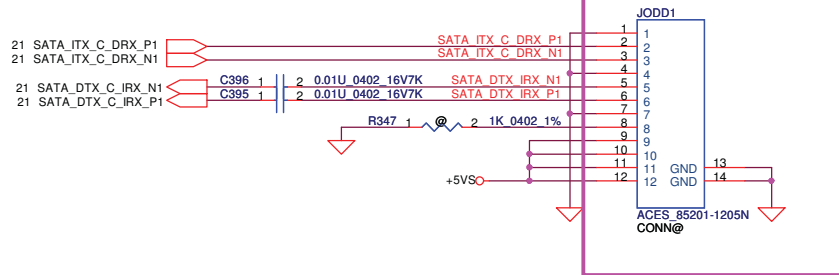




### SATA HDD Conn.

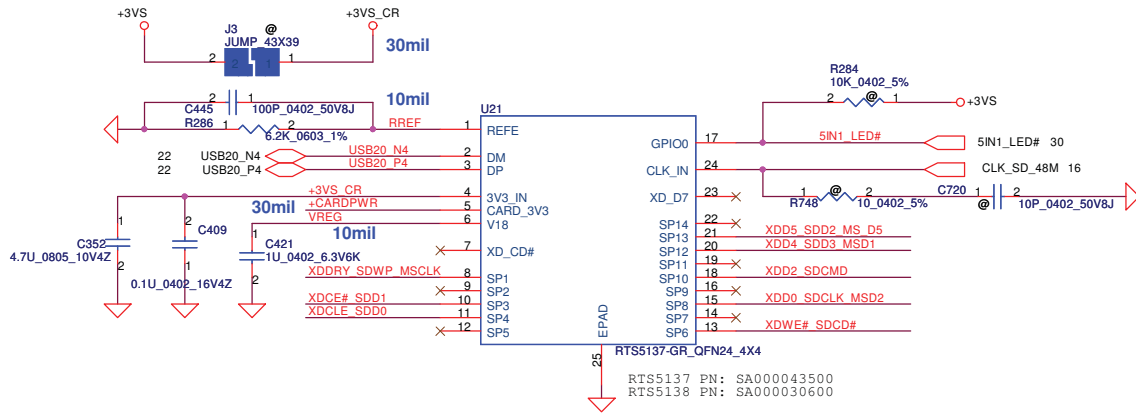


### SATA ODD Conn. LS-6583

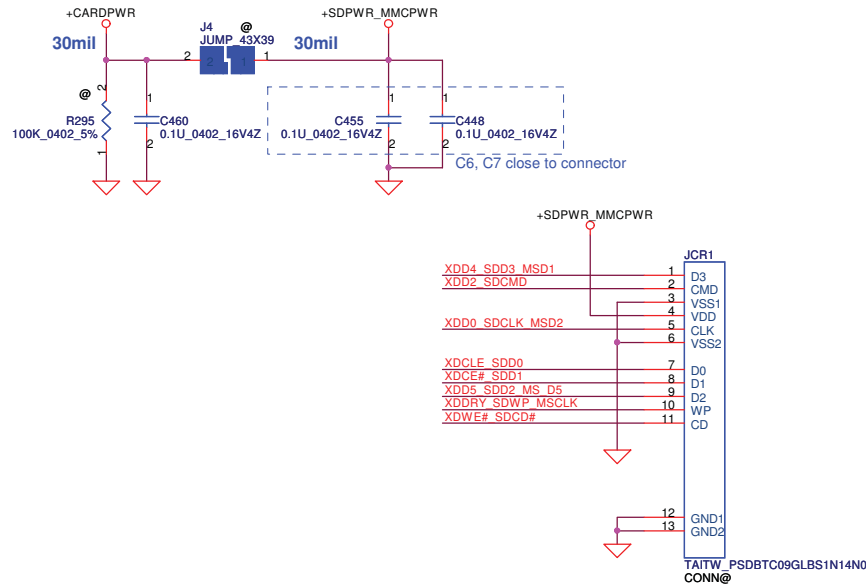


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Size	Document Number	PEW52 M/B LA-6634P Schematic			Rev
Customer	Date	Friday, August 06, 2010	Sheet	24	of 44

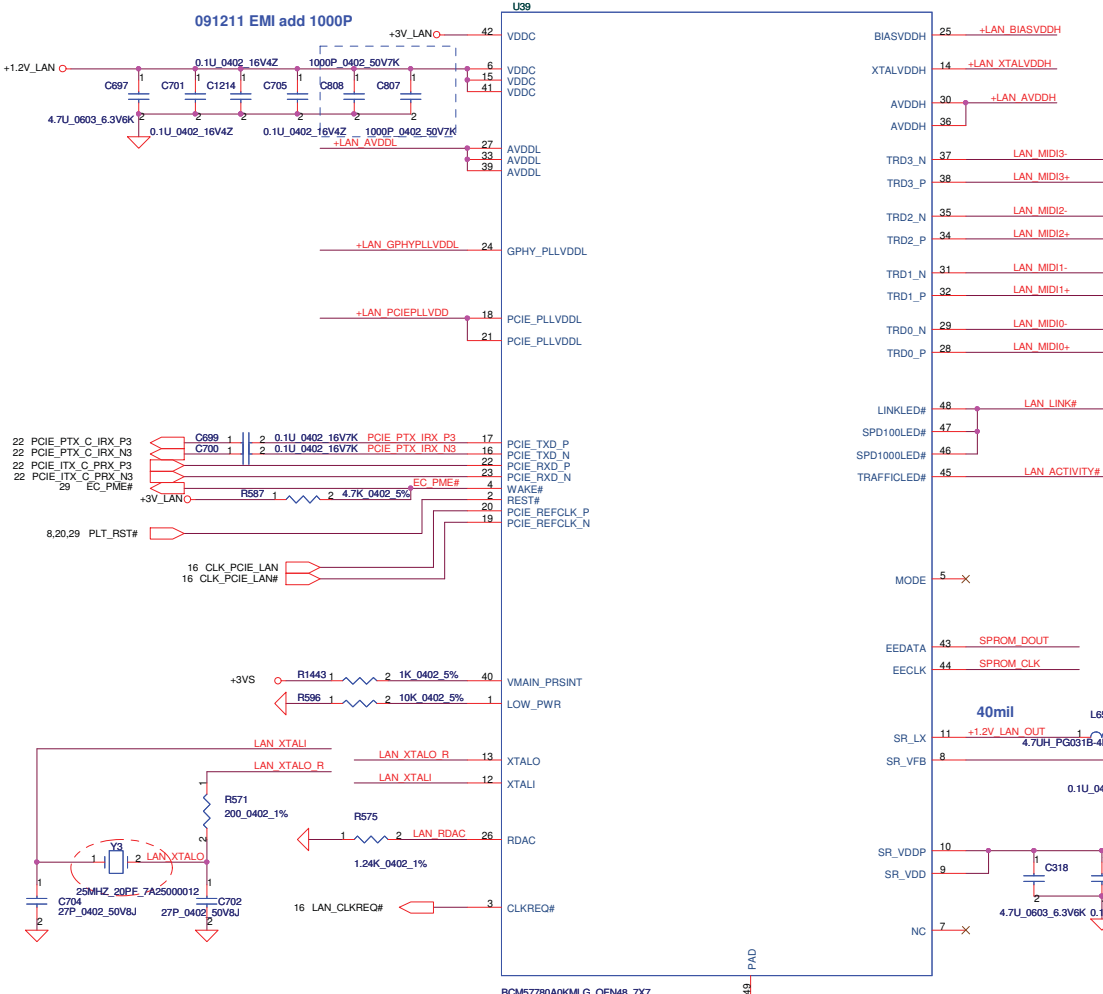
# Card Reader RTS5138 / RTS5137 (only SD+MMC function)



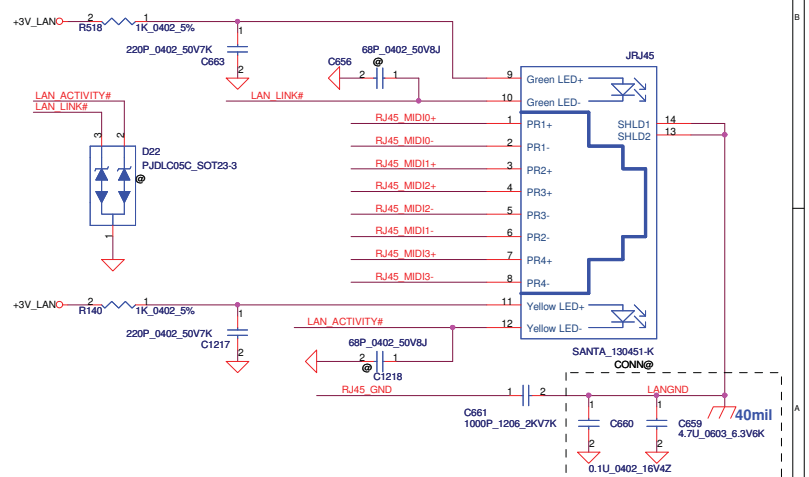
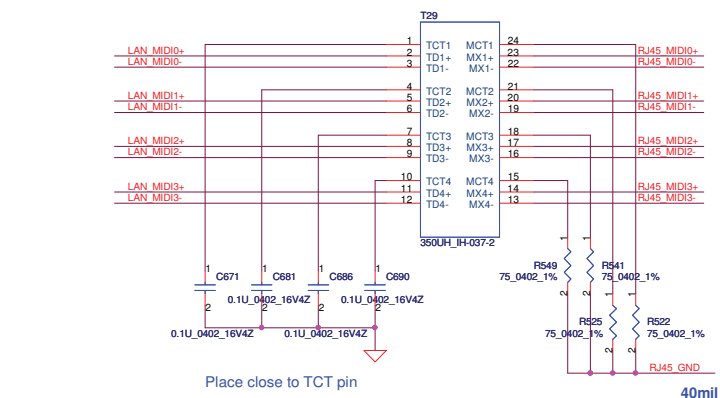
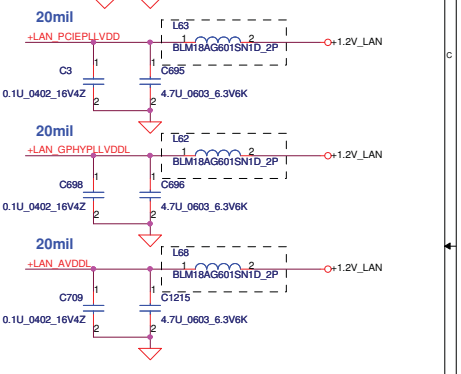
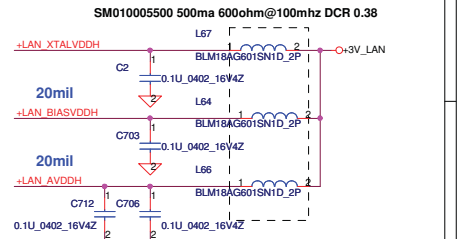
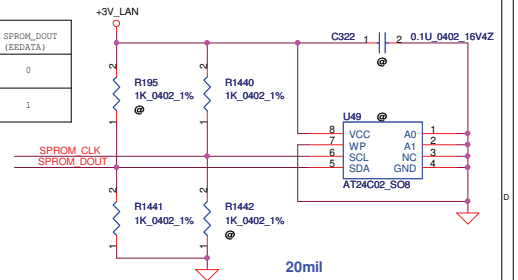
## Card Reader Connector



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Date:	Friday, August 06, 2010	Sheet	25 of 44	



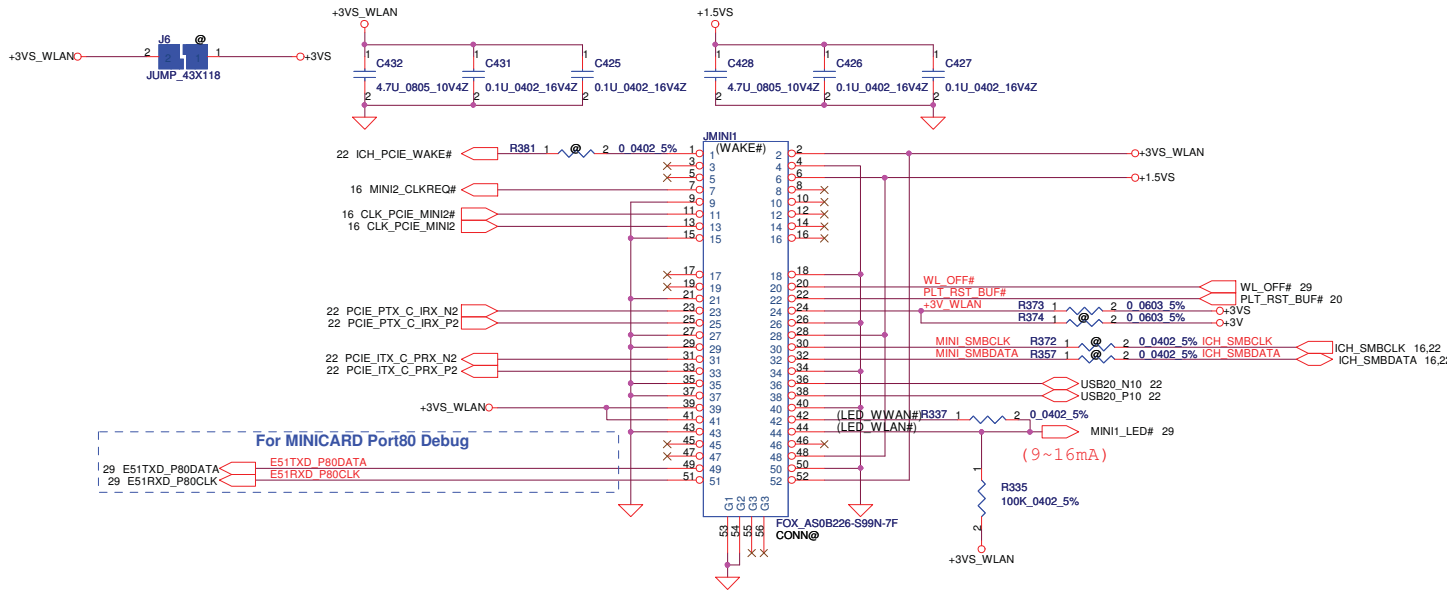
	SPROM_CLK (FECLK)	SPROM_DOUT (FE2DATA)
On chip	1	0
AT24C02	1	1



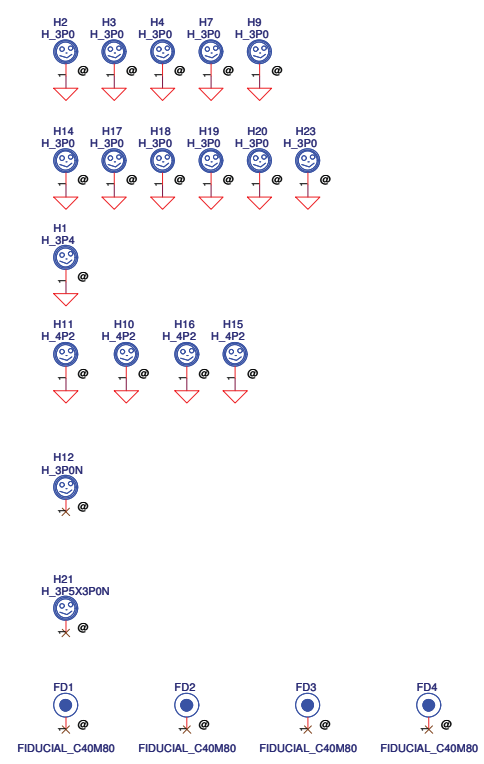
BOTH HAND: S X'FORM\_GST5009-D LF LAN, SP050006B00  
 TIMAG:S X'FORM\_IH-160 LAN , SP050006F00

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Document Number	PEW52 M/B LA-6634P Schematic				Rev	0.2
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# For Wireless LAN

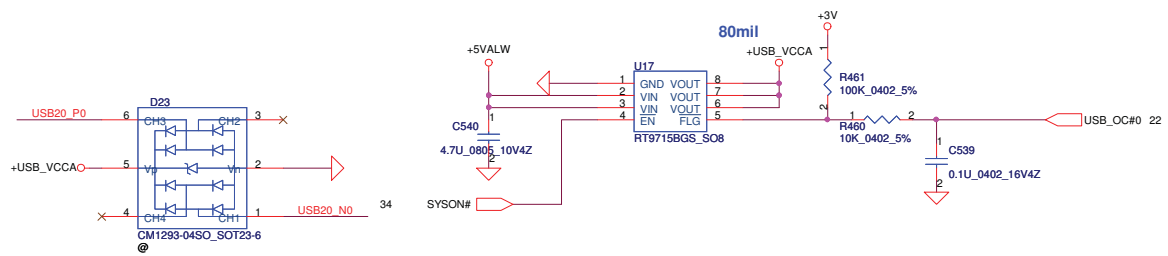


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

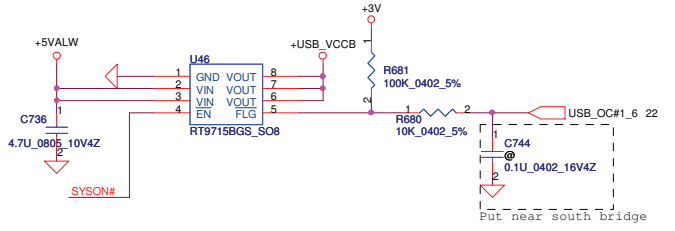


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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				Date:	Friday, August 06, 2010
				Sheet	27 of 44

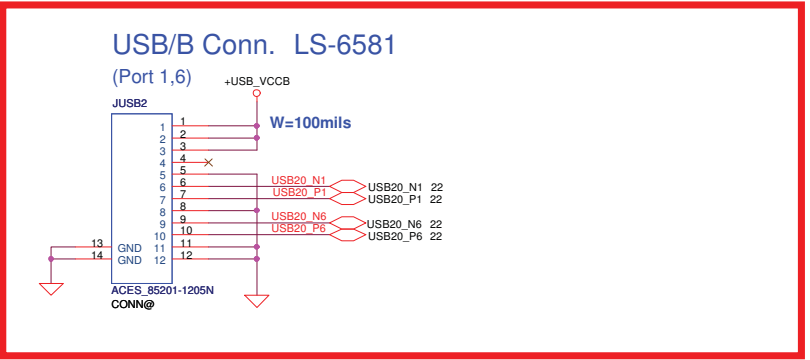
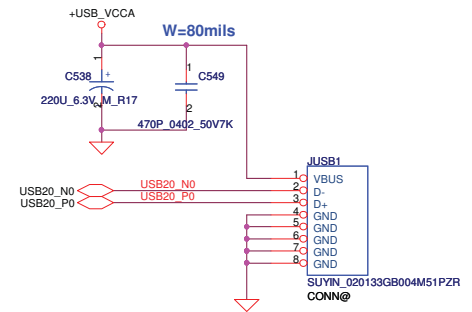
Rev 0.2



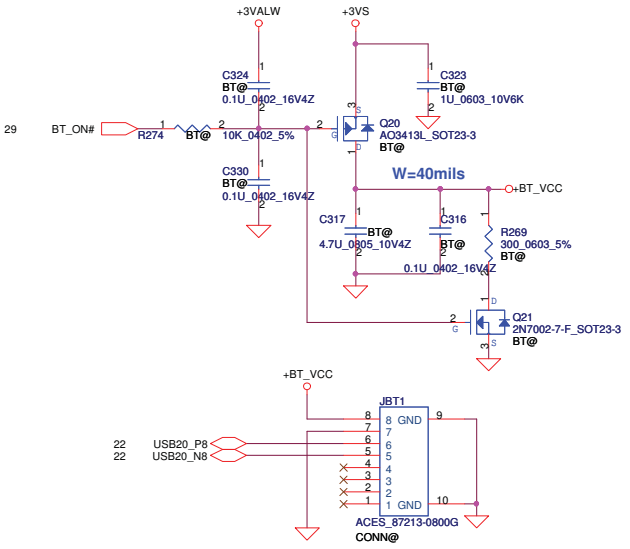
USB Conn.  
(Port 0)



USB/B Conn. LS-6581  
(Port 1,6)

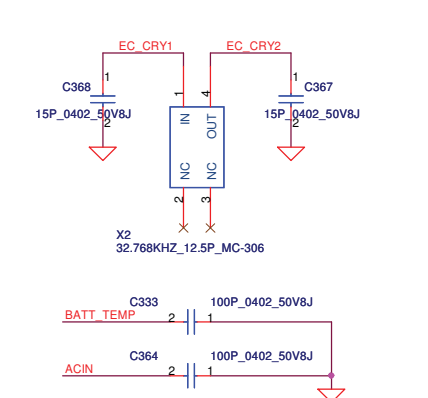
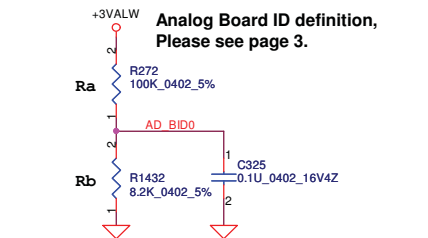
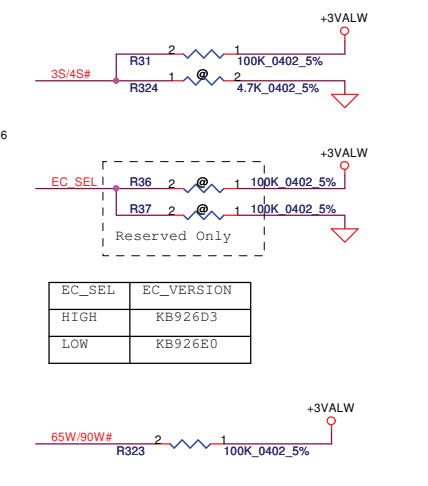
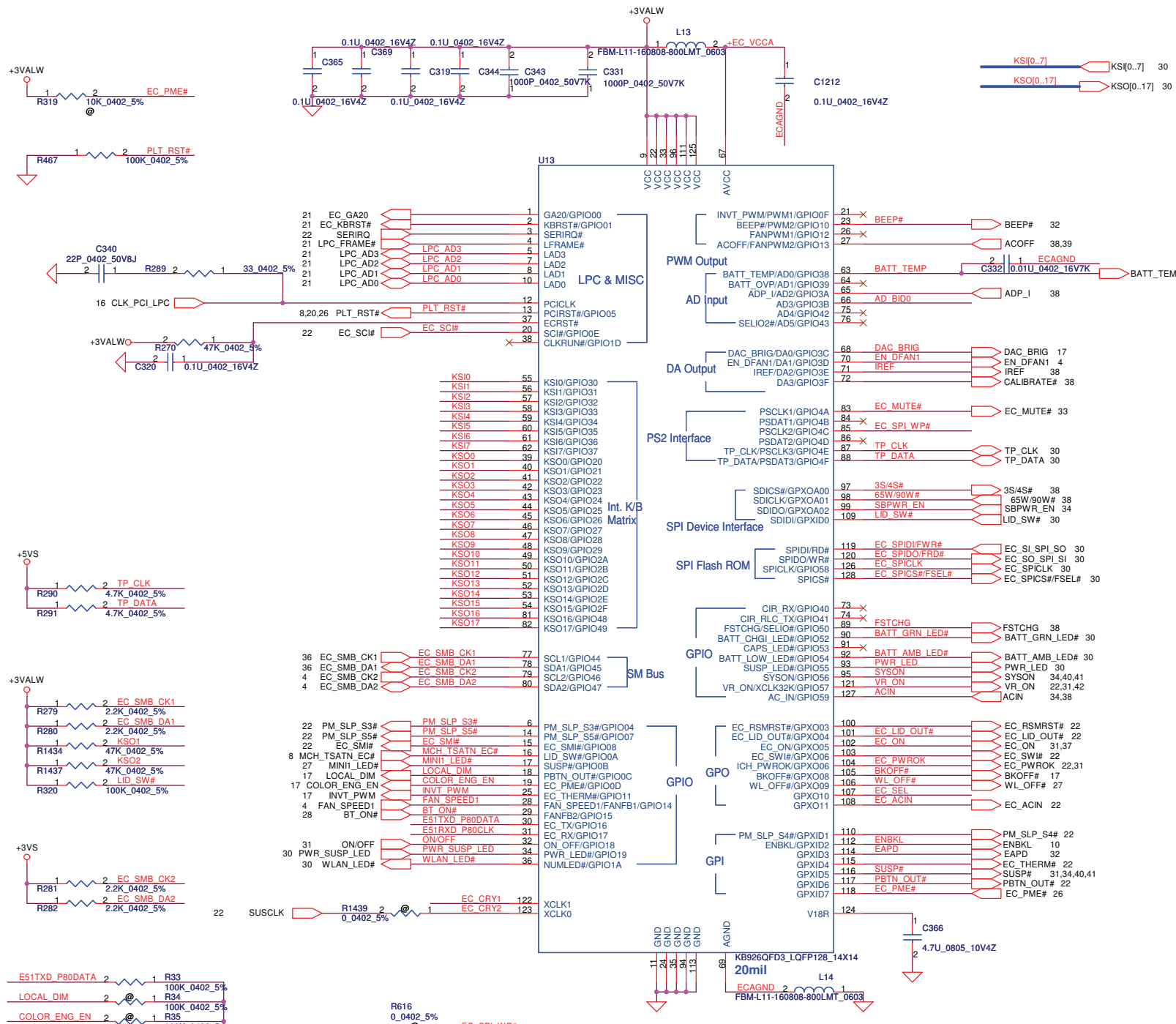
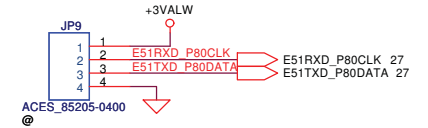


Bluetooth Conn.



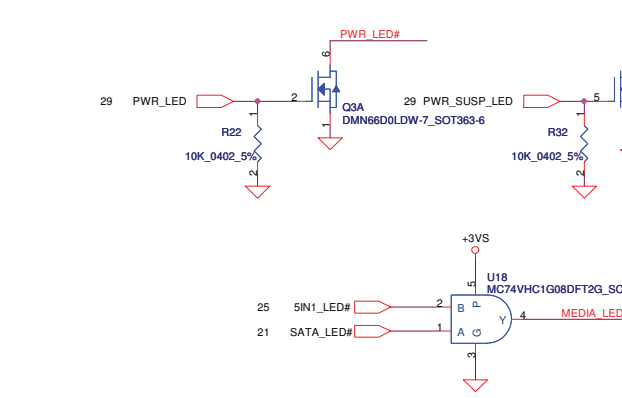
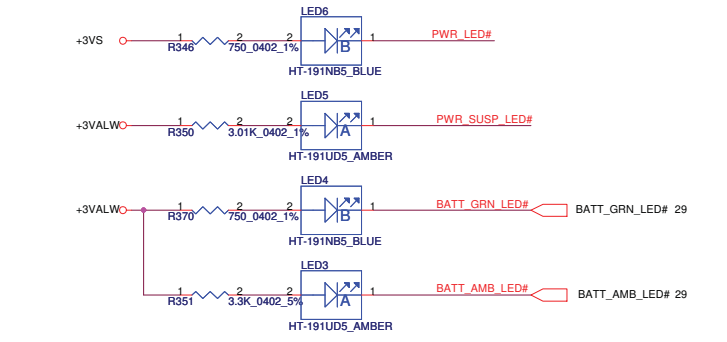
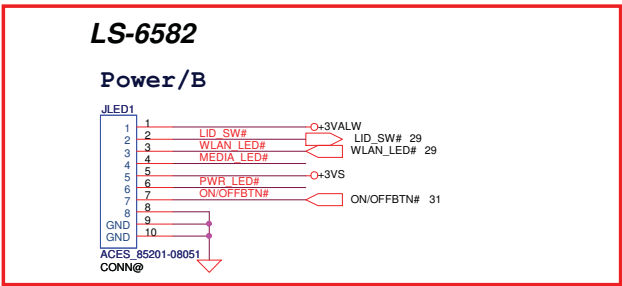
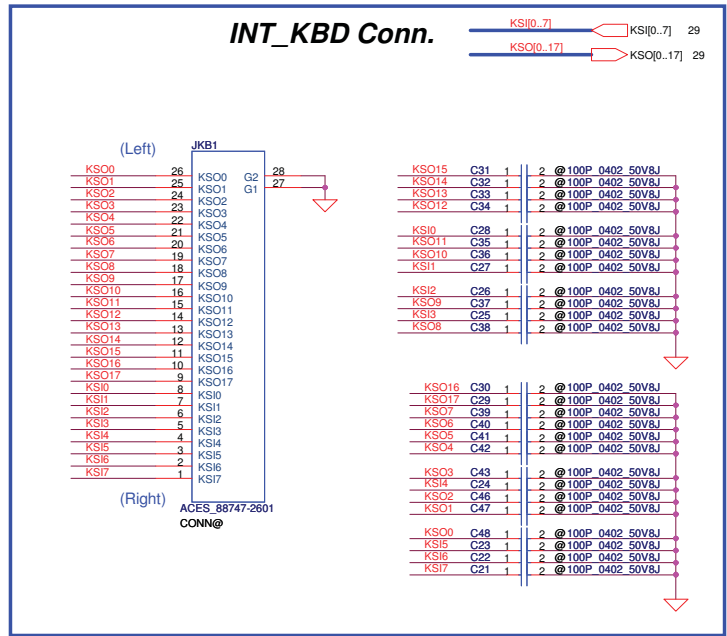
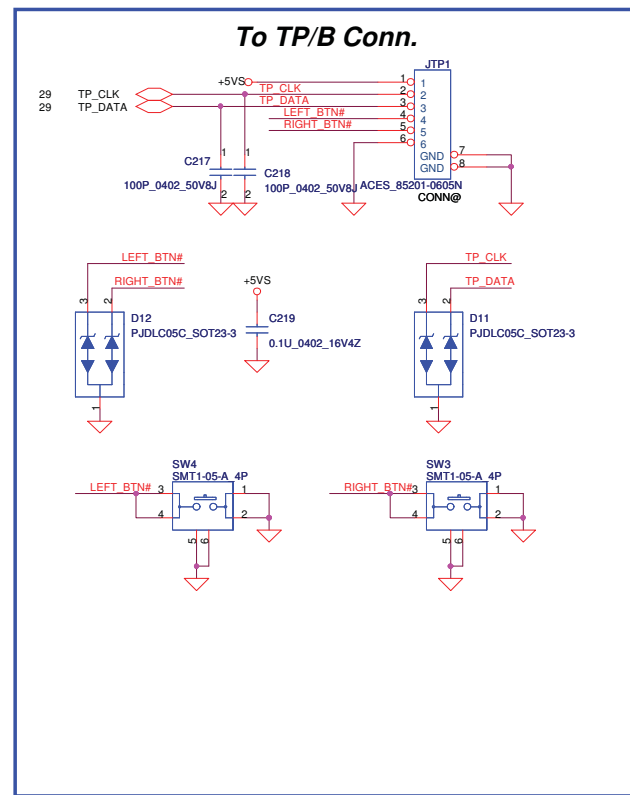
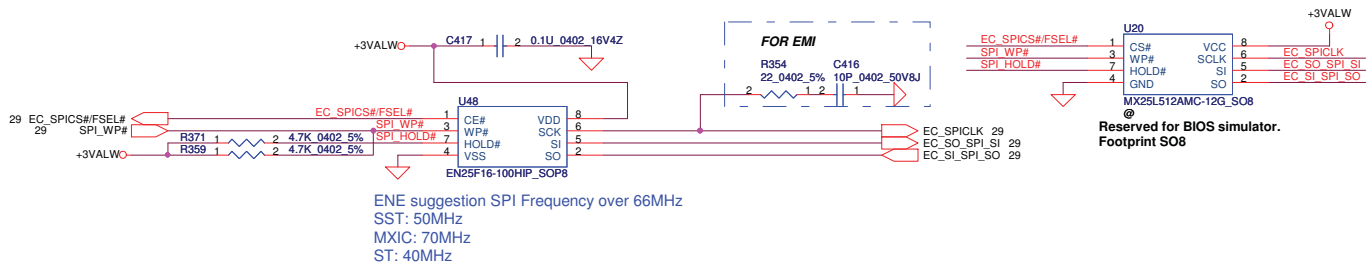
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**For EC Tools**  
Place under MiniCard or DIMM



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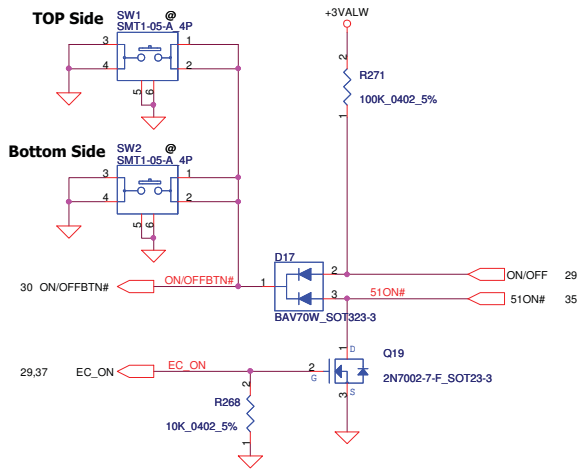




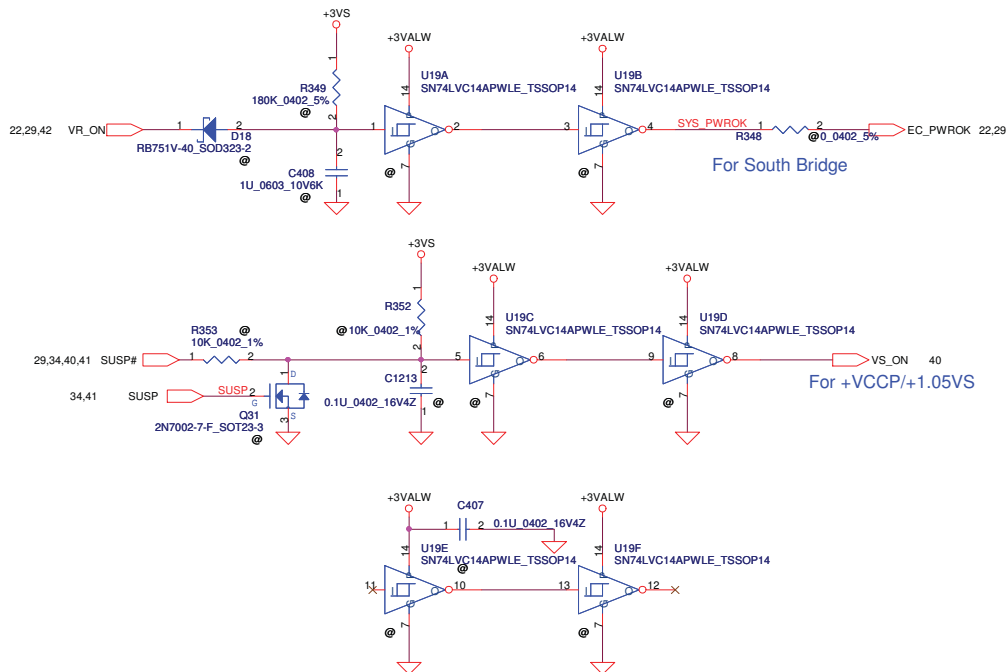
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# Power Button

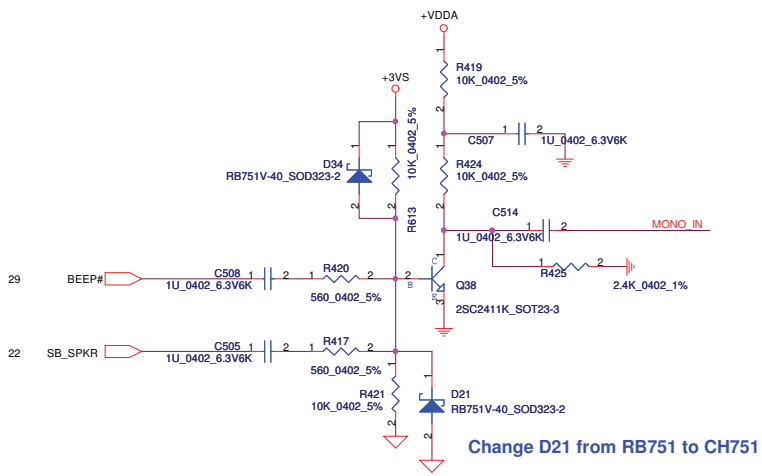
ON/OFF switch



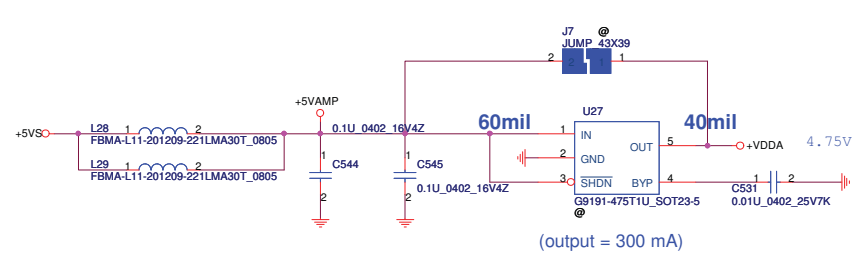
# Power ON Circuit



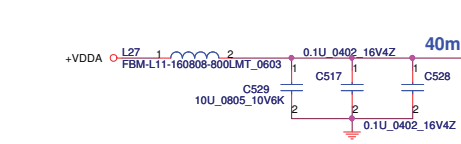
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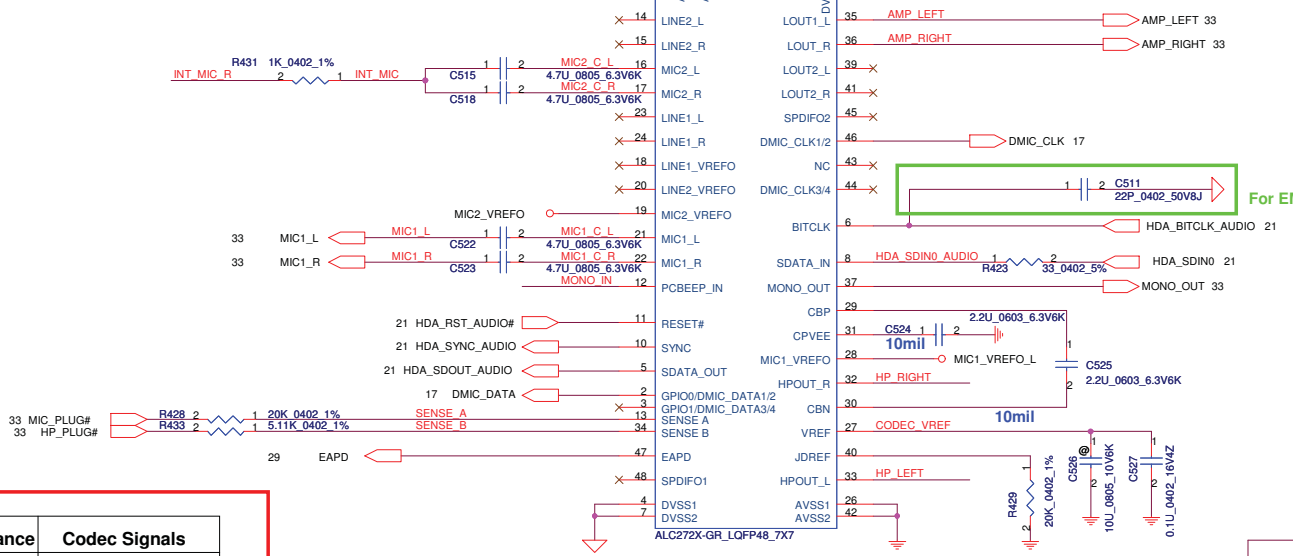
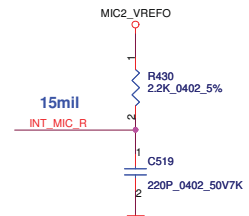
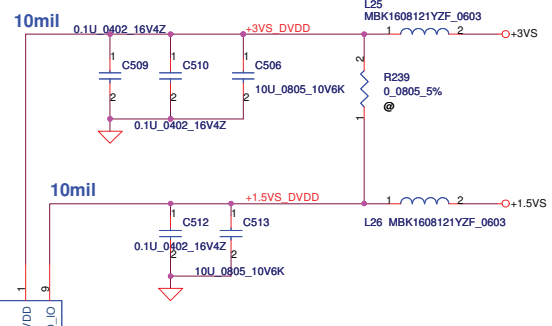
### HD Audio Codec



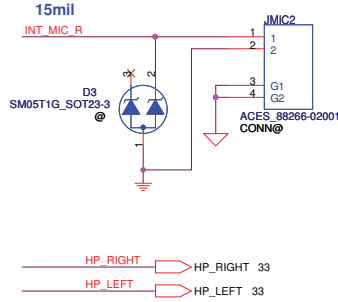
(output = 300 mA)



Change D21 from RB751 to CH751



For EMI

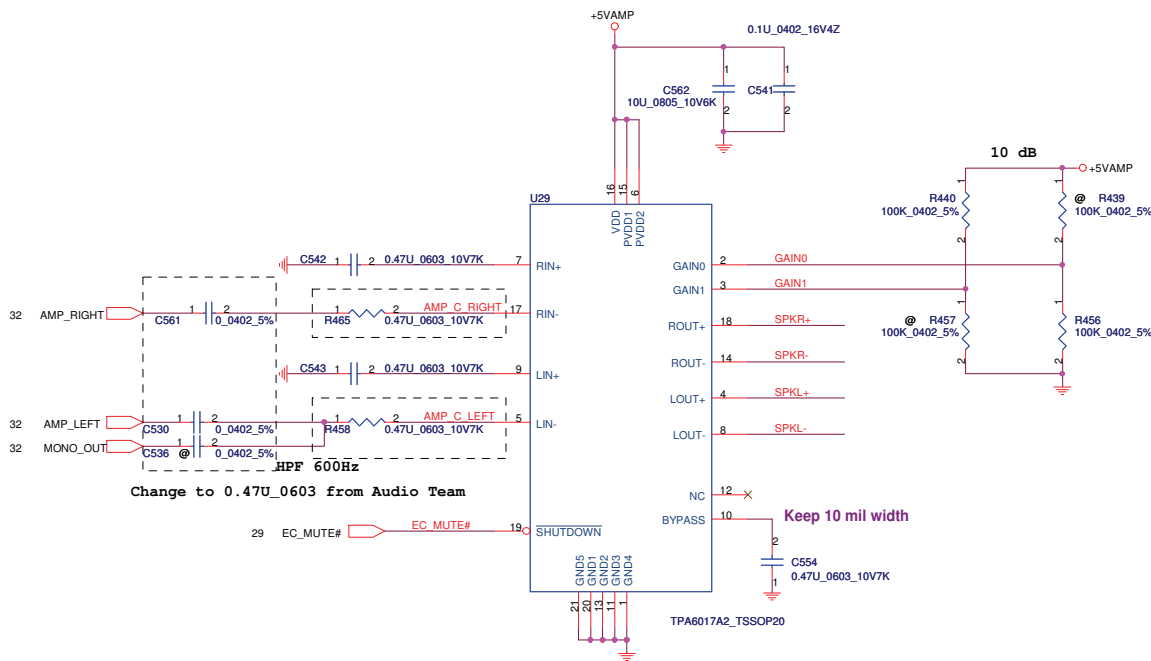


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-B (PIN 21, 22)
	20K	
	10K	
SENSE B	5.1K	PORT-H (PIN 32,33)
	39.2K	
	20K	
	10K	
	5.1K	

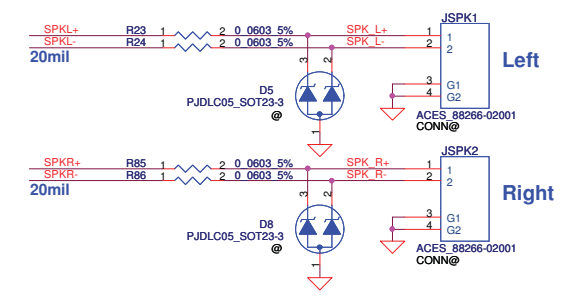
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HD Audio Codec ALC272X

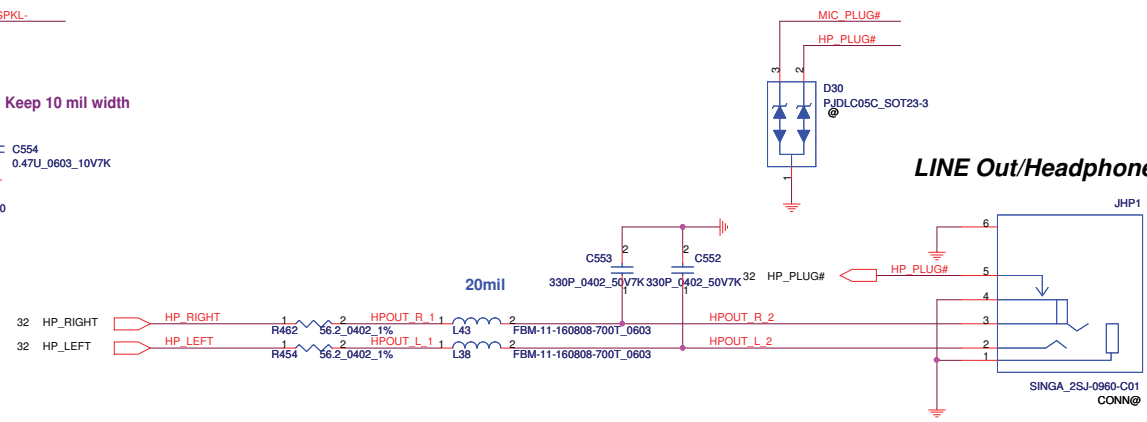
PEW52 M/B LA-6634P Schematic



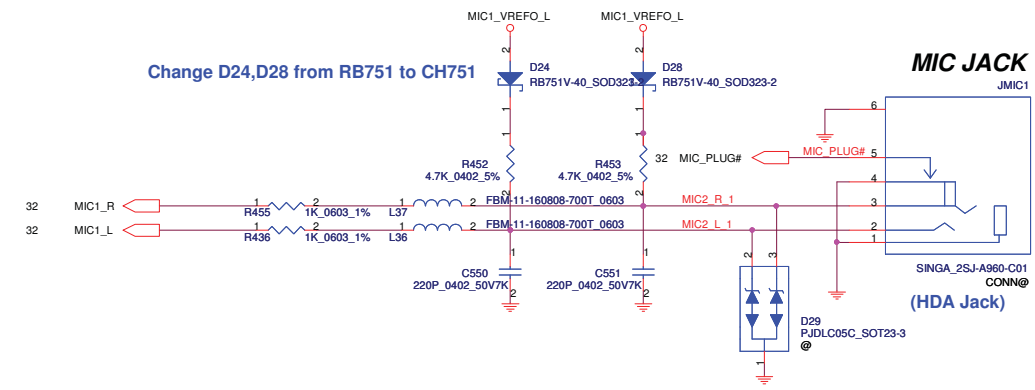
**Int. Speaker Conn.**



**LINE Out/Headphone Out**

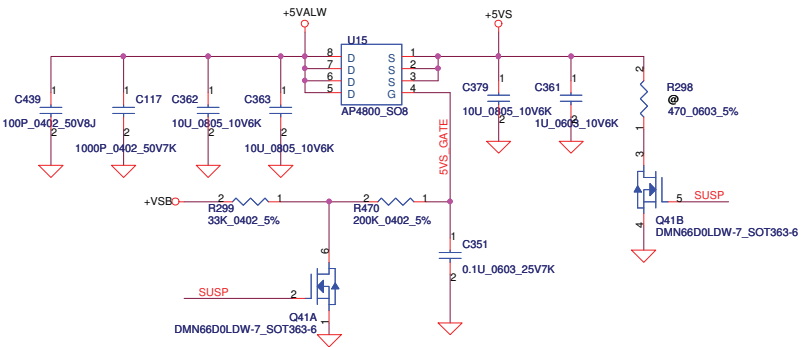


**Change D24,D28 from RB751 to CH751**

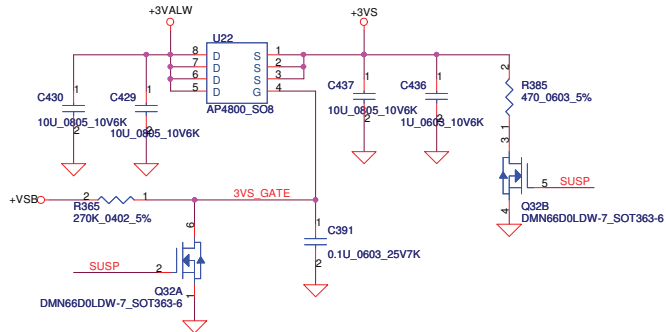


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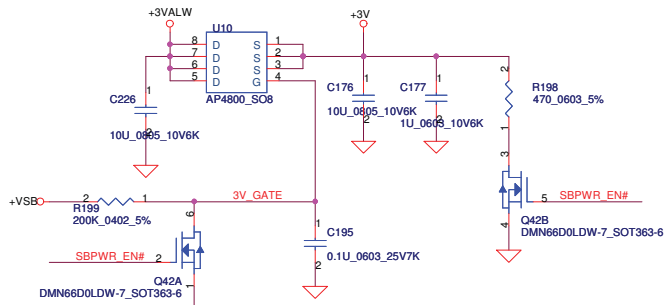
**+5VALW TO +5VS**



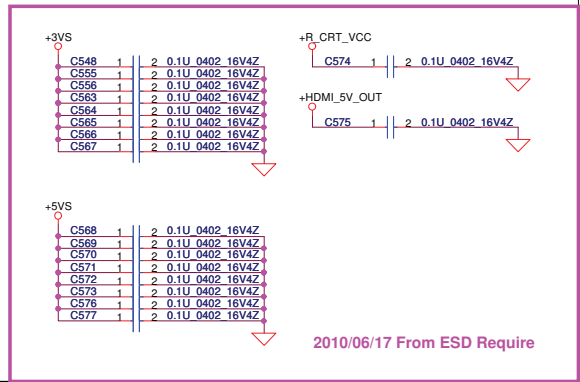
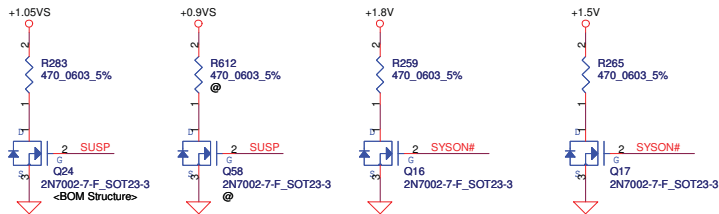
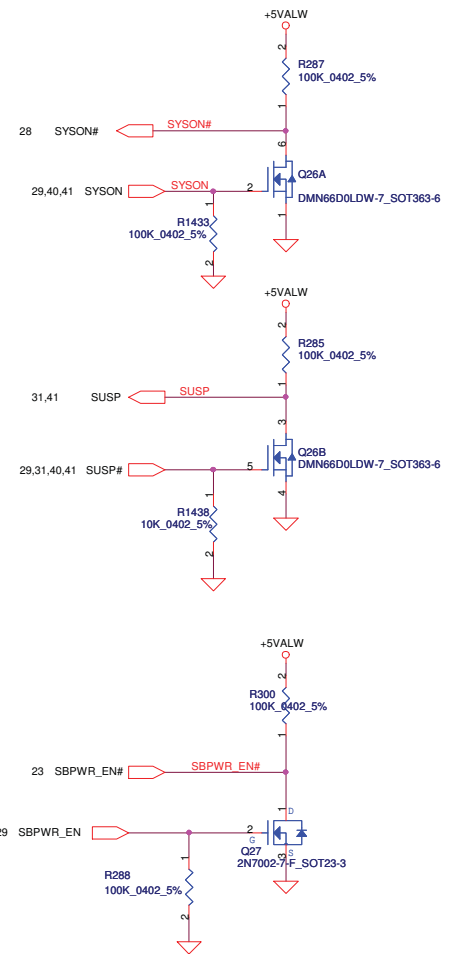
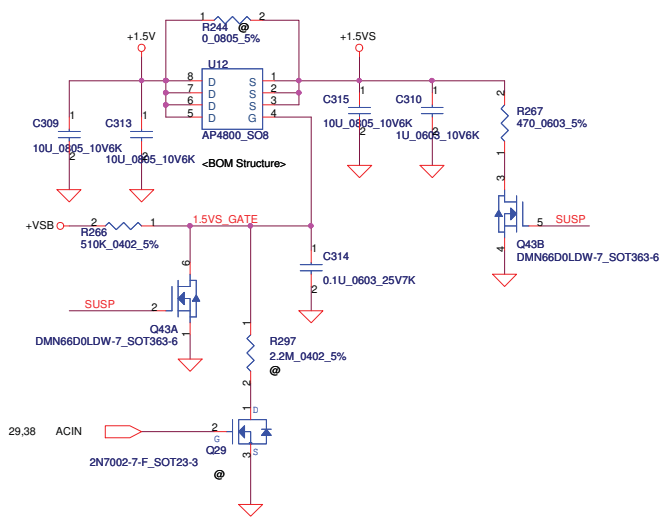
**+3VALW TO +3VS**



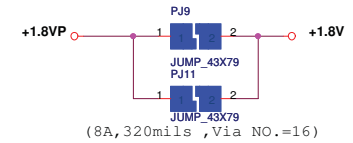
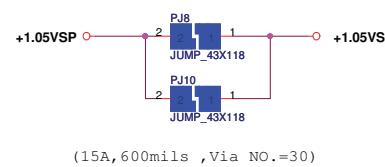
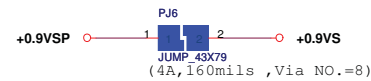
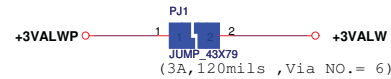
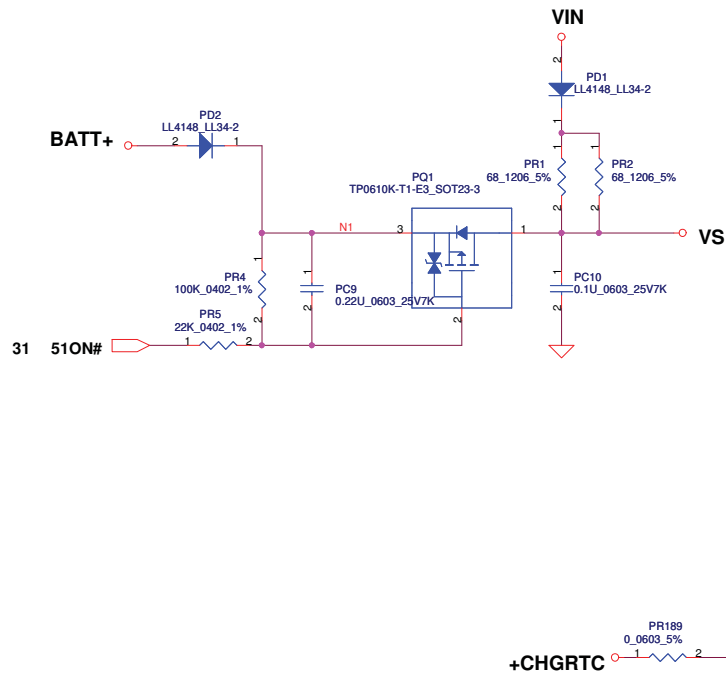
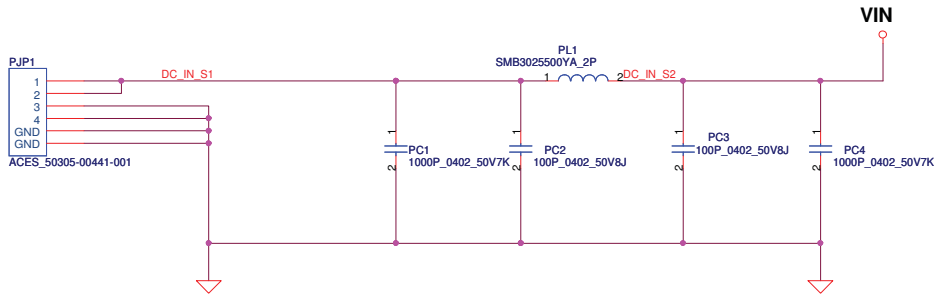
**+3VALW TO +3V\_SB(ICH8M AUX Power)**



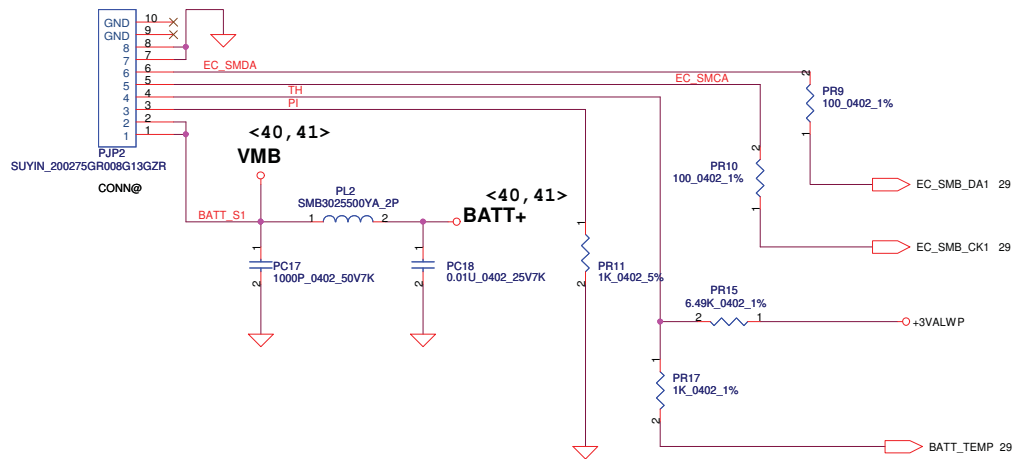
**+1.5V to +1.5VS**



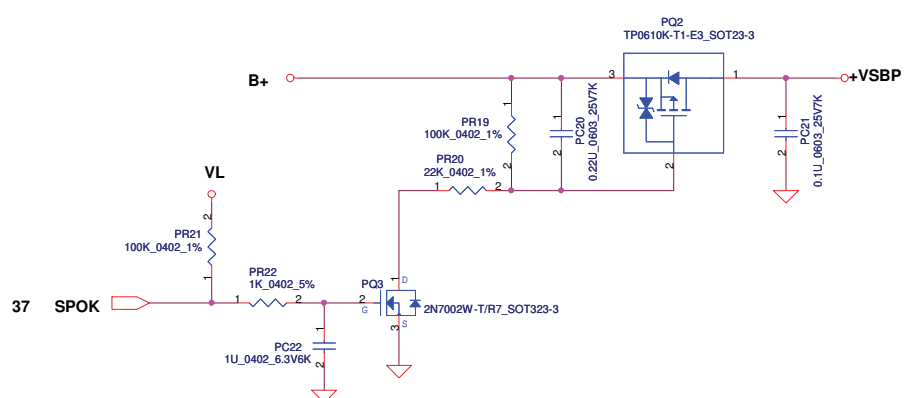
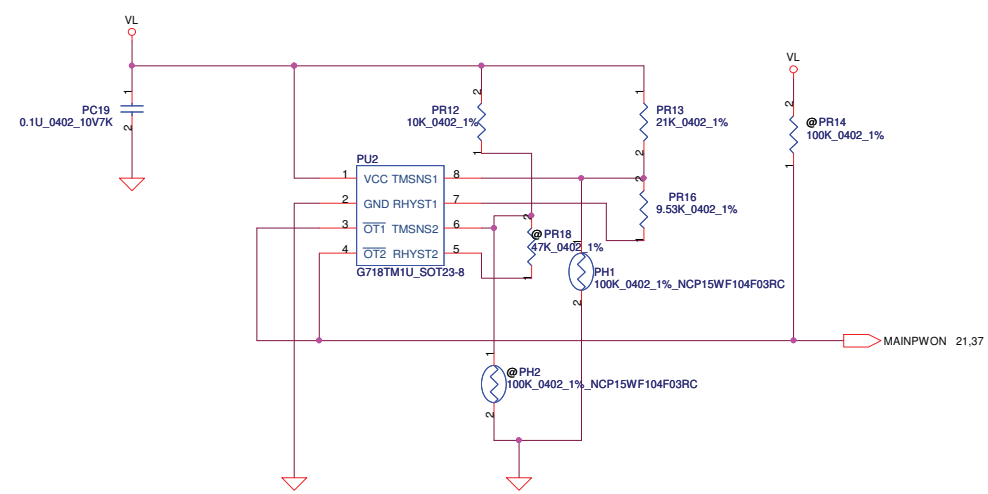
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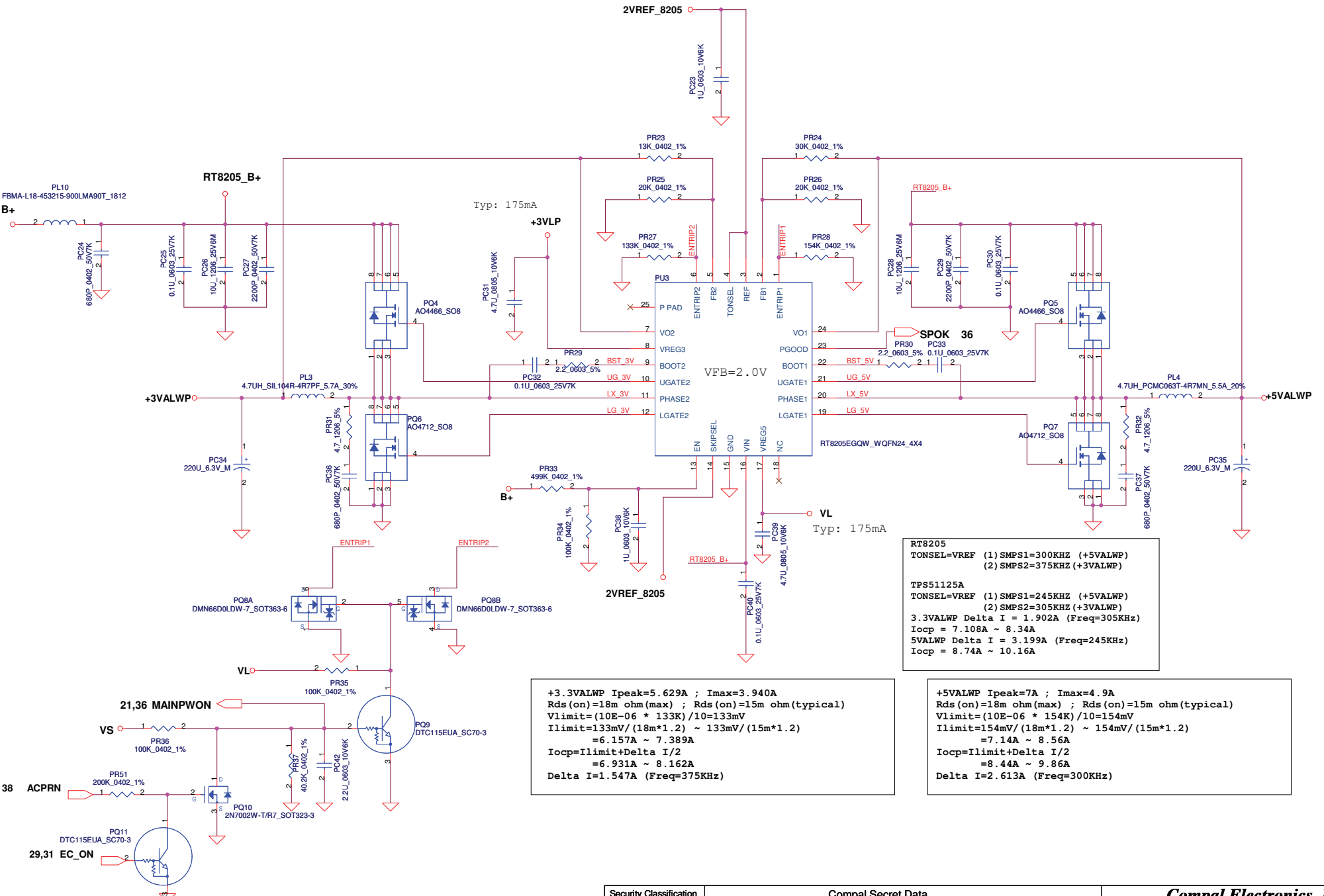
PH1 under CPU bottom side :  
 CPU thermal protection at 92 degree C  
 Recovery at 56 degree C



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Note:  
 Use TPS51125 IC can remove RTC refernece LDO  
 Use TPS51427 IC must keep RTC refernece LDO



**RT8205**  
 TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)  
 (2) SMPS2=375KHZ (+3VALWP)

**TPS51125A**  
 TONSEL=VREF (1) SMPS1=245KHZ (+5VALWP)  
 (2) SMPS2=305KHZ (+3VALWP)  
 3.3VALWP Delta I = 1.902A (Freq=305KHz)  
 Iocp = 7.108A ~ 8.34A  
 5VALWP Delta I = 3.199A (Freq=245KHz)  
 Iocp = 8.74A ~ 10.16A

**+3.3VALWP** Ipeak=5.629A ; Imax=3.940A  
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)  
 Vlimit=(10E-06 \* 133K)/10=133mV  
 Ilimit=133mV/(18m\*1.2) ~ 133mV/(15m\*1.2)  
 =6.157A ~ 7.389A  
 Iocp=Ilimit+Delta I/2  
 =6.931A ~ 8.162A  
 Delta I=1.547A (Freq=375KHz)

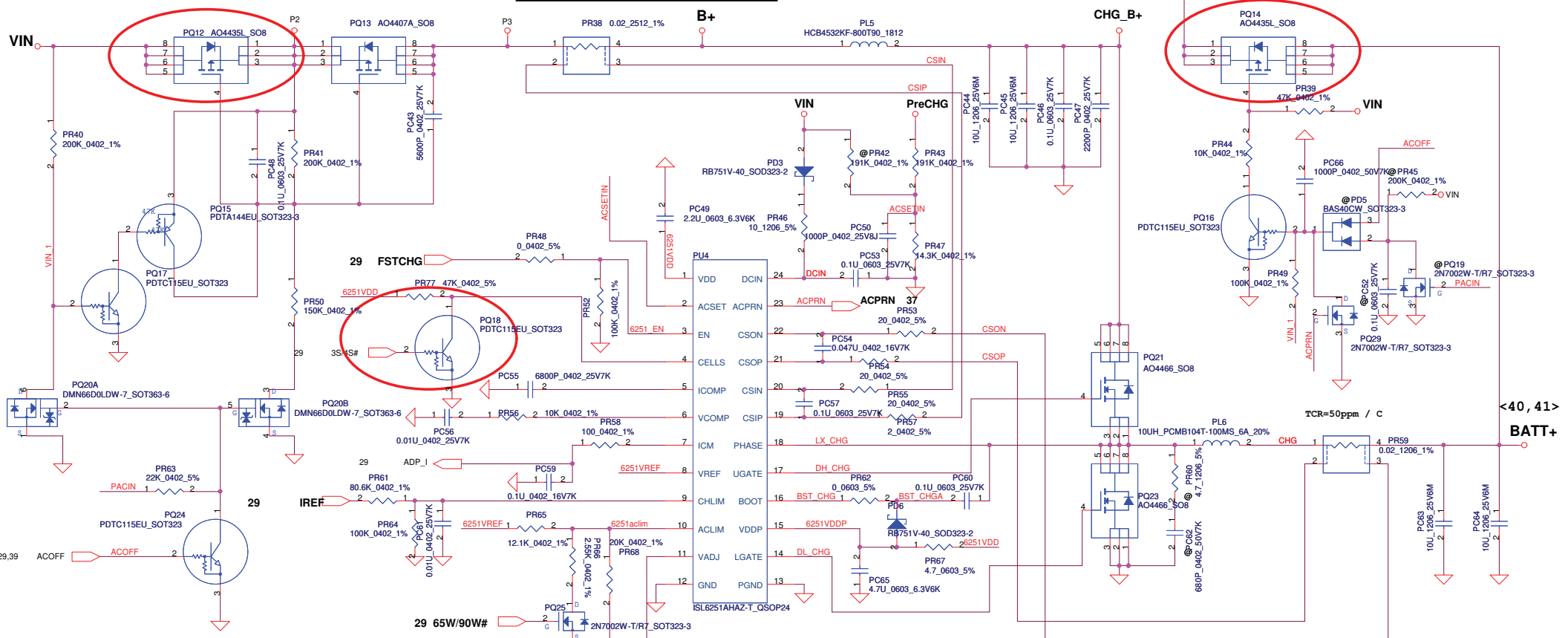
**+5VALWP** Ipeak=7A ; Imax=4.9A  
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)  
 Vlimit=(10E-06 \* 154K)/10=154mV  
 Ilimit=154mV/(18m\*1.2) ~ 154mV/(15m\*1.2)  
 =7.14A ~ 8.56A  
 Iocp=Ilimit+Delta I/2  
 =8.44A ~ 9.86A  
 Delta I=2.613A (Freq=300KHz)

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Iada=0~4.74A (90W/19V=4.736A)  
 Iada=0~3.42A (90W/19V=3.421A)

ADP\_I = 19.9\*Iadapter\*Rsense

CP = 85%\*Iada ; CP = 4.07A  
 CP = 85%\*Iada ; CP = 2.91A



**CP mode**  
 $I_{input} = (1/0.02) (0.05 \cdot V_{ac1m} / 2.39 + 0.05)$   
 where  $V_{ac1m} = 1.502V$ ,  $I_{input} = 4.07A$

**CC=0.6~4.48A**  
 $I_{REF} = 0.7224 \cdot I_{charge}$   
 $K_i = 0.7224$   
 $I_{REF} = 0.43V \sim 3.24V$

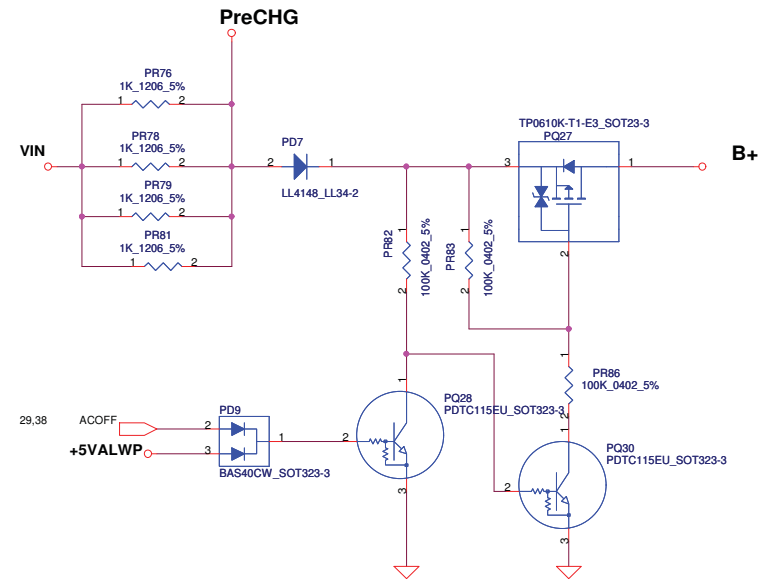
$K_i$   
 $V_{ch1m} = I_{ref} \cdot (PR374 / (PR372 + PR374))$   
 $= I_{ref} \cdot (100K / (80.6K + 100K))$   
 $= I_{ref} \cdot 0.5537$   
 $I_{charge} = (165mV / PR369) \cdot (V_{ch1m} / 3.3V)$   
 $= (165m / 20m) \cdot (1 / 3.3V) \cdot I_{ref} \cdot 0.5537$   
 $= 1.3842 \cdot I_{ref}$   
 $I_{ref} = 0.7224 \cdot I_{charge} \Rightarrow K_i = 0.7224$

$K_v$   
 $R_{internal} = 514K$   $R_{ec} = 3K$   $R_1 = PR379 = 15.4K$   $R_2 = PR381 = 31.6K$   
 $R = 514K // 31.6K // (15.4K + 3K) = 11.372K$   
 $r = 514K // 514K // 31.6K = 28.14K$   
 $V_{ce11} = 0.175 \cdot V_{adj} + 3.99V$   
 $4.2V = 0.175 \cdot V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$   
 $V_{adj} = V_{ref} \cdot (R / (R + 514K)) + CALIBRATE \cdot (r / (r + 514K))$   
 $1.1483 = CALIBRATE \cdot 0.6046 \Rightarrow CALIBRATE = 1.899$   
 $1.899 = (4.2 - (V_{ce11} + 0.175)) \cdot R_v = (4.2 - (4.2 + 0.175)) \cdot R_v$   
 $A = V_{ref} \cdot (R / (R + 514K)) = 0.052$   
 $R_v = 9.451$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

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<b>CHARGER</b>			
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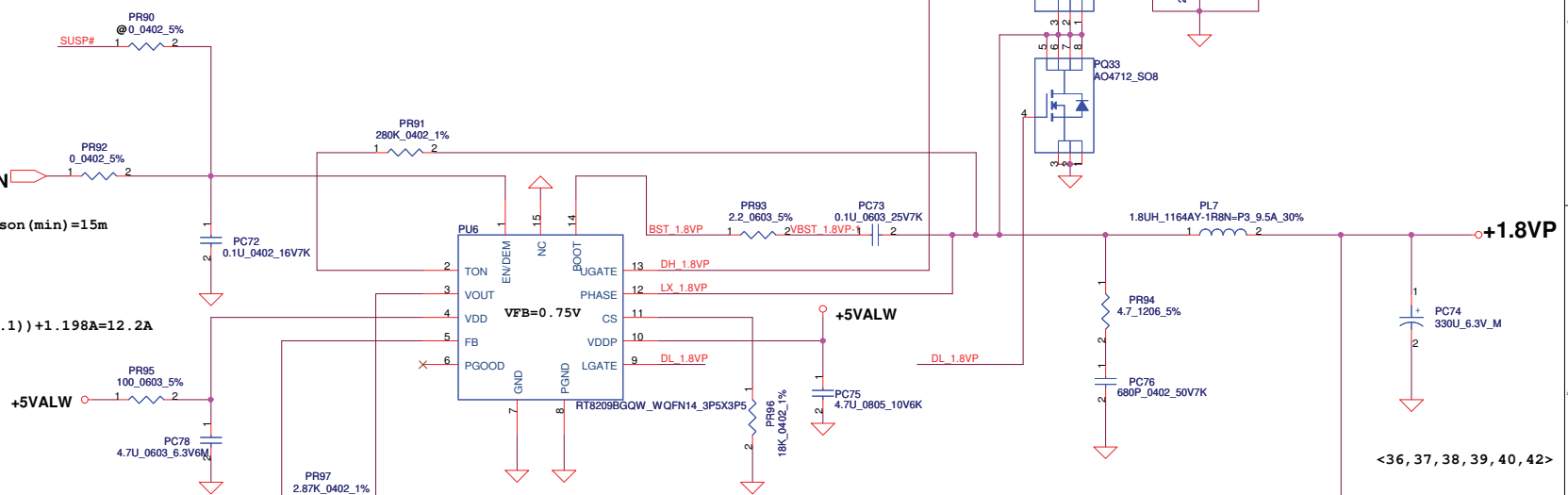


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VFB=0.75V  
 $V_o = VFB * (1 + PR97/PR98) = 0.75 * (1 + 5.9K/5.76K) = 1.8V$   
 $Fsw = 282KHz$

<Vo=1.8V>  
 $Fsw = 262KHz$  Cout ESR=15m ohm Rds(on)(max)=18m Rds(on)(min)=15m  
 $I_{peak} = 11.3A$ ,  $I_{2peak} = 13.56A$ ,  $I_{max} = 7.91A$   
 $\Delta I = ((19-1.5) * (1.5/19)) / (L * Fsw) = 2.3969A$   
 $\Rightarrow 1/2 \Delta I = 1.198A$   
 $V_{trip} = R_{trip} * I_{0uA} = 18K * 10uA = 0.18V$   
 $I_{ocpmin} = V_{trip} / R_{ds(on)(max)} * 1.2 + 1.198 = 12.2A$   
 $I_{ocpmax} = (0.18 / (0.015 * 1.1)) + 1.198A = 12.2A$   
 $I_{ocp} = 9 \sim 12.2A$

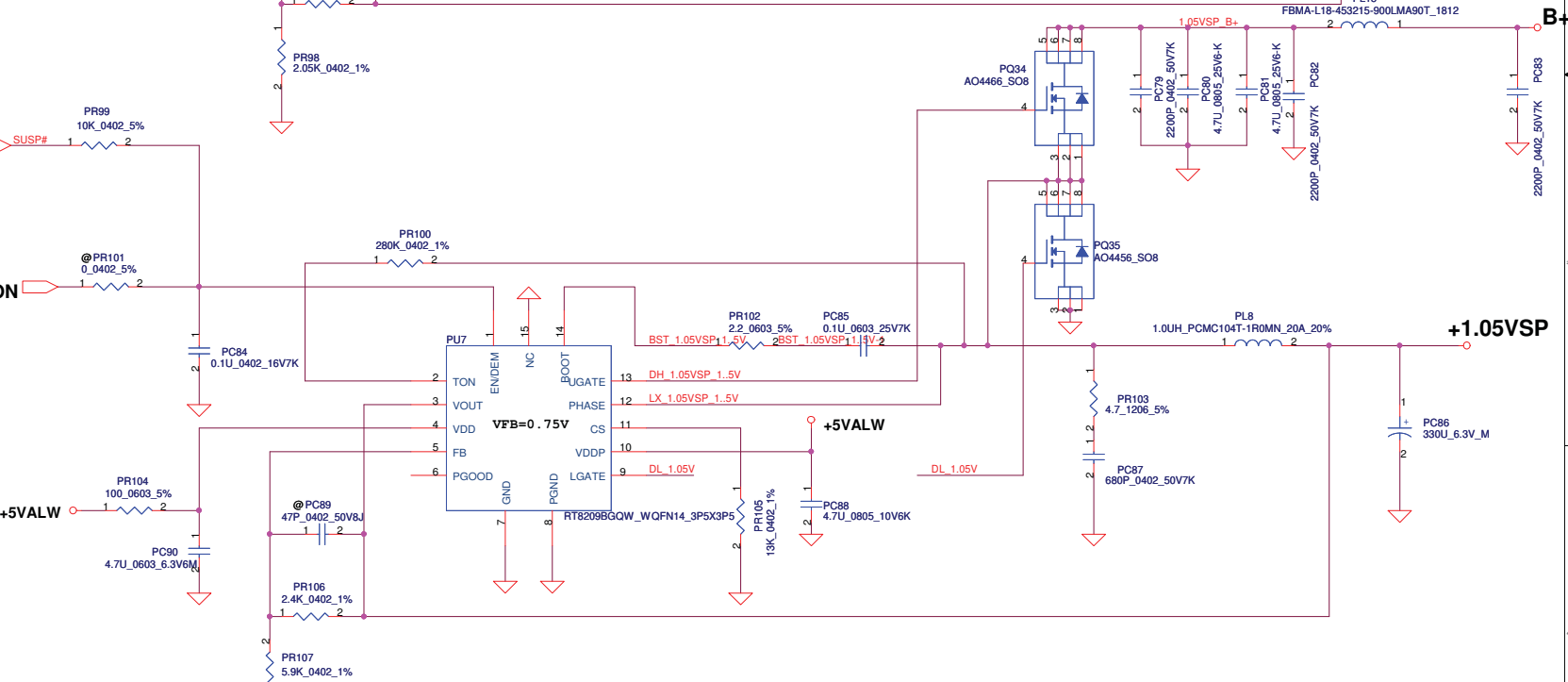
29,34,41 SYSON



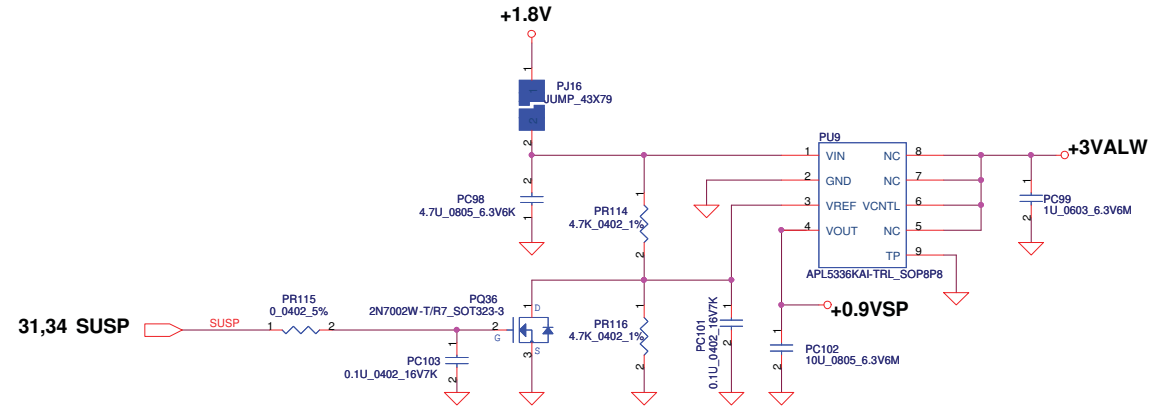
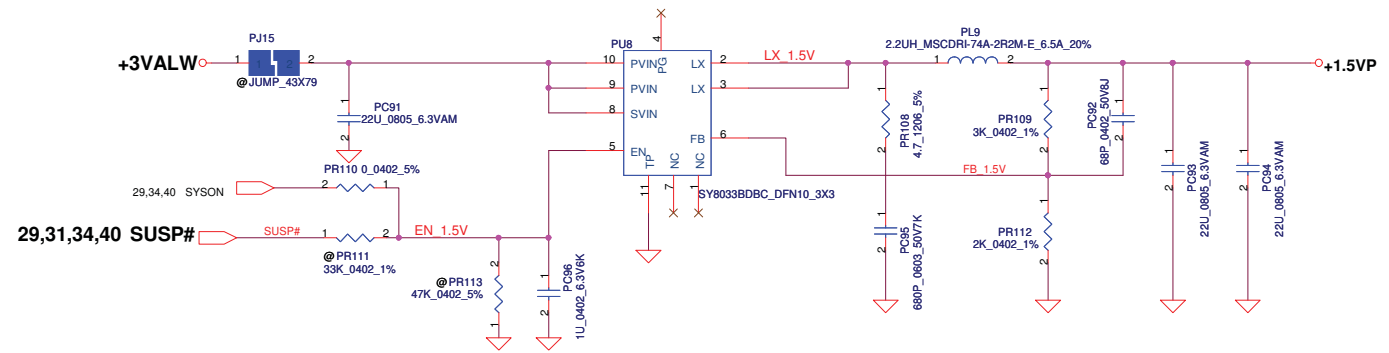
VFB=0.75V  
 $V_o = VFB * (1 + PR108/PR109) = 0.75 * (1 + 12K/30K) = 1.05V$   
 $Ton = 19 * e^{-12 * 143000} * ((2/3) * V_o + 100mV) / 19 + 50ns = 2.645e-7 us$   
 $\Rightarrow V_o / V_{in} = D = Ton / T_s \Rightarrow T_s = 3.35us$   
 $Fsw = 261KHz$  (by calculation tool)

<Vo=1.05V> VFB=0.75V  
 $V_o = VFB * (1 + PR108/PR109) = 0.75 * (1 + 12K/30K) = 1.05V$   
 $Fsw = 261KHz$  Cout ESR=15m ohm Rds(on)(max.)=5.6m  
 $R_{ds(on)(min)} = 4.5m$   
 $I_{peak} = 14.9A$ ,  $I_{max} = I_{peak} * 0.7 = 10.43A$   $I_{ocp} = 17.88A$   
 $\Delta I = ((19-1.05) * (1.05/19)) / (L * Fsw) = 2.11A$   
 $\Rightarrow 1/2 \Delta I = 1.055A$   
 $V_{trip} = R_{trip} * I_{0uA} = 13K * 10uA = 0.13V$   
 $I_{ocpmin} = V_{trip} / R_{ds(on)(max)} * 1.3 + 1.055 = 18.95A$   
 $I_{ocpmax} = (0.13 / (0.0045 * 1.1)) + 1.055A = 27.36A$   
 $I_{ocp} = 18.95A \sim 27.36A$

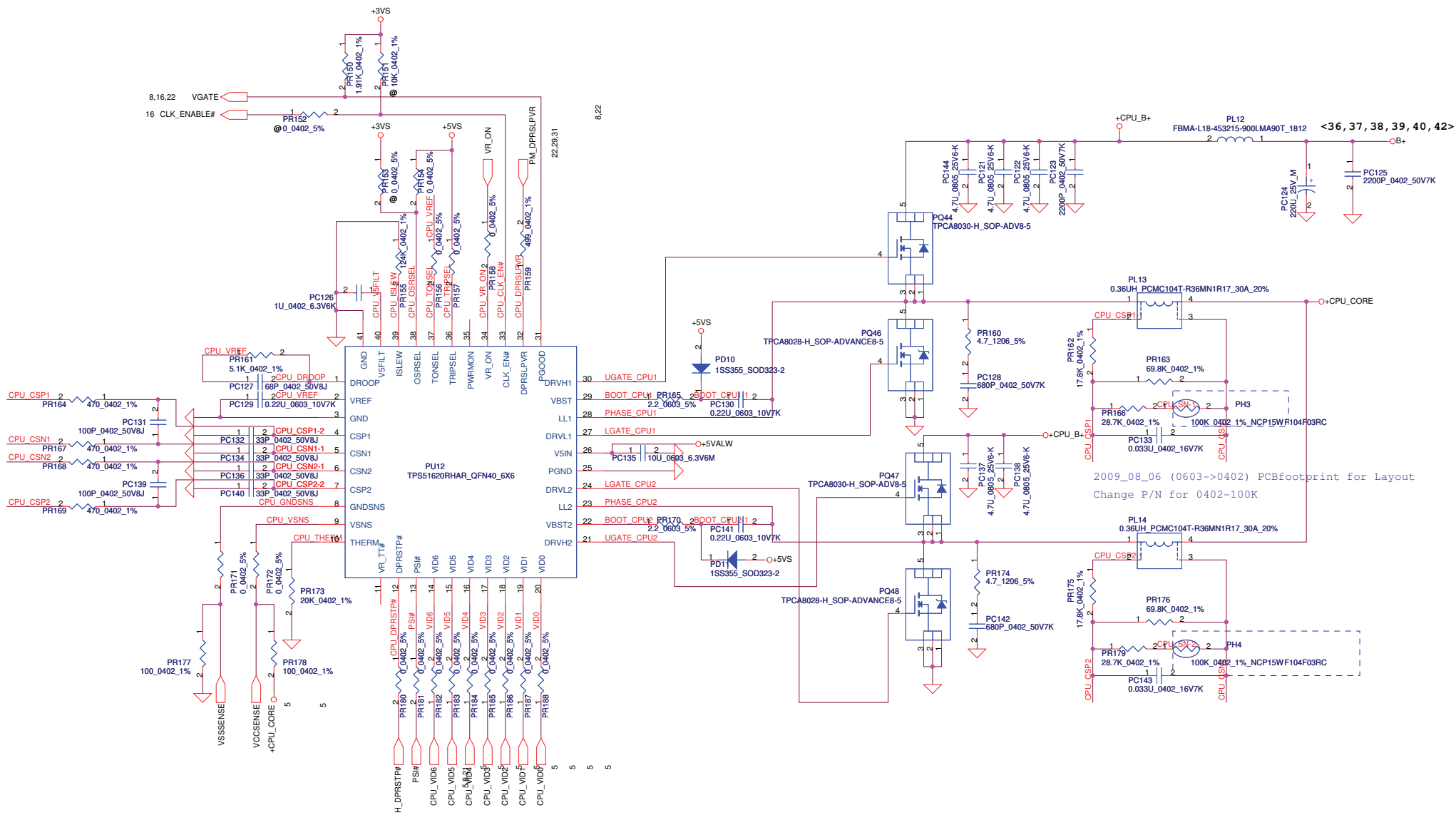
31 VS\_ON



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**Version change list (P.I.R. List)**

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	add 3S/4S pin function	add 4 cell battery	0.2	45	add PQ18 PDTC115EU_SOT323 (SB301150200) and PR77 47K +-5% 0402 (SD028470280)	2010/06/11	EVT
2	ACSETIN net	ACSETIN net no connect	0.2	45		2010/06/11	EVT
3	1.5V enable	1.5V enable BOM error	0.2	45	add PR92 and delete PR90 0_0402_5% (SD028000080)	2010/06/11	EVT
4	EMI issue	add boost R and snubber	0.2	45	add 3/5V 1..05V/1.5V CPU sunbber		
5							
6							
7							
8							
9							
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11							
12							
13							
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17							

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				Size	Document Number
				Custom	PEW72/82 M/B LA-6631P Schematic
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# A --> C Change List

20100806 Update Revision to 0.2

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Date:	Friday, August 06, 2010	Sheet	44	of	44
				Rev	0.2