

Compal Confidential

KALG1 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2009-03-02

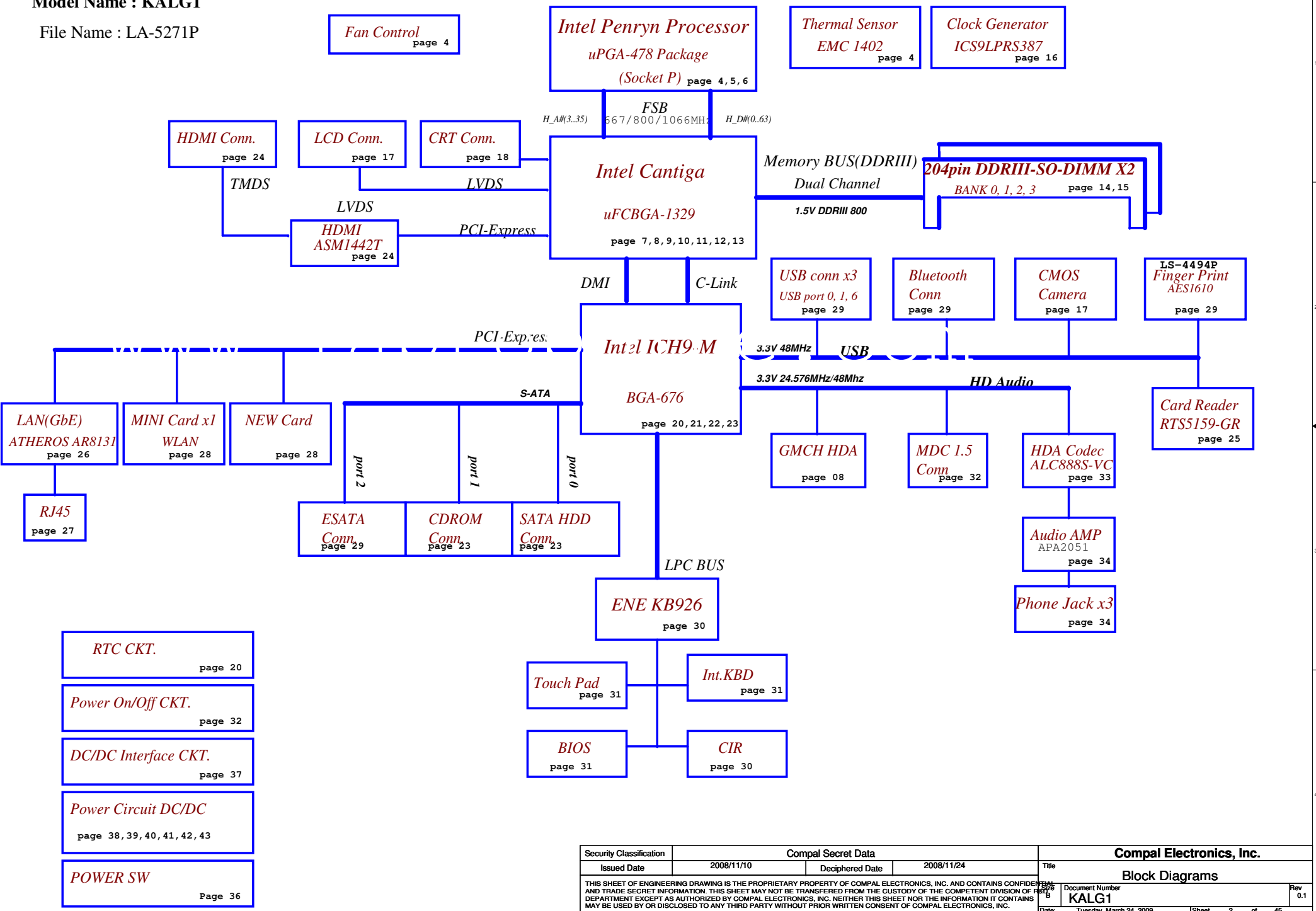
REV 02

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Compal Confidential

Model Name : KALG1

File Name : LA-5271P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75VS power rail for DDR3 terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for NB(LVDS)	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3V	3.3V power rail for SB	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail for SB	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 100X b

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS367, SLG8SP556V)	1101 001Xb
DDR3 DIMMA	1001 000Xb
DDR3 DIMMB	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1				
2				
3				
4				
5				
6				
7				

BOARD ID Table

Board ID	PCB Revision
0	PCB 08Y LA-5271P REV0 M/B
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

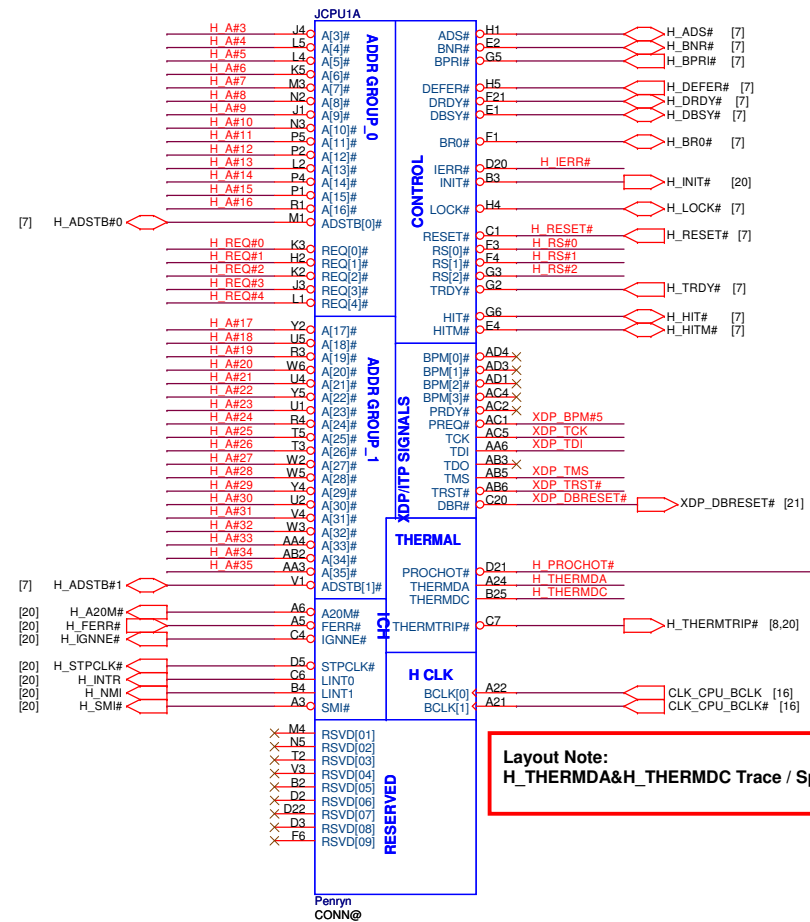
BTO Item	BOM Structure
GL40	GL40@
GM45	GM45@

BOM Configuration Table

Project	BOM Configuration
KALG1-GM45	GM45@/KALG1@/KAL90_G0_90+@
KALG1-GL40	GL40@/KALG1@/KAL90_G0_90+@

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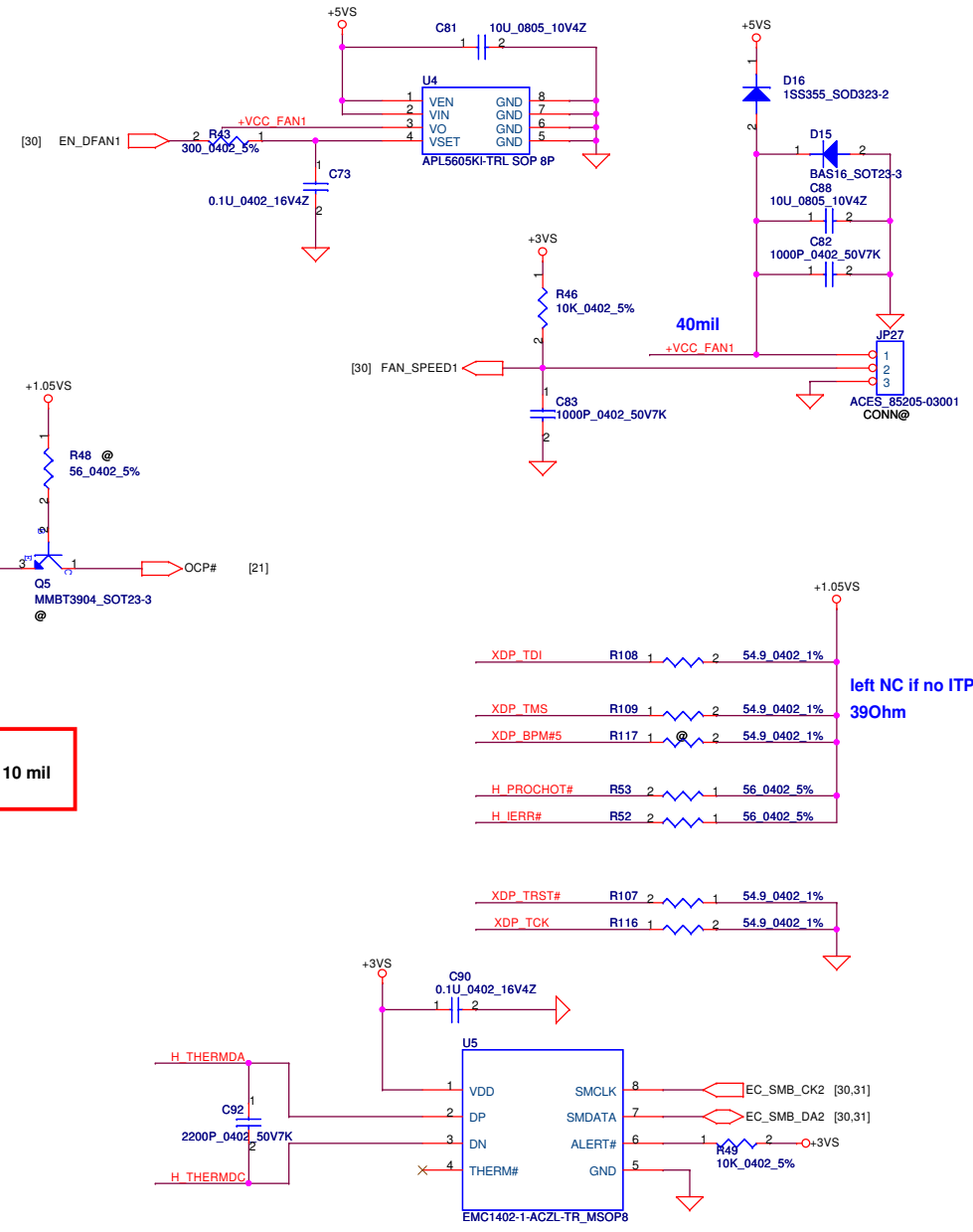
- [7] H_A#[3..35]
- [7] H_REQ#[0..4]
- [7] H_RS#[0..2]

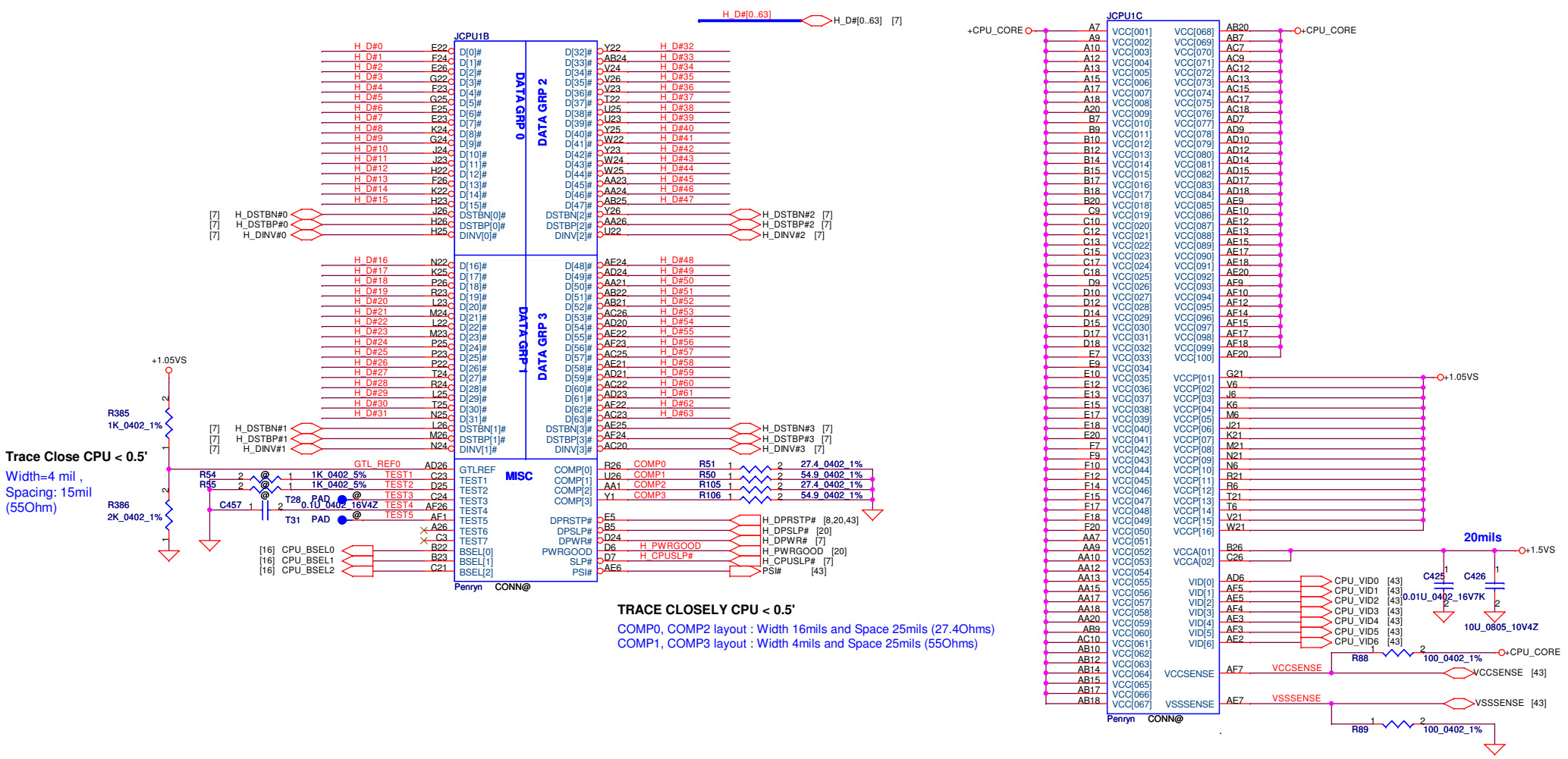


Layout Note:
H_THERMDA&H_THERMDC Trace / Space = 10 / 10 mil

BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166

FAN1 Conn





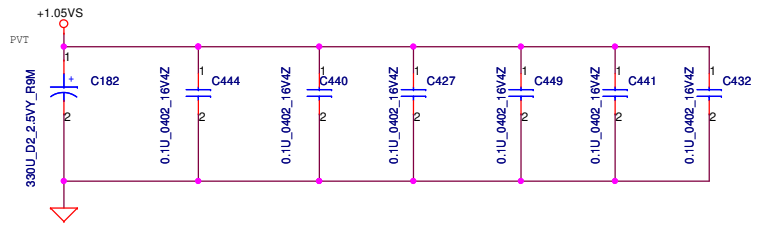
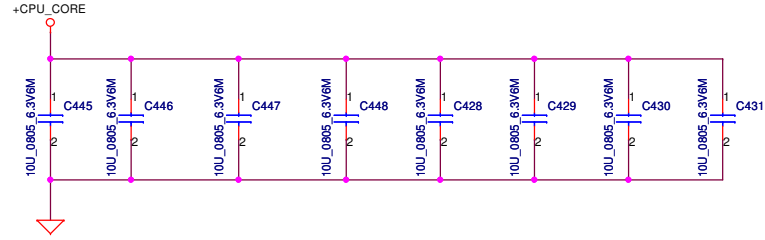
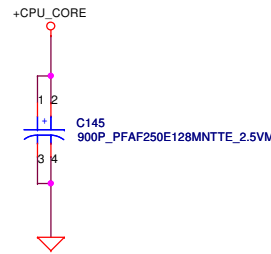
Trace Close CPU < 0.5"
 Width=4 mil,
 Spacing: 15mil
 (55Ohm)

TRACE CLOSELY CPU < 0.5"
 COMP0, COMP2 layout : Width 16mils and Space 25mils (27.4Ohms)
 COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

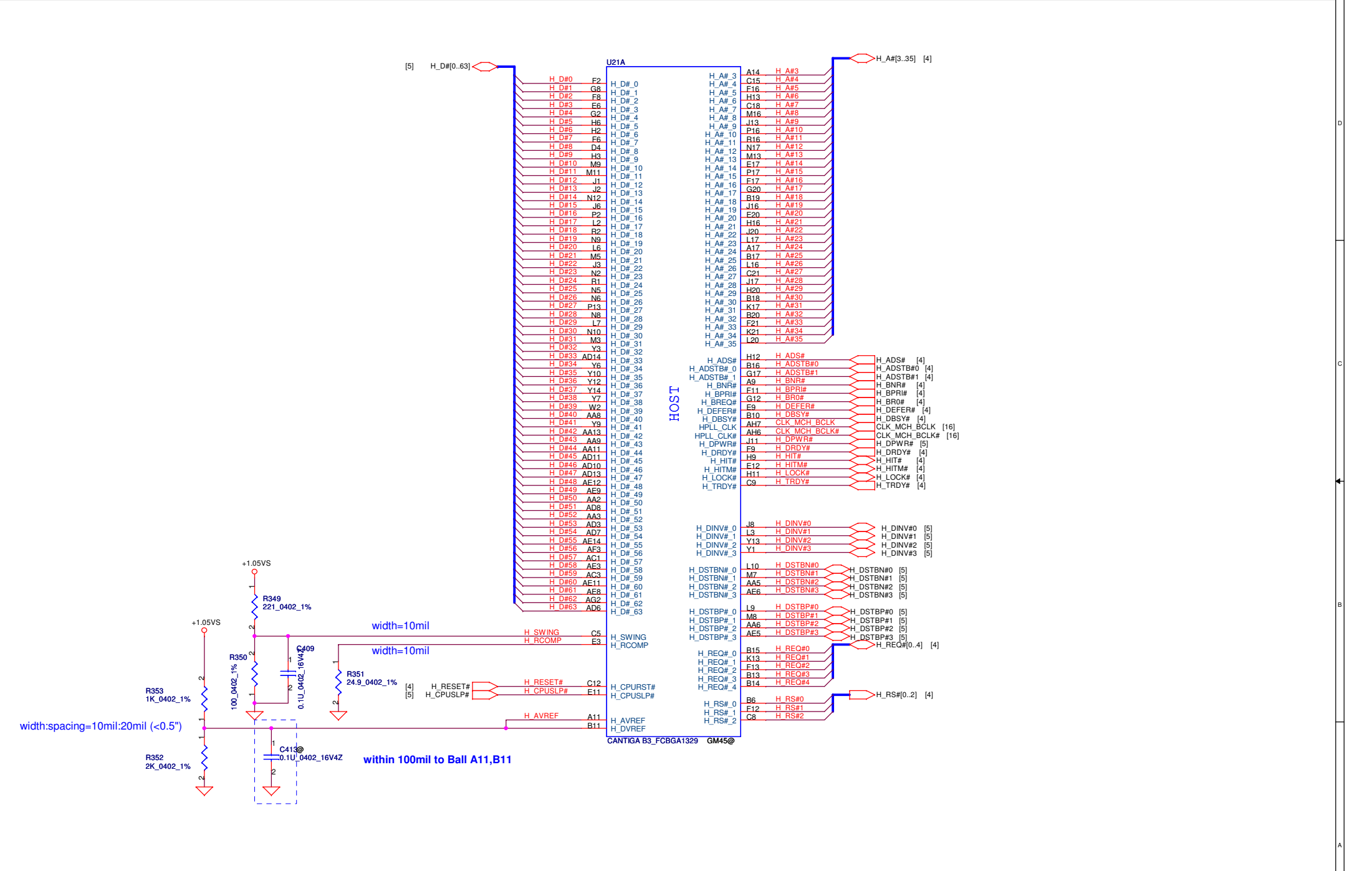
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JCPUID		
A4	VSSJ001	VSSJ082
A8	VSSJ002	VSSJ083
A11	VSSJ003	VSSJ084
A14	VSSJ004	VSSJ085
A16	VSSJ005	VSSJ086
A19	VSSJ006	VSSJ087
A23	VSSJ007	VSSJ088
AF2	VSSJ008	VSSJ089
B6	VSSJ009	VSSJ090
B8	VSSJ010	VSSJ091
B11	VSSJ011	VSSJ092
B13	VSSJ012	VSSJ093
B16	VSSJ013	VSSJ094
B19	VSSJ014	VSSJ095
B21	VSSJ015	VSSJ096
B24	VSSJ016	VSSJ097
C5	VSSJ017	VSSJ098
C8	VSSJ018	VSSJ099
C11	VSSJ019	VSSJ100
C14	VSSJ020	VSSJ101
C16	VSSJ021	VSSJ102
C19	VSSJ022	VSSJ103
C2	VSSJ023	VSSJ104
C22	VSSJ024	VSSJ105
C25	VSSJ025	VSSJ106
D1	VSSJ026	VSSJ107
D4	VSSJ027	VSSJ108
D8	VSSJ028	VSSJ109
D11	VSSJ029	VSSJ110
D13	VSSJ030	VSSJ111
D16	VSSJ031	VSSJ112
D19	VSSJ032	VSSJ113
D23	VSSJ033	VSSJ114
D26	VSSJ034	VSSJ115
E3	VSSJ035	VSSJ116
E6	VSSJ036	VSSJ117
E8	VSSJ037	VSSJ118
E11	VSSJ038	VSSJ119
E14	VSSJ039	VSSJ120
E16	VSSJ040	VSSJ121
E19	VSSJ041	VSSJ122
E21	VSSJ042	VSSJ123
E24	VSSJ043	VSSJ124
F5	VSSJ044	VSSJ125
F8	VSSJ045	VSSJ126
F11	VSSJ046	VSSJ127
F13	VSSJ047	VSSJ128
F16	VSSJ048	VSSJ129
F19	VSSJ049	VSSJ130
F2	VSSJ050	VSSJ131
F22	VSSJ051	VSSJ132
F25	VSSJ052	VSSJ133
G4	VSSJ053	VSSJ134
G1	VSSJ054	VSSJ135
G23	VSSJ055	VSSJ136
G26	VSSJ056	VSSJ137
H3	VSSJ057	VSSJ138
H6	VSSJ058	VSSJ139
H21	VSSJ059	VSSJ140
H24	VSSJ060	VSSJ141
J2	VSSJ061	VSSJ142
J5	VSSJ062	VSSJ143
J22	VSSJ063	VSSJ144
J25	VSSJ064	VSSJ145
K1	VSSJ065	VSSJ146
K4	VSSJ066	VSSJ147
K23	VSSJ067	VSSJ148
K26	VSSJ068	VSSJ149
L3	VSSJ069	VSSJ150
L6	VSSJ070	VSSJ151
L21	VSSJ071	VSSJ152
L24	VSSJ072	VSSJ153
M2	VSSJ073	VSSJ154
M5	VSSJ074	VSSJ155
M22	VSSJ075	VSSJ156
M25	VSSJ076	VSSJ157
N1	VSSJ077	VSSJ158
N4	VSSJ078	VSSJ159
N23	VSSJ079	VSSJ160
N26	VSSJ080	VSSJ161
P3	VSSJ081	VSSJ162
		VSSJ163

Penryn CONN@

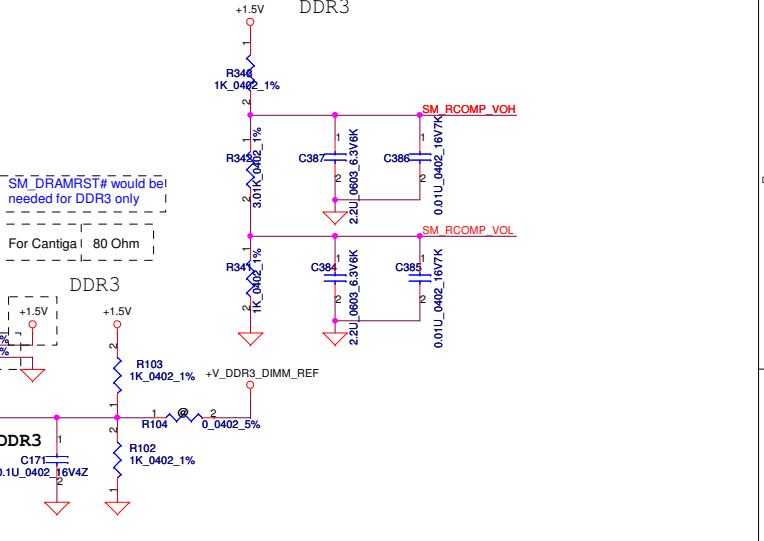
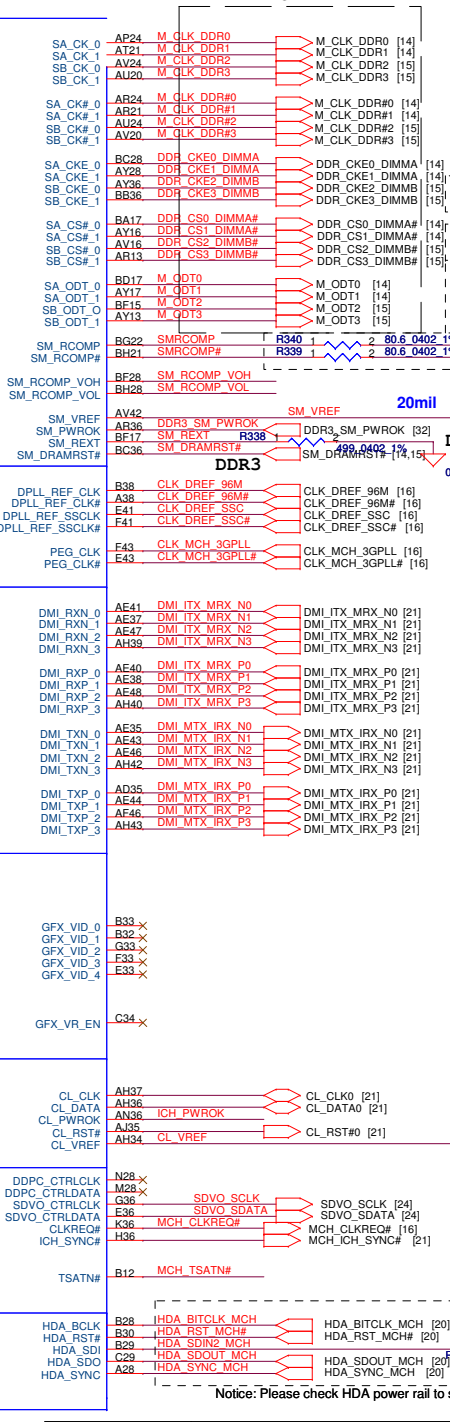
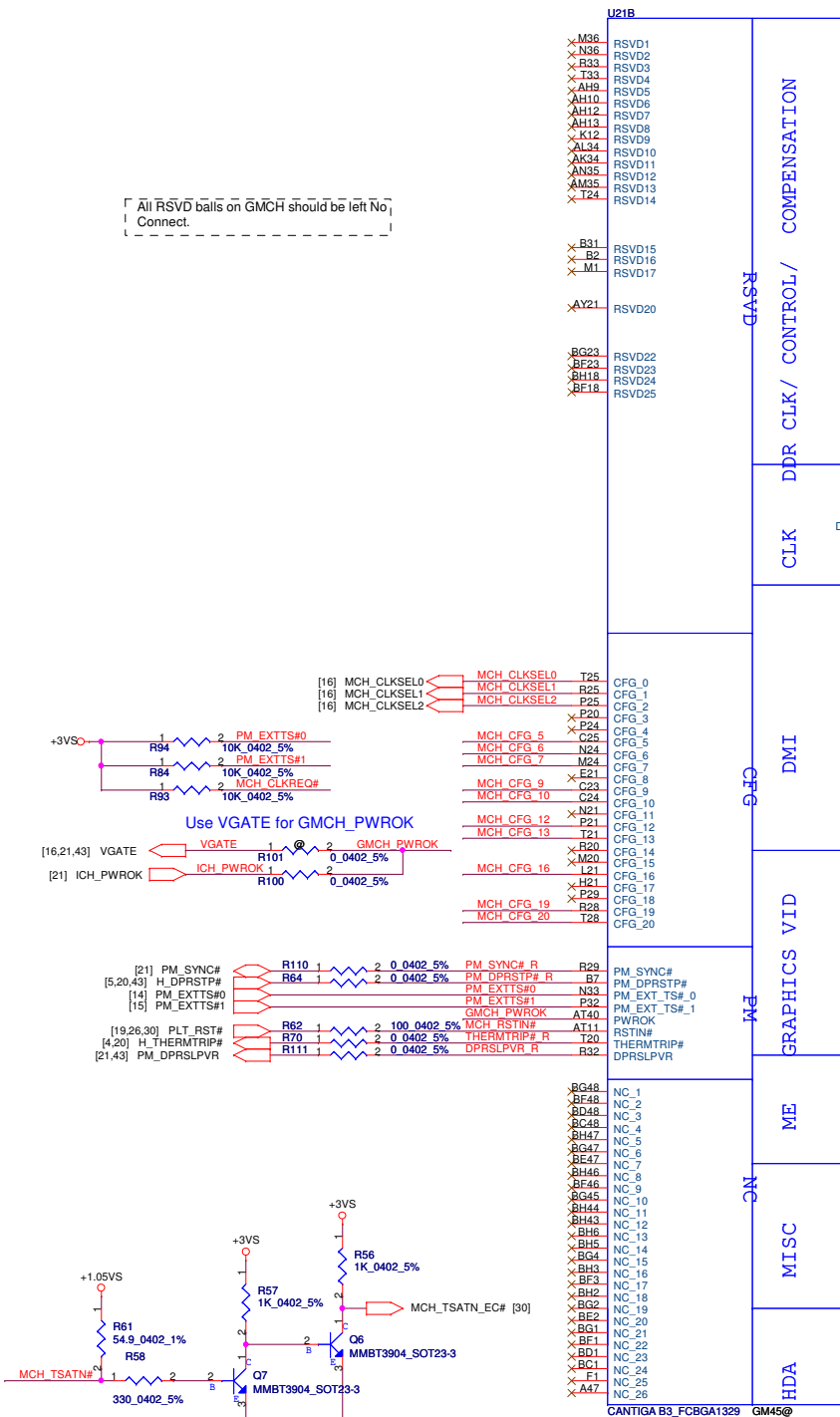


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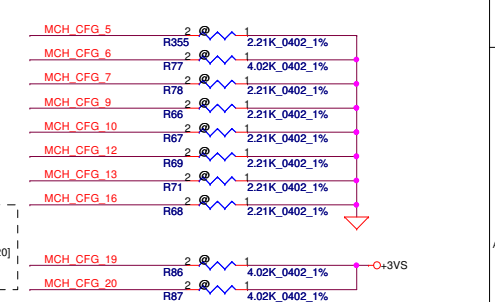
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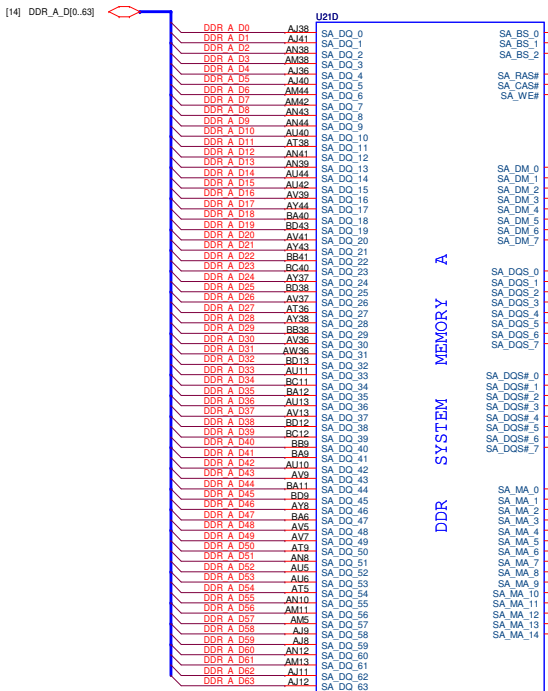
All RSVD balls on GMCH should be left No Connect.



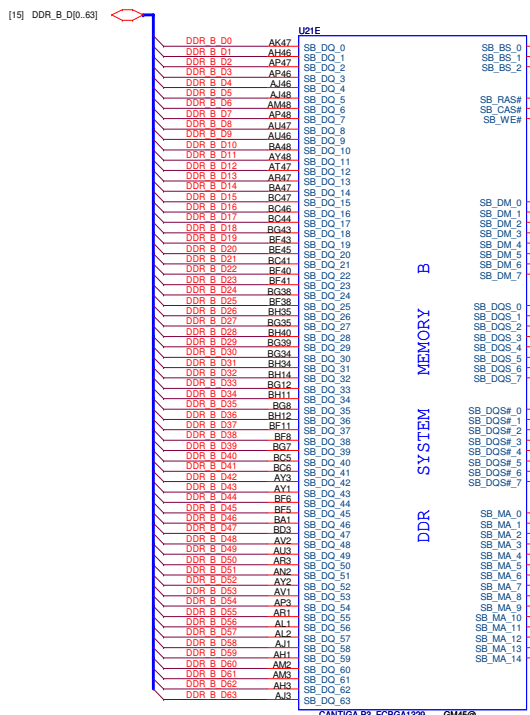
Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation 1 = DMI Lane Reversal Enable * (Default)
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. (Default) 1 = PCIe/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable 1 = LFP Card Present; PCIe disable * (Default)
DDPC_CTRLDATA	0 = Digital DisplayPort Disable 1 = Digital DisplayPort Device Present * (Default)

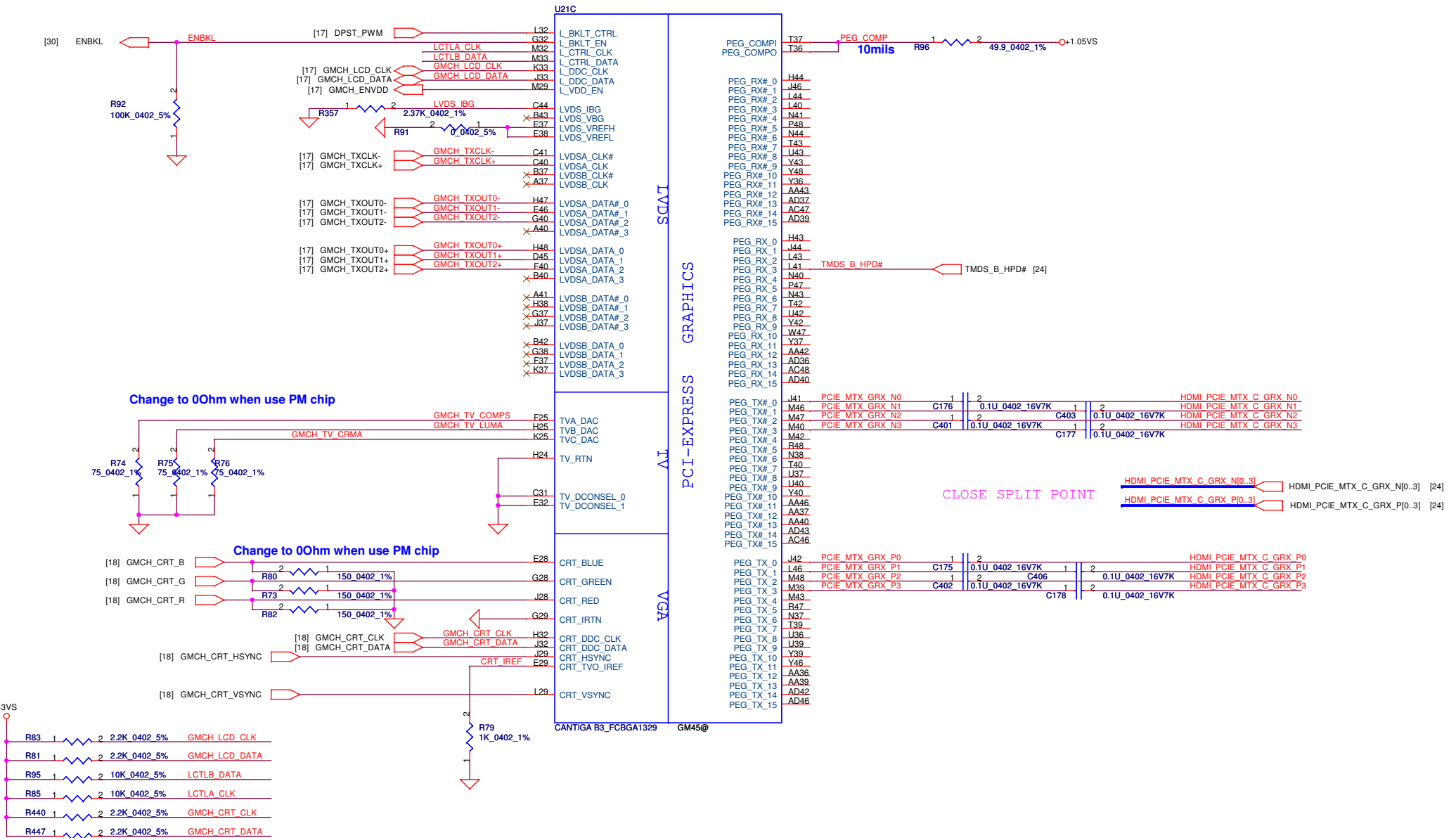




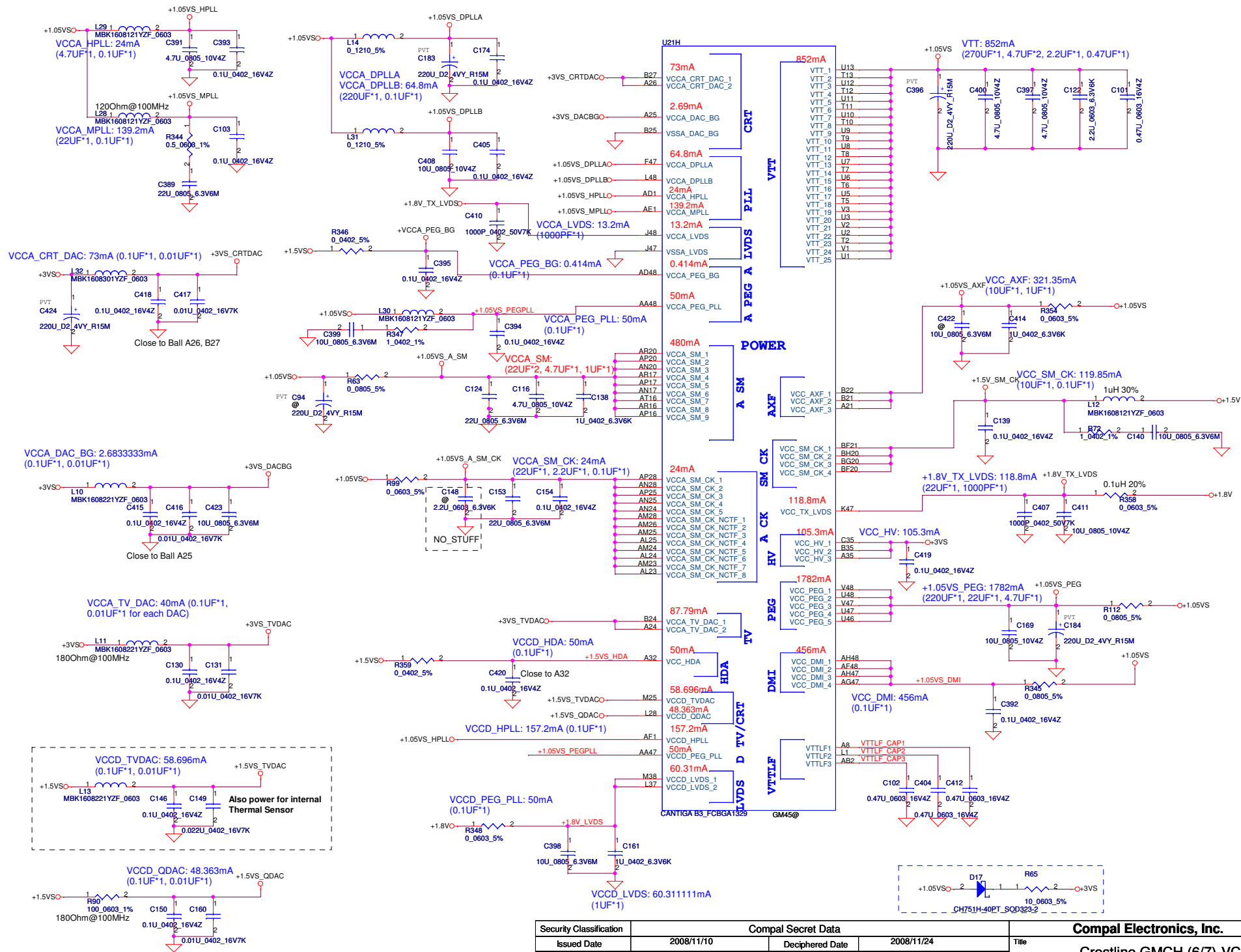
DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B

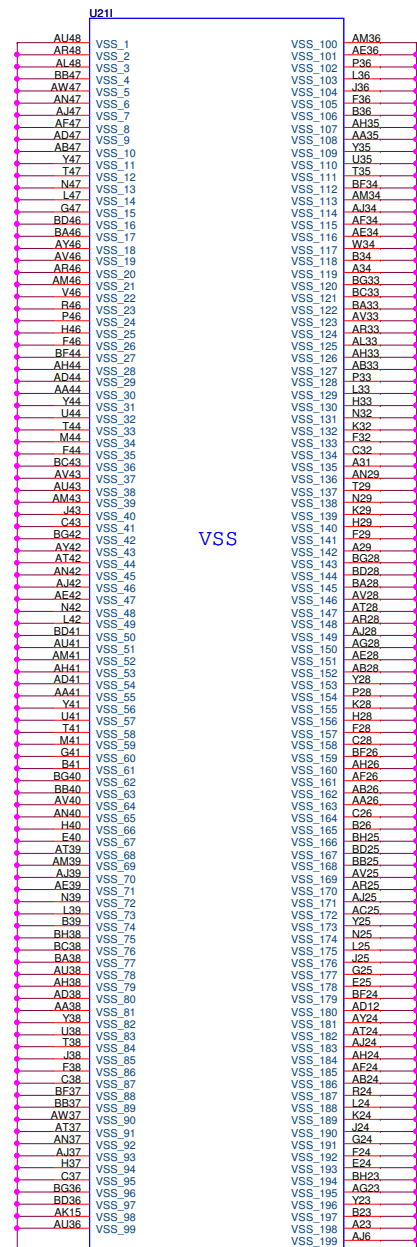


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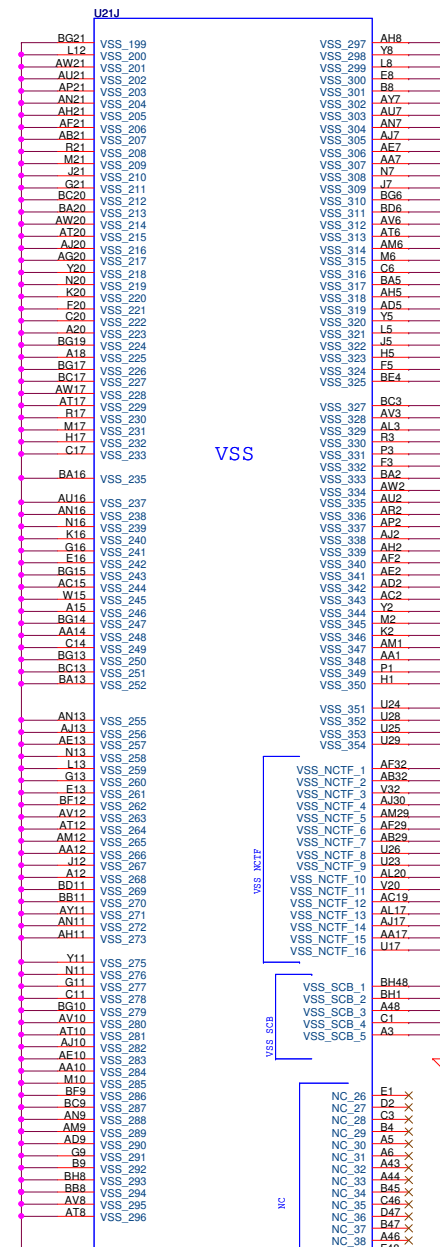


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Crestline GMCH (6/7)-VCC



CANTIGA B3_FCBGA1329 GM45@



CANTIGA B3_FCBGA1329 GM45@

VSS

VSS_NCTF

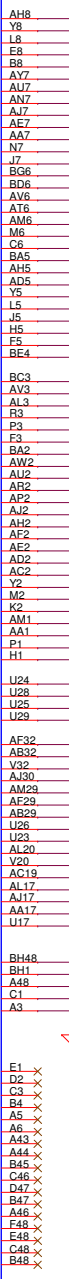
VSS_SCB

NC

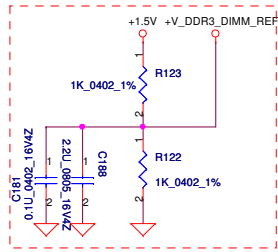
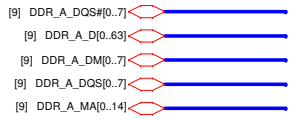
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VSS_NCTF_2
VSS_NCTF_3
VSS_NCTF_4
VSS_NCTF_5
VSS_NCTF_6
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VSS_NCTF_8
VSS_NCTF_9
VSS_NCTF_10
VSS_NCTF_11
VSS_NCTF_12
VSS_NCTF_13
VSS_NCTF_14
VSS_NCTF_15
VSS_NCTF_16

VSS_SCB_1
VSS_SCB_2
VSS_SCB_3
VSS_SCB_4
VSS_SCB_5

NC_26
NC_27
NC_28
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NC_42

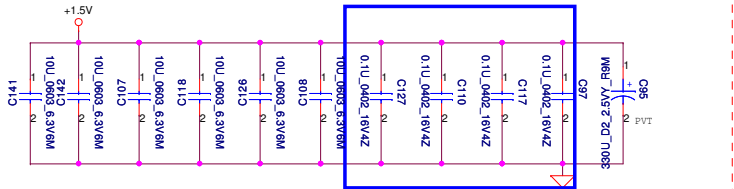


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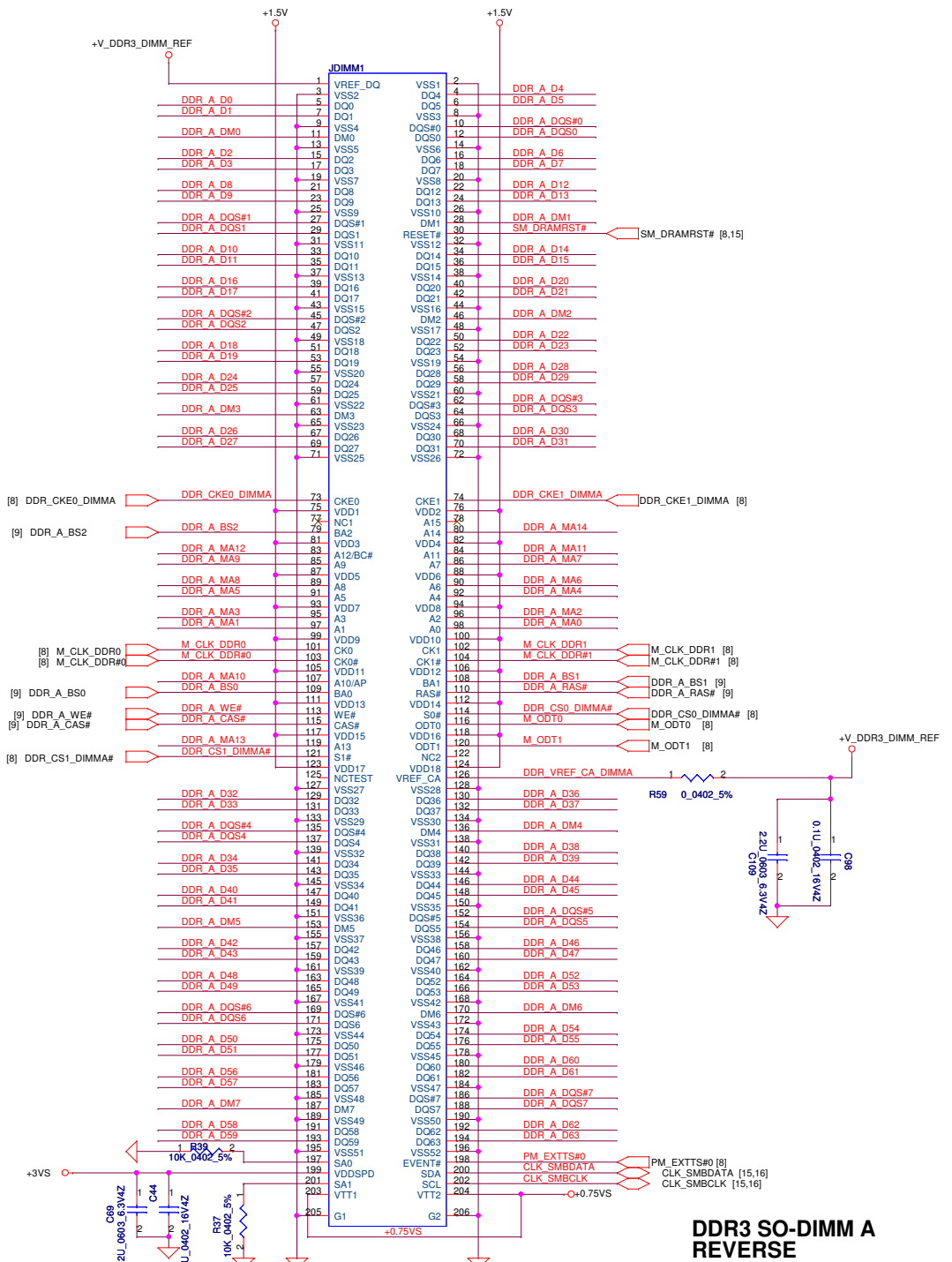
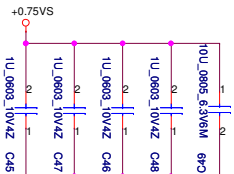


Layout Note:
Place near JP4

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

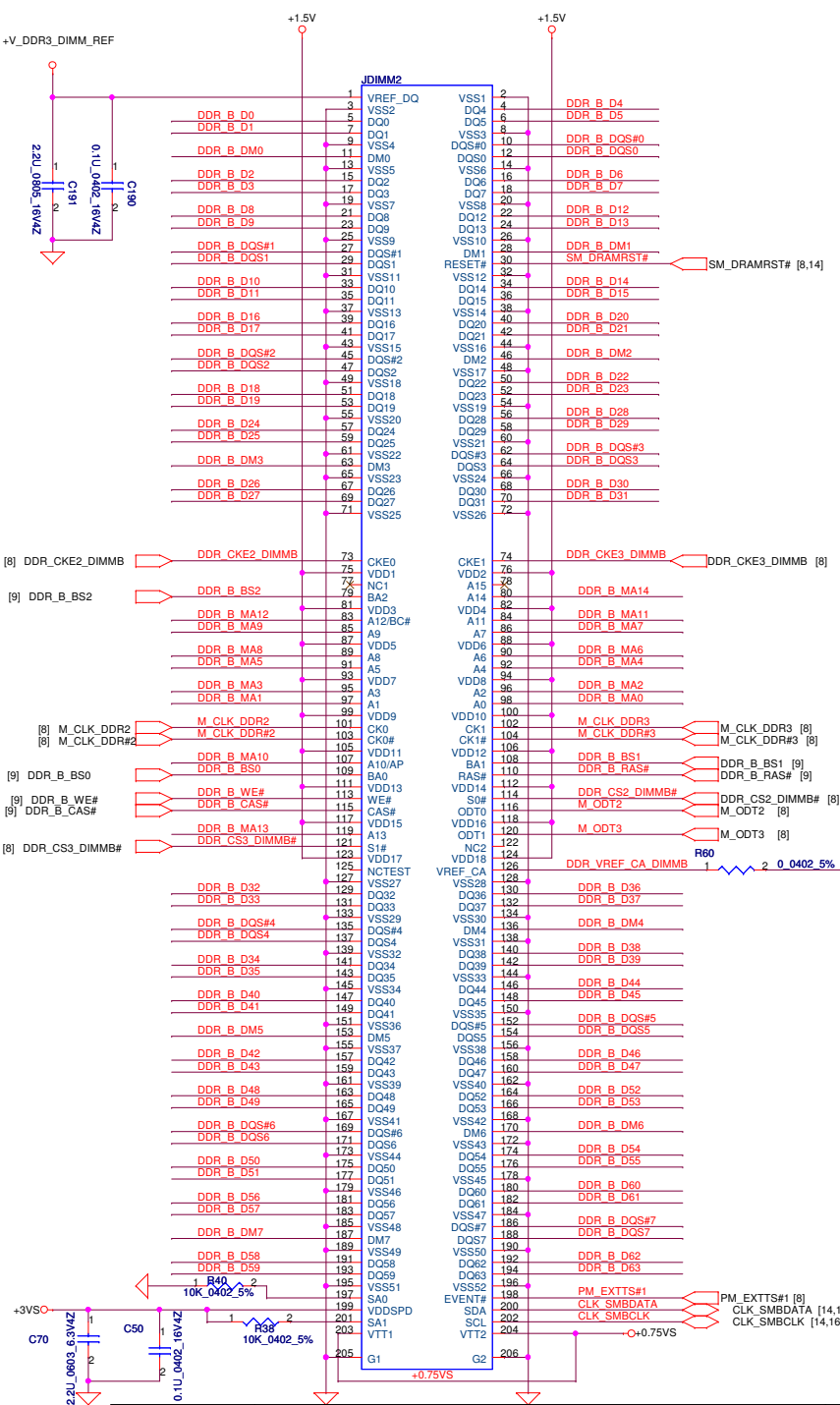
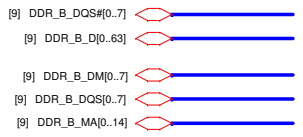


Layout Note:
Place near JP4.203 & JP4.204



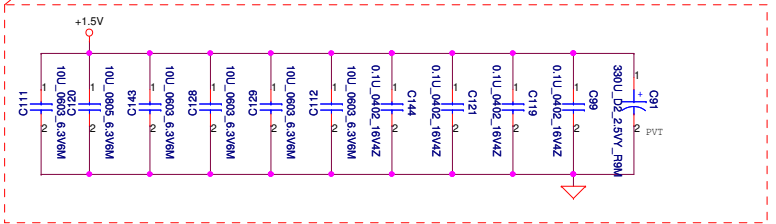
**DDR3 SO-DIMM A
REVERSE**

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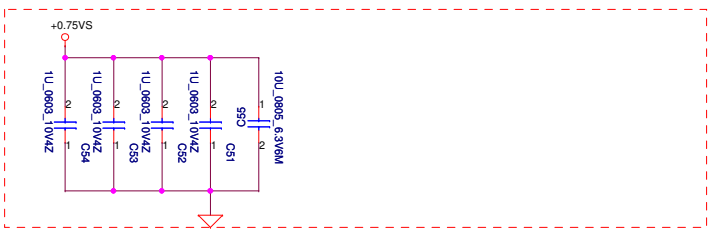


Layout Note:
Place near JP5

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB



Layout Note:
Place near JP5.203 & JP5.204



DDR3 SO-DIMM B REVERSE

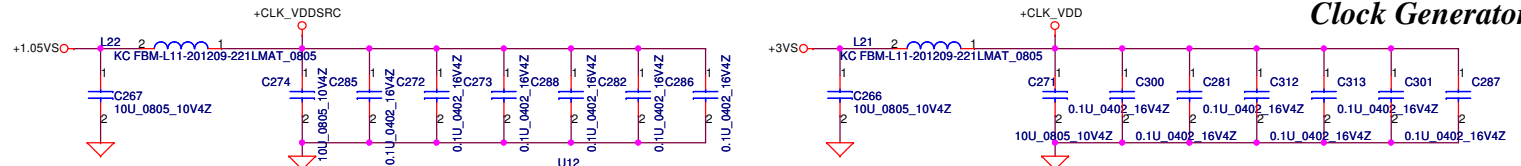
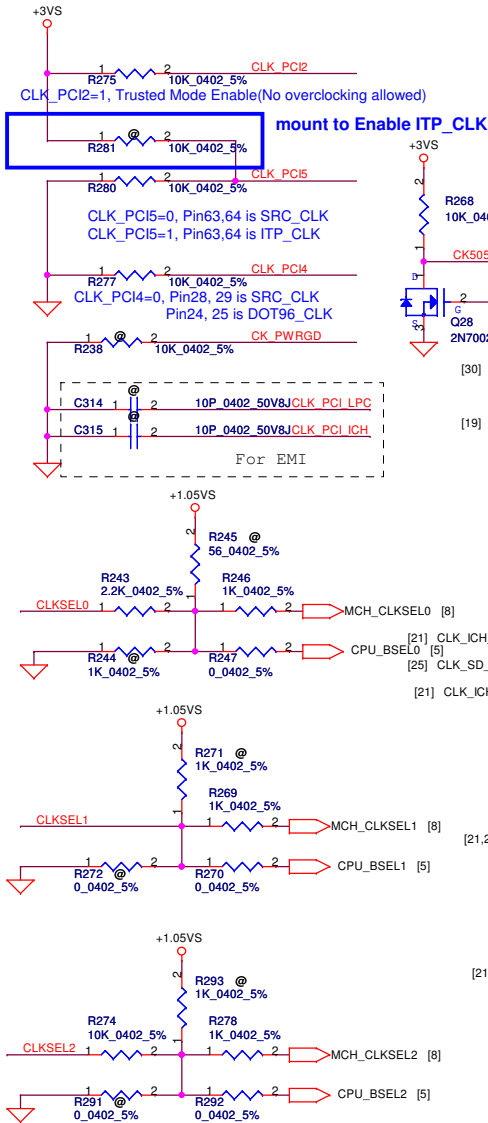
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FSLC	FSLB	FSLA	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

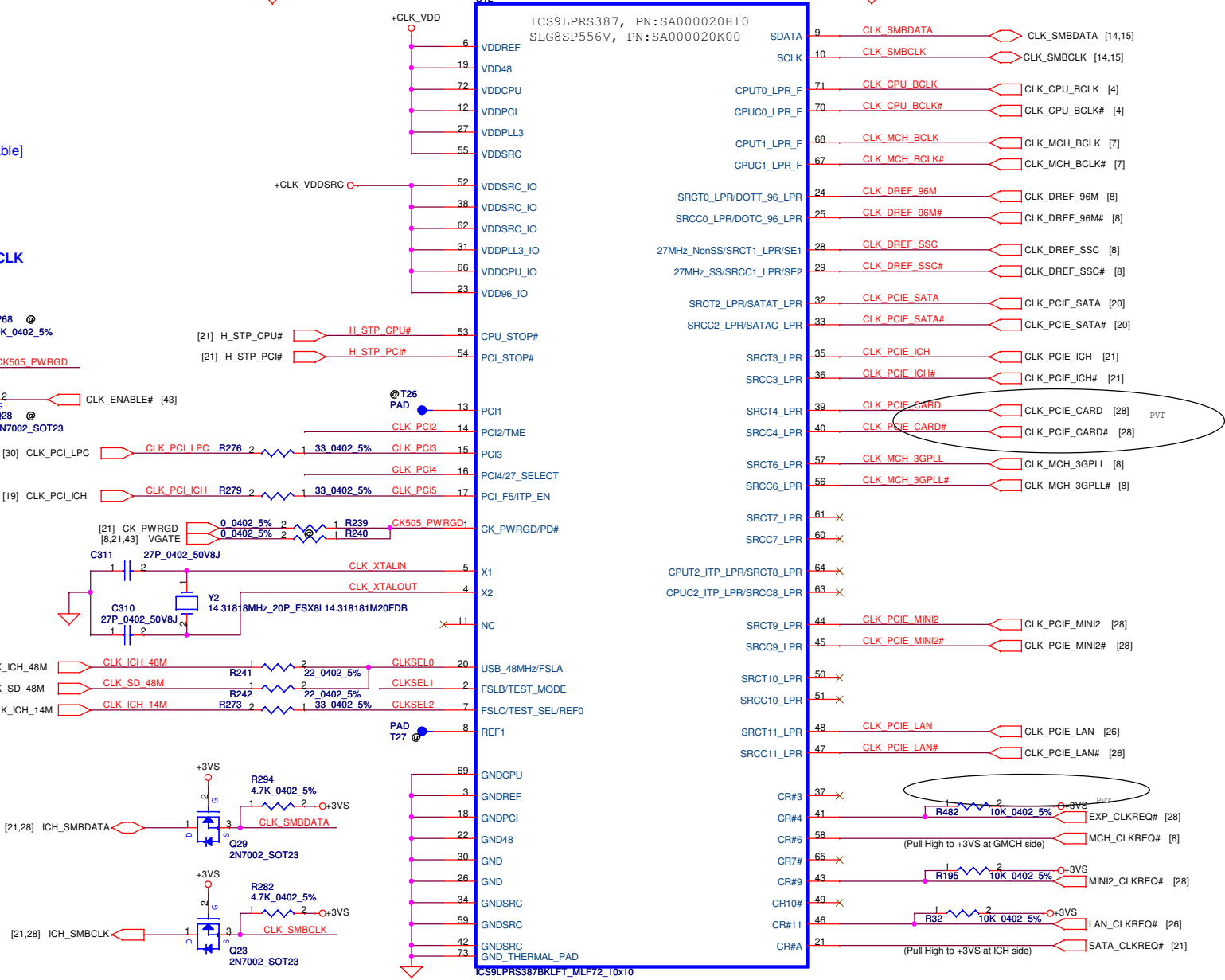
Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SRC7(VGA_CLK): Discrete VGA[Enable] UMA[Disable]

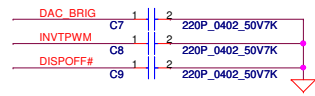
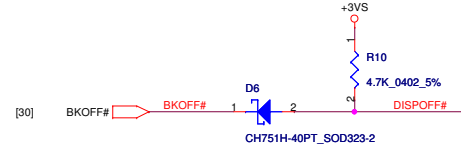
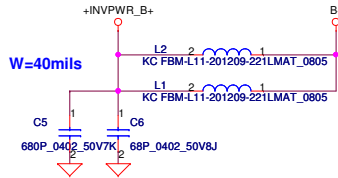
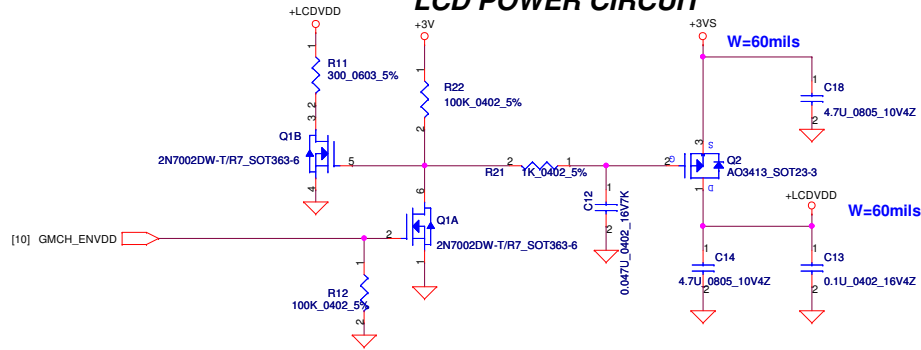


Clock Generator

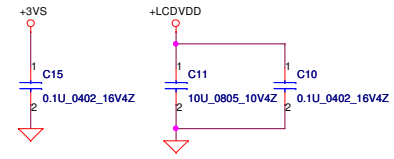
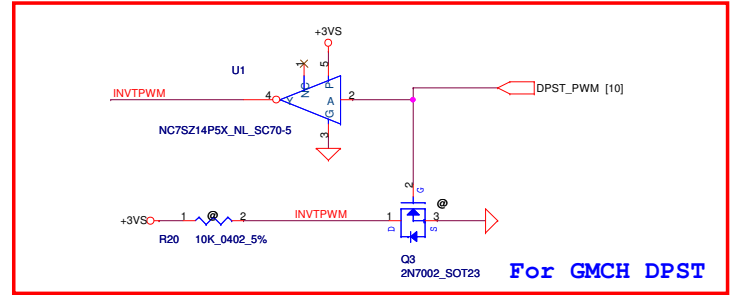
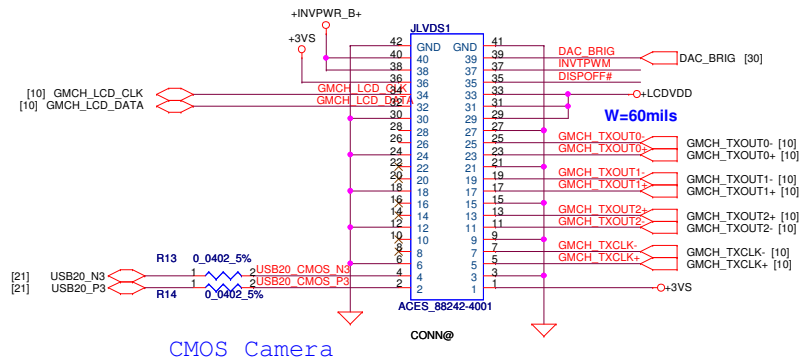


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Size	Document Number	Date		Sheet	Rev
Custom	KALG1	Tuesday, March 24, 2009		16	0.1
				of	45

LCD POWER CIRCUIT

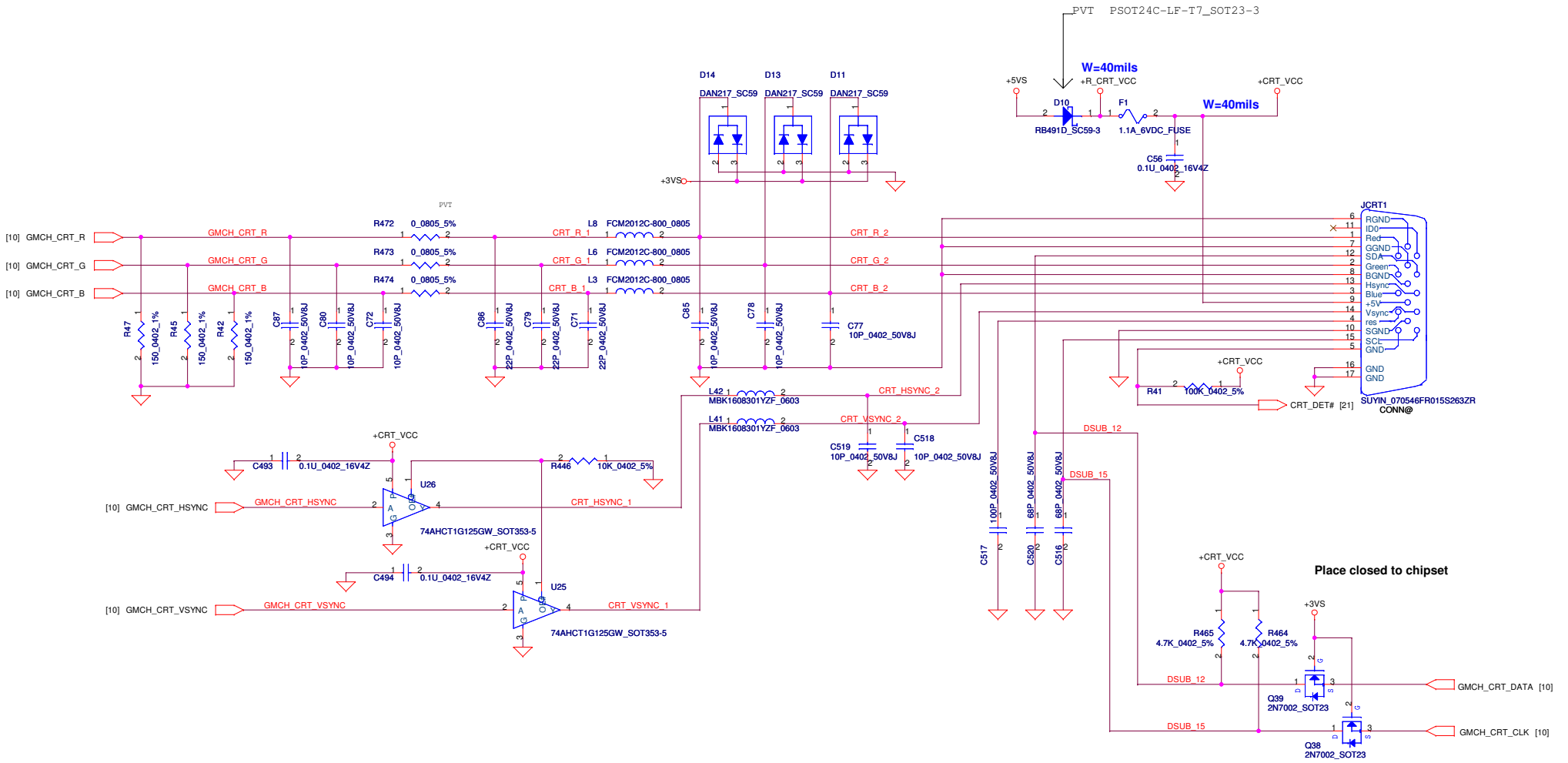


LCD/PANEL BD. Conn.

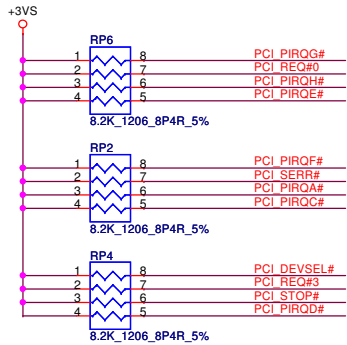
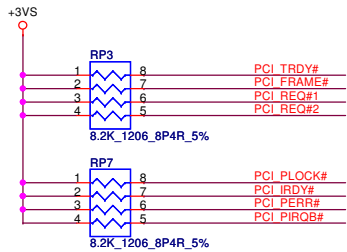


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Date: Tuesday, March 24, 2009			Sheet 17 of 45	

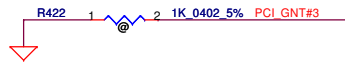
CRT Connector



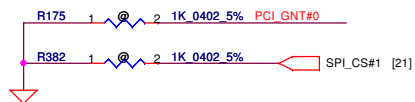
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Date: Tuesday, March 24, 2009				Sheet	18 of 45



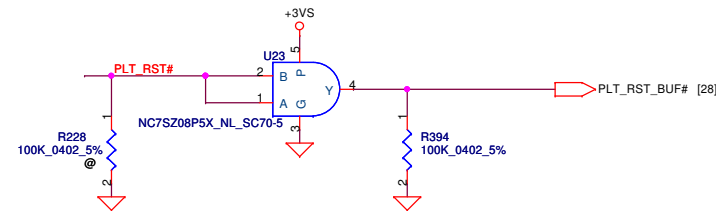
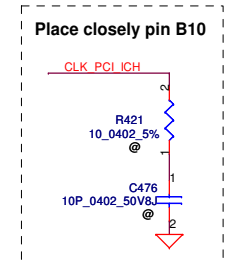
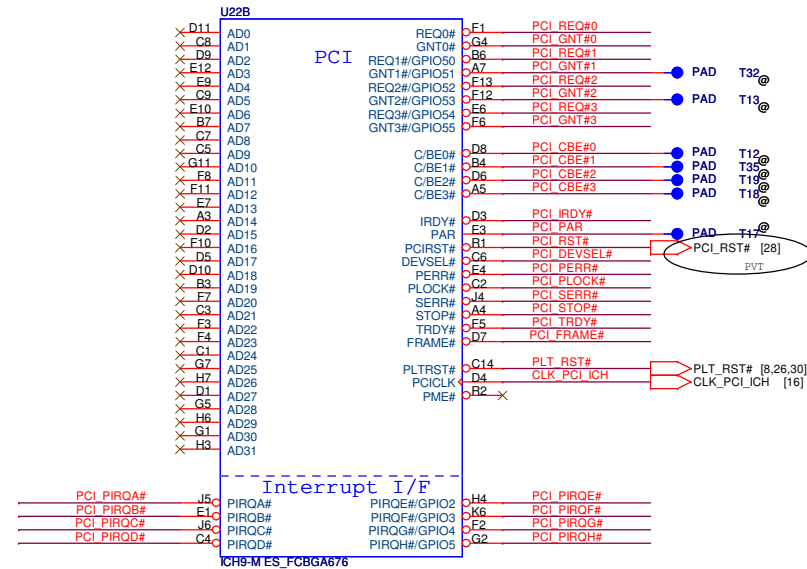
A16 Swap Override Strap
PCI_GNT#3 Low= A16 swap override Enable
 High= Default*



Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

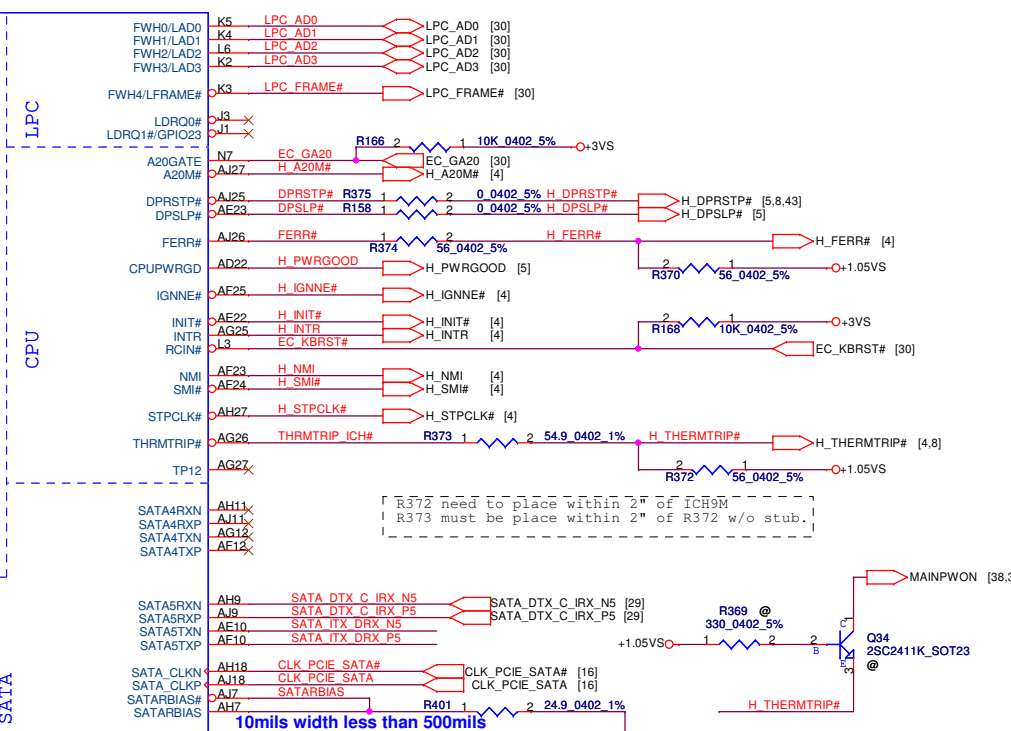
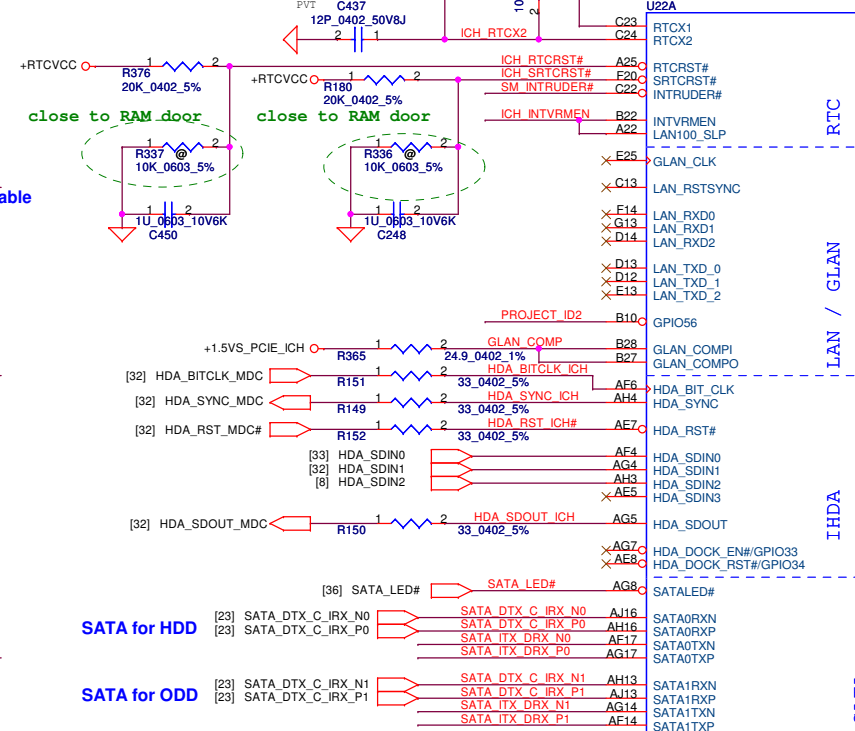
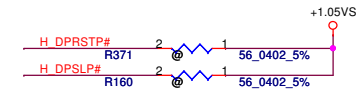


DMI for ESI-compatible operation
PCI_GNT#1 Low= DMI for ESI-compatible operation
 High= Default* (Internal pull-up)

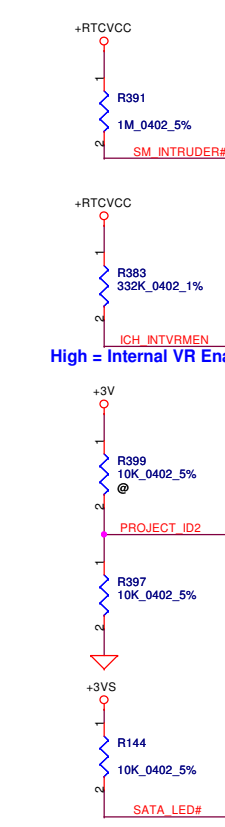


CMOS Settings	R337	TPM Settings	R336
Clear CMOS	SHORT	Clear ME RTC Registers	SHORT
Keep CMOS	OPEN	Keep ME RTC Registers	OPEN

Reset r1290 for power on then shut down issue



R372 need to place within 2" of ICH9M
R373 must be place within 2" of R372 w/o stub.



close to RAM door

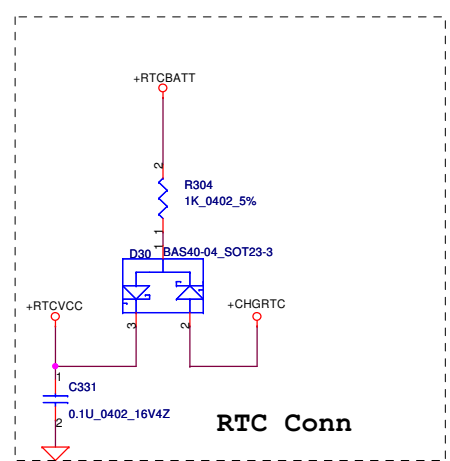
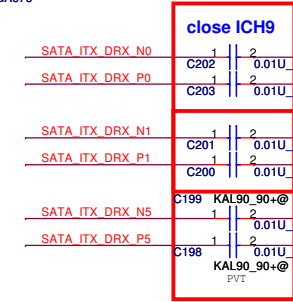
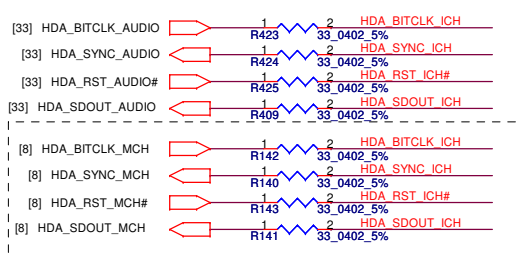
SATA for HDD

SATA for ODD

HDA for AUDIO

HDA for GMCH

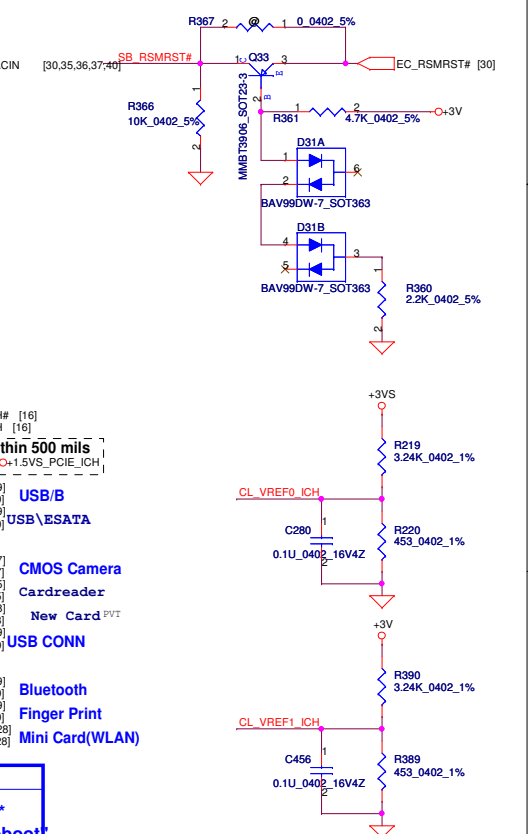
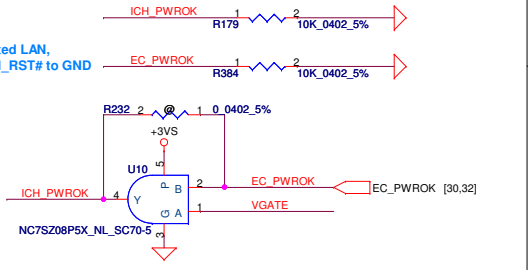
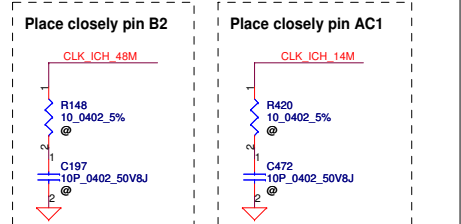
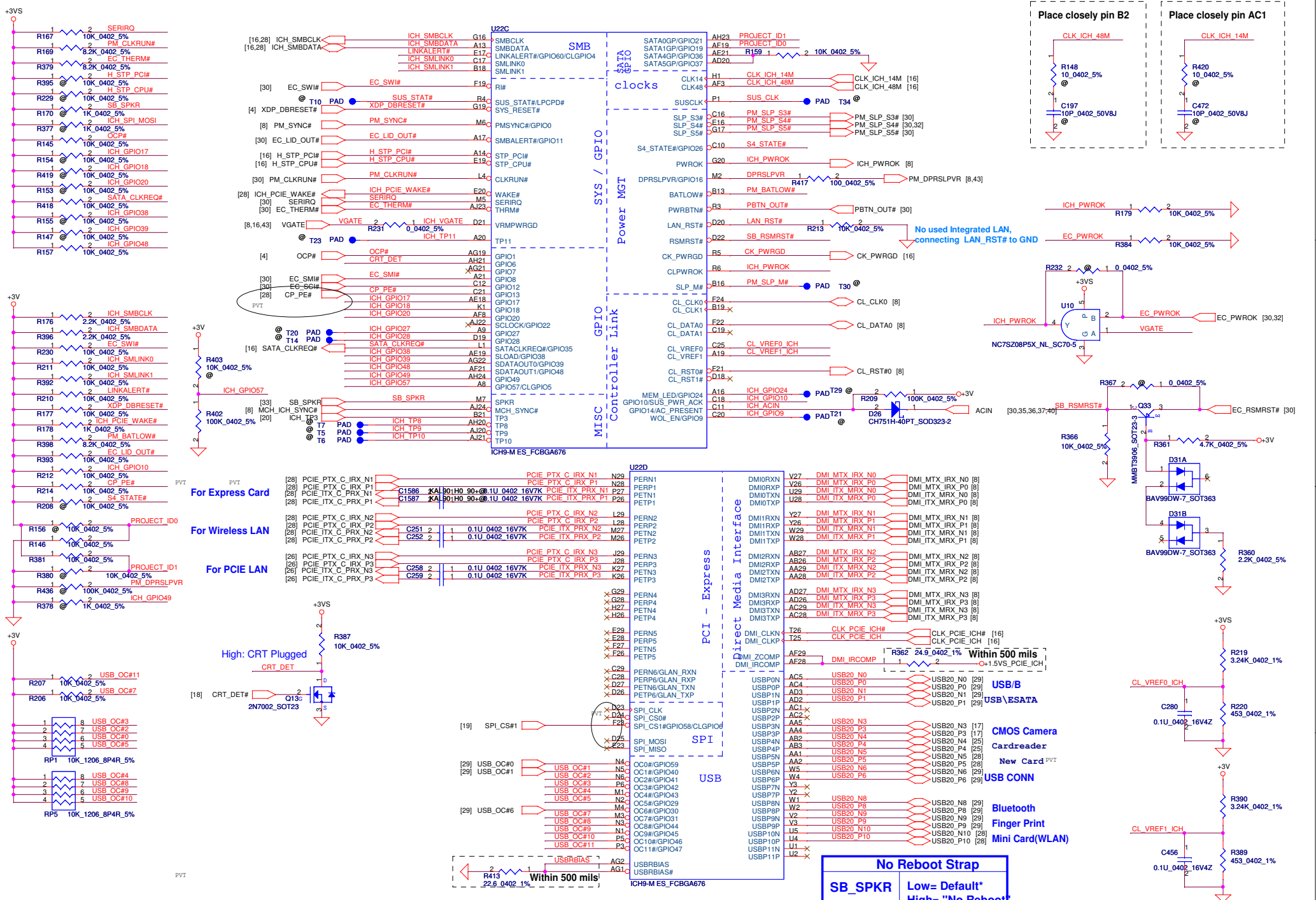
PROJECT_ID	ID0	ID1	ID2
KAL90	0	0	0
KAL90+	1	0	0
KALG1	0	1	0
KALG0	1	1	0



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

Flash Descriptor Security Override Strap
GPIO33 Low= Descriptor Security override
High= Default* (Internal pull-up)

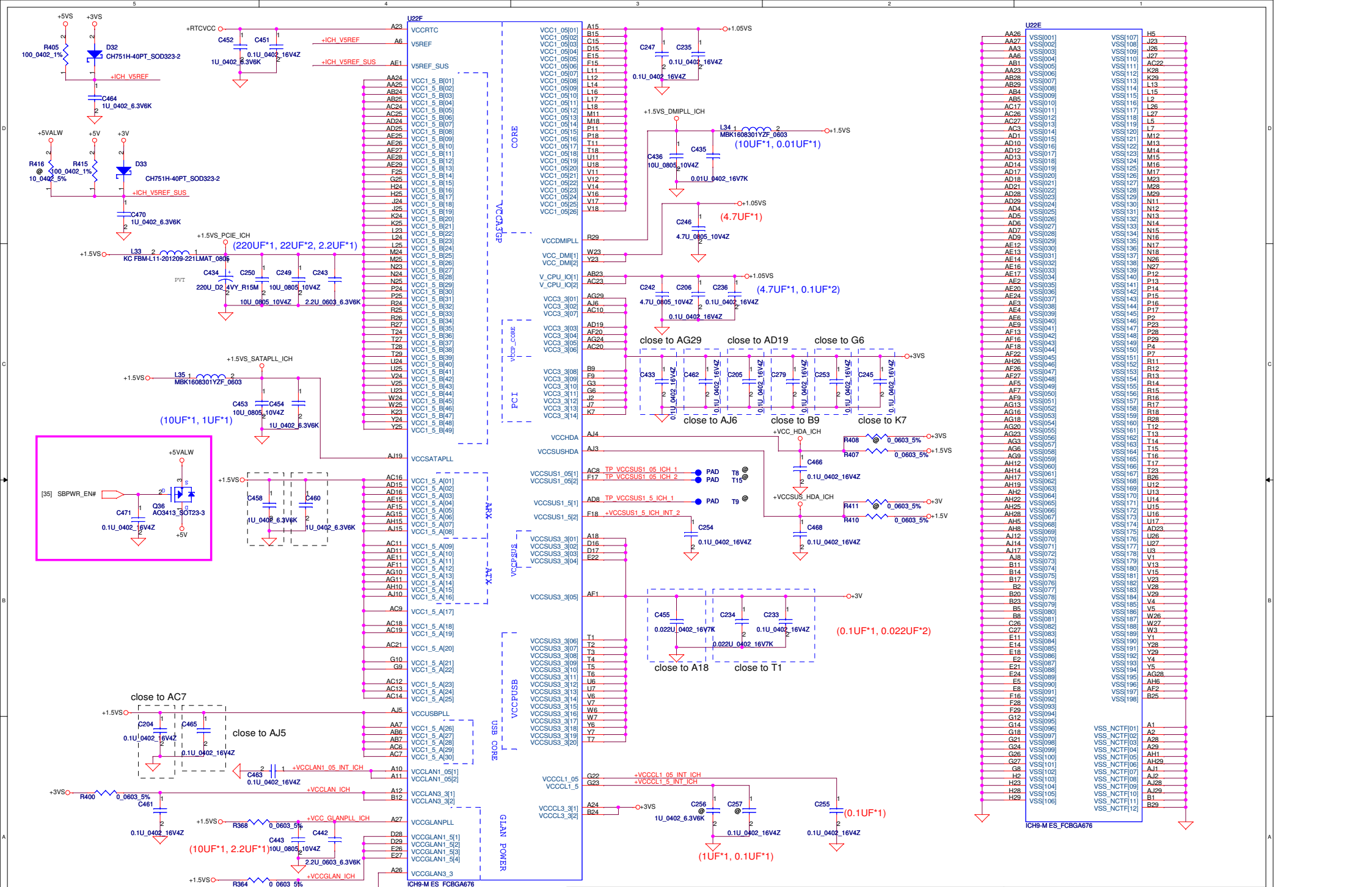
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Issued Date	2008/11/10	Deciphered Date	2008/11/24	ICH9M(2/4)-LAN, IDELPC, RTC		
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Internal TPM Strap	DMI Termination Voltage
SPI_MOSI	GPIO49
Low= Disable*	Low= Desktop used
High= iTPM enable by MCH strap	High= Mobile* (Internal pull-up)

No Reboot Strap
 SB_SPKR Low= Default*
 High= "No Reboot"

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2008/11/10	2008/11/24	KALG1
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Date:	Tuesday, March 24, 2009	Sheet 21 of 45

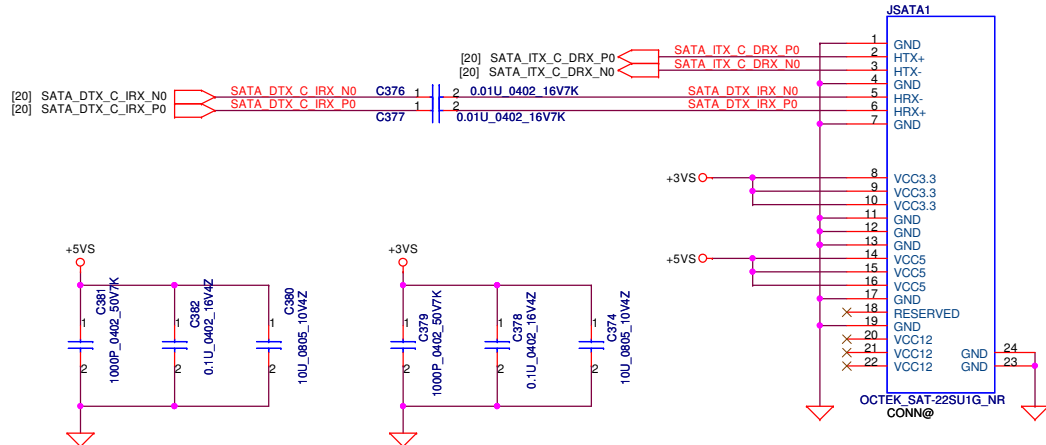


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Issued Date	2008/11/10	Deciphered Date	2008/11/24

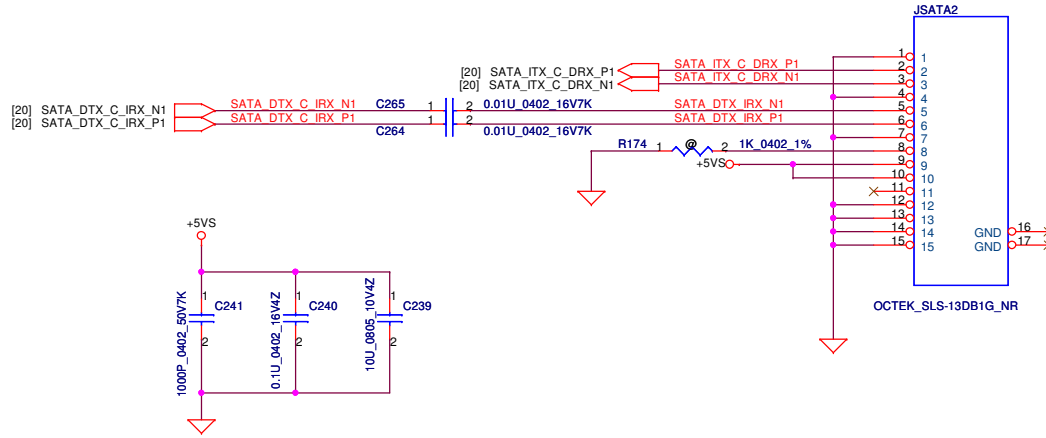
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Compal Electronics, Inc.			
ICH9M(4/4)-POWER&GND			
Size	Document Number	Rev	
Custom	KALG1	0.1	
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SATA HDD Conn.

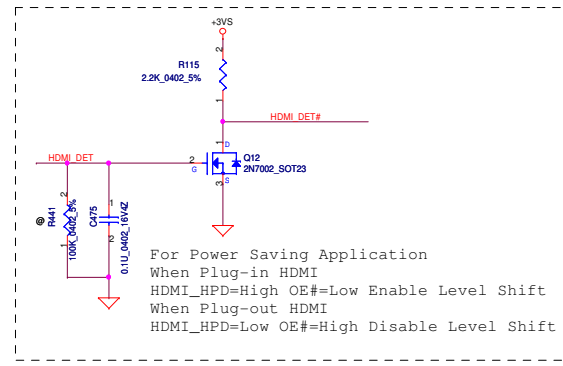
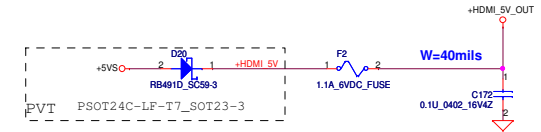
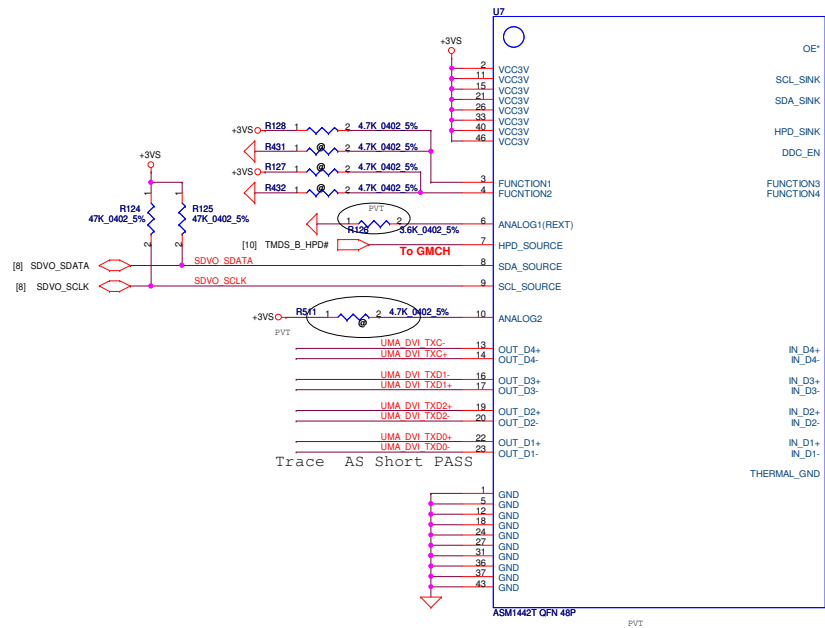
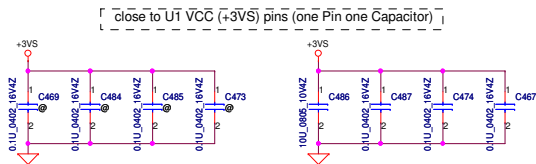


SATA ODD Conn.

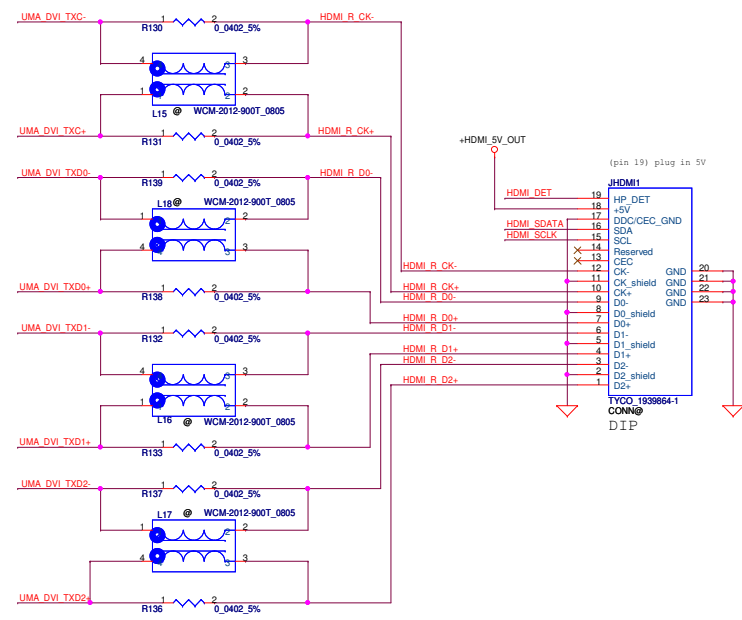


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Title HDD & ODD Connector					
Size Custom	Document Number KALG1				Rev 0.1
Date		Tuesday, March 24, 2009		Sheet 23 of 45	

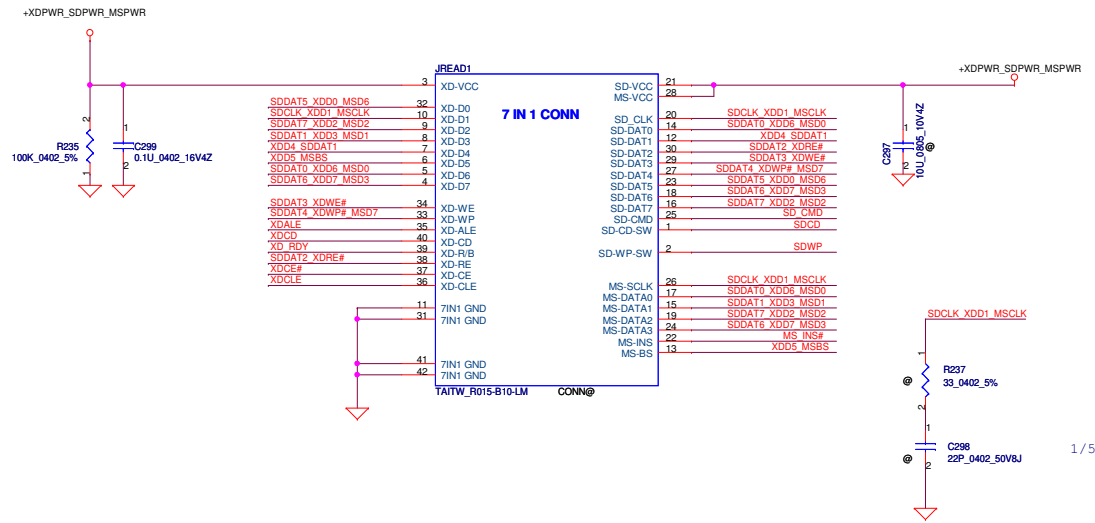
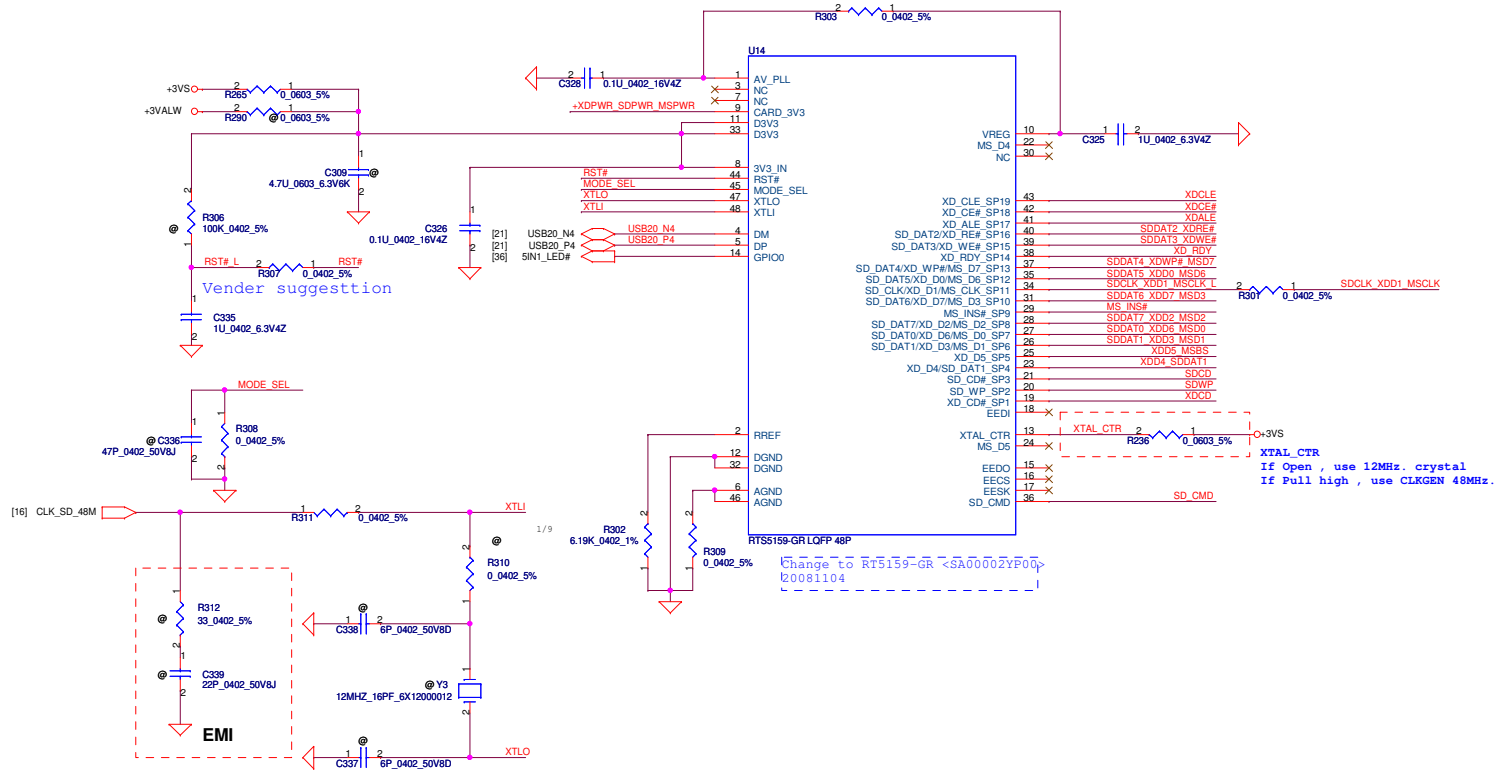
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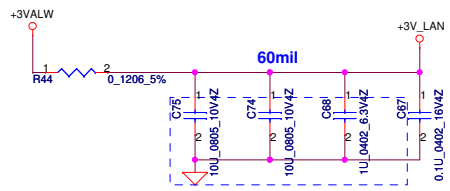
20071031:
Add U1. 49 (THERMAL_GND) to GND Plane



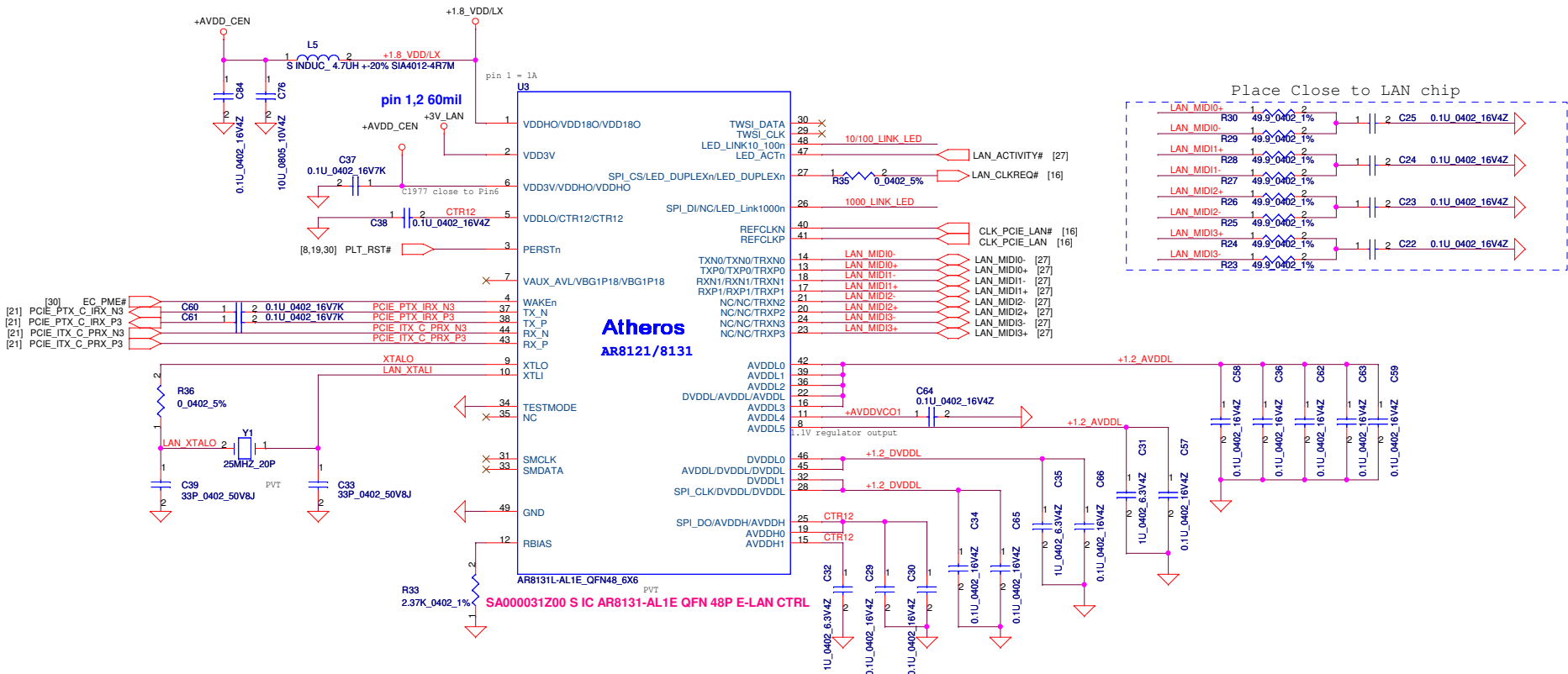
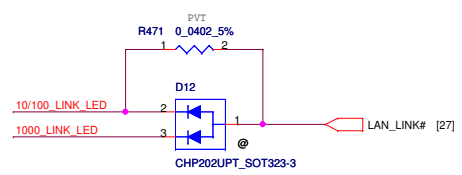
Intel Cantiga TMDS Pin Definition	
TMDS_B_CLK	PEG_TXP_3
TMDS_B_CLK#	PEG_TXN_3
TMDS_B_DATA0	PEG_TXP_2
TMDS_B_DATA0#	PEG_TXN_2
TMDS_B_DATA1	PEG_TXP_1
TMDS_B_DATA1#	PEG_TXN_1
TMDS_B_DATA2	PEG_TXP_0
TMDS_B_DATA2#	PEG_TXN_0
TMDS_B_HPD#	PEG_RXP_3



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Quantity	KALG1	Date		Tuesday, March 24, 2009	
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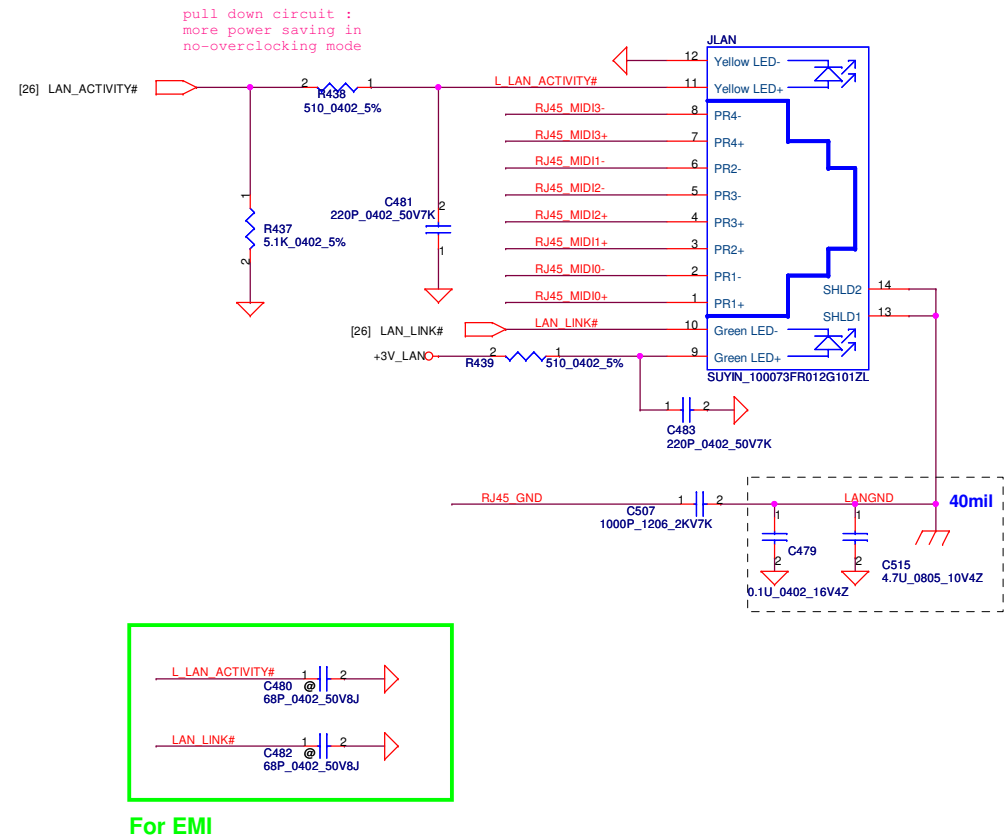
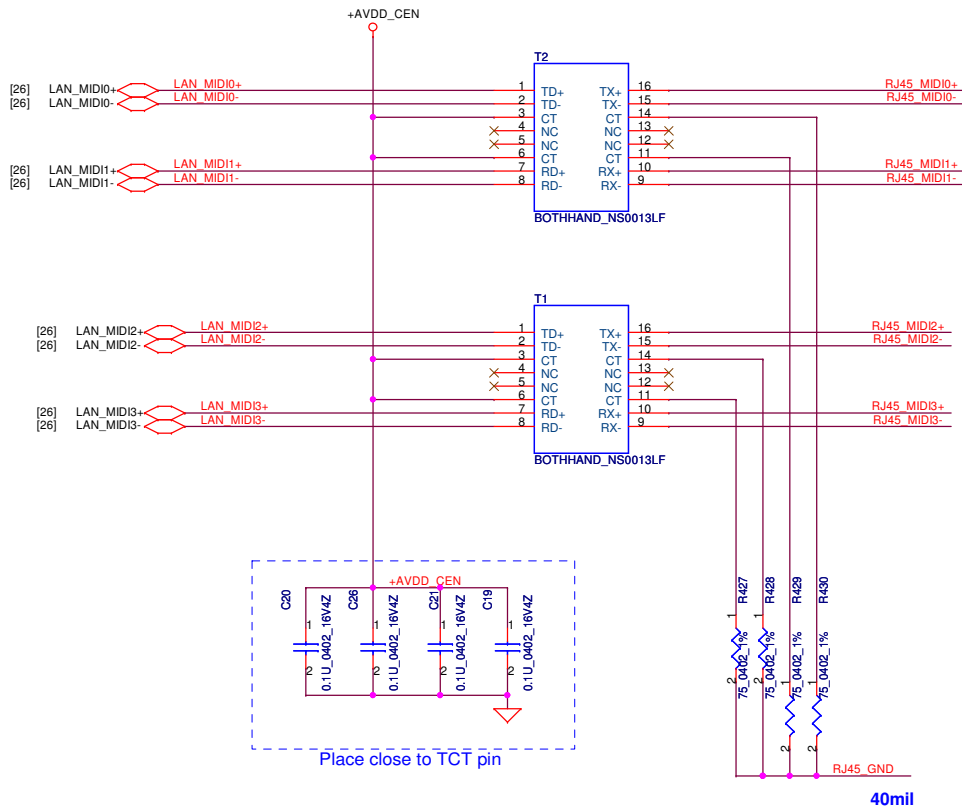


Place Close to Pin 2



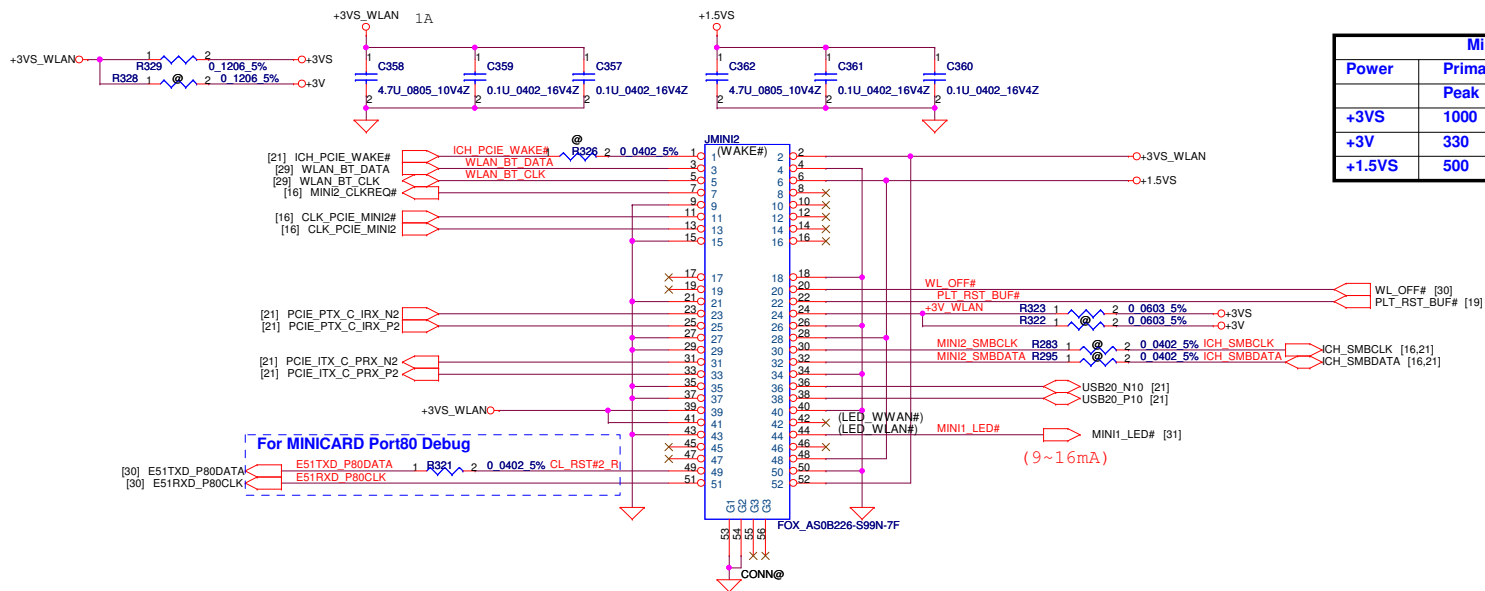
Place Close to LAN chip

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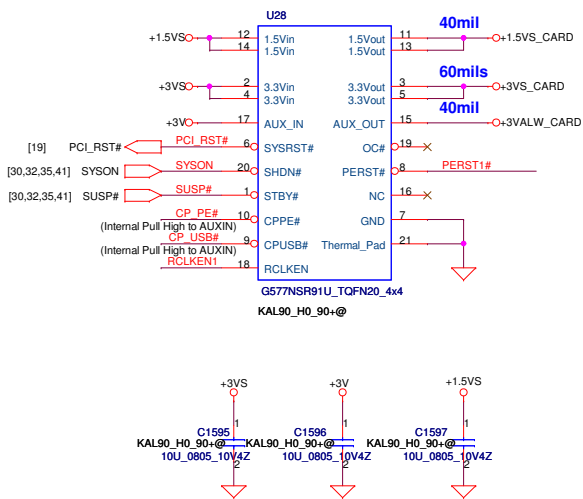
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Issued Date	2008/11/10	Deciphered Date	2008/11/24	Title	
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Size	B	Document Number	KALG1		Rev
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For Wireless LAN

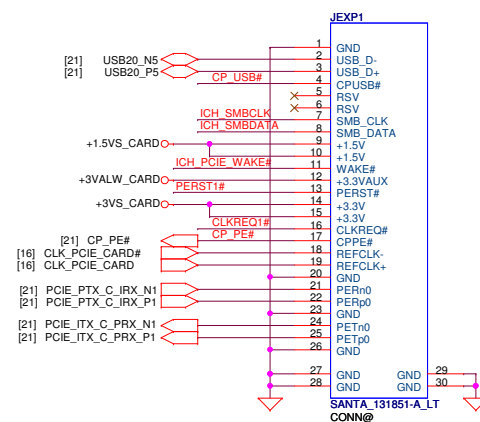
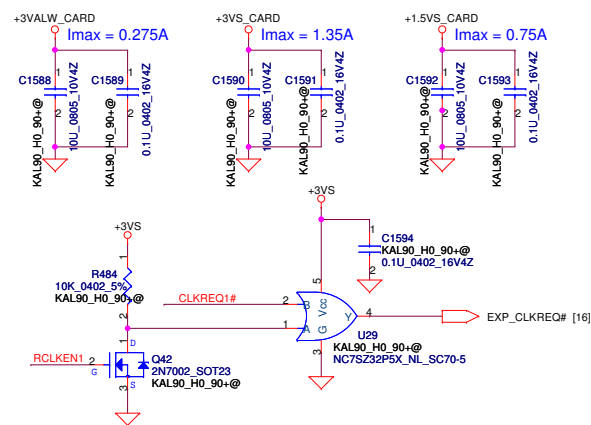


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

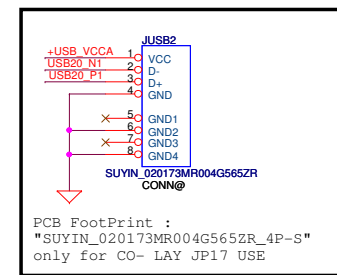
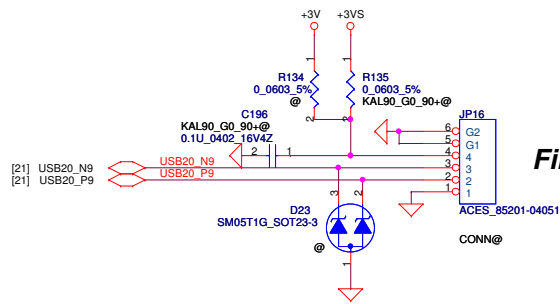
New Card Power Switch



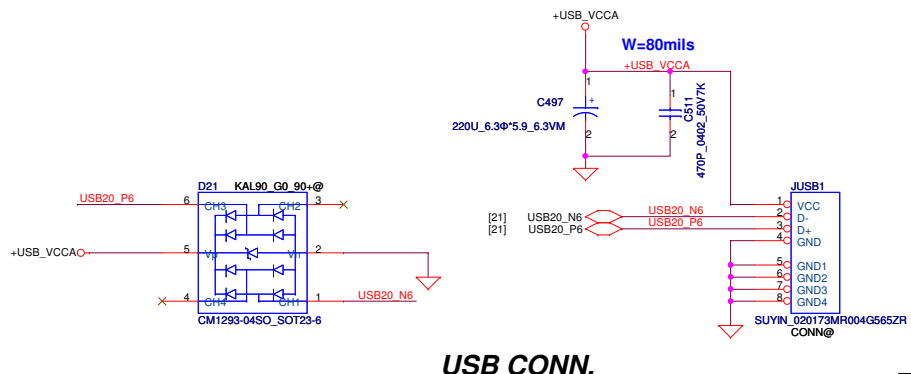
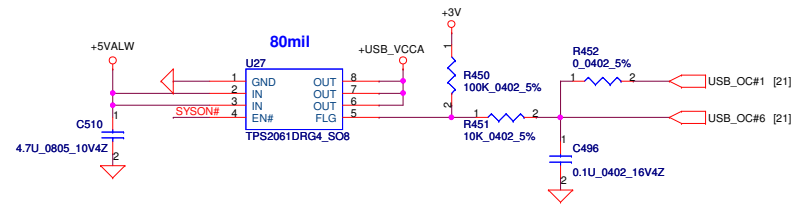
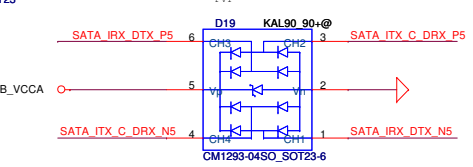
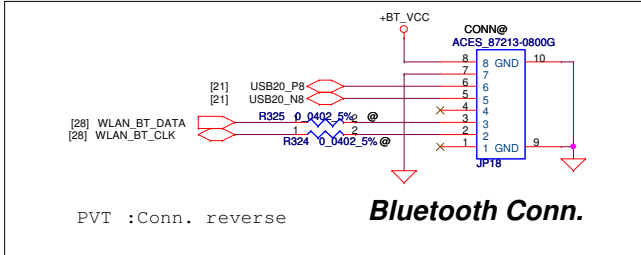
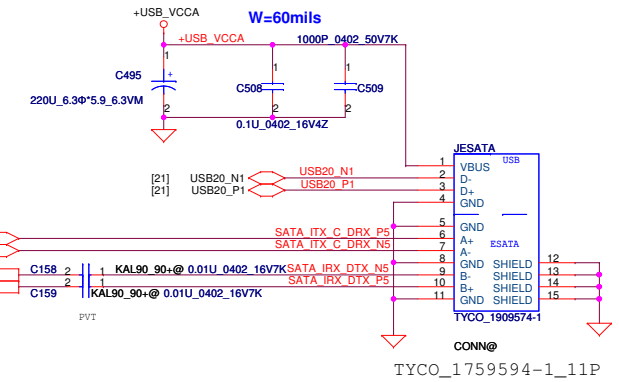
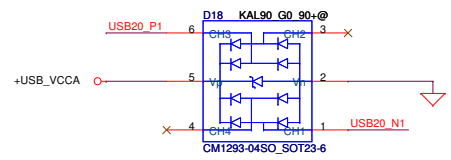
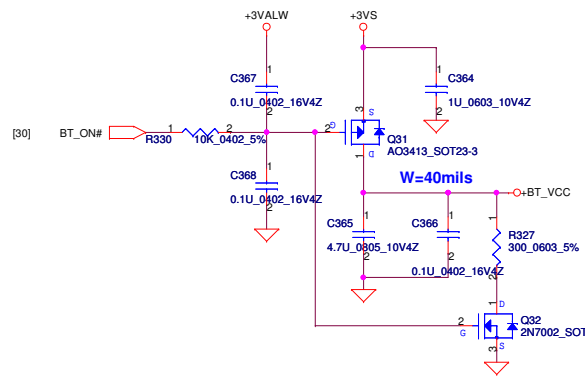
New Card Socket (Left/TOP)



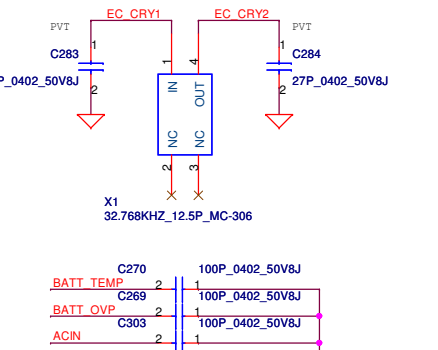
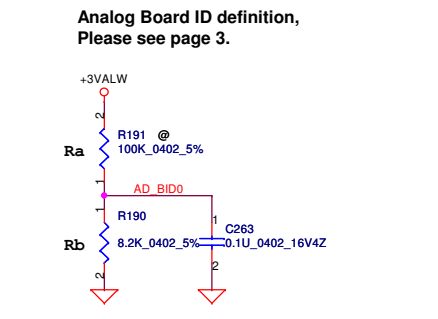
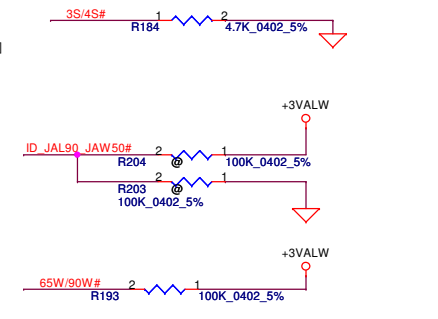
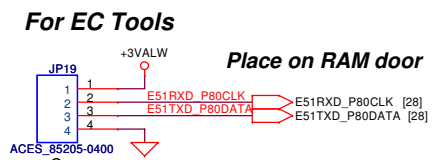
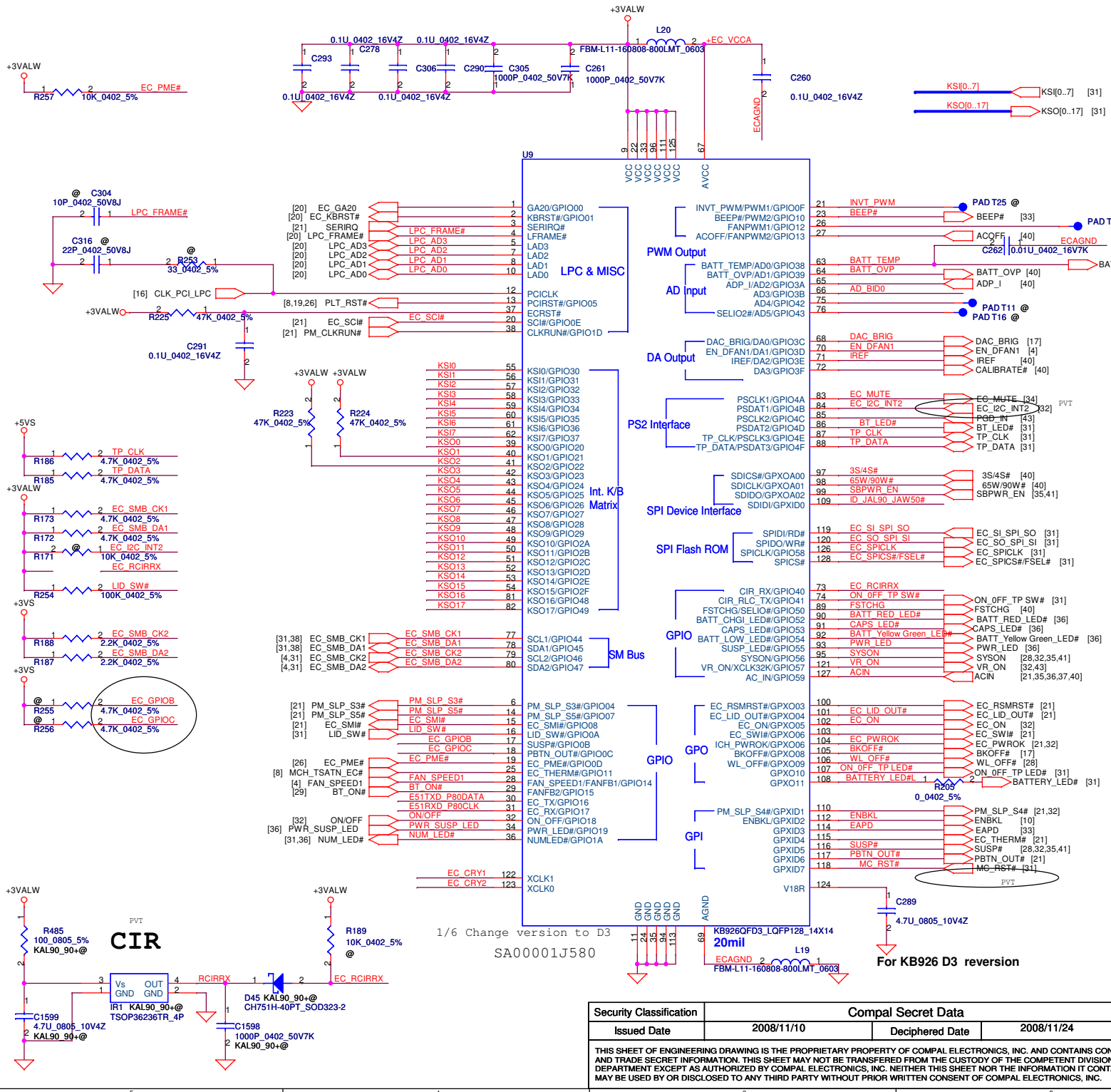
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Issued Date	2008/11/10	Deciphered Date	2008/11/24	Title
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Date: Tuesday, March 24, 2009				Rev 0.1
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ESATA CONN



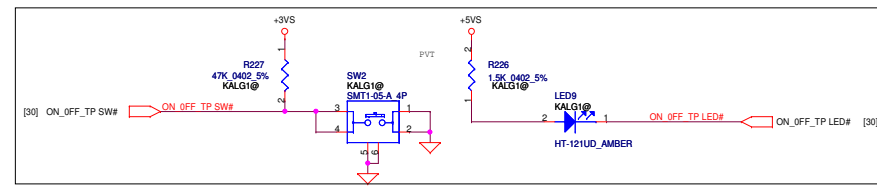
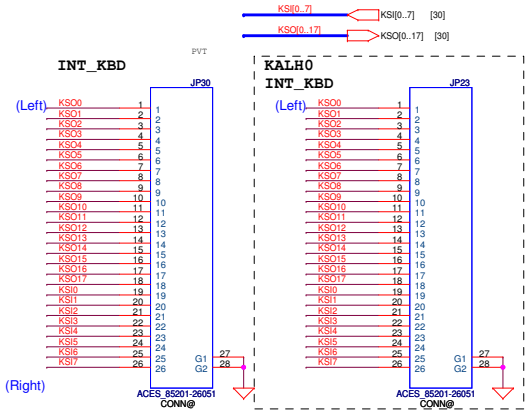
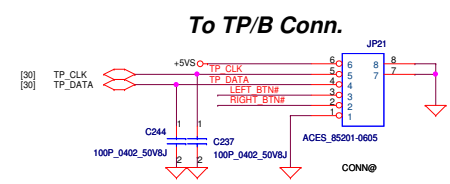
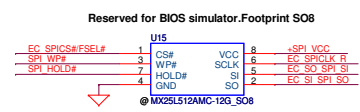
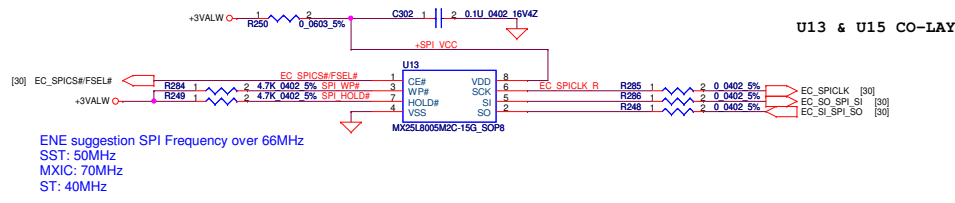
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/11/10	Deciphered Date	2008/11/24	Title
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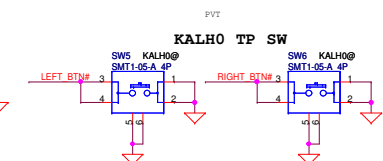
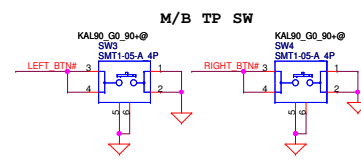
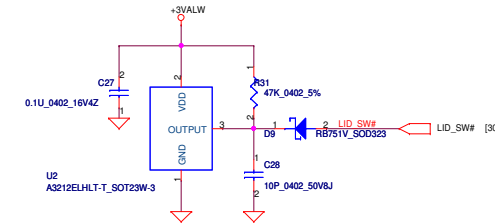
1/6 Change version to D3
SA0001J580
KB926QD3_LQFP128_14X14
20mil
L19
For KB926 D3 reversion

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Issued Date	2008/11/10	Deciphered Date	2008/11/24
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Compal Electronics, Inc.			
Title EC ENE KB926/CIR			
Size B	Document Number KALG1	Rev 0.1	
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Lid Switch (Hall Effect Switch)

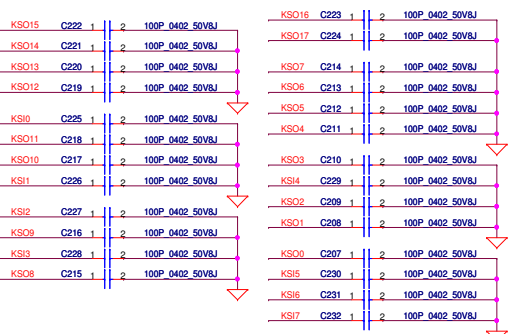
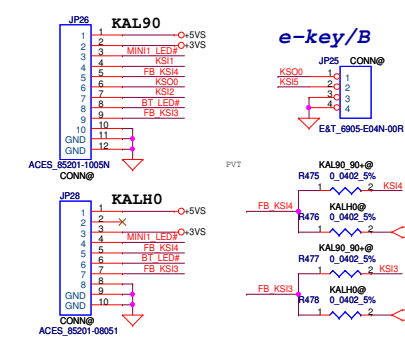


To BTN/B Conn.

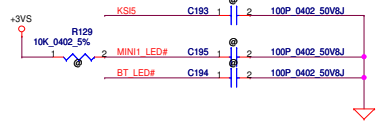
	KSO0
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#

	KSO4	KSO2	KSO3
KSI5	WL_BTN#	Volume Down	Back Up
KSI6	BT_BTN#	Volume Up	Program (KBLG0) Battery (KALG0)

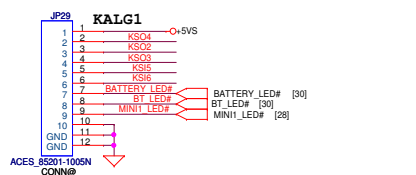
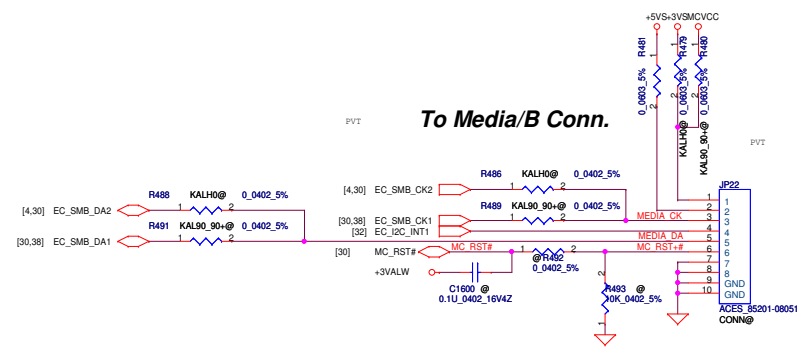
FN/B



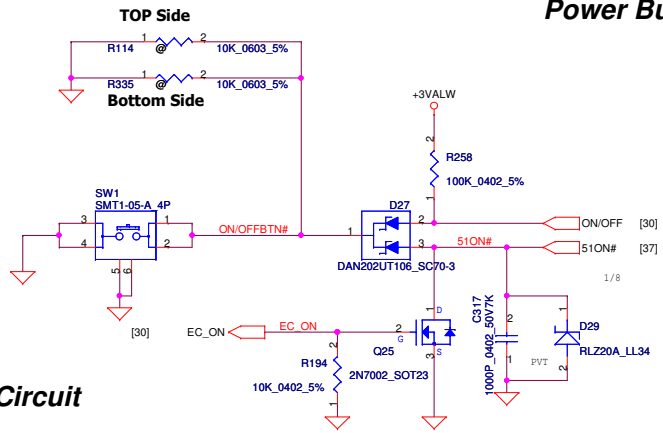
FOR EMI



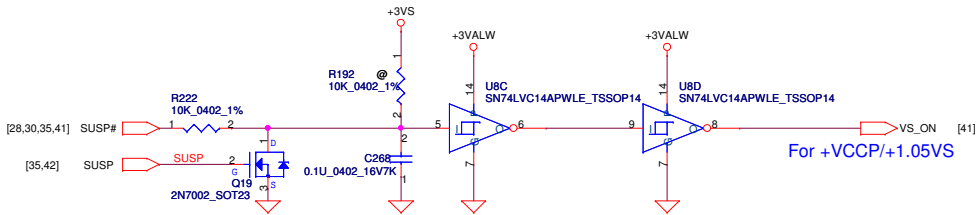
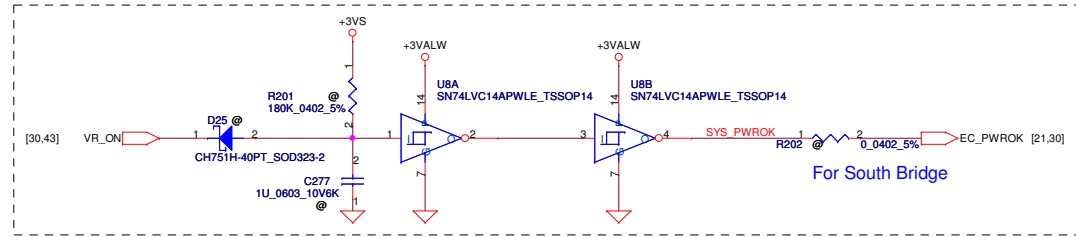
To Media/B Conn.



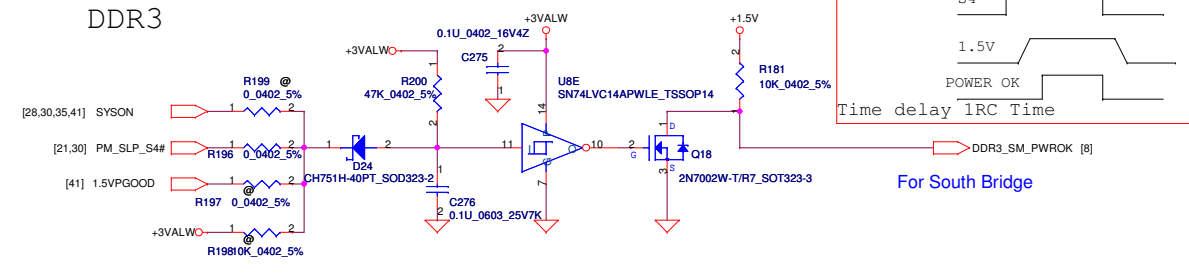
Power Button



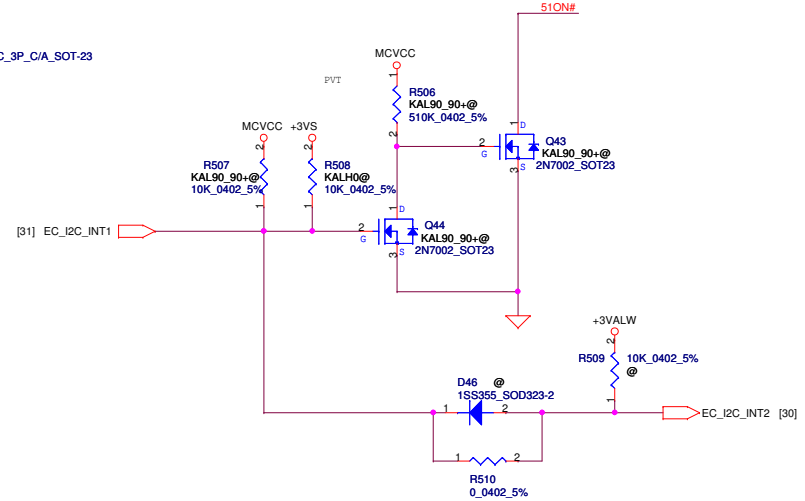
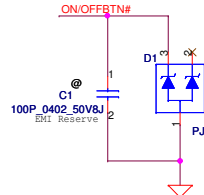
Power ON Circuit



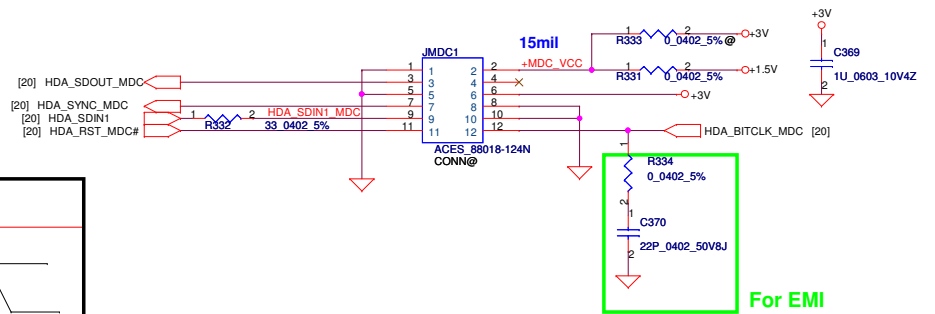
DDR3



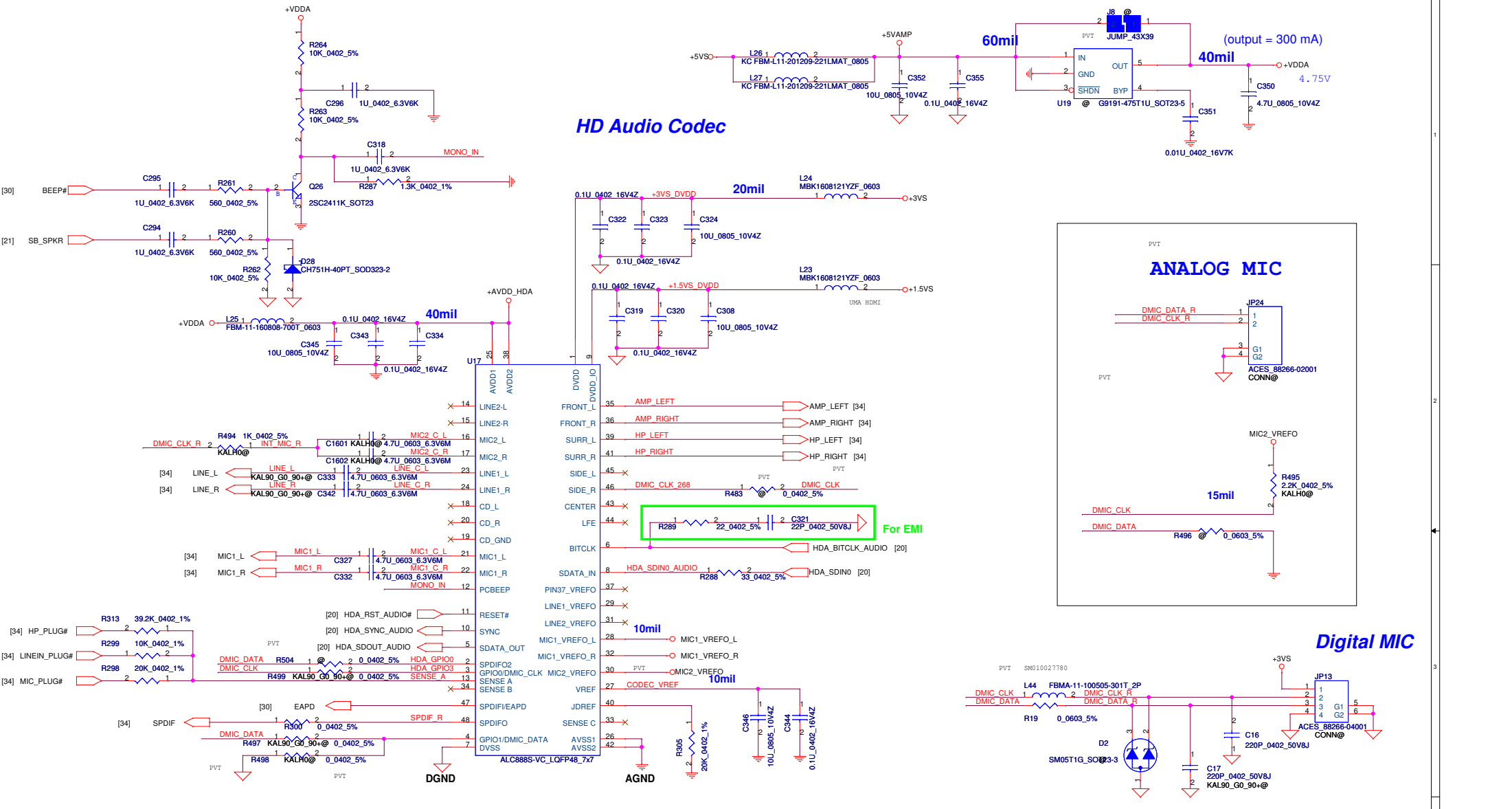
D58 USE
PJSOT24C 3P C/A SOT-23
SCA00000E00
24V



HDA MDC Conn.

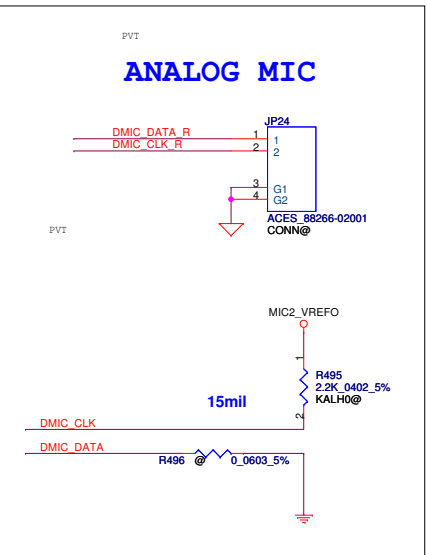


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Issued Date	2008/11/10	Deciphered Date	2008/11/24	Power OK, Reset, MDC	
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File No.	Document Number	Rev	Date: Tuesday, March 24, 2009 Sheet 32 of 45		
	KALG1	0.1			

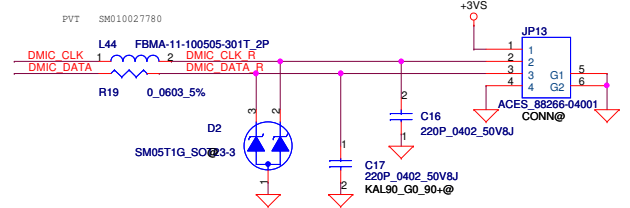


HD Audio Codec

ANALOG MIC



Digital MIC



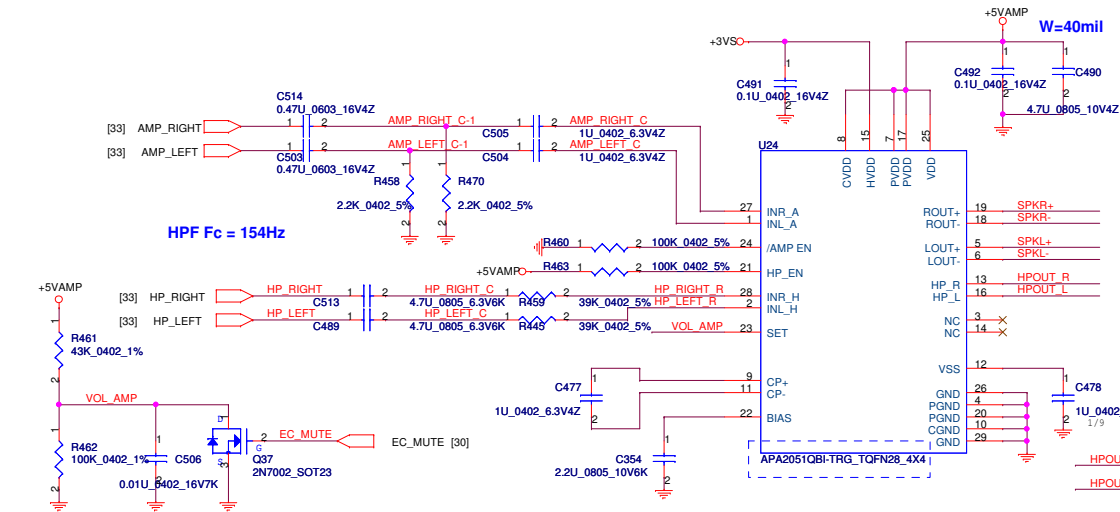
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

SVID=1025
SSID=0260
FOR KALG1 and KALG0.

BOM Option

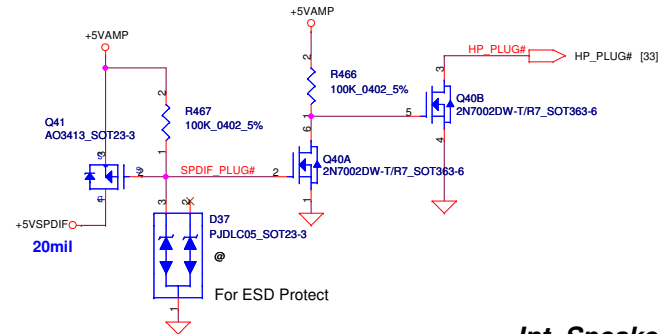
ALC268	268@
ALC888S-VC	888@

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Issued Date	2008/11/10	Deciphered Date	2008/11/24	HD Audio Codec ALC888S-VC
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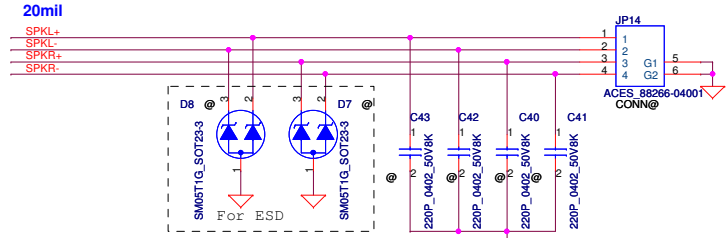


HPF Fc = 154Hz

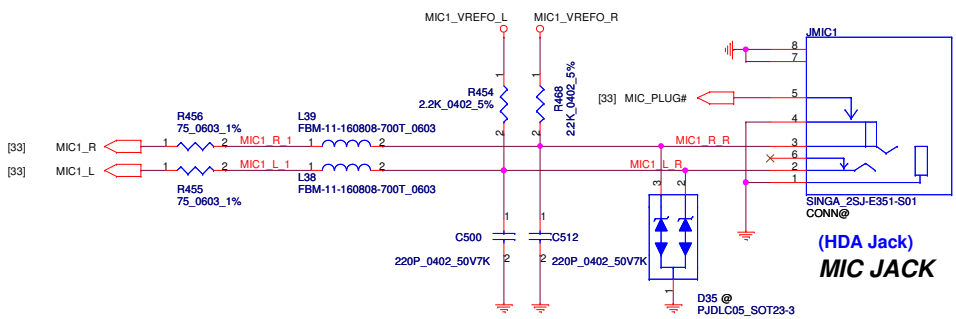
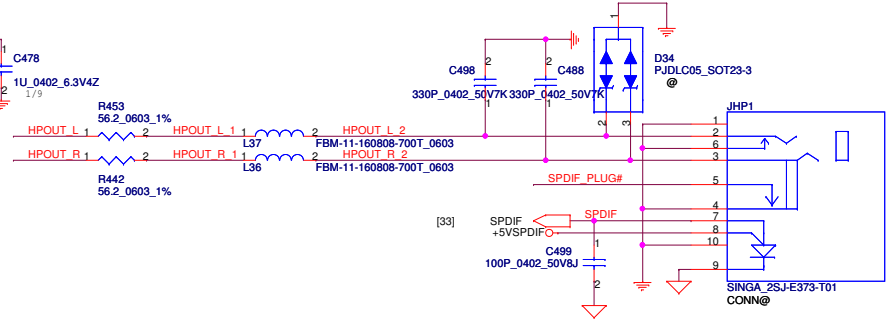
Gain= 10dB



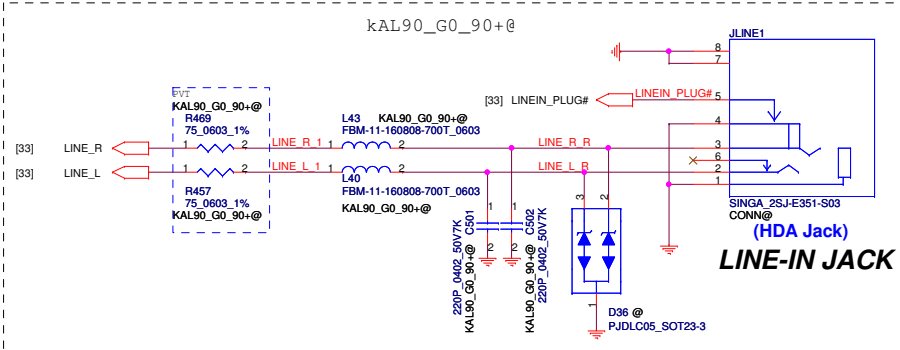
Int. Speaker Conn.



S/PDIF Out JACK
LINE Out/Headphone Out



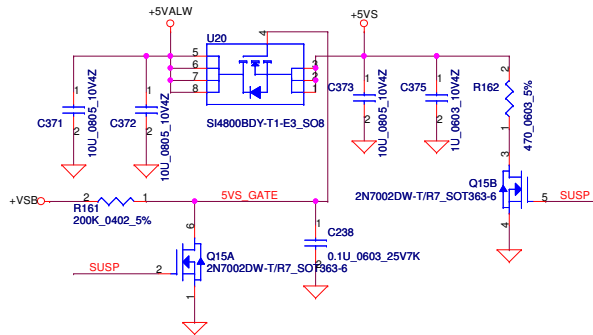
(HDA Jack)
MIC JACK



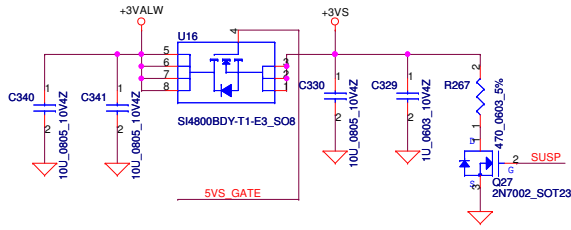
(HDA Jack)
LINE-IN JACK

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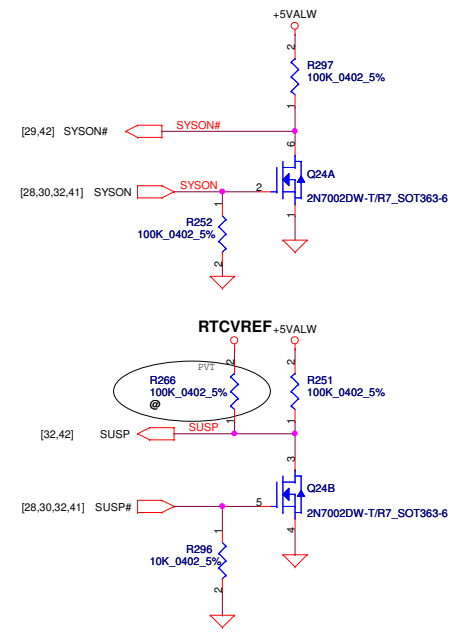
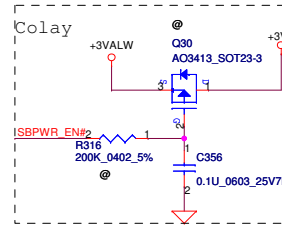
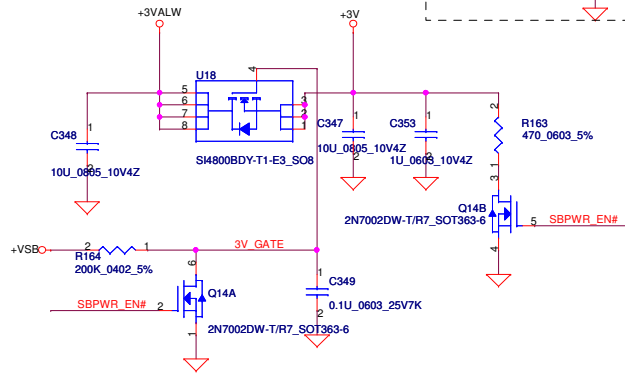
+5VALW TO +5VS



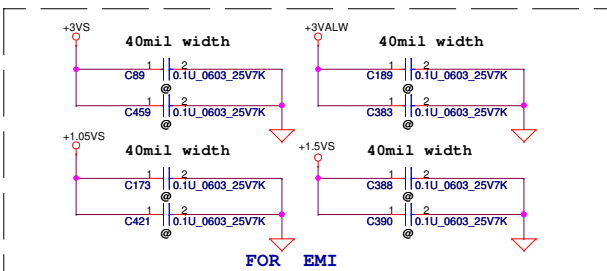
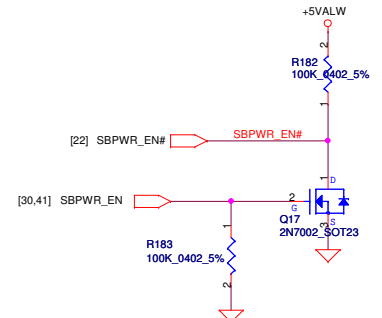
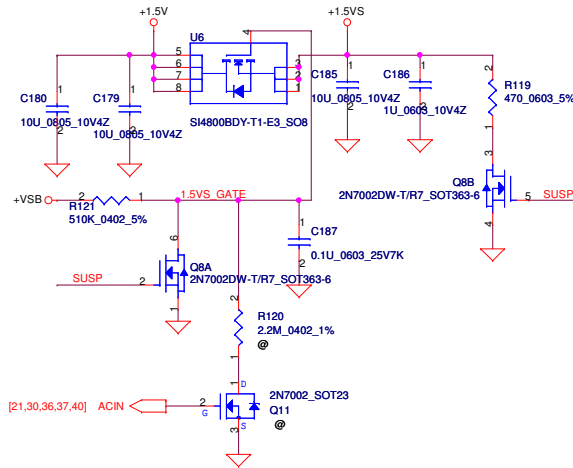
+3VALW TO +3VS



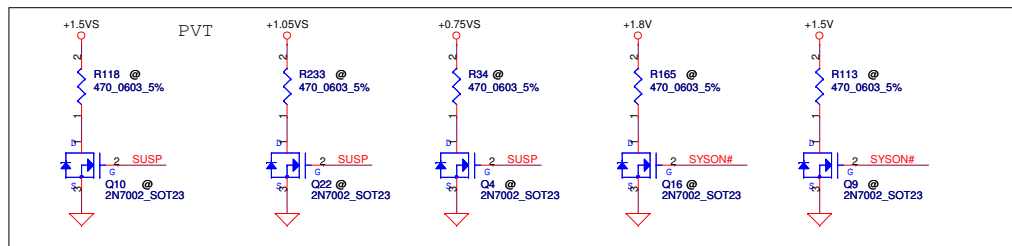
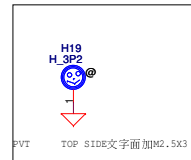
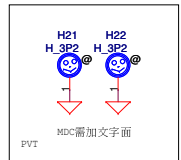
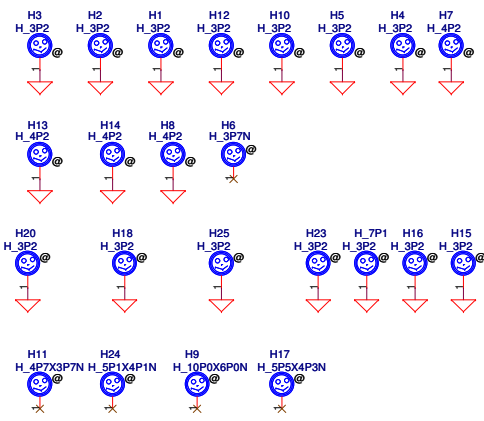
+3VALW TO +3V_SB(ICH8M AUX Power)



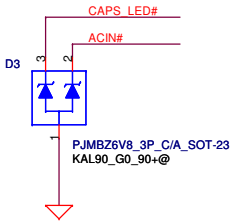
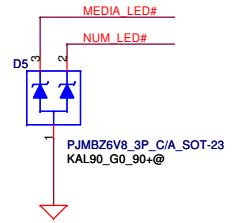
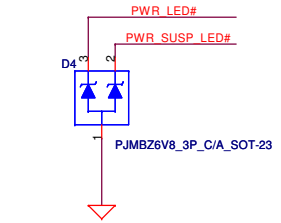
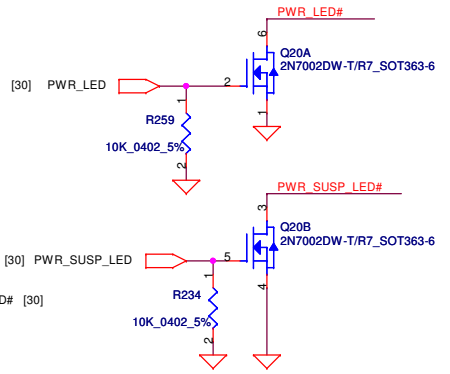
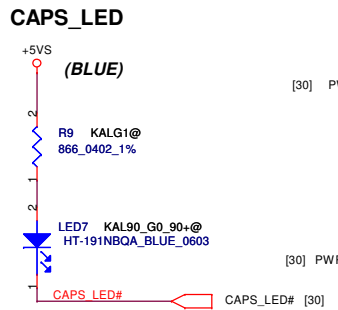
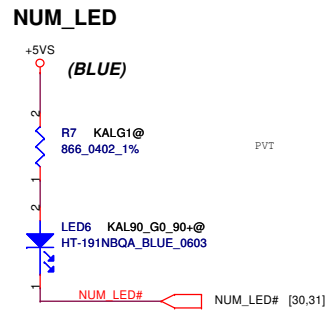
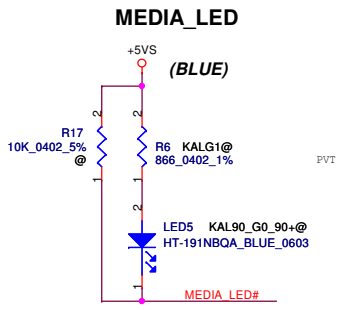
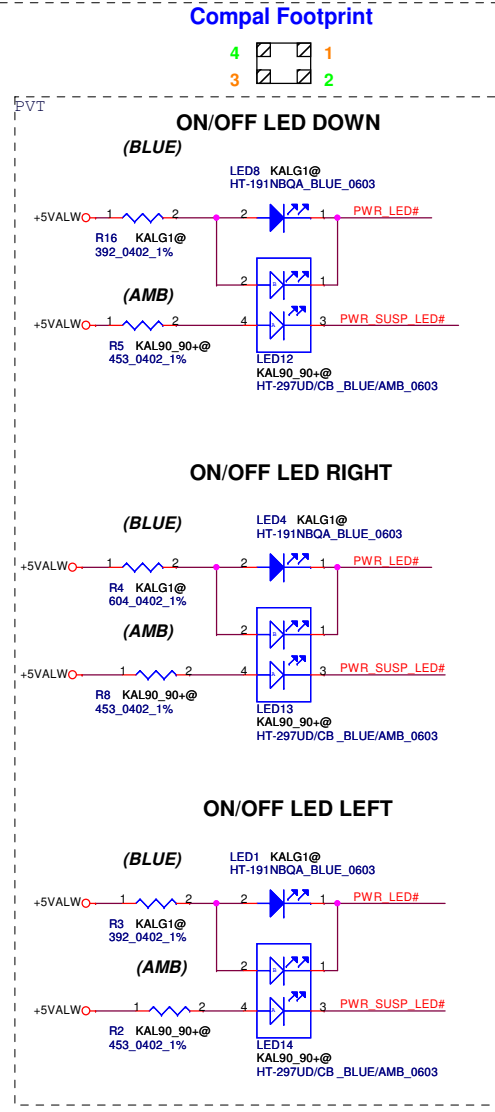
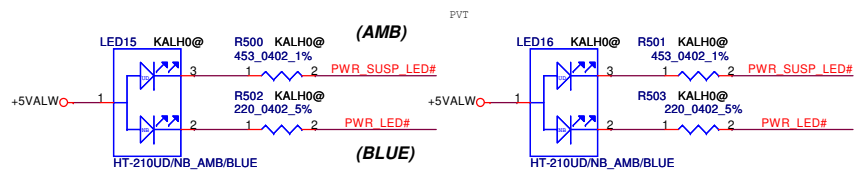
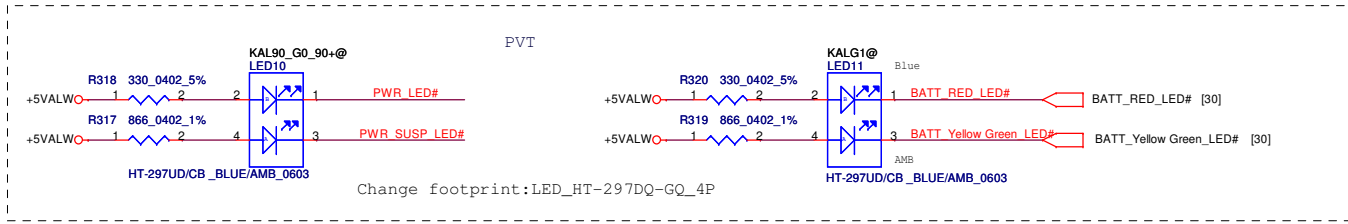
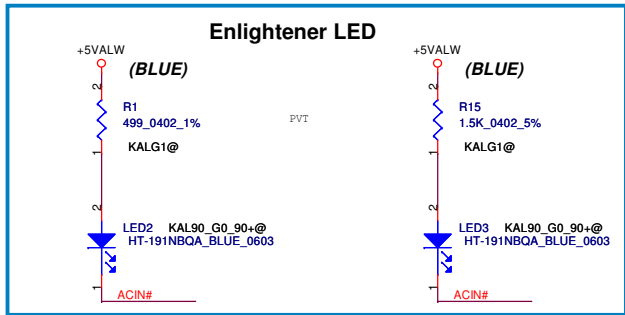
+1.5V to +1.5VS



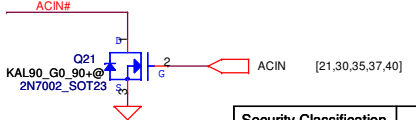
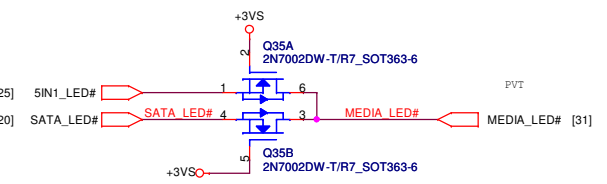
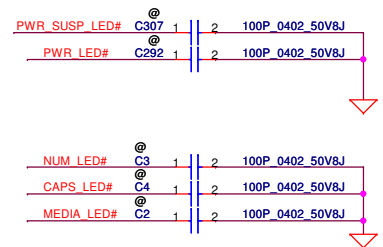
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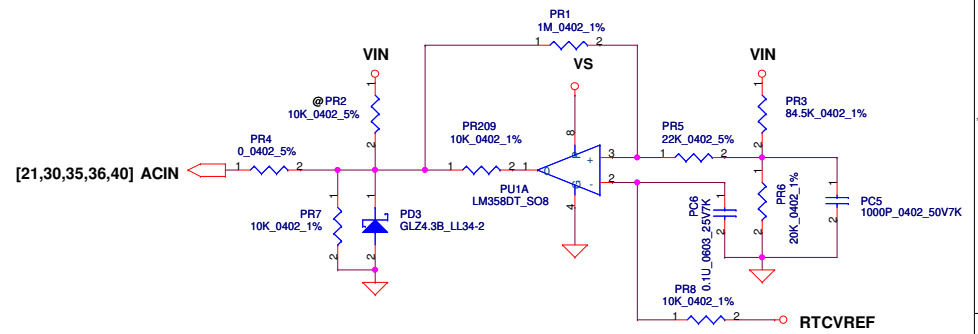
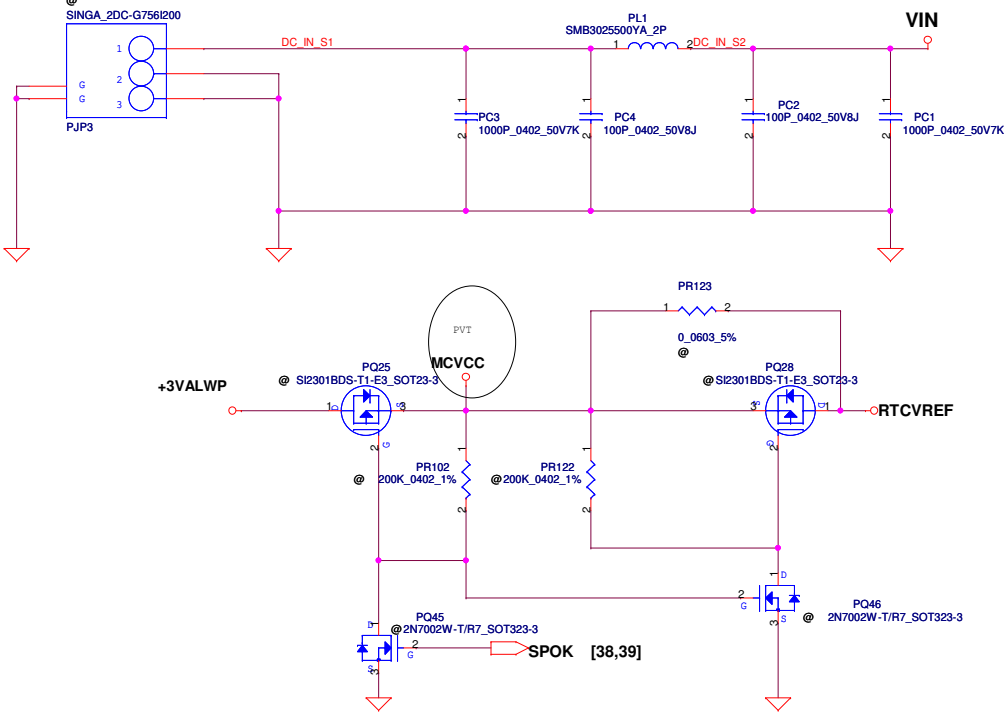


FOR EMI



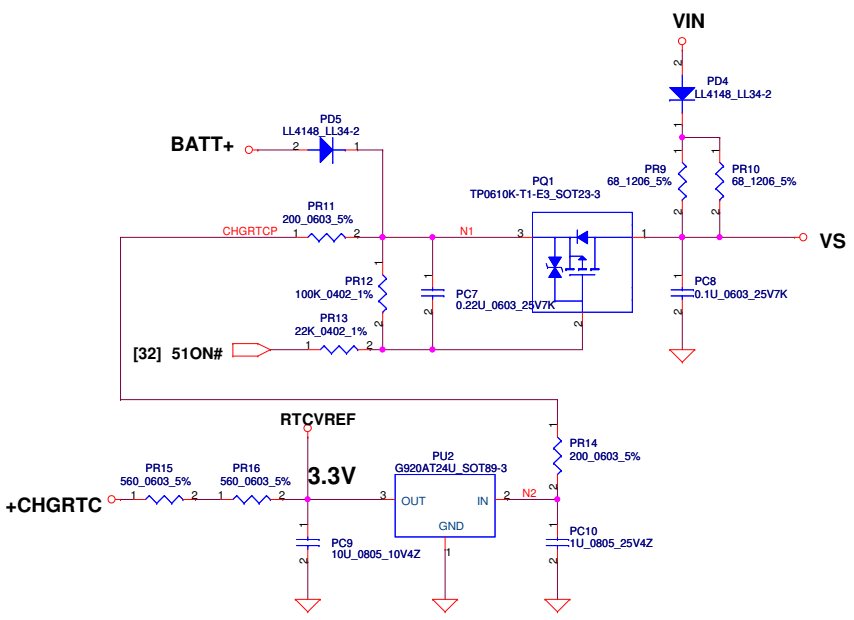
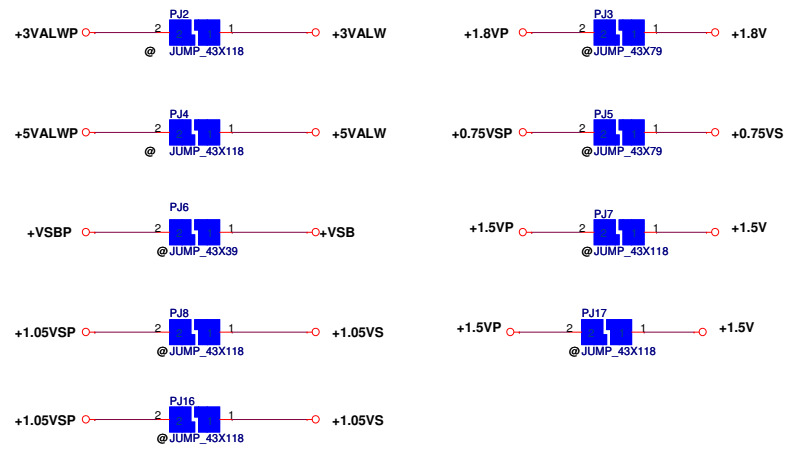
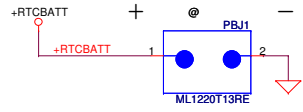
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Issued Date	2008/11/10	Deciphered Date	2008/11/24	Title	
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Size	Document Number			Rev	0.1
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			Sheet	36	of 45

DC231000500

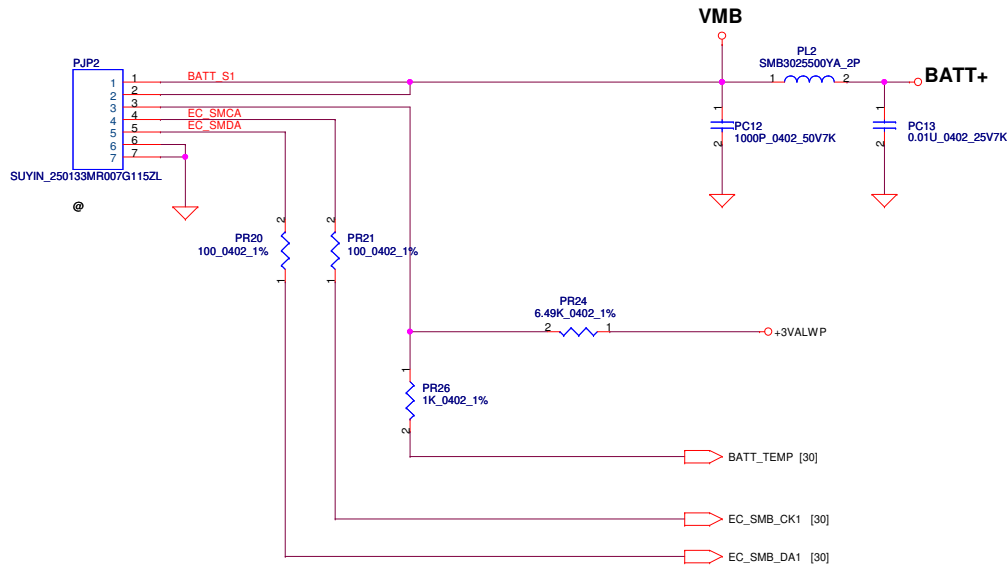


Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

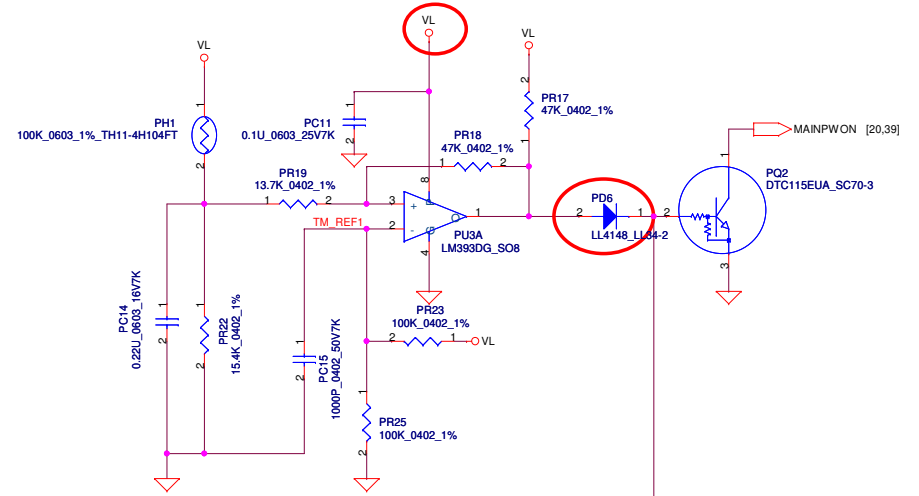
RTC Conn



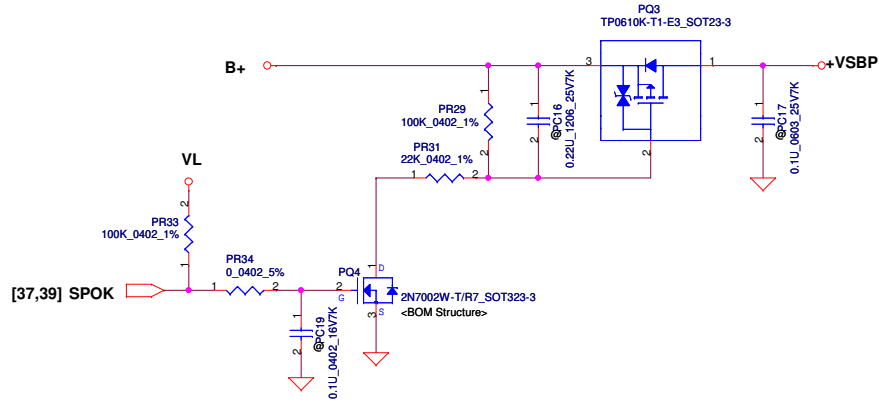
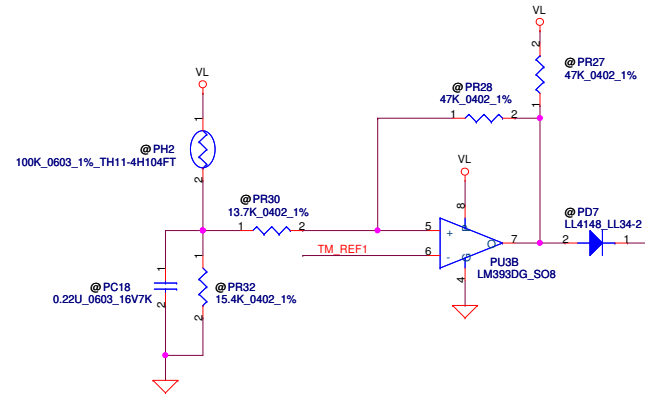
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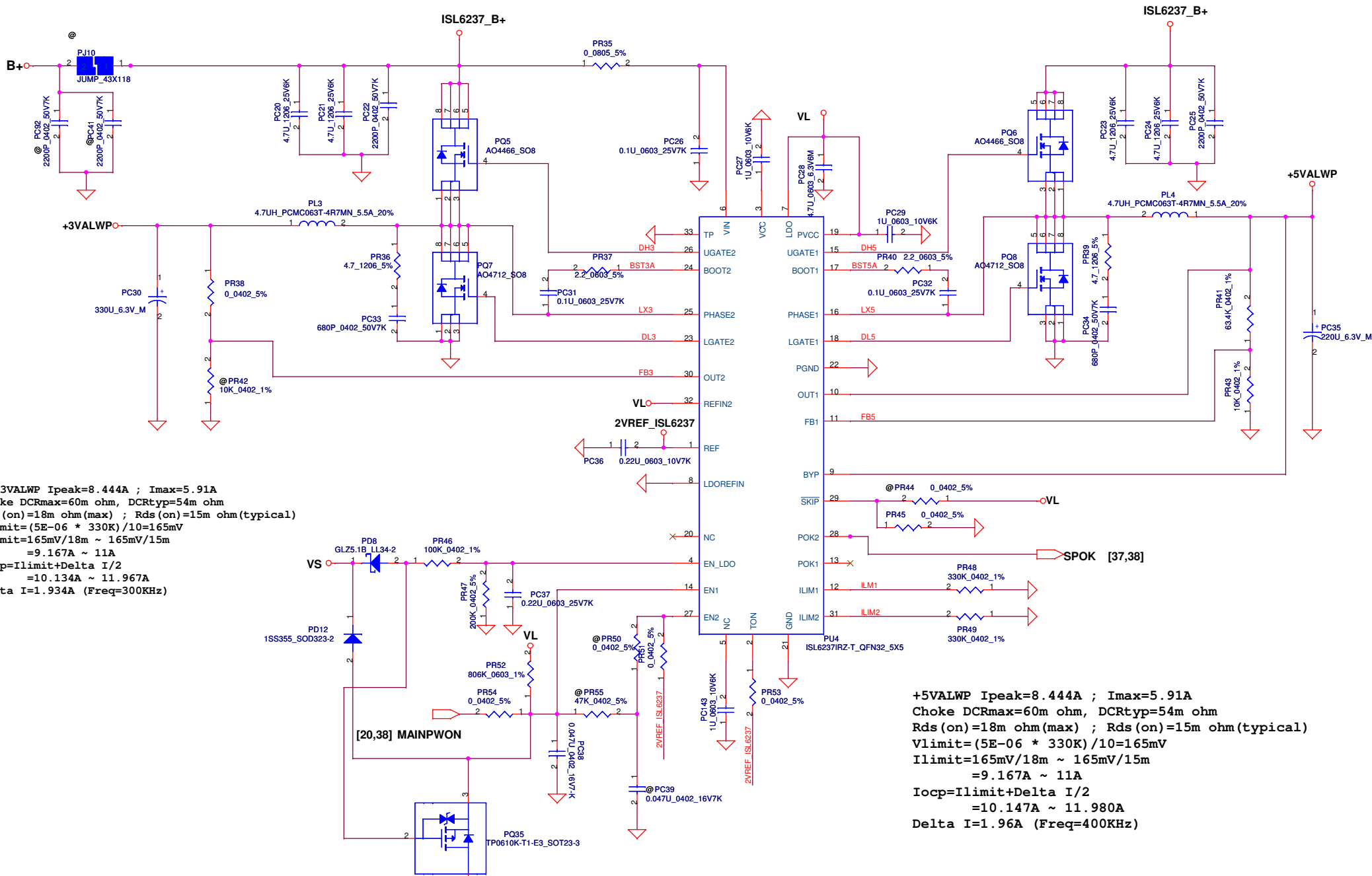
PH1 under CPU botten side :
 CPU thermal protection at 96 degree C
 Recovery at 60 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 47 degree C



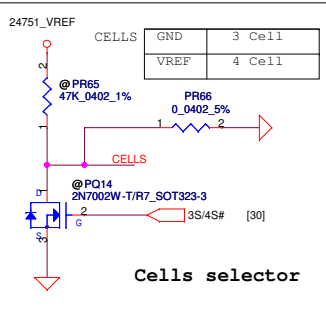
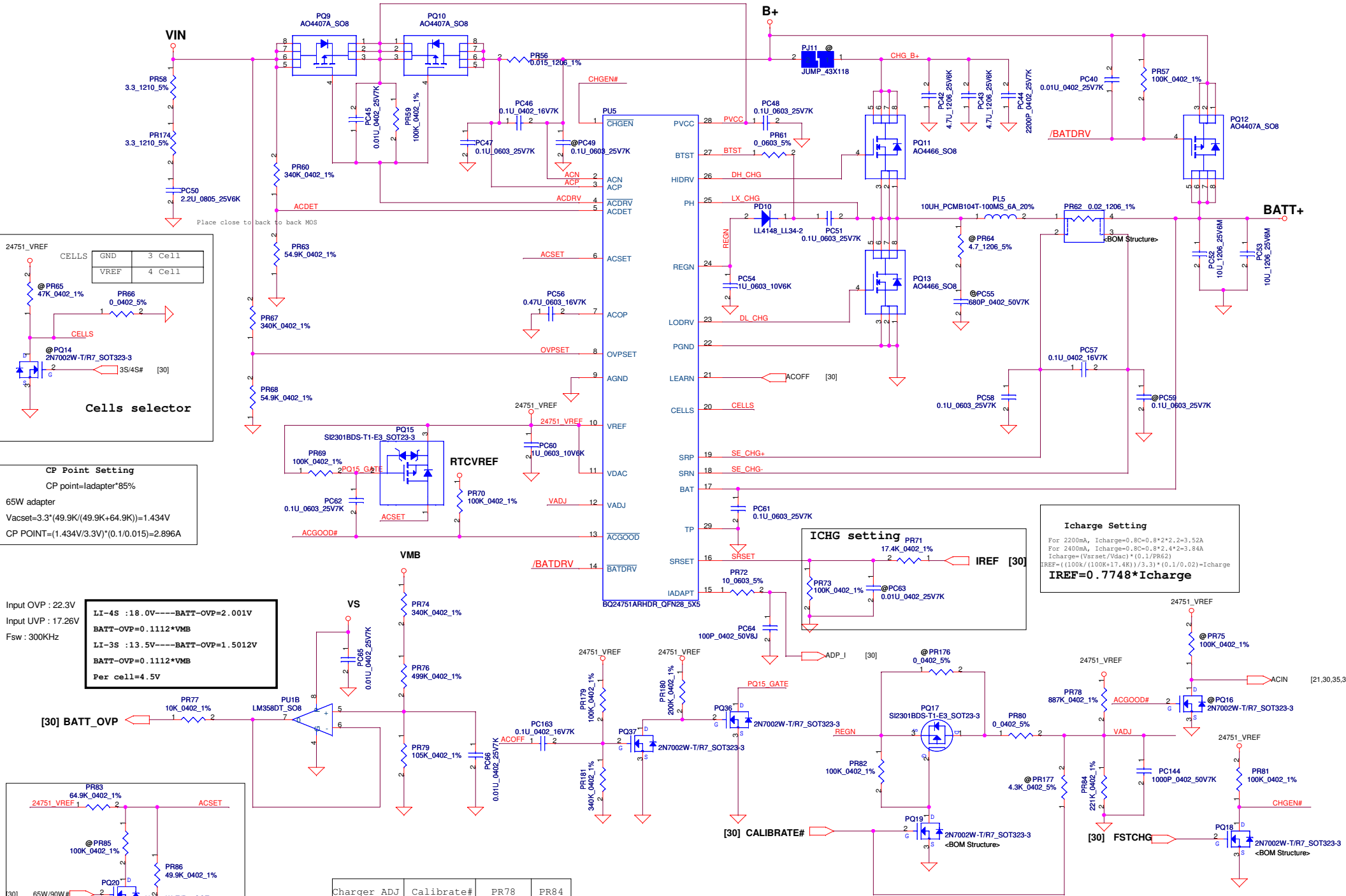
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+3.3VALWP Ipeak=8.444A ; Imax=5.91A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.134A ~ 11.967A
 Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.147A ~ 11.980A
 Delta I=1.96A (Freq=400KHz)

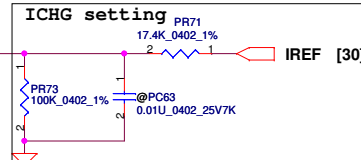
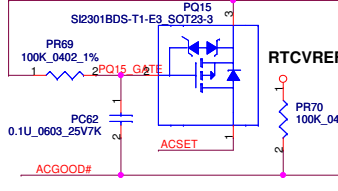
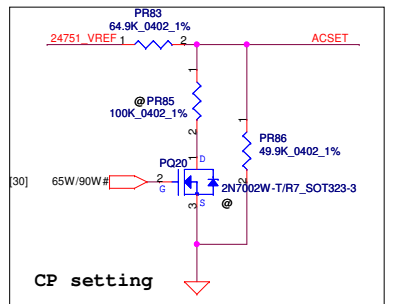
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CP Point Setting
 CP point=ladapter*85%
 65W adapter
 $V_{acset} = 3.3 \cdot (49.9K / (49.9K + 64.9K)) = 1.434V$
 $CP\ POINT = (1.434V / 3.3V) \cdot (0.1 / 0.015) = 2.896A$

Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz

LI-4S : 18.0V ---- BATT-OVP = 2.001V
 BATT-OVP = 0.1112 * VMB
 LI-3S : 13.5V ---- BATT-OVP = 1.5012V
 BATT-OVP = 0.1112 * VMB
 Per cell = 4.5V

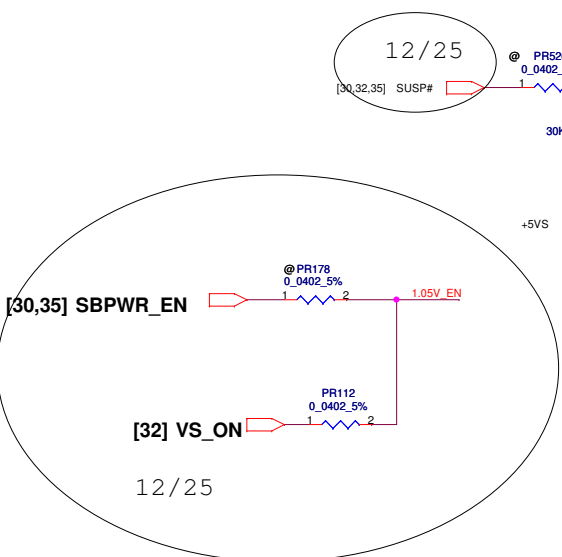


Icharge Setting
 For 2200mA, $I_{charge} = 0.8 \cdot 0.8 \cdot 2 \cdot 2 = 3.52A$
 For 2400mA, $I_{charge} = 0.8 \cdot 0.8 \cdot 2 \cdot 2 = 3.84A$
 $I_{charge} = (V_{acset} / V_{dac}) \cdot (0.1 / PR62)$
 $IREF = ((100K / (100K + 17.4K)) / 3.3) \cdot (0.1 / 0.02) = I_{charge}$
IREF = 0.7748 * Icharge

Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V	H	@	@

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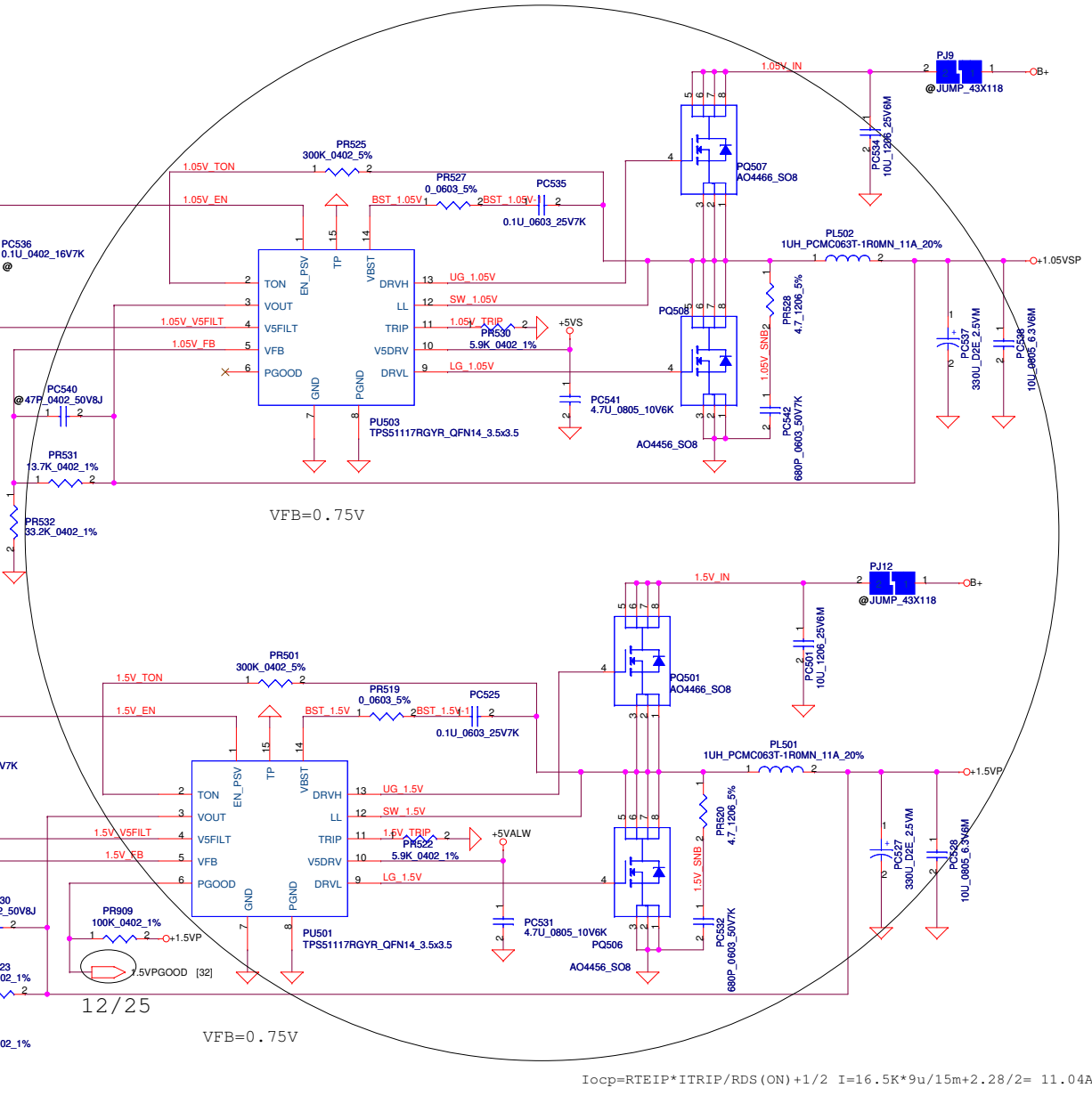
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CHARGER
 Title
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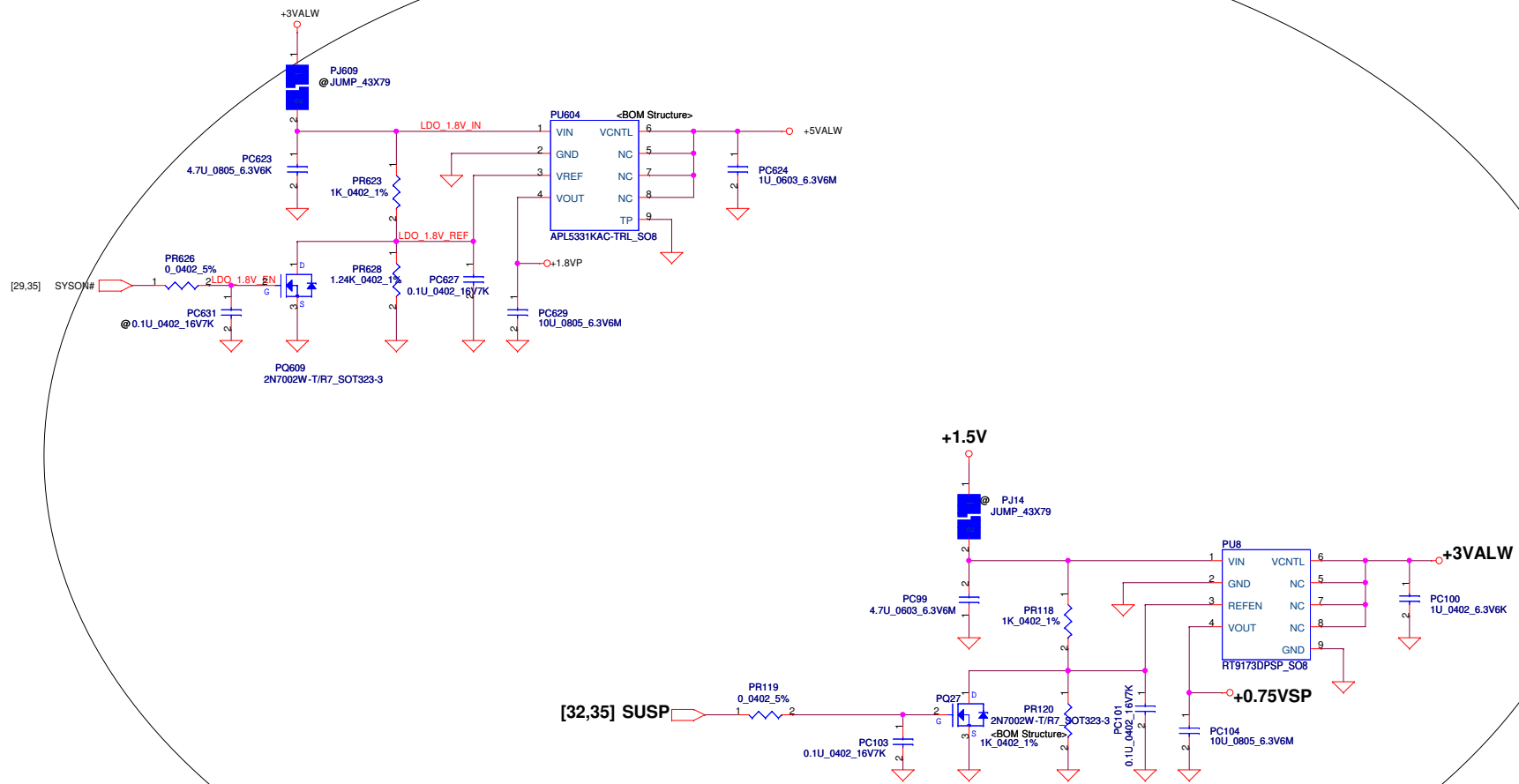
12/25

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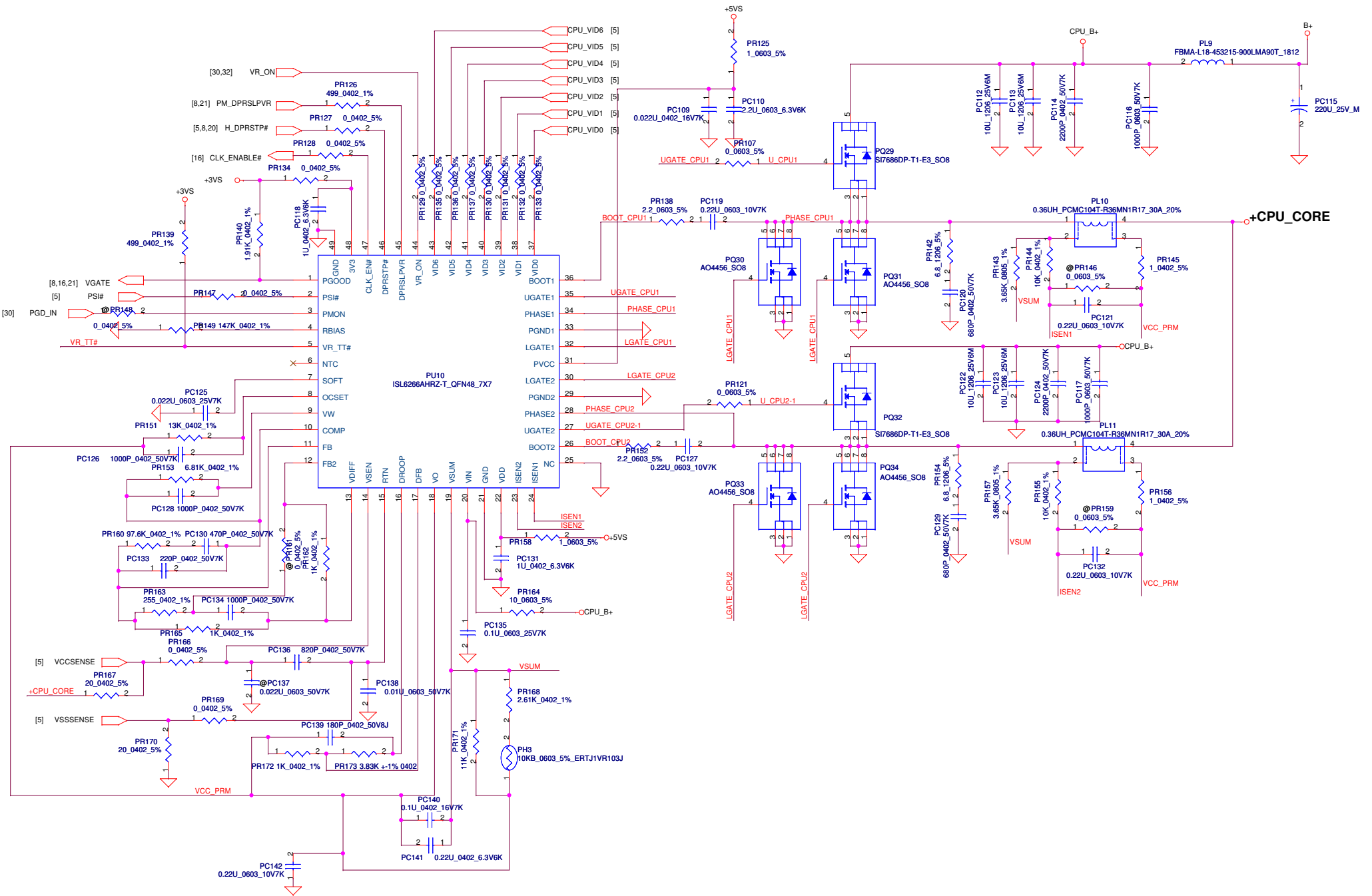


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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Add 3/5V boost resister for EMI request			Change PR37 and PR40 to 2.2 OHM		
2		Modify 1.5V and 1.05V choke to cyntec for eff.			PL501 & PL502		
3		Modify 1.5V and 1.05V frequence from 336K to 264K for eff.			Change PR525 & PR501 from 240K to 300K		
4		Modify 1.5V and 1.05V low side mos for eff.			Change PQ506 & PQ508 from FDS6670 to A04456		
5		Add CPU_core boost resister for EMI request			Change PR138 and PR158 to 2.2 OHM		
6		Modify 1.5V & 1.05V OCP to 14A			Change PR530 & PR522 to 5.9K		
7		Modify 3V & 5V choke to 4.7UH for eff.			Change PL3 & PL4 from 8.2UH to 4.7UH		
8		Modify 5V output cap to OS-CON for costdown			Change PC35		
9		Modify 3V output cap to OS-CON for costdown			Change PC30		
10		Modify dischager mos to AO4407A for rating risk			Change PQ12		
11		Add 30K OHM to TPS51117 EN pin , Disable SMPS mode			ADD PR910 & PR911		
12							
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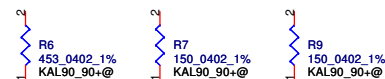
PCB

ZZZ
 LA-5271P MB Rev0: DA60000C500
 PCB 08Y LA-5271P REV0 M/B

North Bridge

U21 PVT
 GL40
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 S IC AC82GL40 SLGGM A1 FCBGA1329 GL ABO
 GL40@

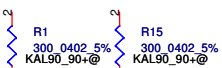
MEDIA_LED NUM_LED CAPS_LED



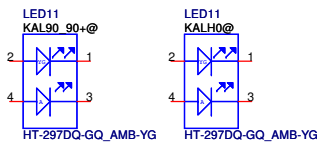
ON/OFF LED Risiter



Enlightener LED



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